LM6511 180 ns 3V Comparator

Check for Samples: LM6511

FEATURES

- **(Typical Unless Otherwise Noted)**
- **Operates at +2.7V, +3V, +3.3V, +5V**
- **Low Power Consumption <9.45 mW @ V^+ = 2.7V (max)**
- **Fast Response Time of 180 ns**

APPLICATIONS

- **Portable Equipment**
- **Cellular Phones**
- **Digital Level Shifting**

DESCRIPTION

The LM6511 voltage comparator is ideal for analog-digital interface circuitry when only a +3V or +3.3V supply is available. The open-collector output permits signal compatibility with a wide variety of digital families: +5V CMOS, +3V CMOS, TTL and so on. Supply voltage may range from 2.7V to 36V between supply voltage leads. The LM6511 operates with little power consumption (P_{diss} < 9.45 mW at V^+ = +2.7V and V^- = 0V).

This voltage comparator offers many features that are available in traditional sub-microsecond comparators: output sync strobe, inputs and output may be isolated from system ground, and wire-ORing. Also, the LM6511 uses the industry-standard, single comparator pinout configuration.

Connection Diagram

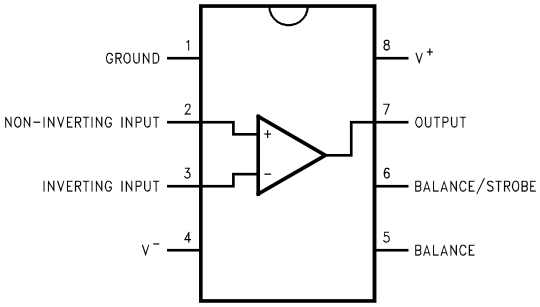


Figure 1. 8-Pin SOIC
See Package Number D

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage		−0.3 to +36V
Output to Negative Supply Voltage		50V
Ground to Negative Supply Voltage		30V
Differential Input Voltage		±30V
Input Voltage		See[1]
Storage Temperature Range		−65°C to +150°C
Soldering Information:	SOIC Package (Vapor Phase in 60 sec)	215°C
	SOIC Package (Infrared in 15 sec)	220°C
Power Dissipation		500 mW
Output Short Circuit Duration		10s
Junction Temperature		150°C
ESD Rating (C = +100 pF, R = 1.5 kΩ)		300V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Operating Ratings[1]

Supply Voltage		2.5V to 30V
Temperature Range		$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	SOIC Package	170°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 2.7V, V^- = 0V, 50Ω ≤ R_L ≤ 50kΩ, and I_L = 1.0 mA unless otherwise specified

Symbol	Parameter	Conditions	Typical	LM6511I	Units (Limits)
				Limit	
V_{OS}	Offset Voltage	$R_S \le 50$ kΩ[1]	1.5	5 **8**	mV max
I_B	Input Bias Current		38	130 **200**	nA max
I_{OS}	Input Offset Current	$R_S \le 50$ kΩ[1]	1.5	20 **50**	nA max
I_S	Positive Supply Current		2.7	3.5 **5**	mA max
	Negative Supply Current		1.5	2.0 **2.5**	
V_{SAT}	Saturation Voltage	$V_{IN} \le 10$ mV I_{SINK} = 8 mA	0.23	0.4 **0.4**	V max
A_V	Large Signal Voltage Gain	ΔV_{OUT} = 2V	40		V/mV
CMRR	Common Mode Rejection Ratio		72		dB
I_{STROBE}	Strobe ON Current	See[2]	2.0	5.0	mA max

(1) The offset voltage and offset current limits are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Therefore, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.
(2) This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 mA to 5 mA.

DC Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 2.7V, V^- = 0V, 50Ω ≤ R_L ≤ 50kΩ, and I_L = 1.0 mA unless otherwise specified

Symbol	Parameter	Conditions	Typical	LM6511I	Units (Limits)
				Limit	
V_{IN}	Input Voltage Range			0.50	V min
				V^+ − 1.25	V max
	Output Leakage Current	V_{IN} ≥ 10 mV, V_{OUT} = 35V, I_{STROBE} = 3 mA	0.2		nA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 2.7V, V^- = 0V, 50Ω ≤ R_L ≤ 50kΩ, and I_L = 1.0 mA unless otherwise specified

Symbol	Parameter	Conditions	Typical	LM6511I	Units (Limits)
				Limit	
T_R	Response Time	See (1)	180		ns

(1) This specification is for a 100 mV input step with a 25 mV overdrive.

LM6511 Typical Performance Characteristics

V_S = 3V unless otherwise noted

Input Bias Current

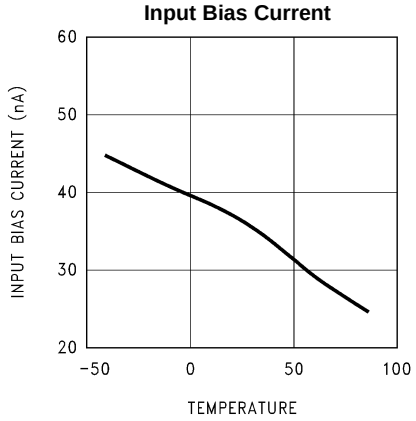


Figure 2.

Input Offset Current

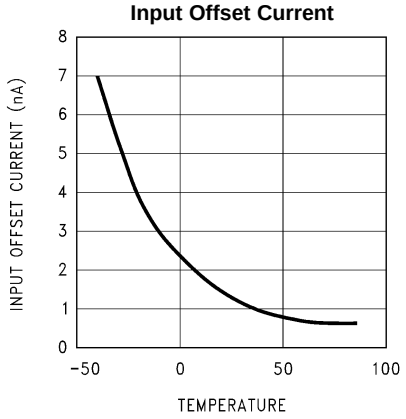


Figure 3.

Input Current vs. Input Voltage

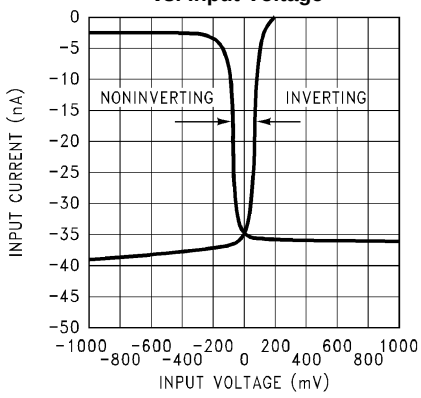


Figure 4.

Common Mode Limits

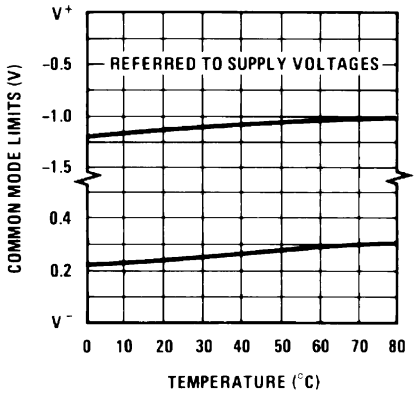


Figure 5.

Transfer Function

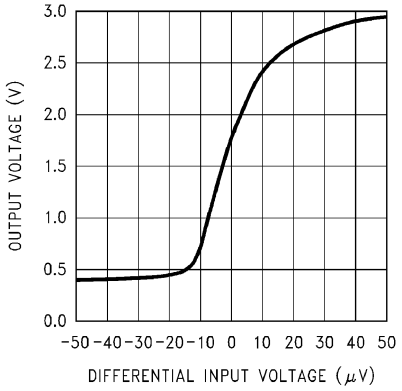


Figure 6.

Output Saturation Voltage

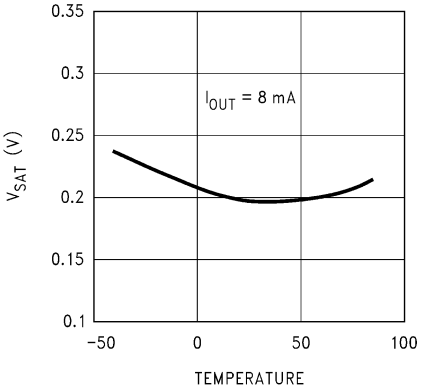


Figure 7.

LM6511 Typical Performance Characteristics (continued)

V_S = 3V unless otherwise noted

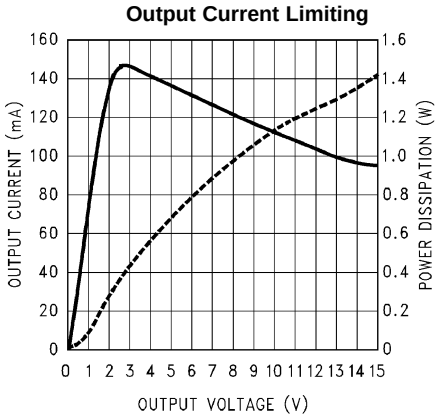


Figure 8.

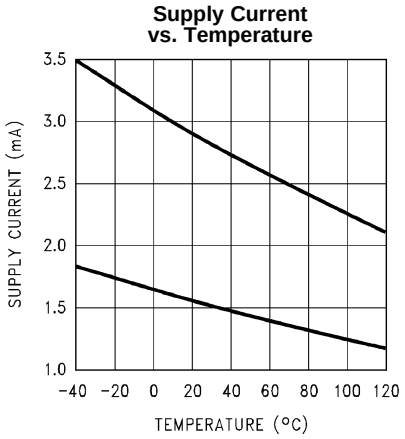


Figure 9.

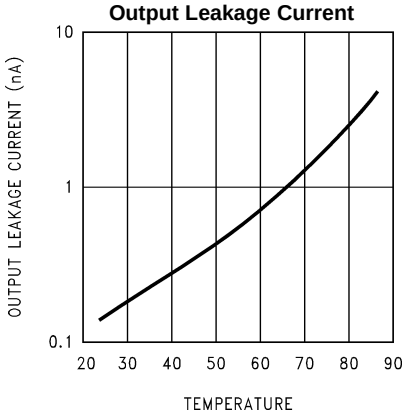


Figure 10.

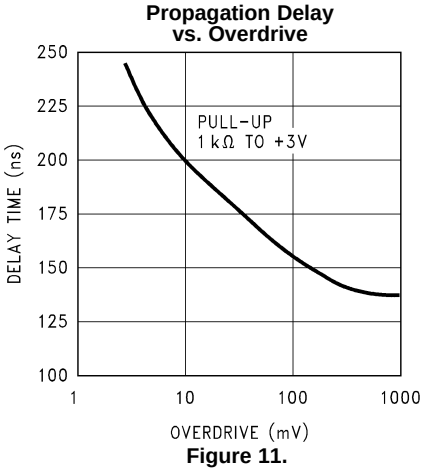
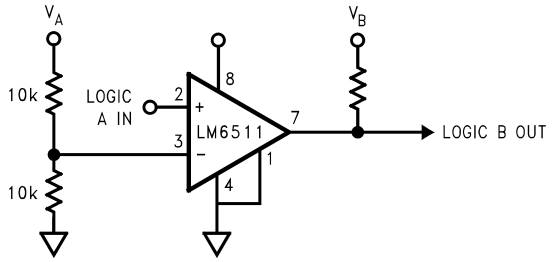


Figure 11.

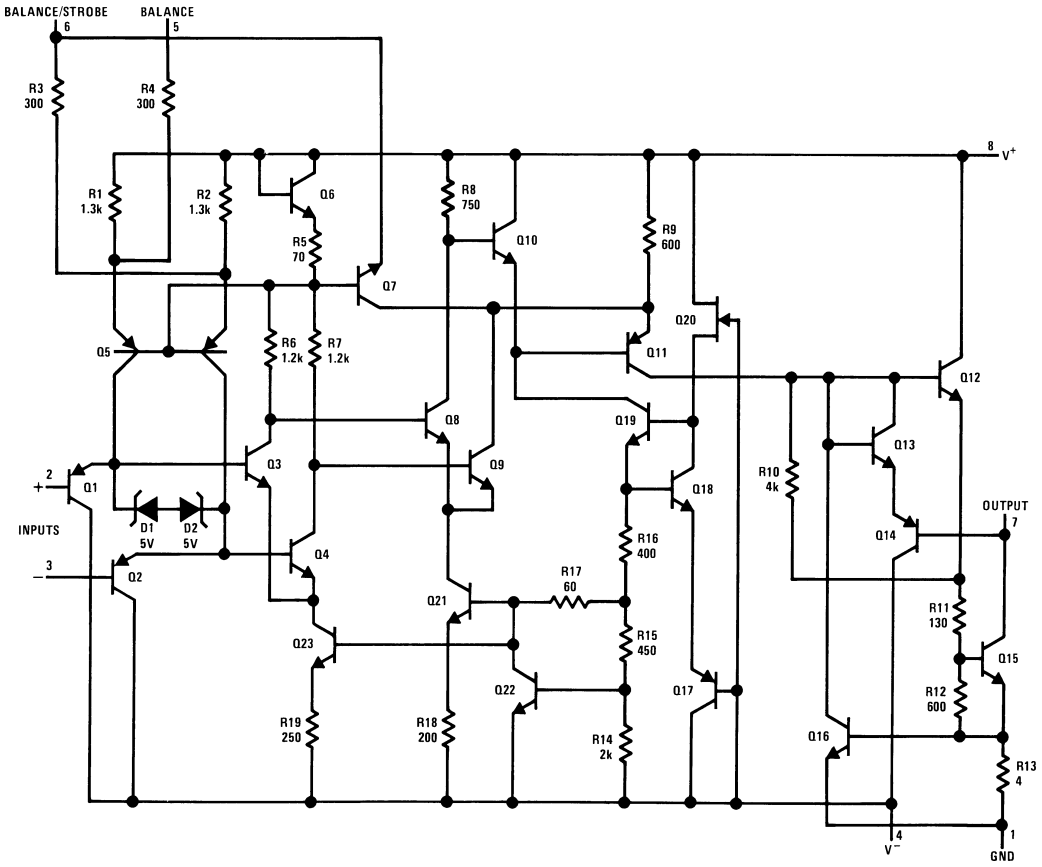
Typical Application



Notes: Because of the very wide operating and output voltage range, the LM6511 may be used to shift logic levels from 3V to TTL or CMOS to the other way around. By biasing the input to ½ of the input logic supply (V_A), this assures that this input remains within the input voltage range. The pull-up resistor should go to the output logic supply (V_B).

Figure 12. Universal Logic Level Shifter

Schematic Diagram



REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	6

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM6511IM	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	LM65 11IM
LM6511IM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM65 11IM
LM6511IM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM65 11IM
LM6511IMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM65 11IM
LM6511IMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM65 11IM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

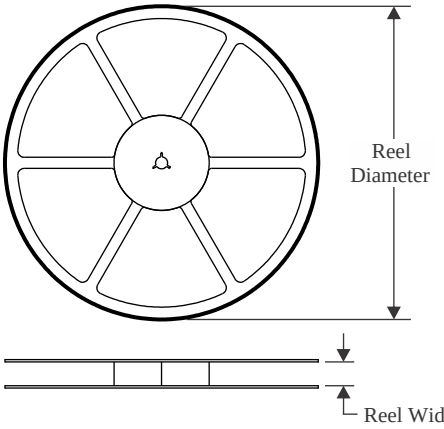
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

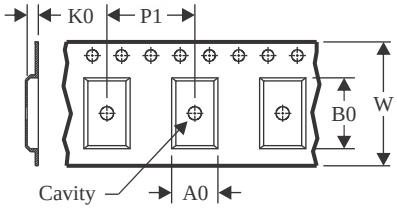
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

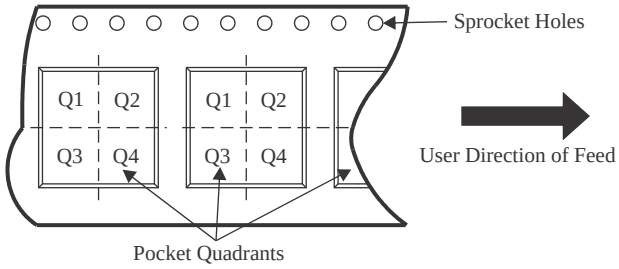


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

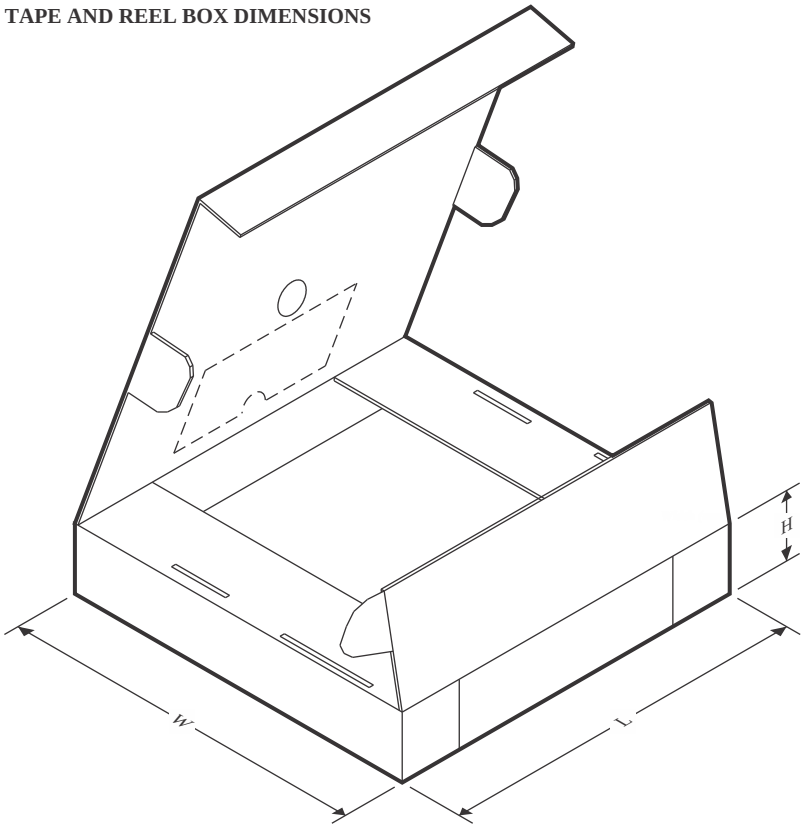
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6511IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

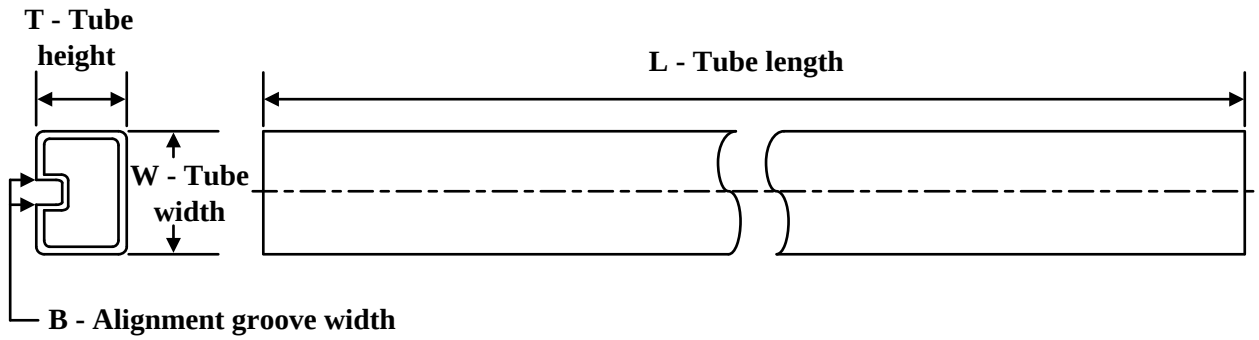
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

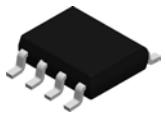
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6511IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM6511IM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM6511IM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05

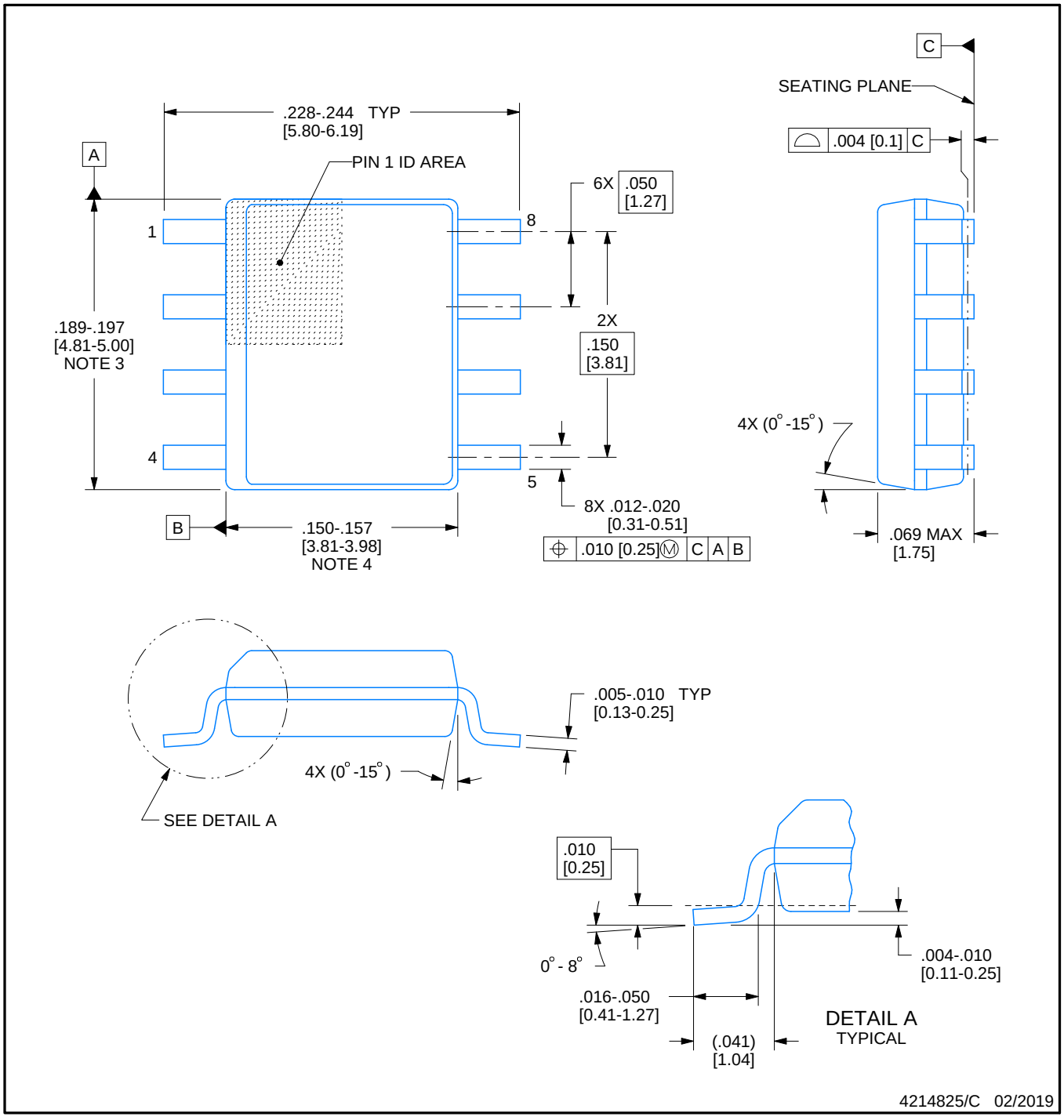


PACKAGE OUTLINE

D0008A

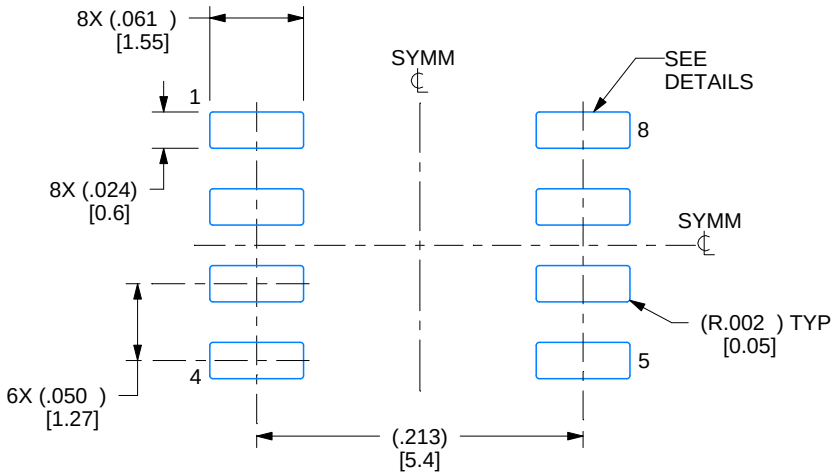
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

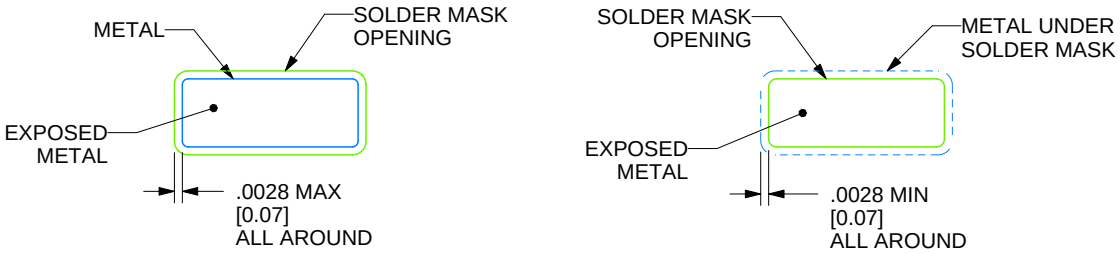


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

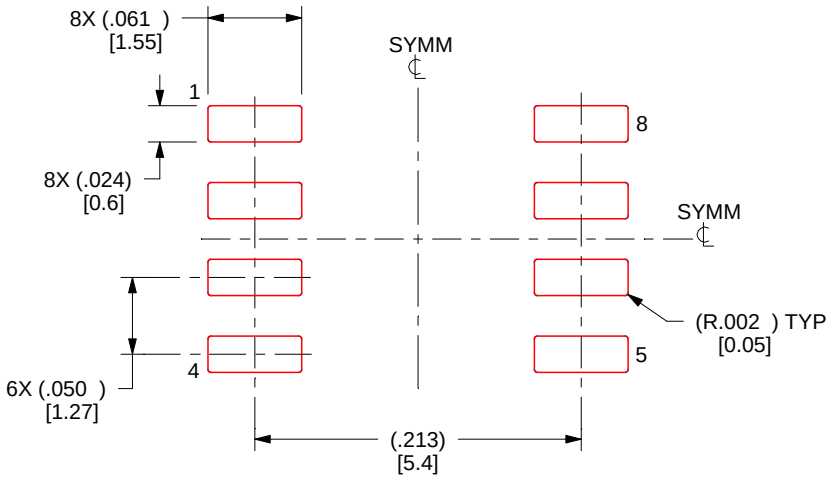
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265