LM644A2-Q1 3V～36V、低 I_Q、デュアル 6A、車載用、マルチフェーズ スタッカブル、降圧コンバータ、両面冷却対応熱特性強化型パッケージ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 1:–40℃～+125℃の動作時周囲温度
  - 最大 150℃の接合部温度で動作
  - 熱特性強化型パッケージは上面と底面に露出サーマル パッドを備え、両面冷却が可能
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 低 EMI 設計
  - グランドとのクリアランスが 1mm を超える対称入力電圧ピン
  - ピン選択可能なスペクトラム拡散オプション
  - ピン選択可能な FPWM または自動モード動作
  - ウェッタブル フランク付き拡張 HotRod™ QFN (25) パッケージ
  - スイッチング周波数:100kHz～2.2MHz
  - CISPR 25 Class 5 EMI 要件に準拠
- シングルとデュアルの出力機能
  - 広い入力電圧範囲:3V～36V
  - 精度 1% の固定 3.3V、5V 出力または可変出力 (0.8V～20V)
  - ヒステリシス付きのヒカップ モード過電流保護およびサーマル シャットダウン保護機能
  - 高精度 ENABLE および PGOOD 機能
  - 50ns の $t_{ON(min)}$ により高い V_{IN}/V_{OUT} 比を実現
  - 80ns の $t_{OFF(min)}$ により低ドロップアウトを実現
- 多用途なデュアル出力動作
  - シャットダウン モード電流:0.5µA (代表値)
  - 無負荷時のスタンバイ電流:9µA (代表値)
  - 内蔵補償と 3ms ソフト スタート
  - 独立した高精度 ENABLE および PGOOD
- 適応可能な単一出力動作
  - 8A 負荷、単一出力、V_{IN} = 12V、V_{OUT} = 5V で 95% を超える効率
  - 外部補償と可変ソフト スタート
  - PGOOD、SYNCIN、SYNCOUT の機能
- LMQ644A2-Q1 とピン互換

2 アプリケーション

- 車載コックピットとディスプレイ
- 車載用 ADAS と集中型コンピューティング
- ボディ エレクトロニクスおよび照明
- 汎用デュアル降圧コンバータ

3 概要

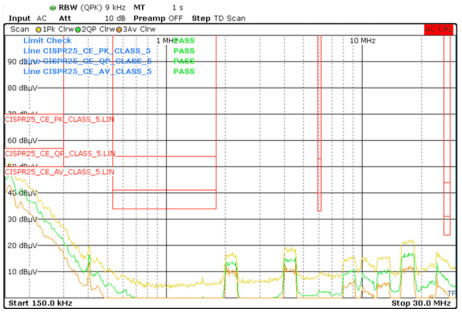
LM644A2-Q1 は、大電流の単一出力またはデュアル出力に対応する 36V 同期整流降圧 DC/DC コンバータです。このデバイスは、インターリーブされたスタック可能な電流モード制御アーキテクチャを使用しているので、ループ補償が簡単であり、過渡応答が高速で、優れた負荷および ライン レギュレーションが可能です。出力クロックによって正確な電流共有を行い、最大 36A の電流について最大 6 相をサポートできます。最小オン時間 50ns のハイサイド スイッチは、大きい降圧率に対応でき、12V、24V または 車載用入力から低電圧レールへの直接変換が可能になり、システムの複雑度と設計コストを下げることができます。

LM644A2-Q1 は、ウェッタブル フランク付きの最適化された拡張 HotRod QFN パッケージに拡散スペクトラムを搭載し、EMI を最小限に抑えるために低インダクタンスの入力バイパス構成を採用しています。デュアル ランダム拡散スペクトラム (DRSS) 周波数ホッピングは ±10% (標準値) に設定されており、三角波と疑似ランダム変調の組み合わせにより、放射を大幅に低減します。BIAS ピンを使用すると、LM644A2-Q1 はコンバータの出力からデバイスに電力を供給することで損失を節約でき、無負荷時の静止電流は 9µA となり、バッテリ駆動システムの動作時間を延長できます。LM644A2-Q1 は、複数のデバイスをスタックする場合でも、軽負荷動作時に高効率を維持し、負荷範囲全体にわたって高効率を実現できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
LM644A2-Q1	VBG (WQFN-FCRLF、24)	5mm × 4mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



CISPR 25 伝導、V_{OUT} = 3.3V、2.1MHz、12A

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4 Device Comparison Table

DEVICE	ORDERABLE PART NUMBER	RATED OUTPUT CURRENT	PACKAGE	JUNCTION TEMPERATURE RANGE
LM644A2-Q1	LM644A2QVBGRQ1	Dual 6A/6A, or stackable 12A	VBG (WQFN, 24)	–40°C to 150°C

5 Pin Configuration and Functions

VGB package, 24-pin VQFN-FCRLF with wettable flanks

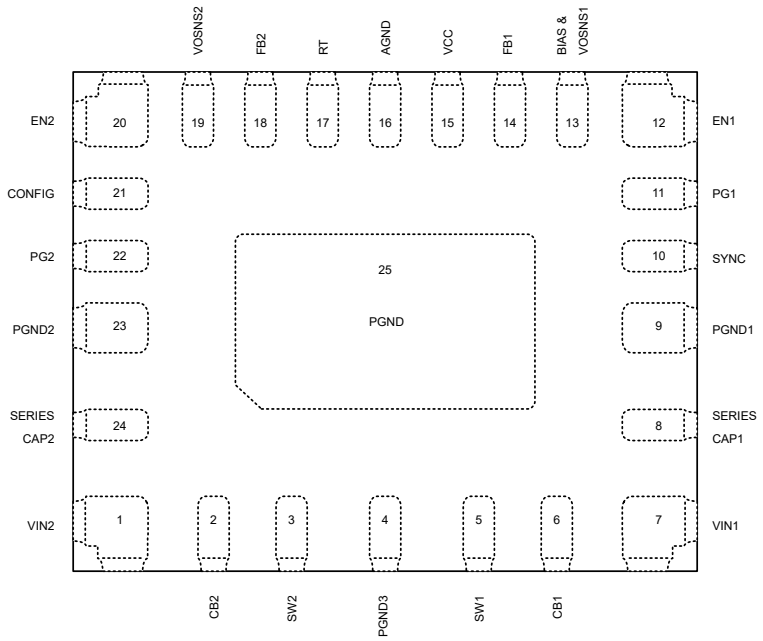


図 5-1. Dual Output (Top View)

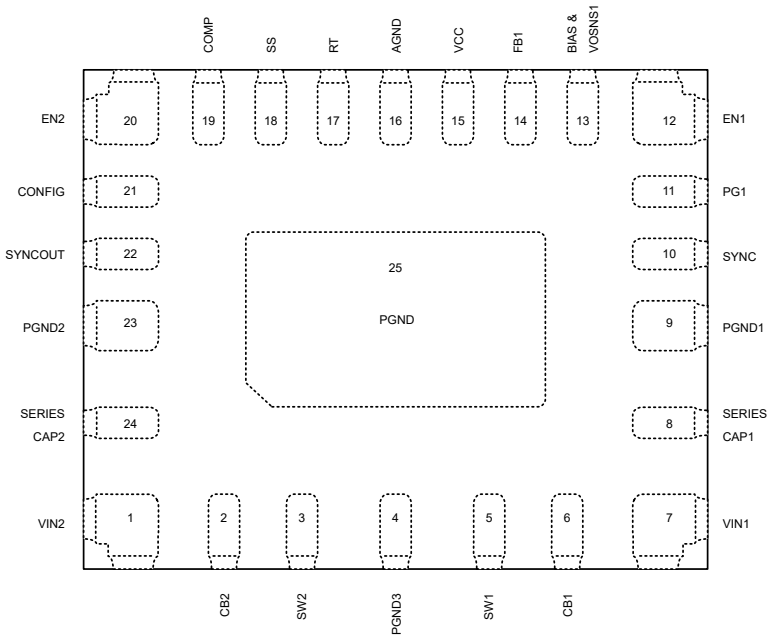


図 5-2. Single Output Primary (Top View)

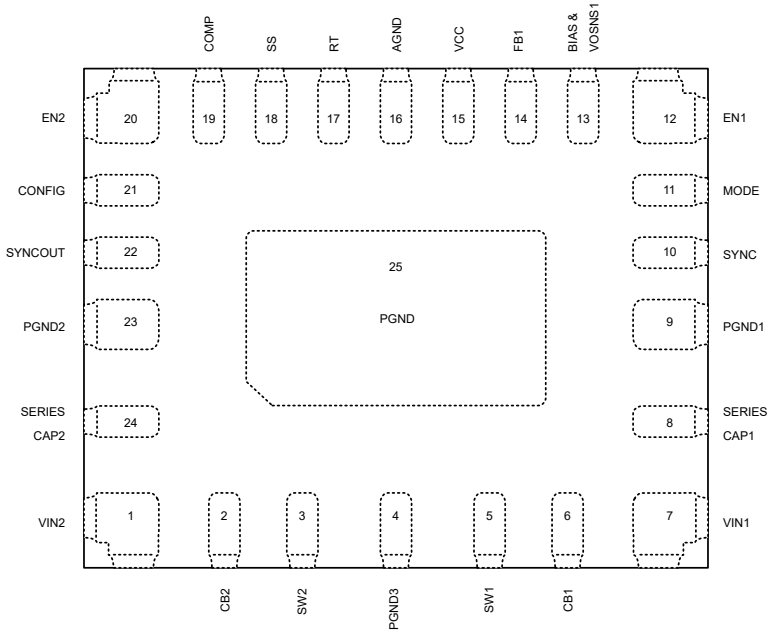


図 5-3. Single Output Secondary (Top View)

表 5-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NO.	NAME			
	DUAL OUTPUT	SINGLE OUTPUT		
1	VIN2	VIN2	I	Input supply to the regulator. Connect a high quality bypass capacitors from this pin to PGND2. Low impedance connection must be provided to VIN1.
2	BOOT2	BOOT2	I/O	Channel 2 high-side driver upper supply rail. Connect a 100nF capacitor between SW2 and BOOT2. An internal diode charges the capacitor while SW2 is low.
3	SW2	SW2	P	Channel 2 Switching node that is internally connected to the source of the high-side NMOS buck switch and the drain of the low-side NMOS synchronous rectifier. Connect to the switching node of the power inductor.
4	PGND3	PGND3	G	Power ground to internal low side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND1, PGND2 and exposed pad.
5	SW1	SW1	P	Channel 1 Switching node that is internally connected to the source of the high-side NMOS buck switch and the drain of the low-side NMOS synchronous rectifier. Connect to the switching node of the power inductor.
6	BOOT1	BOOT1	I/O	Channel 1 High-side driver upper supply rail. Connect a 100nF capacitor between SW1 and BOOT1. An internal diode charges the capacitor while SW1 is low.
7	VIN1	VIN1	I	Input supply to the regulator. Connect a high quality bypass capacitors from this pin to PGND1. Low impedance connection must be provided to VIN2.
8	SERIES CAP1	SERIES CAP1	NC	This pin is not internally connected. The pin is provided for pin compatibility with LMQ644xx series where this pin is connected to mid-point of two series capacitors between pins VIN1 and PGND1. This pin can be left floating, or can be connected to the mid-point of additional bypass capacitors in series configuration if required for the end application.
9	PGND1	PGND1	G	Power ground to internal low side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND2 and PGND3. Connect a high quality bypass capacitors from this pin to VIN1.

表 5-1. Pin Functions (続き)

PIN			TYPE[1]	DESCRIPTION
NO.	NAME			
	DUAL OUTPUT	SINGLE OUTPUT		
10	SYNC	SYNC	I	Multi-function pin. SYNC selects forced pulse width modulation (FPWM) or Diode Emulation mode. Connect SYNC to AGND to enable diode emulation mode. Connect SYNC to VCC to operate the LM644A2-Q1 in FPWM mode with continuous conduction at light loads. SYNC can also be used as a synchronization input to synchronize the internal oscillator to an external clock. When used as a secondary device in single output configuration, the SYNC pin is connected to SYNC_OUT of the primary for clock timing.
11	PG1	MODE	O	Dual function pin. An open drain output that transitions low if VOSNS1 is outside a specified regulation window in dual output and single output primary configuration. In single output secondary mode configuration, this behaves as a mode pin to select between forced PWM (FPWM) mode and Diode Emulation Mode (DEM). Connect MODE of single output secondary to SYNC pin of single output primary to place them in the same mode of operation. For FPWM, connect MODE to VCC through a 10 kOhm resistor. For DEM connect to ground.
12	EN1	EN1	I	An active high input LM644A2-Q1 (V_{OH} > 1.375V) enables Output 1 in dual output operation. When in single output operation, an active high input enables all phases in the system. When disabled, the LM644A2-Q1 is in shutdown mode. EN1 must never be floating.
13	BIAS and VOSNS1	BIAS and VOSNS1	I	Output voltage sense and input to internal voltage regulator. Connect to non-switching side of the inductor. Connect an optional high quality 0.1µF capacitor from this pin to AGND for best performance.
14	FB1	FB1	I	Feedback input to channel 1 of the LM644A2-Q1 in dual output operation and feedback input to all channels in single output operation. Connect FB1 to VCC through a 10 kOhm resistor for a 5V output or connect FB1 to AGND for a 3.3V output. A resistive divider from the non-switching side of the inductor to FB1 sets the output voltage level between 0.8V and 20V. The regulation threshold at FB1 is 0.8V. For lower output voltages use at least a 10kOhm for the top of the resistor divider.
15	VCC	VCC	O	Internal regulator output. Used as supply to internal control circuits. Do not connect to any external loads. Connect a high quality 1µF capacitor from this pin to AGND.
16	AGND	AGND	G	Analog ground connection. Ground return for the internal voltage reference and analog circuits.
17	RT	RT	I	Frequency programming pin. A resistor from RT to AGND sets the oscillator frequency between 100kHz and 2.2MHz.
18	FB2	SS	I	Dual function pin. When in dual output operation, the pin functions as FB2, feedback input to channel 2 of the LM644A2-Q1. Connect FB2 to VCC through a 10 kOhm resistor for a 5V output or connect FB2 to AGND for a 3.3V output. A resistive divider from the non-switching side of the inductor to FB2 sets the output voltage level between 0.8V and 20V. For lower output voltages use at least a 10kOhm for the top of the resistor divider. When in single output mode, the pin functions as SS. An external capacitor must be placed from SS to AGND for external soft-start of the output. Connect the SS pins of primary and secondaries for fault communication between devices.
19	VOSNS2	COMP	I	Dual function pin. In dual output operation, the pin functions as VOSNS2 for the fixed 3.3V and 5V and adjustable output conditions. In single output operation, the pin is the output of the internal error amplifier.
20	EN2	EN2	I	An active high input (V_{OH} > 1.375V) enables Output 2 in dual output operation. When in single output mode, EN2 of all LM644A2-Q1 must be connected together. An active high input enables all secondary phases in the system. When disabled, only one channel in the primary LM644A2-Q1 is active while all remaining phases are in shutdown mode. EN2 must never be floating.
21	CONFIG	CONFIG	I	Single or Dual output selection. Connect specific resistor values to the pin (refer to 表 7-3) to select number of phases, primary and secondary and dither options.
22	PG2	SYNC_OUT	O	Dual function pin. In dual output operation, this pin behaves as PG2, an open drain output that transitions low if VOSNS2 is outside a specified regulation window. In single output mode, the pin functions as SYNC_OUT and provides clock information from primary to secondary.

表 5-1. Pin Functions (続き)

PIN			TYPE(1)	DESCRIPTION
NO.	NAME			
	DUAL OUTPUT	SINGLE OUTPUT		
23	PGND2	PGND2	G	Power ground to internal low side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND1, PGND3 and PGND4. Connect a high quality bypass capacitors from this pin to VIN2.
24	SERIES CAP2	SERIES CAP2	NC	This pin is not internally connected. The pin is provided for pin compatibility with LMQ644xx series where this pin is connected to mid-point of two series capacitors between pins VIN1 and PGND1. This pin can be left floating, or can be connected to the mid-point of additional bypass capacitors in series configuration if required for the end application.
25	PGND4	PGND4	G	Power ground and heat sink connection. Solder directly to system ground plane. Low impedance connection must be provided to PGND1, PGND2 and PGND3.

(1) I = input, O = output, P = power, G = ground

5.1 Wettable Flanks

100% automated visual inspection (AVI) post-assembly is typically required to meet requirements for high reliability and robustness. Optimized QFN packages do not have solderable or exposed pins and terminals that are easily viewed. Visually determining whether or not the package is successfully soldered onto the printed-circuit board (PCB) is therefore difficult. The wettable-flank process was developed to resolve the issue of side-lead wetting of leadless packaging. The LM644A2-Q1 is assembled using a 24-pin, enhanced HotRod QFN package with wettable flanks to provide a visual indicator of solderability, which reduces the inspection time and manufacturing costs.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN1, VIN2 to PGND (transient)	–0.3	42	V
Pin voltage	SW1, SW2 to PGND (less than 10ns transient)	–6	42.3	V
Pin voltage	SW1, SW2 to PGND (transient)	–0.3	42.3	V
Pin voltage	BOOT1 - SW1, BOOT2 - SW2	–0.3	5.5	V
Pin voltage	EN1, EN2 to AGND	–0.3	42	V
Pin voltage	PG1, SYNC_OUT/PG2 to AGND	–0.3	20	V
Pin voltage	SYNC/MODE, FB1, FB2/SS, CONFIG to AGND	–0.3	5.5	V
Pin voltage	BIAS/VOSNS1, COMP/VOSNS2 to AGND	–0.3	22	V
Pin voltage	RT, VCC to AGND	–0.3	5.5	V
Pin voltage	PGND1/2/3 to AGND voltage differential	–1	2	V
Sink current	PG1, PG2		10	mA
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (VIN1, VIN2, EN1, and EN2)	±750	
			Other pins	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{VOSNS1/2}$	Output Voltage range		0.8		20	V
$V_{IN1/2}$	Input supply voltage range	VIN1, VIN2	3		36	V
F_{SW}	Frequency	Switching frequency range	100		2200	kHz
$I_{OUT1/2}$	Output current range	Each phase of LM644A2	0		6	A
T_J	Operating junction temperature		–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM644XX-Q1 VBG (WQFN-FCRLF) 24 PINs	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JESD 51-7)	34	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.36	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7	°C/W

(1) For more information about traditional and new thermal metrics, see the spra953 application note

6.5 Electrical Characteristics

T_J = –40°C to +150°C. Typical values are at T_J = 25°C and V_{IN} = 13.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN-DT3p3)}$	VIN quiescent current, dual output mode, BIAS = 3.3V	Non-switching, V_{EN} = 2V, V_{BIAS} = V_{VOSNS1} = 3.3V + 10%, V_{VOSNS2} = 5V + 10%		7	30	µA
$I_{Q(VIN-ST5p0)}$	VIN quiescent current, single output mode	Non-switching, V_{EN} = 2V, V_{BIAS} = V_{VOSNS1} = 5V + 10%		29	55	µA
$I_{Q(VIN-ST3p3)}$	VIN quiescent current, single output mode	Non-switching, V_{EN} = 2V, V_{BIAS} = V_{VOSNS1} = 3.3V + 10%		18	43	µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = 0V, +25c degrees results only, all corners (n,w,s)		0.5	8	µA
UVLO						
$VIN_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising		3.5	3.80	V
$VIN_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling		2.5		V
$VIN_{UVLO(H)}$	VIN UVLO hysteresis		0.75	1	1.25	V
ENABLE						
$V_{EN(R)}$	EN1/2 voltage rising threshold	EN1/2 rising, enable switching	1.125	1.25	1.375	V
$V_{EN(F)}$	EN1/2 voltage falling threshold	EN1/2 falling, disable switching	0.8	0.9	1.0	V
$V_{EN(H)}$	EN1/2 voltage hysteresis		0.25	0.325	0.55	V
$V_{EN(W)}$	EN1/2 voltage wake-up threshold		0.4			V
I_{EN}	EN1/2 pin sourcing current post EN rising threshold	$V_{EN1/2}$ = V_{IN} = 13.5V		1	400	nA
INTERNAL LDO						
V_{VCC}	Internal LDO output voltage	V_{BIAS} ≥ 3.4V, I_{VCC} ≤ 100mA	2.7	3.1	3.7	V
I_{VCC}	Internal LDO short-circuit current limit	V_{IN} = 13.5V	100	360	880	mA
$V_{VCC(UVLO-R)}$	VCC UVLO rising threshold for startup		3.3	3.5	3.75	V
$V_{VCC(UVLO-F)}$	VCC UVLO falling threshold for shutdown			2.5	3	V
REFERENCE VOLTAGE						
$V_{FB1/2}$	Dual Output FB voltages in adjustable output configuration		788	800	812	mV
V_{FB1_so}	Single Output mode FB voltage in adjustable output configuration		788	800	812	mV
$I_{FB1/2(LKG)}$	FB input leakage current in dual output configuration	$V_{FB1/2}$ = 0.8V		10	250	nA
$I_{FB1\_so(LKG)}$	FB input leakage current in single output configuration	V_{FB} = 0.8V		10	250	nA
$FB_{Sel-5v0}$	Voltage threshold for fixed 5.0V setting		VCC-0.5			V
$FB_{Sel-3v0}$	Resistor for fixed 3.3V setting				300	Ω
$FB_{Sel-ext}$	Minimum Thevenin Equivalent resistance of external FB divider option to select adjustable output voltage.		4			kΩ
ERROR AMPLIFIER						
g_{m-S1}	EA transconductance - single output mode	V_{FB1} = V_{COMP}	625	1000	1300	µS
$I_{COMP(src)}$	EA source current - single output mode	V_{COMP} = 1V, V_{FB1} = 0.4V	100	200	400	µA
$I_{COMP(sink)}$	EA sink current - single output mode	V_{COMP} = 1V, V_{FB1} = 0.8V	100	200	500	µA
SWITCHING FREQUENCY						
$f_{SW1(FPWM)}$	Switching frequency, FCCM operation	R_{RT} = 7.15kΩ to AGND	1.9	2.1	2.3	MHz
$f_{SW2(FPWM)}$	Switching frequency, FCCM operation	R_{RT} = 39.2kΩ to AGND	360	410	450	kHz
$f_{ADJ(FCCM)}$	Adjustable switching frequency range	R_{RT} resistor from 6.81kΩ to 158kΩ to AGND	0.1		2.2	MHz
$f_{SS(int)}$	Spread Spectrum switching frequency range	R_{RT} = 7.15 kΩ, R_{CONFIG}= 73.2k Ω		+-10%		
SYNCHRONIZATION						
$V_{IH(sync)}$	SYNCIN high-level threshold			1.35	1.6	V
$V_{IL(sync)}$	SYNCIN low-level threshold		0.65	0.95		V

6.5 Electrical Characteristics (続き)

T_J = –40°C to +150°C. Typical values are at T_J = 25°C and V_{IN} = 13.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(sync)}$	Sync output high voltage min	10mA load	1.6	2.6		V
$V_{OL(sync)}$	Sync output low voltage max	10mA load		0.35	0.68	V
$f_{SYNC-2p1}$	Frequency sync range around 2.1MHz	R_{RT} = 7.15kΩ to AGND	1.7	2.1	2.4	MHz
$f_{SYNC-0p4}$	Frequency sync range around 400kHz	R_{RT} = 39.2kΩ to AGND	320	400	480	kHz
$t_{SYNC(min)}$	Pulse width of external synchronization signal above $V_{IH(sync)}$		100			ns
$t_{SYNC(max)}$	Pulse width of low external synchronization signal below $V_{IL(sync)}$		100			ns
$t_{SYNC-SW(delay)}$	Delay from SYNC rising edge to SW rising edge - single output mode - secondary				120	ns
STARTUP						
$t_{SS(R)}$	Internal fixed soft-start time - dual output mode	From $V_{VOSNS1/2}$= 0% (first SW pulse) to $V_{VOSNS1/2}$ = 90%	2.7	4.5	7	ms
$t_{SS\_Lockout(R)}$	Time from first SW1/2 pulse to enable FPWM mode if output not in regulation - dual output mode		7	13	32	ms
$I_{SS(R)}$	Soft-start charge current - single output mode	V_{SS} = 0V	15	20	25	µA
$R_{SS(F)}$	Soft-start discharge resistance - single output mode			10	27	Ω
t_{EN}	EN1 (Single output mode) or EN1/ EN2 (whichever first in dual output mode) HIGH to start of switching delay			600	900	µs
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	$V_{BOOT-SW}$ = 3.3V, I_{OUT} = 1A		37	75	mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	V_{VCC} = 3.3V, I_{OUT} = 1A		23.9	50	mΩ
$t_{ON(min)}$	Minimum ON pulse width	V_{IN} = 20V, I_{OUT} = 2A		50	65	ns
$t_{ON(max)}$	Maximum ON pulse width (dual output, single output primary)	R_{RT} = 7.15kΩ	5	8	12	µs
$t_{ON(max)}$	Maximum ON pulse width (single output secondary)	R_{RT} = 7.15kΩ		16	25	µs
$t_{OFF(min)}$	Minimum OFF pulse width	V_{IN} = 4V		80	110	ns
BOOT CIRCUIT						
OVERCURRENT PROTECTION						
$I_{HS(OC3)}$	High-side peak current limit LM644A2	Peak current limit on HS FET when Duty Cycle approaches 0%	8.99	11	13.9	A
$I_{LS(OC3)}$	Low-side valley current limit LM644A2	Valley current limit on LS FET	6.2	7.7	9.27	A
$I_{LS3(NOC)}$	Low-side negative current limit LM644A2	Sinking current limit on LS FET		5		A
$IL_{PEAK3(min-0)}$	Min peak inductor current at minimum duty cycle LM644A2	V_{VCC} = 3.3V, t_{pulse} ≤ 100ns		1.5		A
$IL_{PEAK3(min-100)}$	Min peak inductor current at maximum duty cycle LM644A2	V_{VCC} = 3.3V, t_{pulse} ≥ 1µs		0.4		A
$V_{Hiccup-FB}$	Hiccup threshold on FB pin - dual output mode, adjustable output option	LS FET On-time > 165ns	.25	0.3	0.35	V
$t_{Hiccup-1}$	Wait time before entering Hiccup - single and dual output mode		126	128	130	Curent Limit cycles
$t_{Hiccup-2}$	Hiccup time before re-start		50	88		ms
POWER GOOD						
V_{PGTH-1}	Power-Good threshold (PG1/2)	PGOOD low, $V_{VOSNS1/2}$ rising	93%	95%	97%	
V_{PGTH-2}	Power-Good threshold (PG1/2)	PGOOD high, $V_{VOSNS1/2}$ falling	92%	94%	96%	
V_{PGTH-3}	Power-Good threshold (PG1/2)	PGOOD high, $V_{VOSNS1/2}$ rising	105%	107%	110%	
V_{PGTH-4}	Power-Good threshold (PG1/2)	PGOOD low, $V_{VOSNS1/2}$ falling	104%	106%	109%	

6.5 Electrical Characteristics (続き)

T_J = –40°C to +150°C. Typical values are at T_J = 25°C and V_{IN} = 13.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PGOOD(R)}$	PG1/2 delay from $V_{VOSNS1/2}$ valid to PGOOD high during start-up	$V_{VOSNS1/2}$ = 3.3V		2.3		ms
$t_{PGOOD(F)}$	PG1/2 delay from $V_{VOSNS1/2}$ invalid to PGOOD low	$V_{VOSNS1/2}$ = 3.3V		45		µs
$I_{PG(LKG)}$	PG1/2 pin Leakage current when open drain output is high	V_{PG} = 3.3V			0.1	µA
$V_{PG-D(LOW)}$	PG pin output low-level voltage for both channels	I_{PG} = 1mA, V_{EN} = 0V.			400	mV
R_{PG-1}	Pull Down MOSFET Resistance	I_{PG} = 1mA, V_{EN} = 3.3V.		30	90	Ω
$V_{IN(PG\_VALID)}$	Min VIN for valid PG output	Pull up resistance on PG - R_{PG} = 10kΩ, Voltage Pull up on PG - V_{PULLUP_PG} = 3V, $V_{PG-D\ (LOW)}$ = 0.4V	0.45		1.2	V
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising		168		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			10		°C

6.6 Typical Characteristics

Unless otherwise specified, V_{IN} = 13.5V.

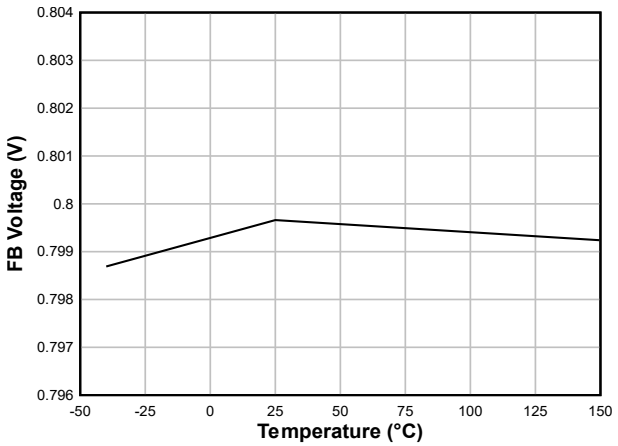
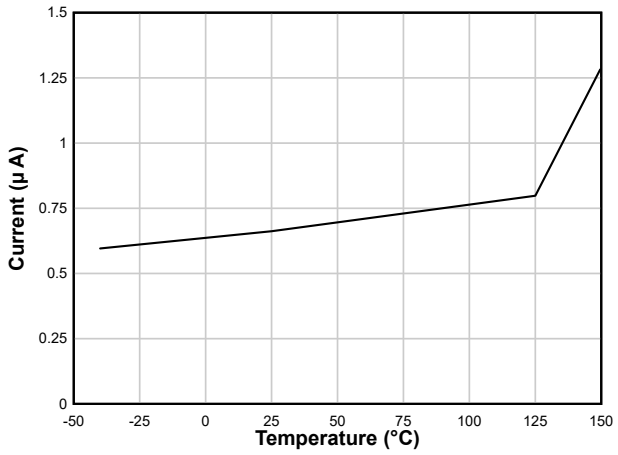


図 6-1. Feedback Voltage



EN = 0V

図 6-2. Shutdown Supply Current

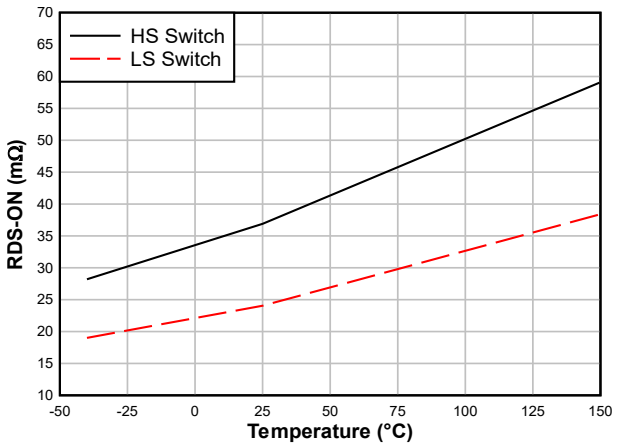


図 6-3. High-side and Low-side Switches R_{DS_ON}

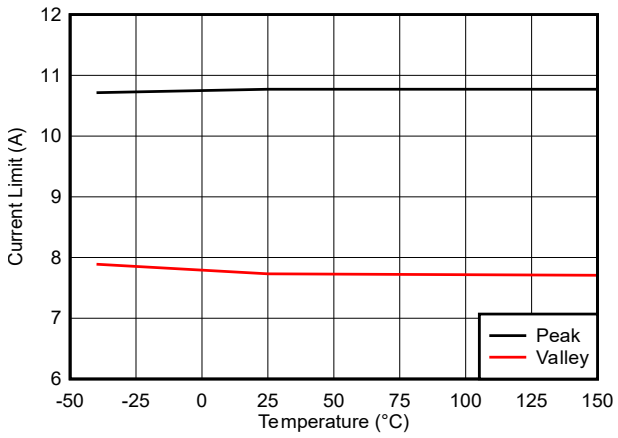


図 6-4. High-side and Low-side Current Limits LM644A2

7 Detailed Description

7.1 Overview

The LM644A2-Q1 is a wide-input, synchronous, buck DC/DC converter for high-current single or dual outputs. The device uses an interleaved, stackable, current-mode control architecture for easy loop compensation, fast transient response, excellent load and line regulation, and accurate current sharing stackable up to six phases for higher output currents up to 36A.

A high-side switch minimum on-time of 50ns allows large step-down ratios, enabling the direct conversion from 12V, 24V, or automotive inputs to low-voltage rails for reduced system complexity and design cost. The LM644A2-Q1 supports input voltage dips as low as 3V, at nearly 100% duty cycle. If the minimum on-time or minimum off-time does not support the desired conversion ratio, the frequency is reduced. This action automatically allows regulation to be maintained during load dump and with very low dropout during cranking.

Power the bias of LM644A2-Q1 from the output of the converter for lower input quiescent current and power loss. Achieving 9µA no-load quiescent current in dual output configuration to extend operating run-time in battery-powered systems.

The LM644A2-Q1 has been designed for low EMI. The device includes the following:

- Reduction of noise at the fundamental switching frequency through interleaving
  - To reduce input capacitor ripple current and EMI filter size, the device can be configured to operate in a stack of either two, four or six phases with corresponding phase shift interleave operation based on the number of phases. For example, in a 4-phase setup, a 90° out-of-phase clock output setup works well for cascaded, multi-channel, or multi-phase power stages. Phase relationship is maintained in light load operation for low output voltage ripple.
- Pin-enabled dual random spread spectrum (DRSS)
  - Dual Random Spread Spectrum (DRSS) frequency hopping is set to ±10% (typical), drastically reducing peak emissions through a combination of triangular and pseudorandom modulation.
- Symmetrical V_{IN} pinout for low input inductance
- Operation over a frequency range above and below AM radio band
  - Resistor-adjustable switching frequency adjustable from 100kHz to 2.2MHz can be synchronized to an external clock source to eliminate beat frequencies in noise-sensitive applications.

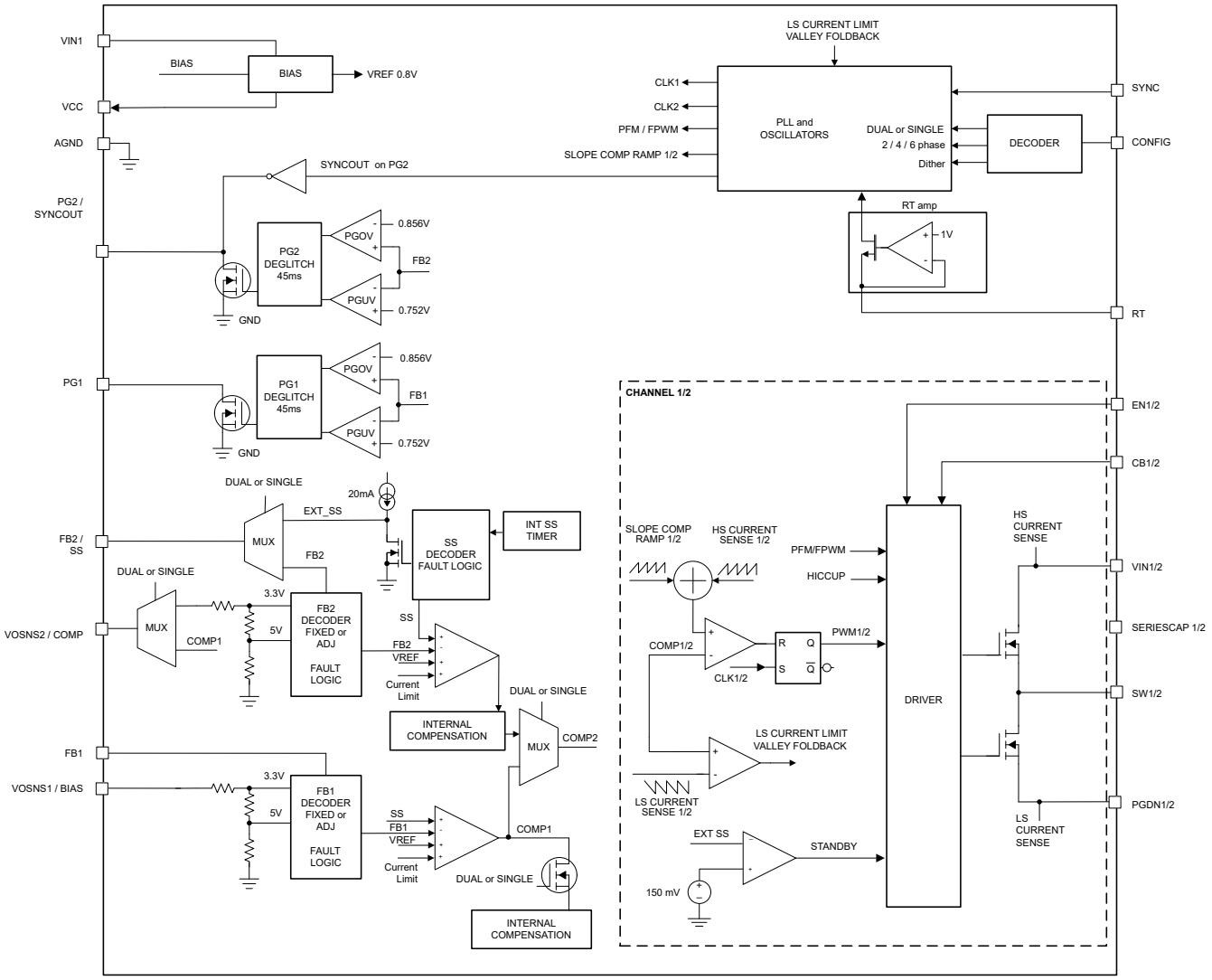
Together, these features can eliminate shielding and other expensive EMI mitigation measures.

The device also includes the following features:

- Internal fixed soft start or adjustable soft start using an external capacitor with monotonic start-up into prebiased loads
- Open-drain Power-Good flags with built-in delayed release for fault reporting and output monitoring
- Independent enable inputs
- Integrated VCC bias supply regulator
- Hiccup-mode overload protection
- Thermal shutdown protection with automatic recovery

The LM644A2-Q1 comes in a 5mm × 4mm, enhanced, HotRod QFN 24-pin package with enlarged corner terminals for improved BLR and wettable flanks, allowing for optical inspection and allowing use in reliability-conscious environments

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage Range (V_{IN})

The LM644A2-Q1 can start up from 3.5V to 36V. After start-up, the input voltage range can extend down to 3V. The device is intended for step-down conversions from 12V automotive and 24V industrial supply rails. The application circuit shows all the necessary components to implement an LM644A2-Q1 based wide-V_{IN} dual-output step-down regulator using a single supply. The LM644A2-Q1 uses an internal LDO subregulator to provide a VCC bias rail for the gate drive and control circuits.

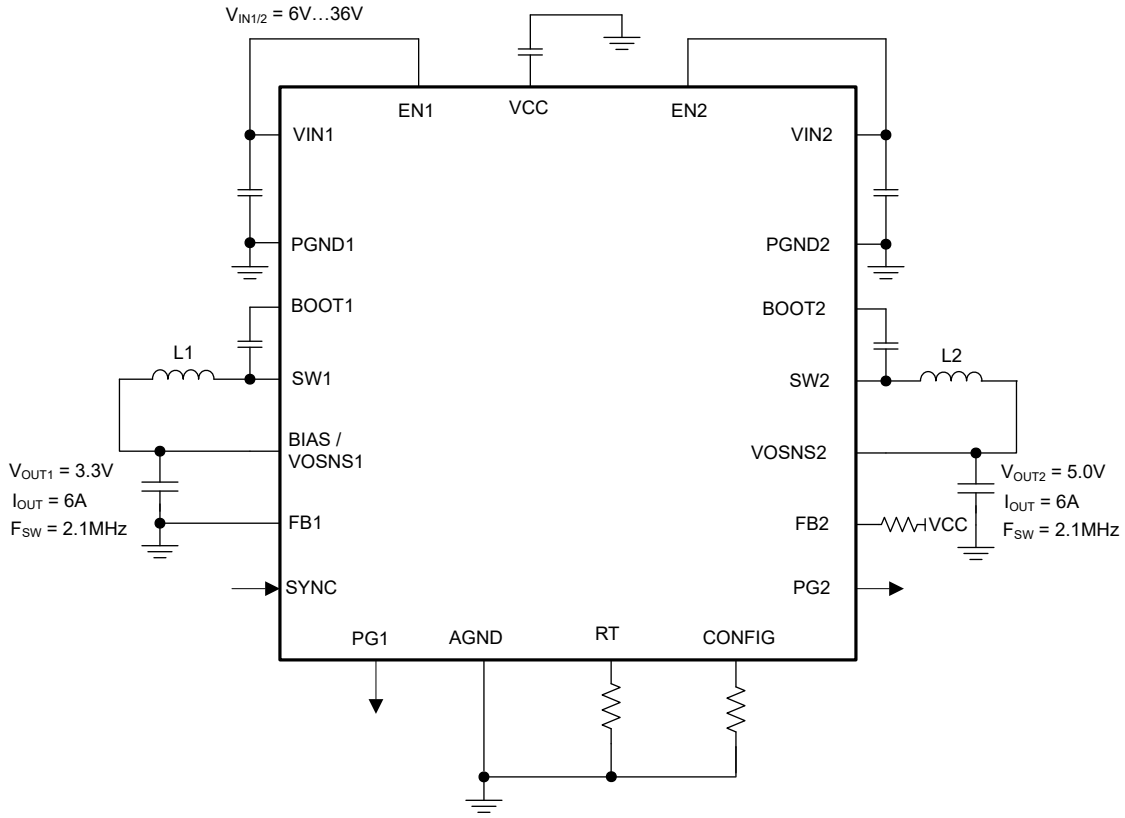


図 7-1. Dual-Output Regulator Schematic Diagram With Input Voltage Operating Range of 6V to 36V

In high input voltage applications, take extra care to make sure the VIN and SW pins do not exceed the absolute maximum voltage rating of 42V during line or load transient events. Voltage excursions that exceed the maximum ratings can damage the IC. Proceed carefully during PCB board layout and use high-quality input bypass capacitors to minimize voltage overshoot and ringing.

7.3.2 Enable EN Pin and Use as V_{IN} UVLO

Apply a voltage less than 0.25V to the EN1 pin to put the LM644A2-Q1 into shutdown mode. In shutdown mode, the quiescent current drops to 0.5µA (typical). Above this voltage but below the lower EN threshold, VCC is active but switching on SW1 and SW2 remains inactive. After EN1 is above V_{EN}, the SW1 becomes active. EN2 controls switching on the second output SW2. In dual output configuration EN2 can be used to independently turn off the second output voltage, but does not control entering shutdown mode. In single-output multi-phase configuration EN1 on primaries and secondaries must be tied together. In single output configuration EN1 must not be used to disable the secondary devices for phase shedding. EN2 of the primary and secondaries must be tied together and can be used to shutdown the secondary phases. The very high efficiency of the device in PFM operation eliminates the need to phase shed in most designs as phase of the secondaries is controlled even under PFM operation.

The EN terminals cannot be left floating. The simplest way to enable the operation is to connect the EN pins to VIN. This action allows the self-start-up of the device when VIN drives the internal VCC above the UVLO level. However, many applications benefit from employing an enable divider string, which establishes a precision input undervoltage lockout (UVLO). The precision UVLO can be used for the following:

- Sequencing
- Preventing the device from retriggering when used with long input cables
- Reducing the occurrence of deep discharge of a battery power source

Note that EN thresholds are accurate. The rising enable threshold has 10% tolerance. Hysteresis is enough to prevent retriggering upon shutdown of the load (approximately 38%). The external logic output of another IC can also be used to drive the EN terminals, allowing system power sequencing.

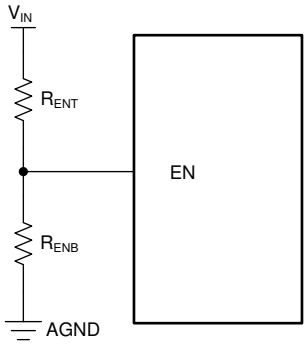


図 7-2. VIN UVLO Using the EN Pin

Resistor values can be calculated using the following equations:

$$R_{ENB} = R_{ENT} \times \left(\frac{V_{EN(R)}}{V_{IN(on)} - V_{EN(R)}} \right) \quad (1)$$

$$V_{OFF} = V_{IN(on)} \times \left(1 - V_{EN(H)} \right) \quad (2)$$

where

- V_{ON} = V_{IN} turn-on voltage
- V_{OFF} = V_{IN} turn-off voltage

7.3.3 Output Voltage Selection and Soft Start

A voltage divider between the output voltage and the FB1 pin is used to create an adjustable output voltage from 0.8V to 20V for the first buck converter. The thevenin impedance of the divider must be larger than 4kohms, to correctly enter adjustable output voltage configuration. TI recommends lower output voltages a minimum of 10kohms for R_{FBT} to meet this requirement. For a fixed 5V output connect FB1 to VCC through a 10 kohm resistor. For a fixed 3.3V connect FB1 to AGND. For fixed output voltage configurations the first channel output voltage is sensed on pin 13 BIAS/VOSNS1.

For dual-output voltage configuration, R_{CONFIG} = 0 (spread spectrum disabled) or 121kΩ (spread spectrum enabled).

FB2 is configured in the same manner as FB1. A voltage divider between output voltage and the FB2 pin is used to create an adjustable output voltage from 0.8 to 20V for the second buck converter. The thevenin impedance of the divider must be larger than 4kohms, to correctly enter adjustable output voltage configuration. For lower output voltages, TI recommends a value of 10kohms for R_{FBT} to meet this requirement. For a fixed 5V output, connect FB2 to VCC through a 10kohm resistor. For a fixed 3.3V connect FB2 to AGND. For fixed output voltage configurations, the second channel output voltage is sensed on pin 19. that is, VOSNS2.

Current sharing between multiple buck channels can increase the current. For one device, single-output multi-phase operation can double the single buck current and provide up to 12A. Using three devices allows six times the current up to 36A. When the device is configured to single-output multi-phase operation (9.53kΩ < R_{CONFIG} < 93.1kΩ) , FB2 is re-configured to provide an adjustable soft start (SS). An external capacitor can be placed from this pin to ground to extend the internal soft-start time. The time can be calculated using the soft-start current of 20µA (typical) charging the external capacitor to the reference voltage of 0.8V (typical). As an example, a 220nF capacitor provides a soft start of 8ms after the initialization of the device. The pin must also be tied to FB2/SS of all other LM stacked devices for fault communication between primary and secondary devices. Faults, such as thermal shutdown, are communicated by pulling the pin low and stops switching for all devices.

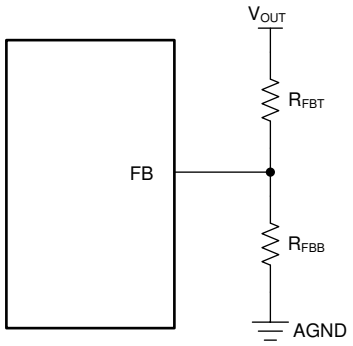


図 7-3. Setting Output Voltage of Adjustable Versions

The LM644A2-Q1 uses a 0.8V reference. The following equation can be used to determine R_{FBB} for a desired output voltage and a given R_{FBT}. Usually, R_{FBT} is limited to a maximum value of 100kΩ to prevent drifting due to PCB leakage under harsh conditions. To improve light load efficiency, a larger resistance of up to 1MΩ can be used in cleaner environments, or the fixed output voltage options can be used under harsher conditions.

$$R_{FBB}[k\Omega] = \frac{0.8 \times R_{FBT}[k\Omega]}{(V_{OUT} - 0.8)} \quad (3)$$

In addition, a feedforward capacitor C_{FF} can be used to optimize the transient response. Typical values are provided in the applications section and were selected based upon the top feedback resistor to place a zero slightly above the cross-over frequency.

7.3.4 SYNC Allows Clock Synchronization and Mode Selection

The SYNC pin can be used to select forced pulse width modulation (FPWM) or pulse frequency modulation (PFM). In FPWM the switching frequency remains constant at lighter output currents. In PFM the low-side FET is turned off when the inductor current goes negative and the frequency is reduced to improve efficiency under light-load conditions. Connect SYNC to AGND to enable PFM. Connect SYNC to VCC to operate the LM644A2-Q1 in FPWM mode with continuous conduction at light loads.

The SYNC pin can also be used to synchronize the internal oscillator to an external clock. When synchronized to an external clock the LM644A2-Q1 operates in FPWM. The internal oscillator can be synchronized to a positive edge into the SYNC pin. The coupled edge voltage at the SYNC pin must exceed the SYNC amplitude threshold of V_{SYNCDH} to trip the internal synchronization pulse detector. The minimum SYNC rising pulse and falling pulse durations must be longer than t_{PULSE_H} and t_{PULSE_L} respectively. The LM644A2-Q1 switching action can be synchronized to an external clock from 200kHz to 2.2MHz. When synchronizing to an external clock, the R_T pin must be used to set the internal frequency to a value close to that of the external clock. This action prevents large frequency changes in the event of loss of synchronization. This action is also used to set the slope compensation for secondary devices.

In single-output two-phase operation, the PG2/SYNC-OUT terminal of the primary can be left floating as clock information is shared internally.

In single-output four-phase operation, the PG2/SYNC-OUT terminal of the primary must be connected to the SYNC pin of the secondary to clock all four phases 90 degrees out of phase.

In single-output six-phase operation, the PG2/SYNC-OUT terminal of the primary must be connected to the SYNC pin of the secondary device. The PG2/SYNC-OUT terminal of the secondary must be connected to the SYNC pin of the tertiary device. In this way, the devices operate all six phases 60 degrees out of phase.

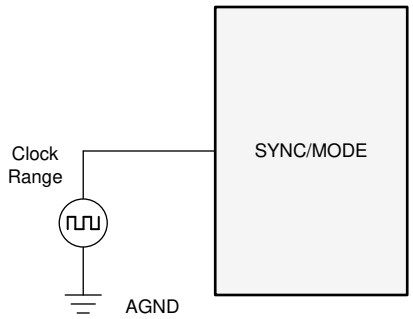
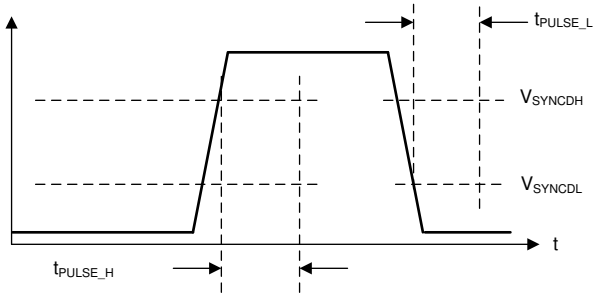


図 7-4. Typical Implementation Allowing Synchronization Using the SYNC/MODE Pin



This image shows the conditions needed for detection of a synchronization signal.

図 7-5. Typical SYNC/MODE Waveform

7.3.5 Clock Locking

After a valid synchronization signal is detected on the primary or dual output converter, a clock locking procedure is initiated. After approximately 32 pulses, the clock frequency abruptly changes to the frequency of the synchronization signal. While the frequency adjusts suddenly, phase is maintained so the clock cycle lying between operation at the default and synchronization frequencies is of intermediate length. There are no very long or very short pulses. After frequency is adjusted, phase is adjusted over a few tens of cycles so that rising synchronization edges correspond to rising the SW node pulses.

7.3.6 Adjustable Switching Frequency

The frequency is set using a resistor on the RT pin. A resistor to AGND is used to set the adjustable operating frequency. See the following table for resistor values. Note that if a resistor value falls outside of the recommended range, this fall can cause the device to stop switching. Do not apply a pulsed signal to this pin to force synchronization. If synchronization is needed, see the SYNC pin.

$$R_T[k\Omega] = \left(\frac{16.4}{F_{SW}[MHz]} - 0.633\right) \quad (4)$$

For example, for f_{SW} = 400kHz, R_T = (16.4 / 0.4) – 0.633 = 40.37, so a 40.2kΩ resistor is selected as the closest choice.

表 7-1. Typical R_T values

R_T (kΩ)	Frequency (kHz)
6.81	2206
7.15	2106
15.4	1005
31.6	497.4
39.2	402
158	101

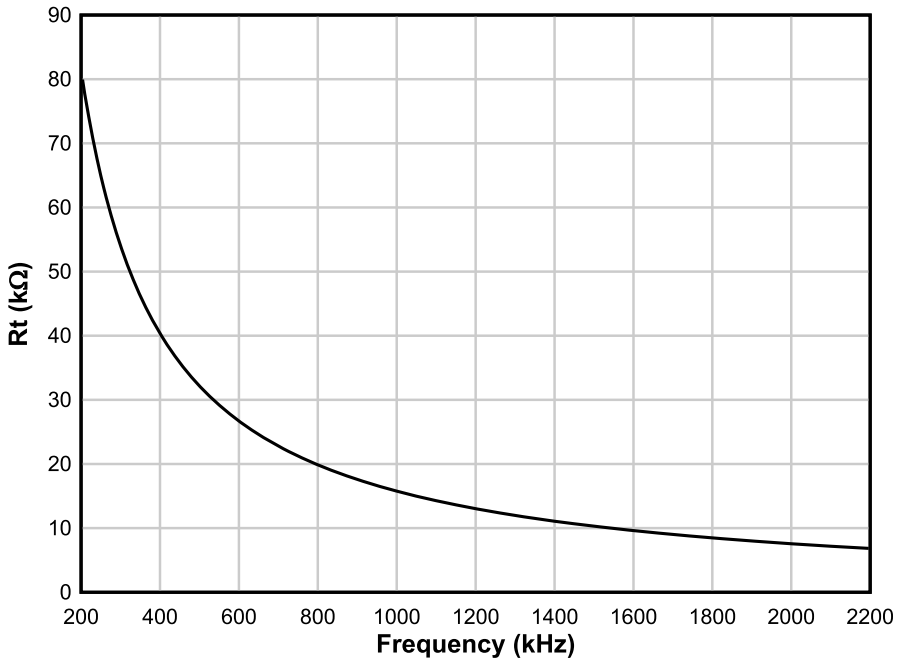


図 7-6. Setting Clock Frequency

7.3.7 Power-Good Output Voltage Monitoring

While the PG1/PG2 of the LM644A2-Q1 resembles a standard power-good function, the functionality is designed to replace a discrete reset IC, reducing BOM cost. There are three major differences between the PG function and the normal power-good function seen in most regulators:

- A delay has been added for release of reset. See 表 7-2.
- PG output signals a fault (pulls the output to ground) while the part is disabled.
- PG continues to operate with input voltage as low as 1.2V. Below this input voltage, PG output can be high impedance.

For dual output configuration (R_{CONFIG} = 0 or 121kΩ), The PG1 is an open-drain and must be tied through a resistor to an external voltage, and pulls low if the monitors on FB1 or VOSNS1 trip. The PG2 flag is configured in the same manner as PG1 and monitors the second output at either FB2 or VOSNS2.

For single-output multiphase operation (9.53kΩ < R_{CONFIG} < 93.1kΩ) , PG2 is re-configured as SYNC-OUT to provide a phase shifted clock to the secondary devices. In this configuration, the PG2/SYNC-OUT terminal of the primary device can be left floating for dual phase operation or tied to the SYNC pin of the secondary device for more than four-phases. For six-phase operation the PG2/SYNC-OUT pin of the secondary device is connected to the SYNC pin of the tertiary device.

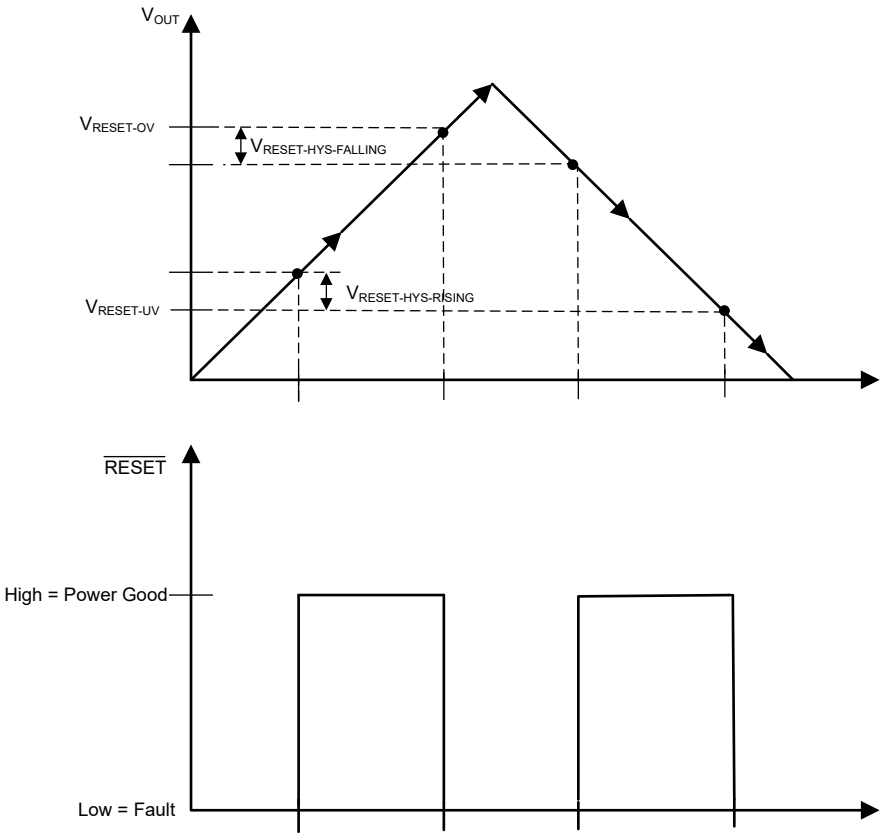


図 7-7. PG Static Voltage Thresholds

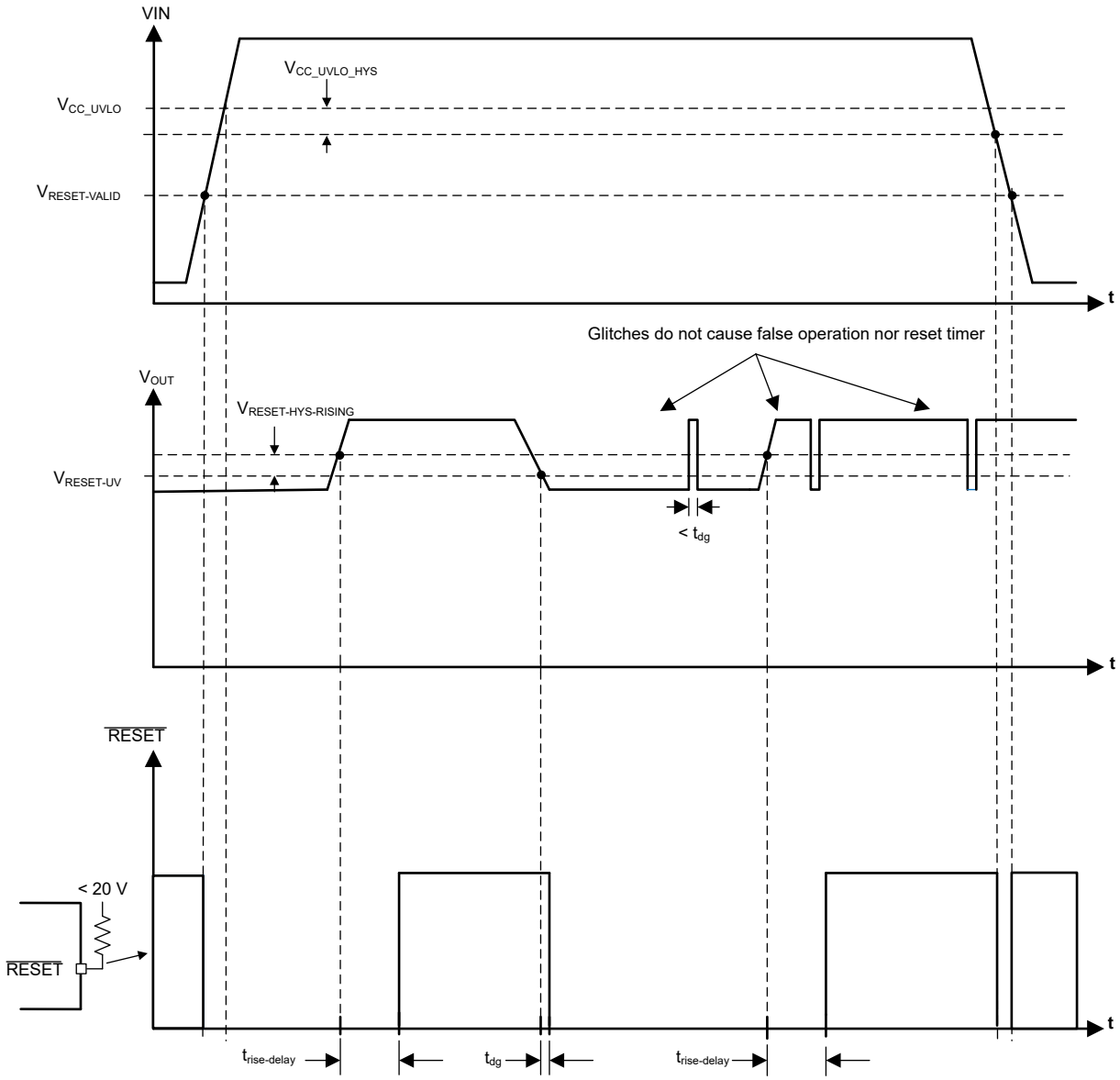


図 7-8. PG Timing Diagram (Excludes OV Events)

表 7-2. Conditions that Cause PG to Signal a Fault (Pull Low)

FAULT CONDITION INITIATED	FAULT CONDITION ENDS (AFTER WHICH t_{RESET_ACT} MUST PASS BEFORE RESET OUTPUT IS RELEASED)
FB below V_{RESET_UV} for longer than t_{RESET_FILTER}	FB above V_{RESET_UV} + V_{RESET_HYST} for longer than t_{RESET_FILTER}
FB above V_{RESET_OV} for longer than t_{RESET_FILTER}	FB below V_{RESET_OV} – V_{RESET_HYST} for longer than t_{RESET_FILTER}
Junction temperature exceeds T_{SD_R}	Junction temperature falls below T_{SD_F} (1)
EN low	t_{EN} passes after EN becomes high(1)
VIN falls low enough so that VCC falls below V_{CC_UVLO} – $V_{CC\_UVLO\_HYST}$. This value is called $V_{IN\_OPERATE}$.	Voltage on VIN is high enough so that VCC pin exceed V_{CC_UVLO} (1)

(1) As an additional operational check, PG remains low during soft start. It is defined as until the lesser of either full output voltage reached or t_{SS2} has passed since initiation. This is true even if all other conditions in this table are met and t_{RESET_ACT} has passed. Lockout during soft start does not require t_{RESET_ACT} to pass before PG is released.

The threshold voltage for the PG function is specified to take advantage of the availability of the internal feedback threshold to the PG circuit. This allows a maximum threshold of 96.5% of selected output voltage to be specified at the same time as 96% of actual operating point. The net result is a more accurate reset function while expanding the system allowance for transient response. See the output voltage error stack-up comparison in 図 7-9.

In addition to signaling a fault upon overvoltage detection (FB above V_{RESET_OV}), the switch node is shut down and a small, approximately 1mA pulldown is applied to the SW node.

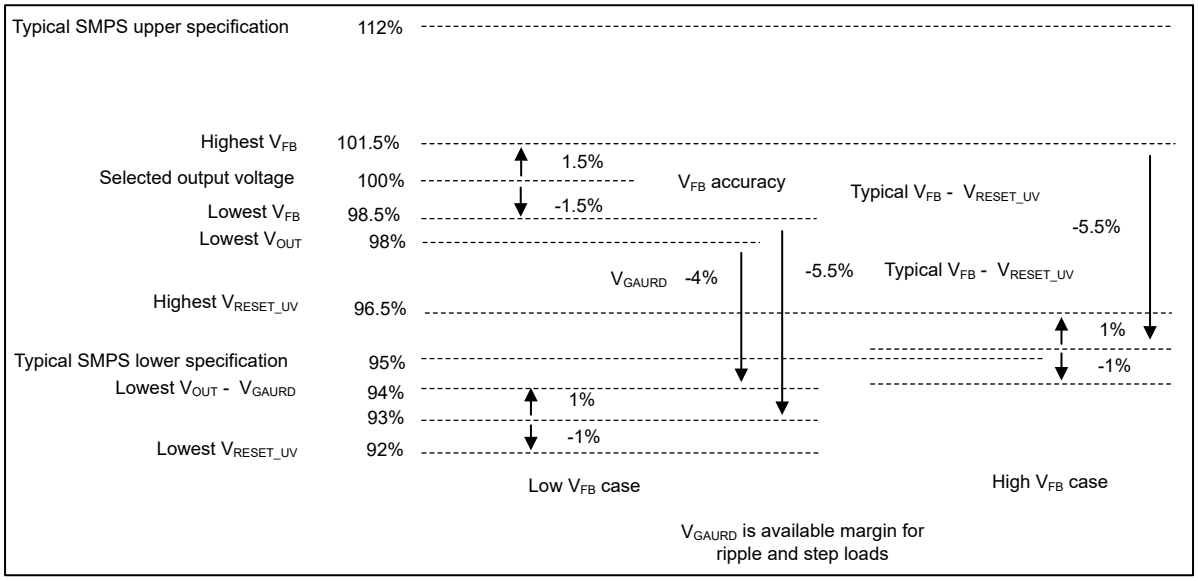


図 7-9. Reset Threshold Voltage Stack-Up

7.3.8 Internal LDO, VCC UVLO, and BIAS Input

The LM644A2-Q1 uses VCC as the internal power supply. VCC is, in turn, powered from VIN or VOSNS1/BIAS. After the device is active power comes from VIN, if BIAS is less than approximately 3.1V. Power comes from BIAS, if BIAS is more than 3.1V. VCC is typically 3V to 3.3V under most conditions, but can be lower if VIN is very low. To prevent unsafe operation, VCC has a UVLO that prevents switching if the internal voltage is too low. See V_{CC_UVLO} and $V_{CC\_UVLO\_HYST}$. During start-up, VCC momentarily exceeds the normal operating voltage until V_{CC_UVLO} is exceeded, then drops to the normal operating voltage. These UVLO values, when combined with the dropout of the LDO when powering the LM644A2-Q1, are used to derive minimum input operating voltage.

7.3.9 Bootstrap Voltage and $V_{CBOOT-UVLO}$ (CB1 and CB2 Pin)

The driver of the power switch (HS switch) requires bias higher than VIN when the HS switch is ON. The capacitors connected between CB1 and SW1 and CB2 and SW2 work as charge pumps to boost voltage on the CB terminals to (SW + VCC). The boot diode is integrated on the LM644A2-Q1 die to minimize the physical design size. TI recommends a 100nF capacitor rated for 10V with X7R or better dielectric for the CBOOT capacitors. The boot (CB1 and CB2) rails have UVLO to protect the chip from operation with too little bias. This UVLO has a threshold of V_{BOOT_UVLO} and is typically 2.1V. If the CBOOT capacitor voltage drops below V_{BOOT_UVLO}, then the device initiates a charging sequence using the low-side FET before attempting to turn on the high-side device.

7.3.10 CONFIG Device Configuration Pin

Several features are included to simplify compliance with CISPR 25 and automotive EMI requirements. To reduce input capacitor ripple current and EMI filter size, the device can be configured to operate in a stack of either two, four, or six phases with corresponding phase shift interleave operation based on the number of phases. For example, in a 4-phase setup, a 90° out-of-phase clock output setup works well for cascaded, multi-channel, or multi-phase power stages. Resistor-adjustable switching frequency as high as 2.2MHz can be synchronized to an external clock source to eliminate beat frequencies in noise-sensitive applications. Optional spread spectrum modulation further improves the EMI signature.

The CONFIG terminal is used to set up the device for either dual output or single output multi-phase operation. The spread spectrum can also be turned on and off with different resistor values.

表 7-3. R_{CONFIG} Resistor Selection

R_{CONFIG} (kΩ)	Mode	Spread Spectrum
0	Dual output	No
9.53	2 phase primary	No
19.1	4 phase primary	No
29.4	6 phase primary	No
41.2	Secondary	N/A
56.2	2 phase primary	Yes
73.2	4 phase primary	Yes
93.1	6 phase primary	Yes
121	Dual output	Yes

When configured in single output multiphase operation, the VOSNS2 pin becomes the output of the error amplifier (COMP) and a resistor and capacitor are needed at this pin to compensate the control loop. R_C = 11kOhms, C_C = 2.2nF can be used in initial evaluation for many designs. Increasing the resistance results in higher loop gain and tends to require proportionately larger output capacitors. Decreasing the capacitance increases the loop response of the device, resulting in faster transients but can lower phase margin at the cross-over frequency and can require adjustments to the output capacitance. The table below has several settings for different output configurations.

表 7-4. Typical Bill of Materials

MODE	V_{OUT1}	V_{OUT2}	FREQUENCY	C_{OUT} EACH PHASE	C_{IN} + C_{HF} EACH PHASE	L1, L2	R_C	C_C
DUAL	3.3V	5V	400kHz	47 + 22µF	2 × 10µF + 1 × 100nF	3.3µH	INTERNAL	INTERNAL
DUAL	3.3V	5V	2200kHz	47 + 22µF	1 × 10µF + 1 × 100nF	0.68µH	INTERNAL	INTERNAL
SINGLE	3.3V	3.3V	400kHz	47 + 22µF	2 × 10µF + 1 × 100nF	3.3µH	11kΩ	2.2nF
SINGLE	5V	5V	2200kHz	47 + 22µF	1 × 10µF + 1 × 100nF	1µH	11kΩ	2.2nF

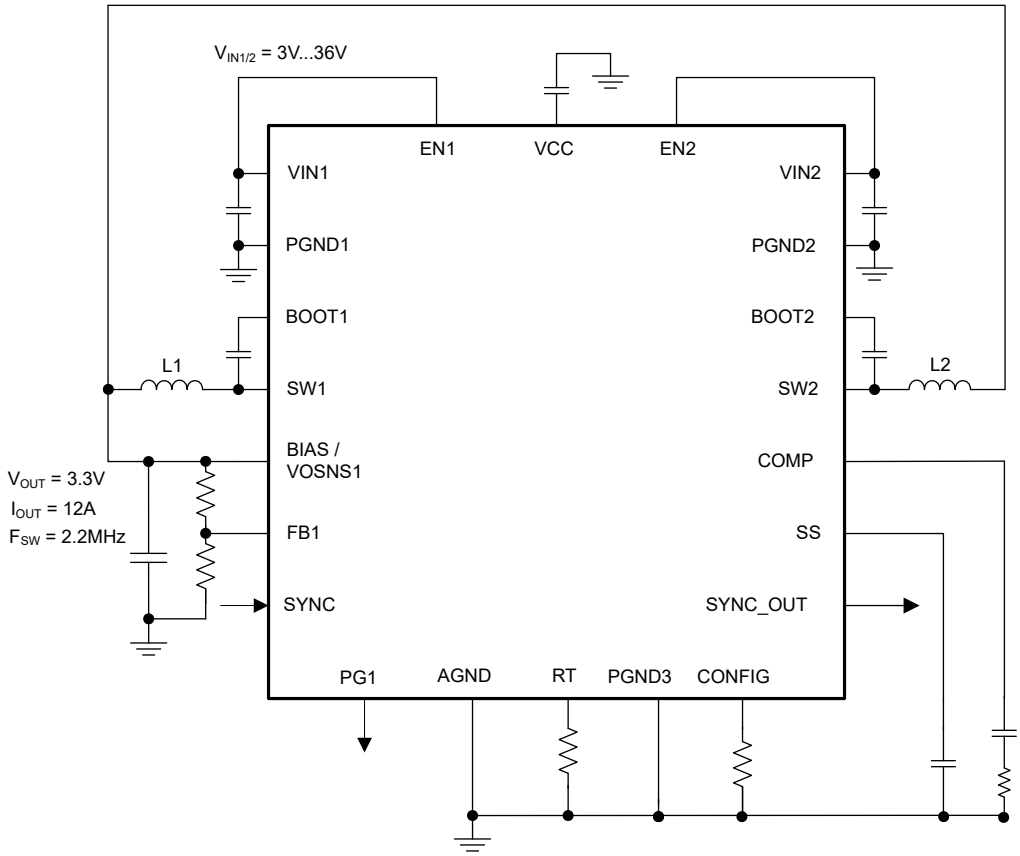


図 7-10. High-Efficiency, Single Output 2-Phase Step-Down Converter

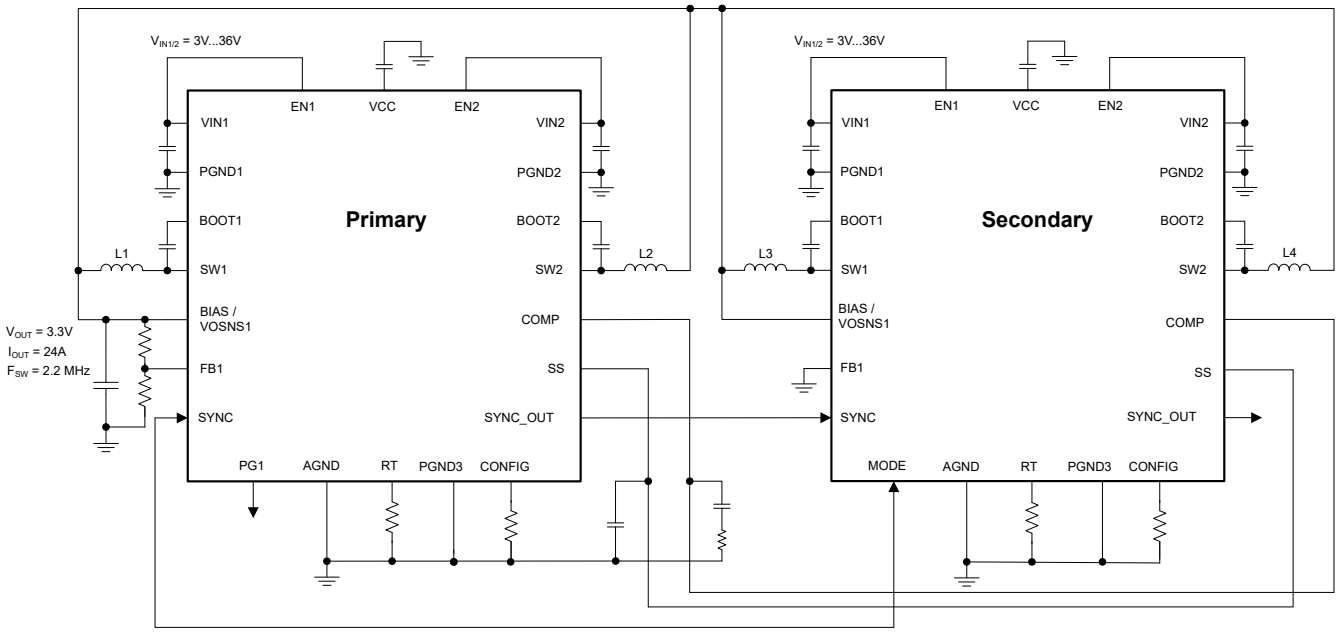
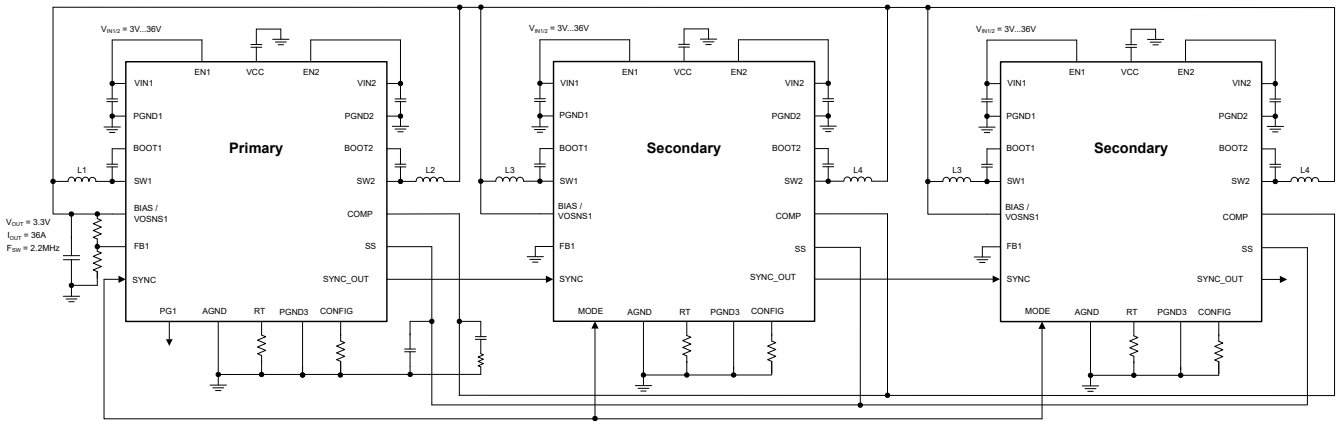


図 7-11. High-Efficiency, Single Output 4-Phase Step-Down Converter



High-Efficiency, Single Output 6-Phase Step-Down Converter

7.3.11 Spread Spectrum

Spread spectrum is configurable using the CONFIG pin. Spread spectrum eliminates peak emissions at specific frequencies by spreading these peaks across a wider range of frequencies than a part with fixed-frequency operation. The LM644A2-Q1 implements a modulation pattern designed to reduce low frequency-conducted emissions from the first few harmonics of the switching frequency. The pattern can also help reduce the higher harmonics that are more difficult to filter, which can fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node and inductor. The LM644A2-Q1 uses a ±10% (typical) spread of frequencies which can spread energy smoothly across the FM and TV bands. The device implements Dual Random Spread Spectrum (DRSS). DRSS is a combination of a triangular frequency spreading pattern and pseudorandom frequency hopping. The combination allows the spread spectrum to be very effective at spreading the energy at the following:

- Fundamental switching harmonic with slow triangular pattern
- High frequency harmonics with additional psuedorandom jumps at the switching frequency

The advantage of DRSS is the equivalent harmonic attenuation in the upper frequencies with a smaller fundamental frequency deviation. This reduces the amount of input current and output voltage ripple that is introduced at the modulating frequency.

The spread spectrum is only available while the clocks of the The LM644A2-Q1 are free running at the natural frequency. Any of the following conditions overrides the clock and can interfere with spread spectrum:

- The clock is slowed due to operation at low input voltage. This is operation in dropout.
- The clock is slowed under light load in auto mode. Note that if the device is operating in FPWM mode, spread spectrum is active, even if there is no load.
- The clock is slowed due to high input-to-output voltage ratio. This mode of operation is expected if on-time reaches minimum on-time. See the *Electrical Characteristics*.
- The clock is synchronized with an external clock.

7.3.12 Soft Start and Recovery From Dropout

When designing with the The LM644A2-Q1, slowed rise in output voltage due to recovery from dropout and soft start must be considered separate phenomena. Soft start is triggered by any of the following conditions:

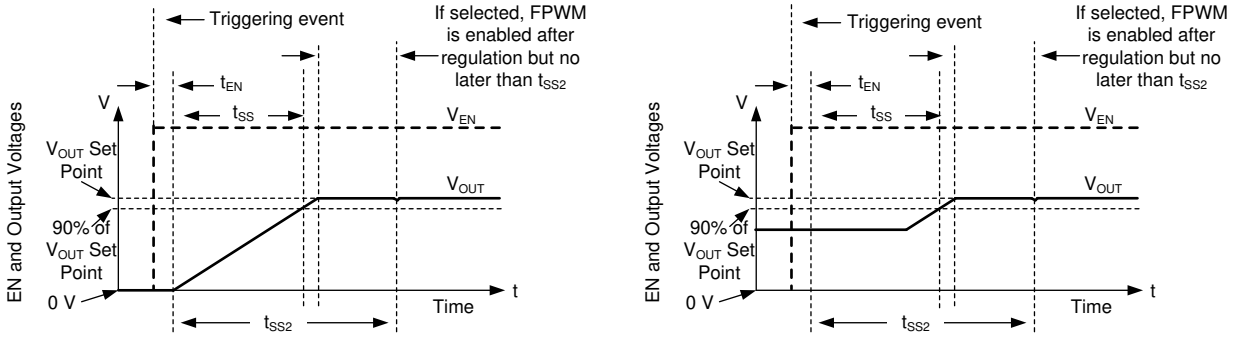
- EN is used to turn on the device.
- Recovery from a hiccup waiting period; see セクション 7.3.14.
- Recovery from shutdown due to overtemperature protection
- Power is applied to the VIN of the IC or the VCC UVLO is released.

After soft start is triggered, the IC takes the following actions:

- The reference used by the IC to regulate output voltage is slowly ramped from zero. The net result is that output voltage, if previously 0V, takes t_{SS} to reach 90% of the desired value.

- Operating mode is set to auto, activating diode emulation. This action allows start-up without pulling output low if there is a voltage already present on the output.
- Hiccup is disabled for the duration of soft start; see セクション 7.3.14.

All of these actions together provide start-up with limited inrush currents. These actions also allow the use of output capacitors and loading conditions that cause current to border on current limit during start-up without triggering hiccup. In addition, if output voltage is already present, output is not pulled down. See 図 7-12.



The left curves show soft start from 0V. The right curves show soft starting behavior from a prebiased or non-zero voltage. In either case, the output voltage reaches within 10% of the desired setpoint t_{SS} time after soft start is initiated. During soft start, FPWM and hiccup are disabled. Both hiccup and FPWM are enabled after output reaches regulation or t_{SS2}, whichever happens first.

図 7-12. Soft-Start Operation

Any time output voltage is more than a few percent low for any reason, output voltage ramps up slowly. This condition, called recovery from dropout, differs from soft start in three important ways:

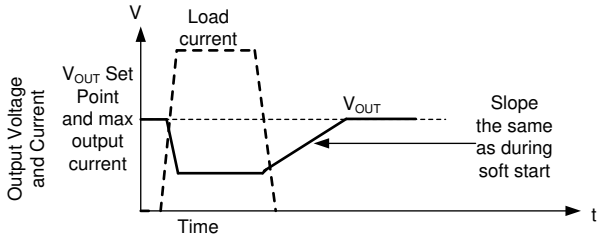
- Hiccup is allowed only if output voltage is less than 0.4 times the set point. Note that during dropout regulation, hiccup is inhibited. See セクション 7.3.14.
- FPWM mode is allowed during recovery from dropout. If output voltage were to suddenly be pulled up by an external supply, the The LM644A2-Q1 can pull down on the output. Note that all the protections that are present during normal operation are in place, protecting the device if output is shorted to a high voltage or ground.
- The reference voltage is set to approximately 1% above that needed to achieve the current output voltage. The reference voltage is not started from zero.

Despite the name, recovery from dropout is active whenever output voltage is more than a few percent lower than the setpoint for long enough that:

- Duty factor is controlled by maximum on-time or
- When the part is operating in current limit.

This primarily occurs under the following conditions:

- Dropout: When there is insufficient input voltage for the desired output voltage to be generated. See セクション 7.4.3.5.
- Overcurrent that is not severe enough to trigger hiccup or if the duration is too short to trigger hiccup. See セクション 7.3.14.



Whether output voltage falls due to high load or low input voltage, after the condition that causes output to fall below the setpoint is removed, output climbs at the same speed as during start-up. Even though hiccup does not trigger due to dropout, hiccup can, in principal, be triggered during recovery if output voltage is below 0.4 times output the setpoint for more than 128 clock cycles during recovery.

図 7-13. Recovery From Dropout

7.3.13 Overcurrent and Short-Circuit Protection

The LM644A2-Q1 is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side and the low-side MOSFETs.

High-side MOSFET overcurrent protection is implemented by the nature of the peak current mode control. The HS switch current is sensed when the HS is turned on after a short blanking time. The HS switch current is compared to the output of the voltage regulation loop minus slope compensation, every switching cycle. Because the voltage loop has a maximum value and slope compensation increases with duty cycle, the HS current limit decreases with increased duty cycle such that the HS current limit is reduced by 35% for high output to input voltage duty ratios. See 図 7-14.

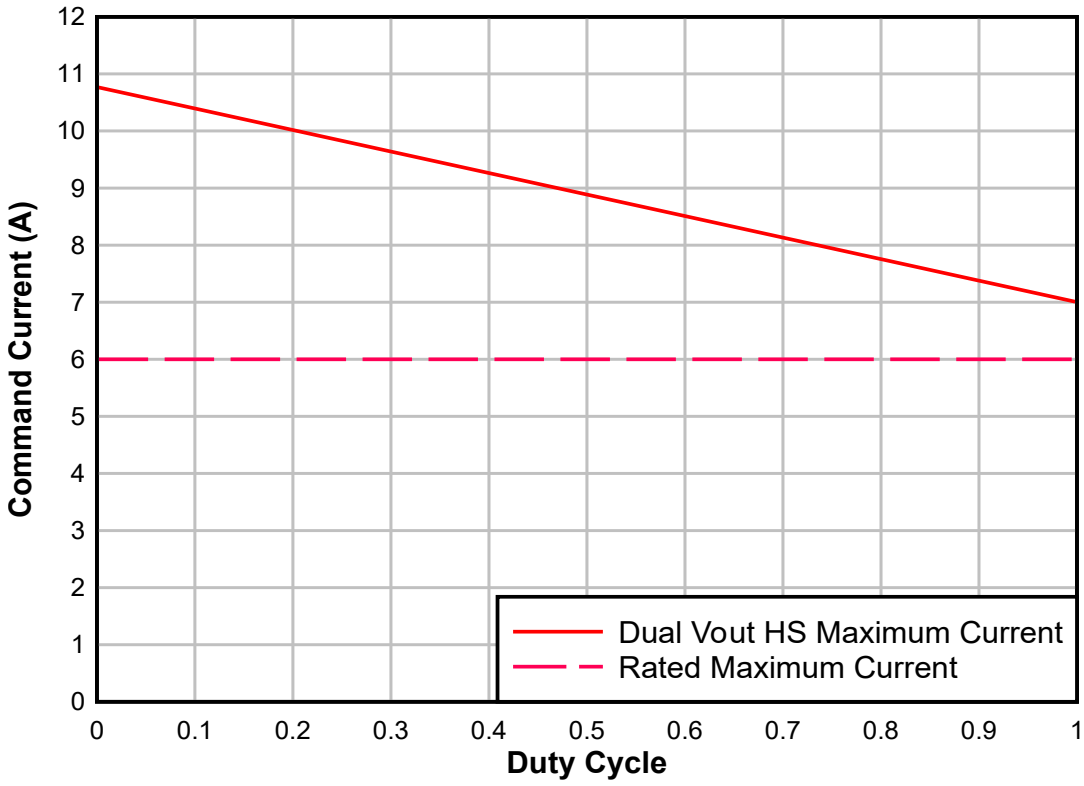


図 7-14. Maximum Current Allowed Through the HS FET - Function of Duty Cycle for LM644A2-Q1

When the LS switch is turned on, the current going through the LS switch is also sensed and monitored. Like the high-side device, the low-side device turn-off is commanded by the voltage control loop. For a low-side device, turn-off is prevented if current exceeds this value, even if the oscillator normally starts a new switching cycle. See セクション 7.4.3.4. Also like the high-side device, there is a limit on how high the turn-off current is allowed to be. This is called the low-side current limit; see the *Electrical Characteristics* for values. If the LS current limit is exceeded, the LS MOSFET stays on and the HS switch is not turned on. The LS switch is turned off after the LS current falls below the limit. The HS switch is turned on again as long as at least one clock period has passed since the last time the HS device has turned on.

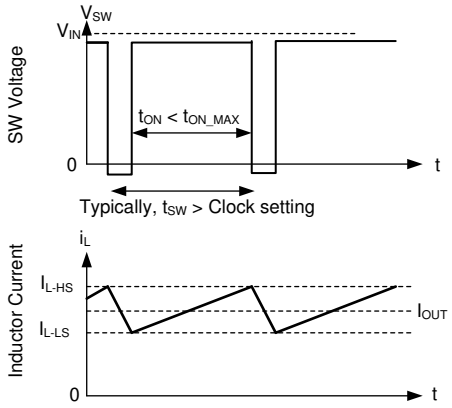


図 7-15. Current Limit Waveforms

The net effect of the operation of high-side and low-side current limit is that the IC operates in hysteretic control. Because the current waveform assumes values between I_{L-HS} and I_{L-LS}, output current is close to the average of these two values unless duty cycle is very high. After operating in current limit, hysteretic control is used and current does not increase as output voltage approaches zero.

If duty cycle is very high, current ripple must be very low to prevent instability; see セクション 8.2.2.3. Because current ripple is low, the part is able to deliver full current unless dropout across device is less than 0.5V. The current delivered is very close to I_{L-LS}.

If overloaded, after the overload is removed, the device recovers as though in soft start; see セクション 7.3.12. Note that hiccup can be triggered if output voltage drops below approximately 0.4 times the intended output voltage.

7.3.14 Hiccup

The LM644A2-Q1 employs hiccup overcurrent protection to prevent overheating in the presence of a short circuit condition.

In dual output mode the part enters hiccup when all of the following conditions are met for 128 consecutive switching cycles:

- A time greater than t_{SS2} has passed since soft start has started; see セクション 7.3.12.
- Output voltage is below approximately 0.4 times output setpoint.
- The part is not operating in dropout defined as having minimum off-time controlled by duty factor.

In single output mode the part enters hiccup when all of the following conditions are met for 128 consecutive switching cycles:

- COMP pin is at maximum of 1.1V.
- The part is not operating in dropout defined as having minimum off-time controlled by duty factor.

In hiccup mode, the device shuts down and attempts to soft start after t_W. Hiccup mode helps reduce the device power dissipation under severe overcurrent conditions and short circuits.

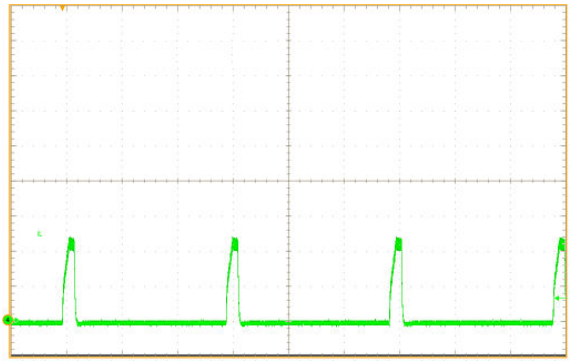


図 7-16. Inductor Current Bursts During Hiccup

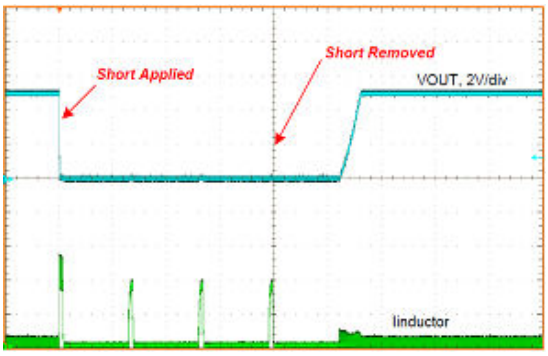


図 7-17. Short-Circuit Transient and Recovery

7.3.15 Thermal Shutdown

Thermal shutdown is a safety mechanism for the device that limits total power dissipation by turning off the internal switches when the a temperature sensor on the IC exceeds 168°C (typical). After thermal shutdown occurs, hysteresis prevents the device from switching until the temperature sensor temperature drops to approximately 159°C (typical). When the sensor temperature falls below 159°C (typical), the LM644A2-Q1 attempts to soft start. While the sensor is close to the power FETs, the sensor must not be used to determine maximum junction temperature of the device under load as there can be temperature gradients across the device. Instead thermal couples and other methods must be used to characterize thermal design in application.

While the LM644A2-Q1 is shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating from a short circuit applied to VCC, the LDO providing power to VCC has reduced current limit while the part is disabled due to high junction temperature. The LDO only provides a few milliamperes during thermal shutdown.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical on and off control of the device. When the EN pin voltage is below 0.4V, both the regulator and the internal LDO have no output voltage and the part is in shutdown mode. In shutdown mode, the quiescent current drops to typically 0.66µA.

7.4.2 Standby Mode

The internal LDO has a lower EN threshold than the output of the regulator. The internal LDO regulates the VCC voltage at 3.3V, typically when:

- The EN pin voltage is above 1.1V (maximum).
- The EN pin voltage is below the precision enable threshold for the output voltage.

The precision enable circuitry is ON after VCC is above the UVLO. The internal power MOSFETs of the SW node remain off unless the voltage on the EN terminal goes above the precision enable threshold. The LM644A2-Q1 also employs UVLO protection. If the VCC voltage is below the UVLO level, the output of the regulator is turned off.

7.4.3 Active Mode

The device is in active mode when the following occurs:

- The EN pin is above V_{EN}.

- V_{IN} is above V_{EN}.
- V_{IN} is high enough to satisfy the V_{IN} minimum operating input voltage.
- No other fault conditions are present.

See セクション 7.3 for protection features. The simplest way to enable the operation is to connect EN to VIN, allowing self-start-up when the applied input voltage exceeds the minimum $V_{IN\_OPERATE}$.

In active mode, depending on the load current, input voltage, and output voltage, the LM644A2-Q1 is in one of six sub-modes:

- Continuous conduction mode (CCM) with fixed switching frequency and peak current mode operation
- Discontinuous conduction mode (DCM) while in auto mode when the load current is lower than half of the inductor current ripple. If current continues to reduce, the device enters Pulse Frequency Modulation (PFM) which reduces the switch frequency to maintain regulation while reducing switching losses to achieve higher efficiency at light load.
- Minimum on-time operation while the on-time of the device needed for full-frequency operation at the requested low-duty cycle is not supported by T_{ON_MIN}
- Forced pulse width modulation (FPWM) similar to CCM with fixed-switching frequency, but extends the fixed frequency range of operation from full to no load
- Dropout mode when switching frequency is reduced to minimize dropout
- Recovery from dropout similar to other modes of operation except the output voltage setpoint is gradually moved up until the programmed setpoint is reached.

7.4.3.1 Peak Current Mode Operation

The following operating description of the LM644A2-Q1 refers to *Functional Block Diagram* and the waveforms in 図 7-18. Both supply a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) NMOS switches with varying duty cycle (D). During the HS switch on-time, the SW terminal voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off-time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, forcing V_{SW} to swing below ground by the voltage drop across the LS switch. The regulator loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on-time of the HS switch over the switching period: $D = T_{ON} / (T_{ON} + T_{OFF})$.

In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: $D = V_{OUT} / V_{IN}$.

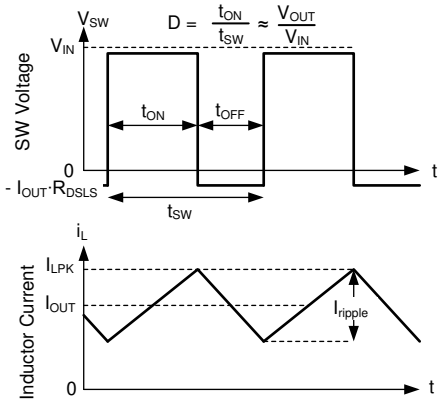


図 7-18. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

To get accurate DC load regulation, a voltage feedback loop is used. Peak and valley inductor currents are sensed for peak current mode control and current protection. The regulator operates with continuous conduction

mode with constant switching frequency when load level is above one half of the minimum peak inductor current. The internally-compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

7.4.3.2 Auto Mode Operation

The LM644A2-Q1 can have two behaviors while lightly loaded. One behavior, called auto mode operation, allows a seamless transition between normal current mode operation while heavily loaded and in highly-efficient light-load operation. The other behavior, called FPWM mode, maintains full frequency even when unloaded. Which mode the LM644A2-Q1 operates in depends on the SYNC/MODE pin. When SYNC/MODE is high, the part is in FPWM. When SYNC/MODE is low, the part is in PFM.

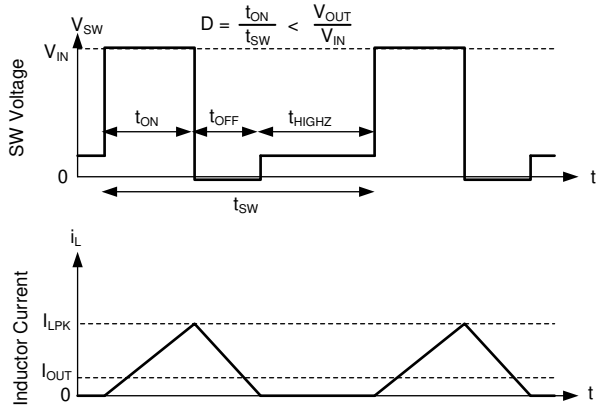
In auto mode, light-load operation is employed in the LM644A2-Q1 at load lower than approximately 1/10th of the rated maximum output current. Light-load operation employs two techniques to improve efficiency:

- Diode emulation, which allows DCM operation
- Frequency reduction

Note that while these two features operate together to create excellent light load behavior, these features operate independently of each other.

7.4.3.2.1 Diode Emulation

Diode emulation prevents reverse current though the inductor, which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. Frequency is reduced when peak inductor current goes below $I_{PEAK-MIN}$. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.



In auto mode, the low-side device is turned off after inductor current is near zero. As a result, after output current is less than half of inductor ripple in CCM, the part operates in DCM. This action is equivalent to saying that diode emulation is active.

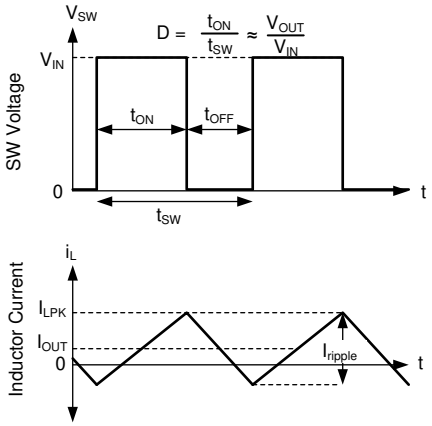
図 7-19. PFM Operation

The LM644A2-Q1 has a minimum peak inductor current setting in auto mode. That being said, when current is reduced to a low value with fixed input voltage, on-time is constant. Regulation is then achieved by adjusting frequency . This mode of operation is called PFM mode regulation.

7.4.3.3 FPWM Mode Operation

Like auto mode operation, FPWM mode operation during light-load operation is selected using the SYNC/MODE pin.

In FPWM Mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry. See the *Electrical Characteristics* for reverse current limit values.



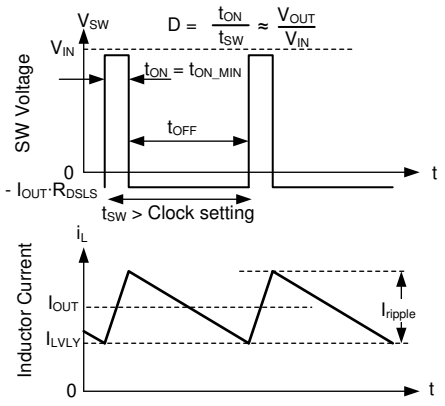
FPWM mode Continuous Conduction (CCM) is possible even if I_{OUT} is less than half of Iripple.

図 7-20. FPWM Mode Operation

In FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on-time, even while lightly loaded. This availability allows good behavior during faults which involves the output being pulled up.

7.4.3.4 Minimum On-time (High Input Voltage) Operation

The LM644A2-Q1 continues to regulate output voltage. This statement is true even if the input-to-output voltage ratio requires an on-time less than the minimum on-time of the chip with a given clock setting. This requirement is accomplished using valley current control. At all times, the compensation circuit dictates both a maximum peak inductor current and a maximum valley inductor current. If, for any reason, valley current is exceeded, the clock cycle is extended until valley current falls below that determined by the compensation circuit. If not operating in current limit, the maximum valley current is set above the peak inductor current. This prevents valley control from being used unless there is a failure to regulate using peak current only. If the input-voltage to output-voltage ratio is too high, even though current exceeds the peak value dictated by compensation, the high-side device cannot be turned off quickly enough to regulate output voltage. See t_{ON_MIN} in the *Electrical Characteristics*. As a result, the compensation circuit reduces both peak and valley current. After a low enough current is selected by the compensation circuit, valley current matches that being commanded by the compensation circuit. Under these conditions, the low-side device is kept on and the next clock cycle is prevented from starting until inductor current drops below the desired valley current. Because on-time is fixed at the minimum value, this type of operation resembles that of a device using a COT control scheme. See 図 7-21.

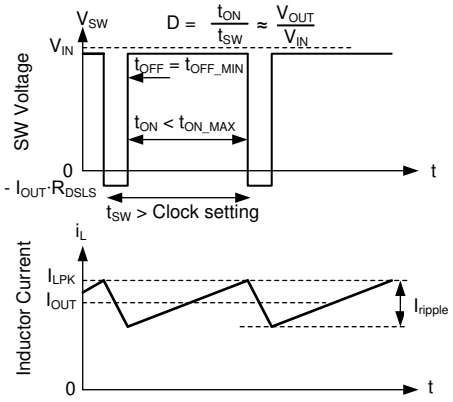


In valley control mode, the minimum inductor current is regulated, not peak inductor current.

図 7-21. Valley Current Mode Operation

7.4.3.5 Dropout

Dropout operation is defined as any input-to-output voltage ratio that requires frequency to drop to achieve the needed duty factor. At a given clock frequency, duty factor is limited by minimum off-time. After this limit is reached, if clock frequency is maintained, output voltage falls. Instead of allowing the output voltage to drop, the LM644A2-Q1 extends on-time past the end of the clock cycle until the required peak inductor current is achieved. The clock can start a new cycle after peak inductor current is achieved or after a pre-determined maximum on-time, t_{ON-MAX}, of approximately 9µs passes. As a result, after the needed duty factor cannot be achieved at the selected clock frequency due to the existence of a minimum off-time, frequency drops to maintain regulation. If input voltage is low enough that the output voltage cannot be regulated even with an on-time of t_{ON_MAX}, output voltage drops to slightly below input voltage.



This image shows the switching waveforms while in dropout. Inductor current takes longer than a normal clock to reach the desired peak value. As a result, frequency drops. This frequency drop is limited by t_{ON_MAX}.

図 7-22. Dropout Waveforms

7.4.3.6 Recovery from Dropout

In some applications, input voltage can drop below the desired output voltage then recover to a higher value suddenly. With most regulators, the sudden increase in input voltage results in output voltage rising at a rate limited only by current limit until regulation is achieved. As input voltage reaches the desired output voltage,

there is overshoot due to wind up in the control loop. This overshoot can be large in applications that have small output capacitors and light loads. Also, large inrush currents can cause large fluctuations on the input line after the regulator starts regulating the output voltage. This action typically requires less current than during this initial inrush.

The LM644A2-Q1 greatly reduces inrush current and overshoot. This reduction is done by engaging the soft-start circuit whenever the input voltage suddenly rises, after dipping low enough to cause the output voltage to droop. To prevent this feature from accidentally engaging, output voltage must fall more than 1% to engage this feature. Also, this feature engages only if operating in dropout or current limit, preventing interference with normal transient response but allowing several percent overshoot while engaging. If output voltage is very close to the desired level, overshoot is reduced by inductor current not having time to rise to a high level before regulation starts.

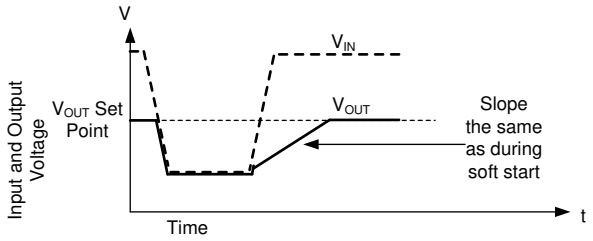


図 7-23. When Output Voltage Falls, Output Voltage Recovers Slowly, Preventing Overshoot and Large Inrush Currents

7.4.3.7 Other Fault Modes

Fault modes and descriptions can be found in セクション 7.3 of this data sheet.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The LM644A2-Q1 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current up to 12A per device. Maximum load current is dependent on the thermal environment of the design. The thermal performance curves for the EVM can be used as a starting point for determining load capability at different ambient temperatures.

The following design procedure can be used to select components for the LM644A2-Q1.

8.2 Typical Application

図 8-1 and 図 8-2 show typical application circuits for the LM644A2-Q1. The following design procedure can be used to select components for the LM644A2-Q1. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick start guide, 表 8-2 provides typical component values for some of the most common configurations. The values given in the table are typical. Other values can be used to enhance certain performance criterion as required by the application. Note that for this eQFN package, the input capacitors are split and placed on either side of the package. See セクション 8.2.2.5 for more details.

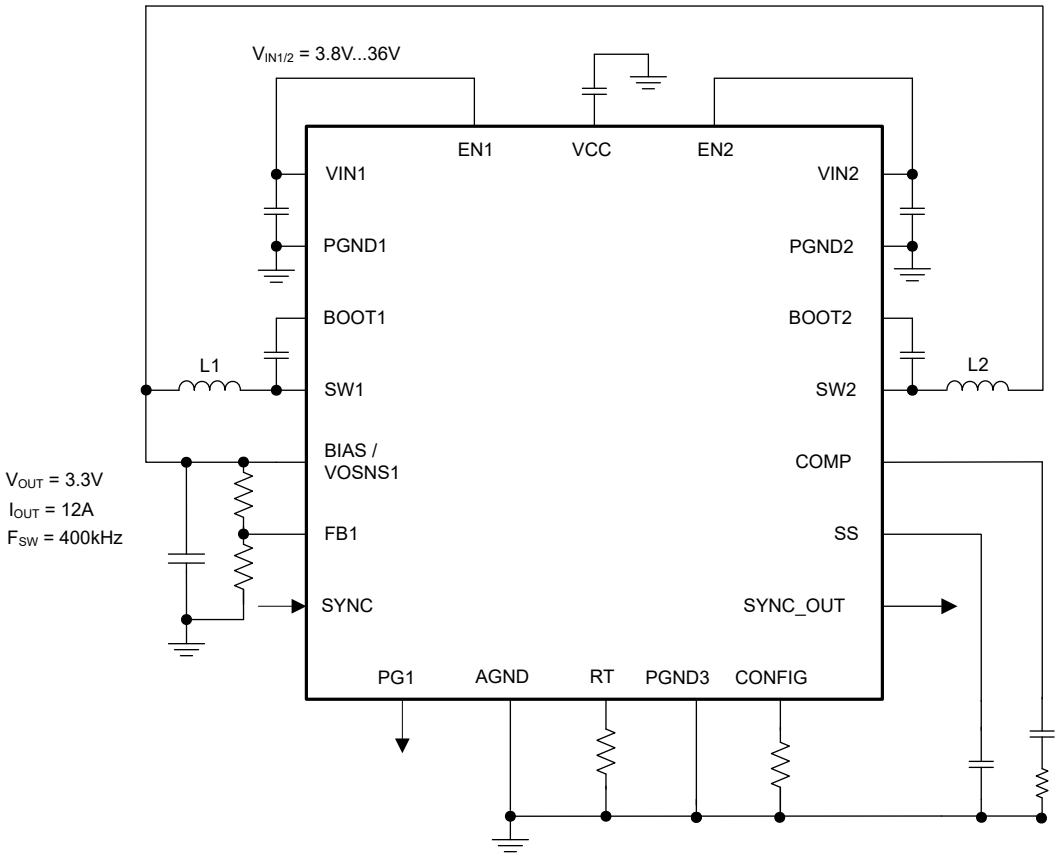


図 8-1. Example Application Circuit - 400kHz Single Adjustable Output

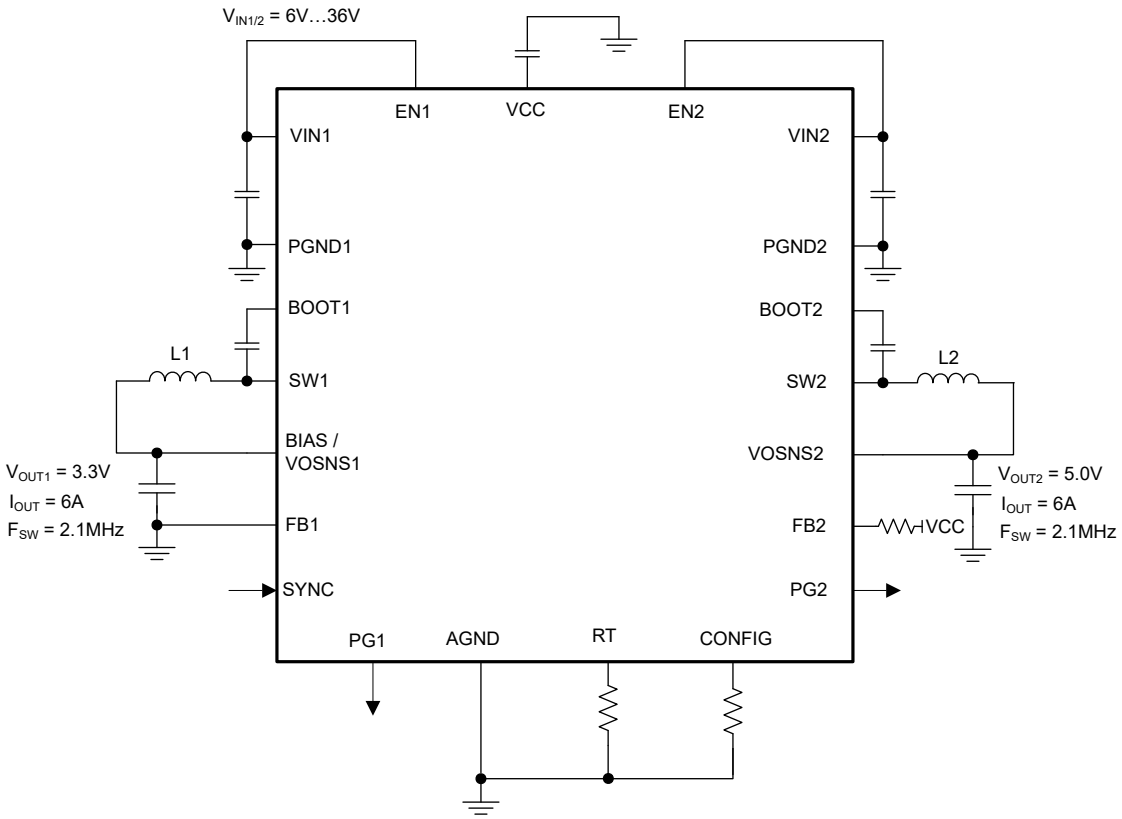


図 8-2. Example Application Circuit - 2.1MHz Dual Fixed Output

8.2.1 Design Requirements

表 8-1 provides the parameters for our detailed design procedure example for 図 8-2:

表 8-1. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	13.5V (6V to 36V)
Output voltage	3.3V and 5V fixed

8.2.2 Detailed Design Procedure

The following design procedure refers to 図 8-2, and 表 8-1.

8.2.2.1 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall design size. Lower switching frequency implies reduced switching losses, usually resulting in less power dissipated in the IC. Lower power dissipated in the IC results in higher system efficiency and a lower IC temperature. However, higher switching frequency allows the use of smaller inductors and output capacitors, hence, a more compact design. Many applications require that the AM band be avoided. These applications tend to operate at around 400kHz (below the AM band), or 2.1MHz (above the AM band). For 400kHz, a 39.2k 1% resistor can be used. For this 2100kHz example, a 7.15k 1% resistor is selected.

8.2.2.2 Setting the Output Voltage

The output regulation target can be programmed to a fixed 3.3V by connecting FB to AGND, or a fixed 5.0V output by connecting FB to VCC through a 10kΩ resistor. Also, the output voltage of the LM644A2-Q1 is externally adjustable using a resistor divider network. The divider network is comprised of the top and bottom feedback resistors, R_{FBT} and R_{FBB}, and closes the loop between the output voltage and the converter. The

converter regulates the output voltage by holding the voltage at the internal error amplifier input equal to the internal reference voltage, V_{FB} = 0.8V. The total resistance of the divider is a compromise between excessive noise pickup and excessive loading of the output. Lower resistance values reduce noise sensitivity but also reduce the light-load efficiency. The recommended value for R_{FBT} is around 100kΩ with a maximum value of 1MΩ.

8.2.2.3 Inductor Selection

The main parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current. The inductance is normally chosen to be in the range of 20% to 50% of the maximum output current. Experience shows that a good value for inductor ripple current is 30% of the maximum load current for systems with a fixed input voltage. This example uses V_{IN} = 13.5V, which is closer to the nominal voltage of a 12V car battery. When selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, the maximum device current must be used for this calculation. 式 5 can be used to determine the value of the inductance. The constant K is the percentage of peak-to-peak inductor current ripple to rated output current. For this 6A, 210kHz, 3.3V example, K = 0.25 is chosen and the closest standard value of 1µH was selected.

$$L = \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{V_{IN} - V_{OUT}}{f_{SW} \times K \times I_{OUT\_MAX}}\right) \quad (5)$$

The saturation current rating of the inductor must be at least as large as the high-side switch current limit, I_{HS}. This rating makes sure that the inductor does not saturate, even during a soft-short condition on the output. A hard short causes the LM644A2-Q1 to enter hiccup mode (see セクション 7.3.14). A soft short can hold the output current near the current limit without triggering hiccup. When the inductor core material saturates, the inductance can fall to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{LS}, is designed to reduce the risk of current runaway, a saturated inductor can cause the current to rise to high values very rapidly. This event can lead to component damage, so the inductor not saturating is crucial. Inductors with a ferrite core material have very hard saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a soft saturation, allowing some relaxation in the saturation current rating of the inductor. However, powered iron cores have more core losses at frequencies typically above 1MHz. To avoid subharmonic oscillation, the inductance value must not be less than that given in 式 6. The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

$$L > \left(\frac{V_{OUT}}{f_{SW} \times I_{RATED}}\right) \quad (6)$$

8.2.2.4 Output Capacitor Selection

The output capacitor value and ESR determine the output voltage ripple and load transient performance. The output capacitor is usually limited by the load transient requirements rather than the output voltage ripple. 表 8-2 can be used to find capacitor values for C_{OUT} and C_{FF} for a few common applications. Note that 4.99kΩ R_{FF} can be used in series with C_{FF} to limit high frequency noise into the FB pin. In this example, 3.3V_{OUT} and 2.1MHz, good transient performance is desired. From the table select 3 × 22µF ceramic as the output capacitor and 10pF as C_{FF}. For other voltage a frequency combinations Cout can be estimated using the desired crossover frequency (fx) and output voltage. Crossover is usually limited by the sampling pole created from the switching frequency. Thus, the crossover is usually a percentage such as 1/10th the switching frequency.

表 8-2. Selected Output Capacitor and C_{FF} Values

FREQUENCY	I_{OUT}	TRANSIENT PERFORMANCE	3.3V OUTPUT		5V OUTPUT	
			C_{OUT} (per phase)	C_{FF}	C_{OUT}	C_{FF}
400kHz	6A	Minimum	3 × 47µF ceramic		2 × 47µF ceramic	
400kHz	6A	Better Transient	4 × 47µF ceramic	10pF	3 × 47µF ceramic	10pF
2.1MHz	6A	Minimum	3 × 22µF ceramic		2 × 22µF ceramic	

表 8-2. Selected Output Capacitor and C_{FF} Values (続き)

FREQUENCY	I_{OUT}	TRANSIENT PERFORMANCE	3.3V OUTPUT		5V OUTPUT	
			C_{OUT} (per phase)	C_{FF}	C_{OUT}	C_{FF}
2.1MHz	6A	Better Transient	4 × 22µF ceramic	10pF	3 × 22µF ceramic	10pF

8.2.2.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 10µF ceramic capacitance is required at each input, ground pin pair of the LM644A2-Q1. Use 2 × 10µF ceramic capacitance or more for better EMI performance. This must be rated for at least the maximum input voltage that the application requires. Having twice the maximum input voltage to reduce DC bias derating is preferable. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size (0603 or 0402) ceramic capacitor can be used at each input, ground pin pair, VIN1/PGND1 and VIN2/PGND2. The capacitor must also have an X7R or better dielectric. Choose the highest capacitor value with these parameters. This choice provides a high frequency bypass to reduce switch-node ring and electromagnetic interference emissions. The eQFN (VBG) package provides two input voltage pins and two power ground pins on opposite sides of the package. This allows the input capacitors to be split and placed optimally with respect to the internal power MOSFETs, thus improving the effectiveness of the input bypassing. This example places two 10µF, 50V, 1206, X7R ceramic capacitors and two 0.1µF, 50V, 0402, X7R ceramic capacitors at each VIN/PGND pin pair.

Often, using an electrolytic capacitor on the input in parallel with the ceramics is desirable. This action is especially true if long leads/traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help dampen ringing on the input supply caused by the inductance of the long power leads. The use of this additional capacitor also helps with momentary voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitors. The approximate worst case RMS value of this current can be calculated with 式 7. This value must be checked against the manufacturer maximum ratings.

$$I_{RMS} \cong I_{OUT} \times \sqrt{\left(\frac{V_{OUT}}{V_{IN}}\right)} \quad (7)$$

8.2.2.6 BOOT Capacitor

The LM644A2-Q1 requires a bootstrap capacitor connected between the CBOOT pin and the SW pin. This capacitor stores energy which is used to supply the gate drivers for the power MOSFETs. TI recommends a high-quality, 100nF ceramic capacitor with a rating of at least 10V.

8.2.2.7 VCC

The VCC pin is the output of the internal LDO used as a supply to the internal control circuits of the regulator. This output requires a 1µF, 10V, X7R or similar, 0603 or similar ceramic capacitor connected from VCC to AGND for proper operation. Generally avoid loading this output with any external circuitry. However, this output can be used to supply the pullup for the PG pin (see セクション 7.3.7) as well as configuring the FB pin for fixed output voltages. A pullup resistor with value of 100kΩ is a good choice in this case. The nominal output voltage on VCC is 3.3V.

8.2.2.8 C_{FF} and R_{FF} Selection

A feedforward capacitor, C_{FF}, on the order of tens of picofarads and no bigger than 15nF, can be used to improve phase margin and transient response of circuits which have output capacitors with low ESR and tight voltage margin requirements. Because this C_{FF} capacitor can conduct noise from the output of the circuit directly to the FB node of the IC, a 4.99kΩ resistor, R_{FF}, can be placed in series with C_{FF} to lower high frequency susceptibility when used. If the ESR zero of the output capacitor is below 200kHz, no C_{FF} must be used. In general, the Cff capacitor can be sized to add phase boost slightly above the desired crossover frequency.

$$C_{FF} = \left(\frac{1}{2 \times \pi \times R_{FBT} \times f_X \times 1.5}\right) \quad (8)$$

If output voltage is less than 2.5V, C_{FF} has little effect, so can be omitted. If output voltage is greater than 14V, C_{FF} must be used cautiously because C_{FF} can easily introduce too much gain at higher frequencies.

If 1MΩ is selected for R_{FBT}, then a feedforward capacitor C_{FF} is usually required to offset parasitic capacitance in PCB construction.

8.2.2.9 SYNCHRONIZATION AND MODE

The SYNC pin allows you to synchronize the converter to an external clock voltage (SYNC). The pin also allows the selection between two modes. The following are the selectable modes:

- Forced pulse width modulation (FPWM) operation, which operates at a fixed frequency at all loads in typical operation
- Auto mode which automatically switches to pulse-frequency modulation (PFM) at light loads to improve light-load efficiency

Connect the SYNC pin to VCC through a 10kOhm resistor for FPWM. Connect to ground for PFM. You can also apply a clock signal to synchronize the switching frequency to an external clock. See セクション 7.3.4 for more information.

8.2.2.10 External UVLO

In some cases, the user can need an input undervoltage lockout (UVLO) level different than that provided internal to the device. This need can be accomplished by using the circuit shown in 図 7-2. The input voltage at which the device turns on is designated V_{ON} while the turn-off voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10kΩ to 100kΩ, then 式 1 is used to calculate R_{ENT} and V_{OFF}.

8.2.2.11 Typical Thermal Performance

The dual thermal pads of the LM644A2-Q1 allow the part to be cooled through the PCB and with a top side heatsink to extend the temperature range of the device. However, as with any power conversion device, the LM644A2-Q1 dissipates internal power while operating, so careful design of the thermal environment is important. The effect of this power dissipation is to raise the internal temperature of the converter above ambient temperature. The internal die temperature (T_J) is a function of the following:

- Ambient temperature
- Power loss
- Effective thermal resistance, $R_{\theta JA}$ of the device
- PCB layout

The maximum internal die temperature for the LM644A2-Q1 must be limited to 150°C. This limit establishes a limit on the maximum device power dissipation and, therefore, the load current. The following equation shows the relationships between the important parameters. Larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. For low ambient temperature designs the converter efficiency can be estimated by using the curves provided in the *Application Curves* section. If the desired operating conditions cannot be found in one of the curves, then the junction temperature can be roughly estimated using the EVM thermal performance as a starting point. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the Semiconductor and IC Package Thermal Metrics application note, the JEDEC value of $R_{\theta JA}$ given in the electrical characteristics table is not always valid for design purposes and must not be used to estimate the thermal performance of the device in a real application. Additionally, adding a heatsink to the top of the package will create a parallel thermal path through $R_{\theta JC(top)}$ and lower $R_{\theta JA}$ accordingly. The values reported in the electrical characteristics table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT\_MAX} = \left(\frac{T_J - T_A}{R_{\theta JA}} \times \frac{\eta}{(1-\eta)} \times \frac{1}{V_{OUT}}\right) \quad (9)$$

where

- η = efficiency
- T_A = ambient temperature
- T_J = junction temperature
- $R_{\theta JA}$ = the effective thermal resistance of the IC junction to the air, mainly through the PCB

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors (just to mention a few of the most critical parameters:

- Power dissipation
- Air temperature
- Airflow
- PCB area
- Copper heat-sink area
- Number of thermal vias under or near the package
- Adjacent component placement

A typical curve of maximum output current versus ambient temperature is shown in 図 8-3 and 図 8-4 for a good thermal layout. This data is calculated using the $R_{\theta JA}$ of the EVM without a heatsink and adding the calculated effect of a HSB43-454515P heatsink under either natural convection or airflow conditions. Remember that the data given in these graphs are for illustration purposes only, and the actual performance in any given application depends on all of the previously mentioned factors.

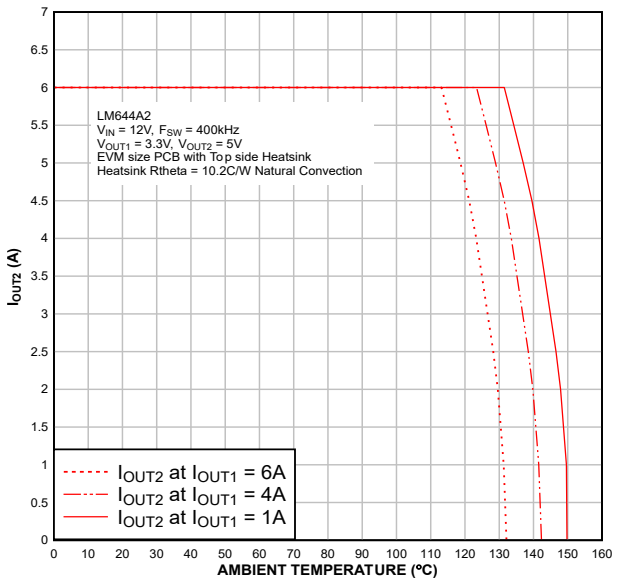


図 8-3. Typical Output Current vs Ambient Temperature, V_{IN} = 12V F_{SW} = 400kHz, Dual Output

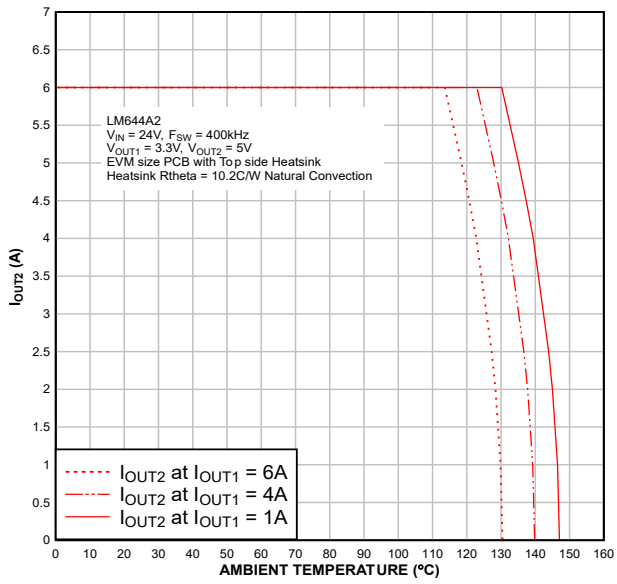


図 8-4. Typical Output Current vs Ambient Temperature, V_{IN} = 24V F_{SW} = 400kHz, Dual Output

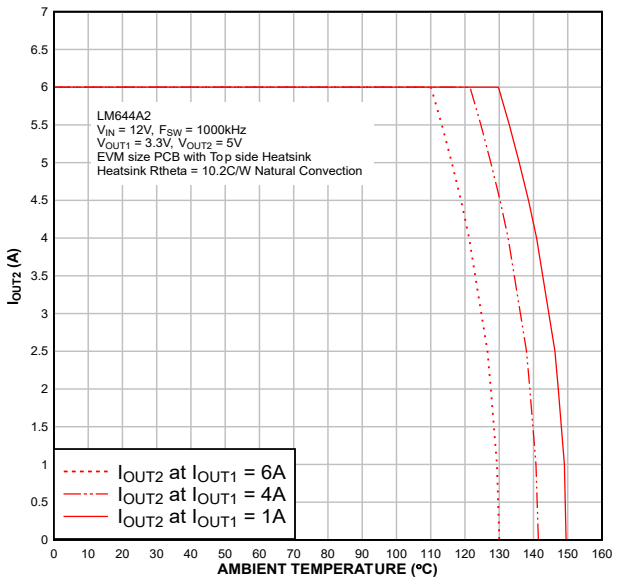


図 8-5. Typical Output Current versus Ambient Temperature, V_{IN} = 12V F_{SW} = 1MHz, Dual Output

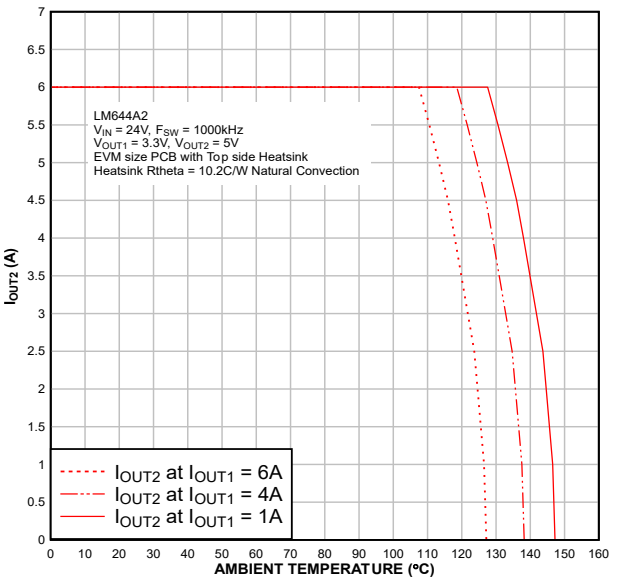


図 8-6. Typical Output Current vs Ambient Temperature, V_{IN} = 24V F_{SW} = 1MHz, Dual Output

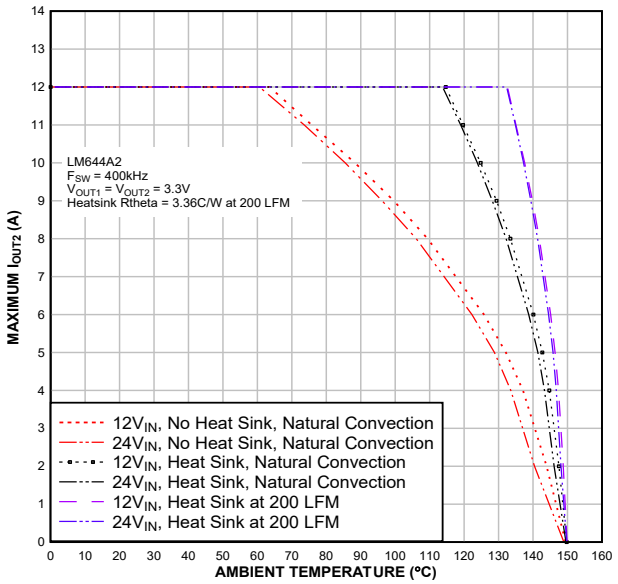


図 8-7. Typical Output Current vs Ambient Temperature, F_{SW} = 400kHz, Single Output

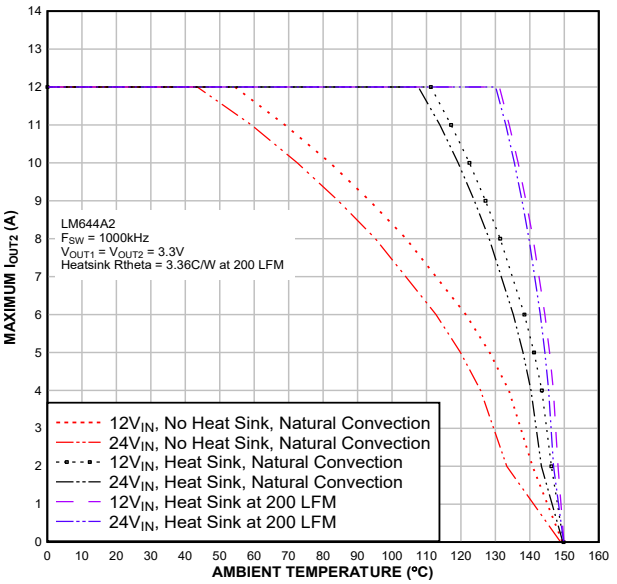


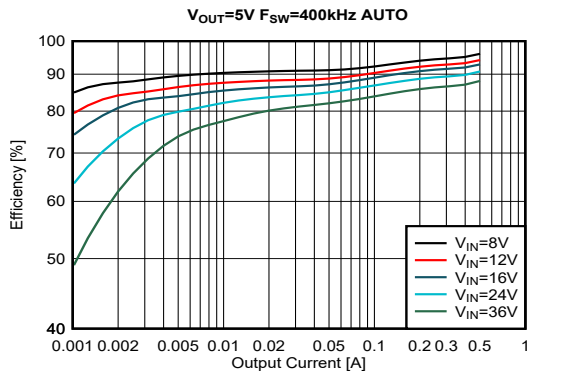
図 8-8. Typical Output Current versus Ambient Temperature, F_{SW} = 1MHz, Single Output

Use the following resources as a guide to excellent thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight* application note
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application note
- *Semiconductor and IC Package Thermal Metrics* application note
- *Quick Reference Guide To TI Buck Switching DC/DC application note*

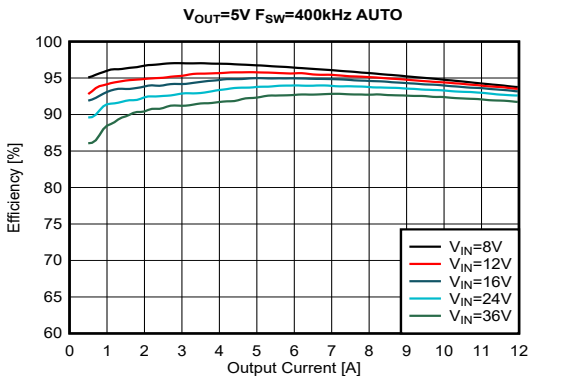
8.2.3 Application Curves

Unless otherwise specified, the following conditions apply: Device: LM644A2-Q1, V_{IN} = 13.5V, T_A = 25°C. The circuit is shown in 図 8-1, and 図 8-2 with the appropriate BOM from 表 8-3. No heatsink was attached during radiated emissions tests.



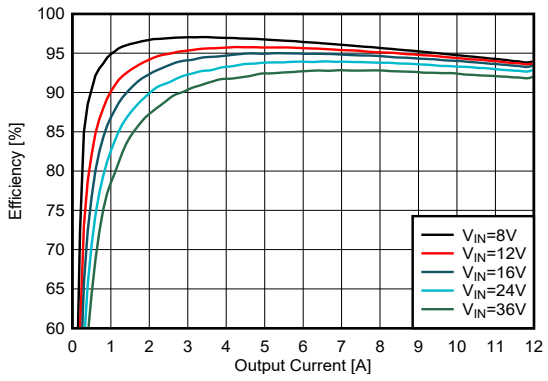
V_{OUT} = 5V F_{SW} = 400kHz Auto mode Single Output

図 8-9. Efficiency



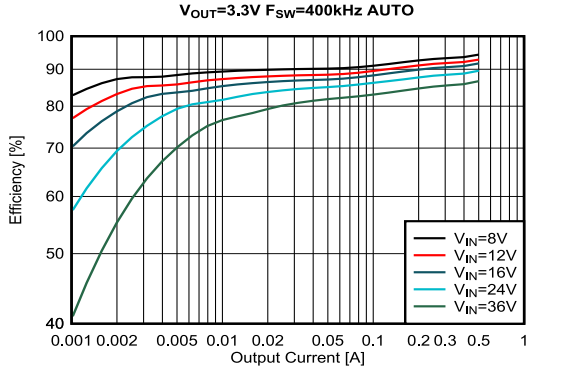
V_{OUT} = 5V F_{SW} = 400kHz Auto mode Single Output

図 8-10. Efficiency



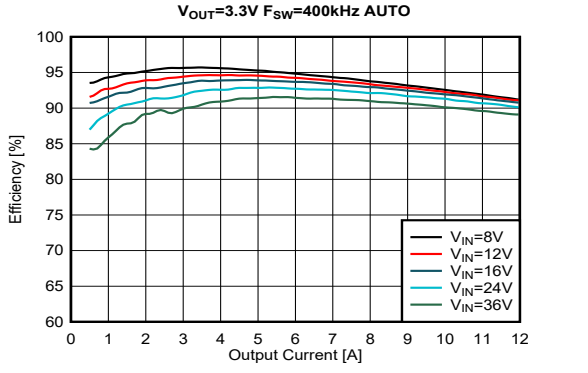
V_{OUT} = 5V F_{SW} = 400kHz FPWM mode Single Output

図 8-11. Efficiency



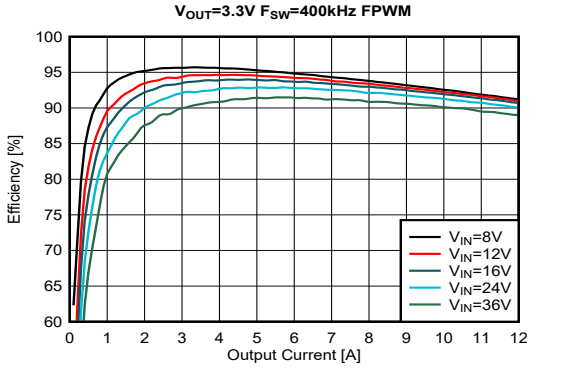
V_{OUT} = 3.3V F_{SW} = 400kHz Auto mode Single Output

図 8-12. Efficiency



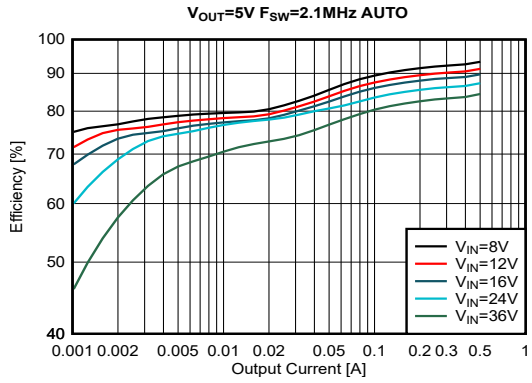
V_{OUT} = 3.3V F_{SW} = 400kHz Auto mode Single Output

図 8-13. Efficiency



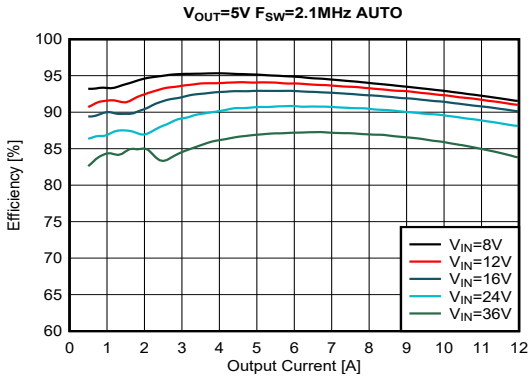
V_{OUT} = 3.3V F_{SW} = 400kHz FPWM mode Single Output

図 8-14. Efficiency



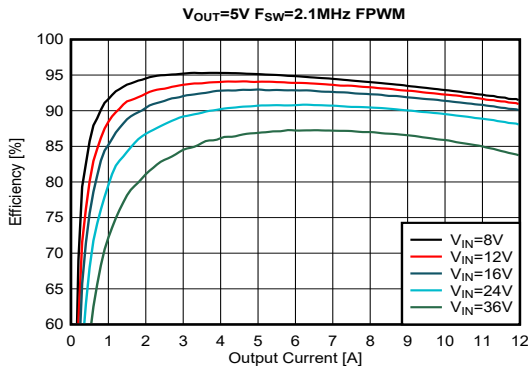
V_{OUT} = 5V F_{SW} = 2.1MHz Auto mode Single Output

図 8-15. Efficiency



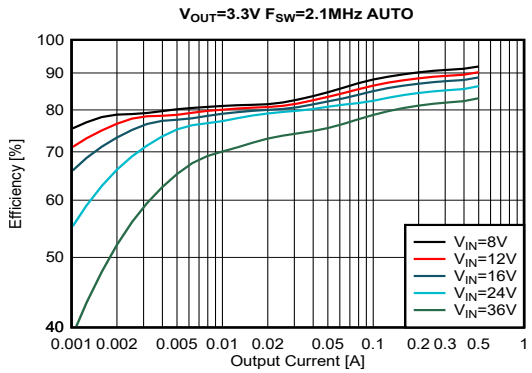
V_{OUT} = 5V F_{SW} = 2.1MHz Auto mode Single Output

図 8-16. Efficiency



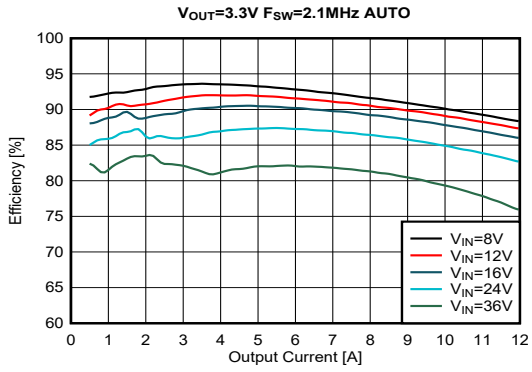
V_{OUT} = 5V F_{SW} = 2.1MHz FPWM mode Single Output

図 8-17. Efficiency



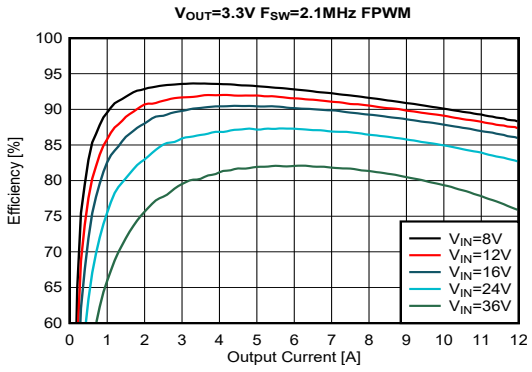
V_{OUT} = 3.3V F_{SW} = 2.1MHz Auto mode Single Output

図 8-18. Efficiency



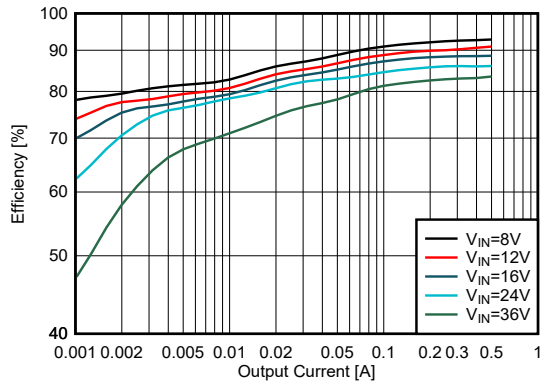
V_{OUT} = 3.3V F_{SW} = 2.1MHz Auto mode Single Output

図 8-19. Efficiency



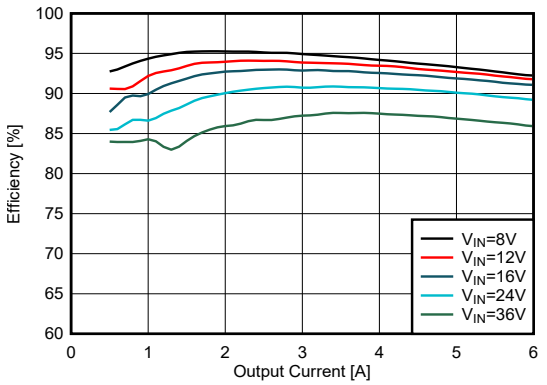
V_{OUT} = 3.3V F_{SW} = 2.1MHz FPWM mode Single Output

図 8-20. Efficiency



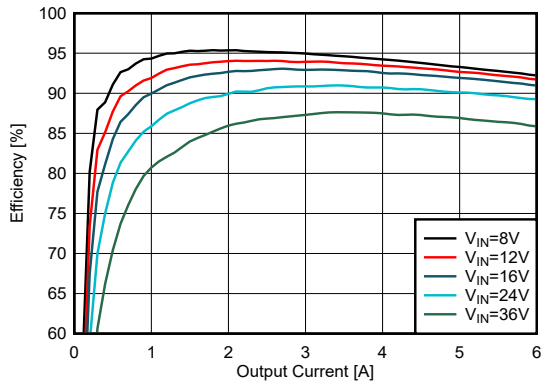
V_{OUT} = 5V F_{SW} = 2.1MHz Auto mode Dual Output

図 8-21. Efficiency



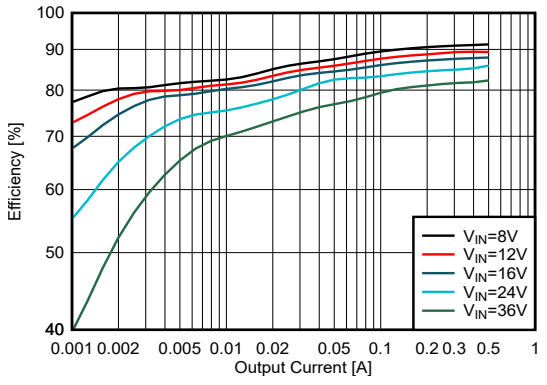
V_{OUT} = 5V F_{SW} = 2.1MHz Auto mode Dual Output

図 8-22. Efficiency



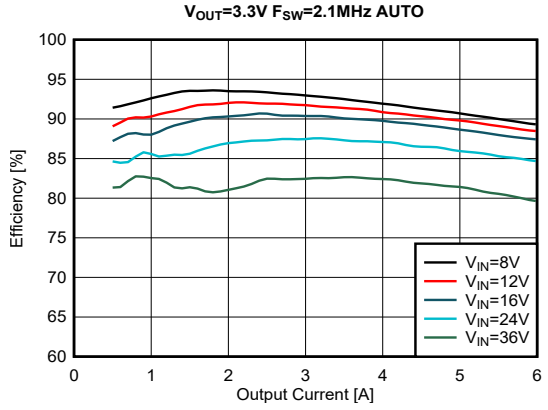
V_{OUT} = 5V F_{SW} = 2.1MHz FPWM mode Dual Output

図 8-23. Efficiency



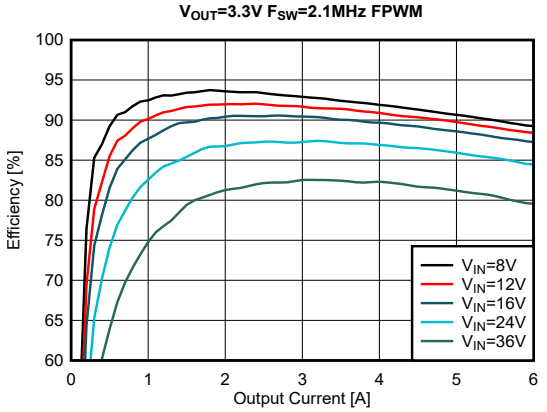
V_{OUT} = 3.3V F_{SW} = 2.1MHz Auto mode Dual Output

図 8-24. Efficiency



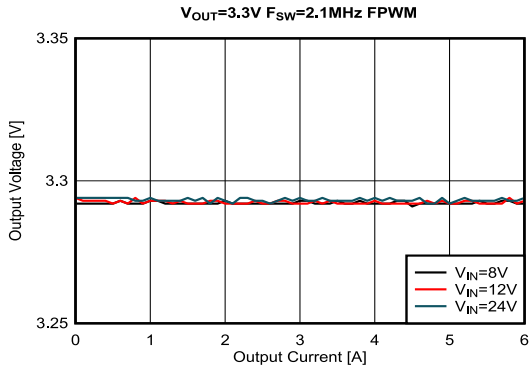
V_{OUT} = 3.3V F_{SW} = 2.1MHz Auto mode Dual Output

図 8-25. Efficiency



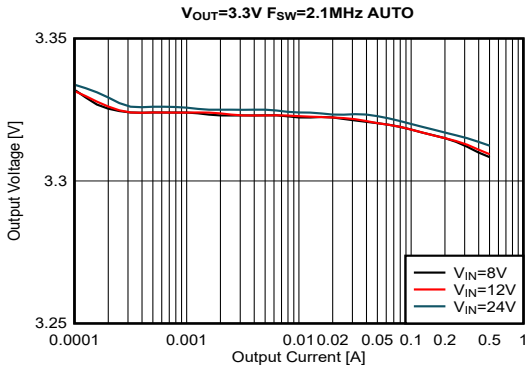
V_{OUT} = 3.3V F_{SW} = 2.1MHz FPWM mode Dual Output

図 8-26. Efficiency



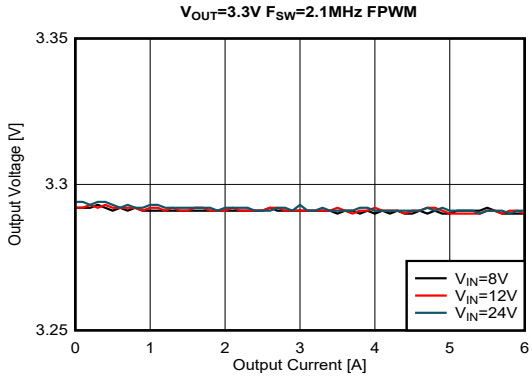
V_{OUT} = 3.3V F_{SW} = 2.1MHz FPWM mode Single Output

図 8-27. Load and Line Regulation



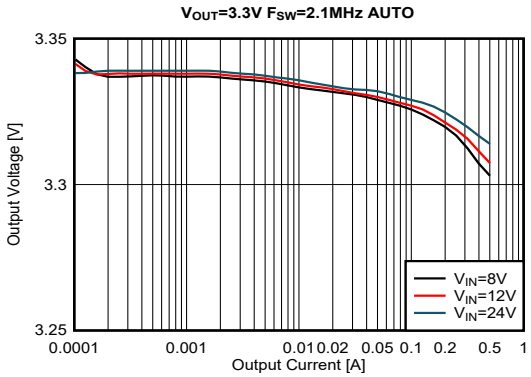
V_{OUT} = 3.3V F_{SW} = 2.1MHz Auto mode Single Output

図 8-28. Load and Line Regulation



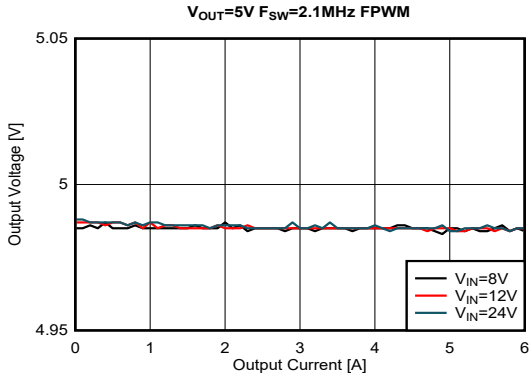
V_{OUT} = 3.3V F_{SW} = 2.1MHz FPWM mode Dual Output

図 8-29. Load and Line Regulation



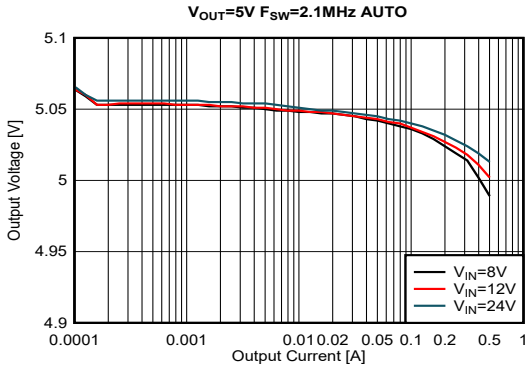
V_{OUT} = 3.3V F_{SW} = 2.1MHz Auto mode Dual Output

図 8-30. Load and Line Regulation



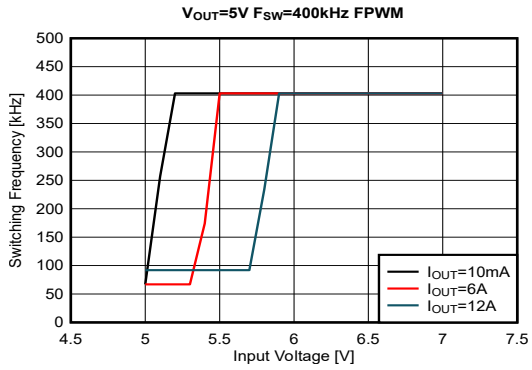
V_{OUT} = 5V F_{SW} = 2.1MHz FPWM mode Dual Output

図 8-31. Load and Line Regulation



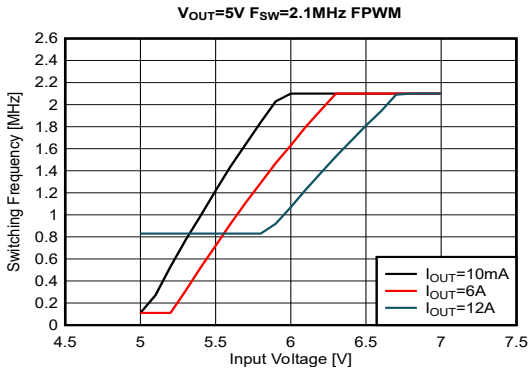
V_{OUT} = 5V F_{SW} = 2.1MHz Auto mode Dual Output

図 8-32. Load and Line Regulation



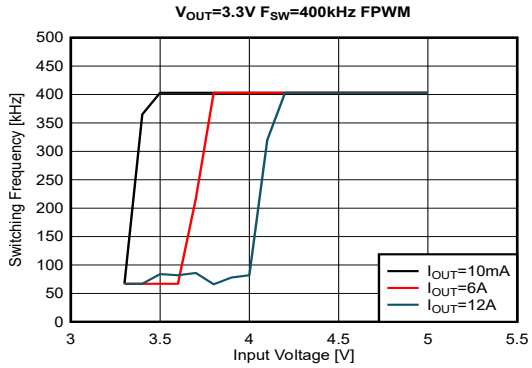
V_{OUT} = 5V F_{SW} = 400kHz FPWM mode Single Output

図 8-33. Dropout



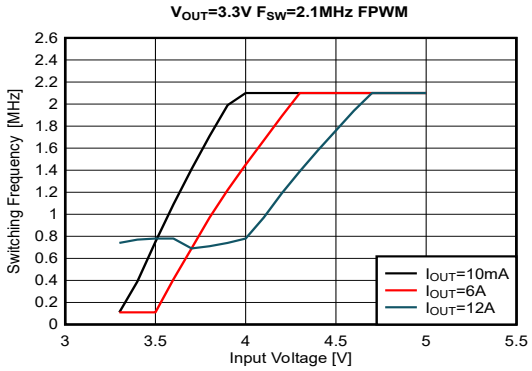
V_{OUT} = 5V F_{SW} = 2.1MHz FPWM mode Single Output

図 8-34. Dropout



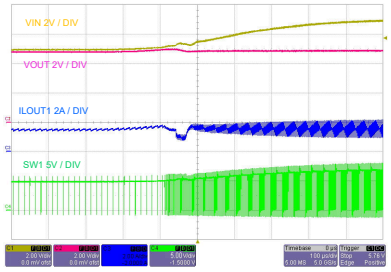
V_{OUT} = 3.3V F_{SW} = 400kHz FPWM mode Single Output

図 8-35. Dropout



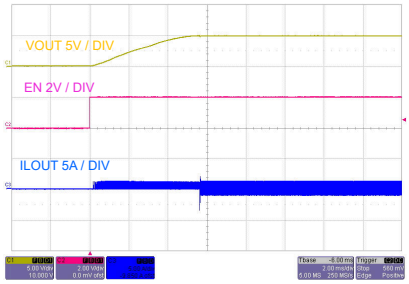
V_{OUT} = 3.3V F_{SW} = 2.1MHz FPWM mode Single Output

図 8-36. Dropout



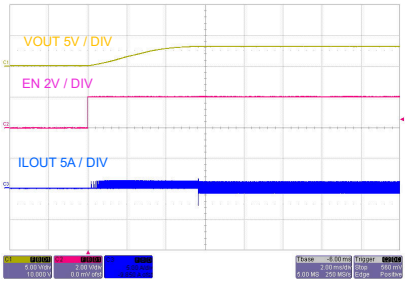
V_{OUT} = 5V F_{SW} = 400kHz Auto mode
I_{OUT} = 3A V_{IN} = 5 to 7V Single Output

図 8-37. Dropout Recovery



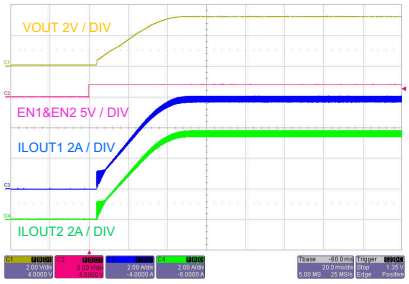
V_{OUT} = 5V F_{SW} = 400kHz FPWM mode
I_{OUT} = 100mA V_{IN} = 13.5V Dual Output

図 8-38. Start-Up With 100mA Load



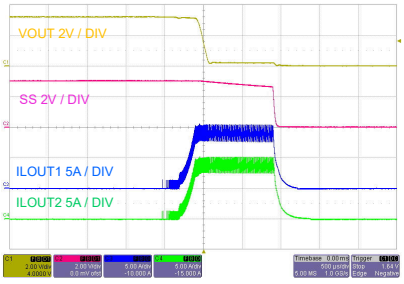
V_{OUT} = 3.3V
I_{OUT} = 100mA
F_{SW} = 400kHz
V_{IN} = 13.5V
FPWM mode
Dual Output

図 8-39. Start-Up With 100mA Load



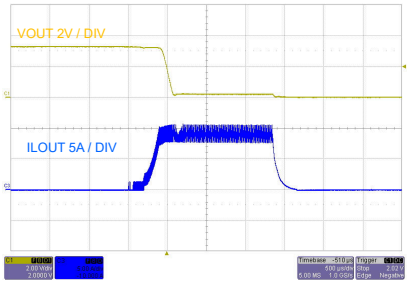
V_{OUT} = 3.3V
I_{OUT} = 12A
F_{SW} = 400kHz
V_{IN} = 13.5V
FPWM mode
Single Output

図 8-40. Start-Up With 12A Load



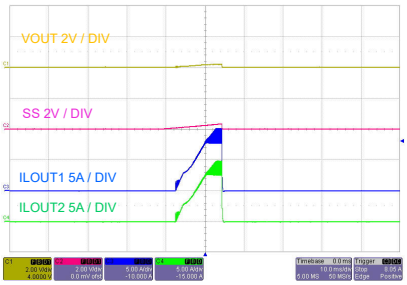
V_{OUT} = 3.3V
I_{OUT} = 0A to short circuit
F_{SW} = 400kHz
V_{IN} = 13.5V
Auto mode
Single Output

図 8-41. Short-Circuit Protection



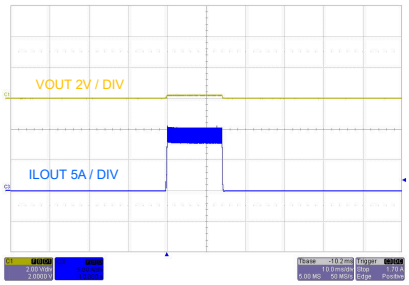
V_{OUT1} = 3.3V
I_{OUT} = 0A to short circuit
F_{SW} = 400kHz
V_{IN} = 13.5V
Auto mode
Dual Output

図 8-42. Short-Circuit Protection



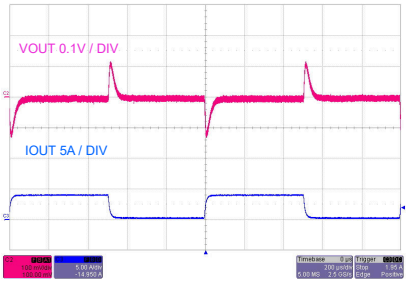
V_{OUT} = 3.3V
I_{OUT} = short circuit to 0A
F_{SW} = 400kHz
V_{IN} = 13.5V
Auto mode
Single Output

図 8-43. Short-Circuit Hiccup



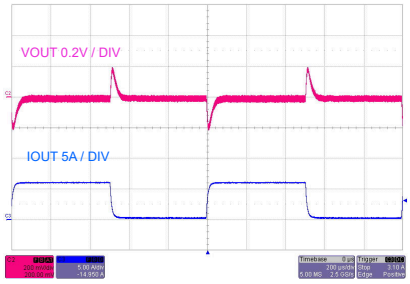
V_{OUT} = 3.3V
I_{OUT} = short circuit to 0A
F_{SW} = 400kHz
V_{IN} = 13.5V
Auto mode
Dual Output

図 8-44. Short-Circuit Hiccup



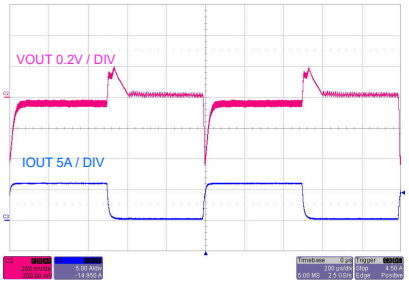
V_{OUT} = 5V
I_{OUT} = 100mA to 6A to 100mA
F_{SW} = 2.1MHz
V_{IN} = 13.5V
FPWM mode
Dual Output

図 8-45. Load Transient



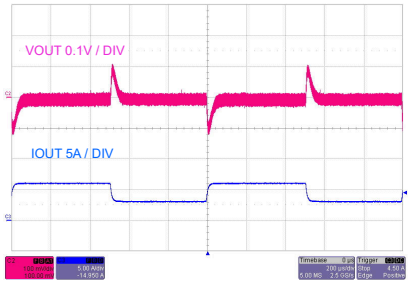
V_{OUT} = 5V
I_{OUT} = 100mA to 6A to 100mA
F_{SW} = 400kHz
V_{IN} = 13.5V
FPWM mode
Dual Output

図 8-46. Load Transient



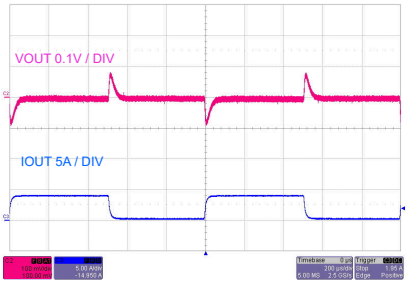
V_{OUT} = 5V
I_{OUT} = 100mA to 6A to 100mA
F_{SW} = 400kHz
V_{IN} = 13.5V
Auto mode
Dual Output

図 8-47. Load Transient



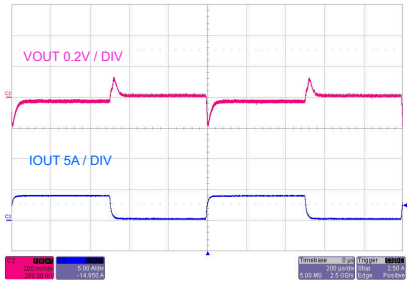
V_{OUT} = 5V
I_{OUT} = 3A to 6A to 3A
F_{SW} = 400kHz
V_{IN} = 13.5V
FPWM mode
Dual Output

図 8-48. Load Transient



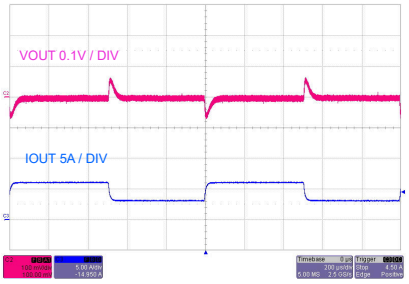
V_{OUT} = 3.3V
I_{OUT} = 100mA to 6A to 100mA
F_{SW} = 2.1MHz
V_{IN} = 13.5V
FPWM mode
Dual Output

図 8-49. Load Transient



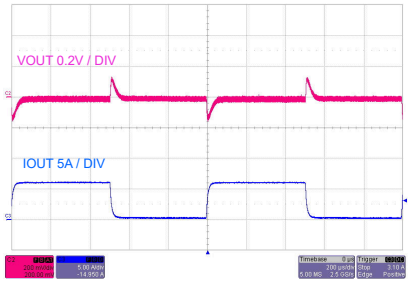
V_{OUT} = 3.3V
I_{OUT} = 100mA to 6A to 100mA
F_{SW} = 2.1MHz
V_{IN} = 13.5V
Auto mode
Dual Output

図 8-50. Load Transient



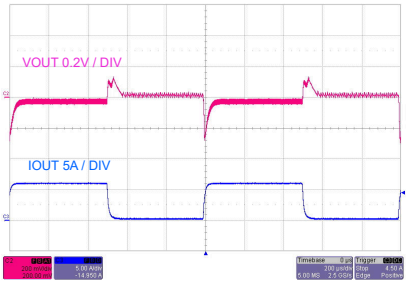
V_{OUT} = 3.3V
I_{OUT} = 3A to 6A to 3A
F_{SW} = 2.1MHz
V_{IN} = 13.5V
FPWM mode
Dual Output

図 8-51. Load Transient



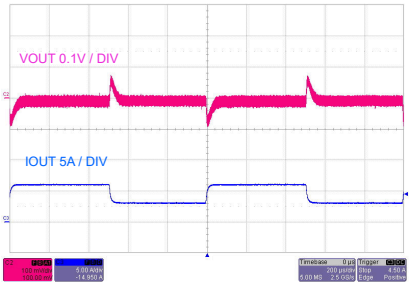
V_{OUT} = 3.3V
I_{OUT} = 100mA to 6A to 100mA
F_{SW} = 400kHz
V_{IN} = 13.5V
FPWM mode
Dual Output

図 8-52. Load Transient



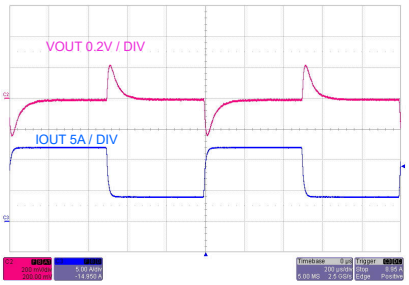
V_{OUT} = 3.3V
I_{OUT} = 100mA to 6A to 100mA
F_{SW} = 400kHz
V_{IN} = 13.5V
Auto mode
Dual Output

図 8-53. Load Transient



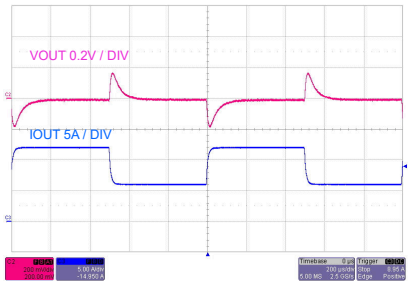
V_{OUT} = 3.3V
I_{OUT} = 3A to 6A to 3A
F_{SW} = 400kHz
V_{IN} = 13.5V
FPWM mode
Dual Output

図 8-54. Load Transient



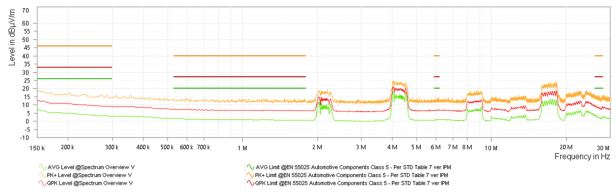
V_{OUT} = 3.3V
I_{OUT} = 4A to 12A to 4A
F_{SW} = 400kHz
V_{IN} = 13.5V
FPWM mode
Single Output

図 8-55. Load Transient



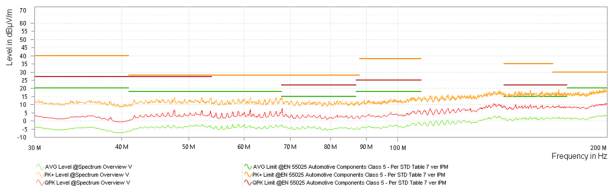
V_{OUT} = 3.3V
I_{OUT} = 6A to 12A to 4A
F_{SW} = 400kHz
V_{IN} = 13.5V
FPWM mode
Single Output

図 8-56. Load Transient



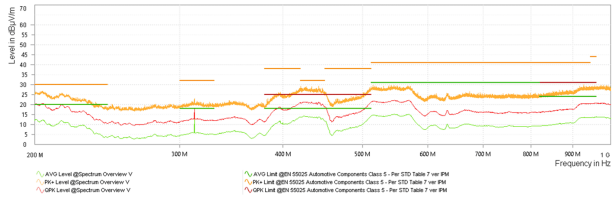
V_{OUT} = 3.3V F_{SW} = 2100kHz I_{OUT} = 12A
Frequency tested: 150kHz to 30MHz

図 8-57. Single Output Monopole Radiated Emissions vs CISPR25 Class 5 Limits (Orange: Peak Signal, Red: Average Signal, Green: Quasi-Peak Signal)



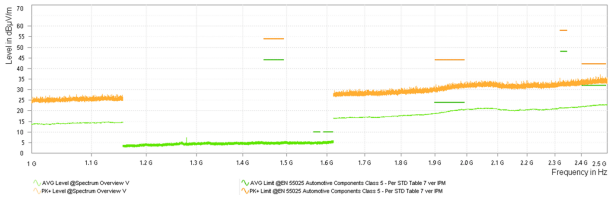
V_{OUT} = 3.3V F_{SW} = 2100kHz I_{OUT} = 12A
Frequency tested: 30MHz to 200MHz

図 8-58. Single Output Bicon Radiated Emissions vs CISPR25 Class 5 Limits (Orange: Peak Signal, Red: Average Signal, Green: Quasi-Peak Signal)



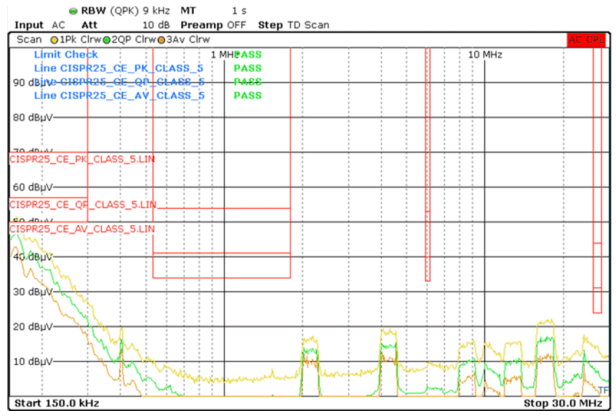
V_{OUT} = 3.3V F_{SW} = 2100kHz I_{OUT} = 12A
Frequency tested: 200MHz to 1000MHz

図 8-59. Single Output Log Radiated Emissions vs CISPR25 Class 5 Limits (Orange: Peak Signal, Red: Average Signal, Green: Quasi-Peak Signal)



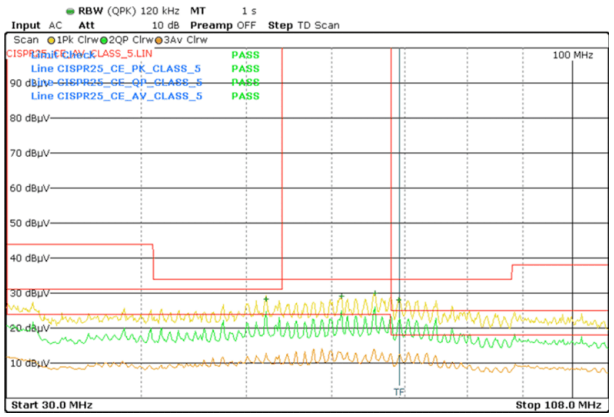
V_{OUT} = 3.3V F_{SW} = 2100kHz I_{OUT} = 12A
Frequency tested: 1000MHz to 2500MHz

図 8-60. Single Output Horn Radiated Emissions vs CISPR25 Class 5 Limits (Orange: Peak Signal, Red: Average Signal, Green: Quasi-Peak Signal)



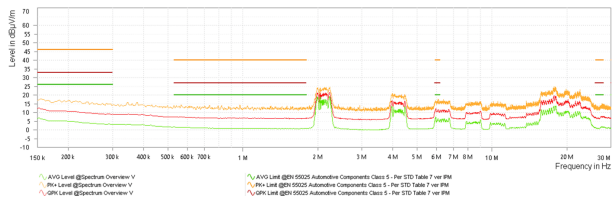
V_{OUT} = 3.3V F_{SW} = 2100kHz I_{OUT} = 12A
Frequency tested: 150kHz to 30MHz

図 8-61. Single Output Conducted Emissions vs CISPR25 Class 5 Limits (Orange: Peak Signal, Red: Average Signal, Green: Quasi-Peak Signal)



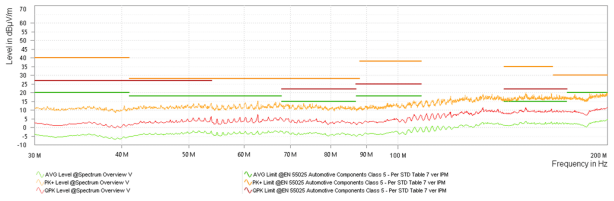
V_{OUT} = 3.3V F_{SW} = 2100kHz I_{OUT} = 12A
Frequency tested: 30MHz to 108MHz

図 8-62. Single Output Conducted Emissions vs CISPR25 Class 5 Limits (Orange: Peak Signal, Red: Average Signal, Green: Quasi-Peak Signal)



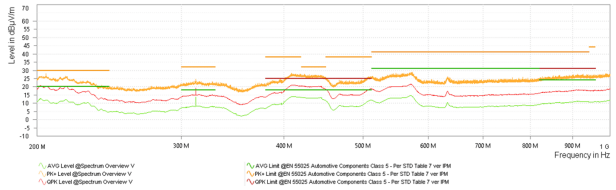
V_{OUT} = 3.3V F_{SW} = 2100kHz I_{OUT} = 12A
Frequency tested: 150kHz to 30MHz

図 8-63. Dual Output Monopole Radiated Emissions vs CISPR25 Class 5 Limits (Orange: Peak Signal, Red: Average Signal, Green: Quasi-Peak Signal)



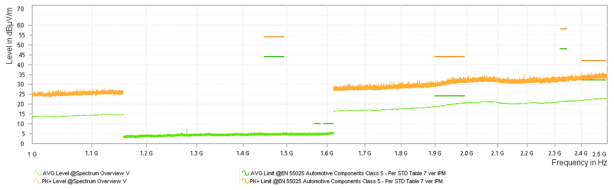
V_{OUT} = 3.3V F_{SW} = 2100kHz I_{OUT} = 12A
Frequency tested: 30MHz to 200MHz

図 8-64. Dual Output Bicon Radiated Emissions vs CISPR25 Class 5 Limits (Orange: Peak Signal, Red: Average Signal, Green: Quasi-Peak Signal)



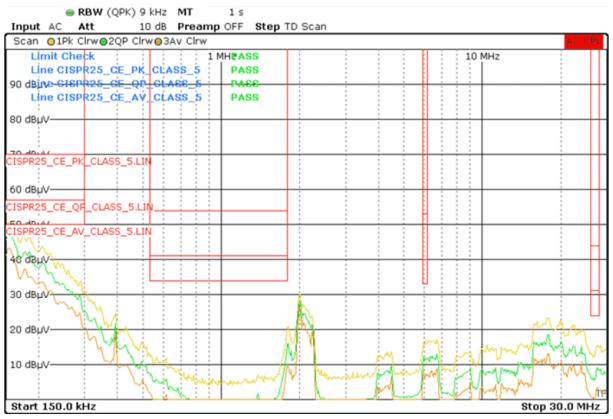
V_{OUT} = 3.3V F_{SW} = 2100kHz I_{OUT} = 12A
Frequency tested: 200MHz to 1000MHz

図 8-65. Dual Output Log Radiated Emissions vs CISPR25 Class 5 Limits (Orange: Peak Signal, Red: Average Signal, Green: Quasi-Peak Signal)



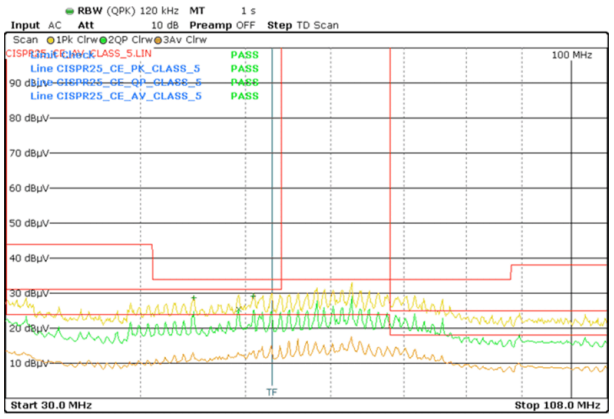
V_{OUT} = 3.3V F_{SW} = 2100kHz I_{OUT} = 12A
Frequency tested: 1000MHz to 2500MHz

図 8-66. Dual Output Horn Radiated Emissions vs CISPR25 Class 5 Limits (Orange: Peak Signal, Red: Average Signal, Green: Quasi-Peak Signal)



V_{OUT} = 3.3V F_{SW} = 2100kHz I_{OUT} = 12A
Frequency tested: 150kHz to 30MHz

図 8-67. Dual Output Conducted Emissions versus CISPR25 Class 5 Limits (Orange: Peak Signal, Red: Average Signal, Green: Quasi-Peak Signal)



V_{OUT} = 3.3V F_{SW} = 2100kHz I_{OUT} = 12A
Frequency tested: 30MHz to 108MHz

図 8-68. Dual Output Conducted Emissions versus CISPR25 Class 5 Limits (Orange: Peak Signal, Red: Average Signal, Green: Quasi-Peak Signal)

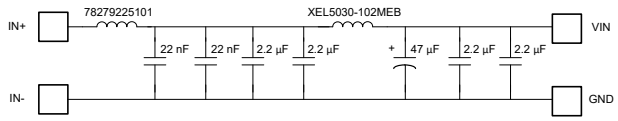


図 8-69. Recommended Input EMI Filter

表 8-3. BOM for Typical Application Curves

V_{OUT}	FREQUENCY	R_{FBB}	C_{OUT} EACH PHASE	C_{IN} + C_{HF} EACH PHASE	L	C_{FF}FOR ADJUSTABLE OUTPUT
3.3V	400kHz	32.4kΩ	47 + 22µF	2 × 10µF + 1 × 100nF	2.8µH	10pF
3.3V	2200kHz	32.4kΩ	47 + 22µF	2 × 10µF + 1 × 100nF	1µH	10pF
5V	400kHz	19.1kΩ	47 + 22µF	2 × 10µF + 1 × 100nF	2.8µH	10pF
5V	2200kHz	19.1kΩ	47 + 22µF	2 × 10µF + 1 × 100nF	1µH	10pF

8.3 Power Supply Recommendations

The characteristics of the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with 式 10.

$$I_{IN} \cong \frac{I_{OUT}}{\eta} \times \left(\frac{V_{OUT}}{V_{IN}}\right) \tag{10}$$

where

- η is the efficiency

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR ceramic input capacitors, can form an underdamped resonant circuit. This can result in overvoltage transients at the input to the regulator or tripping UVLO. Consider that the supply voltage can dip when a load transient is applied to the output depending on the parasitic resistance and inductance of the harness and characteristics of the supply. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kinds of issues is to reduce the distance from the input supply to the regulator. Additionally, use an aluminum input capacitor in parallel with the ceramics. The moderate ESR of this type of capacitor helps damp the input resonant circuit and reduce any overshoots or undershoots. A value in the range of 20µF to 100µF is usually sufficient to provide input damping and help hold the input voltage steady during large load transients.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a snap-back characteristic (thyristor type). TI does not recommend to use a device with this type of characteristic. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharge through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then use a Schottky diode between the input supply and the output.

8.4 Layout

8.4.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the excellent performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced.

Furthermore, the EMI performance of the regulator is dependent on the PCB layout to a great extent. In a buck converter, the most EMI-critical PCB feature is the loop formed by the input capacitor or capacitors and power ground. This loop is shown in 図 8-70. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. Excessive transient voltages can disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short while keeping the loop area as small as possible to reduce the parasitic inductance. 図 8-71 shows a recommended layout for the critical components of the LM644A2-Q1 circuit.

- *Place the input capacitor or capacitors as close as possible to the input pin pairs*: VIN1 to PGND1 and VIN2 to PGND2. Place the small capacitors closest. Each pair of pins are adjacent, simplifying the input capacitor placement. With the QFN package, there are two VIN/PGND pairs on either side of the package. This provides a symmetrical layout and helps minimize switching noise and EMI generation. Use a wide VIN plane on a mid-layer to connect both of the VIN pairs together to the input supply. Route symmetrically from the supply to each VIN pin to best use the benefits of the symmetric pinout.
- *Place the bypass capacitor for VCC close to the VCC pin and AGND pin:* This capacitor must be routed with short, wide traces to the VCC and AGND pins.
- *Place the CBOOT capacitors as close as possible to the device with short, wide traces to the CBOOT and SW pins:* Make sure to route the SW connection with a short wide trace to handle the current, but not longer than necessary to avoid generating common mode noise.
- *Place the feedback divider as close as possible to the FB pin of the device*: Place R_{FBB}, R_{FBT}, C_{FF} if used, and R_{FF} if used, physically close to the device. The connections to FB and AGND through R_{FBB} must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
- *Make layer 2 of the PCB a ground plane*: This plane acts as a noise shield and as a heat dissipation path. Using layer 2 reduces the enclosed area in the input circulating current in the input loop, reducing inductance.
- *Provide wide paths for V_{IN}, V_{OUT}, and GND*: These paths must be as wide and direct as possible to reduce any voltage drops on the input or output paths of the converter to maximize efficiency.
- *Provide enough PCB area for proper heat sinking*: Enough copper area must be used to make sure a low $R_{\theta JA}$, considering maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes. Note that the package of this device dissipates heat through all pins. Wide traces can be used for all pins except where noise considerations dictate minimization of area.
- *Keep the switch area small*: Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

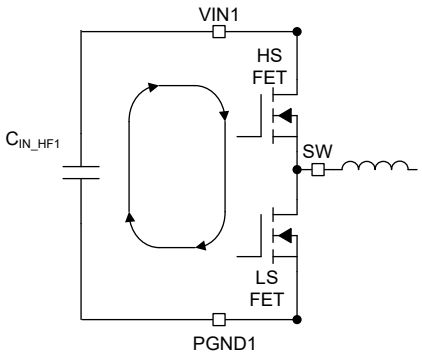


図 8-70. Input Current Loop

8.4.1.1 Ground and Thermal Considerations

As mentioned above, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. A ground plane also provides a quiet reference potential for the control circuitry. The AGND and PGND pins must be connected to the ground planes using vias next to the

bypass capacitors. PGND pins connect directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground plane. The other side of the ground plane contains much less noise and can be used for sensitive traces.

TI recommends providing adequate device heat sinking by using vias near PGND and VIN pins to connect to the system ground plane or V_{IN} strap, both of which dissipate heat. Use as much copper as possible for the system ground plane on the top and bottom layers and avoid plane cuts and bottlenecks for the heat flow for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2oz / 1oz / 1oz / 2oz. A four-layer board with enough copper thickness and proper layout provides low current conduction impedance, proper shielding, and low thermal resistance.

8.4.2 Layout Example

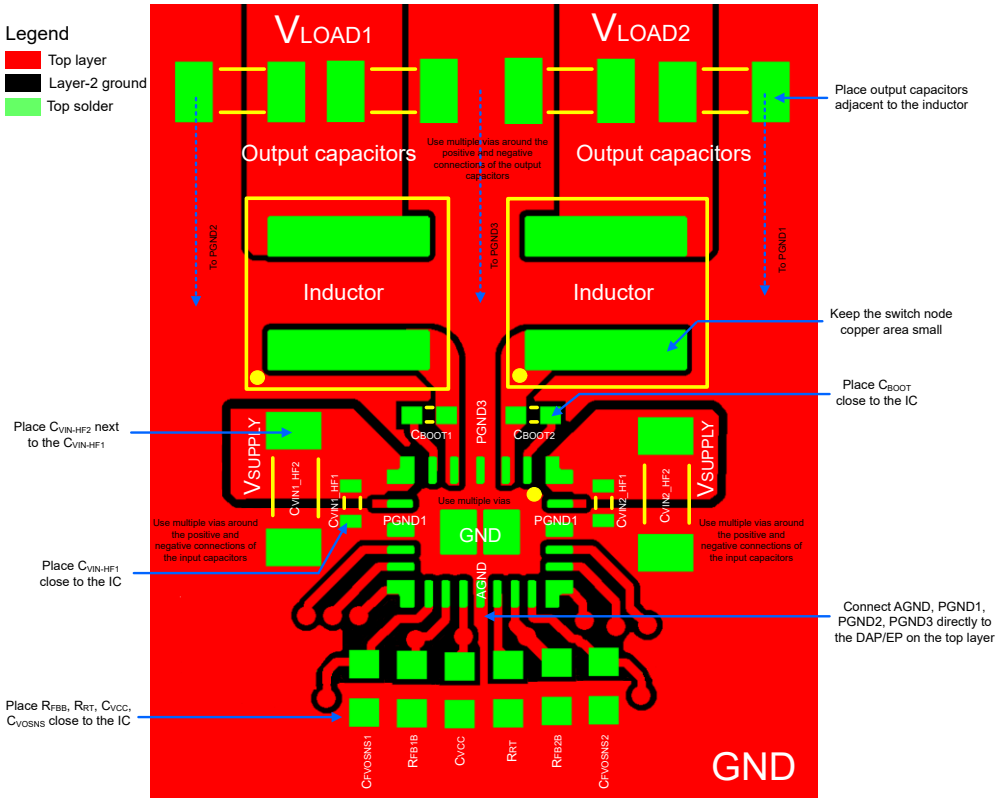


図 8-71. Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

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9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Design by Insight not Hindsight* application note
- Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *Quick Reference Guide To TI Buck Switching DC/DC application note*

9.3 ドキュメントの更新通知を受け取る方法

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9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
November 2024	*	Initial release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM644A2QVBGRQ1	Active	Production	WQFN-FCRLF (VBG) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	LM644A2
LM644A2QVBGRQ1.A	Active	Production	WQFN-FCRLF (VBG) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	LM644A2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

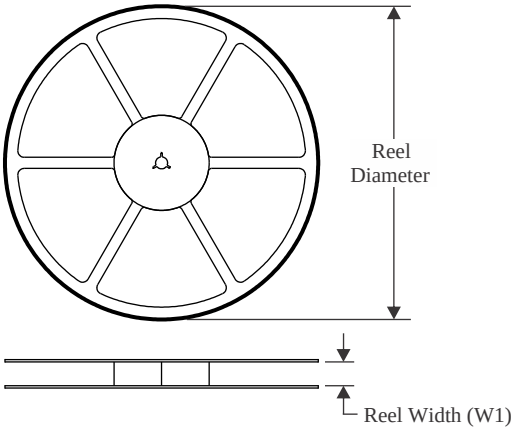
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

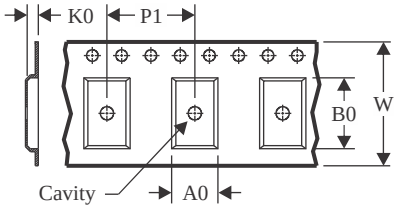
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

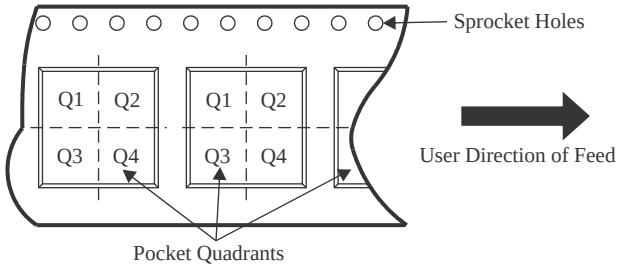


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

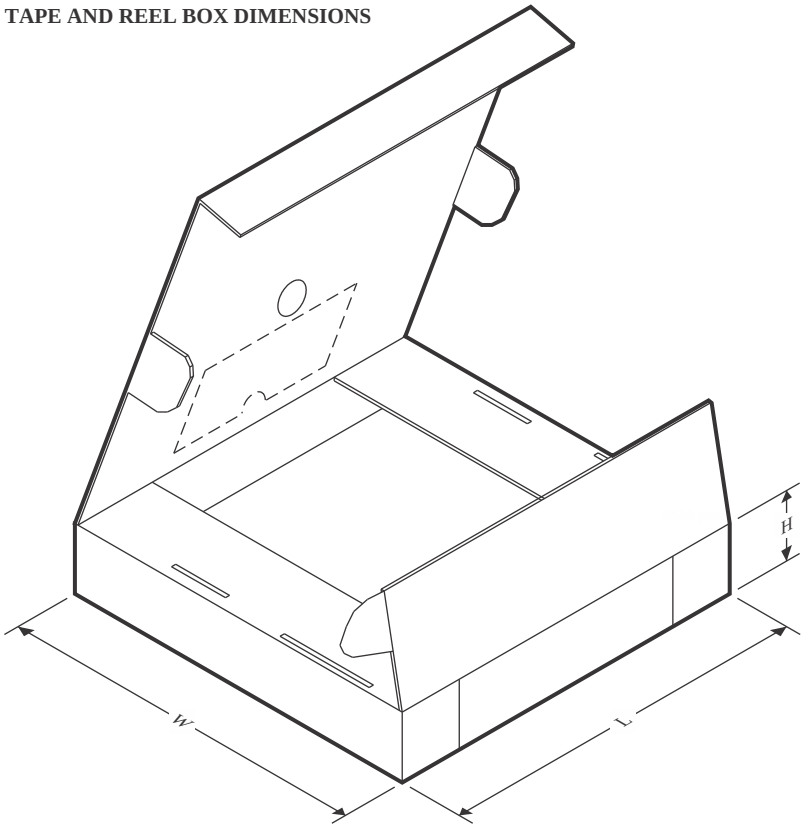
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM644A2QVBGRQ1	WQFN-FCRLF	VBG	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

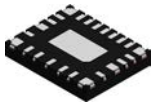


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM644A2QVBGRQ1	WQFN-FCRLF	VBG	24	3000	346.0	346.0	33.0

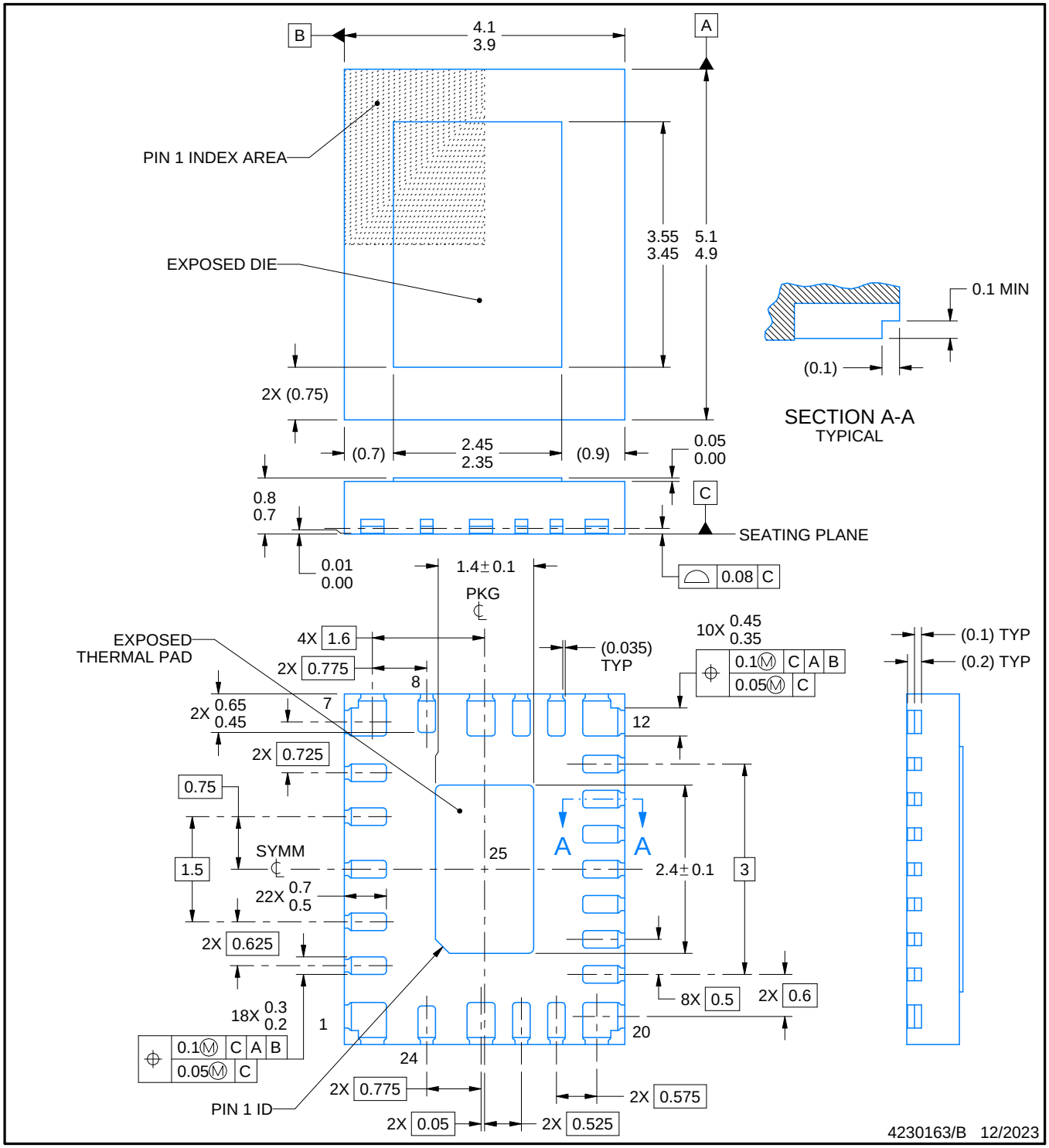
PACKAGE OUTLINE

VBG0024A



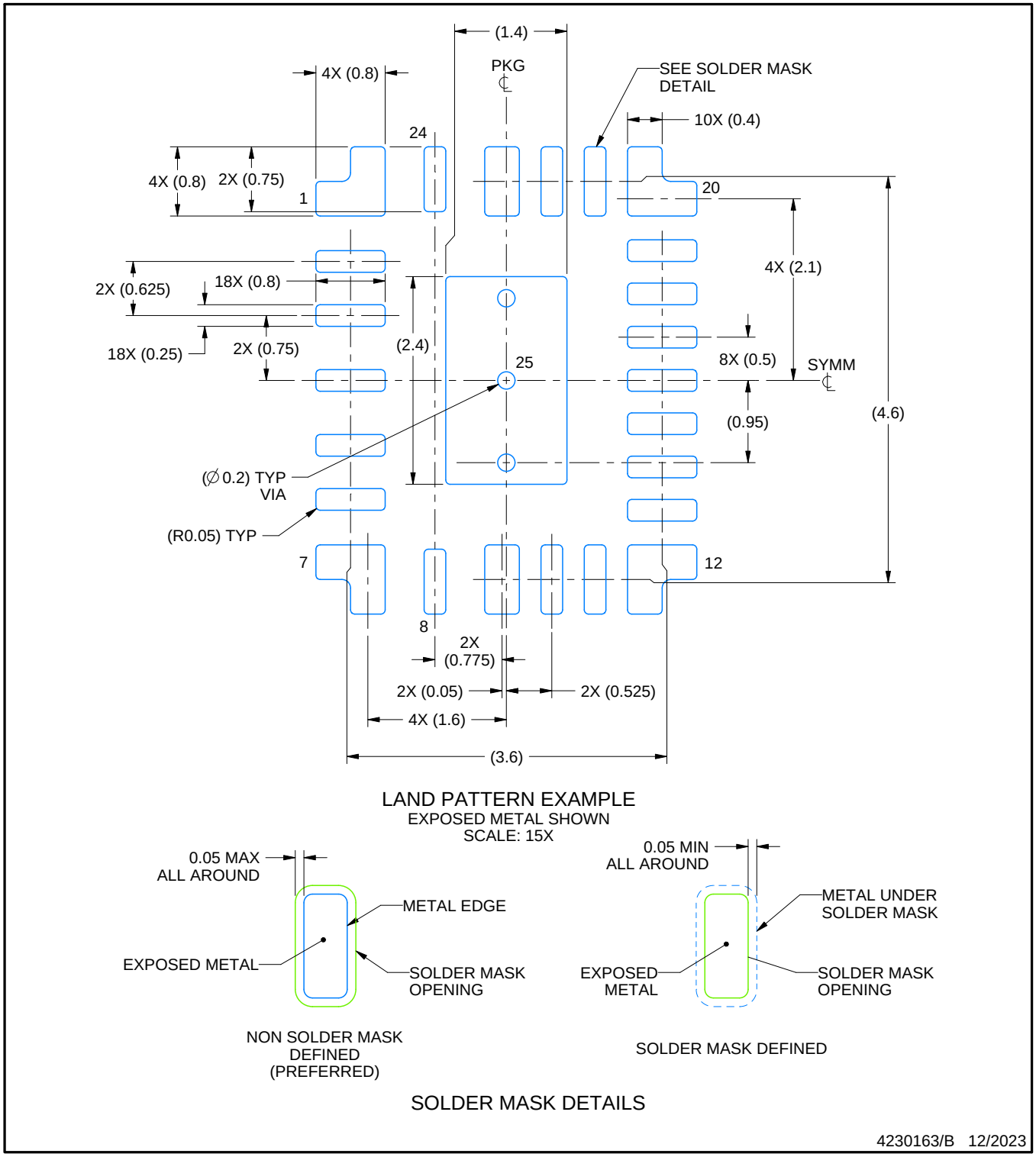
WQFN-FCRLF - 0.8mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

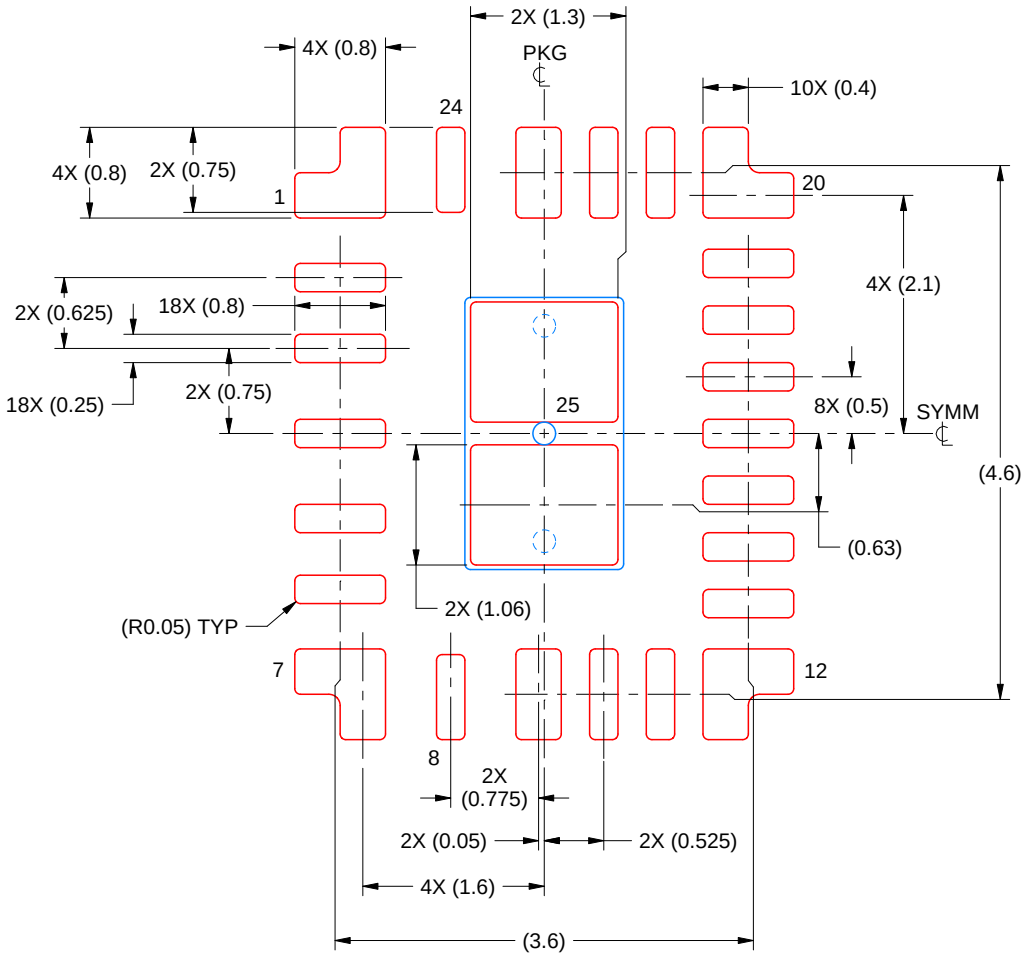
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VBG0024A

WQFN-FCRLF - 0.8mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 23:
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4230163/B 12/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月