TEXAS INSTRUMENTS
LM5152-Q1, LM51521-Q1
JAJSNZ8A – FEBRUARY 2022 – REVISED APRIL 2022

LM5152x-Q1 車載用、アイドリング・ストップ / バックアップ・バッテリ電源向け、低い静止電流 (I_Q)、同期整流昇圧コントローラ

1 特長

- 車載アプリケーション向けに AEC-Q100 認定済み
  - 温度グレード 1:–40℃～+125℃、T_A
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 車載用バッテリ駆動アプリケーションの広い動作範囲に適合
  - 3.8V～42V の入力動作範囲
  - 5V～20V (最大 57V の保護) に動的にプログラム可能な V_{OUT}
  - 最小昇圧入力 0.8V (BIAS ≥ 3.8V の場合
  - バイパス動作 (V_{SUPPLY} > V_{LOAD} の場合、LM5152 のみ、「デバイス比較表」を参照)
- バッテリ・ドレインの最小化
  - シャットダウン電流:3µA 以下
  - 自動的なモード遷移
  - ディープ・スリープ状態でのバッテリ・ドレイン ≤ 11µA (バイパス動作、チャージ・ポンプ・オフ)
  - ディープ・スリープ状態でのバッテリ・ドレイン ≤ 33µA (バイパス動作、チャージ・ポンプ・オン)
  - スリープ時の BIAS I_Q ≤ 13µA (スキップ・モード)
  - 強力な 5V MOSFET ドライバ
- 小さなソリューション・サイズと低いコスト
  - スイッチング周波数:2.2MHz (最大値)
  - ブート・ダイオード内蔵
  - V_{IN} に対する定ピーク電流制限
  - DCR インダクタ電流センシングをサポート
  - ウェッタブル・フランク付き QFN-20
- AM 帯域の干渉とクロストークを回避
  - 選択可能なクロック同期
  - 100kHz～2.2MHz のスイッチング周波数
  - スイッチング・モードを選択可能 (FPWM、ダイオード・エミュレーション、スキップ・モード)
- EMI 低減
  - プログラム可能な拡散スペクトラム (オプション)
  - リードレス・パッケージ
- プログラマビリティとフレキシビリティ
  - 動的な V_{OUT} トラッキング
  - 動的なスイッチング周波数のプログラミング
  - ライン UVLO をプログラム可能
  - 調整可能なソフトスタート
  - アダプティブ・デッド・タイム
  - 昇圧ステータス・インジケータ
- 保護機能内蔵
  - サイクルごとのピーク電流制限
  - 過電圧保護
  - HB-SW 短絡保護
  - サーマル・シャットダウン

2 アプリケーション

- 大出力 / 大電流の車載用アイドリング・ストップ・アプリケーション (ヘッド・ユニット)
- 電圧安定化モジュール
- 緊急通話アプリケーション
- バックアップ・バッテリ / スーパーキャパシタから電力を供給する昇圧コンバータ
- 車載用冗長電源

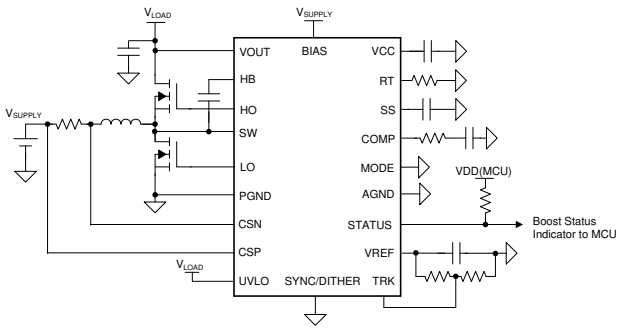
3 概要

LM5152x-Q1 (LM5152-Q1、LM51521-Q1) デバイスは、ピーク電流モード制御を採用した、入力範囲が広い同期整流昇圧コントローラです。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
LM5152-Q1	QFN (20)	3.5mm × 3.5mm
LM51521-Q1		

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (February 2022) to Revision A (April 2022)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更	1

5 概要 (続き)

このデバイスは、シャットダウン時の I_Q が低く、また、I_Q が低いスリープ・モードを備えているため、無負荷および軽負荷の状況でバッテリ・ドレインを最小化できます。さらに、このデバイスは、I_Q が非常に低いディープ・スリープ・モードでのバイパス動作にも対応しているため、電源電圧が昇圧出力レギュレーション目標よりも高い場合の外部バイパス・スイッチが不要です。出力電圧は、トラッキング機能を使用して動的にプログラムできます。

本デバイスの広い入力範囲は自動車のコールド・クランクとロード・ダンプをサポートしています。BIAS が 3.8V 以上のとき、最小入力電圧は 0.8V までの範囲で設定できます。スイッチング周波数は、外付け抵抗により 100kHz～2.2MHz の範囲で動的にプログラムされます。2.2MHz でのスイッチングにより、AM 帯域との干渉が最小化され、ソリューション・サイズの小型化と、高速な過渡応答を実現できます。コントローラ・アーキテクチャにより、コンバータ・アーキテクチャと比較して、過酷な周囲温度条件での熱管理を簡素化できます。

V_{IN} の全範囲にわたって一定のピーク電流制限、過電圧保護、サーマル・シャットダウンなどの保護機能が内蔵されています。外部クロック同期、プログラム可能なスペクトラム拡散変調、最小限の寄生容量でのリードレス・パッケージは、EMI の低減とクロストークの回避に役立ちます。その他の機能として、ライン UVLO、FPWM、ダイオード・エミュレーション、DCR インダクタ電流センシング、プログラム可能なソフトスタート、昇圧ステータス・インジケータがあります。

6 Device Comparison Table

Device Option	Bypass Operation
LM5152-Q1	Enabled
LM51521-Q1	Disabled

7 Pin Configuration and Functions

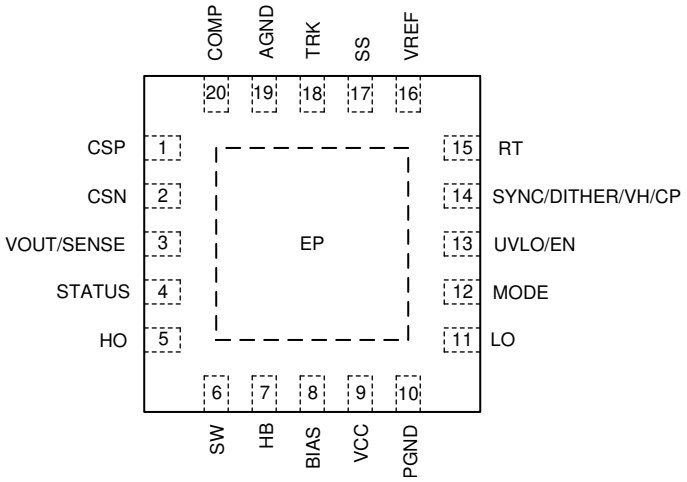


図 7-1. 20-Pin QFN with Wettable Flanks RGR Package (Top View)

表 7-1. Pin Functions

Pin		I/O(1)	Description
Name	NO.		
CSP	1	I	Current sense amplifier input. The pin operates as the positive input pin.
CSN	2	I	Current sense amplifier input. The pin operates as the negative input pin.
VOUT/SENSE	3	I	Output voltage sensing pin. An internal feedback resistor voltage divider is connected from the pin to AGND. Connect a 0.1-µF local VOUT capacitor from the pin to ground.
			High-side MOSFET drain voltage sensing pin. Connect the pin to the drain of the high-side MOSFET through a short, low inductance path.
STATUS	4	O	Status indicator with an open-drain output stage. The internal pulldown switch opens when the output voltage is greater than the overvoltage threshold. The pin can be left floating if not used.
HO	5	O	High-side gate driver output. Connect directly to the gate of the high-side N-channel MOSFET through a short, low inductance path.
SW	6	P	Switching node connection and the high-side MOSFET source voltage sensing pin. Connect directly to the source of the high-side N-channel MOSFET and the drain of the low-side N-channel MOSFET through a short, low inductance path. Connect to PGND for a non-synchronous boost configuration.
HB	7	P	High-side driver supply for bootstrap gate drive. Boot diode is internally connected from VCC to this pin. Connect a 0.1-µF capacitor between this pin and SW. Connect to VCC for a non-synchronous boost configuration.
BIAS	8	P	Supply voltage input to the VCC regulator. Connect a 1-µF local BIAS capacitor from the pin to ground.
VCC	9	P	Output of the internal VCC regulator and supply voltage input of the internal MOSFET drivers. Connect a 4.7-µF capacitor between the pin and PGND.
PGND	10	G	Power-ground pin. Connect directly to the source of the low-side N-channel MOSFET and the power ground plane through a short, low inductance path.
LO	11	O	Low-side gate driver output. Connect directly to the gate of the low-side N-channel MOSFET through a short, low inductance path.
MODE	12	I	Device switching mode (FPWM, diode emulation, or skip) selection pin. The device is configured to skip mode if the pin is open or if a resistor that is greater than 500 kΩ is connected from the pin to AGND during initial power-on. The device is configured to FPWM mode by connecting the pin to VCC or if the pin voltage is greater than 2.0 V during power-on. The device is configured to diode emulation mode by connecting the pin to ground or the pin voltage is less than 0.4 V during initial power-on. The switching mode can be dynamically programmed between FPWM and the DE mode during operation.

表 7-1. Pin Functions (continued)

Pin		I/O[1]	Description
Name	NO.		
UVLO/EN	13	I	Enable pin. The pin enables and disables the device. If the pin is less than 0.35 V, the device shuts down. The pin must be raised above 0.65 V to enable the device.
			Undervoltage lockout programming pin. The converter start-up and shutdown levels can be programmed by connecting the pin to the supply voltage through a resistor voltage divider. The low-side UVLO resistor must be connected to AGND. Connect to BIAS if not used.
SYNC/DITHER/VH/CP	14	I/O	Synchronization clock input. The internal oscillator can be synchronized to an external clock during operation. Connect to AGND if not used.
			Clock dithering and spread spectrum modulation frequency programming pin. If a capacitor is connected between the pin and AGND, the clock dithering and spread spectrum function is activated. During the dithering operation, the capacitor is charged and discharged with an internal 20-µA current source or sink. As the voltage on the pin ramps up and down, the oscillator frequency is modulated between –6% and +5% of the nominal frequency set by the RT resistor. The clock dithering and spread spectrum can be deactivated during operation by pulling down the pin to ground.
			VCC hold pin. If the pin is greater than 2.0 V, the device holds the VCC pin voltage when the EN pin is grounded, which helps to restart quickly without reconfiguration.
			Charge pump enable pin. If the pin is greater than 2.0 V, the internal charge pump maintains the HB pin voltage above its HB UVLO threshold for bypass operation, which allows the high-side switch to turn on 100% during bypass operation (LM5152-Q1 only).
RT	15	I	Switching frequency setting pin. If no external clock is applied to the SYNC pin, the switching frequency is programmed by a single resistor between the pin and AGND. Switching frequency is dynamically programmable during operation.
VREF	16	I/O	1.0-V internal reference voltage output. Connect a 470-pF capacitor from the pin to AGND. The V_{OUT} regulation target can be programmed by connecting a resistor voltage divider from the pin to TRK. The resistance from the pin to AGND must be always greater than 20 kΩ if used. Connect the low-side resistor of the divider to AGND.
			Boost converter output voltage can be dynamically programmed in the range of 5 V to 20 V during operation. The accuracy of the output voltage regulation is specified within the range. If the TRK pin voltage is externally controlled, the resistor voltage divider is not required.
SS	17	I/O	Soft-start time programming pin. An external capacitor and an internal current source set the ramp rate of the internal error amplifier reference during soft start. The device forces diode emulation during soft-start time.
TRK	18	I	Output regulation target programming pin. The V_{OUT} regulation target can be programmed by connecting the pin to VREF through a resistor voltage divider or by controlling the pin voltage directly from a D/A. The recommended operating range of the pin is from 0.25 V to 1.0 V.
AGND	19	G	Analog ground pin. Connect to the analog ground plane through a wide and short path.
COMP	20	O	Output of the internal transconductance error amplifier. Connect the loop compensation components between the pin and AGND.
EP	—	—	Exposed pad of the package. The EP must be soldered to a large analog ground plane to reduce thermal resistance.

(1) G = Ground, I = Input, O = Output, P = Power

8 Specifications

8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range (unless otherwise specified)(1)

		MIN	MAX	UNIT
Input(2)	BIAS to AGND	–0.3	50	V
	UVLO to AGND	–0.3	BIAS + 0.3	
	CSP to AGND	–0.3	50	
	CSP to CSN	–0.3	0.3	
	VOUT to AGND	–0.3	65	
	HB to AGND	–0.3	65	
	HB to SW	–0.3	5.8(3)	
	SW to AGND	–0.3	60	
	SW to AGND (50 ns)	–1		
	MODE, SYNC, TRK to AGND	–0.3	5.5	
	STATUS to AGND	–0.3	VOUT + 0.3	
	RT to AGND	–0.3	2.5	
	PGND to AGND	–0.3	0.3	
Output(2)	VCC to AGND	–0.3	5.8(3)	V
	HO to SW (50 ns)	–1		
	LO to PGND (50 ns)	–1		
	VREF, SS, COMP to AGND(4)	–0.3	5.5	
Operating junction temperature, T_J (5)		–40	150	°C
Storage temperature, T_{STG}		–55	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) It is not allowed to apply an external voltage directly to VREF, COMP, SS, RT, LO, and HO pins.
(3) Operating lifetime is de-rated when the pin voltage is greater than 5.5 V.
(4) Maximum VREF pin sourcing current is 50 µA.
(5) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2		±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 Recommended Operating Conditions

Over the recommended operating junction temperature range (unless otherwise specified)(1)

		MIN	NOM	MAX	UNIT
$V_{SUPPLY(BOOST)}$	Boost converter input (when BIAS ≥ 3.8 V)	0.8		42	V
$V_{LOAD(BOOST)}$	Boost converter output	5		57(3)	
V_{BIAS}	BIAS input	3.8		42	
V_{UVLO}	UVLO input	0		42	
V_{CSP}, V_{CSN}	Current sense input	0.8		42	
V_{VOUT}	Boost output sense	5		57(3)	
V_{TRK}	TRK input	0.25		1	
V_{SYNC}	Synchronization pulse input	0		5.25	
f_{SW}	Typical switching frequency	100		2200	kHz
f_{SYNC}	Synchronization pulse frequency	200		2200	
T_J	Operating junction temperature(2)	–40		150	°C

(1) *Recommended Operating Ratings* are conditions under the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.
(3) V_{VOUT} regulation target can be up to 20 V. The pin voltage should be less than or equal to 57 V.

8.4 Thermal Information

THERMAL METRIC(1)		RGR (QFN) 20 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	43.3	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	39.9	°C/W
R_{qJB}	Junction-to-board thermal resistance	17.8	°C/W
y_{JT}	Junction-to-top characterization parameter	0.8	°C/W
y_{JB}	Junction-to-board characterization parameter	17.8	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 125°C. Unless otherwise stated, V_{BIAS} = 12 V, V_{VOUT} = 12 V, R_T = 9.09 kΩ, R_{VREF} = 65 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT (BIAS, VCC, VOUT)						
$I_{BIAS-SD}$	BIAS current in shutdown	V_{UVLO} = 0 V, V_{OUT} = 11.3 V		2.5	5	µA
$I_{BIAS-DS1}$	BIAS current in deep sleep (skip or diode emulation mode, charge pump off, VCC is supplied by BIAS)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, V_{SYNC} = 0 V, V_{OUT} = 12 V		10	16	µA
$I_{BIAS-DS2}$	BIAS current in deep sleep (FPWM mode, charge pump off, VCC is supplied by BIAS)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, V_{SYNC} = 0 V, V_{OUT} = 12 V		10	16	µA
$I_{BIAS-DS3}$	BIAS current in deep sleep (skip or diode emulation mode, charge pump on, VCC is supplied by BIAS)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, V_{SYNC} = 2.5 V, V_{OUT} = 12 V		32	60	µA
$I_{BIAS-DS4}$	BIAS current in deep sleep (FPWM mode, charge pump on, VCC is supplied by BIAS)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, V_{SYNC} = 2.5 V, V_{OUT} = 12 V		32	60	µA

8.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 125°C. Unless otherwise stated, V_{BIAS} = 12 V, V_{VOUT} = 12 V, R_T = 9.09 kΩ, R_{VREF} = 65 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{BIAS-SLEEP}$	BIAS current in sleep (skip mode, VCC is supplied by BIAS)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, MODE = OPEN, V_{OUT} = 5 V		13	17.5	µA
$I_{BIAS-ACTIVE}$	BIAS current in active (nonswitching, VCC is supplied by BIAS)	V_{UVLO} = 2.5 V, V_{TRK} = 0.6 V, MODE = VCC		1.2	1.5	mA
$I_{VOUT-SD}$	VOUT current in shutdown	V_{UVLO} = 0 V, V_{OUT} = 11.3 V			1	µA
$I_{VOUT-DS}$	VOUT current in deep sleep (diode emulation mode)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, V_{OUT} = 12 V		1.2	1.5	µA
$I_{VOUT-ACTIVE}$	VOUT current in active (nonswitching)	V_{UVLO} = 2.5 V, V_{TRK} = 0.6 V, MODE = VCC		42	55	µA
$I_{BATTERY-SD}$	Battery drain in shutdown	V_{UVLO} = 0 V, V_{OUT} = 11.3 V		2.5	5	µA
$I_{BATTERY-DS1}$	Battery drain in deep sleep (skip or diode emulation mode, charge pump off)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, V_{SYNC} = 0 V		11	17	µA
$I_{BATTERY-DS2}$	Battery drain in deep sleep (FPWM mode, charge pump off)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, V_{SYNC} = 0 V		11	17	µA
$I_{BATTERY-DS3}$	Battery drain in deep sleep (skip or diode emulation mode, charge pump on)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, V_{SYNC} = 2.5 V		33	62	µA
$I_{BATTERY-DS4}$	Battery drain in deep sleep (FPWM mode, charge pump on)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, V_{SYNC} = 2.5 V		33	62	µA
ENABLE, UVLO						
$V_{EN-RISING}$	Enable threshold	EN rising	0.45	0.55	0.65	V
$V_{EN-FALLING}$	Enable threshold	EN falling	0.35	0.45	0.55	V
V_{EN-HYS}	Enable hysteresis	EN falling	55	90	130	mV
$I_{UVLO-HYS}$	UVLO pulldown hysteresis current	V_{UVLO} = 0.7 V	8	10	12	µA
$V_{UVLO-RISING}$	UVLO threshold	UVLO rising	1.05	1.1	1.15	V
$V_{UVLO-FALLING}$	UVLO threshold	UVLO falling	1.025	1.075	1.125	V
$V_{UVLO-HYS}$	UVLO hysteresis	UVLO falling		25		mV
SYNC/DITHER/VH/CP						
$V_{SYNC-RISING}$	SYNC threshold/SYNC detection threshold	SYNC rising			2	V
$V_{SYNC-FALLING}$	SYNC threshold	SYNC falling	0.4			V
	Minimum SYNC pullup pulse width				100	ns
I_{DITHER}	Dither source and sink current		16	21	26	µA
Δf_{SW1}	f_{SW} modulation (upper limit)			5%		
Δf_{SW2}	f_{SW} modulation (lower limit)			–6%		
$V_{DITHER-FALLING}$	Dither disable threshold		0.65	0.75	0.85	V
VCC						
$V_{VCC-REG1}$	VCC regulation	I_{VCC} = 100 mA	4.75	5	5.25	V
$V_{VCC-REG2}$	VCC regulation	No load	4.75	5	5.25	V
$V_{VCC-REG3}$	VCC regulation during dropout	V_{BIAS} = 3.8 V, I_{VCC} = 100 mA	3.45			V
$V_{VCC-UVLO-RISING}$	VCC UVLO threshold	VCC rising	3.55	3.65	3.75	V
$V_{VCC-UVLO-FALLING}$	VCC UVLO threshold	VCC falling	3.2	3.3	3.4	V

8.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 125°C. Unless otherwise stated, V_{BIAS} = 12 V, V_{VOUT} = 12 V, R_T = 9.09 kΩ, R_{VREF} = 65 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VCC-CL}	VCC sourcing current limit	V_{VCC} = 4 V	100			mA
CONFIGURATION (MODE)						
$V_{MODE-RISING}$	FPWM mode threshold	MODE rising			2.0	V
$V_{MODE-FALLING}$	Diode emulation mode threshold	MODE falling	0.4			V
RT						
V_{RT}	RT regulation			0.5		V
VREF, TRK, VOUT						
V_{REF}	VREF regulation target		0.99	1	1.005	V
$V_{OUT-REG}$	VOUT regulation target1 with resistor divider	VREF resistor divider to make V_{TRK} = 0.25 V, R_{VREF} = 65 kΩ	4.915	5	5.085	V
$V_{OUT-REG}$	VOUT regulation target2 with resistor divider	VREF resistor divider to make V_{TRK} = 0.5 V, R_{VREF} = 65 kΩ	9.9	10	10.1	V
$V_{OUT-REG}$	VOUT regulation target3 with resistor divider	VREF resistor divider to make V_{TRK} = 1.0 V, R_{VREF} = 65 kΩ	19.8	20	20.2	V
$V_{OUT-REG}$	VOUT regulation target1 using TRK	V_{TRK} = 0.25 V, R_{VREF} = 65 kΩ	4.91	5	5.09	V
$V_{OUT-REG}$	VOUT regulation target2 using TRK	V_{TRK} = 0.5 V, R_{VREF} = 65 kΩ	9.88	10	10.11	V
$V_{OUT-REG}$	VOUT regulation target3 using TRK	V_{TRK} = 1.0 V, R_{VREF} = 65 kΩ	19.8	20	20.2	V
I_{TRK}	TRK bias current				1	uA
SOFT START, DE to FPWM TRANSITION						
I_{SS}	Soft-start current		17	20	23	µA
$V_{SS-DONE}$	MODE transition start	SS rising	1.3	1.5	1.7	V
R_{SS}	SS pulldown switch R_{DSON}			30	70	Ω
V_{SS-DIS}	SS discharge detection threshold		30	50	75	mV
V_{SS-FB}	internal SS to FB clamp	V_{FB} = 0 V		55	75	mV
CURRENT SENSE (CSP, CSN, SW, SENSE)						
V_{SLOPE}	Peak slope compensation amplitude	Referenced to CS input		45		mV
A_{CS}	Current sense amplifier gain	CSP = 3.0 V		10		V/V
	Current sense amplifier gain	CSP = 1.5 V		10		V/V
V_{CLTH}	Positive peak current limit threshold (CSP-CSN)	CSP = 3.0 V, MODE = GND	54	60	66	mV
	Positive peak current limit threshold (CSP-CSN)	CSP = 1.5 V, MODE = GND	51	60	72	mV
V_{ZCD-DE}	ZCD threshold (SW-SENSE)	MODE = GND		4		mV
I_{CSN}	CSN bias current				1	µA
I_{CSP}	CSP bias current			115		µA
BOOT FAULT PROTECTION (HB)						
	Maximum replenish pulse cycles			4		cycles
	Replenish off cycles			12		cycles
	Number of sets to enter hiccup mode protection			4		sets
	Off-cycle during hiccup mode off			512		cycles
ERROR AMPLIFIER (COMP)						
Gm	Transconductance			1		mA/V

8.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 125°C. Unless otherwise stated, V_{BIAS} = 12 V, V_{VOUT} = 12 V, R_T = 9.09 kΩ, R_{VREF} = 65 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{SOURCE-MAX}$	Maximum COMP sourcing current	V_{COMP} = 0 V	95			µA
$I_{SINK-MAX}$	Maximum COMP sinking current	V_{COMP} = 1.8 V	90			µA
$V_{CLAMP-MAX}$	COMP maximum clamp voltage	COMP rising	1.8	2.2	2.55	V
$V_{CLAMP-MIN}$	COMP minimum clamp voltage, active in sleep and deep sleep mode	COMP falling		0.25		V
PULSE WIDTH MODULATION (PWM)						
f_{SW1}	Switching frequency	R_T = 220 kΩ	85	100	115	kHz
f_{SW2}	Switching frequency	R_T = 9.09 kΩ	1980	2200	2420	kHz
t_{ON-MIN}	Minimum controllable on time	R_T = 9.09 kΩ	14	20	50	ns
$t_{OFF-MIN}$	Minimum forced off time	R_T = 9.09 kΩ	70	95	115	ns
D_{MAX1}	Maximum duty cycle limit	R_T = 220kΩ	90%	94%	98%	
D_{MAX2}	Maximum duty cycle limit	R_T = 9.09 kΩ	75%	80%	83%	
LOW IQ SLEEP MODE						
V_{WAKE}	Internal wakeup threshold	VOUT falling (referenced to $V_{OUT-REG}$)		98.5%		
	Sleep to wake-up delay	R_T = 9.09 kΩ		5		µs
STATUS, OVP						
$V_{OVTH-RISING}$	Overvoltage threshold (OVP threshold, bypass mode threshold)	VOUT rising (referenced to $V_{OUT-REG}$)	104.5%	108%	111%	
$V_{OVTH-FALLING}$	Overvoltage threshold (OVP threshold, bypass mode threshold)	VOUT falling (referenced to $V_{OUT-REG}$)	100.5%	105%	109%	
R_{STATUS}	STATUS pulldown switch R_{DSON}			90	180	Ω
	Minimum BIAS for valid STATUS				2.5	V
MOSFET DRIVER						
	High-state voltage drop (HO driver)	100mA sinking		0.08	0.15	V
	Low-state voltage drop (HO driver)	100mA sourcing		0.04	0.1	V
	High-state voltage drop (LO driver)	100mA sinking		0.08	0.17	V
	Low-state voltage drop (LO driver)	100mA sourcing		0.04	0.1	V
$V_{HB-UVLO}$	HB-SW UVLO threshold	HB-SW falling	2.2	2.5	3.0	V
$I_{HB-SLEEP}$	HB quiescent current in sleep	HB-SW = 5 V		3.5	7	µA
t_{DHL}	HO off to LO on dead time			20		ns
t_{DLH}	LO off to HO on dead time			22		ns
	HB diode resistance			1.2		Ω
THERMAL SHUTDOWN						
$T_{TSD-RISING}$	Thermal shutdown threshold	Temperature rising		175		°C
$T_{TSD-HYS}$	Thermal shutdown hysteresis			15		°C

8.6 Typical Characteristics

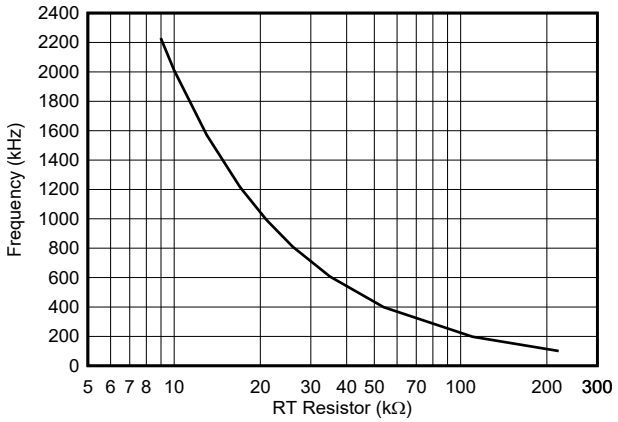


図 8-1. Frequency vs RT Resistance

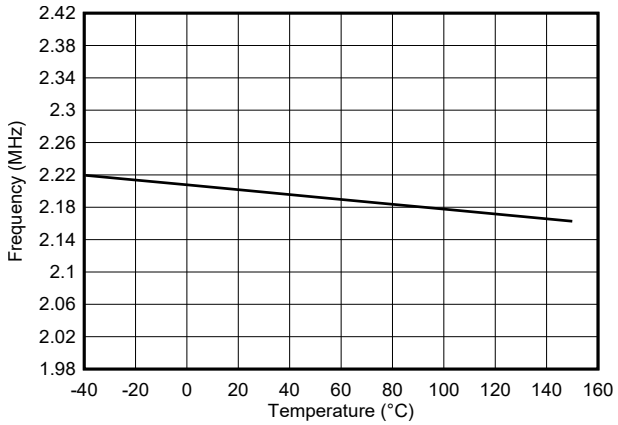


図 8-2. Frequency vs Temperature (RT = 9.09 kΩ, 2.2 MHz)

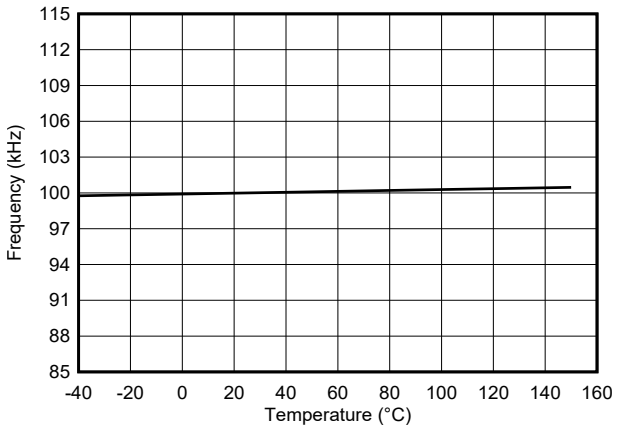


図 8-3. Frequency vs Temperature (RT = 220 kΩ, 100 kHz)

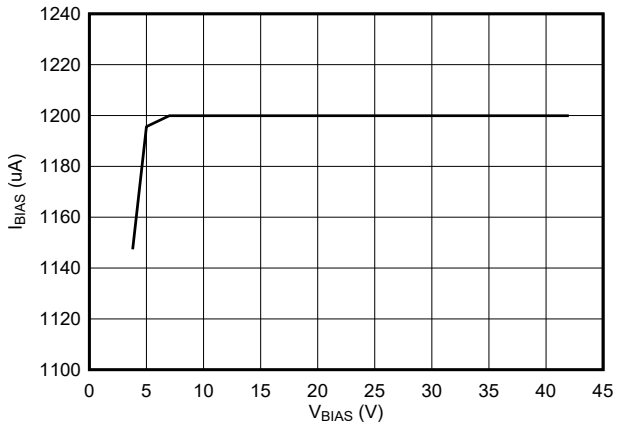


図 8-4. V_{BIAS} vs I_{BIAS} (Active Mode)

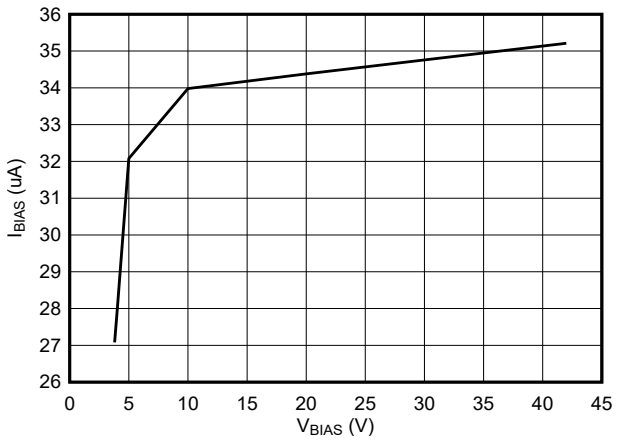


図 8-5. V_{BIAS} vs I_{BIAS} (Bypass Mode, Charge Pump On)

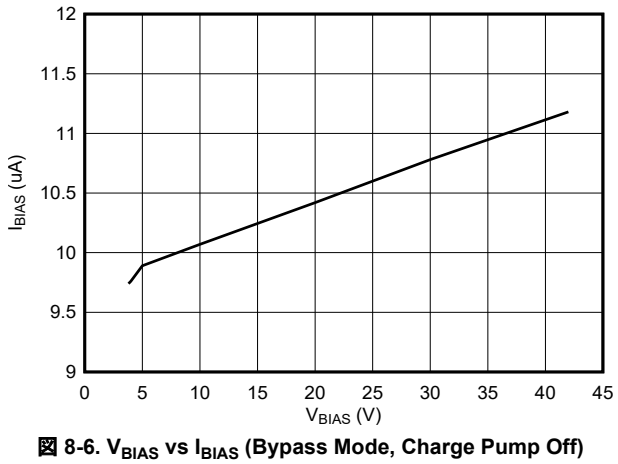


図 8-6. V_{BIAS} vs I_{BIAS} (Bypass Mode, Charge Pump Off)

8.6 Typical Characteristics (continued)

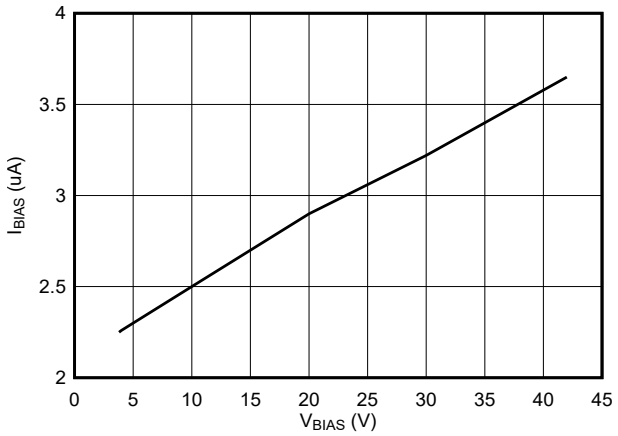


図 8-7. V_{BIAS} vs I_{BIAS} (Shutdown Mode)

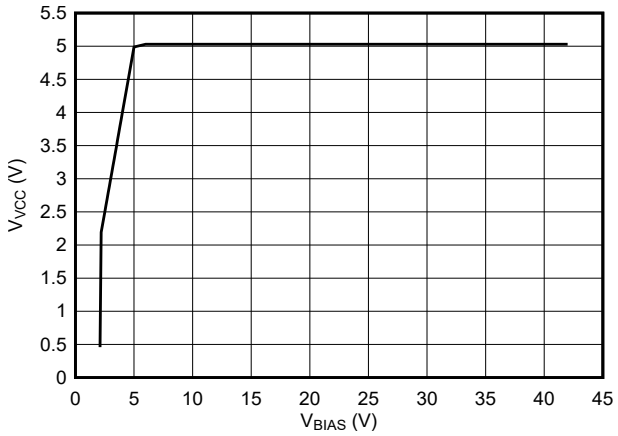


図 8-8. V_{BIAS} vs V_{VCC}

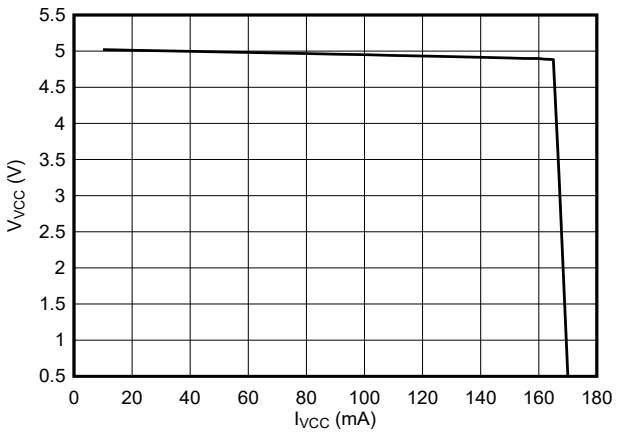


図 8-9. V_{VCC} vs I_{VCC}

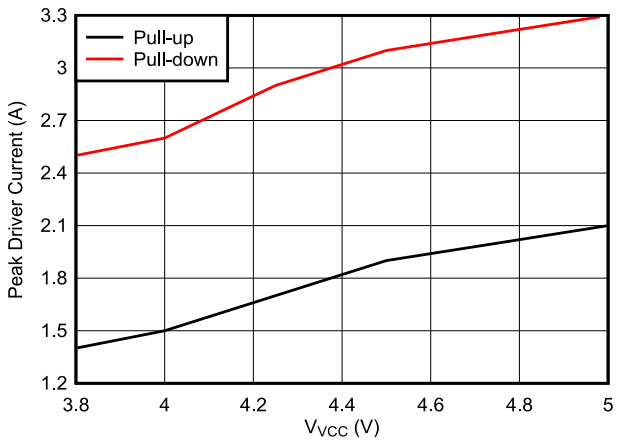


図 8-10. V_{VCC} vs Peak Driver Current

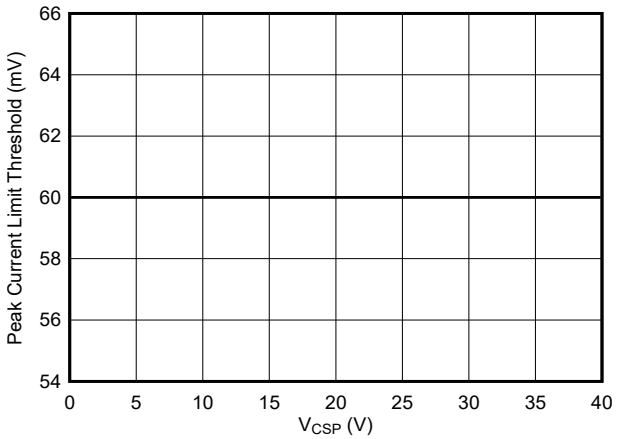


図 8-11. Peak Current Limit Threshold vs V_{CSP}

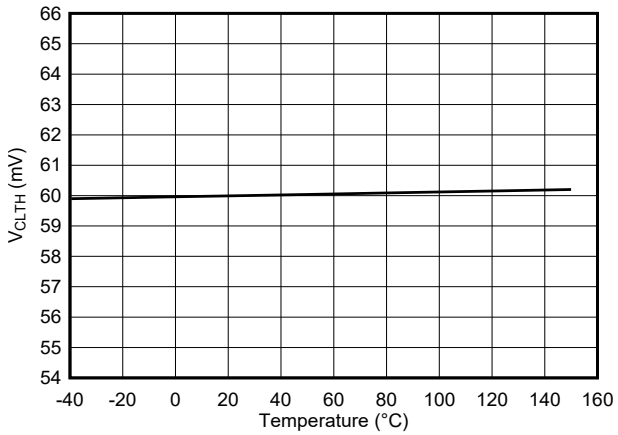


図 8-12. Peak Current Limit Threshold V_{CLTH} vs Temperature (CSP = 3 V)

8.6 Typical Characteristics (continued)

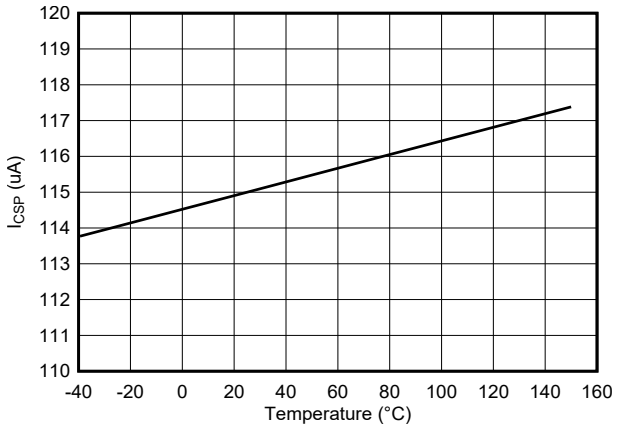


図 8-13. I_{CSP} vs Temperature (Active Mode)

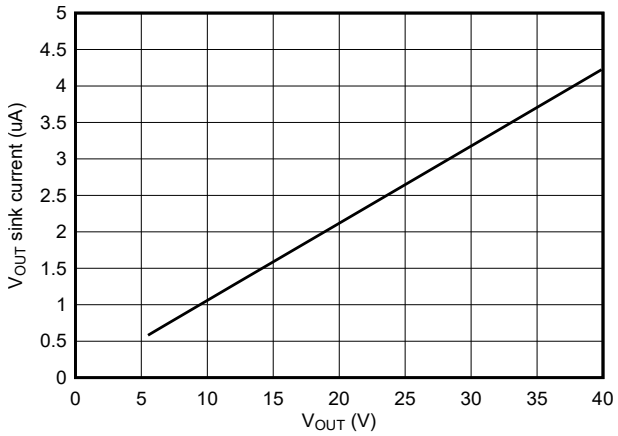


図 8-14. VOUT Sink Current vs VOUT (Deep Sleep)

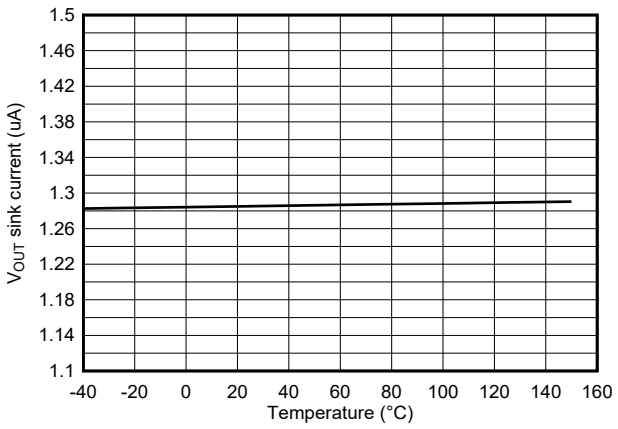


図 8-15. V_{OUT} Sink Current vs Temperature (Deep Sleep)

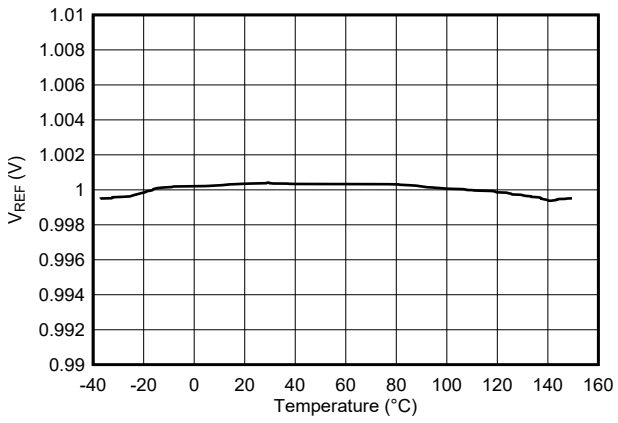


図 8-16. V_{REF} vs Temperature

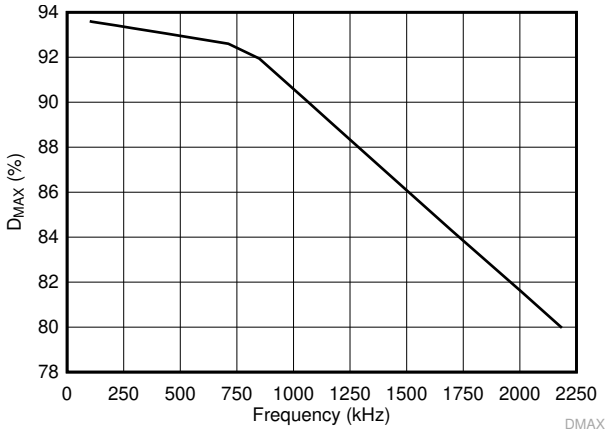


図 8-17. D_{MAX} vs Frequency

9 Detailed Description

9.1 Overview

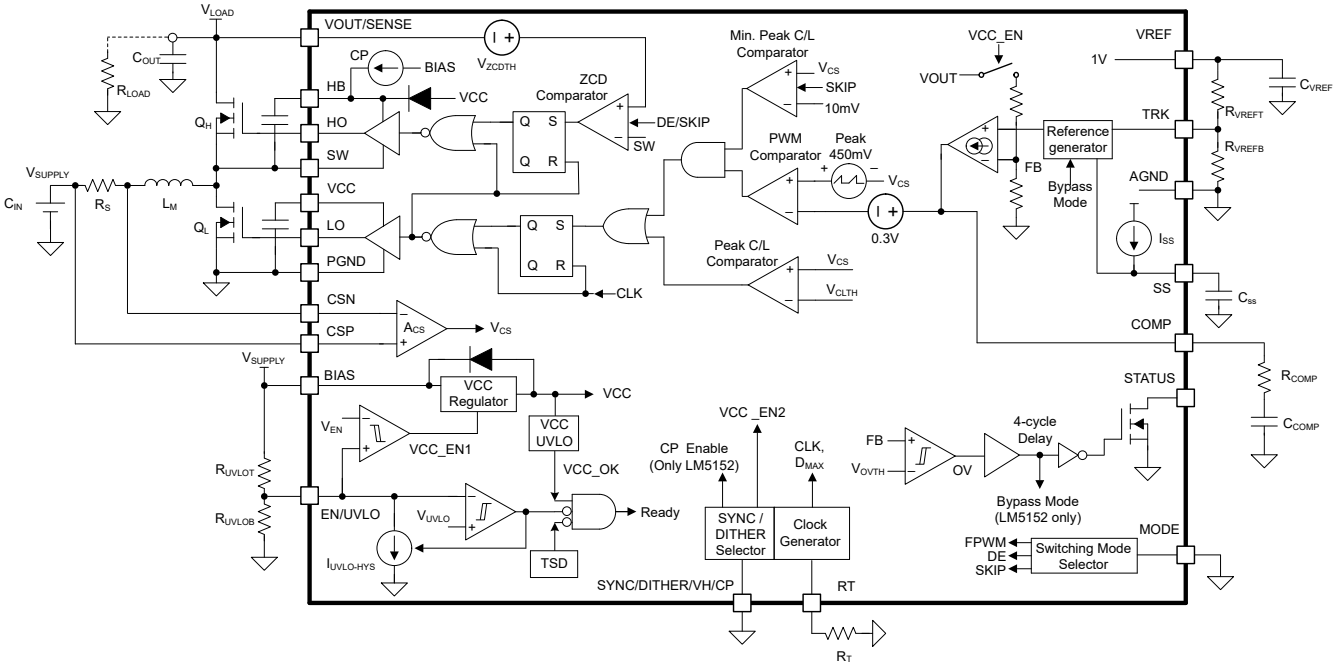
The LM5152x-Q1 (LM5152-Q1 and LM51521-Q1) device is a wide input range synchronous boost controller that employs peak current mode control. The device features a low shutdown I_Q and a low I_Q sleep mode, which minimizes battery drain at no and light load condition. The device also supports an ultra-low I_Q deep sleep mode with bypass operation, which eliminates the need for an external bypass switch when the supply voltage is greater than the boost output regulation target. The output voltage can be dynamically programmed using the tracking function.

The wide input range of the device supports automotive cold-crank and load dump. The minimum input voltage can be as low as 0.8 V when BIAS is equal to or greater than 3.8 V. The switching frequency is dynamically programmed with an external resistor from 100 kHz to 2.2 MHz. Switching at 2.2 MHz minimizes AM band interference and allows for a small solution size and fast transient response. Controller architecture simplifies thermal management at harsh ambient temperature conditions when compared to converter architectures.

The device has built-in protection features such as peak current limit, which is constant over V_{IN}, overvoltage protection, and thermal shutdown. External clock synchronization, programmable spread spectrum modulation, and a lead-less package with minimal parasitic help reduce EMI and avoid cross talk. Additional features include the following:

- Line UVLO
- FPWM
- Diode emulation
- DCR inductor current sensing
- Programmable soft start
- Boost status indicator

9.2 Functional Block Diagram



9.3 Feature Description

注

Read through セクション 9.4 before reading the feature description of the device. It is recommended to understand which device functional modes and what type of light load switching modes are supported by the device.

The parameters or thresholds values mentioned in this section are reference values unless otherwise specified. Refer to the *Electrical Characteristics* to find the minimum, maximum, and typical values.

9.3.1 Device Enable/Disable (EN, VH Pin)

The device shuts down when EN is less than the EN threshold (V_{EN}) and VH is less than the SYNC threshold (V_{SYNC}). The device is enabled when EN is greater than V_{EN} or VH is greater than V_{SYNC}. The VH pin provides a 40-µs internal delay before the device shuts down.

During shutdown, a 33-kΩ internal pulldown resistor on the EN pin is connected to GND to prevent a false turn-on when the pin is floating. Once EN goes above the EN threshold (V_{EN}), the 33-kΩ resistor is disconnected and the $I_{UVLO-HYS}$ current source is enabled to provide the UVLO functionality. The $I_{UVLO-HYS}$ current is designed to avoid chatter around the EN threshold voltage.

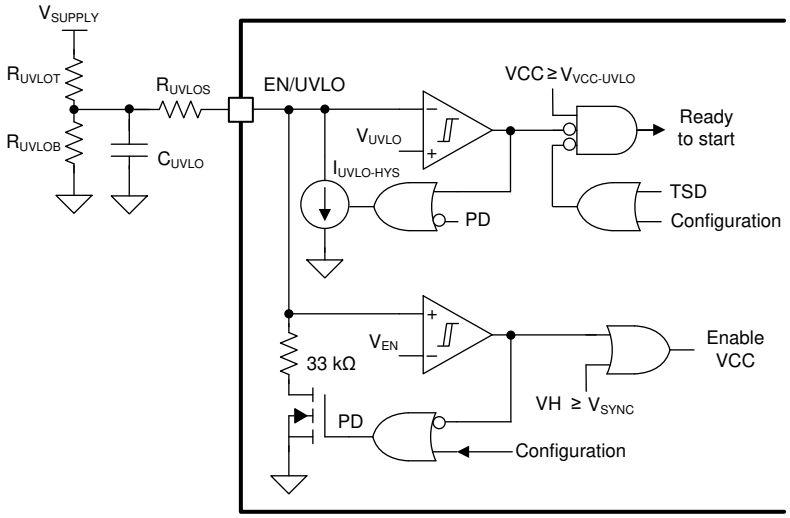


図 9-1. EN/UVLO Circuit

9.3.2 High Voltage VCC Regulator (BIAS, VCC Pin)

The device features a high voltage 5-V VCC regulator, which is sourced from the BIAS pin. The internal VCC regulator turns on 50 µs after the device is enabled and the 120-µs device configuration starts when VCC is above the VCC UVLO threshold ($V_{VCC-UVLO}$). The device configuration is reset when the device shuts down or VCC falls down below 2.2 V. The preferred way to reconfigure the device is to shut down the device. During the configuration time, the light load switching mode is selected.

The high voltage VCC regulator allows the connection of the BIAS pin directly to supply voltages from 3.8 V to 42 V. When BIAS is less than the 5-V VCC regulation target ($V_{VCC-REG}$), the VCC output tracks the BIAS pin voltage with a small dropout voltage, which is caused by the 1.7-Ω resistance of the VCC regulator.

The recommended VCC capacitor value is 4.7 µF. The VCC capacitor should be populated between VCC and PGND as close to the device as possible. The recommended BIAS capacitor value is 1.0 µF. The BIAS capacitor must be populated between BIAS and PGND close to the device.

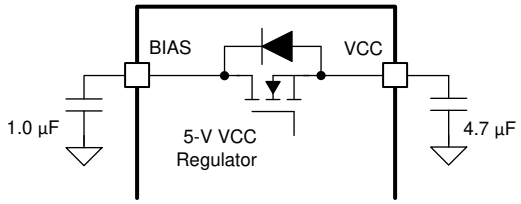


図 9-2. High Voltage VCC Regulator

The VCC regulator features a VCC current limit function that prevents device damage when the VCC pin is shorted to ground accidentally. The minimum sourcing capability of the VCC regulator is 100 mA (I_{VCC-CL}) during either the device configuration time or active mode operation. The minimum sourcing capability of the VCC regulator is reduced to 1 mA during sleep mode or deep sleep mode, or when EN is less than V_{EN} and VH is greater than V_{SYNC}. The VCC regulator supplies the internal drivers and other internal circuits. The external MOSFETs must be carefully selected to make the driver current consumption less than I_{VCC-CL}. The driver current consumption can be calculated in 式 1.

$$I_G = 2 \times Q_{G@5V} \times f_{SW} \quad (1)$$

where

- $Q_{G@5V}$ is the N-channel MOSFET gate charge at 5-V gate-source voltage.

If VIN operation below 3.8 V is required, the BIAS pin must be connected to the output of the boost converter (V_{LOAD}). By connecting the BIAS pin to V_{LOAD}, the boost converter input voltage (V_{SUPPLY}) can drop down to 0.8 V if BIAS is greater than 3.8 V. See セクション 9.3.16 for more detailed information about the minimum V_{SUPPLY}.

9.3.3 Light Load Switching Mode Selection (MODE Pin)

The light load switching mode is selected during the device configuration. The device is configured to skip mode when the MODE pin is floating or a resistor that is greater than 500 kΩ is connected between MODE and AGND during the device configuration. Once the device is configured to skip mode, the light load switching mode cannot be changed until the user reconfigures the device.

If the MODE pin voltage is less than 0.4 V ($V_{MODE-FALLING}$) or grounded during the device configuration, the device is configured to diode emulation (DE) mode. If the MODE pin voltage is greater than 2.0 V ($V_{MODE-RISING}$) or connected to VCC during the device configuration, the device is configured to forced PWM (FPWM) mode. If the device is configured to DE or FPWM mode, light load switching mode can be dynamically changed between DE and FPWM modes during operation without reconfiguration.

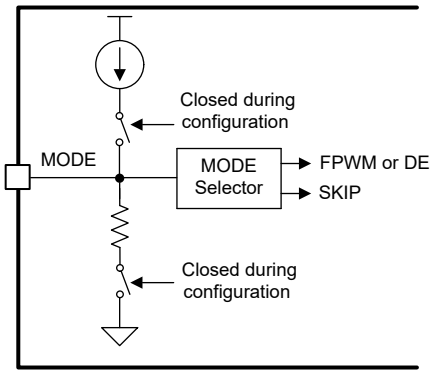


図 9-3. MODE Selection Circuit

9.3.4 Line Undervoltage Lockout (UVLO Pin)

When UVLO is greater than the UVLO threshold (V_{UVLO}), the device enters active mode if the device configuration is finished. UVLO hysteresis is accomplished with an internal 25-mV voltage hysteresis ($V_{UVLO-HYS}$) at the UVLO pin, and an additional 10-µA current sink ($I_{UVLO-HYS}$) that is switched on or off. When the UVLO pin

voltage exceeds V_{UVLO}, the current sink is disabled to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below V_{UVLO} or during the device configuration time, the current sink is enabled, causing the voltage at the UVLO pin to fall quickly.

The external UVLO resistor voltage divider (R_{UVLOT}, R_{UVLOB}) must be designed so that the voltage at the UVLO pin is greater than V_{UVLO} when V_{SUPPLY} is in the desired operating range. The values of R_{UVLOT} and R_{UVLOB} can be calculated as follows.

$$R_{UVLOT} = \frac{\left(V_{SUPPLY\_ON} - \frac{V_{UVLO\_RISING}}{V_{UVLO\_FALLING}} \times V_{SUPPLY\_OFF}\right)}{I_{UVLO\_HYS}} \quad (2)$$

$$R_{UVLOB} = \frac{V_{UVLO\_FALLING} \times R_{UVLOT}}{V_{SUPPLY\_OFF} - V_{UVLO\_FALLING}} \quad (3)$$

A UVLO capacitor (C_{UVLO}) is required in case V_{SUPPLY} drops below $V_{SUPPLY-OFF}$ momentarily during the start-up or during a severe load transient at the low input voltage. If the required UVLO capacitor is large, an additional series UVLO resistor (R_{UVLOS}) can be used to quickly raise the voltage at the UVLO pin when $I_{UVLO-HYS}$ is disabled.

The UVLO pin can be connected to the BIAS pin if not used. Drive the UVLO pin through a minimum of a 5-kΩ resistor if the BIAS pin voltage is less than the UVLO pin voltage in any conditions.

9.3.5 Fast Restart Using VCC HOLD (VH Pin)

The device is prepared for a fast start or restart when VH is greater than V_{SYNC}. The device configuration is completed and the VCC regulator is active. The device stops switching, but keeps the VCC regulator active when EN is less than V_{EN} and VH is greater than V_{SYNC} (see 図 9-5).

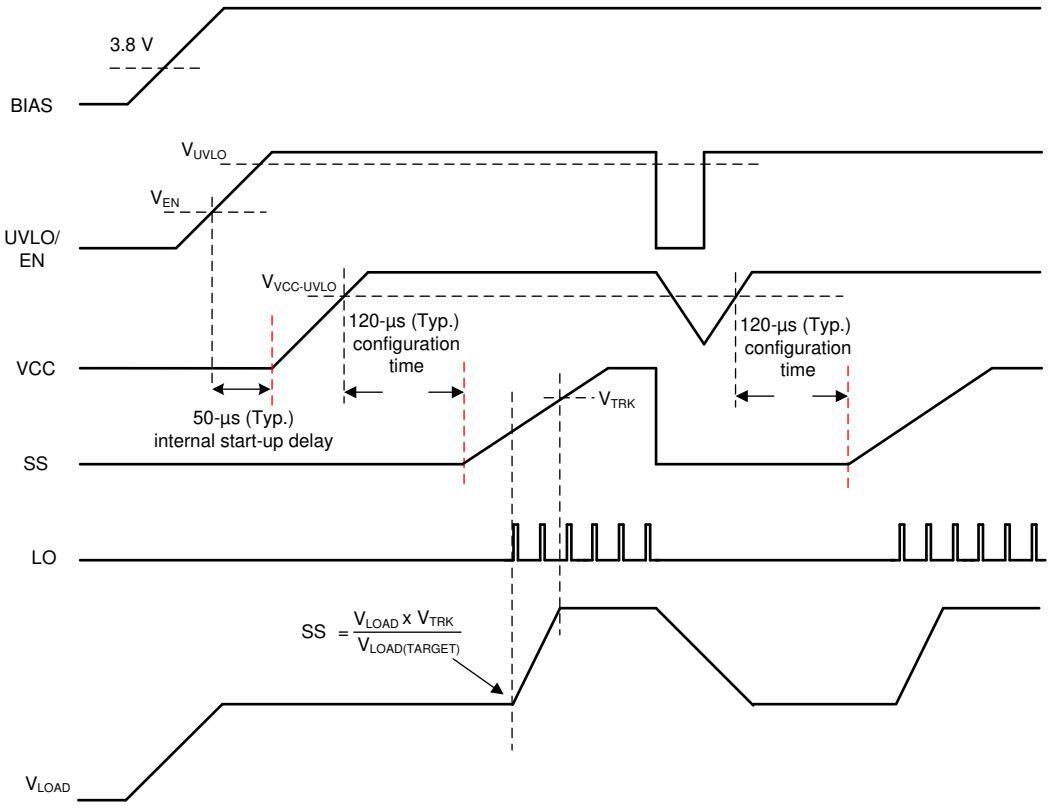


図 9-4. Boost Start-Up Waveforms Case 1: Start-Up by EN/UVLO, Restart when VH < V_{SYNC}

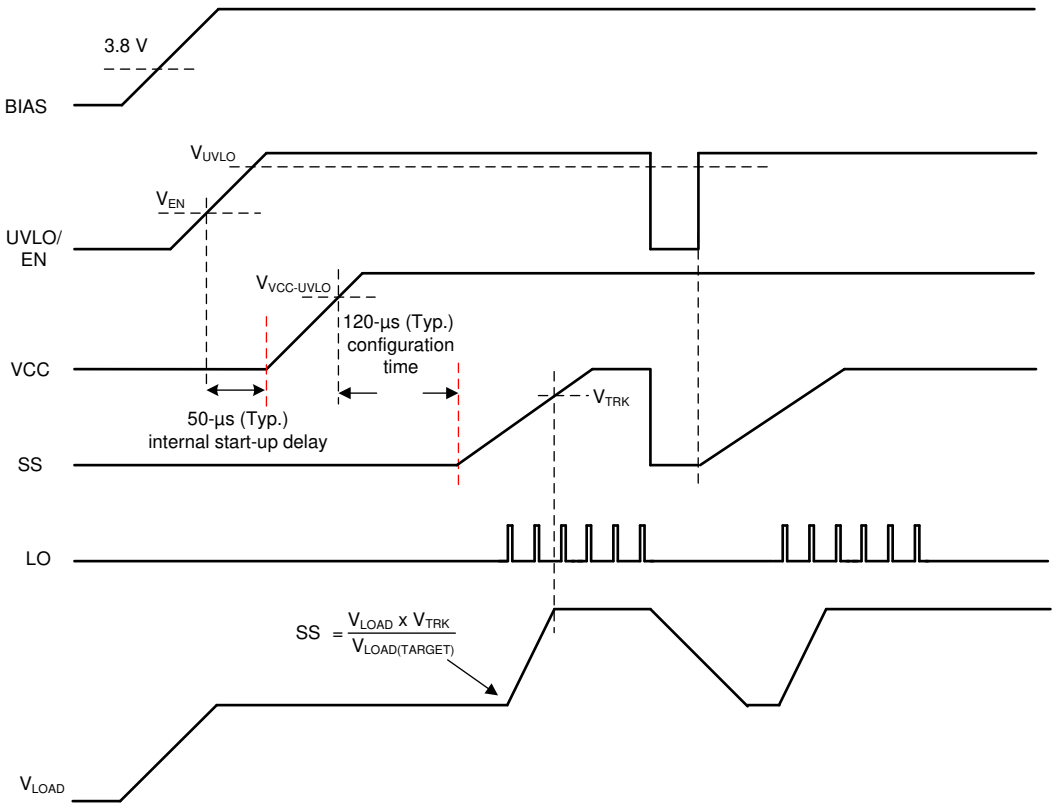


図 9-5. Boost Start-Up Waveforms Case 2: Start-Up by EN/UVLO, Restart when VH > V_{SYNC}

9.3.6 Adjustable Output Regulation Target (VOUT, TRK, VREF Pin)

The V_{OUT} regulation target ($V_{OUT-REG}$) is adjustable by programming the TRK pin voltage, which is the reference of the internal error amplifier. The accuracy of $V_{OUT-REG}$ is given when the TRK voltage is between 0.25 V and 1.0 V. The high impedance TRK pin allows users to program the pin voltage directly by a D/A converter or by connecting to a resistor voltage divider (R_{VREFT}, R_{VREFB}) between VREF and AGND.

The device provides a 1-V voltage reference (V_{REF}), which can be used to program the TRK pin voltage through a resistor voltage divider. It is not recommended to use V_{REF} as a reference voltage of an external circuit because the device periodically disables V_{REF} in sleep or deep sleep mode. For stability reasons, the VREF capacitor (C_{VREF}) should be between 330 pF and 1 nF. 470 pF is recommended.

When R_{VREFT} and R_{VREFB} are used to program the TRK pin voltage, $V_{OUT-REG}$ can be calculated as follows.

$$V_{OUT\_REG} = \frac{20 \times R_{VREFB}}{R_{VREFB} + R_{VREFT}} \quad (4)$$

The TRK pin voltage can be dynamically programmed in active mode, which makes an envelope tracking power supply design easy. When designing a tracking power supply, it is required to adjust the TRK pin voltage slow enough so that the VOUT pin voltage can track the command and the internal overvoltage or undervoltage comparator is not triggered during the transient operation. An RC filter must be used at the TRK pin to slow down the slew rate of the command signal at the TRK pin, especially when a step input is applied. When a trapezoidal or sinusoidal input is applied, the slew rate or the frequency of the command signal must be limited.

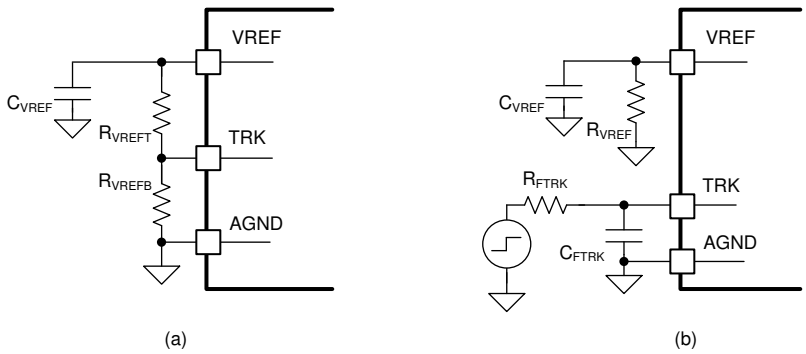


図 9-6. TRK Control (a) Using VREF (b) by External Step Input

$V_{OUT-REG}$ tracks the TRK pin voltage in all operation modes (FPWM, skip or diode mode) with a maximum of a 20-ms delay during deep sleep mode to save power. Take extra care when programming TRK if V_{SUPPLY} is greater than $V_{OUT-REG}$ in any conditions. The device enters active mode with a 5-µs delay if V_{LOAD} falls below $V_{OUT-REG}$ in deep sleep mode, but the device enters active mode with maximum of a 20-ms delay if $V_{OUT-REG}$ is increased by TRK above V_{LOAD} in deep sleep mode.

9.3.7 Overvoltage Protection (VOUT Pin)

The device provides an overvoltage protection (OVP) for boost converter output. The OVP comparator monitors the VOUT pin through internal resistor voltage dividers. If the VOUT pin voltage rises above the overvoltage threshold (V_{OVTH}), OVP is activated. When OVP is triggered, the device turns off the low-side driver and turns on the high-side driver until zero current is detected in diode emulation or skip mode. In FPWM mode, the low-side driver is not turned off when the OVP is triggered.

After at least 40 µs in OVP status, the device enters deep sleep mode and LM5152-Q1 turns on the high-side driver 100% while LM51521-Q1 turns the high-side driver off. The recommended VOUT capacitor (C_{VOUT}) is 0.1 µF.

9.3.8 Boost Status Indicator (STATUS Pin)

The device provides a boost status indicator (STATUS) to simplify sequencing and supervision. STATUS is an open-drain output. A pullup resistor between 5 kΩ and 100 kΩ can be externally connected to the STATUS pin. The STATUS switch opens four cycles after the VOUT pin voltage is greater than the overvoltage voltage (V_{OVTH}). The STATUS pin is pulled down to ground when the following occurs:

- VOUT pin voltage is less than V_{OVTH}.
- UVLO is less than V_{UVLO}.
- VCC is less than $V_{VCC-UVLO}$.
- During thermal shutdown

The STATUS pin voltage cannot be greater than V_{VOUT} + 0.3 V.

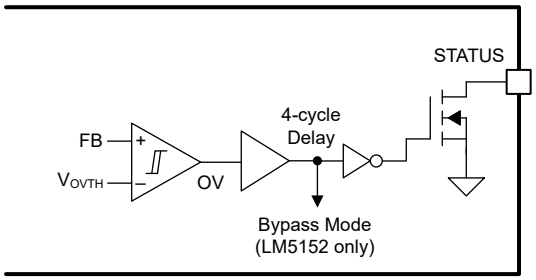


図 9-7. STATUS Indicator

9.3.9 Dynamically Programmable Switching Frequency (RT)

The switching frequency of the device is set by a single RT resistor connected between RT and AGND if no external synchronization clock is applied to the SYNC pin. The resistor value to set the RT switching frequency (R_T) is calculated as follows.

$$R_T = \frac{2.21 \times 10^{10}}{f_{RT(typical)}} - 955 \quad (5)$$

The RT pin is regulated to 0.5 V by an internal RT regulator when the device is in active mode or during the device configuration. The switching frequency can be dynamically programmed during operation as shown in 図 9-8.

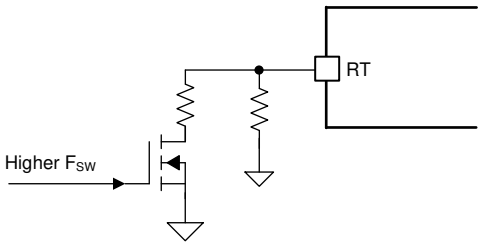


図 9-8. Frequency Hopping Example

9.3.10 External Clock Synchronization (SYNC Pin)

The switching frequency of the device can be synchronized to an external clock by directly applying an external pulse signal to the SYNC pin. The internal clock is synchronized at the rising edge of the external synchronization pulse using an internal PLL. Connect the SYNC pin to ground if not used.

The external synchronization pulse must be greater than V_{SYNC} in the high logic state and must be less than V_{SYNC} in the low logic state. The duty cycle of the external synchronization pulse is not limited, but the minimum on-pulse and the minimum off-pulse widths must be greater than 100 ns. The frequency of the external synchronization pulse must satisfy 式 6 and 式 7.

$$200\text{kHz} \le f_{SYNC} \le 2.2\text{MHz} \quad (6)$$

$$0.75 \times f_{RT(typical)} \le f_{SYNC} \le 1.5 \times f_{RT(typical)} \quad (7)$$

For example, a RT resistor is required for typical 350-kHz switching to cover 263-kHz to 525-kHz clock synchronization without changing the RT resistor.

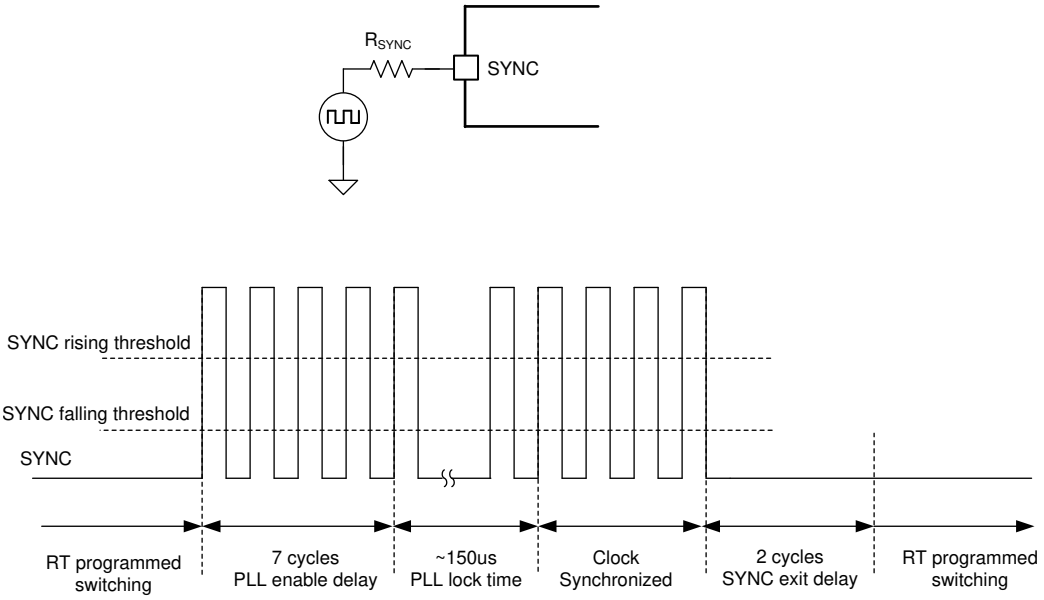


図 9-9. External Clock Synchronization

Drive the SYNC pin through a minimum 1-kΩ resistor if the BIAS pin voltage is less than the SYNC pin voltage in any conditions.

9.3.11 Programmable Spread Spectrum (DITHER Pin)

The device provides an optional programmable spread spectrum (clock dithering) function that is activated by connecting a capacitor between DITHER and AGND. A triangular waveform centered at 1.0 V is generated across the dither capacitor. This triangular waveform modulates the oscillator frequency by –6% to +5% of the frequency set by the RT resistor. The dither capacitance value sets the rate of the low frequency modulation.

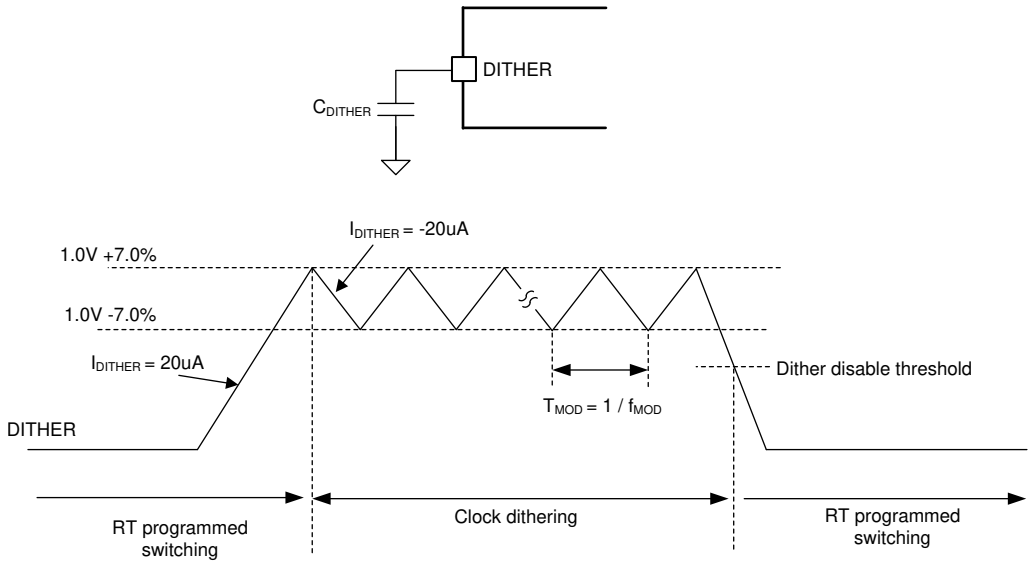


図 9-10. Switching Frequency Dithering

For the dithering circuit to effectively reduce peak EMI, the modulation frequency must be much less than the RT switching frequency. The dither capacitance, which is required for a given modulation frequency (f_{MOD}), can be calculated from 式 8. Setting the f_{MOD} to 9 kHz or 10 kHz is a good starting point.

$$C_{DITHER} = \frac{20\mu A}{f_{MOD} \times 0.29} \quad (8)$$

Connecting DITHER to AGND deactivates clock dithering, and the internal oscillator operates at a fixed frequency set by the RT resistor. Clock dithering is also disabled when an external synchronization pulse is applied.

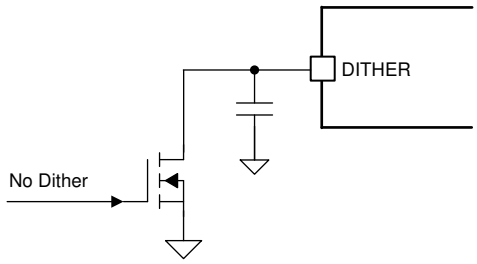


図 9-11. Dynamic Dither On/Off Example

Connecting STATUS to DITHER enables the clock dithering when the STATUS pin is pulled down to ground and also enables the internal charge pump during bypass operation when the STATUS pin is pulled up.

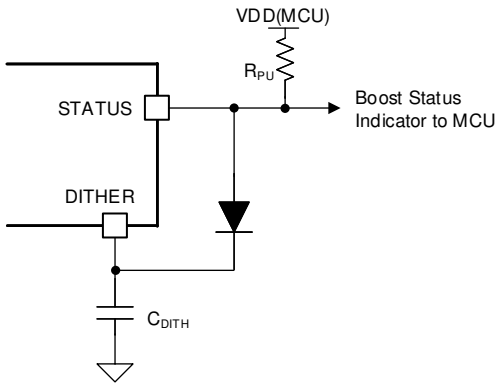


図 9-12. Enable Clock Dithering and Internal Charge Pump Together

9.3.12 Programmable Soft Start (SS Pin)

The soft-start feature helps the converter gradually reach the steady state operating point. To reduce start-up stresses and surges, the device regulates the error amplifier reference to the SS pin voltage or the TRK pin voltage (V_{TRK}), whichever is lower.

The internal 20-µA soft-start (I_{SS}) current turns on 120 µs after the VCC pin crosses $V_{VCC-UVLO}$. I_{SS} gradually increases the voltage on an external soft-start capacitor (C_{SS}). This results in a gradual rise of the output voltage.

In FPWM mode, the device forces diode emulation while the SS pin voltage is less than 1.5 V. When the SS pin voltage is greater than 1.5 V, the device changes the zero current detection (ZCD) threshold gradually from 4 mV to –145 mV to achieve a smooth transition from diode emulation to FPWM mode.

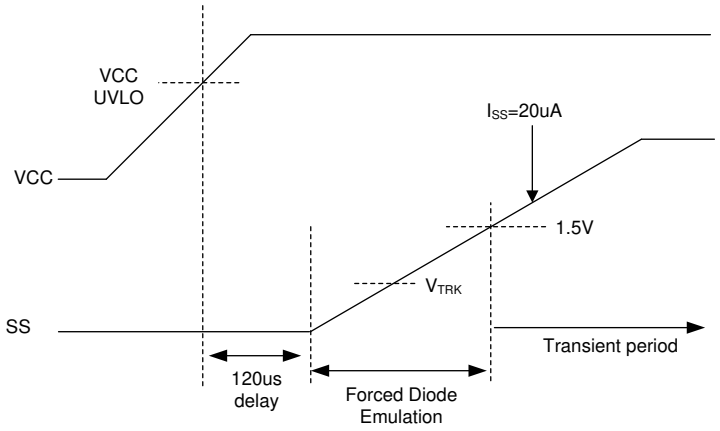


図 9-13. Soft Start and Smooth Transition to FPWM

In boost topology, the soft-start time (t_{SS}) varies with the input supply voltage because the boost output voltage is equal to the boost input voltage at the beginning of the soft-start switching. t_{SS} in boost topology is calculated with 式 9.

$$t_{SS} = V_{TRK} \times \frac{C_{SS}}{20\mu A} \times \left(1 - \frac{V_{SUPPLY}}{V_{LOAD}}\right) \quad (9)$$

In general, it is recommended to choose a soft-start time long enough so that the converter can start up without going into an overcurrent state. If the device is used for a pre-boost in automotive application, it is recommended to use 100-pF C_{SS} to reach steady state as soon as possible.

The device also features an internal SS-to-FB clamp (V_{SS-FB}), which clamps SS 55 mV above FB and is activated if 256 consecutive switching cycles occur with current limit. The SS-to-FB clamp is deactivated if 32 consecutive switching cycles occur without exceeding the current limit threshold. This clamp helps to minimize surges after output shorts or over load situations. The device can enter deep sleep mode when SS is greater than 1.5 V. It is not recommended to pulldown SS to stop switching.

9.3.13 Wide Bandwidth Transconductance Error Amplifier and PWM (TRK, COMP Pin)

The device includes an internal feedback resistor voltage divider. The internal feedback resistor voltage divider is connected to the negative input of the internal transconductance error amplifier, and the TRK pin voltage programs the positive input of the internal transconductance error amplifier after the soft start is finished. The internal transconductance error amplifier features high output resistance (R_O = 10 MΩ) and wide bandwidth (BW = 3 MHz) and sinks (or sources) current, which is proportional to the difference between the negative and the positive inputs of the error amplifier.

The output of the error amplifier is connected to the COMP pin, allowing the use of a Type-2 loop compensation network. R_{COMP}, C_{COMP}, and an optional C_{HF} loop compensation components configure the error amplifier gain and phase characteristics to achieve a stable loop response. This compensation network creates a pole at very low frequency, a mid-band zero, and a high frequency pole.

The PWM comparator in 図 9-14 compares the sum of the amplified sensed inductor current and the slope compensation ramp with the sum of the COMP pin voltage and a –0.3-V internal offset, and terminates the present cycle if the sum of the amplified sensed inductor current and the slope compensation ramp is greater than the sum of the COMP pin voltage and the –0.3-V internal offset.

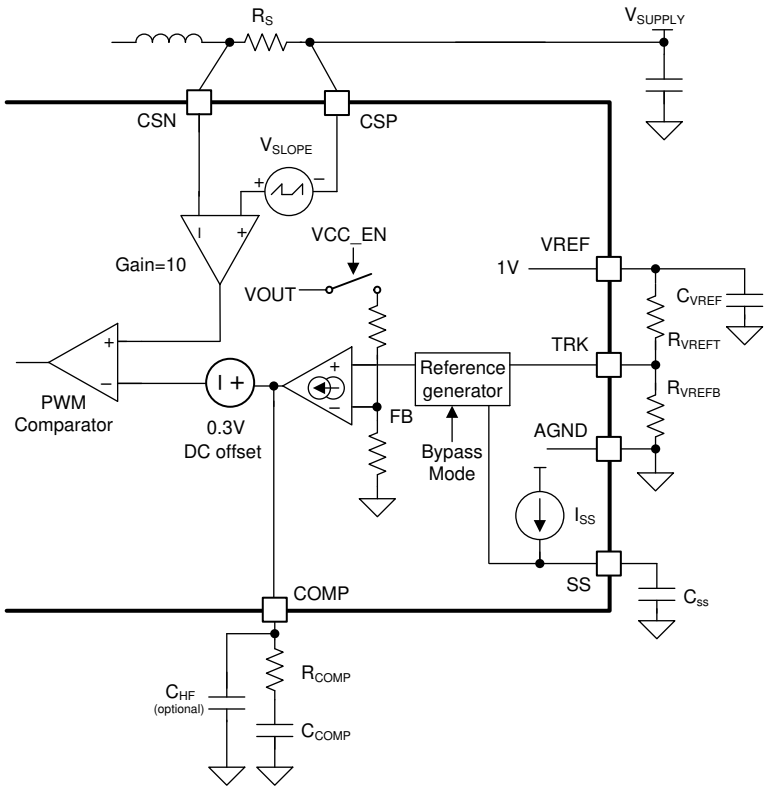


図 9-14. Error Amplifier, Current Sense Amplifier, and PWM

9.3.14 Current Sensing and Slope Compensation (CSP, CSN Pin)

The device features a current sense amplifier with an effective gain of 10 (A_{CS}), and provides an internal slope compensation ramp to the PWM comparator to prevent a subharmonic oscillation at high duty cycle. The device generates the 45-mV peak slope compensation ramp (V_{SLOPE}) at the input of the current sense amplifier, which is a 0.45-V peak (at 100% duty cycle) slope compensation ramp at the PWM comparator input.

According to peak current mode control theory, the slope of the slope compensation ramp must be greater than at least half of the sensed inductor current falling slope to prevent subharmonic oscillation at high duty cycle. Therefore, the minimum amount of the slope compensation must satisfy 式 10.

$$0.5 \times (V_{LOAD} - V_{SUPPLY}) / L_M \times R_S \times \text{Margin} < V_{SLOPE} \times f_{SW} \text{ (in Boost)} \quad (10)$$

where

- 1.5-1.7 is recommended as the margin to cover non-ideal factors.

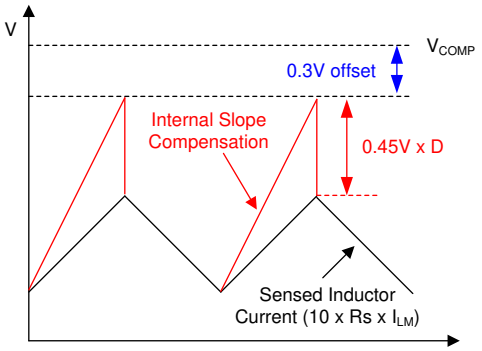


図 9-15. PWM Comparator Input

9.3.15 Constant Peak Current Limit (CSP, CSN Pin)

When the CSP-CSN voltage exceeds the 60-mV cycle-by-cycle current limit threshold (V_{CLTH}), the current limit comparator immediately terminates the LO output. The device provides an constant peak current limit whose peak inductor current limit is constant over the input and output voltage. For the case where the inductor current can overshoot, such as inductor saturation, the current limit comparator skips pulses until the current has decayed below the current limit threshold.

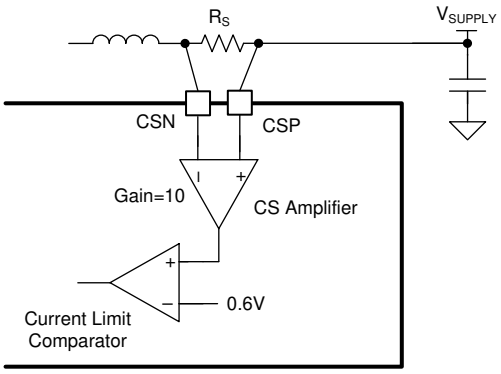


図 9-16. Current Limit Comparator

Cycle-by-cycle peak current limit is calculated as follows:

$$I_{PEAK-CL} = \frac{0.06}{R_S} \quad (11)$$

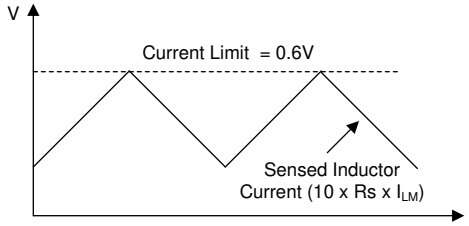


図 9-17. Current Limit Comparator Input

Boost converters have a natural pass-through path from the supply to the load through the high-side MOSFET body diode. Due to this path, boost converters cannot provide the peak current limit protection when the output voltage is close to or less than the input supply voltage, especially the peak current limit protection that does not work during the minimum on time (t_{ON-MIN}).

9.3.16 Maximum Duty Cycle and Minimum Controllable On-Time Limits

The device provides the maximum duty cycle limit (D_{MAX}) and minimum off time to cover the non-ideal factors caused by resistive elements. D_{MAX} decides the minimum input supply voltage ($V_{SUPPLY(MIN)}$), which can achieve the target output voltage (V_{LOAD}) during CCM operation, but $V_{SUPPLY(MIN)}$, which can achieve the target output voltage during DCM operation, is not limited by D_{MAX}. $V_{SUPPLY(MIN)}$, which can achieve the target output voltage during CCM operation, can be estimated as follows. See also 図 8-17.

$$V_{SUPPLY(MIN)} \approx V_{LOAD} \times (1 - D_{MAX}) + I_{SUPPLY(MAX)} \times (R_{DCR} + R_S + R_{DS(ON)}) \quad (12)$$

where

- $I_{SUPPLY(MAX)}$ is the maximum input current at $V_{SUPPLY(MIN)}$.
- R_{DCR} is the DC resistance of the inductor.
- $R_{DS(ON)}$ is the turn-on resistance of the MOSFET.

At very light-load condition or when V_{SUPPLY} is close to $V_{OUT-REG}$, the device skips the low-side driver pulses if the required on time is less than t_{ON-MIN}. This pulse skipping appears as a random behavior. If V_{SUPPLY} is further increased to the voltage higher than $V_{OUT-REG}$, the required on time becomes 0 and eventually the device can start bypass operation (LM5152-Q1 only), which turns on the high-side driver 100% when the VOUT pin voltage is greater than V_{OVTH}.

9.3.17 Deep Sleep Mode and Bypass Operation (HO, CP Pin)

When SS is greater than 1.5 V, the device enters deep sleep mode after at least 40 µs in OVP status. The device re-enters active mode if V_{OUT} falls down below V_{OVP}. During bypass operation, the loss, which is caused by the body diode of the high-side MOSFET, is minimized. The high-side driver of the LM51521-Q1 does not turn on in the deep sleep mode. See セクション 9.4.1.5 for more information.

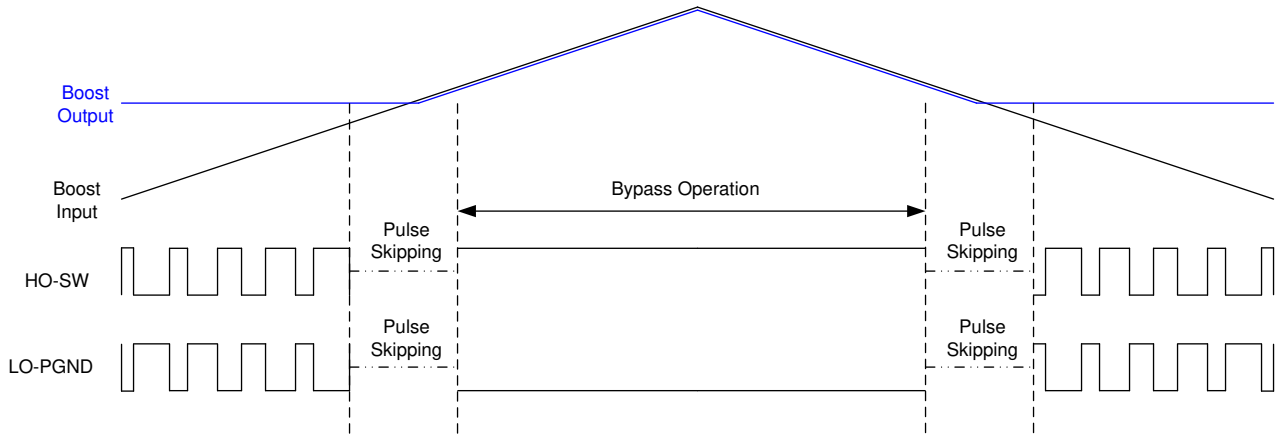


図 9-18. PWM to Bypass Transition in CCM Operation

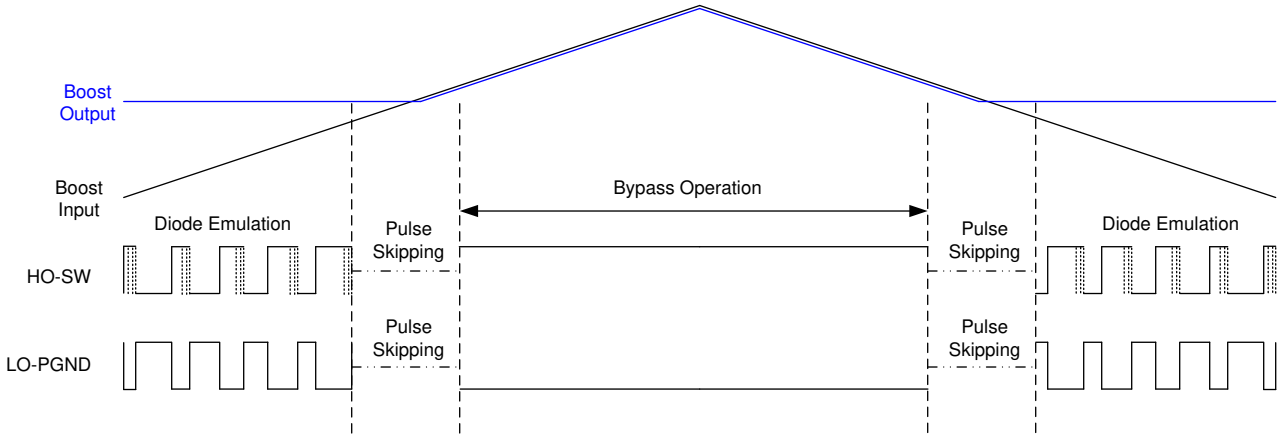


図 9-19. PWM to Bypass Transition in DCM Operation

9.3.18 MOSFET Drivers, Integrated Boot Diode, and Hiccup Mode Fault Protection (LO, HO, HB Pin)

The device provides N-channel logic MOSFET drivers, which can source a peak current of 2.2 A and sink a peak current of 3.3 A. The LO driver is powered by VCC, and is enabled when EN is greater than V_{EN} and VCC is greater than $V_{VCC-UVLO}$. The HO driver is powered by HB, and is enabled when EN is greater than V_{EN} and HB-SW voltage is greater than HB UVLO threshold ($V_{HB-UVLO}$).

When the SW pin voltage is approximately 0 V by turning on the low-side MOSFET, the C_{HB} is charged from VCC through the internal boot diode. The recommended value of the C_{HB} is 0.1 µF.

The LO and HO outputs are controlled with an adaptive dead-time methodology, which makes sure that both outputs are not turned on at the same time. When the device commands LO to be turned on, the adaptive dead-time logic first turns off HO and waits for HO-SW voltage to drop. LO is then turned on after a small delay (t_{DHL}).

Similarly, the HO driver turn-on is delayed until the LO-PGND voltage has discharged. HO is then turned on after a small delay (t_{DLH}).

If the BIAS pin voltage is below the 5-V VCC regulation target, take extra care when selecting the MOSFETs. The gate plateau voltage of the MOSFET switch must be less than the BIAS pin voltage to completely enhance the MOSFET, especially during start-up at low BIAS pin voltage. If the driver output voltage is lower than the MOSFET gate plateau voltage during start-up, the converter may not start up properly and it can stick at the maximum duty cycle in a high-power dissipation state. This condition can be avoided by selecting a lower threshold MOSFET or by turning on the device when the BIAS pin voltage is sufficient. Care should be taken when the converter operates in bypass at any conditions. During the bypass operation, the minimum HO-SW voltage is 3.75 V.

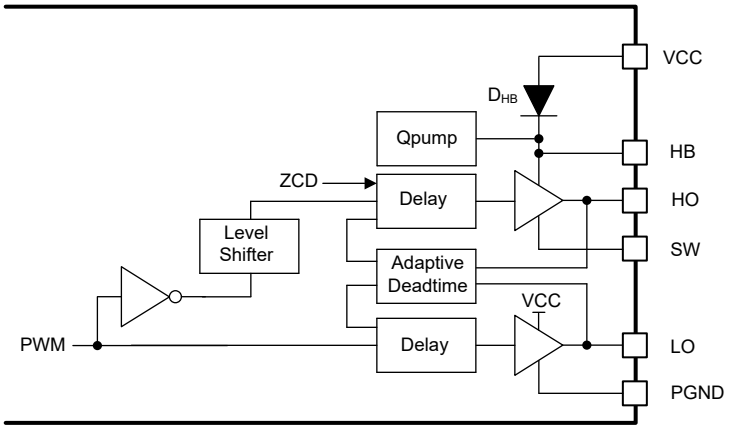


図 9-20. Driver Structure with Internal Boot Diode

The hiccup mode fault protection is triggered by the HB UVLO. If the HB-SW voltage is less than the HB UVLO threshold ($V_{HB-UVLO}$), the LO turns on by force for 75 ns to replenish the boost capacitor. The device allows up to four consecutive replenish switching. After the maximum four consecutive boot replenish switching, the device skips switching for 12 cycles. If the device fails to replenish the boost capacitor after the four sets of the four consecutive replenish switching, the device stops switching and enters 512 cycles of hiccup mode off time. During the hiccup mode off time, SS is grounded.

If required, the slew rate of the switching node voltage can be adjusted by adding a gate resistor in parallel with a pulldown PNP transistor. Extra care should be taken when adding the gate resistor because it can decrease the effective dead time.

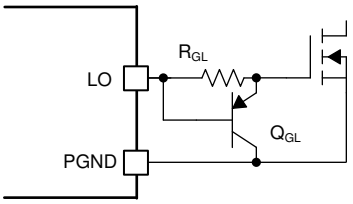


図 9-21. Slew Rate Control

9.3.19 Thermal Shutdown Protection

An internal thermal shutdown (TSD) is provided to protect the device if the junction temperature (T_J) exceeds 175°C. When TSD is activated, the device is forced into a low-power thermal shutdown state with the MOSFET drivers and the VCC regulator disabled. After the T_J is reduced (typical hysteresis is 15ºC), the device restarts. The TSD is disabled during sleep or deep sleep mode.

9.4 Device Functional Modes

9.4.1 Device Status

9.4.1.1 Shutdown Mode

When EN is less than V_{EN} and VH is less than V_{SYNC}, the device shuts down, consuming 3 µA from BIAS. In shutdown mode, COMP, SS, and STATUS are grounded. The device is enabled when EN is greater than V_{EN} or VH is greater than V_{SYNC}.

9.4.1.2 Configuration Mode

When the device is enabled initially, the 120-µs device configuration starts if VCC is greater than $V_{VCC-UVLO}$. During device configuration, the light load switching mode is selected. The device configuration is reset when the device shuts down or VCC falls down below 2.2 V. The preferred way to reconfigure the device is to shut down the device. During the configuration time, a 33-kΩ internal EN pulldown resistor is connected, the minimum sourcing capability of the VCC regulator is 100 mA and the RT pin is regulated to 0.5 V by the internal RT regulator.

9.4.1.3 Active Mode

After the 120-µs initial device configuration is finished, the device enters active mode with all functions enabled if UVLO is greater than V_{UVLO}. In active mode, a soft-start sequence starts and the error amplifier is enabled.

9.4.1.4 Sleep Mode

When skip mode is selected as the light load switching mode and SS is greater than 1.5 V, the device enters sleep mode if the low-side driver skips switching for 16 consecutive cycles. Once the device enters sleep mode, the device cannot re-enter active mode during 8-µs minimum sleep time. During sleep mode, the device stops the internal oscillator to reduce the operating current, disables UVLO comparator, disables the error amplifier, and parks the COMP pin at 0.25 V. The device re-enters active mode if the VOUT pin voltage falls down below the wake up threshold (V_{WAKE}), which is 1.1% lower than $V_{OUT-REG}$.

9.4.1.5 Deep Sleep Mode

When SS is greater than 1.5 V, the device enters deep sleep mode after four cycles in OVP status. During deep sleep mode, the device stops the internal oscillator to reduce the operating current, disables UVLO comparator, disables the error amplifier, and parks the COMP pin at 0.25 V.

In FPWM or DE mode, the device re-enters active mode if V_{OUT} falls down below V_{OVTH}. In skip mode, the device re-enters active mode if VOUT falls down below V_{OVTH}, then immediately enters sleep mode after 16 consecutive cycles of pulse skipping.

9.4.2 Light Load Switching Mode

The device provides three light load switching modes. Inductor current waveforms in each mode are different at the light or no load condition.

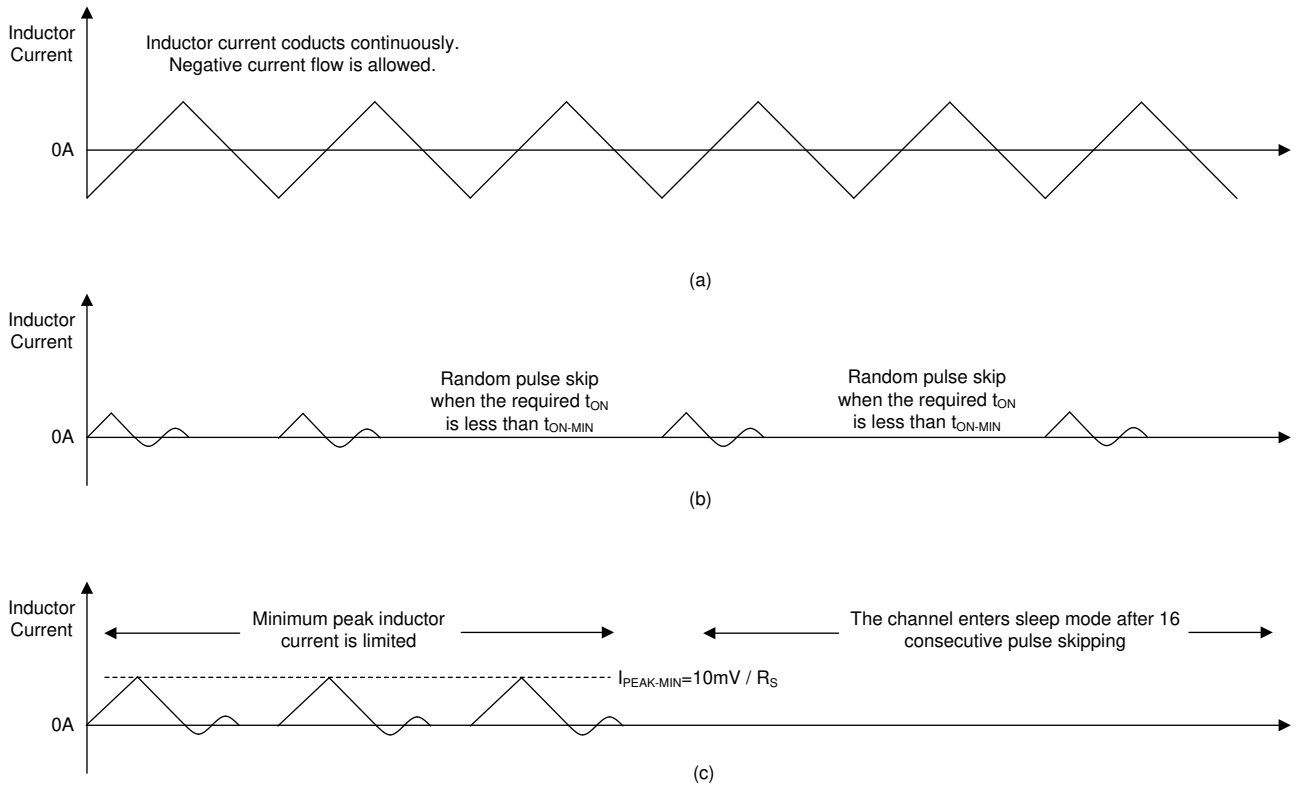


図 9-22. Inductor Current Waveform at Light Load (a) FPWM (b) Diode Emulation (c) Skip Mode

9.4.2.1 Forced PWM (FPWM) Mode

In FPWM mode, the inductor current conducts continuously at light or no load conditions, allowing a continuous conduction mode (CCM) operation. The benefits of FPWM mode are a fast light load to heavy load transient response and constant switching frequency at light or no load conditions. The maximum reverse current is limited to 145 mV/$R_{DS(ON)}$ in FPWM mode.

9.4.2.2 Diode Emulation (DE) Mode

In diode emulation (DE) mode, inductor current flow is allowed only in one direction – from the input source to the output load. The device monitors the SENSE-SW voltage during the high-side switch on time and turns off the high-side switch for the remainder of the PWM cycle when the SENSE-SW voltage falls down below the 5-mV zero current detection (ZCD) threshold (V_{ZCD}). The benefit of the diode emulation is a higher efficiency than FPWM mode efficiency at light load condition.

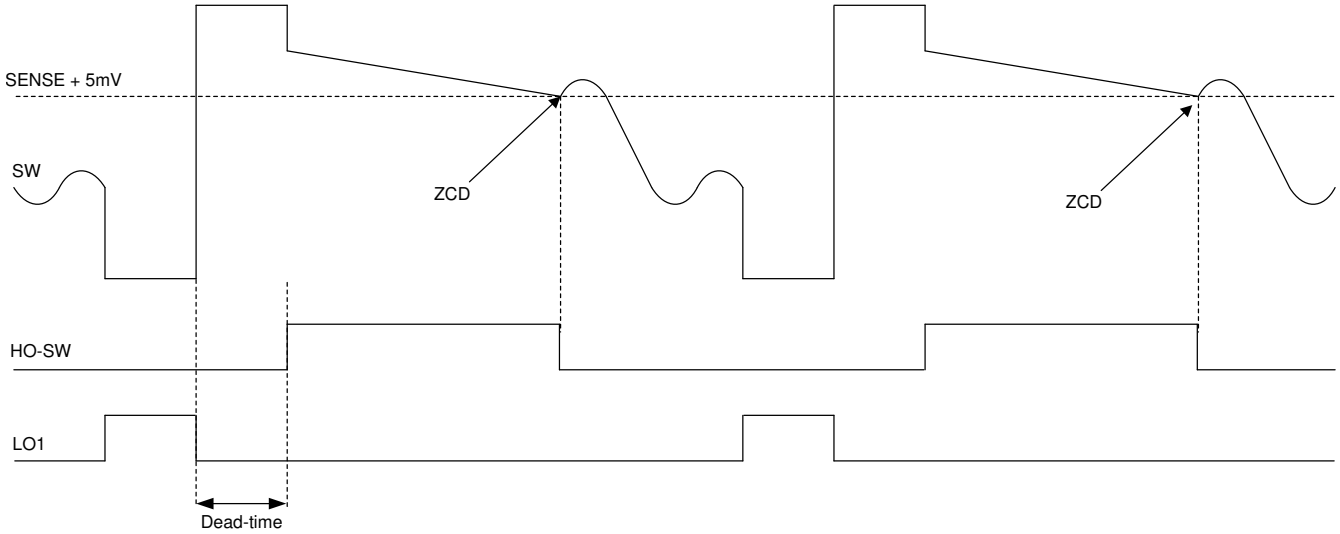


図 9-23. Zero Current Detection

9.4.2.3 Forced Diode Emulation Operation in FPWM Mode

During soft start, the device forces diode emulation while the SS pin voltage is less than 1.5 V. When the SS pin is greater than 1.5 V, the device reduces the zero current detection (ZCD) threshold down to –145 mV. The peak-to-peak inductor current must satisfy 式 13 for a proper FPWM operation at no load.

$$\frac{I_{PP} \times R_{DS(on)}}{2} < 145mV \tag{13}$$

9.4.2.4 Skip Mode

When skip mode is selected as the light load switching mode, the device enters sleep mode when the pulse skip counter detects 16 consecutive cycles of pulse skipping in the active mode, and re-enters the active mode if VOUT falls down below V_{WAKE}.

The light load efficiency can be increased by entering sleep mode more frequently and staying in sleep mode longer. In skip mode and when SS is greater than 1.5 V, the device works in the diode emulation, but the minimum peak current is limited to 10 mV/R_S once the low-side driver turns on. By limiting the minimum peak current, the boost converter is able to supply more current than what is required when switching, and enters sleep mode more frequently and stays longer in the sleep mode.

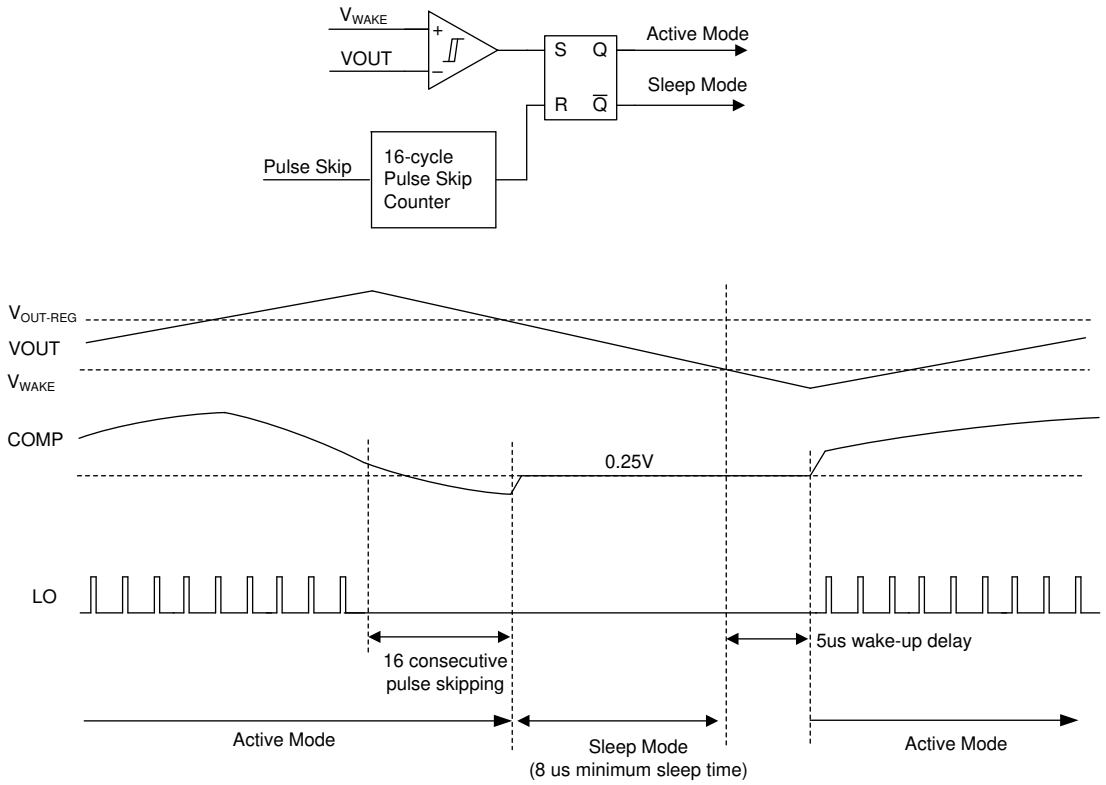


図 9-24. Skip Mode Operation

When skip mode is selected as the light load switching mode, L_M should be selected for the peak inductor to reach the 10m-V minimum peak current limit before LO turns off by D_{MAX} at the minimum V_{SUPPLY}.

10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

The device integrates several optional features to meet system design requirements, including input UVLO, programmable soft start, clock synchronization, spread spectrum, and selectable light load switching mode. Each application incorporates these features as needed for a more comprehensive design.

10.2 Typical Application

図 10-1 shows all optional components to design a boost converter.

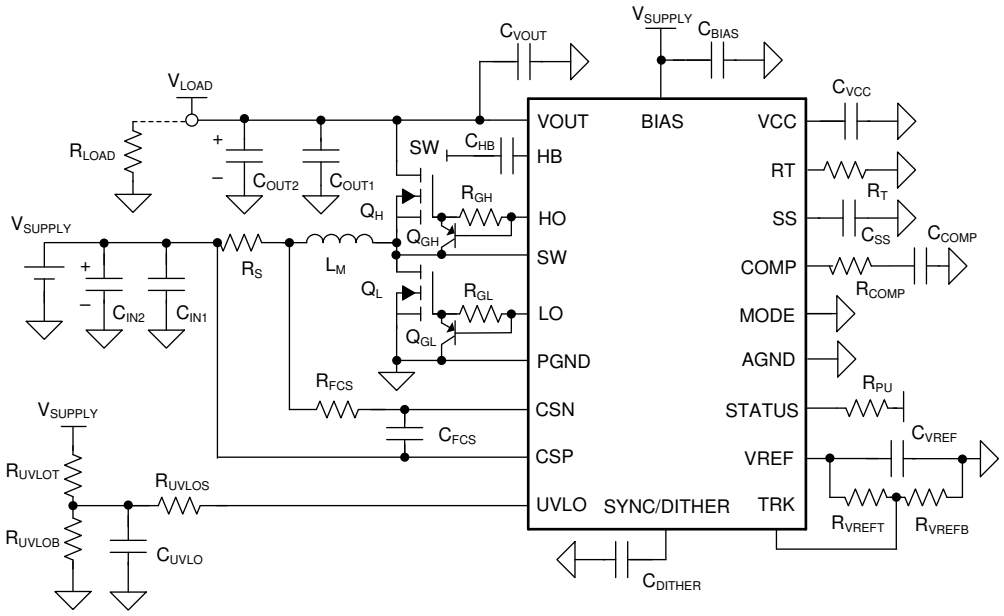


図 10-1. Typical Synchronous Boost Converter with Optional Components

10.2.1 Design Requirements

表 10-1 shows the intended input, output, and performance parameters for this application example.

表 10-1. Design Example Parameters

Design Parameter	Value
Minimum input supply voltage ($V_{SUPPLY(MIN)}$)	2.5 V
Target output voltage (V_{LOAD})	8.5 V
Maximum load current (I_{LOAD})	4 A (96 W)
Typical switching frequency (f_{SW})	440 kHz

10.2.2 Detailed Design Procedure

Use the *LM5152-Q1 Quick Start Calculator* or *LM51521-Q1 Quick Start Calculator* to expedite the process of designing of a regulator for a given application.

Refer to the *LM5152EVM-BST User's Guide* for recommended components and typical application curves.

10.2.2.1 Application Ideas

For applications requiring the lowest cost with minimum conduction loss, inductor DC resistance (DCR) can be used to sense the inductor current rather than using a sense resistor. R_{DCRC} and C_{DCRC} must meet 式 14 to match a time constant.

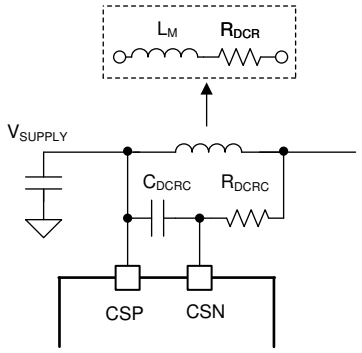


図 10-2. DCR Current Sensing

$$\frac{L_M}{R_{DCR}} = R_{DCRC} \times C_{DCRC} \tag{14}$$

Add a diode from STATUS to DITHER if the clock dithering is required in active mode and the bypass operation is required in deep sleep mode.

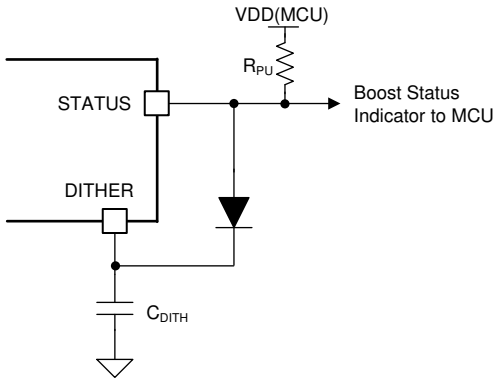


図 10-3. Enable Both Clock Dithering and Bypass Operation

10.2.3 Application Curves

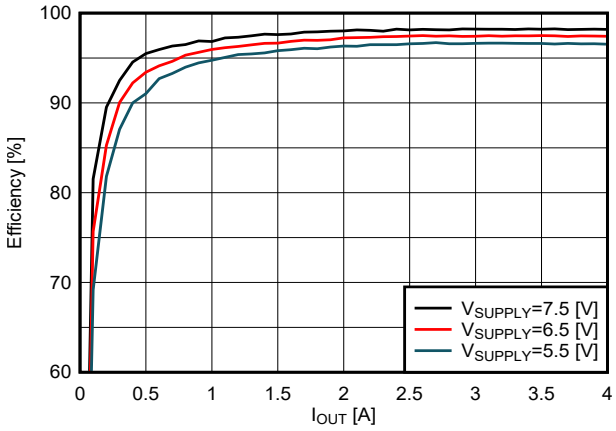


図 10-4. Efficiency vs. I_{OUT}, V_{OUT} = 8.5 V (FPWM)

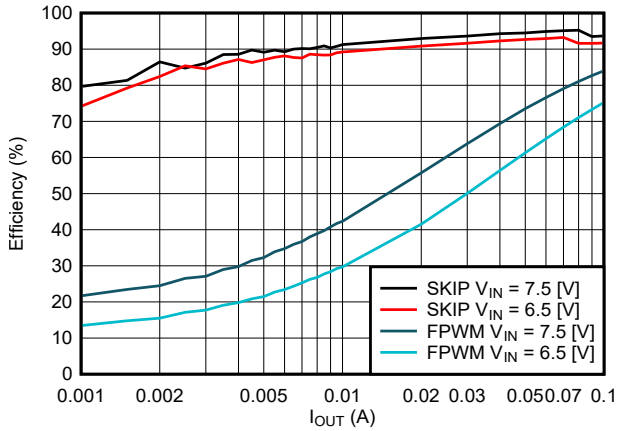


図 10-5. Efficiency vs. I_{OUT}, V_{OUT} = 8.5-V Light Load

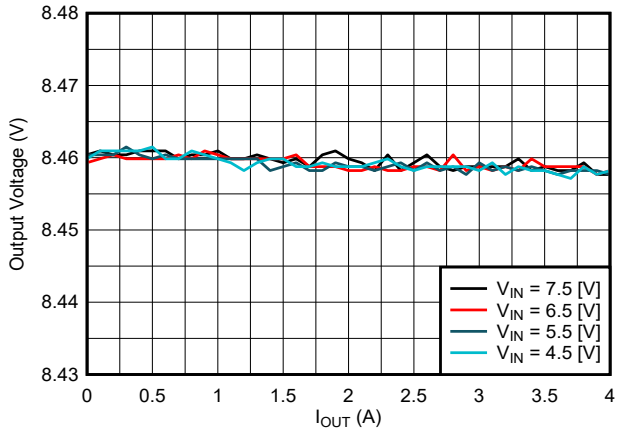


図 10-6. 8.5-V Load Regulation

10.3 System Example

Use the LM5152-Q1 in automotive pre-boost applications. The device can turn on the high-side switch 100% when car battery voltage is in normal range.

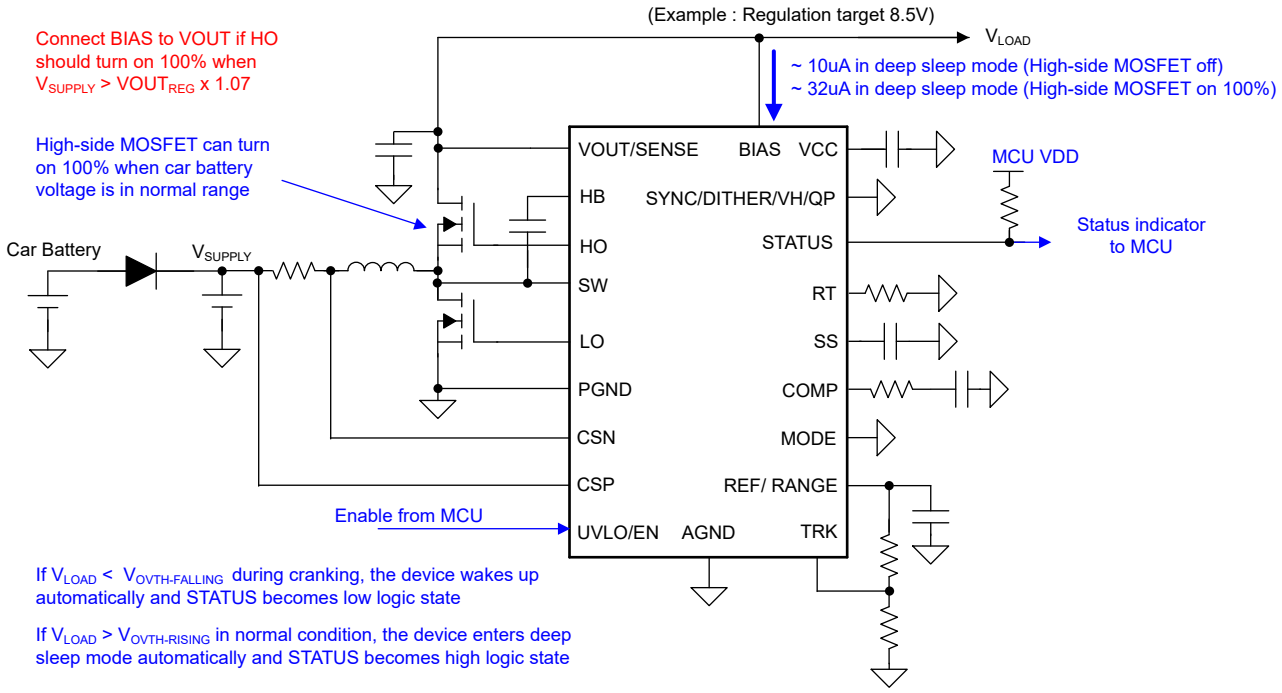


図 10-7. LM5152-Q1 in Automotive Pre-boost Application

Use the LM51521-Q1 in emergency call or backup battery booster application. The LM51521-Q1 turns off the high-side switch when car battery voltage is in normal range.

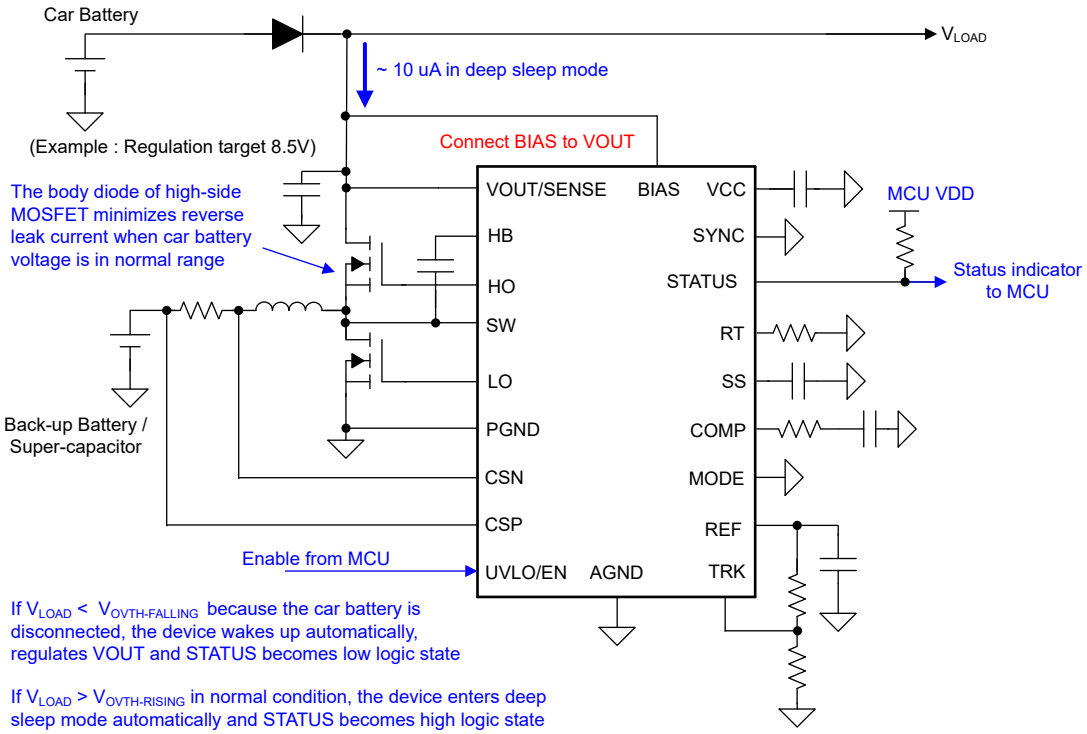


図 10-8. LM51521 in Emergency Call/Backup Battery Booster Application

To configure non-synchronous boost converter, connect SW to PGND, and connect HB to VCC.

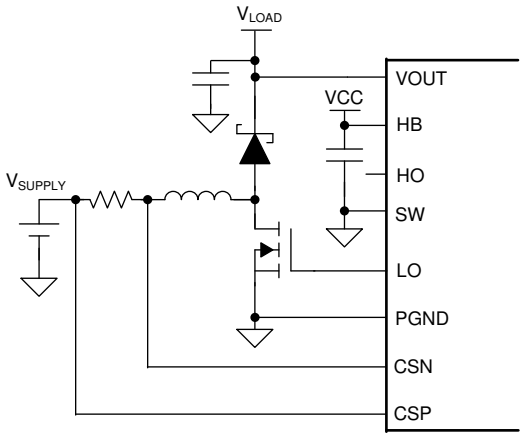


図 10-9. Non-Synchronous Boost Configuration

11 Power Supply Recommendations

The device is designed to operate from a power supply or a battery that has a voltage range is from 0.8 V to 42 V. The input power supply must be able to supply the maximum boost supply voltage and handle the maximum input current at 0.8 V. The impedance of the power supply and battery including cables must be low enough that an input current transient does not cause an excessive drop. Additional input ceramic capacitors can be required at the supply input of the converter.

12 Layout

12.1 Layout Guidelines

The performance of switching converters heavily depends on the quality of the PCB layout. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimize generation of unwanted EMI.

- Place C_{VCC}, C_{BIAS}, C_{HB}, and C_{VOUT} as close to the device. Make direct connections to the pins.
- Place Q_H, Q_L, and C_{OUT}. Make the switching loop (C_{OUT} to Q_H to Q_L to C_{OUT}) as small as possible. A small size ceramic capacitor helps to minimize the loop length. Leave a copper area near the drain connection of Q_H for a thermal dissipation.
- Place L_M, R_S, and C_{IN}. Make the loop (C_{IN} to R_S to L_M to C_{IN}) as small as possible. A small size ceramic capacitor helps to minimize the loop length.
- Connect R_S to CSP-CSN. The CSP-CSN traces must be routed in parallel and surrounded by ground.
- Connect VOUT, HO, and SW. These traces must be routed in parallel using a short, low inductance path. VOUT must be directly connected the drain connection of Q_H. SW must be directly connected to the source connection of Q_H
- Connect LO and PGND. The LO-PGND traces must be routed in parallel using a short, low inductance path. PGND must be directly connected the source connection of Q_L.
- Place R_{COMP}, C_{COMP}, C_{SS}, C_{VREF}, R_{VREFT}, R_{VREFB}, R_T, and R_{UVLOB} as close to the device, and connect to a common analog ground plane.
- Connect the power ground plane (the source connection of the Q_L) to EP through PGND. Connect the common analog ground plane to EP through AGND. PGND and AGND must be connected underneath the device.
- Add several vias under EP to help conduct heat away from the device. Connect the vias to a large analog ground plane on the bottom layer.
- Do not connect C_{OUT} and C_{IN} grounds underneath the device and through the large analog ground plane that is connected to EP.

12.2 Layout Example

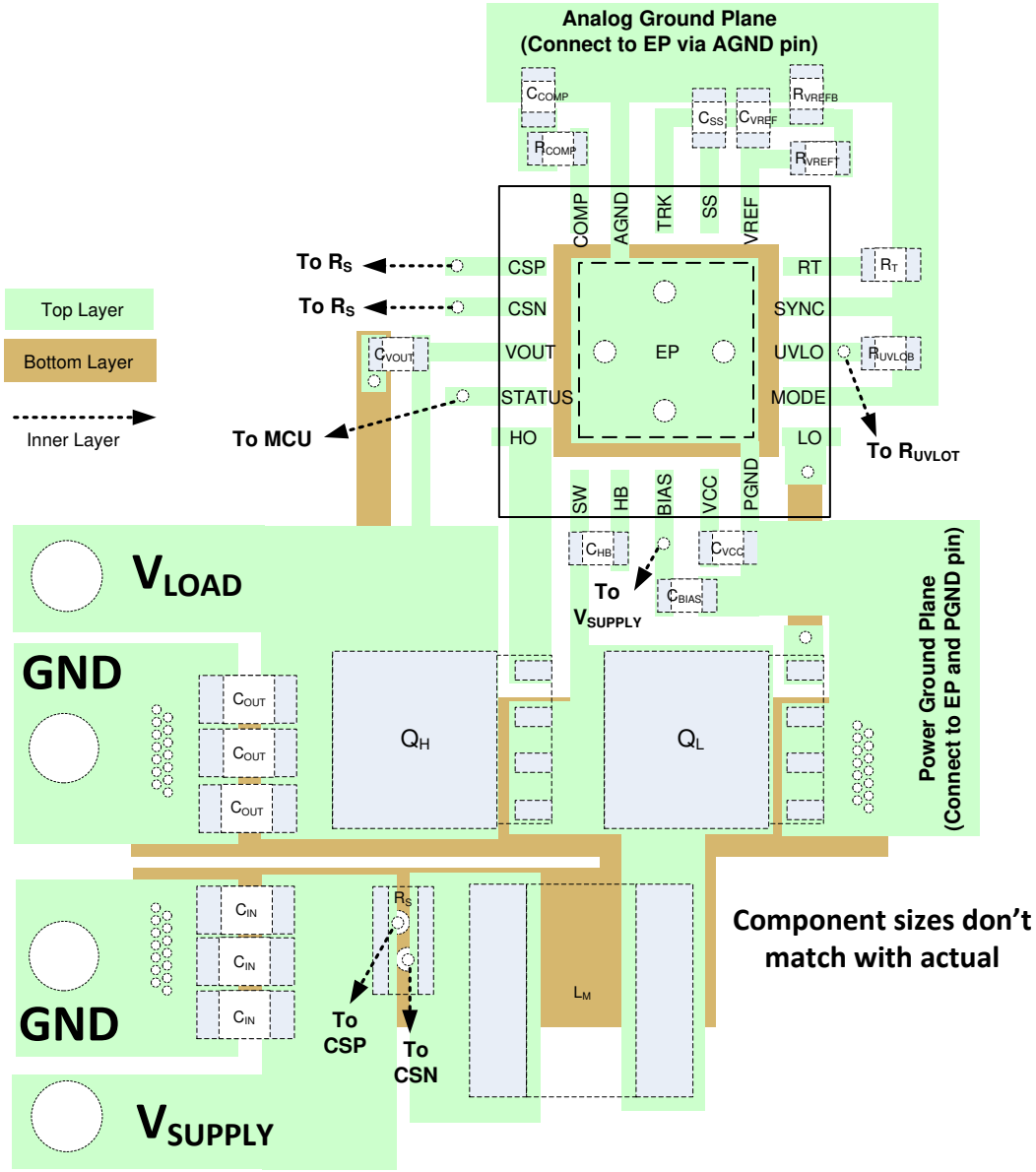


図 12-1. PCB Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM51521QRGRRQ1	Active	Production	VQFN (RGR) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	L51521
LM51521QRGRRQ1.A	Active	Production	VQFN (RGR) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	L51521
LM5152QRGRRQ1	Active	Production	VQFN (RGR) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	LM5152
LM5152QRGRRQ1.A	Active	Production	VQFN (RGR) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	LM5152

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

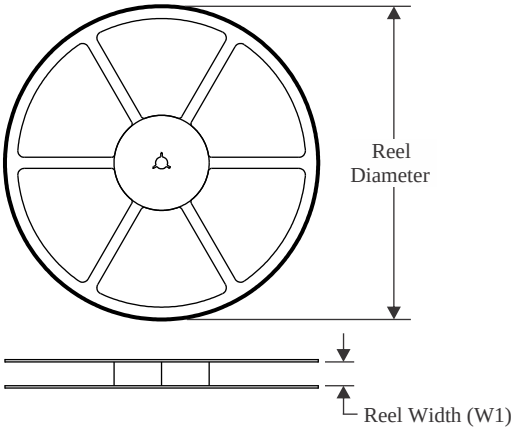
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

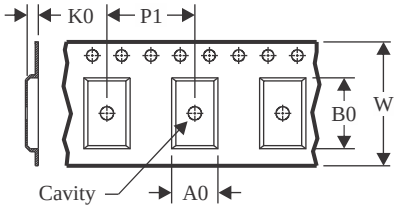
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

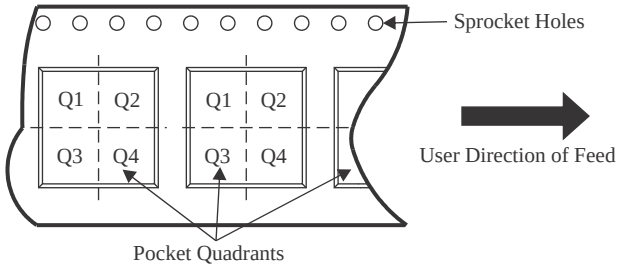


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

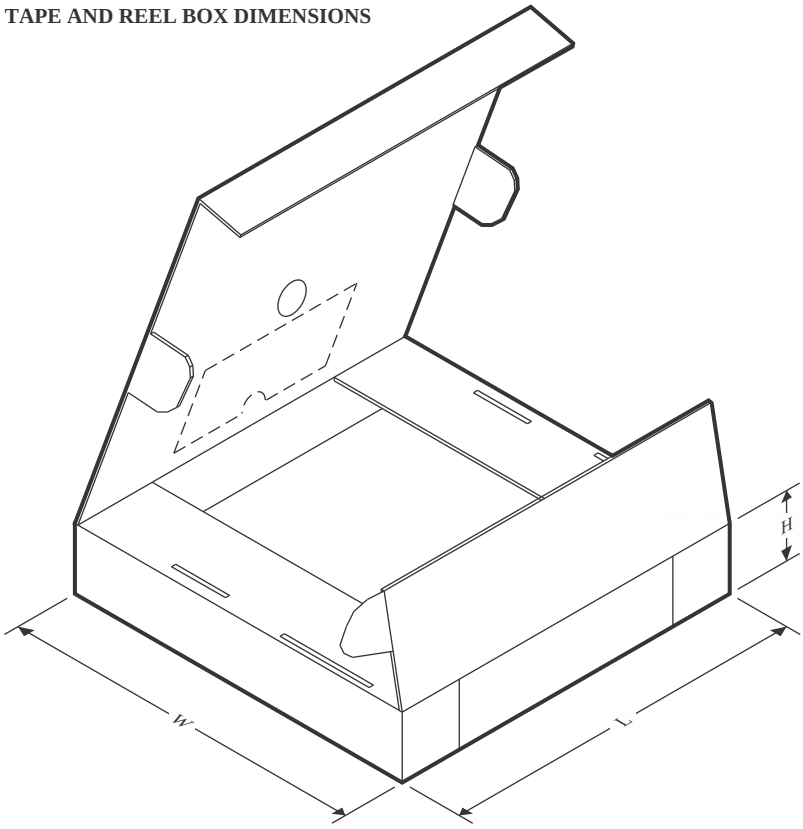
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM51521QRGRRQ1	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
LM5152QRGRRQ1	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM51521QRGRRQ1	VQFN	RGR	20	3000	367.0	367.0	35.0
LM5152QRGRRQ1	VQFN	RGR	20	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

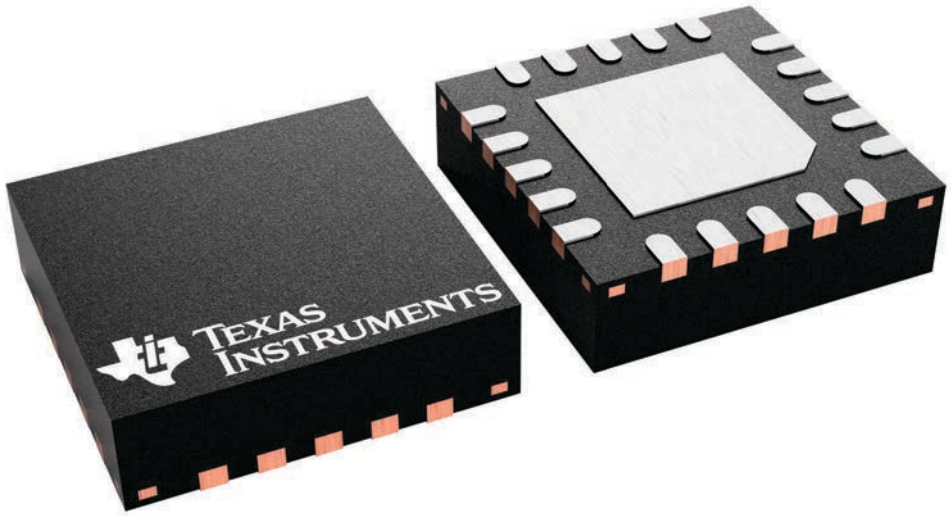
RGR 20

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



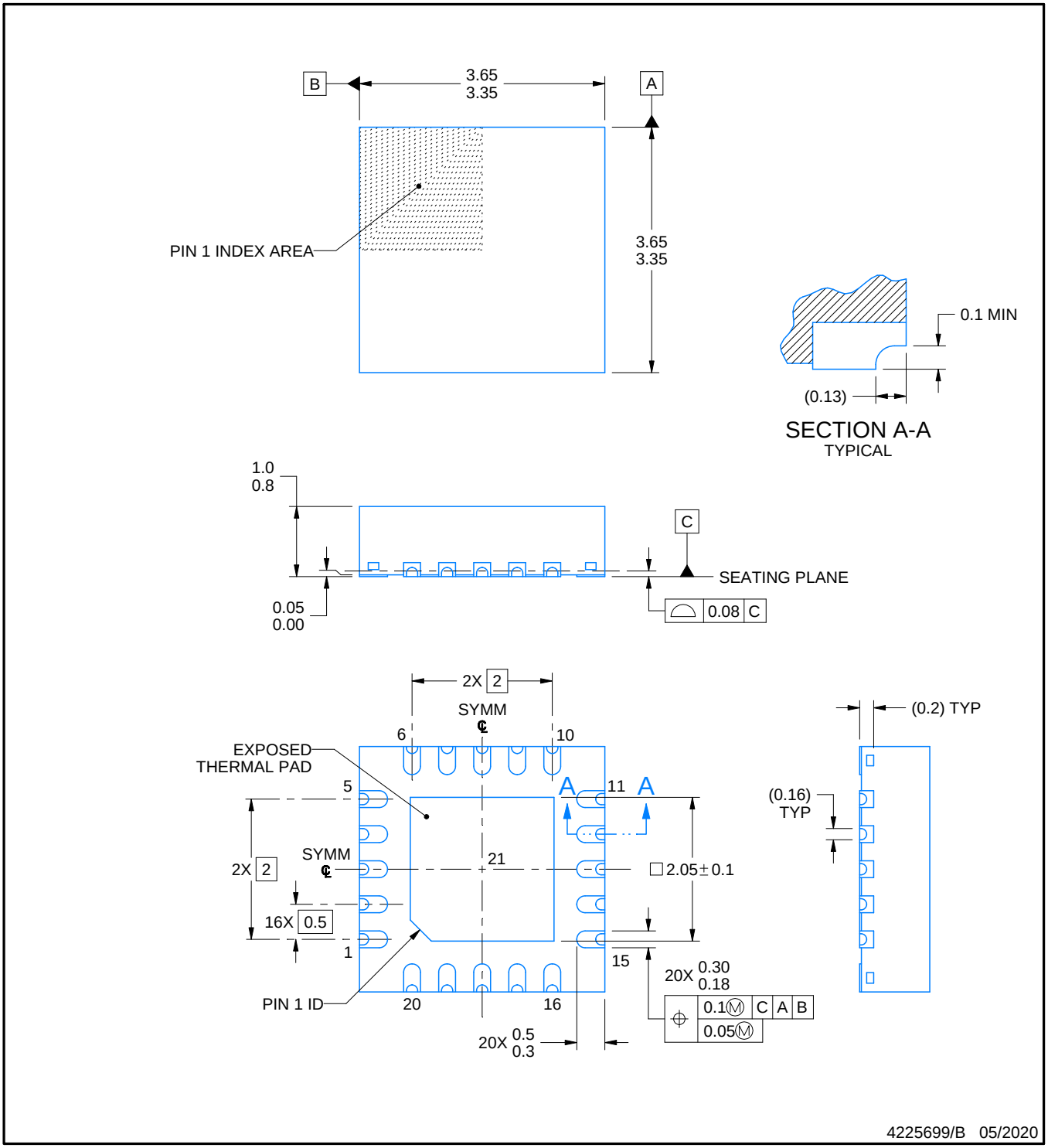
4228482/A

PACKAGE OUTLINE

RGR0020C

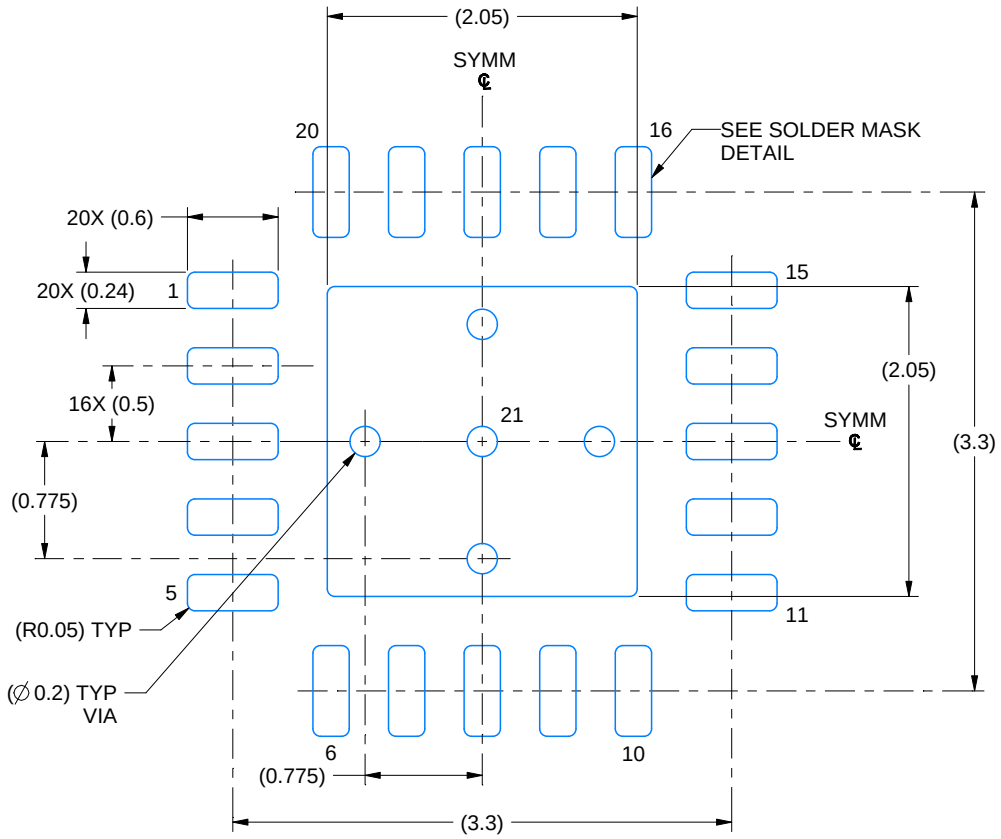
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

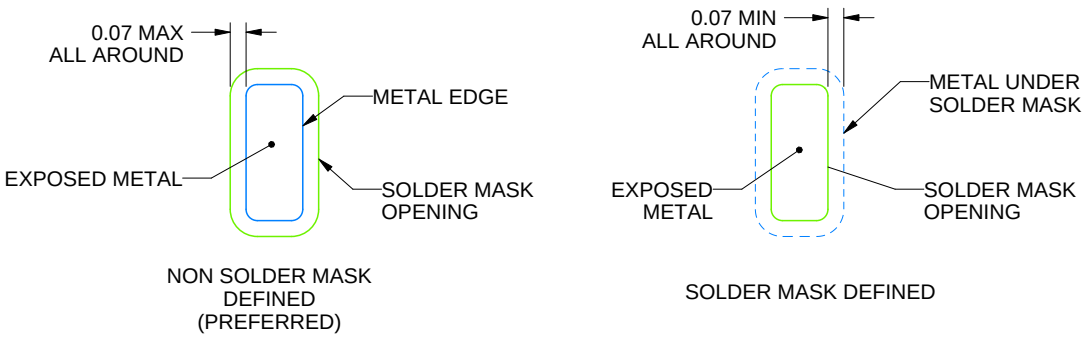


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

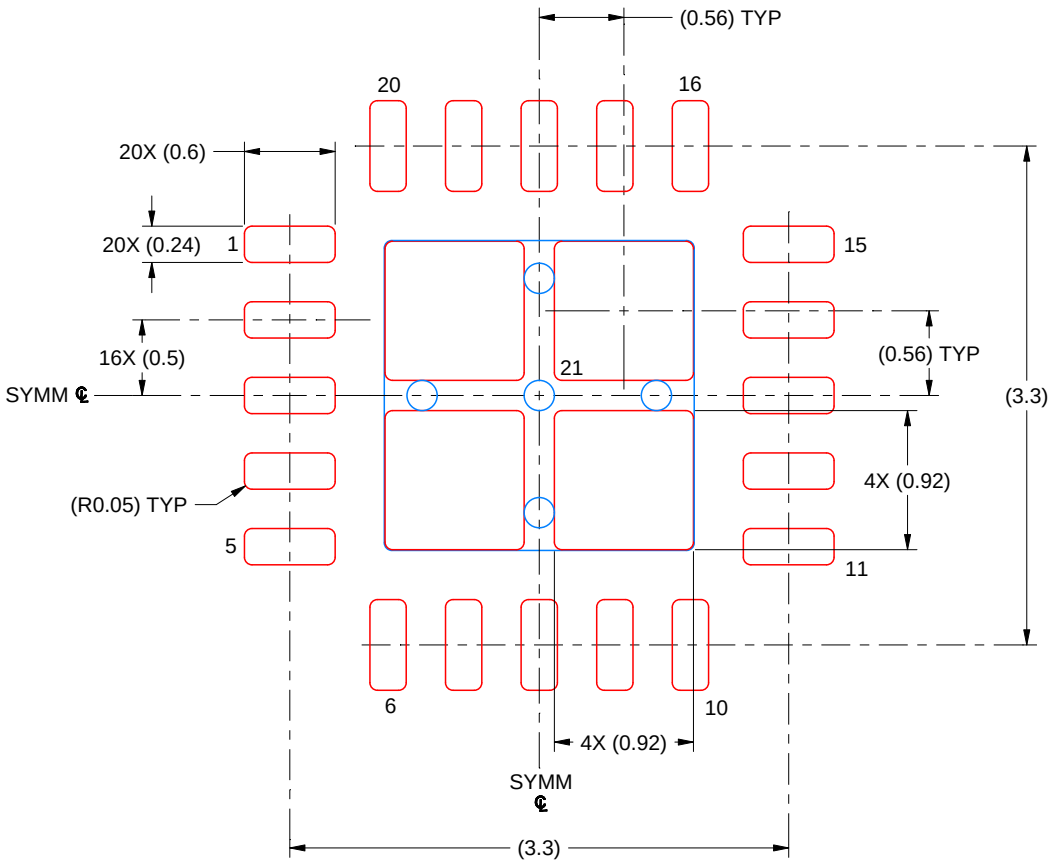


SOLDER MASK DETAILS

4225699/B 05/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月