TEXAS INSTRUMENTS
LM5137-Q1
JAJSV63A – AUGUST 2024 – REVISED AUGUST 2024

LM5137-Q1 車載用、 4V～80V、100% デューティ サイクル対応、デュアル チャネル同期整流降圧コントローラ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 1:–40℃～125℃の動作時周囲温度
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 機能安全準拠オプション – ASIL B および ASIL D – リクエストにより入手可能 (LM5137F-Q1)
- 多用途のデュアル同期整流降圧 DC/DC コントローラ
  - 4V～80V の広い入力電圧範囲
  - 精度 1% の固定 3.3V、5V、12V 出力または可変出力 (0.8V～60V)
  - 接合部温度:150℃ (最大値)
  - 100% デューティ サイクルに対応するチャージ ポンプ ゲート ドライバ
- 2 つのインターリーブ同期整流降圧チャネル
  - 2 チャネルまたは単一出力多相
  - 最大 4 相にスタック可能
  - SYNC In および SYNC Out 機能
- 堅牢な設計用の本質的な保護機能
  - ヒカップ モードによる過電流の内部保護
  - 独立した ENABLE および PGOOD 機能
  - 可変出力電圧ソフト スタート
  - VCC とゲート駆動の UVLO 保護
  - ヒステリシス付きのサーマル シャットダウン保護
- 超低 EMI 要件向けの設計
  - デュアル ランダム スペクトラム拡散機能 (DRSS)
  - スイッチング周波数:100kHz～2.5MHz
- ウェッタブル フランク付き VQFN-36 パッケージ
- WEBENCH® Power Designer により、LM5137-Q1 を使用するカスタム設計を作成

2 アプリケーション

- 車載用電子システム
- インフォテインメント システム、インストルメント クラスタ、ADAS
- ボディ エレクトロニクスおよび照明
- 高電圧バッテリ駆動システム

3 概要

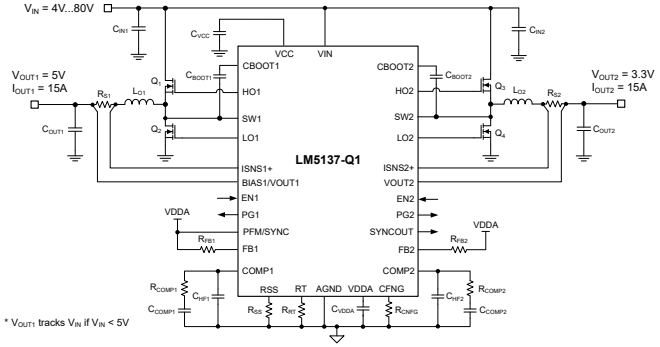
LM5137-Q1 は、80V の同期整流降圧 DC/DC コントローラ ファミリであり、機能安全を実現するための次の 3 つのオプションが用意されています。対応、ASIL B、ASIL D。インターリーブ方式のスタック可能なピーク電流モード アーキテクチャにより、容易なループ補償、高速な過渡応答、優れた負荷 / ライン制御、並列化した相での正確なカレント シェア (電流共有) を実現し、より大きな出力電流に対応します。

最小オン時間 15ns のハイサイド スイッチは大きい降圧率に対応できるため、12V、24V、48V の車載用入力から低電圧レールへの直接変換が可能になり、システムの設計コストと複雑性を下げることができます。LM5137-Q1 は、最低 4V の入力電圧ディップ時にも動作を継続でき、必要に応じて 100% のデューティ サイクルでも動作できます。無負荷時静止電流 (出力電圧をレギュレートした状態) は 12.7µA であるため、バッテリ駆動の車載用システムの動作時間を延長できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
LM5137-Q1	RHA (VQFN、36)	6.0mm × 6.0 mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



LM5137-Q1 デュアル出力降圧スイッチング レギュレータ - 概略回路図

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CISPR 25 および車載用 EMI 要件への準拠を容易にする複数の機能が搭載されています。大電流 MOSFET ゲート ドライバは、適応的にタイミングを制御し、スイッチング遷移時のボディ ダイオードの導通を最小限にとどめて、スイッチング損失を低減するとともに、高入力電圧および高スイッチング周波数時の熱および EMI 性能を高めます。入力コンデンサのリップル電流を小さくし、EMI フィルタを小型化するために、2 つの出力の 180° インターリーブ動作もサポートしています。90° 位相差のあるクロック出力は、カスケード、マルチチャネル、多相電力段に最適です。スイッチング周波数は、抵抗により最大 2.2MHz まで設定可能で、最大 2.5MHz の外部クロック ソースと同期できるため、ノイズに敏感な用途でビート周波数を除去できます。

LM5137-Q1 のその他の機能として、最大 150℃の接合部温度での動作、ユーザー選択可能な PFM モードによる軽負荷時消費電流の低減、設定可能なソフトスタート機能、オープンドレインの PG フラグによるフォルト報告と出力監視、独立したイネーブル入力、プリバイアスされた負荷への単調なスタートアップ、内蔵 VCC バイアス電源レギュレータ (VIN または BIAS1/VOUT1 から電源を供給)、ヒカップ モード過負荷保護、自動回復機能付きサーマル シャットダウン保護があります。電流検出では、インダクタの DCR を使用して最高水準の効率を実現できます。また、オプションのシャント抵抗を使用すれば、高精度を実現できます。

LM5137-Q1 コントローラは、車載用アプリケーション向けの AEC-Q100 グレード 1 に認定済みであり、6mm × 6mm の熱特性強化された 36 ピンの VQFN パッケージに搭載されています。また、信頼性向上のための追加ピン クリアランスとウェッタブル フランク ピン付きで、製造中の光学検査が容易になります。広い入力電圧範囲、低い静止電流消費、高温での動作、サイクルごとの電流制限、低い EMI シグネチャ、小型設計サイズにより、堅牢性と耐久性の強化向上が求められるアプリケーションに最適なポイント オブ ロード レギュレータ ソリューションを実現できます。

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4 Device Comparison Table

表 4-1. Orderable Part Numbers

GENERIC PART NUMBER	ORDERABLE PART NUMBER	FUNCTIONAL SAFETY CLASSIFICATION(1)	PRODUCT DATA SHEET
LM5137-Q1	LM5137QRHARQ1	Functional safety-capable	This data sheet
LM5137F-Q1	LM5137FBQRHARQ1	ASIL B functional safety-compliant	Request here
	LM5137FDQRHARQ1	ASIL D functional safety-compliant	

(1) Refer to the functional safety homepage to understand the different functional safety classifications (in terms of the development process, analysis report, and diagnostics description).

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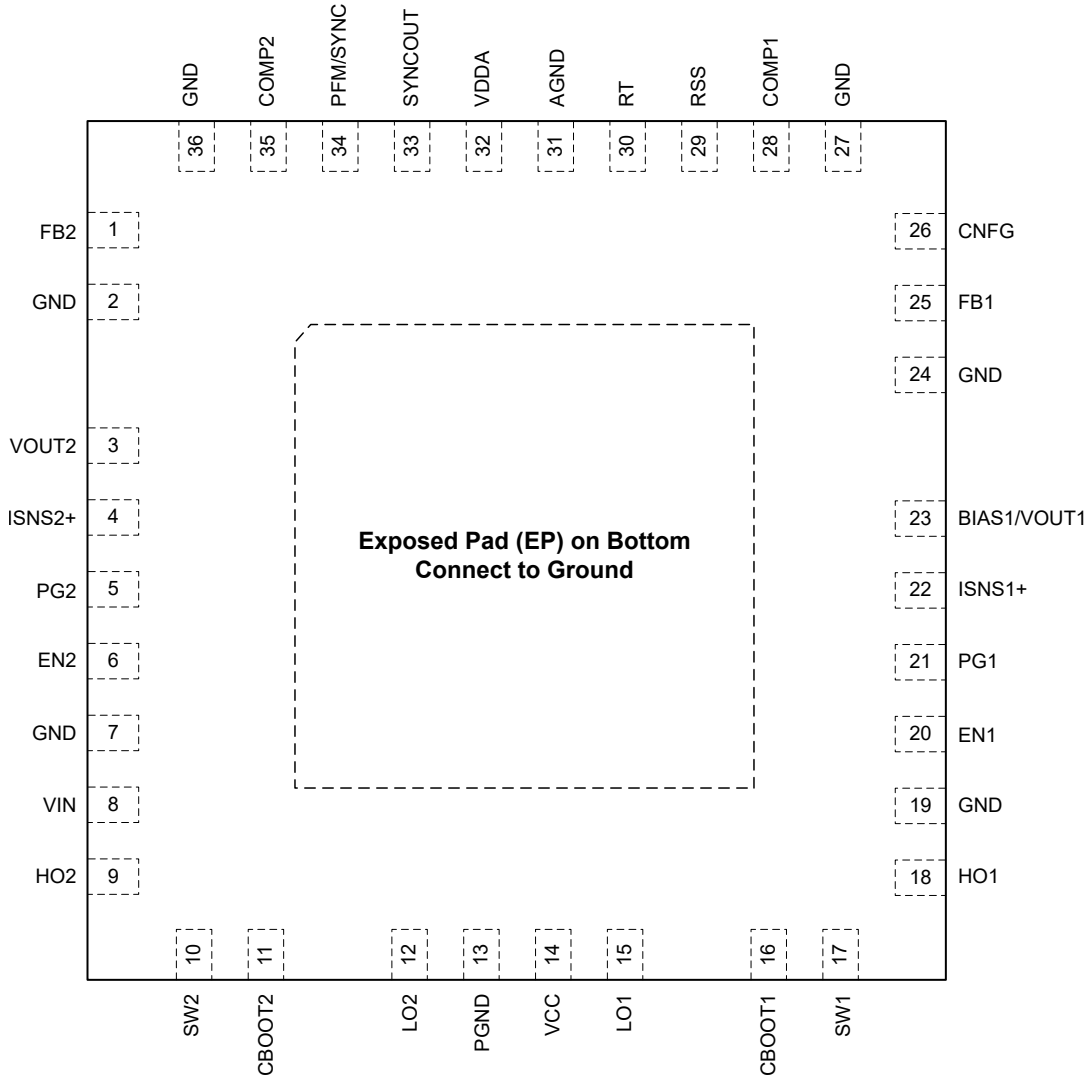
5 Pin Configuration and Functions



Connect the exposed pad on the bottom to AGND and PGND on the PCB.

図 5-1. RHA Package, 36-pin VQFN With Wettable Flanks (Top View)

表 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
FB2	1	I	Connect FB2 through a 7.5kΩ, 24.9kΩ or 48.7kΩ resistor to VDDA to set the output voltage at 3.3V, 5V or 12V, respectively. Alternatively, use a resistive divider from VOUT2 to FB2 to set the output voltage setpoint of channel 2 between 0.8V and 60V. The FB2 regulation voltage is 0.8V.
VOUT2	3	I	Output voltage sense and the current sense amplifier input of channel 2. Connect VOUT2 to the output side of the channel 2 current sense resistor (or to the relative sense capacitor terminal if inductor DCR current sensing is used).
ISNS2+	4	I	Channel 2 current sense amplifier input. Connect ISNS2+ to the inductor side of the external current sense resistor (or to the relevant sense capacitor terminal if inductor DCR current sensing is used) using a low-current Kelvin connection.
PG2	5	O	An open-collector output that goes low if VOUT2 is outside a specific regulation window
EN2	6	I	An active high input (V_{EN2} > 1V typical) enables channel 2. If V_{EN2} < 0.5V, channel 2 is disabled and is in shutdown mode unless a SYNC signal is present at PFM/SYNC pin. EN2 must never be left floating.
VIN	8	P	Supply voltage input source for the VCC regulator
HO2	9	P	Channel 2 high-side gate driver output
SW2	10	P	Switching node of the channel 2 buck regulator. Connect to the bootstrap capacitor, the source terminal of the high-side MOSFET, and the drain terminal of the low-side MOSFET.
CBOOT2	11	P	Channel 2 high-side driver supply for bootstrap gate drive
LO2	12	P	Channel 2 low-side gate driver output
PGND	13	G	Power ground connection pin for the low-side MOSFET gate driver
VCC	14	P	VCC bias supply pin. Connect a ceramic capacitor between VCC and PGND.
LO1	15	P	Channel 1 low-side gate driver output
CBOOT1	16	P	Channel 1 high-side driver supply for bootstrap gate drive
SW1	17	P	Switching node of the channel 1 buck regulator. Connect to the bootstrap capacitor, the source terminal of the high-side MOSFET, and the drain terminal of the low-side MOSFET.
HO1	18	P	Channel 1 high-side gate driver output
EN1	20	O	An active high input (V_{EN1} > 1V) enables channel 1. If V_{EN1} < 0.5V, channel 1 is disabled and is in shutdown mode unless a SYNC signal is present at PFC/SYNC pin. EN1 must never be left floating.
PG1	21	O	An open-collector output that goes low if VOUT1 is outside a specified regulation window.
ISNS1+	22	I	Channel 1 current sense amplifier input. Connect ISNS1+ to the inductor side of the external current sense resistor (or to the relevant sense capacitor terminal if inductor DCR current sensing is used) using a low-current Kelvin connection.
BIAS1/ VOUT1	23	I	If V_{BIAS1} > 4.3V, BIAS1 becomes the supply voltage to the internal VCC regulator. BIAS1 also acts as the primary VOUT1 sensing for fixed VOUT options.
CNFG	26	I	Connect a resistor from CNFG to GND to set the output configuration and to activate DRSS at one of two modulation frequencies (or to disable). Refer to 表 7-3.
FB1	25	I	Connect FB1 through a 7.5kΩ, 24.9kΩ or 48.7kΩ resistor to VDDA to set the output voltage at 3.3V, 5V or 12V, respectively. Alternatively, use a resistive divider from VOUT1 to FB1 to set the output voltage setpoint of channel 1 between 0.8V and 60V. The FB1 regulation voltage is 0.8V.
COMP1	28	O	Output of the channel 1 transconductance error amplifier. COMP1 is high impedance in interleaved or secondary mode. Pulling COMP1 below 100mV in interleaved mode disables the HO1 and LO1 gate driver outputs.
RSS	29	O	Connect a resistor from RSS to GND to set the soft-start time between 1.5ms and 20ms
RT	30	O	Frequency programming pin. A resistor from RT to AGND sets the oscillator frequency between 100kHz and 2.2MHz.
AGND	31	G	Analog ground connection. Ground return for the internal voltage reference and analog circuits.
VDDA	32	P	Internal analog bias regulator output. Connect a 1µF ceramic decoupling capacitor from VDDA to AGND.
SYNCOUT	33	O	SYNCOUT is a logic-level signal with a rising edge approximately 90° lagging HO1 (or 90° leading HO2). When SYNCOUT is used to synchronize a second LM5137-Q1 controller, the phases operate at 0°, 90°, 180° and 270° as needed.

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表 5-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
PFM/SYNC	34	I	Connect PFM/SYNC to VDDA to operate the LM5137-Q1 in PFM mode. Connect PFM/SYNC to GND to enable forced PWM (FPWM) mode with continuous conduction at light loads. Use PFM/SYNC as a synchronization input to synchronize the internal oscillator to an external clock.
COMP2	35	O	Output of the channel 2 transconductance error amplifier. COMP2 is high impedance in single-output interleaved mode. Pulling COMP2 below 100mV in interleaved mode disables the HO2 and LO2 gate driver outputs.
GND	2, 7, 19, 24, 27, 36	G	Unused pins – connect to the exposed pad on the PCB.

(1) P = Power, G = Ground, I = Input, O = Output

5.1 Wettable Flanks

100% automated visual inspection (AVI) post-assembly is typically required to meet requirements for high reliability and robustness. Standard quad-flat no-lead (QFN) packages do not have solderable or exposed pins and terminals that are easily viewed. Visually determining whether or not the package is successfully soldered onto the printed-circuit board (PCB) is therefore difficult. The wettable-flank process was developed to resolve the issue of side-lead wetting of leadless packaging. The LM5137-Q1 is assembled using a 36-pin VQFN package with wettable flanks to provide a visual indicator of solderability, which reduces inspection time and manufacturing costs.

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6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40℃ to 150℃ (unless otherwise noted). (1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	–0.3	85	V
	SW1, SW2 to PGND	–0.3	85	V
	SW1, SW2 to PGND, transient < 20ns	–5		V
	BIAS1/VOUT1, VOUT2, EN1, EN2 to PGND	–0.3	85	V
	ISNS1+, ISNS2+ to GND	–0.3	85	V
	FB1, FB2 to AGND	–0.3	20	V
	PFM/SYNC, RT, CNFG, RSS to AGND	–0.3	6.5	V
	CNFG to AGND	–0.3	5.5	V
	AGND to PGND	–0.3	0.3	V
Output voltage	PG1, PG1 to AGND	–0.3	85	V
	VCC, VDDA, SYNCOUT to AGND	–0.3	6.5	V
	CBOOT1 to SW1, CBOOT2 to SW2	–0.3	6.5	V
	CBOOT1 to SW1, CBOOT2 to SW2, transient < 20ns	–5		V
	HO1 to SW1, HO2 to SW2 to PGND	–0.3	V_{CBOOT} + 0.3	V
	HO1 to SW1, HO2 to SW2, transient < 20ns	–0.5		V
	LO1, LO2 to PGND	–0.3	V_{VCC} + 0.3	V
	LO1, LO2 to PGND, SW, transient < 20ns	–5		V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011	Corner pins (1, 9, 10, 17, 18, 26, 27, and 36)	±750	V
			Other pins	±500	

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6.3 Recommended Operating Conditions

Over the operating junction temperature range of –40℃ to 150℃ (unless otherwise noted). (1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	4		80	V
V_{OUT}	Output voltage range	0.8		60	V
	SW1, SW2 to PGND	–0.3		80	V
	HO1 to SW1, HO2 to SW2	–0.3		V_{CBOOT} + 0.3	V
	CBOOT1 to SW1, CBOOT2 to SW2	–0.3	5	5.3	V
	FB1, FB2 to AGND	–0.3		15	V
	EN1, EN2, PG1, PG2 to AGND	–0.3		80	V
	ISNS1+, ISNS2+, BIAS1/VOUT1, VOUT2, to AGND	–0.3		80	V
	VCC, VDDA, RSS to PGND	–0.3	5	5.3	V
$I_{SYNCOUT}$	SYNCOUT current			2	mA
	PGND to AGND	–0.3		0.3	V
T_J	Operating junction temperature	–40		150	°C

(1) Recommended operating conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.

6.4 Thermal Information

THERMAL METRIC(1)		LM5137-Q1 RHA (VQFN) 36 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33,2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note

6.5 Electrical Characteristics

T_J = –40°C to 150°C, Typical values are at T_J = 25°C and V_{IN} = 12V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY (VIN)						
I_{Q-VIN1}	VIN shutdown current	Non-switching, V_{EN1} = V_{EN2} = 0V		4		µA
I_{Q-VIN2}	VIN standby current	Non-switching, 0.5V ≤ $V_{EN1/2}$ ≤ 1V		130		µA
I_{SLEEP1}	Sleep current, V_{VOUT1} = 5V, V_{VOUT2} = 3.3V	1.05V ≤ $V_{EN1/2}$ ≤ 80V, V_{VOUT1} = 5V, V_{VOUT2} = 3.3V in regulation, no load, not switching		15.5		µA
I_{SLEEP2}	Sleep current, V_{VOUT1} = 5V	1.05V ≤ V_{EN1} ≤ 80V, V_{EN2} = 0V, V_{VOUT1} = 5V in regulation, no load, not switching		12.7	24	µA
INTERNAL LDO (VCC)						
$V_{VCC-REG}$	VCC regulation voltage	I_{VCC} = 0mA to 150mA	4.7	5.0	5.3	V
$V_{VCC-OVP}$	VCC OVP detect, V_{VCC} rising			5.8		V
$V_{VCC-OVP-HYS}$	VCC OVP detect hysteresis			225		mV
$V_{VCC-UVLO}$	VCC UVLO rising threshold			3.8		V
$V_{VCC-HYST}$	VCC UVLO hysteresis			300		mV
$I_{VCC-REG}$	Internal LDO short-circuit current limit		175	225		mA
INTERNAL LDO (VDDA)						
$V_{VDDA-REG}$	VDDA regulation voltage			5		V
R_{VDDA}	VDDA resistance to VCC			12		Ω

6.5 Electrical Characteristics (続き)

T_J = –40°C to 150°C, Typical values are at T_J = 25°C and V_{IN} = 12V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL BIAS (BIAS1)						
$V_{BIAS-ON}$	$V_{BIAS1/VOUT1}$ rising		4.1	4.3	4.4	V
$V_{BIAS-HYST}$				130		mV
REFERENCE VOLTAGE (FB1, FB2)						
V_{REF1}	Regulated FB voltage		792	800	808	mV
V_{BG1}	Bandgap1 voltage for regulation		1.2206	1.2237	1.2267	V
ENABLE (EN1, EN2)						
$V_{SDN1/2}$	Shutdown to standby threshold	$V_{EN1/2}$ rising		0.6		V
$V_{EN1/2-HIGH}$	Enable voltage rising threshold	$V_{EN1/2}$ rising, enable switching	0.95	1.0	1.05	V
$I_{EN1/2-HYS}$	Enable hystersis	$V_{EN1/2}$ = 1.1V	–12	–10	–8	µA
OUTPUT VOLTAGE (VOUT1/BIAS1, VOUT2)						
$V_{OUT1/2-3.3V}$	3.3V output setpoint	$R_{FB1/2}$ = 7.5kΩ	3.267	3.3	3.33	V
$V_{OUT1/2-5V}$	5V output setpoint	$R_{FB1/2}$ = 24.9kΩ	4.95	5.0	5.05	V
$V_{OUT1/2-12V}$	12V output setpoint	$R_{FB1/2}$ = 48.7kΩ	11.88	12	12.12	V
ERROR AMPLIFIER (COMP1, COMP2)						
$g_{m1/2}$	EA transconductance	ΔV_{FB} ±50mV	400	600		µS
$V_{COMP1/2-CLAMP}$	COMP clamp voltage	$V_{FB1/2}$ = 0V		1.75		V
$I_{COMP1/2-SRC}$	EA source current	$V_{COMP1/2}$ = 1V, $V_{FB1/2}$ = 0.6V		120		µA
$I_{COMP1/2-SINK}$	EA sink current	$V_{COMP1/2}$ = 1V, $V_{FB1/2}$ = 1V		120		µA
$V_{DRIVER1/2-DISABLE}$	Drive output disable signal	I_{SINK} = 200µA, INTLV only		100		mV
POWER GOOD (PG1, PG2)						
$V_{PG1/2-OVP}$	Power-Good overvoltage	Rising threshold	103	105	107	%
$V_{PG1/2-OVP-HYST}$	Power-Good OV hysteresis			1		%
$V_{PG1/2-UVP}$	Power-Good undervoltage protection	Falling with respect to the regulated voltage	93	95	98	%
$t_{PG1/2-DEGLITCH(R)}$	Power-Good deglitch rising		1.4	2	2.6	ms
$t_{PG1/2-DEGLITCH(F)}$	Power-Good deglitch falling		60	90	120	µs
$R_{ON1/2(PG)}$	PG1/2 on resistance	Open drain, I_{PG} = 250µA		100	250	Ω
SWITCHING FREQUENCY						
F_{SW1}	Switching frequency 1	R_{RT} = 100kΩ to AGND		230		kHz
F_{SW2}	Switching frequency 2	R_{RT} = 10kΩ to AGND	1.98	2.2	2.42	MHz
F_{SW3}	Switching frequency 3	R_{RT} = 230kΩ to AGND		100		kHz
$SLOPE_1$	Internal slope compensation 1	R_{RT} = 10kΩ to AGND		480		mV/µs
$SLOPE_2$	Internal slope compensation 2	R_{RT} = 100kΩ to AGND		47		mV/µs
$t_{ON(min)}$	Minimum on-time			15	35	ns
$t_{OFF(min)}$	Minimum off-time			45	65	ns
D_{MAX}	Maximum duty cycle			100		%
SYNCHRONIZATION OUTPUT (SYNCOUT)						
$V_{SYNCOUT-HO}$	SYNCOUT high-state voltage	$I_{SYNCOUT}$ = 4mA	2.0			V
$V_{SYNCOUT-LO}$	SYNCOUT low-state voltage	$I_{SYNCOUT}$ = 4mA			0.8	V
$t_{SYNCOUT1}$	Delay from HO1 rising edge to SYNCOUT rising edge	$V_{PFM/SYNC}$ = 0V, T_S = 1/F_{SW}, F_{SW} set by R_{RT} = 230kΩ		2.5		µs
$t_{SYNCOUT2}$	Delay from HO1 rising edge to SYNCOUT falling edge	$V_{PFM/SYNC}$ = 0V, T_S = 1/F_{SW}, F_{SW} set by R_{RT} = 230kΩ		7.5		µs
PULSE FREQUENCY MODULATION (PFM/SYNC)						
V_{PFM-LO}	PFM detection threshold low				0.8	V
V_{PFM-HI}	PFM detection threshold high		1.2			V
V_{ZC-SW}	Zero-cross threshold			–5.5		mV

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6.5 Electrical Characteristics (続き)

T_J = –40°C to 150°C, Typical values are at T_J = 25°C and V_{IN} = 12V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$F_{SYNCIN-MAX}$	Maximum frequency sync range	R_{RT} = 10kΩ, ±20% of the nominal oscillator frequency			2640	kHz
$F_{SYNCIN-MAX}$	Minimum frequency sync range	R_{RT} = 10kΩ, ±20% of the nominal oscillator frequency	1760			kHz
$t_{SYNC-MIN}$	Minimum pulse-width of external synchronization		20			ns
$t_{SYNCIN-HO}$	Delay from SYNCIN rising edge to HO rising edge			70		ns
$t_{PFM-FILTER}$	SYNCIN to PFM mode		14		70	µs
CBOOT1, CBOOT2						
$V_{BOOT1/2-DROP}$	Internal diode forward drop	$I_{CBOOT1/2}$ = 20mA, VCC to CBOOT		0.8		V
$I_{BOOT1/2}$	CBOOT to SW quiescent current, not switching	$V_{EN1/2}$ = 5V, $V_{CBOOT1/2} – V_{SW1/2}$ = 5V		2		µA
$V_{BOOT1/2-SW-UV-R}$	CBOOT to SW UVLO rising threshold	$V_{CBOOT1/2} – V_{SW1/2}$ rising		2.7		V
$V_{BOOT1/2-SW-UV-F}$	CBOOT to SW UVLO falling threshold	$V_{CBOOT1/2} – V_{SW1/2}$ falling		2.5		V
$V_{BOOT1/2-SW-UV-HYS}$	CBOOT to SW UVLO hysteresis			0.25		V
$V_{CHARGE1/2–PUMP-UNLOADED}$	Charge pump output voltage	$I_{CBOOT1/2}$ = 0 µA, per channel		4.8		V
$I_{CHARGE1/2–PUMP}$	Charge pump output current	$V_{CBOOT1/2}$ = 3.5V		20		µA
$V_{CHARGE1/2–PUMP-LOADED}$	Charge pump output voltage	$I_{CBOOT1/2}$ = 20µA, per channel		4.25		V
HIGH-SIDE GATE DRIVER (HO1, HO2)						
$V_{HO1/2-HIGH}$	HO1/2 high-state output voltage	$I_{HO1/2}$ = –100mA		100		mV
$V_{HO1/2-LOW}$	HO1/2 low-state output voltage	$I_{HO1/2}$ = 100mA		45		mV
$t_{HO1/2-RISE}$	HO1/2 rise time (10% to 90%)	$C_{LOAD1/2}$ = 2.7nF		5.4		ns
$t_{HO1/2-FALL}$	HO1/2 fall time (90% to 10%)	$C_{LOAD1/2}$ = 2.7nF		4		ns
$I_{HO1/2-SRC}$	HO1/2 peak source current	$V_{HO1/2} = V_{SW1/2}$ = 0V		2		A
$I_{HO1/2-SINK}$	HO1/2 peak sink current	$V_{CBOOT1/2}$ = 5V		3		A
LOW-SIDE GATE DRIVER (LO1, LO2)						
$V_{LO1/2-HIGH}$	LO1/2 high-state output voltage	$I_{HO1/2}$ = –100mA		100		mV
$V_{LO1/2-LOW}$	LO1/2 low-state output voltage	$I_{HO1/2}$ = 100mA		45		mV
$I_{LO1/2-SRC}$	LO1/2 peak source current	$V_{LO1/2} = V_{SW1/2}$ = 0V		2		A
$I_{LO1/2-SINK}$	LO1/2 peak sink current	V_{VCC} = 5V		3		A
ADAPTIVE DEADTIME CONTROL						
t_{DEAD1}	HO off to LO on deadtime			21		ns
t_{DEAD2}	LO off to HO on deadtime			21		ns
START-UP						
R_{SS1}	1.5ms soft-start time	R_{SS} = 0Ω		1.25		ms
R_{SS2}	2ms soft-start time	R_{SS} = 10kΩ		2.2		ms
R_{SS3}	20ms soft-start time	R_{SS} = 100kΩ		22		ms
DUAL RANDOM SPREAD SPECTURM (DRSS)						
f_{m1}	Modulation frequency		7.2		16.8	kHz
Δf_{SS1-LF}	Low-frequency triangular spread spectrum modulation range1 maximum		–5		5	%
Δf_{SS2-LF}	Low-frequency triangular spread spectrum modulation range2 maximum		–10		10	%
OVERCURRENT PROTECTION						
$V_{CS1/2-TH}$	Current limit threshold	Measured from ISNS1/2+ to VOUT1/2	54	60	66	mV
$t_{DELAY1/2-ISNS+}$	ISNS+ delay from V_{CS-TH} to HO off			70		ns
$G_{CS1/2}$	CS amplifier gain		9.5	10	10.5	V/V
$V_{CS-SHARE}$	COMP to current accuracy	$V_{COMP1/2}$ = 1.2V	54	60	66	mV

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6.5 Electrical Characteristics (続き)

T_J = –40°C to 150°C, Typical values are at T_J = 25°C and V_{IN} = 12V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL HICCUP MODE						
HIC_{DLY}	Hiccup mode activation delay	$V_{ISNS1/2+} – V_{VOUT1/2}$ > 60 mV		512		cycles
HIC_{TIME}	Hiccup mode duration	$V_{ISNS1/2+} – V_{VOUT1/2}$ > 60 mV		16384		cycles
THERMAL SHUTDOWN						
$T_{SHD\ 1/2}$	Thermal shutdown threshold	Temperature rising		175		°C
$T_{SHD-HYS1/2}$	Thermal shutdown hysteresis			15		°C

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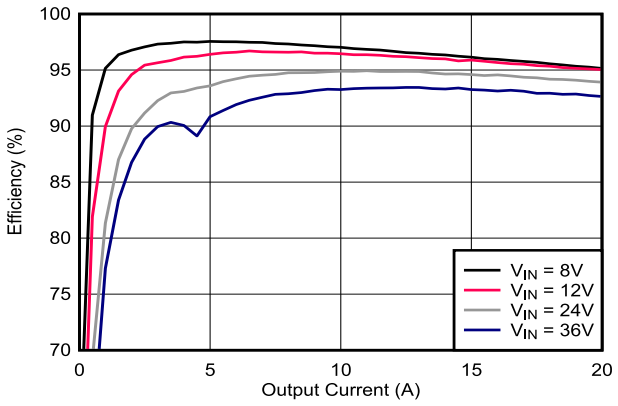
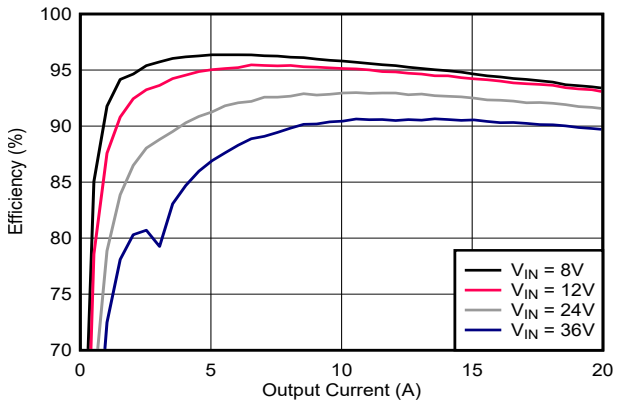
6.6 Typical Characteristics

V_{IN} = 12V, T_J = 25°C, unless otherwise stated.



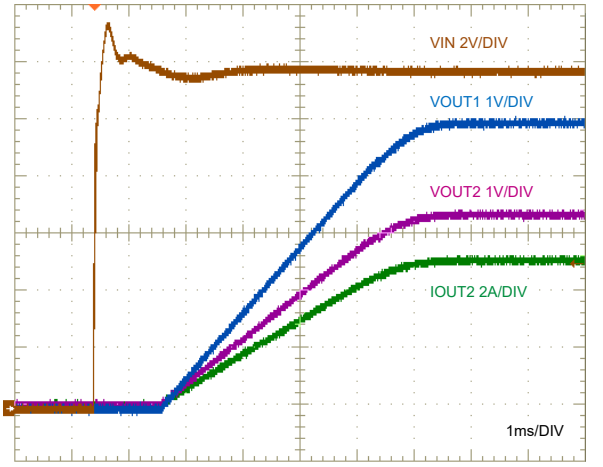
See 図 8-4 F_{SW} = 440kHz

図 6-1. Efficiency vs Load, 5V Output



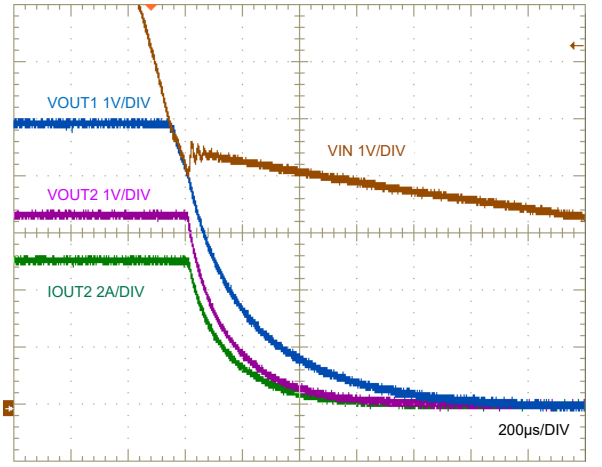
See 図 8-4 F_{SW} = 440kHz

図 6-2. Efficiency vs Load, 3.3V Output



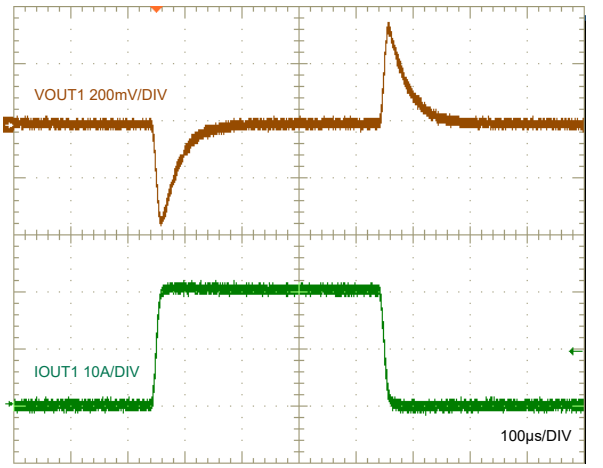
See 図 8-4 5A resistive loads

図 6-3. Start-up Characteristic



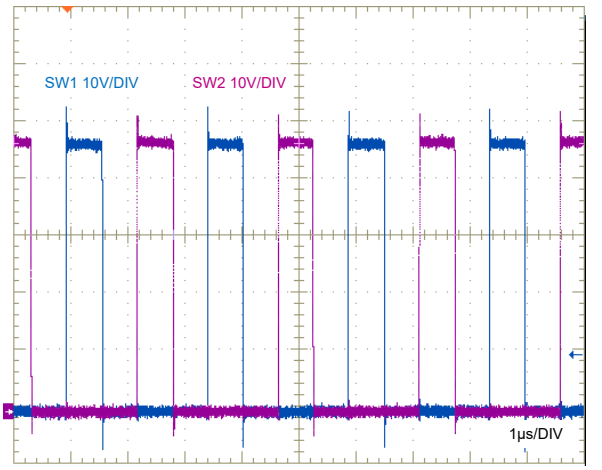
See 図 8-4 5A resistive loads

図 6-4. Shutdown Characteristic



See 図 8-4 V_{OUT} = 5V 2A/µs slew rate

図 6-5. Load Transient Response



See 図 8-16 V_{IN} = 48V V_{OUT} = 12V

図 6-6. Switch-Node Voltages

6.6 Typical Characteristics (continued)

V_{IN} = 12V, T_J = 25°C, unless otherwise stated.

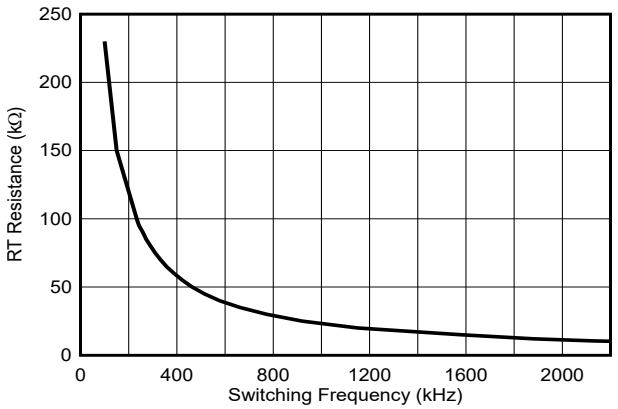


図 6-7. RT Resistance vs Switching Frequency

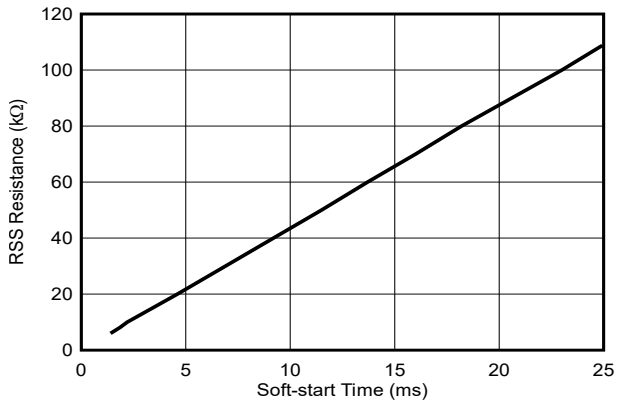


図 6-8. RSS Resistance vs Soft-start Time

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7 Detailed Description

7.1 Overview

The LM5137-Q1 is a dual-channel switching DC/DC controller that features all of the functions necessary to implement a high-efficiency synchronous buck regulator. The device is offered from a controller family with three options for functional safety applications: Capable, ASIL B, or ASIL D, with the latter two options designated by an "F" suffix in the part number.

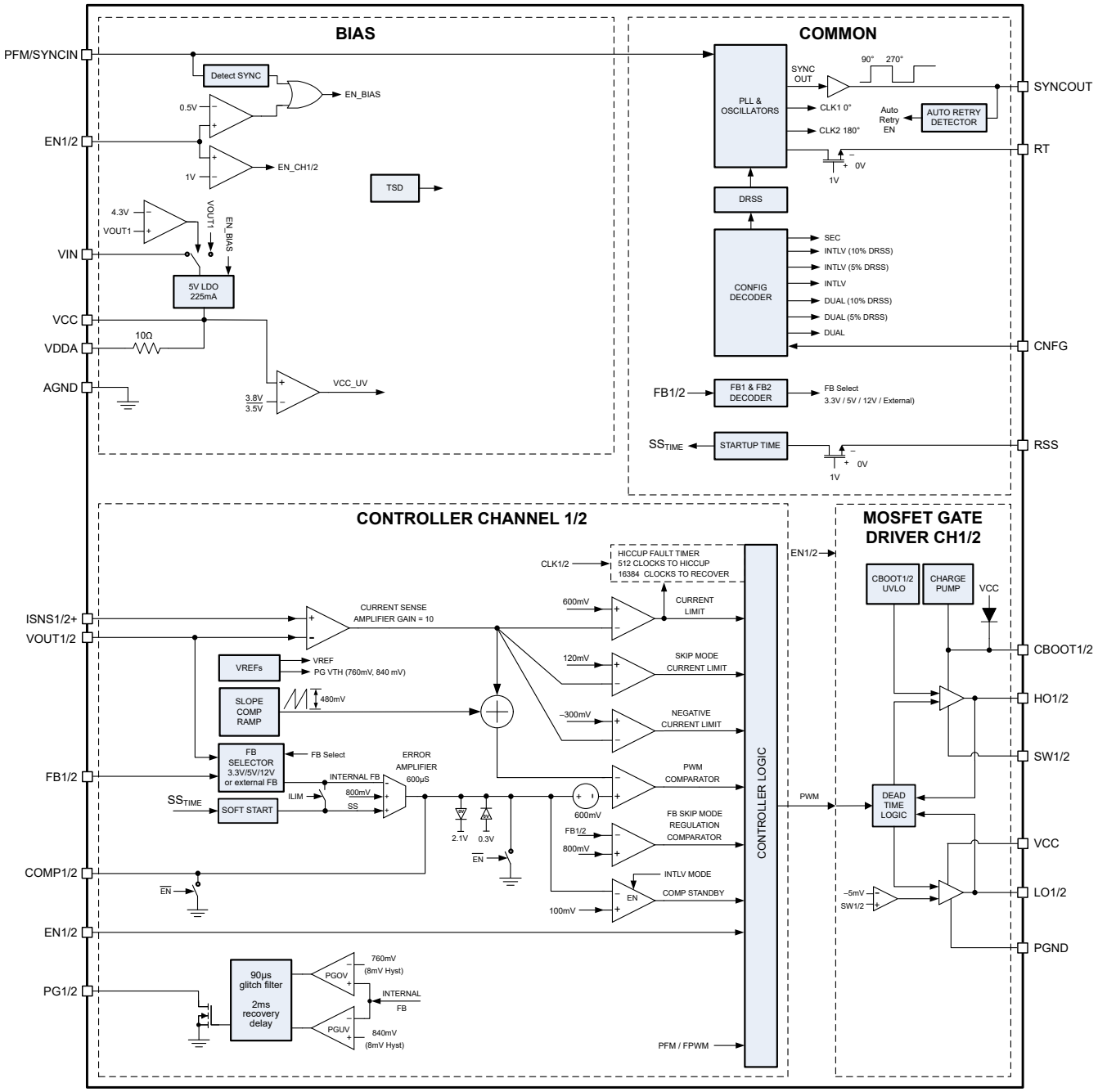
Operating over a wide input voltage range from 4V to 80V, the LM5137-Q1 is configured to provide a fixed 3.3V, 5V or 12V output, or an adjustable output between 0.8V and 60V. This easy-to-use controller integrates high-side and low-side MOSFET gate drivers, each capable of sourcing 2A and sinking 3A peak current. Adaptive dead-time control is designed to minimize body diode conduction during switching transitions.

Peak current-mode control using a shunt resistor or inductor DCR current sensing provides inherent line feed forward, cycle-by-cycle peak current limiting, and easy loop compensation. Current-mode control also supports a wide duty cycle range for high input voltage and low dropout applications as well as when a high voltage conversion ratio (for example, 10-to-1) is required. The oscillator frequency is user-programmable between 100kHz to 2.2MHz, and the frequency can be synchronized as high as 2.5MHz by applying an external clock to PFM/SYNC. A user-selectable PFM mode feature enables discontinuous conduction mode (DCM) operation to further improve efficiency and reduce power dissipation during light-load conditions.

The LM5137-Q1 incorporates features to simplify the compliance with automotive EMI requirements (CISPR 25). An optional spread spectrum frequency modulation (DRSS) technique reduces the peak EMI signature, while the adaptive gate drivers minimize high-frequency emissions. Finally, 180° out-of-phase interleaved operation of the two controller channels reduces input filtering and capacitor requirements.

The LM5137-Q1 is provided in a 36-pin VQFN package with a wettable flank pinout and an exposed pad to aid in thermal dissipation.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Input Voltage Range (VIN)

The LM5137-Q1 input voltage operating range is from 4V to 80V. The device is intended for step-down conversions from 12V, 24V and 48V automotive supply rails. The circuit in 図 7-1 shows the essential components to implement an LM5137-Q1 based wide-V_{IN} dual-output buck regulator using a single input supply.

The LM5137-Q1 uses an internal LDO subregulator to provide a 5V VCC bias rail for the gate drive and control circuits (assuming the input voltage is higher than 5V plus the necessary subregulator dropout specification). As V_{IN} approaches the V_{OUT} setpoint, the LM5137-Q1 activates the integrated charge pump to keep the high-side MOSFET on and thus achieve true 100% duty cycle. This action allows for the lowest possible dropout voltage at the output.

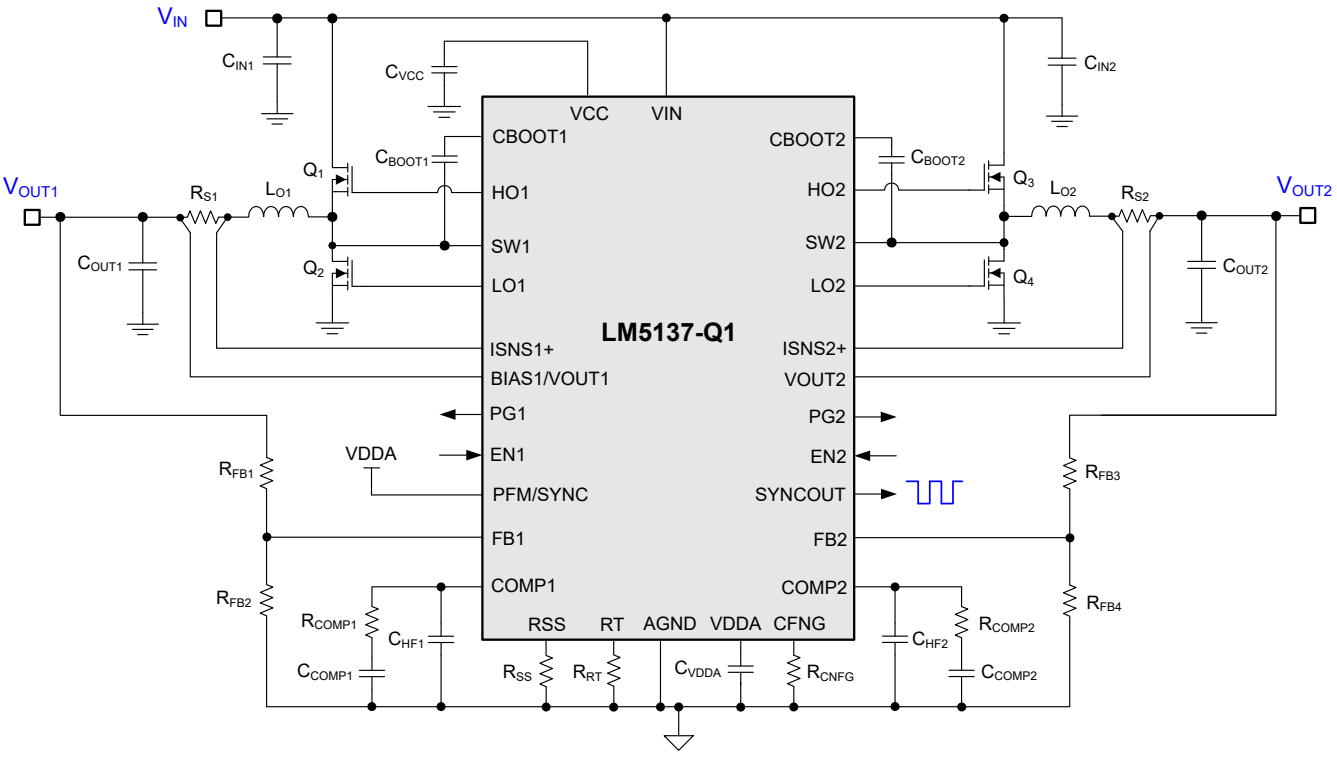

図 7-1. LM5137-Q1 Dual-Output Regulator Schematic

In high input voltage applications, make sure that the VIN, SW1, and SW2 pin voltages do not exceed the absolute maximum voltage rating of 85V during line or load transient events. Voltage excursions that exceed the *Absolute Maximum Ratings* can damage the IC. Proceed carefully during PCB board layout and use high-quality input bypass capacitors to minimize switch voltage overshoot and ringing.

表 7-1. Errata

ITEM	OBSERVED BEHAVIOR
1	At oscillator frequencies greater than 1MHz, there is a large hysteresis as the LM5137-Q1 comes out of dropout (100% duty cycle). VIN can need to increase several volts above the voltage at which VIN entered dropout.

7.3.2 Bias Supply Regulator (VCC, BIAS1/VOUT1, VDDA)

The LM5137-Q1 contains an internal high-voltage VCC bias regulator that provides the bias supply for the PWM controller and the gate drivers of the external MOSFETs. Connect the input voltage pin (VIN) directly to an input voltage source up to 80V. When the input voltage is below the VCC setpoint of 5V, the VCC voltage tracks VIN minus a small voltage drop.

The VCC regulator current limit is 175mA (minimum). At power up, the regulator sources current into the VCC capacitor. When the VCC voltage exceeds 3.8V (typical), both output channels are enabled (if EN1 and EN2 are above 1V) and the soft-start sequence begins. Both channels remain active unless the VCC voltage falls below the falling UVLO threshold of 3.5V (typical) or EN is switched to a low state. Connect a 2.2µF to 10µF ceramic capacitor from VCC to PGND.

A 10Ω resistor connects VDDA to VCC. Bypass VDDA to AGND with a 1µF ceramic capacitor to achieve a low-noise internal bias rail. Normally VDDA is 5V, but there are two operating conditions where VDDA regulates at 3.3V. The first is in skip cycle mode when V_{OUT1} is set to 3.3V and V_{OUT2} is disabled. The second is in a cold-crank startup where V_{IN} is 4V and V_{OUT1} is 3.3V.

If the BIAS1/VOUT1 voltage is above 4.3V, BIAS1/VOUT1 internally connects to a second input of the VCC regulator. This helps to reduce the internal power dissipation of the LM5137-Q1, as bias current derives from VOUT1 instead of VIN. Avoid connecting BIAS1/VOUT1 or VOUT2 to a voltage greater than 60V or less than –0.3V.

表 7-2. Errata

ITEM	OBSERVED BEHAVOR
1	Upon recovering from sleep mode in PFM, with the oscillator frequency set above 1MHz and at load currents around 300mA, VCC is observed to loose regulation and can reach the falling UVLO threshold (3.5V).

7.3.3 Precision Enable (EN1, EN2)

The LM5137-Q1 has a precision enable circuit on each EN input. When the EN1 or EN2 voltage is greater than 1V, switching is enabled on the respective channel. If the EN1 and EN2 pins are pulled below 0.5V, the LM5137-Q1 is in shutdown with an I_Q of 4µA (typical) current consumption from V_{IN}. When the EN1 or EN2 voltage is between 0.5V and 1V, the LM5137-Q1 is in standby mode with the VCC regulator active but the controller is not switching. The non-switching input quiescent current in standby mode is 130µA typical.

The LM5137-Q1 is enabled with a voltage greater than 1V. However, many applications benefit from using a resistor divider R_{UV1} and R_{UV2}, as shown in 図 7-2, to establish a precision UVLO level. Add R_{UV3} in series to provide additional voltage hystersis. Avoid leaving the EN1 and EN2 pins floating. Keep the EN1/2 voltage under 80V.

Use 式 1 to calculate the UVLO resistors, where $V_{IN(on)}$ and $V_{IN(off)}$ are the required input voltage turn-on and turn-off thresholds.

$$R_{UV2} = \left[\frac{V_{EN(off)} - \left(V_{IN(off)} / V_{IN(on)} \right) \cdot V_{EN(on)}}{I_{EN(hys)}} - R_{UV3} \right] \cdot \frac{V_{IN(on)}}{V_{IN(on)} - V_{EN(on)}}$$

$$R_{UV1} = R_{UV2} \cdot \left(\frac{V_{IN(on)}}{V_{EN(on)}} - 1 \right) \quad (1)$$

ADVANCE INFORMATION

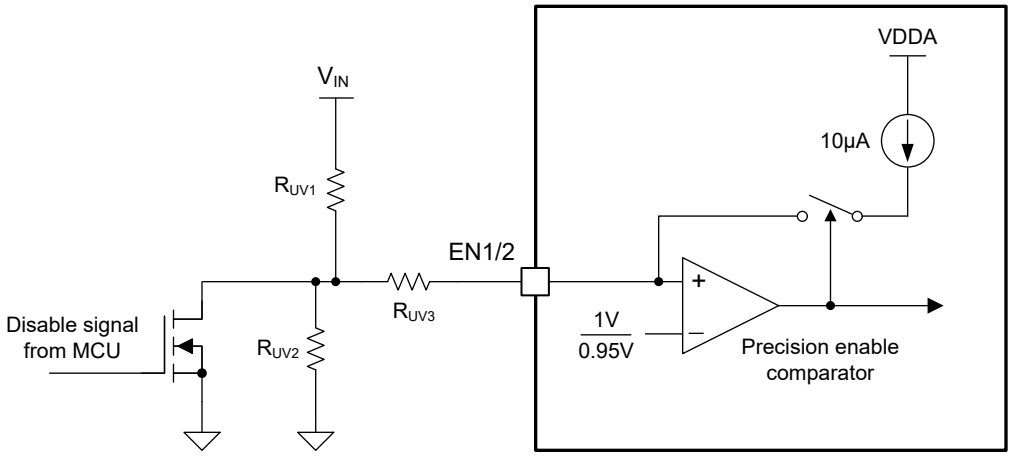

図 7-2. Programmable Input Voltage UVLO Turn On/Off

7.3.4 Switching Frequency (RT)

Program the LM5137-Q1 oscillator with a resistor from RT to AGND to set the free-running switching frequency between 100kHz and 2.2MHz. Calculate the RT resistance for a given switching frequency using 式 2.

$$R_{RT}\left[k\Omega\right] = \frac{\frac{10^6}{F_{SW}\left[kHz\right]} - 15}{42.8} \tag{2}$$

7.3.5 Pulse Frequency Modulation and Synchronization (PFM/SYNC)

A synchronous buck regulator implemented with a low-side synchronous MOSFET rather than a diode has the capability to sink negative current from the output during light load, output overvoltage, and prebias startup conditions. The LM5137-Q1 provides a diode emulation feature that can be enabled to prevent reverse (drain-to-source) current flow in the low-side MOSFET. When configured for diode emulation mode, the low-side MOSFET is switched off when reverse current flow is detected by sensing the SW voltage using a zero-cross comparator. The benefit of this configuration is lower power loss during light-load conditions. The disadvantage of diode emulation mode is slower light-load transient response.

Use the PFM/SYNC pin to configure diode emulation. To enable diode emulation and thus achieve high efficiency at light loads, connect PFM/SYNC to VDDA. If FPWM with continuous conduction mode (CCM) operation is preferred, tie PFM/SYNC to AGND. Note that diode emulation is automatically engaged to prevent reverse current flow during a prebiased startup. A gradual change from DCM to CCM operation provides monotonic startup performance.

To synchronize the LM5137-Q1 to an external clock source, apply a logic-level signal to the PFM/SYNC pin. The LM5137-Q1 can be synchronized to ±20% of the programmed free-running frequency up to a maximum of 2.5MHz. If there is an RT resistor and a synchronization clock signal, the LM5137-Q1 ignores the RT resistor and synchronizes to the external clock. However, under low V_{IN} conditions when the minimum off-time is reached, the synchronization signal is ignored, allowing the switching frequency to reduce to maintain output voltage regulation.

7.3.6 Synchronization Out (SYNCOUT)

The SYNCOUT voltage is a logic-level signal with a rising edge approximately 90° lagging HO2 (or 90° leading HO1). When the SYNCOUT signal is used to synchronize a second LM5137-Q1 controller, all four phases are 90° out of phase, thus optimizing ripple current cancellation.

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7.3.7 Dual Random Spread Spectrum (DRSS)

The LM5137-Q1 provides a digital spread spectrum, which reduces the EMI signature of the switching regulator over a wide frequency range. As shown in 図 7-3, DRSS combines a low-frequency triangular modulation profile with a high frequency cycle-by-cycle random modulation profile. The low-frequency modulation improves performance in lower radio-frequency bands, while the high-frequency random modulation improves performance in higher radio-frequency bands.

Spread spectrum functions by converting a narrowband signal into a wideband signal that spreads the energy over multiple frequencies. Because industry standards require different EMI receiver resolution bandwidth (RBW) settings for different frequency bands, the RBW has an impact on the spread spectrum performance. For example, the RBW setting in an EMI receiver for CISPR 25 in the frequency band from 150kHz to 30MHz is 9kHz. For frequencies greater than 30MHz, the RBW is 120kHz. DRSS is able to simultaneously improve the EMI performance with low and high RBWs with the low-frequency triangular and high-frequency cycle-by-cycle random modulation profiles, respectively. DRSS can reduce conducted emissions by 15dBµV in the CISPR 25 low-frequency band (150kHz to 30MHz) and 5dBµV in the high-frequency band (30MHz to 108MHz). Applying an external clock signal to the PFM/SYNCIN pin disables DRSS. See 表 7-3 to configure the LM5137-Q1 using a resistor from CNFG to AGND.

表 7-3. CNFG Resistor Configuration

R_{CNFG}	PRIMARY / SECONDARY	DRSS	INDEPENDENT OR INTERLEAVED
10kΩ	Primary	Disabled	Independent
19.1kΩ	Primary	±5%	Independent
29.4kΩ	Primary	±10%	Independent
41.2kΩ	Primary	Disabled	Interleaved
54.9kΩ	Primary	±5%	Interleaved
71.5kΩ	Primary	±10%	Interleaved
90.9kΩ	Secondary	N/A	Interleaved

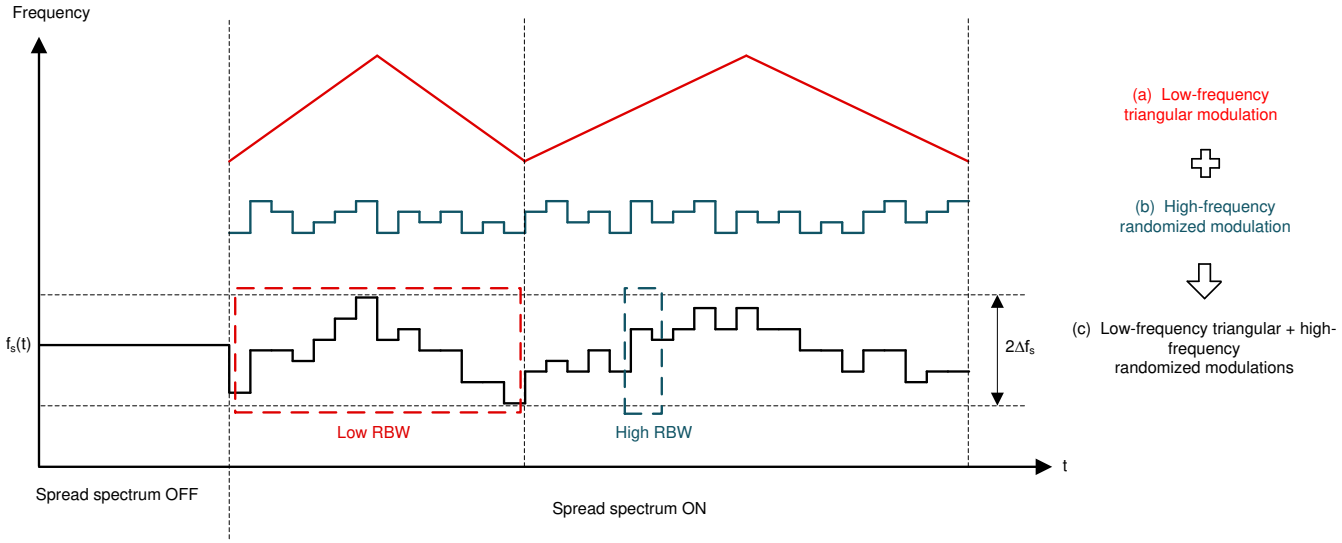

図 7-3. DRSS Implementation

7.3.8 Configurable Soft Start (RSS)

The soft-start feature of the LM5137-Q1 allows the regulator to gradually reach the steady-state operating point, thus reducing start-up stresses and inrush current. Program the soft-start time with a resistor from RSS to AGND. If the RSS pin is shorted to AGND, the soft-start time is 1.25ms. If the RSS resistance is greater than 500kΩ (or the pin is left open circuit), the LM5137-Q1 defaults to a soft-start time of 6.5ms.

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Use 式 3 to calculate the RSS resistance for a given soft-start time.

$$R_{SS}\left[k\Omega\right] = 4.38 \cdot t_{SS}\left[ms\right] \quad (3)$$

7.3.9 Output Voltage Setpoints (FB1, FB2)

The LM5137-Q1 outputs can be independently configured for one of the three fixed output voltage setpoints or adjusted to the desired voltage using an external resistor divider. As shown in 表 7-4, configure V_{OUT1} or V_{OUT2} for a 3.3V, 5V, or 12V voltage setpoint by connecting the respective FB pin with a 7.5kΩ, 24.9kΩ, or 48.7kΩ to VDDA.

表 7-4. Feedback Configuration Resistor

PULLUP RESISTOR TO VDDA	V_{OUT} SETPOINT
7.5kΩ	3.3V
24.9kΩ	5V
48.7kΩ	12V
Not installed	External FB divider setting

The configuration settings are latched and cannot be changed until the LM5137-Q1 is powered down with the VCC voltage decreasing below the falling UVLO threshold, and then powered up again with VCC above 3.8V.

Alternatively, set the output voltage with an external resistor divider from the output to AGND. The FB regulation voltage is 0.8V, and the output voltage setpoint range is from 0.8V to 60V. Use 式 4 to calculate the upper and lower feedback resistors, designated R_{FB1} and R_{FB2}, respectively. See 図 7-4.

$$R_{FB1} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \cdot R_{FB2} \quad (4)$$

A recommended starting value for R_{FB2} is between 10kΩ and 20kΩ.

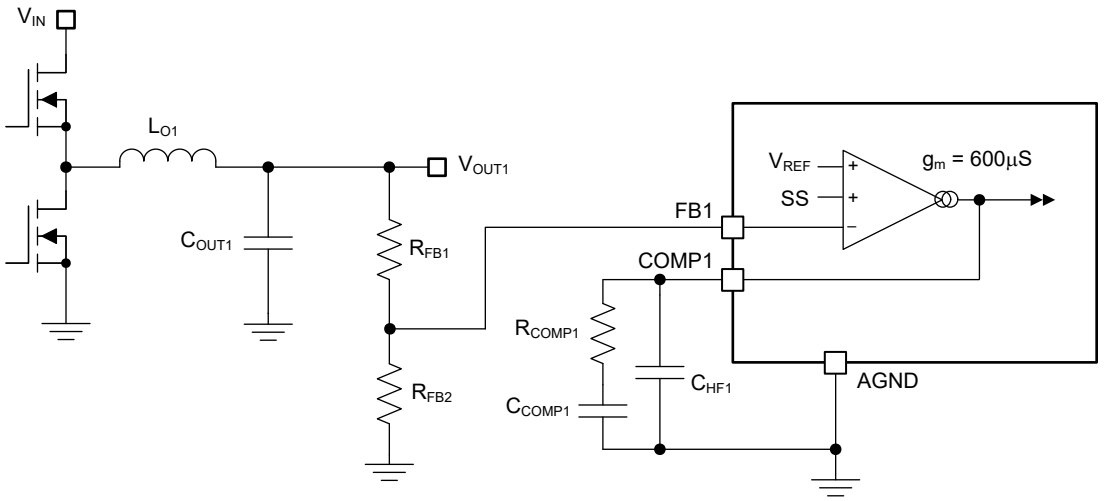

図 7-4. Voltage Loop With Adjustable Output Setting

If high light-load efficiency is required, take care when selecting the external resistors. The current consumption of the external divider adds to the LM5137-Q1 sleep current. The divider current reflected to V_{IN} scales by the ratio of V_{OUT}/V_{IN}.

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7.3.10 Minimum Controllable On-Time

There are two limitations to the minimum output voltage adjustment range: the LM5137-Q1 voltage reference of 0.8V and the minimum controllable switch-node pulse width, $t_{ON(min)}$.

$t_{ON(min)}$ effectively limits the voltage step-down conversion ratio of V_{OUT}/V_{IN} at a given switching frequency. For fixed-frequency PWM operation, the voltage conversion ratio must satisfy 式 5.

$$\frac{V_{OUT}}{V_{IN}} > t_{ON(min)} \cdot F_{SW} \tag{5}$$

where

- $t_{ON(min)}$ is 15ns (typical)
- F_{SW} is the switching frequency

If the desired voltage conversion ratio does not meet the above condition, the LM5137-Q1 transitions from fixed switching frequency operation to a pulse-skipping mode to maintain output voltage regulation. For example, if the desired output voltage is 1.2V with an input voltage is 24V and switching frequency of 2.1MHz, the voltage conversion ratio test in 式 6 is satisfied.

$$\frac{1.2\,V}{24\,V} > 15\,ns \cdot 2.1\,MHz$$

$$0.05 > 0.032 \tag{6}$$

For wide V_{IN} applications and low output voltages, an alternative is to reduce the LM5137-Q1 switching frequency to meet the requirement of 式 5.

7.3.11 Error Amplifier and PWM Comparator (FB1, FB2, COMP1, COMP2)

Each channel of the LM5137-Q1 has an independent high-gain transconductance amplifier that generates an error current proportional to the difference between the feedback voltage and an internal precision reference (0.8V). The output of the transconductance amplifier connects to the respective COMP pin, allowing the user to provide external control loop compensation. TI generally recommends a type-II compensation network for peak current-mode control. The HO1/2 and LO1/2 driver outputs can be disabled if COMP1/2 is pulled below 100mV.

7.3.11.1 Slope Compensation

The LM5137-Q1 provides internal slope compensation for stable operation with peak current-mode control and a duty cycle greater than 50%. Calculate the buck inductance to provide a slope compensation contribution equal to one times the inductor current downslope using 式 7.

$$L_{O(IDEAL)}\left[\mu H\right] = \frac{V_{OUT}\left[V\right] \cdot R_S\left[m\Omega\right]}{22 \cdot F_{SW}\left[MHz\right]} \tag{7}$$

- A lower inductance value generally increases the peak-to-peak inductor ripple current, which minimizes size and cost, and improves transient response at the cost of reduced light-load efficiency due to higher cores losses and peak currents.
- A higher inductance value generally decreases the peak-to-peak inductor ripple current, reducing switch peak and RMS currents at the cost of requiring larger output capacitors to meet load-transient specifications.

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7.3.12 Inductor Current Sense (ISNS1+, BIAS1/VOUT1, ISNS2+, VOUT2)

There are two methods to sense the inductor current of the buck power stage. The first uses a current sense resistor (also known as a shunt) in series with the inductor, and the second avails of the DC resistance of the inductor (DCR current sensing).

7.3.12.1 Shunt Current Sensing

図 7-5 illustrates inductor current sensing using a shunt resistor. This configuration continuously monitors the inductor current to provide accurate overcurrent protection across the operating temperature range. For optimal current sense accuracy and overcurrent protection, use a *low parasitic inductance* shunt resistor of ±1% tolerance connected between the inductor and the output. Use Kelvin sense connections at the shunt and route the sense lines differentially back to the LM5137-Q1.

If the peak voltage sensed differentially at [ISNS1+, BIAS1/VOUT1] or [ISNS2+, VOUT2] exceeds the current limit threshold of 60mV, the current limit comparator immediately terminates the respective HO output for cycle-by-cycle current limiting. Calculate the shunt resistance using 式 8.

$$R_S = \frac{V_{CS\text{-}TH}}{I_{OUT(CL)} + \frac{\Delta I_L}{2}} \tag{8}$$

where

- $V_{CS\text{-}TH}$ is current sense threshold of 60mV.
- $I_{OUT(CL)}$ is the overcurrent setpoint that is set higher than the maximum load current to avoid tripping the overcurrent comparator during load transients.
- ΔI_L is the peak-to-peak inductor ripple current.

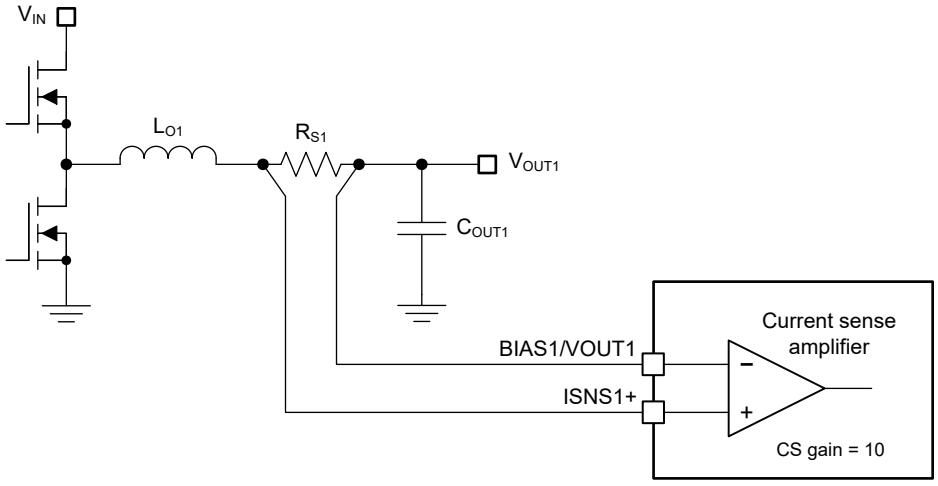

図 7-5. Shunt Current Sensing Implementation

7.3.12.2 Inductor DCR Current Sensing

For high-power applications that do not require accurate current-limit protection, inductor DCR current sensing is preferable. This technique provides lossless and continuous monitoring of the inductor current using an RC sense network in parallel with the inductor. Select an inductor with a low DCR tolerance to achieve a typical current limit accuracy within the range of 10% to 15% at room temperature. Components R_{CS} and C_{CS} in 図 7-6 create a low-pass filter across the inductor to enable differential sensing of the voltage drop across the inductor DCR.

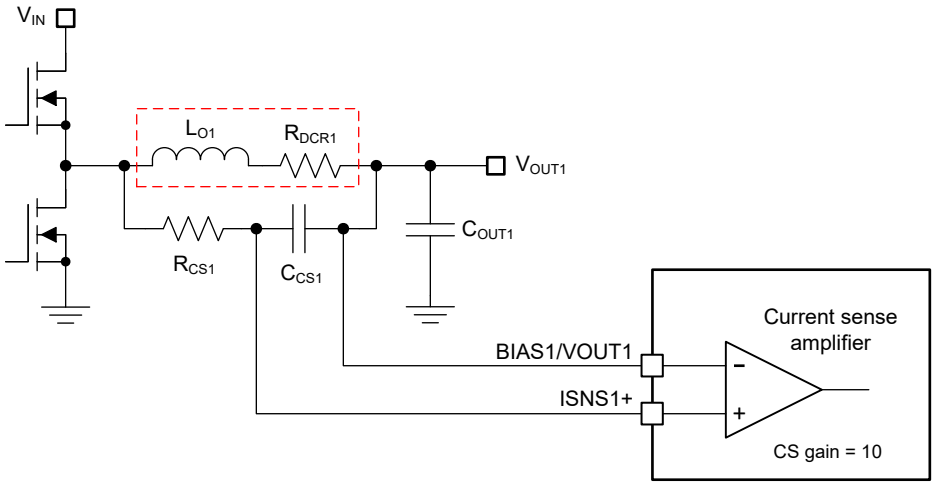

図 7-6. Inductor DCR Current Sensing Implementation

Use 式 9 to calculate the voltage drop across the sense capacitor in the s-domain. When the $R_{CS}C_{CS}$ time constant is equal to L_O/R_{DCR}, the voltage developed across the sense capacitor, C_{CS}, is a replica of the inductor DCR voltage and accurate current sensing is achieved. If the $R_{CS}C_{CS}$ time constant is not equal to the L_O/R_{DCR} time constant, there is a sensing error as follows:

- $R_{CS}C_{CS} > L_O/R_{DCR}$ → the DC level is correct, but the AC amplitude is attenuated.
- $R_{CS}C_{CS} < L_O/R_{DCR}$ → the DC level is correct, but the AC amplitude is amplified.

$$V_{CS}(s) = \frac{1 + s \cdot \frac{L_O}{R_{DCR}}}{1 + s \cdot R_{CS} \cdot C_{CS}} \cdot R_{DCR} \cdot \left(I_{OUT(CL)} + \frac{\Delta I_L}{2} \right) \quad (9)$$

Choose the C_{CS} capacitance greater than or equal to 100nF to maintain a low-impedance sensing network, thus reducing the susceptibility of noise pickup from the switch node. Carefully observe *セクション 8.4.1* to make sure that noise and DC errors do not corrupt the differential current sense signals applied between the respective ISNS1/2+ and VOUT1/2 pins.

7.3.13 MOSFET Gate Drivers (HO1, HO2, LO1, LO2)

The LM5137-Q1 contains N-channel MOSFET gate drivers and associated high-side level shifters to drive the external N-channel MOSFETs. The high-side gate driver works in conjunction with the integrated bootstrap diode and external bootstrap capacitor C_{BOOT}. During the conduction interval of the low-side MOSFET, the SW voltage is approximately 0V and C_{BOOT} charges from VCC through the diode.

The LM5137-Q1 controls the HO and LO outputs with an adaptive dead-time methodology such that both outputs (HO and LO) are never enabled at the same time, preventing cross conduction. When the controller commands LO to be enabled, the adaptive dead-time logic first disables HO and waits for the HO minus SW differential voltage to drop below 2V (typical). LO is then enabled after a small delay (HO fall to LO rising delay). Similarly, the HO turn-on is delayed until the LO voltage has dropped below 2V. HO is then enabled after a small delay (LO falling to HO rising delay). This technique provides adequate dead-time for any size N-channel MOSFET component or parallel MOSFET configurations.

As V_{IN} approaches the V_{OUT} setpoint, the LM5137-Q1 turns on the integrated charge pump to keep the high-side MOSFET on, thus achieving true 100% duty cycle. This action allows for the lowest possible dropout voltage from input to output. Caution is advised when adding series gate resistors, as this can decrease the effective dead-time. The selected N-channel high-side MOSFET determines the appropriate bootstrap capacitance values C_{BOOT} in accordance with 式 10.

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$$C_{BOOT} = \frac{Q_G}{\Delta V_{CBOOT}} \quad (10)$$

where

- Q_G is the total gate charge of the high-side MOSFET at the applicable gate drive voltage, normally 5V
- ΔV_{CBOOT} is the voltage variation of the high-side MOSFET driver after turn-on

To determine C_{BOOT}, choose ΔV_{CBOOT} so that the available gate drive voltage is not significantly impacted. An acceptable range of ΔV_{CBOOT} is 100mV to 200mV. The bootstrap capacitor must be a low-ESR ceramic capacitor, typically 0.1µF. Given the nominal VCC voltage of 5V, use logic-level power MOSFETs with $R_{DS(on)}$ rated at V_{GS} = 4.5V.

7.3.14 Output Configurations (CNFG)

Using a resistor designated as R_{CNFG} connected from CNFG to AGND, configure the LM5137-Q1 as a primary controller (independent dual outputs or interleaved single output) or as a secondary controller for paralleled phases in high-current applications.

7.3.14.1 Independent Dual-Output Operation

The LM5137-Q1 has two outputs that can operate independently. Both V_{OUT1} and V_{OUT2} can be set to fixed output setpoints of 3.3V, 5V, or 12V using one resistor from VDDA to FB1 or FB2 as needed. Alternatively, set the output voltage setpoints between 0.8V and 60V using external feedback resistors based on 式 4. See 表 7-5 and 図 7-7.

表 7-5. Configuration Modes for Independent Dual Outputs

R_{CNFG}	PRIMARY / SECONDARY	DRSS	INDEPENDENT OR INTERLEAVED OUTPUTS
10kΩ	Primary	OFF	Independent
19.1kΩ	Primary	DRSS1	Independent
29.4kΩ	Primary	DRSS2	Independent

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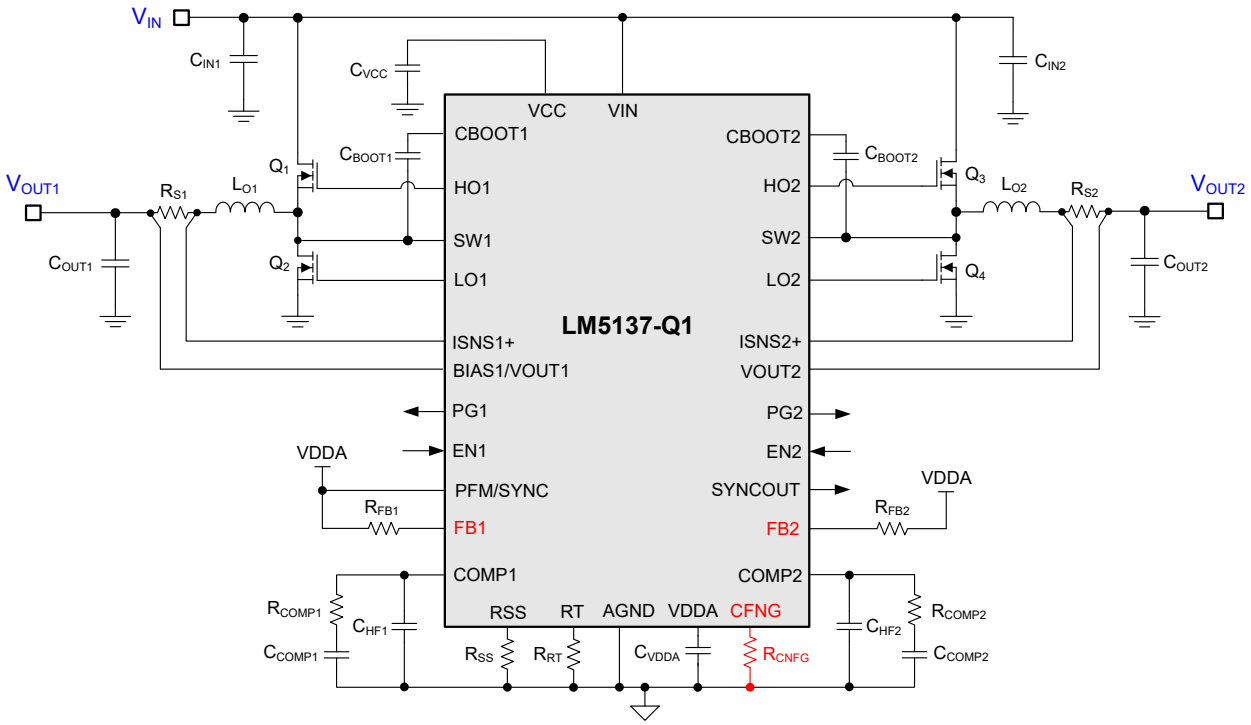

図 7-7. LM5137-Q1 Regulator Schematic Configured for Independent Dual Outputs

7.3.14.2 Single-Output Interleaved Operation

Based on a resistor R_{CNFG} connected from CNFG to AGND, configure the LM5137-Q1 as for single-output interleaved operation. As shown in 表 7-6, use 41.2kΩ to disable DRSS and 54.9kΩ or 71.5kΩ to enable DRSS at 5% or 10% frequency spreading, respectively. This setup disables the error amplifier of channel 2 and places the error amplifier in a high impedance state. The controller is then in a primary, secondary configuration, and the SYNCOUT clock is 180° lagging HO2 (or 180° leading HO1).

As shown in 図 7-8, connect COMP1 to COMP2 and use FB1 to set the output voltage setpoint.

表 7-6. Configuration Modes for Single-Output Interleaved Operation

R_{CNFG}	PRIMARY / SECONDARY	DRSS	INDEPENDENT OR INTERLEAVED OUTPUTS
41.2kΩ	Primary	OFF	Interleaved
54.9kΩ	Primary	DRSS1	Interleaved
71.5kΩ	Primary	DRSS2	Interleaved

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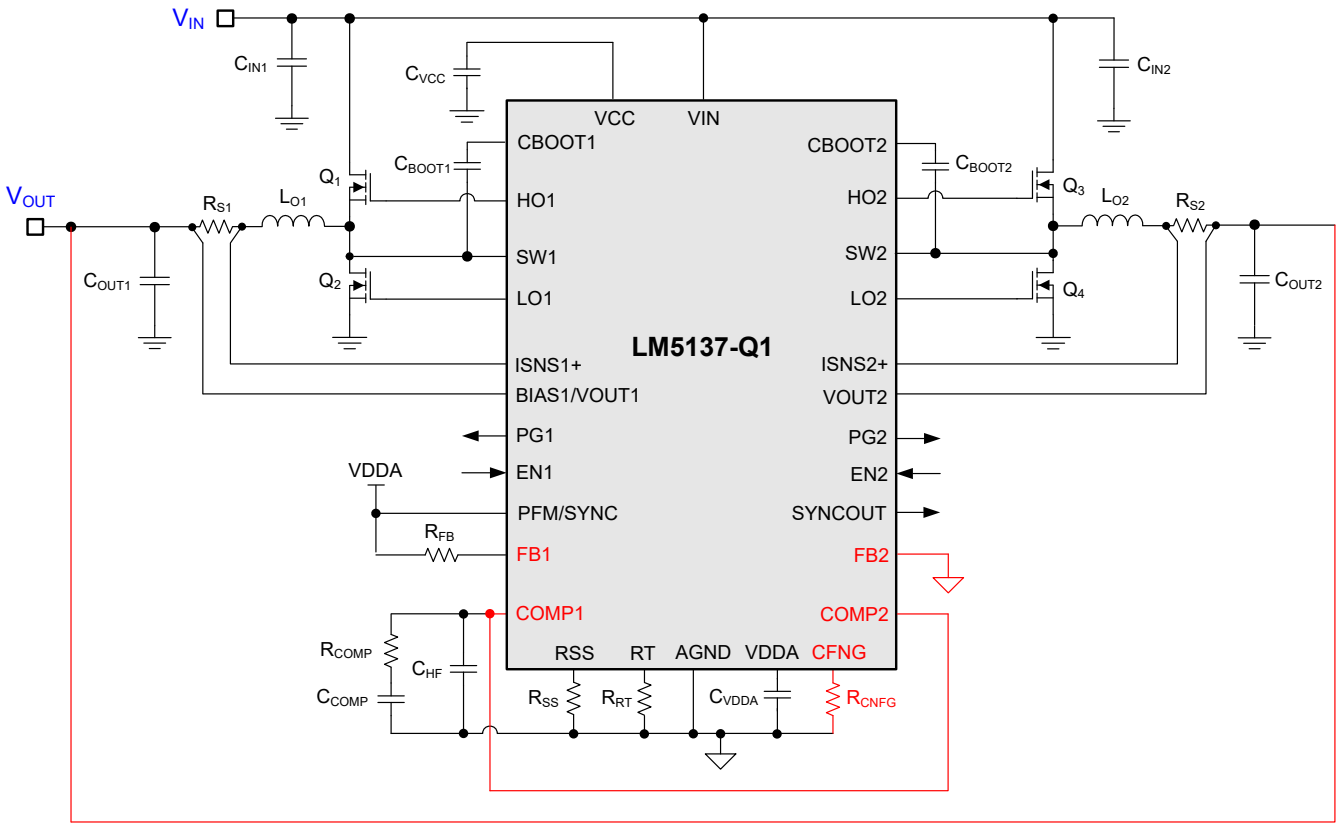

図 7-8. LM5137-Q1 Two-phase Regulator Schematic Configured for Single-output Interleaved Operation

7.3.14.3 Single-Output Multiphase Operation

A multiphase (three or four phases) regulator requires two LM5137-Q1 controllers, as illustrated in 図 7-9.

Configure the first controller (CNTRL1) as a primary and the second controller (CNTRL2) as a secondary. To configure the second controller, connect a 90.kΩ resistor from CNFG to AGND. This disables both feedback error amplifiers of the secondary controller, placing them in a high-impedance state.

- Connect the COMP1 and COMP2 pins together on both primary and secondary controllers
- Connect SYNCOUT from the primary to PFM/SYNC of the secondary controller
- Connect the RSS pins of the both controllers
- Connect all the outputs together
- Tie FB2 (primary controller) and FB4 (secondary controller) to GND
- If PFM mode operation is required, connect FB1 of the secondary controller to PFM/SYNC of the primary controller. Otherwise, connect FB1 to GND.

The SYNCOUT of the primary controller is 90° out-of-phase and facilitates interleaved operation. RT is not used for the oscillator when the LM5137-Q1 is in secondary mode but instead used for slope compensation. Therefore, select the RT resistance to be the same as that of the primary. See 表 7-7.

See the *Benefits of a Multiphase Buck Converter* white paper and *Multiphase Buck Design From Start to Finish* application report for more information.

表 7-7. Configuration Modes for Single-Output Multiphase Operation

R_{CNFG}	PRIMARY / SECONDARY	DRSS	INDEPENDENT OR INTERLEAVED OUTPUTS
41.2kΩ	Primary	OFF	Interleaved
54.9kΩ	Primary	DRSS1	Interleaved
71.5kΩ	Primary	DRSS2	Interleaved

表 7-7. Configuration Modes for Single-Output Multiphase Operation (続き)

R_{CNFG}	PRIMARY / SECONDARY	DRSS	INDEPENDENT OR INTERLEAVED OUTPUTS
90.9kΩ	Secondary	N/A	Interleaved

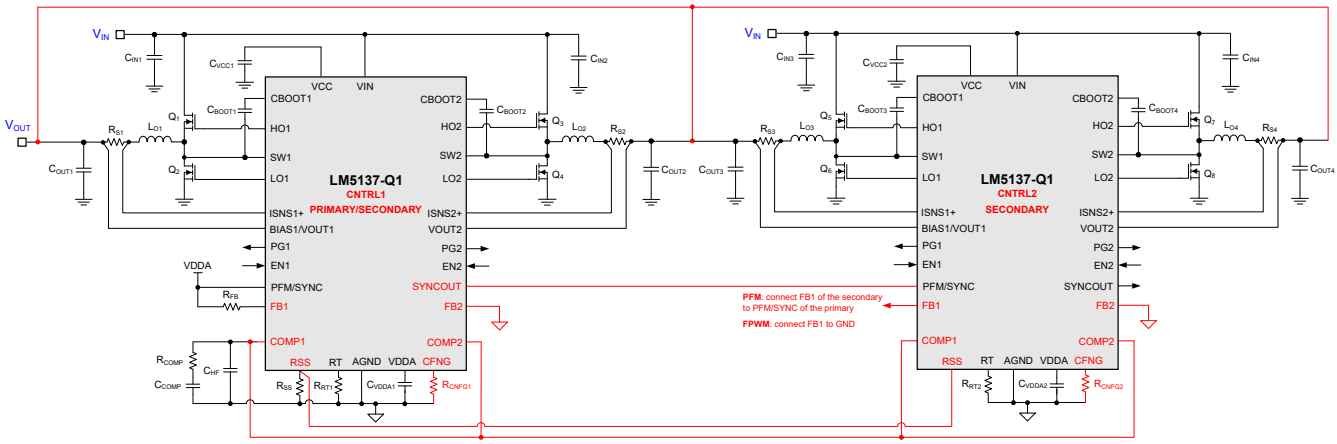

図 7-9. LM5137-Q1 Multiphase Regulator Schematic Configured for Single-Output Interleaved Operation

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7.4 Device Functional Modes

7.4.1 Sleep Mode

The LM5137-Q1 operates with peak current-mode control such that the compensation (COMP) voltage is proportional to the peak inductor current. During no-load or light-load conditions, the output capacitor discharges very slowly. As a result, the COMP voltage does not demand the driver output pulses on a cycle-by-cycle basis. When the LM5137-Q1 controller detects 16 missed switching cycles, the device enters sleep mode and switches to a low I_Q state to reduce the current drawn from the input. For the LM5137-Q1 to go into sleep mode, the device must be programmed for diode emulation (tie PFM/SYNC to VDDA).

The typical controller I_Q in sleep mode is 12.7µA with channel 1 set to 5V output and channel 2 disabled. When the LM5137-Q1 goes to sleep, PG1/2 are disabled. The nFAULT1/2 output are still active in case a fault is detected.

7.4.2 PFM Mode

A synchronous buck regulator implemented with a low-side MOSFET rather than a diode has the capability to sink negative current from the output during light-load, overvoltage, and prebias start-up conditions. The LM5137-Q1 provides a diode emulation feature that can be enabled to prevent reverse (drain-to-source) current flow in the low-side MOSFET. When configured for diode emulation (DEM), the low-side MOSFET is switched off when reverse current flow is detected by sensing of the applicable SW voltage using a zero-cross comparator. The benefit of this configuration is lower power loss at light-load conditions; the disadvantage being slower light-load transient response.

The diode emulation feature is configured with the PFM/SYNCIN pin. To enable diode emulation and thus achieve discontinuous conduction mode (DCM) operation at light loads, connect PFM/SYNCIN to VDDA. If FPWM or continuous conduction mode (CCM) operation is desired, tie PFM/SYNCIN to AGND. See 表 7-8. Note that diode emulation is automatically engaged (in both PFM and FPWM modes) to prevent reverse current flow during a prebias start-up. A gradual change from DCM to CCM operation provides monotonic start-up performance.

表 7-8. PFM Settings

PFM/SYNCIN	FPWM / PFM
VDDA	PFM
AGND	FPWM
External clock	FPWM

表 7-9. Errata

ITEM	OBSERVED BEHAVIOR	COMMENTS
1	LO on one channel can be deactivated when the SW voltage on the other channel transitions high. This event only occurs in PFM mode.	This event can decrease the efficiency in PFM.

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8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LM5137-Q1 is a dual-channel or dual-phase synchronous buck controller used to convert a higher input voltage to one or two lower output voltages. The following sections consider the power-train and compensation components and provide specific circuit design examples for single- and dual-output implementations. To expedite and streamline the process of designing of an LM5137-Q1-based regulator, a comprehensive LM5137-Q1 Quickstart Calculator is available for download to assist the designer with component selection for a given application.

8.1.1 Power Train Components

A comprehensive understanding of the buck regulator power train components is critical to successfully completing an efficient and reliable synchronous buck regulator design. The following sections discuss the following:

- Power MOSFETs
- Buck inductor
- Input and output capacitors
- EMI input filter

8.1.1.1 Power MOSFETs

The choice of power MOSFETs has an outsized impact on DC/DC regulator performance. A MOSFET with low on-state resistance, $R_{DS(on)}$, reduces conduction loss, whereas low parasitic capacitances enable faster transition times and reduced switching loss. Normally, the lower the $R_{DS(on)}$ of a MOSFET, the higher the gate charge and output charge (Q_G and Q_{OSS}, respectively), and vice versa. As a result, the product of $R_{DS(on)}$ and Q_G is commonly specified as a MOSFET figure-of-merit. Low thermal resistance of a given package makes sure that the MOSFET power dissipation does not result in excessive MOSFET die temperature.

The main parameters affecting power MOSFET selection in an LM5137-Q1 application are as follows:

- $R_{DS(on)}$ at V_{GS} = 5V
- Drain-source voltage rating, BV_{DSS}, is typically 40V, 60V or 80V, depending on the maximum input voltage.
- Gate charge parameters at V_{GS} = 5V
- Output charge, Q_{OSS}, at the relevant input voltage
- Body diode reverse recovery charge, Q_{RR}
- Gate threshold voltage, $V_{GS(th)}$, derived from the Miller plateau evident in the Q_G versus V_{GS} plot in the MOSFET data sheet. With a Miller plateau voltage typically in the range of 2.5V to 3.2V, the 5V gate drive amplitude of the LM5137-Q1 provides an adequately-enhanced MOSFET when on and a margin against Cdv/dt shoot-through when off.

The MOSFET-related power losses for one channel are summarized by the equations presented in 表 8-1, where suffixes 1 and 2 represent high-side and low-side MOSFET parameters, respectively. While the influence of inductor ripple current is considered, second-order loss modes, such as those related to parasitic inductances and switch-node voltage ringing, are not included. A comprehensive *Quickstart Calculator* available from the LM5137-Q1 product folder provides power loss calculations based on the entered MOSFET parameters, including $R_{DS(on)}$ and Q_G.

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表 8-1. MOSFET Power Losses

POWER LOSS MODE	HIGH-SIDE MOSFET	LOW-SIDE MOSFET
MOSFET conduction(2) (3)	$P_{cond1} = D \cdot \left(I_{OUT}^{2} + \frac{\Delta I_L^2}{12} \right) \cdot R_{DS(on)1}$	$P_{cond2} = D' \cdot \left(I_{OUT}^{2} + \frac{\Delta I_L^2}{12} \right) \cdot R_{DS(on)2}$
MOSFET switching	$P_{sw1} = \frac{V_{IN} \cdot F_{SW}}{2} \left[\left(I_{OUT} - \frac{\Delta I_L}{2} \right) \cdot t_R + \left(I_{OUT} + \frac{\Delta I_L}{2} \right) \cdot t_F \right]$	Negligible
MOSFET gate drive(1)	$P_{Gate1} = V_{CC} \cdot F_{SW} \cdot Q_{G1}$	$P_{Gate2} = V_{CC} \cdot F_{SW} \cdot Q_{G2}$
MOSFET output charge(4)	$P_{Coss} = F_{SW} \cdot \left(V_{IN} \cdot Q_{oss2} + E_{oss1} - E_{oss2} \right)$	
Body diode conduction	N/A	$P_{cond_{BD}} = V_F \cdot F_{SW} \left[\left(I_{OUT} + \frac{\Delta I_L}{2} \right) \cdot t_{dt1} + \left(I_{OUT} - \frac{\Delta I_L}{2} \right) \cdot t_{dt2} \right]$
Body diode reverse recovery(5)	$P_{RR} = V_{IN} \cdot F_{SW} \cdot Q_{RR2}$	

(1) Gate drive loss is apportioned based on the internal gate resistance of the MOSFET, externally added series gate resistance, and the relevant driver resistance of the LM5137-Q1.
(2) MOSFET $R_{DS(on)}$ has a positive temperature coefficient of approximately 4500ppm/°C. The MOSFET junction temperature, T_J, and the rise over ambient temperature is dependent upon the device total power dissipation and the thermal impedance. When operating at or near minimum input voltage, make sure that the MOSFET $R_{DS(on)}$ is rated for the available gate drive voltage.
(3) D' = 1–D is the duty cycle complement.
(4) MOSFET output capacitances, C_{oss1} and C_{oss2}, are highly non-linear with voltage. These capacitances are charged losslessly by the inductor current at high-side MOSFET turnoff. During turn-on, however, a current flows from the input to charge the output capacitance of the low-side MOSFET. E_{oss1}, the energy of C_{oss1}, is dissipated at turn-on, but this dissipation is offset by the stored energy E_{oss2} on C_{oss2}. For more detail, refer to *Comparison of deadtime effects on the performance of DC-DC converters with GaN FETs and silicon MOSFETs*, ECCE 2016.
(5) MOSFET body diode reverse recovery charge, Q_{RR}, depends on many parameters, particularly forward current, current transition speed, and temperature.

The high-side (control) MOSFET carries the inductor current during the PWM on-time (or D interval) and typically incurs most of the switching losses, so make sure to choose a high-side MOSFET that balances conduction and switching loss contributions. The total power dissipation in the high-side MOSFET is the sum of the following:

- Losses due to conduction
- Switching (voltage-current overlap)
- Output charge
- Typically two-thirds of the net loss attributed to body diode reverse recovery

The low-side (synchronous) MOSFET carries the inductor current when the high-side MOSFET is off (or 1–D interval). The low-side MOSFET switching loss is negligible as is switched at zero voltage – current just communicates from the channel to the body diode or vice versa during the transition dead times. The LM5137-Q1, with the adaptive gate drive timing, minimizes body diode conduction losses when both MOSFETs are off. Such losses scale directly with switching frequency.

In high step-down ratio applications, the low-side MOSFET carries the current for a large portion of the switching period. Therefore, to attain high efficiency, optimizing the low-side MOSFET for low $R_{DS(on)}$ is critical. In cases where the conduction loss is too high or the target $R_{DS(on)}$ is lower than available in a single MOSFET, connect two low-side MOSFETs in parallel. The total power dissipation of the low-side MOSFET is the sum of the losses due to channel conduction, body diode conduction, and typically one-third of the net loss attributed to body diode reverse recovery. The LM5137-Q1 is well suited to drive TI's portfolio of power MOSFETs.

8.1.1.2 Buck Inductor

For most applications, choose a buck inductance such that the inductor ripple current, ΔI_L, is between 30% and 50% of the maximum DC output current at nominal input voltage. Choose the inductance using 式 11 based on a peak inductor current given by 式 12.

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$$L_O = \frac{V_{OUT}}{\Delta I_L \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

$$I_{L(peak)} = I_{OUT} + \frac{\Delta I_L}{2} \quad (12)$$

Check the inductor data sheet to make suret hat the saturation current rating is well above the peak inductor current of a particular design. Ferrite-cored inductors have very low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. Low inductor core loss is evidenced by reduced no-load input current and higher light-load efficiency. However, ferrite core materials exhibit a hard saturation characteristic where the inductance collapses abruptly when the saturation current is exceeded. This action results in an outsized increase in inductor ripple current and higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that the saturation current rating of an inductor generally decreases as the core temperature increases. Of course, accurate overcurrent protection is critical to avoiding inductor saturation.

8.1.1.3 Output Capacitors

Ordinarily, the output capacitor energy store of the regulator combined with the control loop response are prescribed to maintain the integrity of the output voltage within the dynamic (transient) tolerance specifications. The usual boundaries restricting the output capacitors in power management applications are driven by finite available PCB area, component footprint and profile, and cost. As the load step amplitude and slew rate increase, the capacitor parasitics – equivalent series resistance (ESR) and equivalent series inductance (ESL) – take greater precedence in shaping the load transient response of the regulator.

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a reservoir of charge for step-load transient events. Typically, ceramic capacitors provide extremely low ESR to reduce the output voltage ripple and noise spikes, while tantalum and polymer electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

Based on the static specification of peak-to-peak output voltage ripple denoted by ΔV_{OUT}, choose an output capacitance that is higher than that given by 式 13.

$$C_{OUT} \geq \frac{\Delta I_L}{8 \cdot F_{SW} \sqrt{\Delta V_{OUT}^2 - \left(R_{ESR} \cdot \Delta I_L\right)^2}} \quad (13)$$

図 8-1 conceptually illustrates the relevant current waveforms during both load-on and load-off transitions. As shown, the slew rate of the inductor current represent a large-signal constraint as the inductor current ramps to match the new load-current level following a load transient. This slew-rate limiting exacerbates the deficit of charge in the output capacitor, which must be replenished as rapidly as possible during and after a load-on transient. Similarly, during and after a load-off transient, the slew rate limiting of the inductor current adds to the surplus of charge in the output capacitor that must be depleted as quickly as possible.

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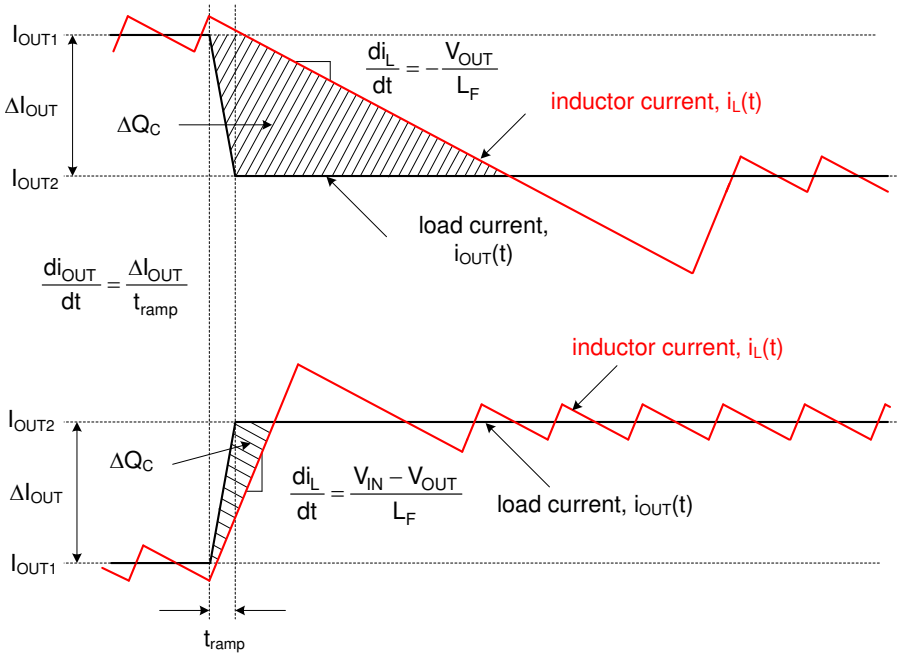

図 8-1. Load Transient Response Representation Showing C_{OUT} Charge Surplus or Deficit

In a typical regulator application of 12V input to low output voltage (for example, 3.3V), the load-off transient represents the worst case in terms of output voltage transient deviation. In that voltage conversion ratio application, the steady-state duty cycle is close to 30% and the large-signal inductor current slew rate when the duty cycle collapses to zero is approximately $-V_{OUT}/L$. Compared to a load-on transient, the inductor current takes much longer to transition to the required level. The surplus of charge in the output capacitor causes the output voltage to significantly overshoot. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp below the nominal level following the load step. In this scenario, a large output capacitance can be advantageously employed to absorb the excess charge and minimize the voltage overshoot.

式 13 calculates the output capacitance to meet the dynamic specification of output voltage overshoot during such a load-off transient (denoted as $\Delta V_{OVERSHOOT}$ with step reduction in output current given by ΔI_{OUT}).

$$C_{OUT} \geq \frac{L_O \cdot \Delta I_{OUT}^2}{\left(V_{OUT} + \Delta V_{OVERSHOOT}\right)^2 - V_{OUT}^2} \tag{14}$$

The capacitor manufacturer data sheet provides the ESR and ESL, either explicitly as specifications or implicitly in the impedance versus frequency curve. Depending on the type, size, and construction, electrolytic capacitors have significant ESR, 10mΩ and above, and relatively high ESL, 10nH to 20nH. PCB traces contribute some parasitic resistance and inductance as well. Ceramic output capacitors, have low ESR and ESL contributions at the switching frequency, and the capacitive impedance dominates. However, depending on the package and voltage rating of the ceramic capacitor, the effective capacitance can drop quite significantly with applied DC voltage and operating temperature.

Ignoring the ESR term in 式 13 gives a quick estimation of the minimum ceramic capacitance necessary to meet the output ripple specification. Two to four 47µF, 6.3V or 10V, X7R capacitors in 1210 footprint are a common choice for a 5V output. Use 式 14 to determine if additional capacitance is necessary to meet the load-off transient overshoot specification.

A composite implementation of ceramic and electrolytic capacitors highlights the rationale for paralleling capacitors of dissimilar chemistries yet complementary performance. The frequency response of each capacitor

is accretive in that each capacitor provides desirable performance over a certain part of the applicable frequency range. While the ceramic provides excellent mid- and high-frequency decoupling characteristics with low ESR and ESL to minimize the switching frequency output ripple, the electrolytic device with large bulk capacitance provides low-frequency energy storage to cope with lower frequency load-transient demands.

8.1.1.4 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the buck power stage due to switching-frequency AC currents. TI recommends using X7S or X7R dielectric ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching power loop, position the input capacitors as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET. Use 式 15 to calculate the input capacitor RMS current for a single-channel buck regulator.

$$I_{CIN,rms} = \sqrt{D \cdot \left({I_{OUT}}^2 \cdot (1-D) + \frac{\Delta I_L^2}{12} \right)} \tag{15}$$

The highest input capacitor RMS current occurs at D = 0.5, at which point the RMS current rating of the input capacitors is approximately equal to half the output current.

Ideally, the DC component of input current is provided by the input voltage source and the AC component by the input ceramic capacitors. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{OUT} − I_{IN}) during the D interval and sink I_{IN} during the 1−D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, use 式 16 to calculate the peak-to-peak ripple voltage amplitude.

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D \cdot (1-D)}{F_{SW} \cdot C_{IN}} + I_{OUT} \cdot R_{ESR} \tag{16}$$

Use 式 17 to calculate the input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN}.

$$C_{IN} \geq \frac{D \cdot (1-D) \cdot I_{OUT}}{F_{SW} \cdot (\Delta V_{IN} - R_{ESR} \cdot I_{OUT})} \tag{17}$$

Place low-ESR ceramic capacitors in parallel with a higher valued bulk capacitance to provide optimized input filtering for the regulator and damping to mitigate the effects of input parasitic inductance resonating with high-Q ceramics. While dependent on switching frequency and load current level, four 10µF, 50V, X7R, ceramic decoupling capacitors are usually sufficient for 12V battery automotive applications. As outlined in セクション 8.1.1.5, select the input bulk capacitor equal to three to four times the derated ceramic value and make sure the bulk capacitor is rated for the full operating temperature range.

Of course, a two-channel buck regulator with 180° out-of-phase interleaved switching provides input ripple current cancellation and reduced input capacitor current stress. The previous equations represent valid calculations when one output is disabled and the other output is fully loaded.

8.1.1.5 EMI Filter

Switching regulators exhibit a negative input impedance characteristic, which is lowest at the minimum input voltage and full load. An underdamped LC filter exhibits a high output impedance at the resonant frequency of the filter. For stability, the filter output impedance, approximated by the characterisitic impedance of the LC components, must be less than the absolute value of the regulator input impedance.

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$$Z_{IN} = \left| -\frac{V_{IN(min)}^{2}}{P_{IN}} \right| \tag{18}$$

The EMI filter design steps are as follows:

- Calculate the required attenuation of the EMI filter at the switching frequency, where C_{IN} represents the existing capacitance at the input of the switching regulator.
- The input filter inductor L_{IN} is usually selected between 1µH and 6.8µH, but can be lower to reduce losses in a high-current design.
- Calculate input filter capacitor C_F.

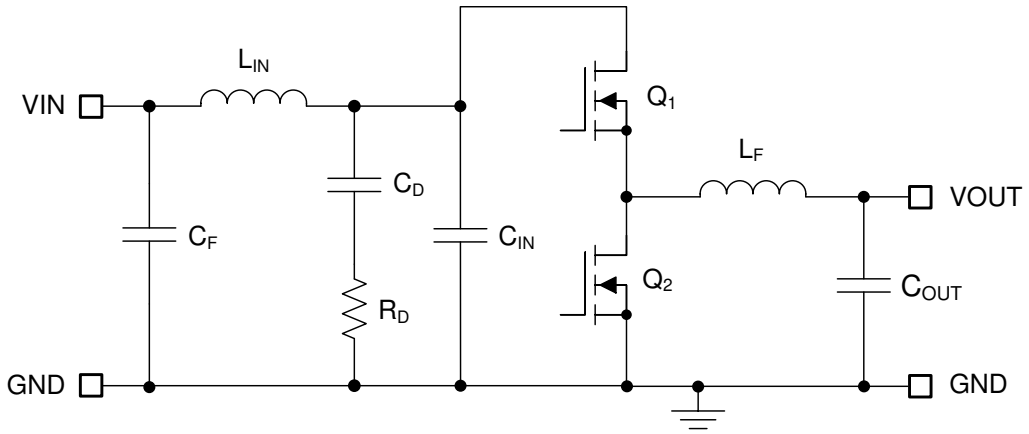

図 8-2. Buck Regulator With π-Stage EMI Filter

By calculating the first harmonic current from the Fourier series of the input current waveform and multiplying by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), 式 19 presents an expression to obtain the required attenuation.

$$Attn = 20\log\left(\frac{I_{L(PEAK)}}{\pi^{2} \cdot F_{SW} \cdot C_{IN}} \cdot \sin\left(\pi \cdot D_{MAX}\right) \cdot \frac{1}{1\,\mu V} \right) - V_{MAX} \tag{19}$$

where

- V_{MAX} is the allowed dBµV noise level for the applicable conducted EMI specification (for example, CISPR 25 Class 5)
- C_{IN} is the existing input capacitance of the buck regulator
- D_{MAX} is the maximum operating duty cycle (at minimum input voltage)
- $I_{L(PEAK)}$ is the peak inductor current

For filter design purposes, the current at the input can be modeled as a square-wave. Determine the EMI filter capacitance C_F from 式 20.

$$C_F = \frac{1}{L_{IN}} \left(\frac{10^{\frac{|Attn|}{40}}}{2\pi \cdot F_{SW}} \right)^{2} \tag{20}$$

Adding an input filter to a switching regulator as shown in 図 8-2 modifies the control-to-output transfer function. The output impedance of the filter must be sufficiently low such that the input filter does not significantly affect

the loop gain of the buck regulator. The impedance peaks at the filter resonant frequency. Use 式 21 to calculate the resonant frequency of the filter.

$$f_{res} = \frac{1}{2\pi \cdot \sqrt{L_{IN} \cdot C_F}} \tag{21}$$

The purpose of R_D in 図 8-2 is to reduce the peak output impedance of the filter at the resonant frequency. Capacitor C_D blocks the DC component of the input voltage to avoid excessive power dissipation in R_D. Capacitor C_D must have lower impedance than R_D at the resonant frequency with a capacitance value greater than that of the input capacitor C_{IN}. This requirement prevents C_{IN} from interfering with the cutoff frequency of the main filter. Added damping is needed when the output impedance of the filter is high at the resonant frequency (Q of the filter formed by L_{IN} and C_{IN} is too high). Use an electrolytic capacitor C_D for parallel damping with a value given by 式 22.

$$C_D \geq 4 \cdot C_{IN} \tag{22}$$

Use 式 23 to select the damping resistor R_D.

$$R_D = \sqrt{\frac{L_{IN}}{C_{IN}}} \tag{23}$$

8.1.2 Error Amplifier and Compensation

図 8-3 shows a type-II compensator using a transconductance error amplifier (EA) for the voltage loop. As shown in 式 24, the dominant pole of the EA open-loop gain is set by the EA output resistance, $R_{O\text{-}EA}$, and effective bandwidth-limiting capacitance, C_{BW}.

$$G_{EA(openloop)}(s) = -\frac{g_m \cdot R_{O\text{-}EA}}{1 + s \cdot R_{O\text{-}EA} \cdot C_{BW}} \tag{24}$$

式 24 neglects the EA parasitic high-frequency pole. Use 式 25 to calculate the compensator transfer function from output voltage to COMP node, including the gain contribution from the (internal or external) feedback resistor network

$$G_c(s) = \frac{\hat{v}_c(s)}{\hat{v}_{out}(s)} = -\frac{V_{REF}}{V_{OUT}} \cdot \frac{g_m \cdot R_{O\text{-}EA} \cdot \left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right)} \tag{25}$$

where

- V_{REF} is the internal feedback voltage reference of 0.8V
- g_m is the EA transconductance of 600µS
- $R_{O\text{-}EA}$ is the error amplifier output resistance of 74MΩ

$$\omega_{Z1} = \frac{1}{R_{COMP} \cdot C_{COMP}} \tag{26}$$

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$$\omega_{p1} = \frac{1}{R_{O\text{-}EA} \cdot \left(C_{COMP} + C_{HF} + C_{BW}\right)} \cong \frac{1}{R_{O\text{-}EA} \cdot C_{COMP}} \quad (27)$$

$$\omega_{p2} = \frac{1}{R_{COMP} \cdot \left(C_{COMP} \left\| \left(C_{HF} + C_{BW}\right)\right.\right)} \cong \frac{1}{R_{COMP} \cdot C_{HF}} \quad (28)$$

The EA compensation components create a pole close to the origin, a zero, and a high-frequency pole. Typically, R_{COMP} << $R_{O\text{-}EA}$ and C_{COMP} >> C_{BW} and C_{HF}, so the approximations are valid.

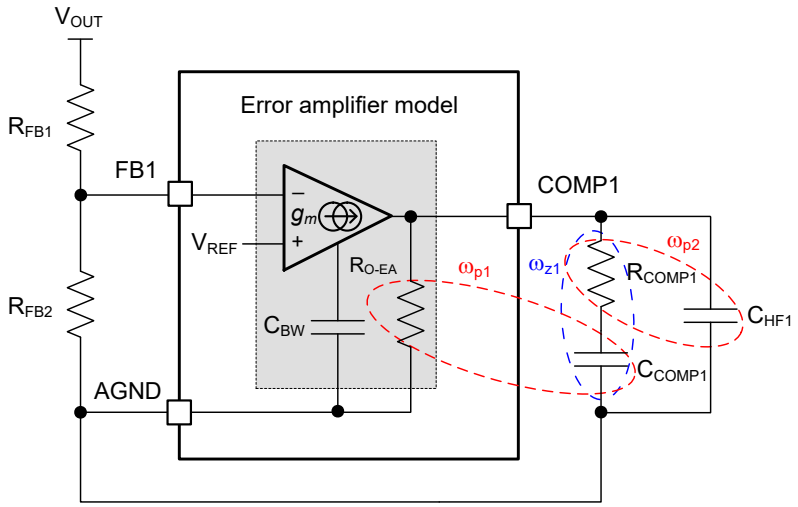

図 8-3. Voltage-loop Error Amplifier and Compensation Network

ADVANCE INFORMATION

8.2 Typical Applications

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation and test results of an LM5137-Q1-powered implementation, see the *TI Designs* reference design library.

8.2.1 Design 1 – Dual 5V and 3.3V, 20A Buck Regulator for 12V Automotive Battery Applications

図 8-4 shows the schematic diagram of a dual-output synchronous buck regulator with output voltage setpoints of 5V and 3.3V and a rated load current of 20A for each output. In this example, the target half-load and full-load efficiencies are 96% and 94%, respectively, based on a nominal input voltage of 13.5V that ranges from 6.5V to 36V. The switching frequency is set at 440kHz by resistor R_{RT}. The 5V output provides bias power to reduce IC power dissipation and improve efficiency.

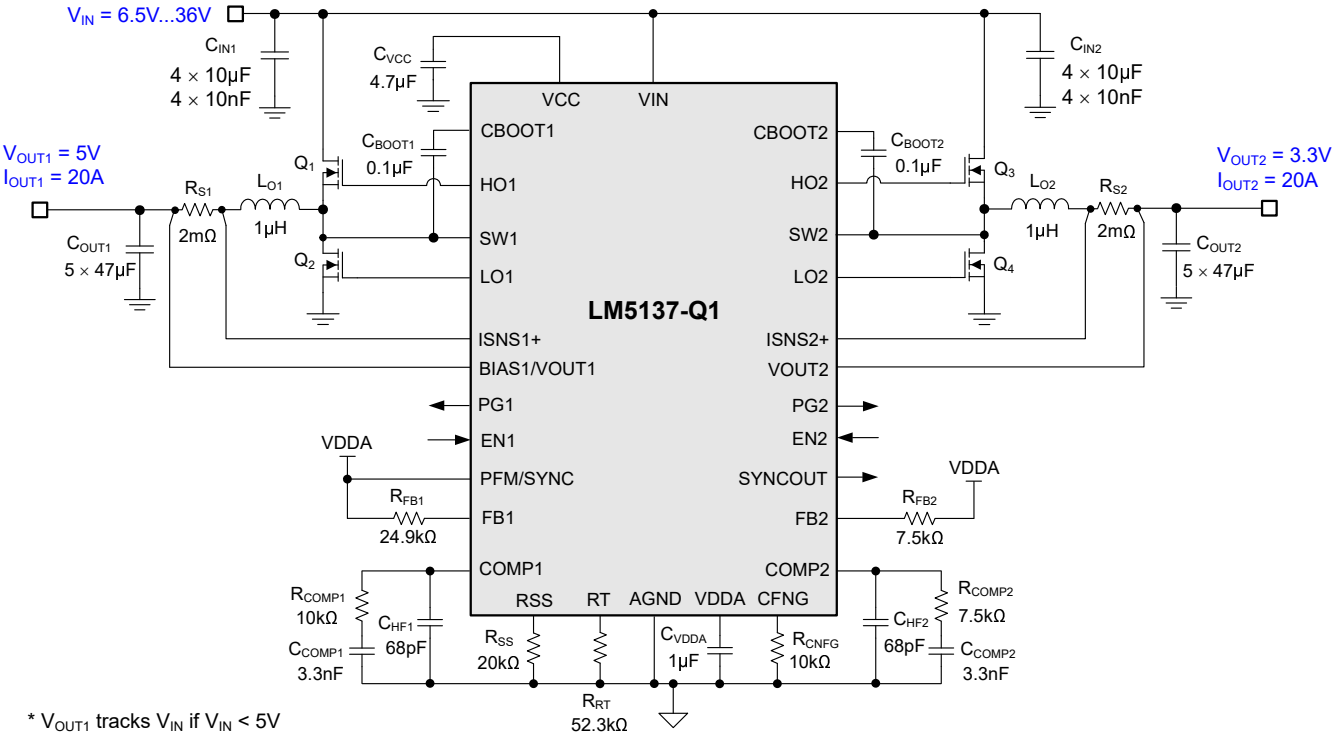

図 8-4. Application Circuit 1 Using The LM5137-Q1 Buck Controller at 440kHz

注

This and subsequent circuit examples are provided herein to showcase the LM5137-Q1 controller in several different applications. Depending on the source impedance of the input supply, connect an input electrolytic capacitor to make sure of stability, particularly at low input voltage and high power operating conditions. See セクション 8.3 for more detail.

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8.2.1.1 Design Requirements

表 8-2 shows the intended input, output, and performance parameters for this automotive circuit example.

表 8-2. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady state)	6.5V to 36V, nominal 13.5V
Minimum transient input voltage (cold crank)	4.5V
Maximum transient input voltage (load dump)	36V
Output voltages	5V, 3.3V
Output currents (EDC) (1)	20A
Output currents (TDC) (1)	15A
Switching frequency	440kHz
Target efficiency at 5V, 15A	96%
Target efficiency at 3.3V, 15A	94.5%
Output voltage regulation	±1%
Loop crossover frequency	60kHz
Phase margin	> 45°
No-load sleep current, channel 2 disabled	< 20µA
Shutdown current	4µA

(1) EDC and TDC refer to electrical and thermal design currents, respectively.

Resistor R_{RT} sets the switching frequency at 440kHz. In terms of control loop performance, the target loop crossover frequency is set in the range of 10% to 15% of switching frequency – 60kHz in this example – with a target phase margin greater than 45°. Connecting a resistance of 20kΩ at RSS sets the output voltage soft-start times to 4.6ms.

表 8-3 cites the selected buck regulator powertrain components, with many of the components available from multiple vendors. *セクション 8.1.1.1* describes selection of power MOSFETs for lowest conduction and switching power loss. This application circuit uses 40V logic-level MOSFETs, metal-alloy buck inductors with low DCR, low-ESL shunts, and ceramic input and output capacitors – all AEC qualified.

表 8-3. List of Materials for Application Circuit 1

REFERENCE DESIGNATOR	QTY	SPECIFICATION (1)	MANUFACTURER	PART NUMBER
C_{IN1}, C_{IN2}	8	10µF, 50V, X7R, 1210, ceramic, AEC-Q200	TDK	CNA6P1X7R1H106K
		10µF, 50V, X7S, 1210, ceramic, AEC-Q200	Murata	GCM32EC71H106K
			TDK	CGA6P3X7S1H106K
C_{OUT1}, C_{OUT2}	8	47µF, 10V, X7S, 1210, ceramic, AEC-Q200	TDK	CNA6P1X7S1A476M
			Murata	GCM32EC71A476K
L_{O1}, L_{O2}	2	1µH, 2.3mΩ, 37A, 10.85 × 10 × 5.2mm, AEC-Q200	Cyntec	VCHA105D-1R0MS6
		1µH, 2.3mΩ, 37A, 11 × 10 × 5.1mm, AEC-Q200	Bourns	SRP1050WA-1R0M
		1µH, 2.1mΩ, 24A, 10.8 × 10 × 5mm, AEC-Q200	Eaton	HCM1A1105V2-1R0-R
		1µH, 2.7mΩ, 33.8A, 10.85 × 10 × 3.8mm, AEC-Q200	Würth Electronik	784373680010
		1µH, 2.4mΩ, 36.6A, 10.5 × 10 × 6.5mm, AEC-Q200	TDK	SPM10065VT-1R0M-D
Q_1, Q_3	2	40V, 3.6mΩ, 9nC, SON 5 × 6, AEC-Q101	Infineon	IAUCN04S7L028ATMA1
Q_2, Q_4	2	40V, 2.4mΩ, 15nC, SON 5 × 6, AEC-Q101	Infineon	IAUCN04S7L019ATMA1
R_{S1}, R_{S2}	2	Shunt, 2mΩ ±2%, ±100ppm/°C, 1225, 3W, AEC-Q200	Susumu	KRL6432E-M-R002-G
U_1	1	LM5137-Q1 80V dual-channel buck controller, AEC-Q100	Texas Instruments	LM5137QRHARQ1

(1) See the *Third-Party Products Disclaimer*.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5137-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Custom Design With Excel Quickstart Tool

Select components based on the regulator specifications using the LM5137-Q1 *Quickstart Calculator* available for download from the LM5137-Q1 product folder.

8.2.1.2.3 Inductor Calculations

1. Use 式 29 to calculate the required buck inductance for each channel based on an approximate 30% inductor peak-to-peak ripple current at nominal input voltage.

$$L_{O1} = \frac{V_{OUT1}}{\Delta I_{LO1} \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT1}}{V_{IN(nom)}}\right) = \frac{5\,V}{6A \cdot 440kHz} \cdot \left(1 - \frac{5\,V}{12\,V}\right) = 1.1\mu H$$

$$L_{O2} = \frac{V_{OUT2}}{\Delta I_{LO2} \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT2}}{V_{IN(nom)}}\right) = \frac{3.3\,V}{6\,A \cdot 440kHz} \cdot \left(1 - \frac{3.3\,V}{12\,V}\right) = 0.9\mu H \quad (29)$$

2. Select a standard inductor value of 1µH for both channels. Use 式 30 to calculate the peak inductor currents at maximum steady-state input voltage. Subharmonic oscillation occurs with a duty cycle greater than 50% for peak current-mode control. For design simplification, the LM5137-Q1 has an internal slope compensation ramp proportional to the switching frequency that is added to the current sense signal to damp any tendency toward subharmonic oscillation.

$$I_{LO1(PK)} = I_{OUT1} + \frac{\Delta I_{LO1}}{2} = I_{OUT1} + \frac{V_{OUT1}}{2 \cdot L_{O1} \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT1}}{V_{IN(max)}}\right) = 20\,A + \frac{5\,V}{2 \cdot 1\mu H \cdot 440kHz} \cdot \left(1 - \frac{5\,V}{36\,V}\right) = 24.9\,A$$

$$I_{LO2(PK)} = I_{OUT2} + \frac{\Delta I_{LO2}}{2} = I_{OUT2} + \frac{V_{OUT2}}{2 \cdot L_{O2} \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT2}}{V_{IN(max)}}\right) = 20\,A + \frac{3.3\,V}{2 \cdot 1\mu H \cdot 440kHz} \cdot \left(1 - \frac{3.3\,V}{36\,V}\right) = 23.4\,A \quad (30)$$

3. Based on 式 29, use 式 31 to cross-check the inductances to align the slope compensation ramp to an ideal one times the inductor current downslope.

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$$L_{O1,sc} = \frac{V_{OUT}[V] \cdot R_S[m\Omega]}{22 \cdot F_{SW}[MHz]} = \frac{5V \cdot 2m\Omega}{22 \cdot 0.44MHz} = 1.03\mu H$$

$$L_{O2,sc} = \frac{V_{OUT}[V] \cdot R_S[m\Omega]}{22 \cdot F_{SW}[MHz]} = \frac{3.3V \cdot 2m\Omega}{22 \cdot 0.44MHz} = 0.68\mu H \quad (31)$$

8.2.1.2.4 Shunt Resistors

1. Calculate the shunt resistance based on a maximum peak current capability at least 20% higher than the peak inductor current at full load to provide sufficient margin during startup and load-step transients. Calculate the shunt resistances using 式 32.

$$R_{S1} = \frac{V_{CS(th)}}{1.2 \cdot I_{LO1(PK)}} = \frac{60mV}{1.2 \cdot 24.9A} = 2.01m\Omega$$

$$R_{S2} = \frac{V_{CS(th)}}{1.2 \cdot I_{LO2(PK)}} = \frac{60mV}{1.2 \cdot 23.4A} = 2.14m\Omega \quad (32)$$

   where

   - $V_{CS(th)}$ is the 60mV current limit threshold.
2. Select a standard resistance value of 2mΩ for both shunts. A 1225 footprint component with wide aspect ratio termination design provides a 3W power rating, parasitic inductance (ESL) less than 1nH, and compact PCB layout. Carefully adhere to the layout guidelines in *セクション 8.4.1* to make sure that noise and DC errors do not corrupt the current-sense voltages measured differentially at the [ISNS1+, VOUT1] and [ISNS2+, VOUT2] pins.
3. Place the shunt resistor close to the inductor.
4. Use Kelvin sense connections and route the sense lines differentially from the shunt to the applicable pins of the LM5137-Q1.
5. The current-sense-to-output propagation delay (related to the current limit comparator, internal logic and power MOSFET gate drivers) causes the peak current to increase above the calculated current limit threshold. For a total propagation delay of $t_{CS-DELAY}$ of 70ns, use 式 33 to calculate the worst-case peak inductor current with the output shorted.

$$I_{LO1,pk-sc} = I_{LO2,pk-sc} = \frac{V_{CS(th)}}{R_{S1}} + \frac{V_{IN(max)} \cdot t_{CS-DELAY}}{L_{O1}} = \frac{60mV}{2m\Omega} + \frac{36V \cdot 70ns}{1\mu H} = 32.5A \quad (33)$$

6. Based on this result, select an inductor for each channel with saturation current greater than 33A across the full operating temperature range.

8.2.1.2.5 Ceramic Output Capacitors

1. Use 式 34 to estimate the output capacitance required to manage the output voltage overshoot during a load-off transient of 10A, assuming a load transient deviation specification of 100mV.

$$C_{OUT1} \geq \frac{L_{O1} \cdot \Delta I_{OUT1}^2}{(V_{OUT1} + \Delta V_{OVERSHOOT1})^2 - V_{OUT1}^2} = \frac{1\mu H \cdot (10A)^2}{(5V + 100mV)^2 - (5V)^2} = 99\mu F$$

$$C_{OUT2} \geq \frac{L_{O2} \cdot \Delta I_{OUT2}^2}{(V_{OUT2} + \Delta V_{OVERSHOOT2})^2 - V_{OUT2}^2} = \frac{1\mu H \cdot (10A)^2}{(3.3V + 100mV)^2 - (3.3V)^2} = 149\mu F \quad (34)$$

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2. Noting the voltage coefficient of ceramic capacitors where the effective capacitance decreases significantly with applied voltage, select four 47µF, 10V, X7R, 1210 ceramic output capacitors for each channel. According to the design tool from the capacitor vendor, these capacitors are each effectively 32µF and 41µF at 5V and 3.3V DC voltage, respectively.
3. Use 式 35 to estimate the peak-to-peak output voltage ripple of channel 1 at nominal input voltage.

$$\Delta V_{OUT1} = \Delta I_{LO1} \cdot \sqrt{\frac{1}{\left(8 \cdot F_{SW} \cdot C_{OUT1}\right)^2} + R_{ESR}^{\ 2}} = 6.8A \cdot \sqrt{\frac{1}{\left(8 \cdot 440kHz \cdot 128\mu F\right)^2} + \left(1m\Omega\right)^2} \approx 16mV \quad (35)$$

where

- R_{ESR} is the effective equivalent series resistance (ESR) of the output capacitors.
- 128µF is the total effective (derated) ceramic output capacitance at 5V.

4. Use 式 36 to calculate the output capacitor RMS ripple current at maximum input voltage. Verify that it is within the capacitor ripple current rating.

$$I_{CO1,RMS} = \frac{\Delta I_{LO1}}{\sqrt{12}} = \frac{10A}{\sqrt{12}} = 2.9A$$

$$I_{CO2,RMS} = \frac{\Delta I_{LO2}}{\sqrt{12}} = \frac{7A}{\sqrt{12}} = 2A \quad (36)$$

8.2.1.2.6 Ceramic Input Capacitors

A power supply input typically has a relatively high source impedance at the switching frequency. Good-quality input capacitors are necessary to limit the input ripple voltage. As mentioned earlier, dual-channel interleaved operation significantly reduces the input ripple amplitude. In general, the ripple current splits between the input capacitors based on the relative impedance of the capacitors at the switching frequency.

1. Select the input capacitors with sufficient voltage and RMS ripple current ratings.
2. Worst case input ripple for a two-channel buck regulator typically corresponds to when one channel operates at full load and the other channel is disabled or operates at no load. Use 式 37 to calculate the input capacitor RMS ripple current assuming a worst-case duty-cycle operating point of 50%.

$$I_{CIN,RMS} = I_{OUT1} \cdot \sqrt{D \cdot \left(1 - D\right)} = 20A \cdot \sqrt{0.5 \cdot \left(1 - 0.5\right)} = 10A \quad (37)$$

3. Use 式 38 to find the required input capacitance.

$$C_{IN} \geq \frac{D \cdot \left(1 - D\right) \cdot I_{OUT1}}{F_{SW} \cdot \left(\Delta V_{IN} - R_{ESR} \cdot I_{OUT1}\right)} = \frac{0.5 \cdot \left(1 - 0.5\right) \cdot 20A}{440kHz \cdot \left(270mV - 1m\Omega \cdot 20A\right)} = 45\mu F \quad (38)$$

where

- ΔV_{IN} is the input peak-to-peak ripple voltage specification.
- R_{ESR} is the input capacitor ESR.

4. Recognizing the voltage coefficient of ceramic capacitors, select four 10µF, 50V, X7R, 1210 ceramic input capacitors for each channel. Place these capacitors adjacent to the relevant power MOSFETs.
5. Use four 10nF, 50V, X7R, 0603 ceramic capacitors near each high-side MOSFET to supply the high di/dt current during MOSFET switching transitions. Such capacitors offer high self-resonant frequency (SRF) and low effective impedance above 100MHz. The result is lower power loop parasitic inductance, thus minimizing switch-node voltage overshoot and ringing for lower EMI signature. Refer to 図 8-25 and 図 8-27 for additional context.

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8.2.1.2.7 Feedback Resistors

Configure the dual outputs for fixed 5V and 3.3V voltage setpoints by tying the respective FB pins to VDDA through 24.9kΩ and 7.5kΩ resistors, respectively.

Alternatively, use feedback resistor dividers values for 5V and 3.3V output voltage setpoints based on the 0.8V feedback reference of the LM5137-Q1. Calculate the upper feedback resistors using 式 39 assuming a value of 15kΩ for the lower resistors.

$$R_{FB1} = R_{FB2} \cdot \left(\frac{V_{OUT1}}{V_{REF}} - 1 \right) = 15\,k\Omega \cdot \left(\frac{5\,V}{0.8\,V} - 1 \right) = 78.75\,k\Omega$$

$$R_{FB3} = R_{FB4} \cdot \left(\frac{V_{OUT1}}{V_{REF}} - 1 \right) = 15\,k\Omega \cdot \left(\frac{3.3\,V}{0.8\,V} - 1 \right) = 46.88\,k\Omega \quad (39)$$

式 40 calculates the resultant output voltage setpoints when using 78.7kΩ, 47kΩ and 15kΩ standard E192 0.5% resistor values.

$$V_{OUT1} = V_{REF} \cdot \left(1 + \frac{R_{FB2}}{R_{FB1}} \right) = 0.8\,V \cdot \left(1 + \frac{78.7\,k\Omega}{15\,k\Omega} \right) = 4.997\,V$$

$$V_{OUT2} = V_{REF} \cdot \left(1 + \frac{R_{FB3}}{R_{FB4}} \right) = 0.8\,V \cdot \left(1 + \frac{47\,k\Omega}{15\,k\Omega} \right) = 3.306\,V \quad (40)$$

In contrast to a fixed output option, installing a feedback resistor divider with a suitable series resistor, typically 50Ω, facilitates measurement of the loop gain characteristic as needed to characterize stability.

8.2.1.2.8 Input Voltage UVLO Resistors

Use 式 41 and 式 42 to calculate the input UVLO divider resistors, designated as R_{UV1} and R_{UV2} in 図 7-2, given input turn-on and turn-off voltages specified as 6.5V and 4.5V, respectively. Use a 10kΩ resistor in series with the applicable EN pin, designated as R_{UV3}, to increase the effective voltage hysteresis without using higher divider resistances.

$$R_{UV2} = \left[\frac{V_{EN(off)} - \left(V_{IN(off)} / V_{IN(on)} \right) \cdot V_{EN(on)}}{I_{EN(hys)}} - R_{UV3} \right] \cdot \frac{V_{IN(on)}}{V_{IN(on)} - V_{EN(on)}}$$

$$= \left[\frac{0.95\,V - \left(4.5\,V / 6.5\,V \right) \cdot 1V}{10\mu A} - 10\,k\Omega \right] \cdot \frac{6.5\,V}{6.5\,V - 1V} = 18.6\,k\Omega \quad (41)$$

$$R_{UV1} = R_{UV2} \cdot \left(\frac{V_{IN(on)}}{V_{EN(on)}} - 1 \right) = 19.1\,k\Omega \cdot \left(\frac{6.5\,V}{1V} - 1 \right) = 105\,k\Omega \quad (42)$$

Selecting standard 1% resistor values of 105kΩ and 19.1kΩ, calculate the actual input voltage turn-on and turn-off setpoints using 式 43.

$$V_{IN(on)} = V_{EN(on)} \cdot \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) = 1V \cdot \left(1 + \frac{105k\Omega}{19.1k\Omega}\right) = 6.5V$$

$$V_{IN(off)} = \left[V_{EN(off)} - I_{EN(hys)} \cdot \left(R_{UV3} + R_{UV1} \| R_{UV2}\right)\right] \cdot \left(1 + \frac{R_{UV1}}{R_{UV2}}\right)$$

$$= \left[0.95V - 10\mu A \cdot \left(10k\Omega + 105k\Omega \| 19.1k\Omega\right)\right] \cdot \left(1 + \frac{105k\Omega}{19.1k\Omega}\right) = 4.5V \quad (43)$$

8.2.1.2.9 Compensation Components

Choose compensation components for a stable control loop using the procedure outlined as follows.

1. Based on the target loop crossover frequency, f_C, of 60kHz, use 式 44 to calculate R_{COMP1}, assuming an effective output capacitance of 128µF. Select R_{COMP1} equal to 10kΩ.

$$R_{COMP1} = 2 \cdot \pi \cdot f_C \cdot \frac{V_{OUT}}{V_{REF}} \cdot \frac{R_S \cdot G_{CS}}{g_m} \cdot C_{OUT} = 2 \cdot \pi \cdot 60kHz \cdot \frac{5V}{0.8V} \cdot \frac{2m\Omega \cdot 10}{600\mu S} \cdot 128\mu F = 10k\Omega \quad (44)$$

2. Calculate C_{COMP1} to create a zero at the higher of (1) one tenth of the crossover frequency, or (2) the load pole. Select a capacitor value for C_{COMP1} of 3.3nF. In general, set the time constant of R_{COMP1} and C_{COMP1} at approximately 25µs to maintain a fast settling time of the output voltage following a load transient.

$$C_{COMP1} = \frac{10}{2 \cdot \pi \cdot f_C \cdot R_{COMP1}} = \frac{10}{2 \cdot \pi \cdot 60kHz \cdot 10\ k\Omega} = 2.6nF \quad (45)$$

3. Calculate C_{HF1} to create a pole at the lower of the ESR zero frequency or at half switching frquency (to attenuate high-frequency noise). Select a capacitor value for C_{HF1} of 68pF.

$$C_{HF1} = \frac{1}{2 \cdot \pi \cdot \frac{F_{SW}}{2} \cdot R_{COMP1}} = \frac{1}{2 \cdot \pi \cdot 220kHz \cdot 10\ k\Omega} = 72pF \quad (46)$$

注

Set a high loop crossover frequency with high R_{COMP} and low C_{COMP} values to improve the large-signal response when recovering from operation in dropout.

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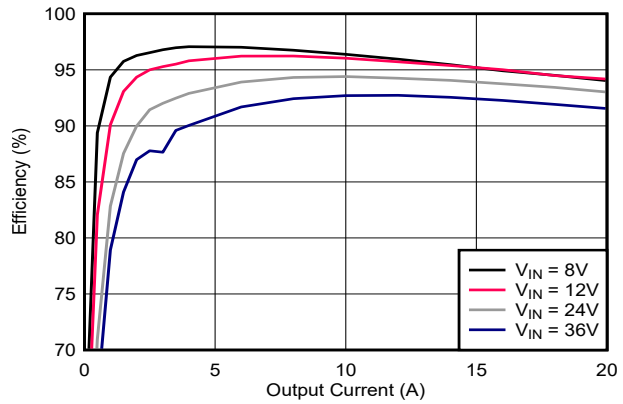
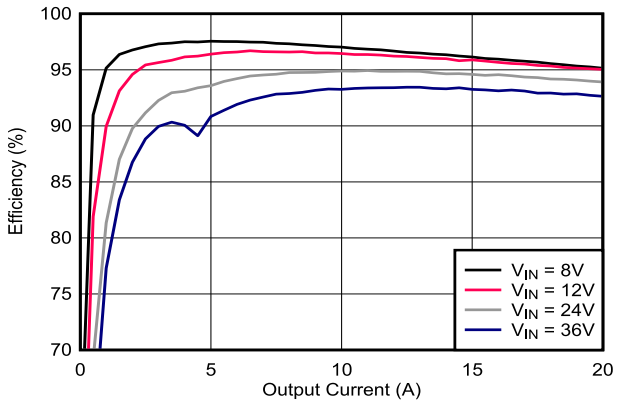
8.2.1.3 Application Curves



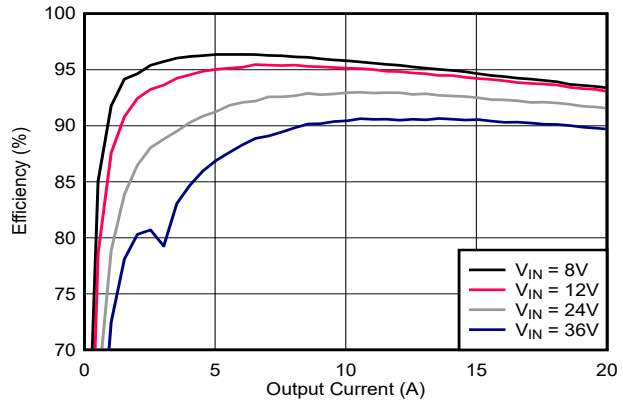
Channels 1 and 2 loaded equally

図 8-5. Efficiency vs I_{OUT}



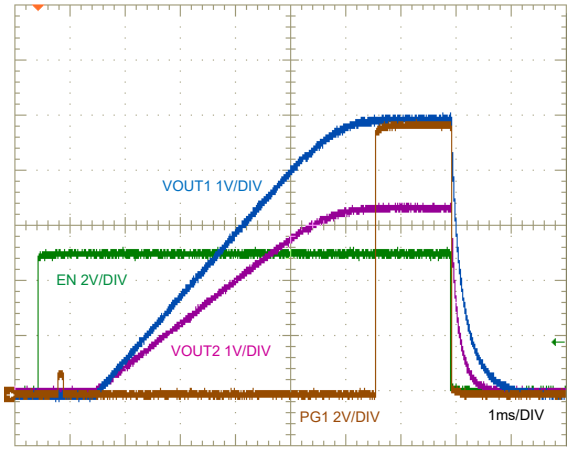
5V output, channel 2 disabled

図 8-6. Efficiency vs I_{OUT1}



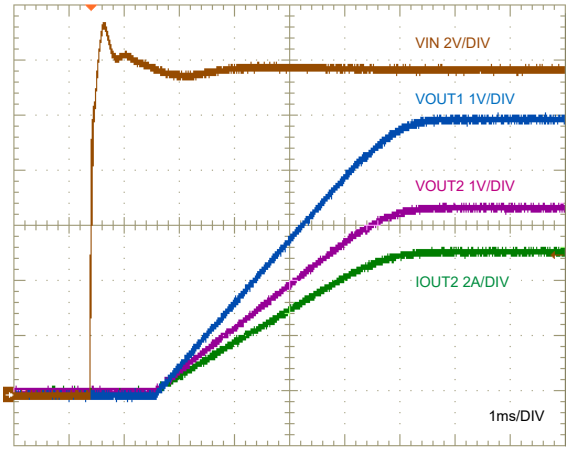
3.3V output, channel 1 disabled

図 8-7. Efficiency vs I_{OUT2}



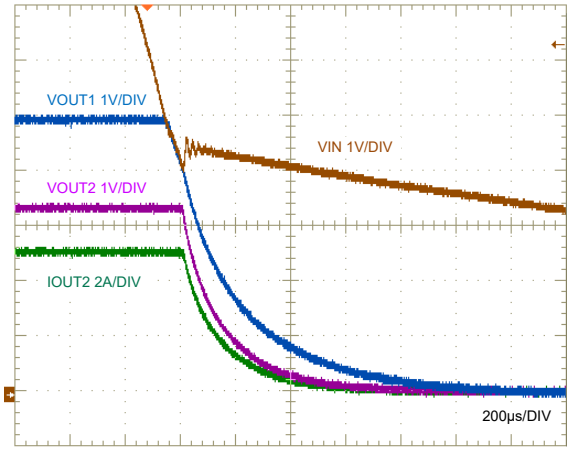
V_{IN} = 12V, V_{EN1} = V_{EN2} 5A resistive loads

図 8-8. Enable ON and OFF Characteristic



V_{IN} stepped to 12V 5A resistive loads

図 8-9. Ch1 and Ch2 Start-Up Characteristic



V_{IN} decreasing from 12V 5A resistive loads

図 8-10. Ch1 and Ch2 Shutdown Characteristic

8.2.1.3 Application Curves (continued)

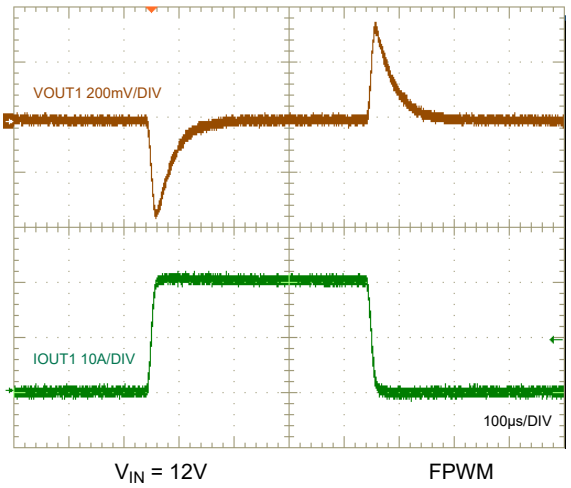


図 8-11. Load Transient, 5V Output, 0A to 20A

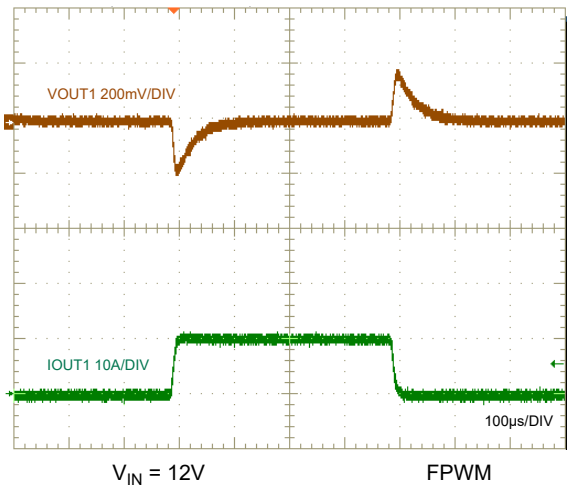


図 8-12. Load Transient, 5V Output, 0A to 10A

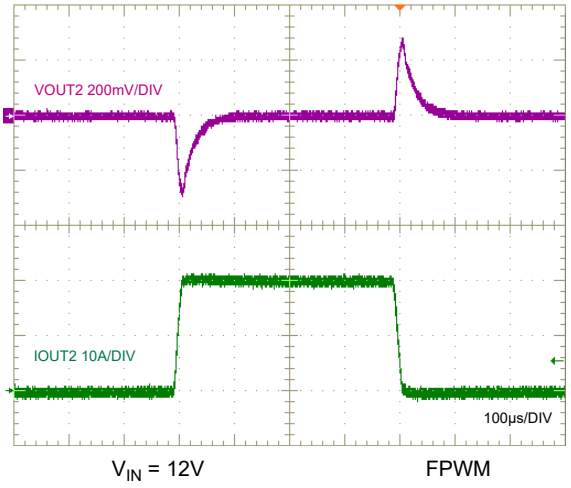


図 8-13. Load Transient, 3.3V Output, 0A to 20A

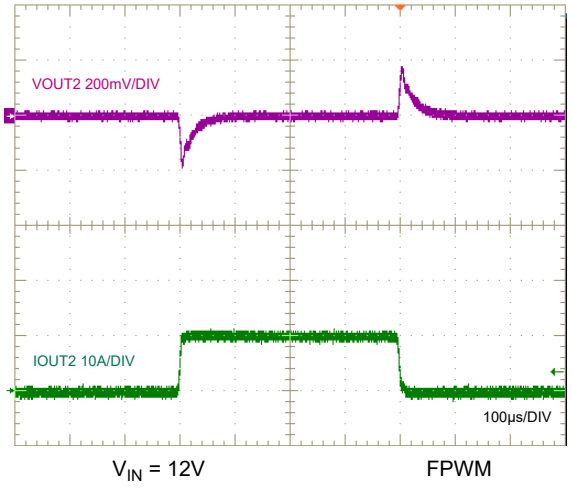


図 8-14. Load Transient, 3.3V Output, 0A to 10A

ADVANCE INFORMATION

8.2.2 Design 2 – Two-Phase, Single-Output Buck Regulator for Automotive ADAS Applications

図 8-15 shows the schematic diagram of a single-output, two-phase synchronous buck regulator with an output voltage of 5V and rated load current of 20A. In this example, the target half-load and full-load efficiencies are 93% and 91%, respectively, based on a nominal input voltage of 12V that ranges from 6V to 36V. The switching frequency is set at 2.1MHz by resistor R_{RT}. The 5V output supplies bias current to the controller to improve light-load efficiency. An output voltage of 3.3V is also possible simply by changing the voltage-set resistor (R_{FB} tied from FB1 to VDDA) from 24.9kΩ to 7.5kΩ.

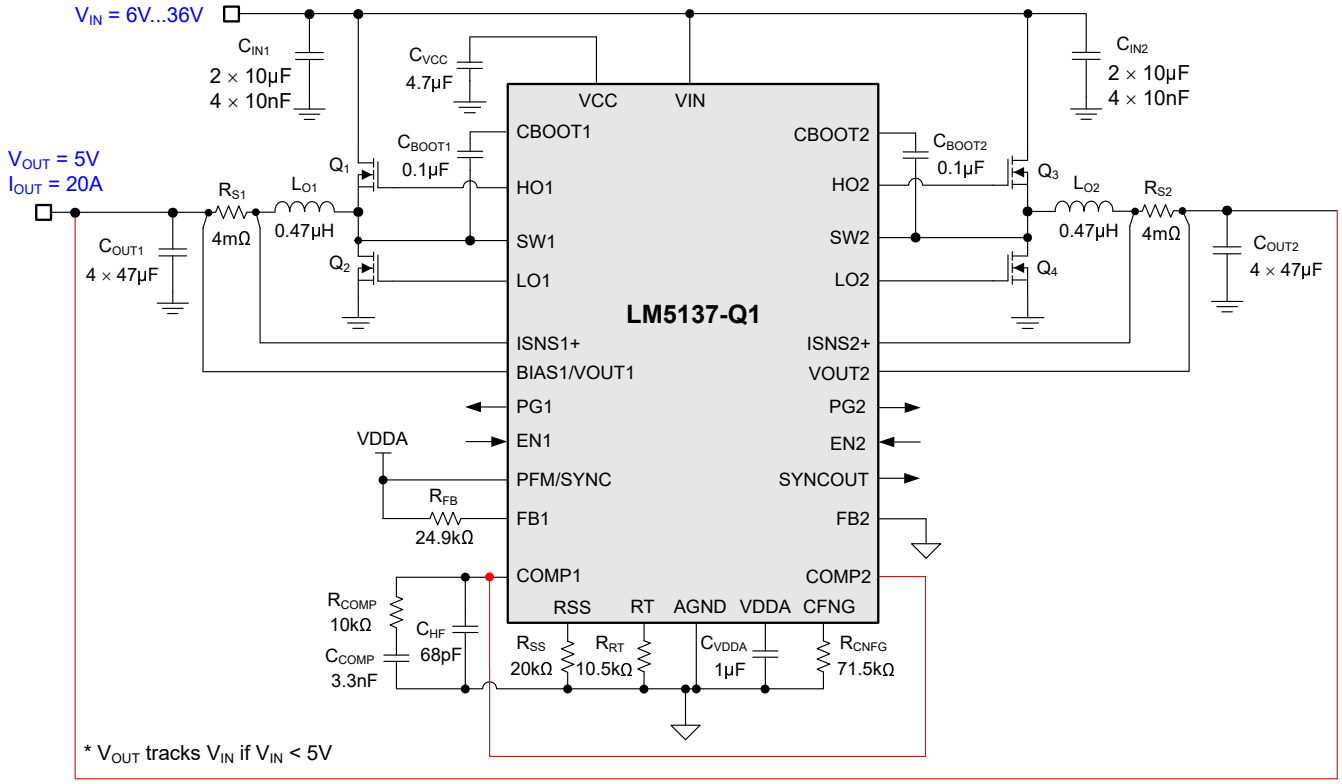


図 8-15. Application Circuit 2 With an LM5137-Q1 Two-phase Buck Regulator at 2.1MHz

8.2.2.1 Design Requirements

表 8-4 shows the intended input, output, and performance parameters for this automotive circuit example.

表 8-4. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady state)	8V to 18V
Minimum transient input voltage (cold crank)	6V
Maximum transient input voltage (load dump)	36V
Output voltage	5V
Output current	20A
Switching frequency	2.1MHz
Output voltage regulation	±1%
No-load sleep current with phase 2 disabled	< 20µA
Shutdown current	4µA

Resistor R_{RT} of 10.5kΩ sets the switching frequency at 2.1MHz. In terms of control loop performance, the target loop crossover frequency is 80kHz with a phase margin greater than 50°. Leaving the RSS pin open sets the output voltage soft-start time to 6.5ms.

表 8-5 cites the selected buck regulator powertrain components, with many of the components available from multiple vendors. Similar to circuit example 1, this design uses 40V logic-level MOSFETs, shielded buck inductors, shunt resistors with wide aspect ratio for low ESL, and an all-ceramic input and output capacitor implementation.

表 8-5. List of Materials for Application Circuit 2

REFERENCE DESIGNATOR	QTY	SPECIFICATION(1)	MANUFACTURER	PART NUMBER
C_{IN1}, C_{IN2}	4	10µF, 50V, X7R, 1210, ceramic, AEC-Q200	TDK	CNA6P1X7R1H106K
		10µF, 50V, X7S, 1210, ceramic, AEC-Q200	Murata	GCM32EC71H106KA03
			TDK	CGA6P3X7S1H106M
C_{OUT1}, C_{OUT2}	8	47µF, 6.3V, X7R, 1210, ceramic, AEC-Q200	Murata	GCM32ER70J476KE19L
			Taiyo Yuden	JMK325B7476KMHTR
		47µF, 6.3V, X7S, 1210, ceramic, AEC-Q200	TDK	CGA6P1X7S0J476M
L_{O1}, L_{O2}	2	0.47µH, 2.2mΩ, 26.5A, 6.71 × 6.51 × 3.1mm, AEC-Q200	Coilcraft	XGL6030-471MEC
		0.47µH, 3mΩ, 25A, 6.95 × 6.6 × 4.3mm, AEC-Q200	Cyntec	VCUW064ER47MS5
		0.47µH, 3.1mΩ, 20A, 7 × 6.9 × 3.8mm, AEC-Q200	Würth Electronik	744311047
		0.56µH, 3mΩ, 29A, 6.6 × 6.4 × 2.8mm, AEC-Q200	Bourns	SRP6030CA-R56M
Q_1, Q_3	2	40V, 4.7mΩ, 7nC, SON 5 × 6, AEC-Q101	Infineon	IAUC60N04S6L039ATMA
Q_2, Q_4	2	40V, 3.6mΩ, 9nC, SON 5 × 6, AEC-Q101	Infineon	IAUCN04S7L028ATMA
R_{S1}, R_{S2}	2	Shunt, 4mΩ ±1%, ±50ppm/°C, 0612, 1.5W, AEC-Q200	Susumu	KRL3216E-C-R004-F
U_1	1	LM5137-Q1 80V two-phase buck controller, AEC-Q100	Texas Instruments	LM5137QRHARQ1

(1) See *Third-Party Products Disclaimer*.

8.2.2.2 Detailed Design Procedure

See セクション 8.2.1.2.

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8.2.3 Design 3 – 12V, 20A, 400kHz, Two-Phase Buck Regulator for 48V Automotive Applications

図 8-16 shows the schematic diagram of a single-output, two-phase synchronous buck regulator with an output voltage of 12V and rated load current of 20A. In this example, the target half-load and full-load efficiencies are above 95% based on a nominal input voltage of 48V that ranges from 36V to 65V, with transients to 30V and 72V. The switching frequency is set at 400kHz by resistor R_{RT}. Bias power derives from the 12V output, thus improving light-load efficiency in particular. R_{FB} of 48.7kΩ (connected from FB1 to VDDA) establishes a fixed output setting of 12V.

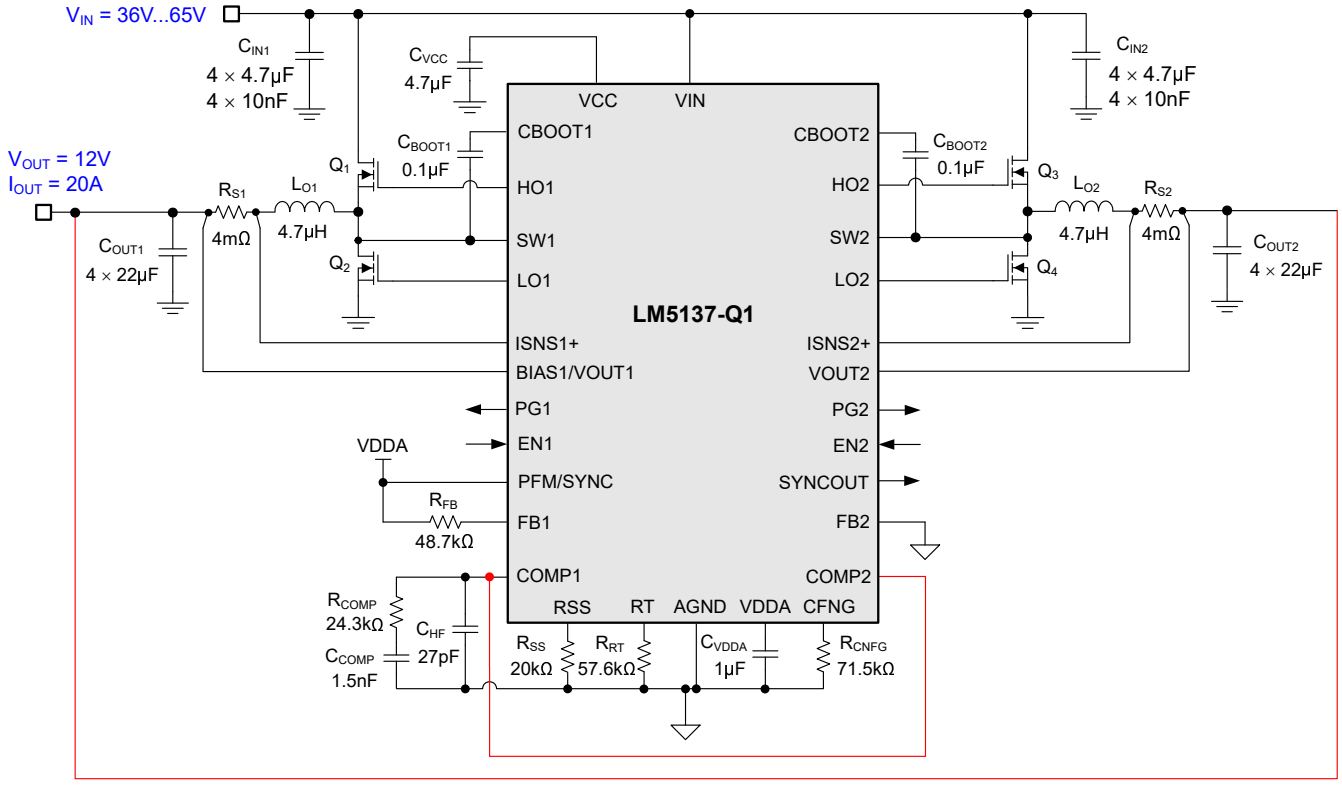

図 8-16. Application Circuit 3 With an LM5137-Q1 Two-phase Buck Regulator at 400kHz

8.2.3.1 Design Requirements

表 8-6 shows the intended input, output, and performance parameters for this circuit example.

表 8-6. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady state)	36V to 65V
Minimum transient input voltage	30V
Maximum transient input voltage	72V
Output voltage	12V
Output current	20A
Switching frequency	400kHz
Target efficiency at 20A	95.5%
Input voltage UVLO on, off	34V, 28V
No-load sleep current with phase 2 disabled	< 20µA
Shutdown current	4µA

Resistor R_{RT} of 57.6kΩ sets the switching frequency at 400kHz. In terms of control loop performance, the target loop crossover frequency is 60kHz with a phase margin greater than 50°. An RSS resistance of 20kΩ sets the output voltage soft-start time to 4.6ms.

表 8-7 cites the selected buck regulator powertrain components, with many of the components available from multiple vendors. This design uses 80V logic-level MOSFETs, shielded buck inductors, shunt resistors with wide aspect ratio for low ESL, 100V-rated ceramic input capacitors and 25V-rated ceramic output capacitors.

表 8-7. List of Materials for Application Circuit 3

REFERENCE DESIGNATOR	QTY	SPECIFICATION(1)	MANUFACTURER	PART NUMBER
C_{IN1}, C_{IN2}	8	4.7µF, 100V, X7S, 1210, ceramic, AEC-Q200	TDK	CGA6M3X7S2A475K200
			Murata	GCM32DC72A475KE02L
C_{OUT1}, C_{OUT2}	8	22µF, 25V, X7R, 1210, ceramic, AEC-Q200	TDK	CGA6P3X7R1E226M250
		22µF, 25V, X7S, 1210, ceramic, AEC-Q200	Murata	GCM32EC71E226KE36
L_{O1}, L_{O2}	2	4.7µH, 8.3mΩ, 15.7A, 10.85 × 10 × 5.2mm, AEC-Q200	Cyntec	VCHA105D-4R7MS6
		4.7µH, 9mΩ, 17A, 11 × 10 × 5.1mm, AEC-Q200	Bourns	SRP1050WA-4R7M
		4.7µH, 11.7mΩ, 13A, 10.8 × 10 × 5mm, AEC-Q200	Eaton	HCM1A1105V2-4R7-R
		4.7µH, 13.5mΩ, 16A, 10.85 × 10 × 3.8mm, AEC-Q200	Würth Electronik	784373680047
Q_1, Q_3	2	80V, 13.4mΩ, 8nC, SON 5 × 6, AEC-Q101	onsemi	NVMFS6H852NLT1G
Q_2, Q_4	2	80V, 6.2mΩ, 16nC, SON 5 × 6, AEC-Q101	onsemi	NVMFS6H836NLT1G
R_{S1}, R_{S2}	2	Shunt, 4mΩ ±1%, ±50ppm/°C, 0612, 1.5W, AEC-Q200	Susumu	KRL3216E-C-R004-F
U_1	1	LM5137-Q1 80V two-phase buck controller, AEC-Q100	Texas Instruments	LM5137QRHARQ1

8.2.3.2 Detailed Design Procedure

See セクション 8.2.1.2.

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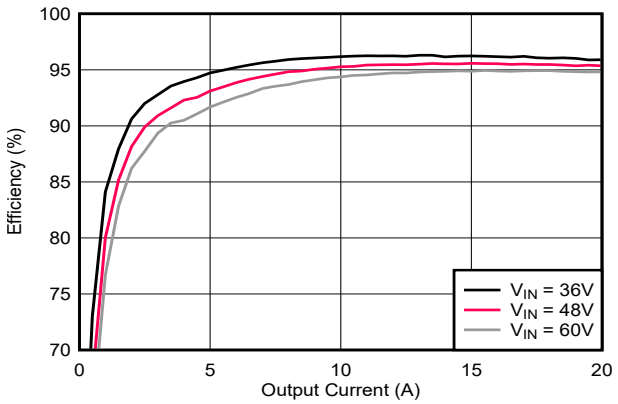
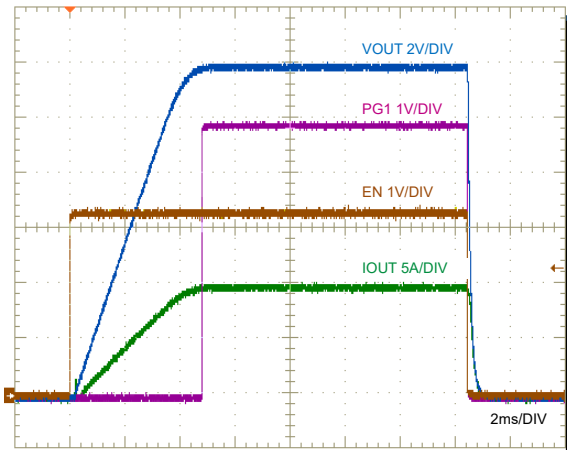
8.2.3.3 Application Curves



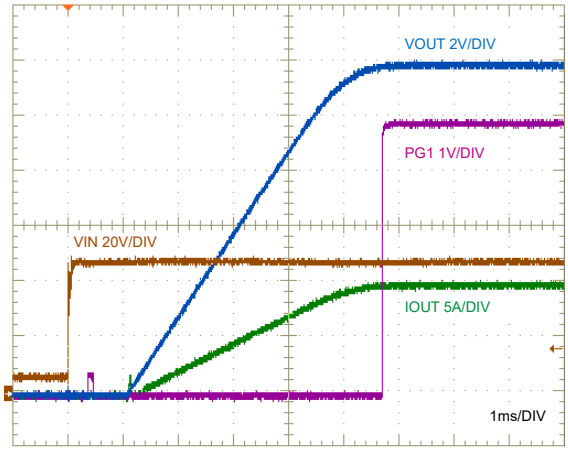
25°C ambient temperature

図 8-17. Efficiency vs I_{OUT}



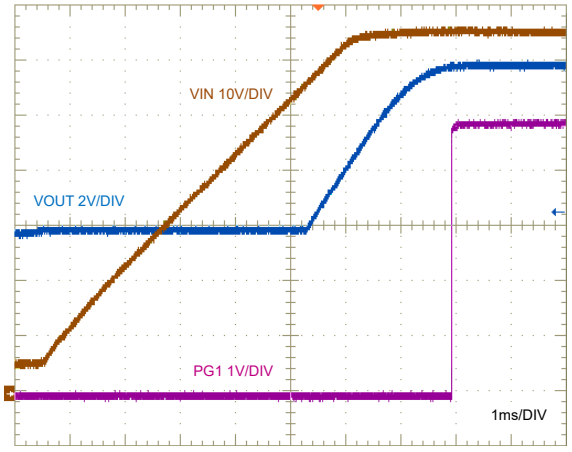
V_{IN} = 48V, V_{EN1} = V_{EN2} 10A resistive load

図 8-18. Enable ON and OFF Characteristic



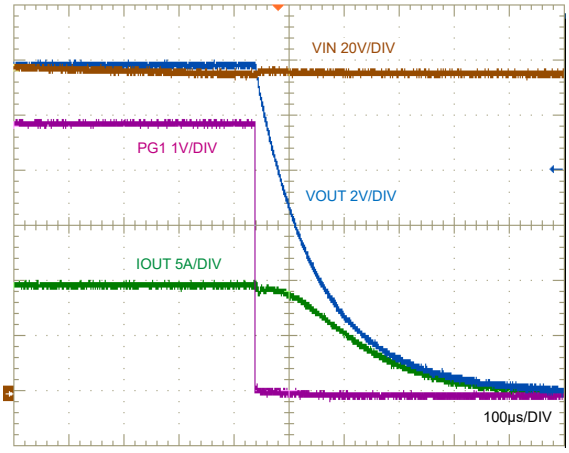
V_{IN} stepped to 48V 10A resistive load

図 8-19. Start-Up Characteristic



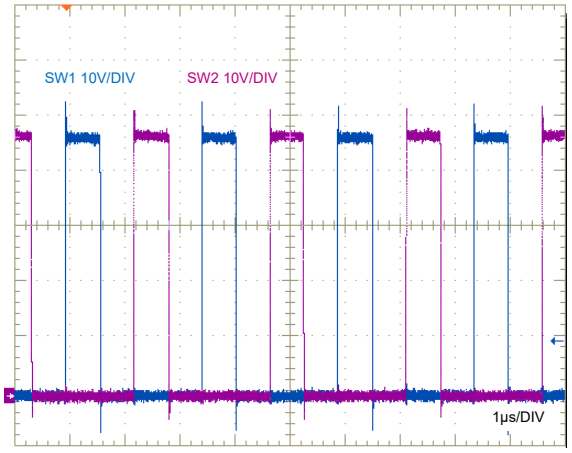
V_{IN} ramped to 65V 10A resistive load

図 8-20. Prebiased Start-Up Characteristic



V_{IN} decreasing from 48V 10A resistive load

図 8-21. Shutdown Characteristic



V_{IN} = 48V 10A load

図 8-22. Switch-node Voltages

8.2.3.3 Application Curves (continued)

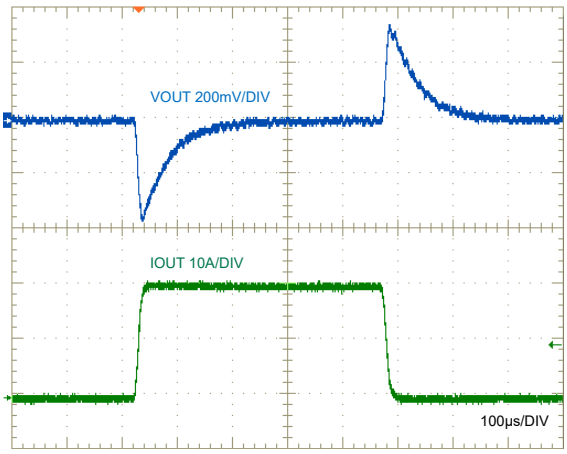


図 8-23. Load Transient, 0A to 20A

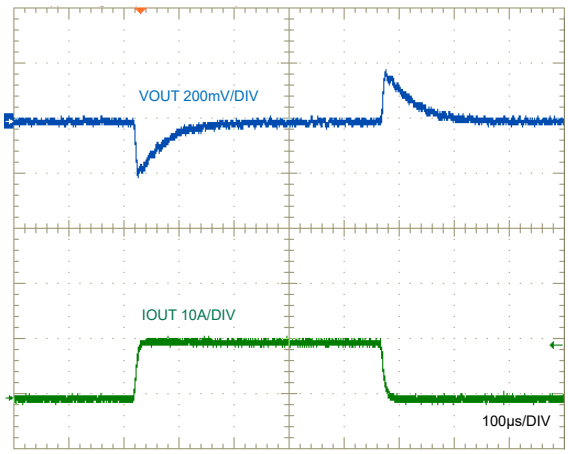


図 8-24. Load Transient, 0A to 10A

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8.3 Power Supply Recommendations

The LM5137-Q1 buck controller is designed to operate from a wide input voltage range of 4V to 80V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* tables. In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Use 式 47 to estimate the average input current.

$$I_{IN} = \frac{P_{OUT}}{V_{IN} \cdot \eta} \tag{47}$$

where

- η is the efficiency

If the regulator is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse effect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 47µF to 330µF is usually sufficient to provide parallel input damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the affects mentioned above. The *Simple Success with Conducted EMI for DC-DC Converters* application report provides helpful suggestions when designing an input filter for any switching regulator.

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8.4 Layout

8.4.1 Layout Guidelines

Proper PCB design and layout is important in a high-current, fast-switching circuit (with high current and voltage slew rates) to achieve a robust and reliable design. As expected, certain issues must be considered before designing a PCB layout using the LM5137-Q1. The high-frequency power loop of a buck regulator power stage is denoted by loop 1 in the shaded area of 図 8-25. The topological architecture of a buck regulator means that particularly high di/dt current flows in the components of loop 1, and reducing the parasitic inductance of this loop by minimizing the effective loop area becomes mandatory. Also important are the gate drive loops of the high-side and low-side MOSFETs, denoted by 2 and 3, respectively, in 図 8-25.

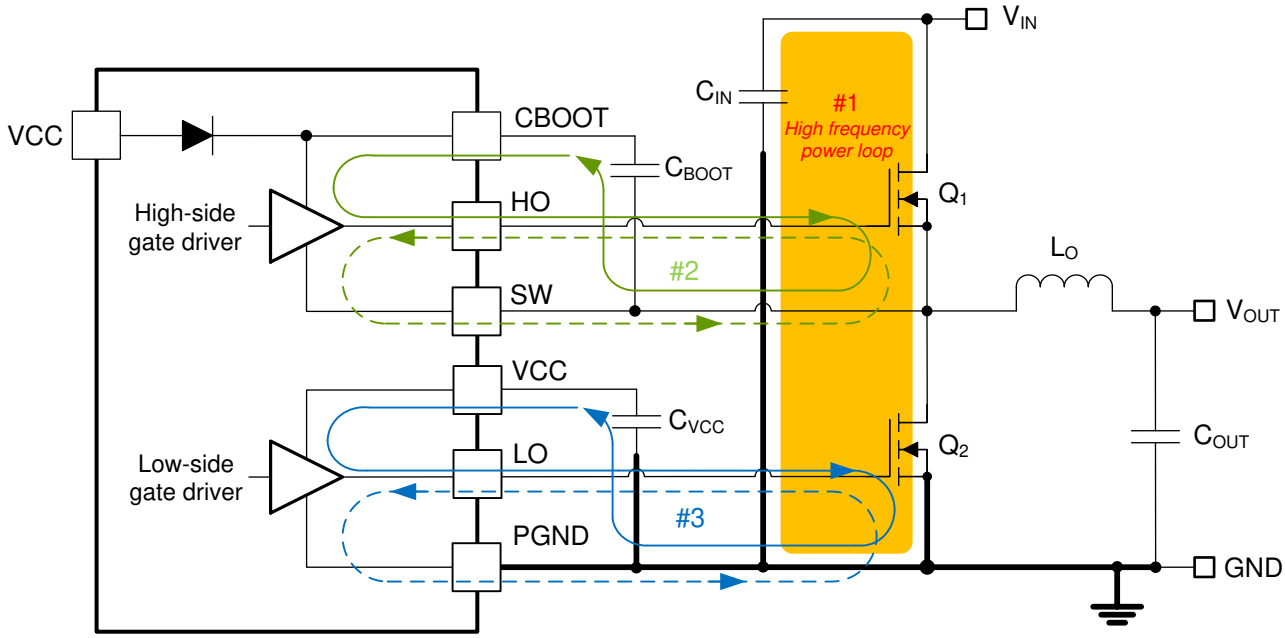

図 8-25. DC/DC Regulator Ground System With Power Stage and Gate Drive Circuit Switching Loops

8.4.1.1 Power Stage Layout

1. Input capacitors, output capacitors, and MOSFETs are the constituent components of the power stage of a buck regulator and are typically placed on the top side of the PCB (solder side). The benefits of convective heat transfer are maximized because of leveraging any system-level airflow. In a two-sided PCB layout, small-signal components are typically placed on the bottom side (component side). Insert at least one inner plane, connected to ground, to shield and isolate the small-signal traces from noisy power traces and lines.
2. The DC/DC regulator has several high-current loops. Minimize the area of these loops to suppress generated switching noise and optimize switching performance.
   - Loop 1: The most important loop area to minimize is the path from the input capacitor or capacitors through the high- and low-side MOSFETs, and back to the capacitor or capacitors through the ground connection. Connect the input capacitor or capacitors negative terminal close to the source of the low-side MOSFET (at ground). Similarly, connect the input capacitor or capacitors positive terminal close to the drain of the high-side MOSFET (at VIN). Refer to "loop 1" in 図 8-25.
   - Another loop, not as critical as loop 1, is the path from the low-side MOSFET through the inductor and output capacitor or capacitors, and back to source of the low-side MOSFET through ground. Connect the source of the low-side MOSFET and negative terminal of the output capacitor or capacitors at ground as close as possible.

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3. The PCB trace defined as SW node, which connects to the source of the high-side (control) MOSFET, the drain of the low-side (synchronous) MOSFET and the high-voltage side of the inductor, must be short and wide. However, the SW connection is a source of injected EMI and thus must not be too large.
4. Follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.
5. The SW pin connects to the switch node of the power conversion stage and acts as the return path for the high-side gate driver. The parasitic inductance inherent to loop 1 in 図 8-25 and the output capacitance (C_{OSS}) of both power MOSFETs form a resonant circuit that induces high frequency (greater than 50MHz) ringing at the SW node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. Make sure that the peak ringing amplitude does not exceed the absolute maximum rating limit for the SW pin. In many cases, a series resistor and capacitor snubber network connected from the SW node to GND damps the ringing and decreases the peak amplitude. Provide provisions for snubber network components in the PCB layout. If testing reveals that the ringing amplitude at the SW pin is excessive, then include snubber components as needed.

8.4.1.2 Gate Drive Layout

The LM5137-Q1 high-side and low-side gate drivers incorporate short propagation delays, adaptive deadtime control, and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turn-on and turnoff transitions of the power MOSFETs. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled.

Minimization of stray or parasitic gate loop inductance is key to optimizing gate drive switching performance, whether it be series gate inductance that resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) that provides a negative feedback component opposing the gate drive command, thereby increasing MOSFET switching times. The following loops are important:

- Loop 2: high-side MOSFET, Q_1. During the high-side MOSFET turn-on, high current flows from the bootstrap (boot) capacitor through the gate driver and high-side MOSFET, and back to the negative terminal of the boot capacitor through the SW connection. Conversely, to turn off the high-side MOSFET, high current flows from the gate of the high-side MOSFET through the gate driver and SW, and back to the source of the high-side MOSFET through the SW trace. Refer to "loop 2" of 図 8-25.
- Loop 3: low-side MOSFET, Q_2. During the low-side MOSFET turn-on, high current flows from the VCC decoupling capacitor through the gate driver and low-side MOSFET, and back to the negative terminal of the capacitor through ground. Conversely, to turn off the low-side MOSFET, high current flows from the gate of the low-side MOSFET through the gate driver and GND, and back to the source of the low-side MOSFET through ground. Refer to "loop 3" of 図 8-25.

TI strongly recommends following circuit layout guidelines when designing with high-speed MOSFET gate drive circuits.

- Connections from gate driver outputs, HO1/HO2 and LO1/LO2, to the respective gates of the high-side or low-side MOSFETs must be as short as possible to reduce series parasitic inductance. Be aware that peak gate drive currents can be as high as 3A. Use 0.65mm (25mils) or wider traces. Use via or vias, if necessary, of at least 0.5mm (20mils) diameter along these traces. Route the [HO1, SW1] and [HO2, SW2] gate traces as differential pairs from the LM5137-Q1 to the applicable high-side MOSFETs, taking advantage of flux cancellation.
- Minimize the current loop path from the VCC and CBOOT1/CBOOT2 pins through the respective capacitors as these provide the high instantaneous current, up to 3A, to charge the MOSFET gate capacitances. Specifically, locate the bootstrap capacitors, C_{BST1} and C_{BST2}, close to the respective [CBOOT1, SW1] and [CBOOT2, SW2] pin pairs of the LM5137-Q1 to minimize the areas of "loop 2" associated with the high-side drivers. Similarly, locate the VCC capacitor, C_{VCC}, close to the VCC and PGND pins of the LM5137-Q1 to minimize the areas of "loop 3" associated with the low-side drivers.

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8.4.1.3 PWM Controller Layout

With the proviso to locate the controller as close as possible to the power MOSFETs to minimize gate driver trace runs, the components related to the analog and feedback signals as well as current sensing are considered in the following:

1. Separate power and signal traces, and use a ground plane to provide noise shielding.
2. Place all sensitive analog traces and components related to COMP1/2, FB1/2, ISNS1/2+, RSS, and RT away from high-voltage switching nodes such as SW1/2, HO1/2, LO1/2 or CBOOT1/2 to avoid mutual coupling. Use internal layers as ground planes. Pay particular attention to shielding the feedback (FB) trace from power traces and components.
3. Locate the upper and lower feedback resistors (if required) close to the respective FB pins, keeping the FB traces as short as possible. Route the trace from the upper feedback resistors to the required output voltage sense points at the loads.
4. Route the [ISNS1+, BIAS1/VOUT1] and [ISNS2+, VOUT1/2] traces as differential pairs to minimize noise pickup and use Kelvin connections to the applicable shunt resistor (if shunt current sensing is used) or to the sense capacitor (if inductor DCR current sensing is used). In particular, use a wide trace for the connection to BIAS1/VOUT1, preferably *80mils* (2mm), to minimize the voltage drop related to bias current flowing to that pin.
5. Minimize the loop area from the VCC and VIN pins through the respective decoupling capacitors to the PGND pin. Locate these capacitors as close as possible to the LM5137-Q1.

8.4.1.4 Thermal Design and Layout

The useful operating temperature range of a PWM controller with integrated gate drivers and bias supply LDO regulator is greatly affected by the following:

- Average gate drive current requirements of the power MOSFETs
- Switching frequency
- Operating input voltage (affecting bias regulator LDO voltage drop and hence the power dissipation)
- Thermal characteristics of the package and operating environment

For a PWM controller to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The LM5137-Q1 controller is available in a small 6mm × 6mm 36-pin VQFNP (RHA) PowerPAD package to cover a range of application requirements. *Thermal Information* summarizes the thermal metrics of this package.

The 36-pin VQFNP package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. While the exposed pad of the package is not directly connected to any leads of the package, exposed pad of the package is thermally connected to the substrate of the LM5137-Q1 device (ground). This connection allows a significant improvement in heat sinking, and designing the PCB with thermal lands, thermal vias, and a ground plane to complete the heat removal subsystem is imperative. The exposed pad of the LM5137-Q1 is soldered to the ground-connected copper land on the PCB directly underneath the device package, reducing the thermal resistance to a very low value.

Numerous vias with a 0.3mm diameter connected from the thermal land to the internal and solder-side ground plane or planes are vital to help dissipation. In a multi-layer PCB design, a solid ground plane is typically placed on the PCB layer below the power components. Not only does this action provide a plane for the power stage currents to flow but this action also represents a thermally conductive path away from the heat generating devices.

The thermal characteristics of the MOSFETs also are significant. The drain pads of the high-side MOSFETs are normally connected to a VIN plane for heat sinking. The drain pads of the low-side MOSFETs are tied to the respective SW planes, but the SW plane area is purposely kept as small as possible to mitigate EMI concerns.

8.4.1.5 Ground Plane Design

As mentioned previously, TI recommends using one or more of the inner PCB layers as a solid ground plane. A ground plane offers shielding for sensitive circuits and traces and also provides a quiet reference potential for the control circuitry. Connect the PGND pin of the LM5137-Q1 to the system ground plane using an array of vias

ADVANCE INFORMATION

under the exposed pad. Also connect the PGND copper directly to the return terminals of the input and output capacitors. The PGND nets contain noise at the switching frequency and can bounce because of load current variations. The power traces (polygons) to the power-stage components for PGND, VIN and SW1/SW2 can be restricted to one side of the ground plane. The other side of the ground plane contains much less noise and is an excellent choice for sensitive analog trace routes.

8.4.2 Layout Example

Based on the *LM5137F-Q1-EVM5D3* design, 図 8-26 shows a single-sided layout of a dual-output synchronous buck regulator. The design uses layer 2 of the PCB as a power-loop ground return path directly underneath the top layer to create a low-area switching power loop of approximately 2mm². This loop area, and hence parasitic inductance, must be as small as possible to minimize switch-node voltage overshoot and ringing (and hence the overall EMI signature). Refer to the *LM25137F-Q1-EVM5D3 Evaluation Module* EVM user's guide for more detail.

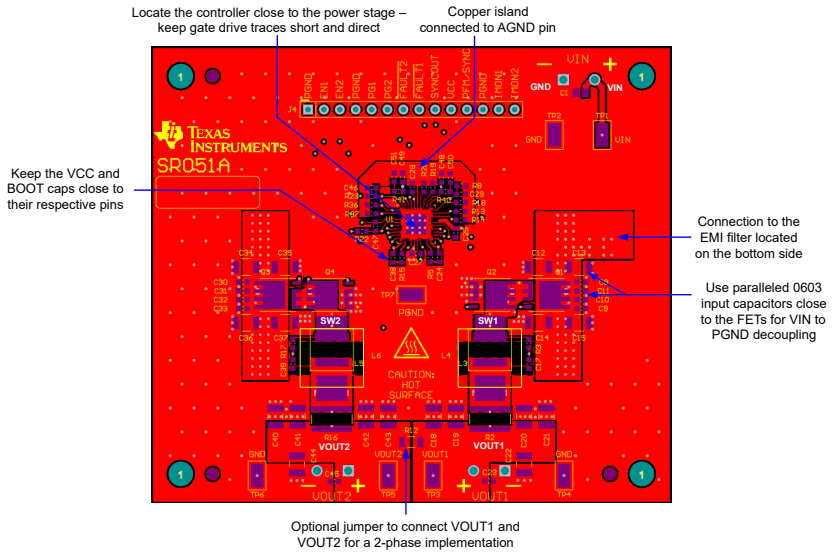

図 8-26. PCB Top Layer

As shown in 図 8-27, the high-frequency power loop current flows through MOSFETs Q3 and Q4, through the power ground plane on layer 2, and back to VIN through the 0603 ceramic capacitors C30 through C33. The currents flowing in opposing directions in the vertical loop configuration provide field self-cancellation, reducing parasitic loop inductance. 図 8-28 shows a side view to illustrate the concept of creating a low-profile, self-canceling loop in a multilayer PCB structure. The layer-2 GND plane layer, shown in 図 8-27, provides a tightly-coupled current return path directly under the MOSFETs to the source terminals of Q4.

Four 10nF input capacitors with small 0603 case size, place in parallel close to the drain of each high-side MOSFET. The low ESL and high self-resonant frequency (SRF) of the small footprint capacitors yield excellent high-frequency performance. The negative terminals of these capacitors connect to the layer-2 GND plane with multiple 12mil (0.3mm) diameter vias, further reducing parasitic inductance.

Additional steps used in this layout example include:

- Keep the SW connection from the power MOSFETs to the inductor (for each channel) at minimum copper area to reduce capacitive coupling and radiated EMI.
- Locate the IC close to the gate terminals of the MOSFETs and route the gate drive traces short and direct.
- Create an analog ground plane near the IC for sensitive analog components. Connect the AGND plane and the PGND power ground planes at a single point at the die attach pad (DAP) of the IC.

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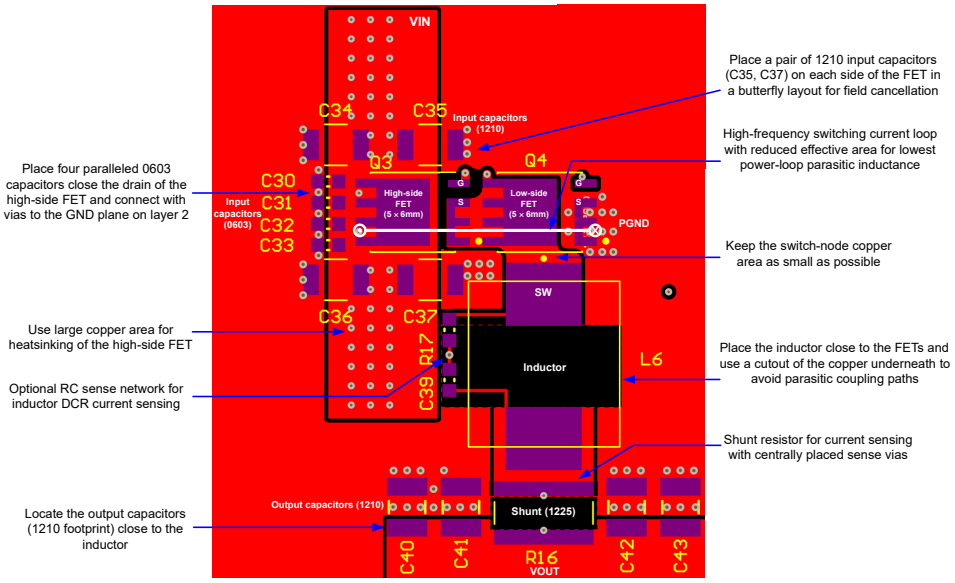
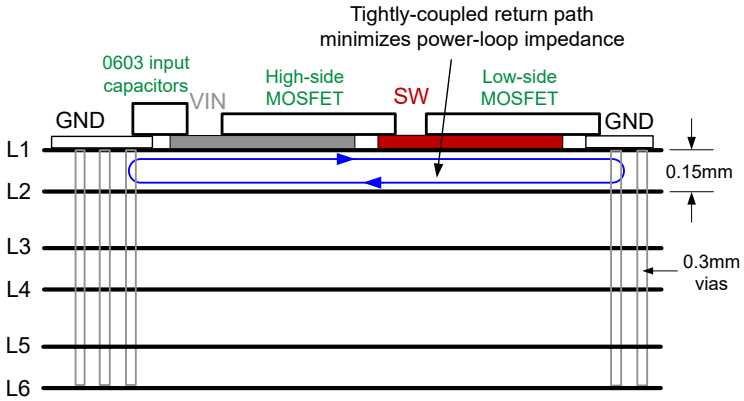


図 8-27. Power Stage Component Layout



注

See the *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout* application brief for more detail.

図 8-28. PCB Stack-Up Diagram With Low L1-L2 Intra-layer Spacing

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

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9.1.2 Development Support

With an input operating voltage as low as 3.5V and up to 100V as specified in 表 9-1, the LM(2)514x-Q1 family of automotive synchronous buck controllers from TI provides flexibility, scalability and optimized design size for a variety of applications.

With the LM5137-Q1 and LM25137-Q1 now available to aid in functional safety system design up to ASIL D, the controller family enables DC/DC designs with high density, low EMI, and increased system reliability. All controllers are rated for a maximum operating junction temperature of 150°C and have AEC-Q100 grade 1 qualification.

表 9-1. Automotive Synchronous Buck DC/DC Controller Family

DC/DC CONTROLLER	SINGLE or DUAL	V_{IN} RANGE	CONTROL METHOD	GATE DRIVE VOLTAGE	SYNC OUTPUT	PROGRAMMABLE SPREAD SPECTRUM
LM5137-Q1	Dual	4V to 80V	Peak current mode	5V	90° phase shift	DRSS (5% or 10%)
LM25137-Q1	Dual	4V to 42V	Peak current mode	5V	90° phase shift	DRSS (5% or 10%)
LM5140-Q1	Dual	3.8V to 65V	Peak current mode	5V	180° phase shift	N/A
LM5141-Q1	Single	3.8V to 65V	Peak current mode	5V	N/A	Triangular
LM25141-Q1	Single	3.8V to 42V	Peak current mode	5V	N/A	Triangular
LM5143A-Q1	Dual	3.5V to 65V	Peak current mode	5V	90° phase shift	Triangular
LM25143-Q1	Dual	3.5V to 42V	Peak current mode	5V	90° phase shift	Triangular
LM5145-Q1	Single	5.5V to 75V	Voltage mode	7.5V	180° phase shift	N/A
LM5146-Q1	Single	5.5V to 100V	Voltage mode	7.5V	180° phase shift	N/A
LM5148-Q1	Single	3.5V to 80V	Peak current mode	5V	180° phase shift	DRSS
LM25148-Q1	Single	3.5V to 42V	Peak current mode	5V	180° phase shift	DRSS
LM5149-Q1	Single	3.5V to 80V	Peak current mode	5V	180° phase shift	DRSS
LM25149-Q1	Single	3.5V to 42V	Peak current mode	5V	180° phase shift	DRSS

For development support, see the following:

- LM(2)5137-Q1 DC/DC controller *Quickstart Calculator* and PSPICE simulation models
- LM(2)5137-Q1 EVM PCB layout files
- For TI's WEBENCH design environments, visit the WEBENCH® Design Center
- For TI's reference design library, visit TI Designs
- TI Designs:
  - *Automotive Wide V_{IN} Front-end Reference Design for Digital Cockpit Processing Units*
- Technical articles:
  - *High-Density PCB Layout of DC/DC Converters*
  - *Synchronous Buck Controller Solutions Support Wide V_{IN} Performance and Flexibility*
  - *How to Use Slew Rate for EMI Control*

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5137-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.

ADVANCE INFORMATION

2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer gives a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- User's guides:
  - Texas Instruments, *LM25137-Q1 Synchronous Buck Controller EVM*
  - Texas Instruments, *LM5143-Q1 Synchronous Buck Controller EVM*
  - Texas Instruments, *LM5141-Q1 Synchronous Buck Controller EVM*
  - Texas Instruments, *LM5146-Q1 EVM User's Guide*
  - Texas Instruments, *LM5145EVM-HD-20A High Density Evaluation Module*
- Application reports:
  - Texas Instruments, *LM5143-Q1 4-phase Buck Regulator Design for Automotive ADAS Applications*
  - Texas Instruments, *AN-2162 Simple Success With Conducted EMI From DCDC Converters*
  - Texas Instruments, *Maintaining Output Voltage Regulation During Automotive Cold-Crank with LM5140-Q1 Dual Synchronous Buck Controller*
- Analog design journal:
  - Texas Instruments, *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics*
- White papers:
  - Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies*
  - Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies*
  - Texas Instruments, *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*

9.2.1.1 PCB Layout Resources

- Application reports:
  - Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies*
  - Texas Instruments, *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x*
- Application brief:
  - Texas Instruments, *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout*
- Seminar:
  - Texas Instruments, *Constructing Your Power Supply – Layout Considerations*

9.2.1.2 Thermal Design Resources

- Application reports:
  - Texas Instruments, *AN-2020 Thermal Design by Insight, Not Hindsight*
  - Texas Instruments, *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
  - Texas Instruments, *Semiconductor and IC Package Thermal Metrics*
  - Texas Instruments, *Thermal Design Made Simple with LM43603 and LM43602*
  - Texas Instruments, *PowerPAD™ Thermally Enhanced Package*

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- Texas Instruments, *PowerPAD Made Easy*
- Texas Instruments, *Using New Thermal Metrics*

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (August 2024) to Revision A (August 2024)	Page
• データシート全体に機能安全対応デバイスの情報を追加	1
• 最初のページの回路図を更新	1
• Updated the functional block diagram	15

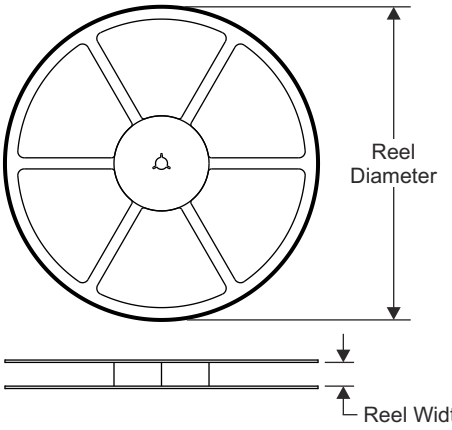
11 Mechanical, Packaging, and Orderable Information

The following pages show mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

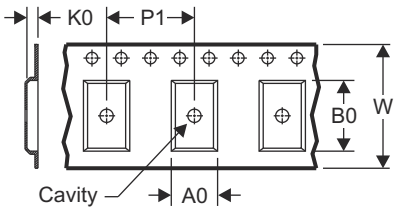
ADVANCE INFORMATION

11.1 Tape and Reel Information

REEL DIMENSIONS

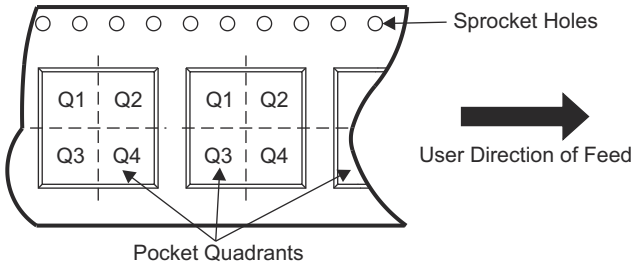


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
P5137QRHARQ1	VQFN	RHA	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q1

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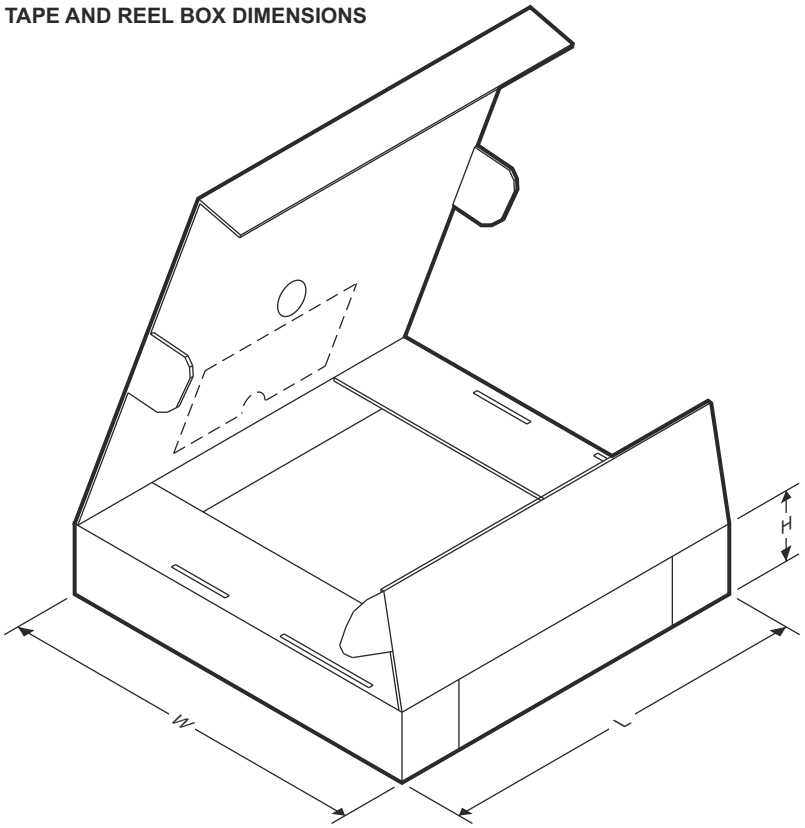
ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



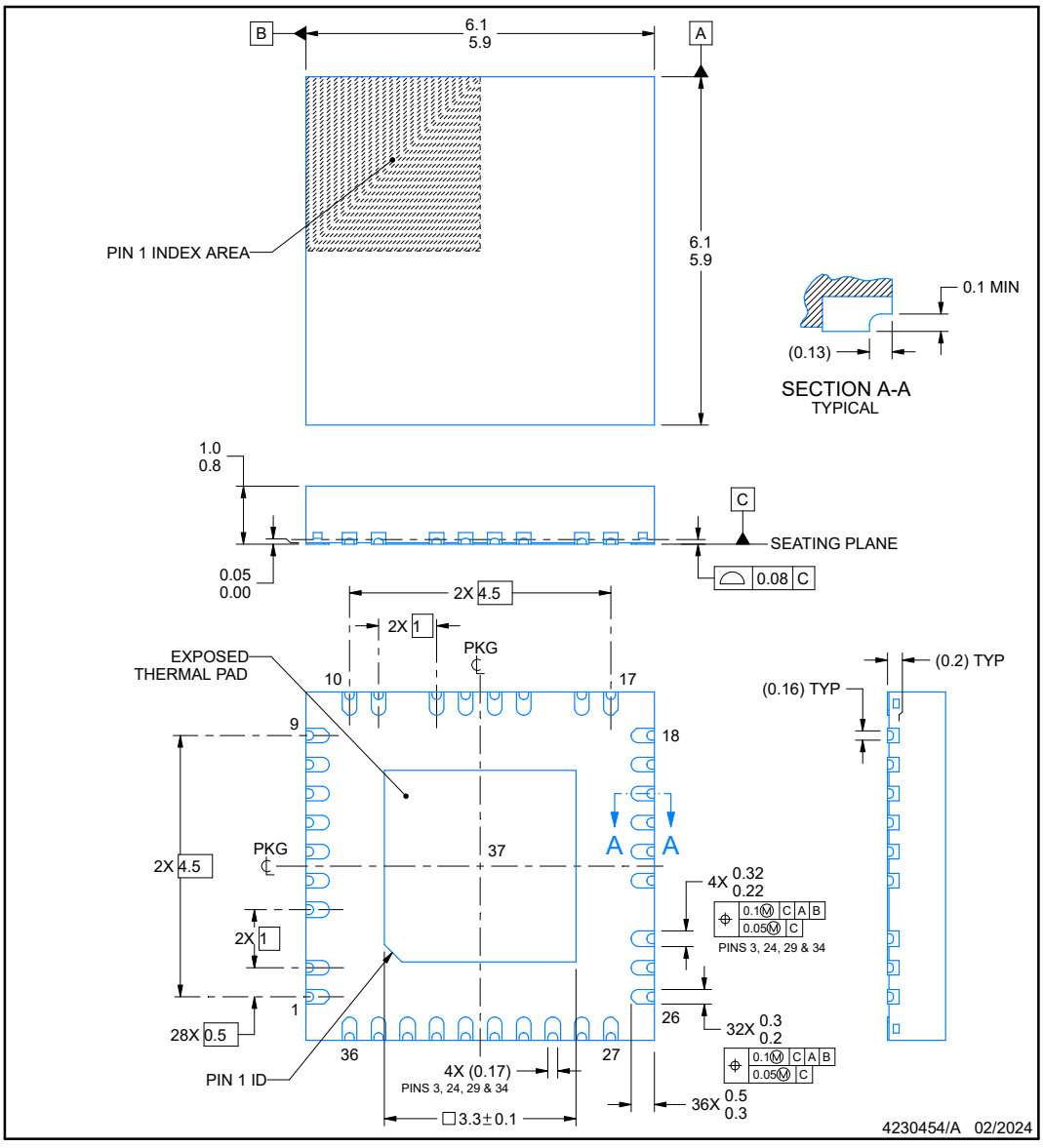
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
P5137QRHARQ1	VQFN	RHA	36	2500	367.0	367.0	35.0

PACKAGE OUTLINE

RHA0036D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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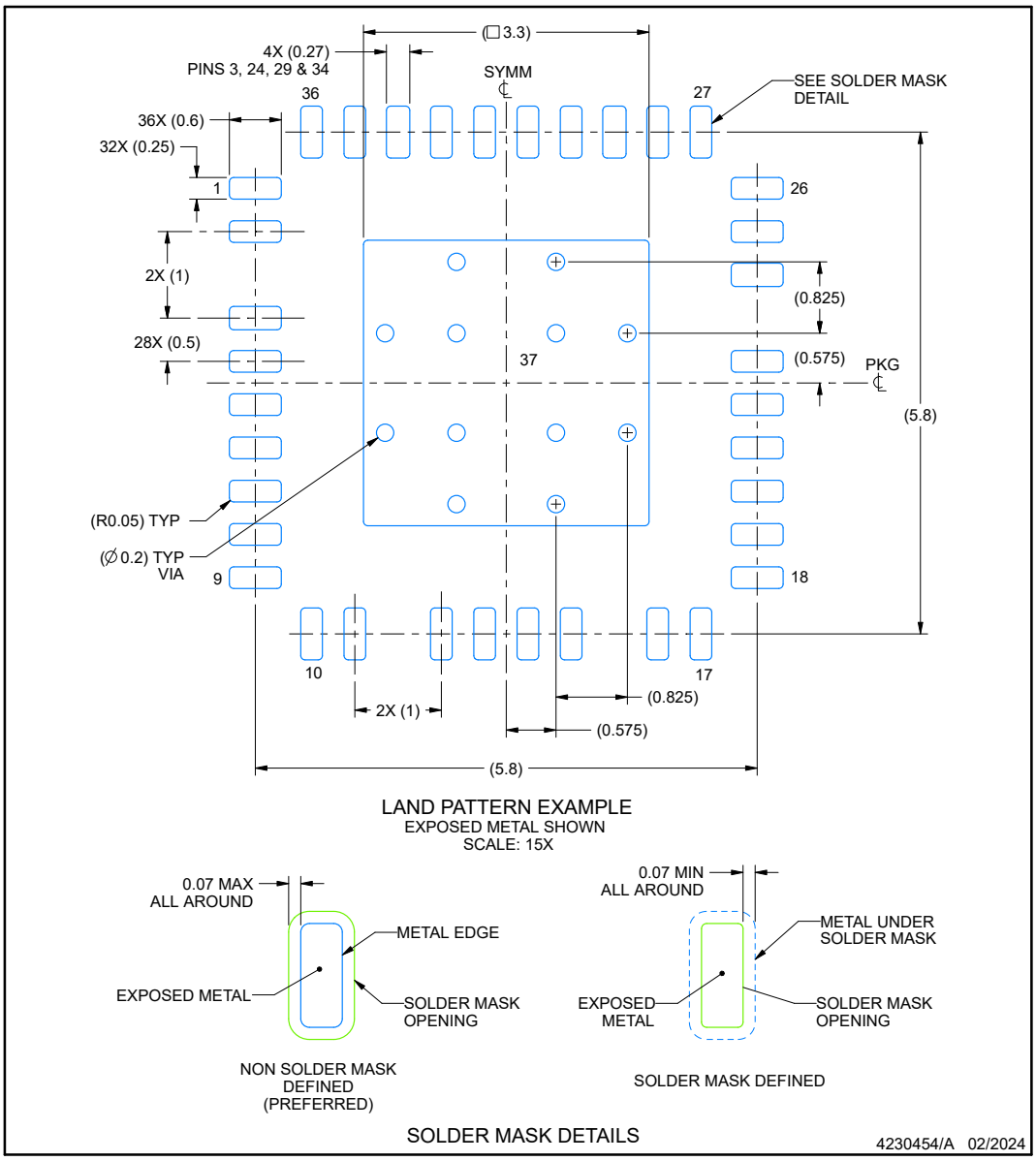
EXAMPLE BOARD LAYOUT

RHA0036D — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



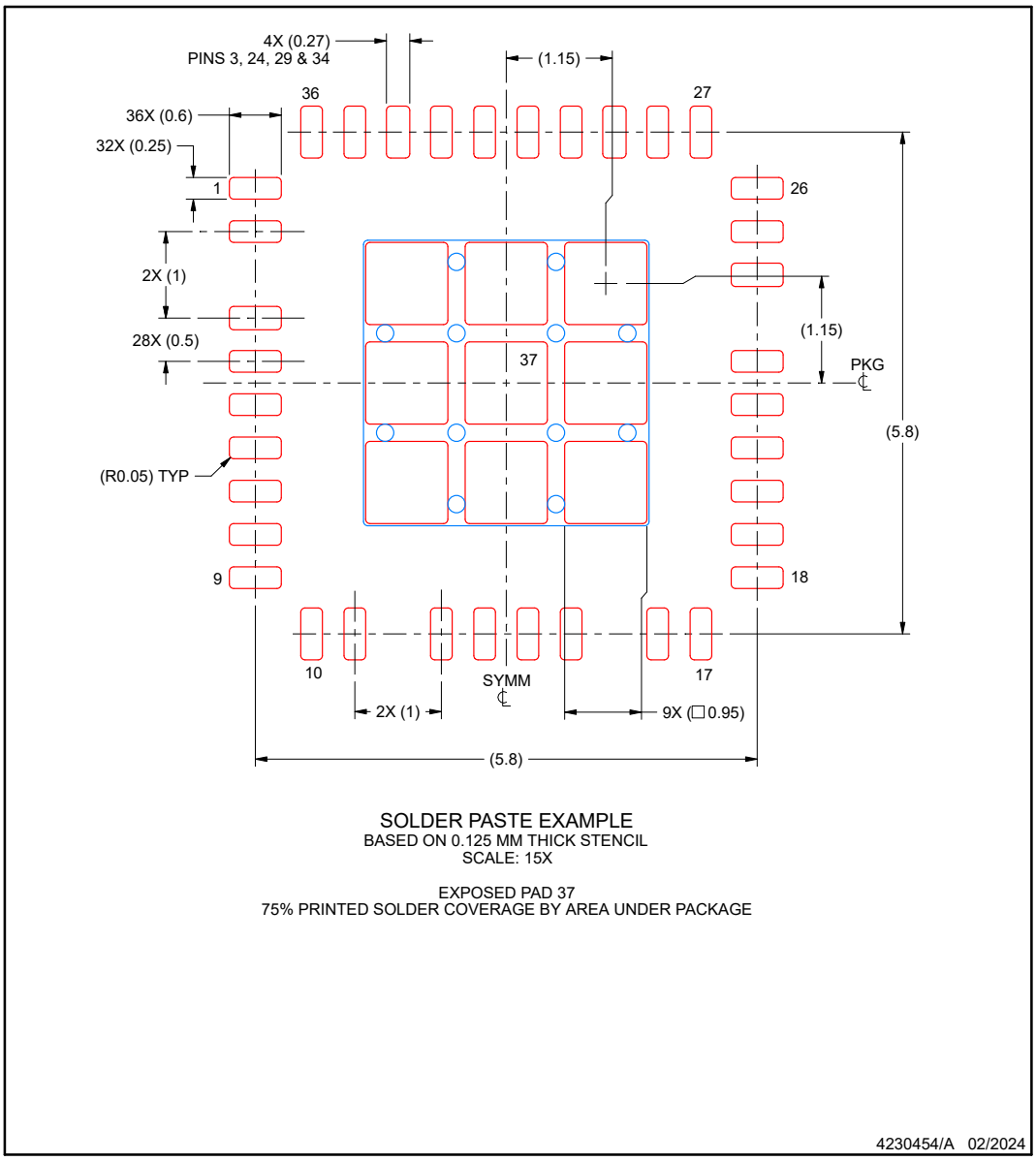
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHA0036D — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
P5137QRHARQ1	Active	Preproduction	VQFN (RHA) | 36	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 150	
P5137QRHARQ1.A	Active	Preproduction	VQFN (RHA) | 36	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

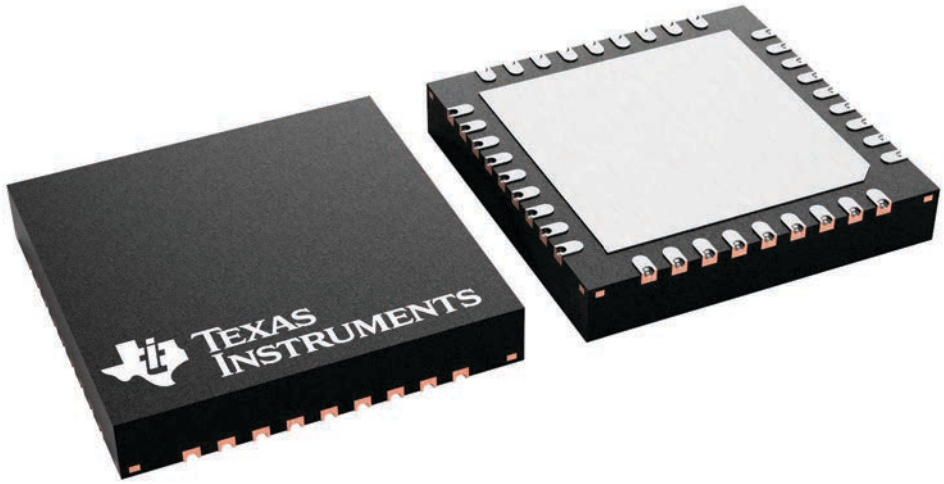
RHA 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



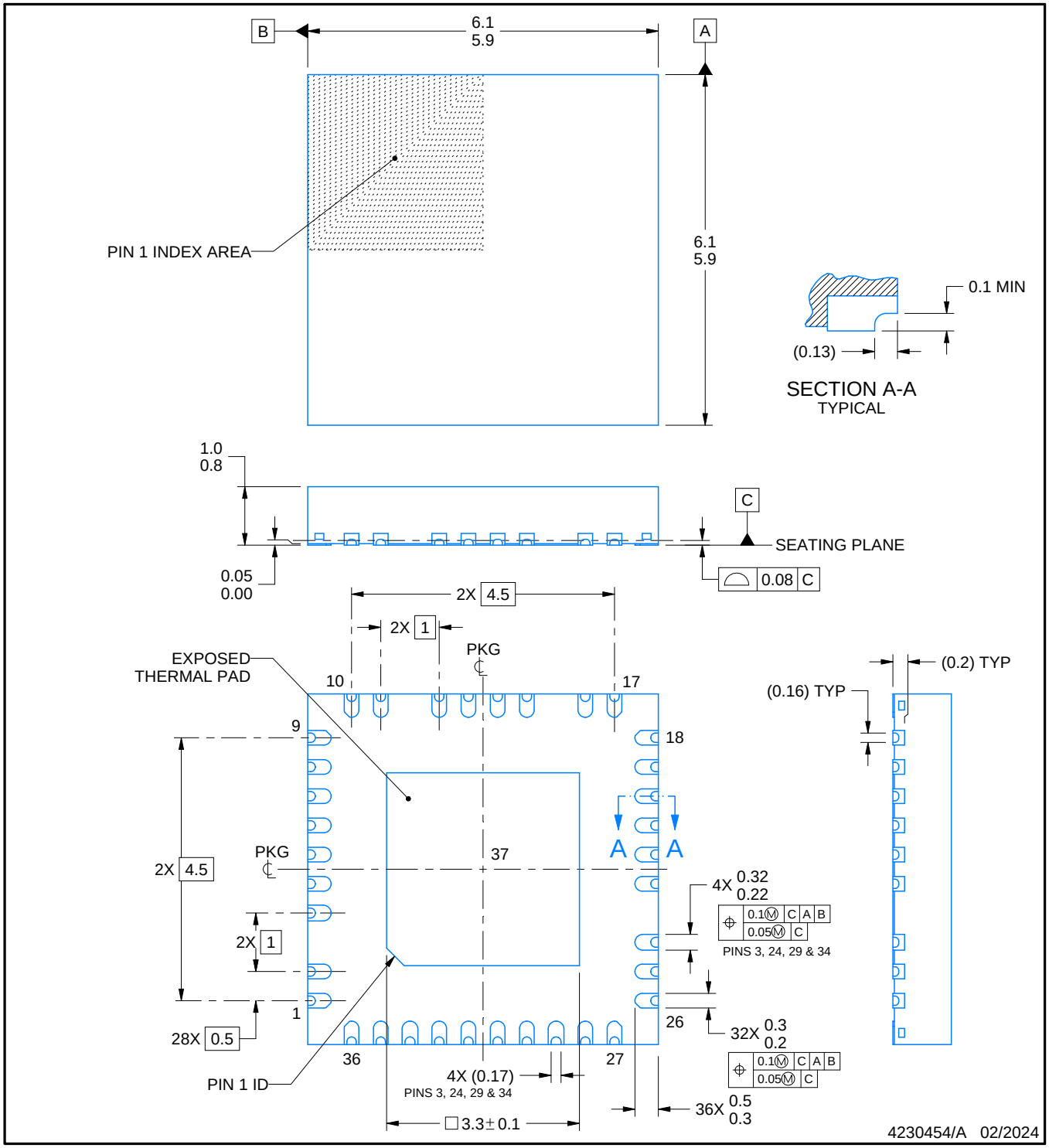
4228438/A

RHA0036D

PACKAGE OUTLINE

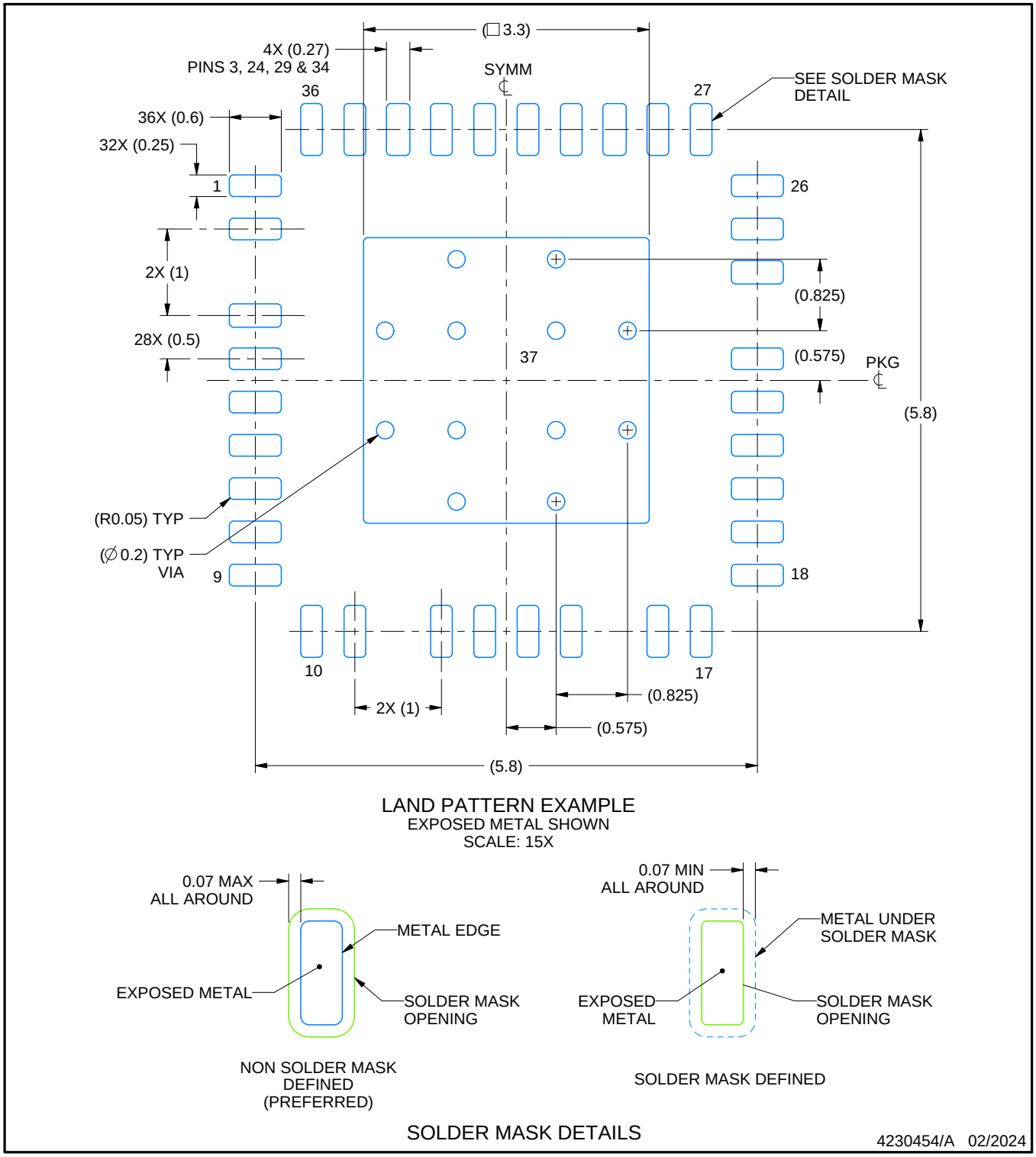
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



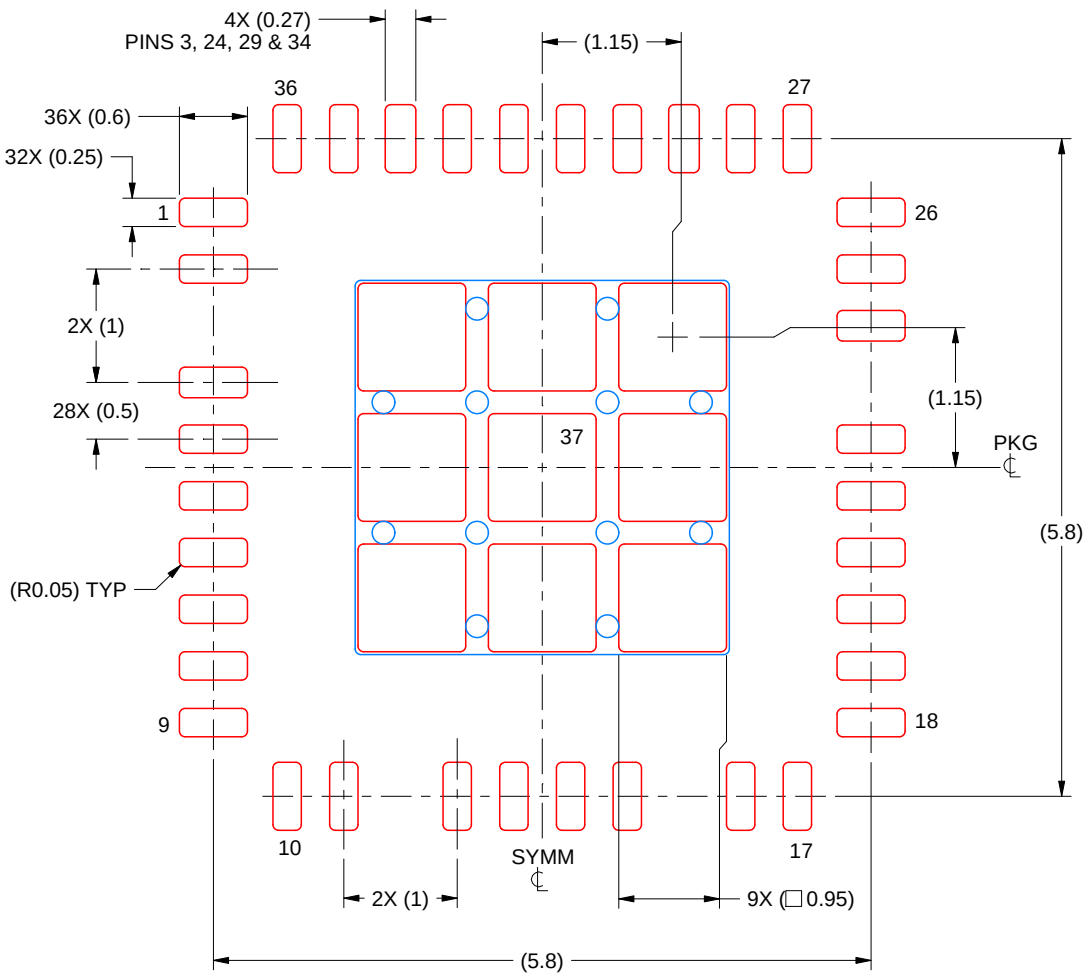
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4230454/A 02/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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