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#### LM5022

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# LM5022 60V、昇圧およびSEPIC用ローサイド・コントローラ

Technical

Documents

### 1 特長

- 内部的な60Vスタートアップ・レギュレータ
- 1AピークMOSFETゲート・ドライバ
- V<sub>IN</sub>範囲: 6V~60V (スタートアップ後に最低3V で動作)
- デューティ・サイクル制限90%
- プログラム可能でヒステリシス付きのUVLO
- サイクルごとの電流制限
- 外部同期可能(ACカップリング)
- 単一の抵抗による発振器周波数の設定
- スロープ補償
- 調整可能なソフト・スタート
- 10ピンのVSSOPパッケージ

### 2 アプリケーション

- 昇圧コンバータ
- SEPICコンバータ

### 3 概要

Tools &

Software

LM5022デバイスは、高電圧のローサイドNチャネル MOSFETコントローラで、昇圧およびSEPICレギュレータ に理想的です。シングル・エンドのプライマリ・トポロジを実 装するため必要なすべての機能が搭載されています。出 力電圧レギュレーションは電流モード制御を基礎としてい るため、ループ補償の設計が簡単になるとともに、入力電 圧のフィードフォワードが組み込まれています。LM5022 にはスタートアップ・レギュレータが搭載されており、6V~ 60Vの広い入力電圧範囲で動作します。PWMコントロー ラは高速動作用に設計されており、最高2.2MHzの発振 器周波数と、100ns未満の総伝搬遅延を実現していま す。追加機能として、エラー・アンプ、高精度の基準電圧、 ライン低電圧誤動作防止、サイクル単位の電流制限、勾 配補償、ソフトスタート、外部同期機能、サーマル・シャット ダウンがあります。LM5022は10ピンのVSSOPパッケージ で利用可能です。

#### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)			
LM5022	VSSOP (10)	3.00mm×3.00mm			

(1) 提供されているすべてのパッケージについては、巻末の注文情報 を参照してください。





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### 目次

8

9

11.5

1	特長	
2	アプ	リケーション 1
3	概要	
4	改訂	履歴2
5	Pin	Configuration and Functions
6	Spe	cifications 4
	6.1	Absolute Maximum Ratings 4
	6.2	ESD Ratings 4
	6.3	Recommended Operating Conditions 4
	6.4	Thermal Information 4
	6.5	Electrical Characteristics 5
	6.6	Typical Characteristics 7
7	Deta	ailed Description
	7.1	Overview
	7.2	Functional Block Diagram 9
	7.3	Feature Description 10
	7.4	Device Functional Modes 12

### 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Revision H (December 2016) から Revision I に変更

•	Changed 1 To: C2 in Equation 55	24

### Revision G (December 2013) から Revision H に変更

### 「ESD定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関 する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケー Changed slope compensation amplitude, V<sub>SLOPE</sub>, values From: 80 To: 83 (Minimum), From: 105 To: 110 (Typical), Page Revision F (March 2013) から Revision G に変更

•	Changed timing resistor equation. Incorrect change when converting to TI format	12

### Revision E (March 2013) から Revision F に変更

•	ナショナル・セミコンダクターのデータシートのレイアウトをTIフォーマットへ 変更	1
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Application and Implementation ..... 14 8.1 Application Information...... 14 8.2 Typical Application ..... 14 

10.1 Layout Guidelines ...... 29 10.2 Layout Examples...... 30 11 デバイスおよびドキュメントのサポート ...... 32 11.3 ドキュメントの更新通知を受け取る方法...... 32 11.4 コミュニティ・リソース...... 32 

11.6 静電気放電に関する注意事項 ...... 32 11.7 Glossary...... 32 

www.ti.com

Pa	g	e

Page

Page

2



#### LM5022 JAJSAO5I – JANUARY 2007 – REVISED DECEMBER 2017

### 5 Pin Configuration and Functions



### **Pin Functions**

PIN		PIN NO	DESCRIPTION	
NO.	NAME	1/0	DESCRIPTION	
1	VIN	I	Source input voltage: Input to the startup regulator. Operates from 6 V to 60 V.	
2	FB	Ι	Feedback pin: Inverting input to the internal voltage error amplifier. The noninverting input of the error amplifier connects to a 1.25-V reference.	
3	COMP	I/O	Error amplifier output and PWM comparator input: The control loop compensation components connect between this pin and the FB pin.	
4	VCC	0	Output of the internal, high-voltage linear regulator: This pin must be bypassed to the GND pin with a ceramic capacitor.	
5	OUT	0	Output of MOSFET gate driver: Connect this pin to the gate of the external MOSFET. The gate driver has a 1-A peak current capability.	
6	GND	—	System ground	
7	UVLO	I	Input undervoltage lockout: Set the start-up and shutdown levels by connecting this pin to the input voltage through a resistor divider. A 20-µA current source provides hysteresis.	
8	CS	I	Current sense input: Input for the switch current used for current mode control and for current limiting.	
9	RT/SYNC	I	Oscillator frequency adjust pin and synchronization input: An external resistor connected from this pin to GND sets the oscillator frequency. This pin can also accept an AC-coupled input for synchronization from an external clock.	
10	SS	I	Soft-start pin: An external capacitor placed from this pin to ground is charged by a 10-µA current source, creating a ramp voltage to control the regulator start-up.	

### 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

	MIN	MAX	UNIT
VIN to GND	-0.3	65	V
VCC to GND	-0.3	16	V
RT/SYNC to GND	-0.3	5.5	V
OUT to GND	−1.5 for < 100 ns		V
All other pins to GND	-0.3 7		V
Power dissipation	Internally limited		
Junction temperature, $T_J^{(3)}$	150		°C
Storage temperature, T <sub>stg</sub>	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)(2)</sup> Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(3)</sup>	±2000	V	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(3)</sup>	±750	v

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) The human-body model is a 100-pF capacitor discharged through a 1.5-k $\Omega$  resistor into each pin.

(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage	6	60	V
External voltage at V <sub>CC</sub>	7.5	14	V
Junction temperature	-40	125	°C

(1) Device thermal limitations may limit usable range

### 6.4 Thermal Information

		LM5022	
	THERMAL METRIC <sup>(1)</sup>	DGS (VSSOP)	UNIT
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	161.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	81.3	°C/W
ΨJT	Junction-to-top characterization parameter	5.7	°C/W
Ψјв	Junction-to-board characterization parameter	80	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	_	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

### 6.5 Electrical Characteristics

Typical limits apply for  $T_J=25^{\circ}$ C and are provided for reference purposes only; minimum and maximum limits apply over the junction temperature ( $T_J$ ) range of -40°C to 125°C.  $V_{IN} = 24$  V and  $R_T = 27.4$  k $\Omega$  (unless otherwise noted).<sup>(1)</sup>

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PARAMETERS						
V <sub>FB</sub>	FB pin voltage		1.225	1.25	1.275	V
STARTUP R	REGULATOR					
		$10 \text{ V} \leq \text{V}_{\text{IN}} \leq 60 \text{ V}, \text{ I}_{\text{CC}} = 1 \text{ mA}$	6.6	7	7.4	
VCC	VCC regulation <sup>(2)</sup>	6 V ≤ V <sub>IN</sub> < 10V, VCC Pin Open Circuit	5			V
I <sub>CC</sub>	Supply current	OUT Pin Capacitance = 0, VCC = 10 V		3.5	4	mA
I <sub>CC-LIM</sub>	VCC current limit	$VCC = 0 V^{(2)(3)}$	15	35		mA
V <sub>IN</sub> - VCC	Dropout voltage across bypass switch	$I_{\rm CC} = 0 \text{ mA}, f_{\rm SW} < 200 \text{ kHz}, \\ 6 \text{ V} \le \text{V}_{\rm IN} \le 8.5 \text{ V}$		200		mV
V <sub>BYP-HI</sub>	Bypass switch turnoff threshold	V <sub>IN</sub> increasing		8.7		V
V <sub>BYP-HYS</sub>	Bypass switch threshold hysteresis	V <sub>IN</sub> Decreasing		260		mV
Z <sub>VCC</sub>		$V_{IN} = 6 V$		58		
	VCC pin output impedance	V <sub>IN</sub> = 8 V		53		Ω
	$0 \text{ mA} \leq 100 \leq 5 \text{ mA}$	V <sub>IN</sub> = 24 V		1.6		
VCC-HI	VCC pin UVLO rising threshold			5		V
VCC-HYS	VCC pin UVLO falling hysteresis			300		mV
I <sub>VIN</sub>	Startup regulator leakage	V <sub>IN</sub> = 60 V		150	500	μA
I <sub>IN-SD</sub>	Shutdown current	V <sub>UVLO</sub> = 0 V, VCC = Open Circuit		350	450	μA
ERROR AM	PLIFIER					
GBW	Gain bandwidth			4		MHz
A <sub>DC</sub>	DC gain			75		dB
I <sub>COMP</sub>	COMP pin current sink capability	V <sub>FB</sub> = 1.5 V, V <sub>COMP</sub> = 1 V	5	17		mA
UVLO						
V <sub>SD</sub>	Shutdown threshold		1.22	1.25	1.28	V
I <sub>SD-HYS</sub>	Shutdown hysteresis current source		16	20	24	μA
CURRENT L	IMIT					
t <sub>LIM-DLY</sub>	Delay from ILIM to output	CS steps from 0 V to 0.6 V, OUT transitions to 90% of VCC		30		ns
V <sub>CS</sub>	Current limit threshold voltage		0.45	0.5	0.55	V
t <sub>BLK</sub>	Leading edge blanking time			65		ns
R <sub>CS</sub>	CS pin sink impedance	Blanking active		40	75	Ω
SOFT STAR	т					
I <sub>SS</sub>	Soft-start current source		7	10	13	μA
V <sub>SS-OFF</sub>	Soft start to COMP offset		0.35	0.55	0.75	V

(1) All Minimum and Maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control. The junction temperature (T<sub>J</sub> in °C) is calculated from the ambient temperature (T<sub>A</sub> in °C) and power dissipation (P<sub>D</sub> in Watts) as follows: T<sub>J</sub> = T<sub>A</sub> + (P<sub>D</sub> × R<sub>θJA</sub>) where R<sub>θJA</sub> (in °C/W) is the package thermal impedance provided in *Thermal Information*.

(2) VCC provides bias for the internal gate drive and control circuits.

(3) Device thermal limitations may limit usable range.

### **Electrical Characteristics (continued)**

Typical limits apply for  $T_J=25^{\circ}$ C and are provided for reference purposes only; minimum and maximum limits apply over the junction temperature ( $T_J$ ) range of -40°C to 125°C.  $V_{IN} = 24$  V and  $R_T = 27.4$  k $\Omega$  (unless otherwise noted).<sup>(1)</sup>

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
	RT to GND = 84.5 k $\Omega$		170 <sup>(4)</sup>	200	230	kHz
f <sub>SW</sub>	RT to GND = 27.4 k $\Omega$	See <sup>(4)</sup>	525	600	675	kHz
	RT to GND = 16.2 k $\Omega$	See <sup>(4)</sup>	865	990	1115	kHz
V <sub>SYNC-HI</sub>	Synchronization rising threshold				3.8	V
PWM COMPA	RATOR	•	•			
t <sub>COMP-DLY</sub>	Delay from COMP to OUT transition	$V_{COMP}$ = 2 V, CS stepped from 0 V to 0.4 V		25		ns
D <sub>MIN</sub>	Minimum duty cycle	V <sub>COMP</sub> = 0 V			0%	
D <sub>MAX</sub>	Maximum duty cycle		90%	95%		
A <sub>PWM</sub>	COMP to PWM comparator gain			0.33		V/V
V <sub>COMP-OC</sub>	COMP pin open circuit voltage	$V_{FB} = 0 V$	4.3	5.2	6.1	V
I <sub>COMP-SC</sub>	COMP pin short circuit current	$V_{COMP} = 0 V, V_{FB} = 1.5 V$	0.6	1.1	1.5	mA
SLOPE COMP	PENSATION					
V <sub>SLOPE</sub>	Slope compensation amplitude		83	110	137	mV
MOSFET DRI	/ER					
V <sub>SAT-HI</sub>	Output high saturation voltage (VCC - VOUT)	I <sub>OUT</sub> = 50 mA		0.25	0.75	V
V <sub>SAT-LO</sub>	Output low saturation voltage (VOUT)	I <sub>OUT</sub> = 100 mA		0.25	0.75	V
t <sub>RISE</sub>	OUT pin rise time	OUT Pin load = 1 nF		18		ns
t <sub>FALL</sub>	OUT pin fall time	OUT Pin load = 1 nF		15		ns
THERMAL CH	IARACTERISTICS					
T <sub>SD</sub>	Thermal shutdown threshold			165		°C
T <sub>SD-HYS</sub>	Thermal shutdown hysteresis			25		°C

(4) Specification applies to the oscillator frequency.



### 6.6 Typical Characteristics





### **Typical Characteristics (continued)**





### 7 Detailed Description

### 7.1 Overview

The LM5022 is a low-side, N-channel MOSFET controller that contains all of the features required to implement single-ended power converter topologies. The LM5022 includes a high-voltage start-up regulator that operates over a wide input range of 6 V to 60 V. The PWM controller is designed for high-speed capability including an oscillator frequency range up to 2.2 MHz and total propagation delays less than 100 ns. Additional features include an error amplifier, precision reference, input undervoltage lockout, cycle-by-cycle current limit, slope compensation, soft start, oscillator sync capability, and thermal shutdown.

The LM5022 is designed for current-mode control power converters that require a single drive output, such as boost and SEPIC topologies. The LM5022 provides all of the advantages of current-mode control including input voltage feedforward, cycle-by-cycle current limiting, and simplified loop compensation.

### 7.2 Functional Block Diagram



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### 7.3 Feature Description

### 7.3.1 High-Voltage Start-Up Regulator

The LM5022 contains an internal high-voltage start-up regulator that allows the VIN pin to be connected directly to line voltages as high as 60 V. The regulator output is internally current limited to 35 mA (typical). When power is applied, the regulator is enabled and sources current into an external capacitor,  $C_F$ , connected to the VCC pin. The recommended capacitance range for  $C_F$  is 0.1 µF to 100 µF. When the voltage on the VCC pin reaches the rising threshold of 5 V, the controller output is enabled. The controller remains enabled until VCC falls below 4.7 V. In applications using a transformer, an auxiliary winding can be connected through a diode to the VCC pin. This winding must raise the VCC pin voltage to above 7.5 V to shut off the internal start-up regulator. Powering VCC from an auxiliary winding improves conversion efficiency while reducing the power dissipated in the controller. The capacitance of  $C_F$  must be high enough that it maintains the VCC voltage greater than the VCC UVLO falling threshold (4.7 V) during the initial start-up. During a fault condition when the converter auxiliary winding is inactive, external current draw on the VCC line must be limited such that the power dissipated in the start-up regulator does not exceed the maximum power dissipation capability of the controller.

An external start-up or other bias rail can be used instead of the internal start-up regulator by connecting the VCC and the VIN pins together and feeding the external bias voltage (7.5 V to 14 V) to the two pins.

### 7.3.2 Input Undervoltage Detector

The LM5022 contains an input undervoltage lockout (UVLO) circuit. UVLO is programmed by connecting the UVLO pin to the center point of an external voltage divider from VIN to GND. The resistor divider must be designed such that the voltage at the UVLO pin is greater than 1.25 V when  $V_{IN}$  is in the desired operating range. If the undervoltage threshold is not met, all functions of the controller are disabled and the controller remains in a low power standby state. UVLO hysteresis is accomplished with an internal 20-µA current source that is switched on or off into the impedance of the setpoint divider. When the UVLO threshold is exceeded, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.25-V threshold the current source is turned off, causing the voltage at the UVLO pin to fall. The UVLO pin can also be used to implement a remote enable or disable function. If an external transistor pulls the UVLO pin below the 1.25-V threshold, the converter is disabled. This external shutdown method is shown in Figure 11.



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Figure 11. Enable or Disable Using UVLO



### **Feature Description (continued)**

### 7.3.3 Error Amplifier

An internal high gain error amplifier is provided within the LM5022. The amplifier's noninverting input is internally set to a fixed reference voltage of 1.25 V. The inverting input is connected to the FB pin. In non-isolated applications such as the boost converter the output voltage,  $V_0$ , is connected to the FB pin through a resistor divider. The control loop compensation components are connected between the COMP and FB pins. For most isolated applications, the error amplifier function is implemented on the secondary side of the converter and the internal error amplifier is not used. The internal error amplifier is configured as an open-drain output and can be disabled by connecting the FB pin to ground. An internal 5-k $\Omega$  pullup resistor between a 5-V reference and COMP can be used as the pullup for an opto-coupler in isolated applications.

### 7.3.4 Current Sensing and Current Limiting

The LM5022 provides a cycle-by-cycle over current protection function. Current limit is accomplished by an internal current sense comparator. If the voltage at the current sense comparator input exceeds 0.5 V, the MOSFET gate drive is immediately terminated. A small RC filter, placed near the controller, is recommended to filter noise from the current sense signal. The CS input has an internal MOSFET which discharges the CS pin capacitance at the conclusion of every cycle. The discharge device remains on an additional 65 ns after the beginning of the new cycle to attenuate leading edge ringing on the current sense signal.

The LM5022 current sense and PWM comparators are very fast, and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the pins of the controller (CS and GND). If a current sense transformer is used, both leads of the transformer secondary must be routed to the sense resistor and the current sense filter network. The current sense resistor can be placed between the source of the primary power MOSFET and power ground, but it must be a low inductance type. When designing with a current sense resistor all of the noise sensitive low-power ground connections must be connected together locally to the controller and a single connection must be made to the high current power ground (sense resistor ground point).

#### 7.3.5 PWM Comparator and Slope Compensation

The PWM comparator compares the current ramp signal with the error voltage derived from the error amplifier output. The error amplifier output voltage at the COMP pin is offset by 1.4 V and then further attenuated by a 3:1 resistor divider. The PWM comparator polarity is such that 0 V on the COMP pin results in a zero duty cycle at the controller output. For duty cycles greater than 50%, current mode control circuits can experience subharmonic oscillation. By adding an additional fixed-slope voltage ramp signal (slope compensation) this oscillation can be avoided. Proper slope compensation damps the double pole associated with current mode control (see *Control Loop Compensation*) and eases the design of the control loop compensator. The LM5022 generates the slope compensation with a sawtooth-waveform current source with a slope of 45  $\mu$ A ×  $f_{SW}$ , generated by the clock (see Figure 12). This current flows through an internal 2-k $\Omega$  resistor to create a minimum compensation ramp with a slope of 100 mV ×  $f_{SW}$  (typical). The slope of the compensation ramp increases when external resistance is added for filtering the current sense (R<sub>S1</sub>) or in the position R<sub>S2</sub>. As shown in Figure 12 and the *Functional Block Diagram*, the sensed current slope and the compensation slope add together to create the signal used for current limiting and for the control loop itself.

### Feature Description (continued)



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Figure 12. Slope Compensation

In peak current mode control, the optimal slope compensation is proportional to the slope of the inductor current during the power switch off-time. For boost converters, the inductor current slope while the MOSFET is off is  $(V_O - V_{IN}) / L$ . This relationship is combined with the requirements to set the peak current limit and is used to select  $R_{SNS}$  and  $R_{S2}$  in *Application and Implementation*.

### 7.3.6 Soft Start

The soft-start feature allows the power converter output to gradually reach the initial steady-state output voltage, thereby reducing start-up stresses and current surges. At power on, after the VCC and input undervoltage lockout thresholds are satisfied, an internal 10-µA current source charges an external capacitor connected to the SS pin. The capacitor voltage ramps up slowly and limits the COMP pin voltage and the switch current.

### 7.3.7 MOSFET Gate Driver

The LM5022 provides an internal gate driver through the OUT pin that can source and sink a peak current of 1 A to control external, ground-referenced N-channel MOSFETs.

### 7.3.8 Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the LM5022 in the event that the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power standby state, disabling the output driver and the VCC regulator. After the temperature is reduced (typical hysteresis is 25°C) the VCC regulator is re-enabled and the LM5022 performs a soft start.

### 7.4 Device Functional Modes

#### 7.4.1 Oscillator, Shutdown, and SYNC

A single external resistor,  $R_T$ , connected between the RT/SYNC and GND pins sets the LM5022 oscillator frequency. To set the switching frequency ( $f_{SW}$ ),  $R_T$  can be calculated with Equation 1.

$$R_{T} = \frac{\left(1 - 8 \times 10^{-8} \times f_{SW}\right)}{f_{SW} \times 5.77 \times 10^{-11}}$$

where

- f<sub>SW</sub> is in Hz
- $R_T$  is in  $\Omega$

(1)



### **Device Functional Modes (continued)**

The LM5022 can also be synchronized to an external clock. The external clock must have a higher frequency than the free-running oscillator frequency set by the  $R_T$  resistor. The clock signal must be capacitively coupled into the RT/SYNC pin with a 100-pF capacitor as shown in Figure 13. A peak voltage level greater than 3.8 V at the RT/SYNC pin is required for detection of the sync pulse. The sync pulse width must be set between 15 ns to 150 ns by the external components. The  $R_T$  resistor is always required, whether the oscillator is free-running or externally synchronized. The voltage at the RT/SYNC pin is internally regulated to 2 V, and the typical delay from a logic high at the RT/SYNC pin to the rise of the OUT pin voltage is 120 ns.  $R_T$  must be placed very close to the device and connected directly to the pins of the controller (RT/SYNC and GND).



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Figure 13. SYNC Operation

### 8 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The most common circuit controlled by the LM5022 is a non-isolated boost regulator. The boost regulator steps up the input voltage and has a duty ratio D in Equation 2.

$$\mathsf{D} = \frac{\mathsf{V}_{\mathsf{O}} - \mathsf{V}_{\mathsf{IN}} + \mathsf{V}_{\mathsf{D}}}{\mathsf{V}_{\mathsf{O}} + \mathsf{V}_{\mathsf{D}}}$$

where

V<sub>D</sub> is the forward voltage drop of the output diode

The following is a design procedure for selecting all the components for the boost converter circuit shown in Figure 14. The application is *in-cabin* automotive, meaning that the operating ambient temperature ranges from  $-20^{\circ}$ C to  $85^{\circ}$ C. This circuit operates in continuous conduction mode (CCM), where inductor current stays above 0 A at all times, and delivers an output voltage of 40 V  $\pm 2\%$  at a maximum output current of 0.5 A. Additionally, the regulator must be able to handle a load transient of up to 0.5 A while keeping V<sub>O</sub> within  $\pm 4\%$ . The voltage input comes from the battery or alternator system of an automobile, where the standard range of 9 V to 16 V and transients of up to 32 V must not cause any malfunction.

### 8.2 Typical Application



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Figure 14. LM5022 Typical Application

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(2)

### **Typical Application (continued)**

### 8.2.1 Design Requirements

For typical low-side controller applications, use the parameters listed in Table 1.

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DESIGN PARAMETER	EXAMPLE VALUE						
Input voltage range	9 V to 16 V						
Output voltage	40 V						
Maximum output current	500 mA						
Switching frequency	500 kHz						

### **Table 1. Design Parameters**

### 8.2.2 Detailed Design Procedure

Table 2 lists the bill of materials for this design example.

ID	PART NUMBER	TYPE	SIZE	PARAMETERS	QTY	VENDOR
U1	LM5022	Low-Side Controller	10-pin VSSOP	60 V	1	TI
Q1	Si4850EY	MOSFET	SO-8	60 V, 31 mΩ, 27 nC	1	Vishay
D1	CMSH2-60M	Schottky Diode	SMA	60 V, 2 A	1	Central Semi
L1	SLF12575T-M3R2	Inductor	12.5 × 12.5 × 7.5 mm	33 $\mu\text{H},$ 3.2 A, 40 m $\Omega$	1	TDK
Cin1, Cin2	C4532X7R1H475M	Capacitor	1812	4.7 $\mu\text{F},$ 50 V, 3 m $\Omega$	2	TDK
Co1, Co2	C5750X7R2A475M	Capacitor	2220	4.7 $\mu$ F,100 V, 3 m $\Omega$	2	TDK
Cf	C2012X7R1E105K	Capacitor	0805	1 µF, 25 V	1	TDK
Cinx Cox	C2012X7R2A104M	Capacitor	0805	100 nF, 100 V	2	TDK
C1	VJ0805A561KXXAT	Capacitor	0805	560 pF 10%	1	Vishay
C2	VJ0805Y124KXXAT	Capacitor	0805	120 nF 10%	1	Vishay
Css	VJ0805Y103KXXAT	Capacitor	0805	10 nF 10%	1	Vishay
Ccs	VJ0805Y102KXXAT	Capacitor	0805	1 nF 10%	1	Vishay
R1	CRCW08053011F	Resistor	0805	3.01 kΩ 1%	1	Vishay
Rfb1	CRCW08056490F	Resistor	0805	649 Ω 1%	1	Vishay
Rfb2	CRCW08052002F	Resistor	0805	20 kΩ 1%	1	Vishay
Rs1	CRCW0805101J	Resistor	0805	100 Ω 5%	1	Vishay
Rs2	CRCW08053571F	Resistor	0805	3.57 kΩ 1%	1	Vishay
Rsns	ERJL14KF10C	Resistor	1210	100 mΩ, 1%, 0.5 W	1	Panasonic
Rt	CRCW08053322F	Resistor	0805	33.2 kΩ 1%	1	Vishay
Ruv1	CRCW08052611F	Resistor	0805	2.61 kΩ 1%	1	Vishay
Ruv2	CRCW08051002F	Resistor	0805	10 kΩ 1%	1	Vishay

### Table 2. BOM for Example Circuit

### 8.2.2.1 Switching Frequency

The selection of switching frequency is based on the tradeoffs between size, cost, and efficiency. In general, a lower frequency means larger, more expensive inductors and capacitors is required. A higher switching frequency generally results in a smaller but less efficient solution, as the power MOSFET gate capacitances must be charged and discharged more often in a given amount of time. For this application, a frequency of 500 kHz was selected as a good compromise between the size of the inductor and efficiency. PCB area and component height are restricted in this application. Following Equation 1, a 33.2-k $\Omega$  1% resistor must be used to switch at 500 kHz.

### 8.2.2.2 MOSFET

Selection of the power MOSFET is governed by tradeoffs between cost, size, and efficiency. Breaking down the losses in the MOSFET is one way to determine relative efficiencies between different devices. For this example, the SO 8-pin package provides a balance of a small footprint with good efficiency (see Q1 in Table 2).

Losses in the MOSFET can be broken down into conduction loss, gate charging loss, and switching loss.

Conduction, or  $I^2R$  loss (P<sub>c</sub>) is approximately Equation 3.

П

$$P_{c} = D \times \left[ \left( \frac{I_{O}}{1 - D} \right) \times R_{DSON} \times 1.3 \right]$$
(3)

The factor 1.3 accounts for the increase in MOSFET on-resistance due to heating. Alternatively, the factor of 1.3 can be ignored and the maximum on-resistance of the MOSFET can be used.

Gate charging loss, P<sub>G</sub>, results from the current required to charge and discharge the gate capacitance of the power MOSFET and is approximated with Equation 4.

$$P_{G} = VCC \times Q_{G} \times f_{SW}$$
<sup>(4)</sup>

Q<sub>G</sub> is the total gate charge of the MOSFET. Gate charge loss differs from conduction and switching losses because the actual dissipation occurs in the LM5022 and not in the MOSFET itself. If no external bias is applied to the VCC pin, additional loss in the LM5022 IC occurs as the MOSFET driving current flows through the VCC regulator. This loss ( $P_{VCC}$ ) is estimated with Equation 5.

$$\mathsf{P}_{\mathsf{VCC}} = (\mathsf{V}_{\mathsf{IN}} - \mathsf{VCC}) \times \mathsf{Q}_{\mathsf{G}} \times \mathsf{f}_{\mathsf{SW}}$$

Switching loss (PSW) occurs during the brief transition period as the MOSFET turns on and off. During the transition period both current and voltage are present in the channel of the MOSFET. The loss can be approximated with Equation 6.

$$\mathsf{P}_{\mathsf{SW}} = 0.5 \times \mathsf{V}_{\mathsf{IN}} \times [\mathsf{I}_{\mathsf{O}} \,/\, (\mathsf{1} - \mathsf{D})] \times (\mathsf{t}_{\mathsf{R}} + \mathsf{t}_{\mathsf{F}}) \times f_{\mathsf{SW}}$$

where

- $t_R$  is the rise time of the MOSFET
- $t_{F}$  is the fall time of the MOSFET

For this example, the maximum drain-to-source voltage applied across the MOSFET is V<sub>o</sub> plus the ringing due to parasitic inductance and capacitance. The maximum drive voltage at the gate of the high-side MOSFET is VCC, or 7 V typical. The MOSFET selected must be able to withstand 40 V plus any ringing from drain to source, and be able to handle at least 7 V plus ringing from gate to source. A minimum voltage rating of 50-V<sub>D-S</sub> and 10-V<sub>G-S</sub> MOSFET is used. Comparing the losses in a spreadsheet leads to a 60 V<sub>D-S</sub> rated MOSFET in SO-8 with an  $R_{DSON}$  of 22 m $\Omega$  (the maximum value is 31 m $\Omega$ ), a gate charge of 27 nC, and rise and falls times of 10 ns and 12 ns, respectively.

#### 8.2.2.3 Output Diode

16

The boost regulator requires an output diode D1 (see Figure 14) to carrying the inductor current during the MOSFET off-time. The most efficient choice for D1 is a Schottky diode due to low forward drop and near-zero reverse recovery time. D1 must be rated to handle the maximum output voltage plus any switching node ringing when the MOSFET is on. In practice, all switching converters have some ringing at the switching node due to the diode parasitic capacitance and the lead inductance. D1 must also be rated to handle the average output current, l<sub>0</sub>.

The overall converter efficiency becomes more dependent on the selection of D1 at low duty cycles, where the boost diode carries the load current for an increasing percentage of the time. This power dissipation can be calculating by checking the typical diode forward voltage, V<sub>D</sub>, from the I-V curve on the diode's data sheet and then multiplying it by Io. Diode data sheets also provides a typical junction-to-ambient thermal resistance, R<sub>0JA</sub>, which can be used to estimate the operating die temperature of the Schottky. Multiplying the power dissipation  $(P_D = I_O \times V_D)$  by  $R_{\theta JA}$  gives the temperature rise. The diode case size can then be selected to maintain the Schottky diode temperature below the operational maximum.

(5)

(6)



In this example a Schottky diode rated to 60 V and 1 A is suitable, as the maximum diode current is 0.5 A. A small case such as SOD-123 can be used if a small footprint is critical. Larger case sizes generally have lower  $R_{\theta JA}$  and lower forward voltage drop, so for better efficiency the larger SMA case size is used.

#### 8.2.2.4 Boost Inductor

The first criterion for selecting an inductor is the inductance itself. In fixed-frequency boost converters this value is based on the desired peak-to-peak ripple current,  $\Delta i_L$ , which flows in the inductor along with the average inductor current,  $I_L$ . For a boost converter in CCM  $I_L$  is greater than the average output current,  $I_O$ . The two currents are related by Equation 7.

$$I_{\rm L} = I_{\rm O} / (1 - {\rm D})$$
 (7)

As with switching frequency, the inductance used is a tradeoff between size and cost. Larger inductance means lower input ripple current, however because the inductor is connected to the output during the off-time only there is a limit to the reduction in output ripple voltage. Lower inductance results in smaller, less expensive magnetics. An inductance that gives a ripple current of 30% to 50% of  $I_L$  is a good starting point for a CCM boost converter. Minimum inductance must be calculated with Equation 8 at the extremes of input voltage to find the operating condition with the highest requirement.

$$L_{1} = \frac{V_{IN} \times D}{f_{SW} \times \Delta i_{L}}$$
(8)

By calculating in terms of amperes, volts, and megahertz, the inductance value comes out in micro henries.

To ensure that the boost regulator operates in CCM a second equation is required, and must also be evaluated with Equation 9 at the corners of input voltage to find the minimum inductance required.

$$L_2 = \frac{D(1-D) \times V_{IN}}{I_O \times f_{SW}}$$
(9)

By calculating in terms of volts, amps, and megahertz, the inductance value comes out in µH.

For this design,  $\Delta i_L$  is set to 40% of the maximum  $I_L$ . Duty cycle is evaluated first at  $V_{IN(MIN)}$  and at  $V_{IN(MAX)}$ . Second, the average inductor current is evaluated at the two input voltages. Third, the inductor ripple current is determined. Finally, the inductance can be calculated, and a standard inductor value selected that meets all the criteria.

1. Inductance for Minimum Input Voltage (Equation 10, Equation 11, and Equation 12)

$$D_{VIN(MIN)} = (40 - 9 + 0.5) / (40 + 0.5) = 78\% I_{L-VIN(MIN)} = 0.5 / (1 - 0.78) = 2.3 \text{ A} \Delta i_L = 0.4 \times 2.3 \text{ A} = 0.92 \text{ A}$$
(10)

$$L_{1-\text{VIN}(\text{MIN})} = \frac{9 \times 0.78}{0.5 \times 0.92} = 15.3 \ \mu\text{H}$$
(11)

$$L_{2-\text{VIN}(\text{MIN})} = \frac{0.78 \times 0.22 \times 9}{0.5 \times 0.5} = 6.2 \ \mu\text{H}$$
(12)

2. Inductance for Maximum Input Voltage (Equation 13, Equation 14, and Equation 15)

$$D_{VIN(MAX)} = (40 - 16 + 0.5) / (40 + 0.5) = 60\% I_{L-VIN(MIAX)} = 0.5 / (1 - 0.6) = 1.25 A \Delta i_L = 0.4 \times 1.25 A = 0.5 A$$
(13)

$$L_{1-\text{VIN}(\text{MIN})} = \frac{16 \times 0.6}{0.5 \times 0.5} = 38.4 \ \mu\text{H}$$
(14)

$$L_{2 - \text{VIN}(\text{MIN})} = \frac{0.6 \times 0.4 \times 16}{0.5 \times 0.5} = 15.4 \ \mu\text{H}$$
(15)

Maximum average inductor current occurs at V<sub>IN(MIN)</sub>, and the corresponding inductor ripple current is 0.92 A<sub>P-P</sub>. Selecting an inductance that exceeds the ripple current requirement at V<sub>IN(MIN)</sub> and the requirement to stay in CCM for V<sub>IN(MAX)</sub> provides a tradeoff that allows smaller magnetics at the cost of higher ripple current at maximum input voltage. For this example, a 33-µH inductor satisfies these requirements.

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LM5022 JAJSAO5I – JANUARY 2007 – REVISED DECEMBER 2017

The second criterion for selecting an inductor is the peak current carrying capability. This is the level above which the inductor saturates. In saturation, the inductance can drop off severely, resulting in higher peak current that may overheat the inductor or push the converter into current limit. In a boost converter, peak current,  $I_{PK}$ , is equal to the maximum average inductor current plus one half of the ripple current. First, the current ripple must be determined under the conditions that give maximum average inductor current with Equation 16.

$$\Delta i_{L} = \frac{V_{IN} \times D}{f_{SW} \times L}$$
(16)

Maximum average inductor current occurs at V<sub>IN(MIN)</sub>. Using the selected inductance of 33 µH yields Equation 17.

$$\Delta i_{I} = (9 \times 0.78) / (0.5 \times 33) = 425 \text{ mA}_{P,P}$$

The highest peak inductor current over all operating conditions is therefore Equation 18.

 $I_{PK} = I_L + 0.5 \times \Delta i_L = 2.3 + 0.213 = 2.51 \text{ A}$ 

Hence an inductor must be selected that has a peak current rating greater than 2.5 A and an average current rating greater than 2.3 A. One possibility is an off-the-shelf 33  $\mu$ H ±20% inductor that can handle a peak current of 3.2 A and an average current of 3.4 A. Finally, the inductor current ripple is recalculated with Equation 19 at the maximum input voltage.

 $\Delta i_{L-VIN(MAX)} = (16 \times 0.6) / (0.5 \times 33) = 0.58 A_{P-P}$ 

### 8.2.2.5 Output Capacitor

The output capacitor in a boost regulator supplies current to the load during the MOSFET on-time and also filters the AC portion of the load current during the off-time. This capacitor determines the steady-state output voltage ripple,  $\Delta V_0$ , a critical parameter for all voltage regulators. Output capacitors are selected based on their capacitance,  $C_0$ , their equivalent series resistance (ESR) and their RMS or AC current rating.

The magnitude of  $\Delta V_O$  is comprised of three parts, and in steady-state the ripple voltage during the on-time is equal to the ripple voltage during the off-time. For simplicity the analysis is performed for the MOSFET turning off (off-time) only. The first part of the ripple voltage is the surge created as the output diode D1 turns on. At this point, inductor and diode current are at peak value, and the ripple voltage increase can be calculated with Equation 20.

$$\Delta V_{O1} = I_{PK} \times ESR \tag{20}$$

The second portion of the ripple voltage is the increase due to the charging of  $C_0$  through the output diode. This portion can be approximated with Equation 21.

$$\Delta V_{O2} = (I_O / C_O) \times (D / f_{SW})$$
(21)

The final portion of the ripple voltage is a decrease due to the flow of the diode and inductor current through the ESR of the output capacitor. This decrease can be calculated with Equation 22.

$$\Delta V_{O3} = \Delta i_{L} \times ESR \tag{22}$$

The total change in output voltage is Equation 23.

$$\Delta V_{\rm O} = \Delta V_{\rm O1} + \Delta V_{\rm O2} - \Delta V_{\rm O3} \tag{23}$$

The combination of two positive terms and one negative term may yield an output voltage ripple with a net rise or a net fall during the converter off-time. The ESR of the output capacitor(s) has a strong influence on the slope and direction of  $\Delta V_0$ . Capacitors with high ESR such as tantalum and aluminum electrolytic create an output voltage ripple that is dominated by  $\Delta V_{01}$  and  $\Delta V_{03}$ , with a shape shown in Figure 15. Ceramic capacitors, in contrast, have very low ESR and lower capacitance. The shape of the output ripple voltage is dominated by  $\Delta V_{02}$ , with a shape shown in Figure 16.

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(19)

(17)

(18)







Figure 15.  $\Delta V_0$  Using High-ESR Capacitors

Figure 16.  $\Delta V_0$  Using Low-ESR Capacitors

For this example the small size and high temperature rating of ceramic capacitors make them a good choice. The output ripple voltage waveform of Figure 16 is assumed, and the capacitance is selected first. The desired  $\Delta V_O$  is ±2% of 40 V, or 0.8 V<sub>P-P</sub>. Beginning with the calculation for  $\Delta V_{O2}$ , the required minimum capacitance is in Equation 24.

$$C_{\text{O-MIN}} = (I_{\text{O}} / \Delta V_{\text{O}}) \times (D_{\text{MAX}} / f_{\text{SW}}) C_{\text{O-MIN}} = (0.5 / 0.8) \times (0.77 / 5 \times 10^5) = 0.96 \,\mu\text{F}$$
(24)

The next higher standard 20% capacitor value is 1  $\mu$ F, however to provide margin for component tolerance and load transients two capacitors rated 4.7  $\mu$ F each (C<sub>O</sub>= 9.4  $\mu$ F) is used. Ceramic capacitors rated 4.7  $\mu$ F ±20% are available from many manufacturers. The minimum quality dielectric that is suitable for switching power supply output capacitors is X5R, while X7R (or better) is preferred. Pay careful attention to the DC voltage rating and case size, as ceramic capacitors can lose 60% or more of their rated capacitance at the maximum DC voltage. This is the reason that ceramic capacitors are often de-rated to 50% of their capacitance at their working voltage. The output capacitors for this example has a 100-V rating in a 2220 case size.

The typical ESR of the selected capacitors is 3 m $\Omega$  each, and in parallel is approximately 1.5 m $\Omega$ . The worstcase value for  $\Delta V_{O1}$  occurs during the peak current at minimum input voltage in Equation 25.

$$\Delta V_{01} = 2.5 \times 0.0015 = 4 \text{ mV}$$
(25)

The worst-case capacitor charging ripple occurs at maximum duty cycle in Equation 26.

$$\Delta V_{O2} = (0.5 / 9.4 \times 10^{-6}) \times (0.77 / 5 \times 10^{5}) = 82 \text{ mV}$$
<sup>(26)</sup>

Finally, the worst-case value for  $\Delta V_{O3}$  occurs when inductor ripple current is highest, at maximum input voltage in Equation 27.

$$\Delta V_{O3} = 0.58 \times 0.0015 = 1 \text{ mV} \text{ (negligible)}$$
 (27)

The output voltage ripple can be estimated by summing the three terms in Equation 28.

 $\Delta V_{O} = 4 \text{ mV} + 82 \text{ mV} - 1 \text{ mV} = 85 \text{ mV}$ 

The RMS current through the output capacitor(s) can be estimated using the following, worst-case equation in Equation 29.

$$I_{O-RMS} = 1.13 \times I_L \times \sqrt{D} \times (1-D)$$
<sup>(29)</sup>

The highest RMS current occurs at minimum input voltage. For this example the maximum output capacitor RMS current is calculated with Equation 30.

$$I_{O-RMS(MAX)} = 1.13 \times 2.3 \times (0.78 \times 0.22)^{0.5} = 1.08 A_{RMS}$$
(30)

These 2220 case size devices are capable of sustaining RMS currents of over 3 A each, making them more than adequate for this application.

(28)

#### LM5022 JAJSAO5I – JANUARY 2007 – REVISED DECEMBER 2017

### 8.2.2.6 VCC Decoupling Capacitor

The VCC pin must be decoupled with a ceramic capacitor placed as close as possible to the VCC and GND pins of the LM5022. The decoupling capacitor must have a minimum X5R or X7R type dielectric to ensure that the capacitance remains stable over voltage and temperature, and be rated to a minimum of 470 nF. One good choice is a  $1-\mu$ F device with X7R dielectric and 1206 case size rated to 25 V.

#### 8.2.2.7 Input Capacitor

The input capacitors to a boost regulator control the input voltage ripple ( $\Delta V_{IN}$ ) hold up the input voltage during load transients and prevent impedance mismatch (also called power supply interaction) between the LM5022 and the inductance of the input leads. Selection of input capacitors is based on their capacitance, ESR, and RMS current rating. The minimum value of ESR can be selected based on the maximum output current transient,  $I_{STEP}$ , using Equation 31.

$$\mathsf{ESR}_{\mathsf{MIN}} = \frac{(1-\mathsf{D}) \times \Delta \mathsf{V}_{\mathsf{IN}}}{2 \mathsf{x} \mathsf{I}_{\mathsf{STEP}}}$$
(31)

For this example, the maximum load step is equal to the load current or 0.5 A. The maximum permissable  $\Delta V_{IN}$  during load transients is  $4\%_{P-P}$ .  $\Delta V_{IN}$  and duty cycle are taken at minimum input voltage to give the worst-case value in Equation 32.

$$\text{ESR}_{\text{MIN}} = [(1 - 0.77) \times 0.36] / (2 \times 0.5) = 83 \text{ m}\Omega$$

The minimum input capacitance can be selected based on  $\Delta V_{IN}$ , based on the drop in  $V_{IN}$  during a load transient, or based on prevention of power supply interaction. In general, the requirement for greatest capacitance comes from the power supply interaction. The inductance and resistance of the input source must be estimated, and if this information is not available, they can be assumed to be 1  $\mu$ H and 0.1  $\Omega$ , respectively. Minimum capacitance is then estimated with Equation 33.

$$C_{MIN} = \frac{2 \times L_{S} \times V_{O} \times I_{O}}{V_{IN}^{2} \times R_{S}}$$
(33)

As with ESR, the worst-case, highest minimum capacitance calculation comes at the minimum input voltage. Using the default estimates for  $L_S$  and  $R_S$ , minimum capacitance is calculated with Equation 34.

$$C_{MIN} = \frac{2 \times 1\mu \times 40 \times 0.5}{9^2 \times 0.1} = 4.9 \ \mu F$$
(34)

The next highest standard 20% capacitor value is 6.8  $\mu$ F, but because the actual input source impedance and resistance are not known, two 4.7- $\mu$ F capacitors is used. In general, doubling the calculated value of input capacitance provides a good safety margin. The final calculation is for the RMS current. For boost converters operating in CCM this can be estimated with Equation 35.

$$I_{\rm RMS} = 0.29 \times \Delta I_{\rm L(MAX)} \tag{35}$$

From the inductor section, maximum inductor ripple current is 0.58 A, hence the input capacitor(s) must be rated to handle  $0.29 \times 0.58 = 170 \text{ mA}_{\text{RMS}}$ .

The input capacitors can be ceramic, tantalum, aluminum, or almost any type, however the low capacitance requirement makes ceramic capacitors particularly attractive. As with the output capacitors, the minimum quality dielectric used must X5R, with X7R or better preferred. The voltage rating for input capacitors requirement not be as conservative as the output capacitors, as the requirement for capacitance decreases as input voltage increases. For this example, the capacitor selected is 4.7  $\mu$ F ±20%, rated to 50 V in the 1812 case size. The RMS current rating of these capacitors is over 2 A each, more than enough for this application.

#### 8.2.2.8 Current Sense Filter

Parasitic circuit capacitance, inductance and gate drive current create a spike in the current sense voltage at the point where Q1 turns on. To prevent this spike from terminating the on-time prematurely, every circuit must have a low-pass filter that consists of  $C_{CS}$  and  $R_{S1}$ , shown in Figure 14. The time constant of this filter must be long enough to reduce the parasitic spike without significantly affecting the shape of the actual current sense voltage. The recommended range for  $R_{S1}$  is between 10  $\Omega$  and 500  $\Omega$ , and the recommended range for  $C_{CS}$  is between 100 pF and 2.2 nF. For this example, the values of  $R_{S1}$  and  $C_{CS}$  is 100  $\Omega$  and 1 nF, respectively.



(32)



### LM5022 JAJSAO5I – JANUARY 2007–REVISED DECEMBER 2017

### 8.2.2.9 R<sub>SNS</sub>, R<sub>S2</sub> and Current Limit

The current sensing resistor  $R_{SNS}$  is used for steady-state regulation of the inductor current and to sense overcurrent conditions. The slope compensation resistor is used to ensure control loop stability, and both resistors affect the current limit threshold. The  $R_{SNS}$  value selected must be low enough to keep the power dissipation to a minimum, yet high enough to provide good signal-to-noise ratio for the current sensing circuitry.  $R_{SNS}$ , and  $R_{S2}$  must be set so that the current limit comparator, with a threshold of 0.5 V, trips before the sensed current exceeds the peak current rating of the inductor, without limiting the output power in steady state.

For this example the peak current, at V<sub>IN(MIN)</sub>, is 2.5 A, while the inductor itself is rated to 3.2 A. The threshold for current limit, I<sub>LIM</sub>, is set slightly between these two values to account for tolerance of the circuit components, at a level of 3 A. The required resistor calculation must take both the switch current through R<sub>SNS</sub> and the compensation ramp current flowing through the internal 2 k $\Omega$ , R<sub>S1</sub> and R<sub>S2</sub> resistors into account. R<sub>SNS</sub> must be selected first because it is a power resistor with more limited selection. Equation 36 and Equation 37 must be evaluated at V<sub>IN(MIN)</sub>, when duty cycle is highest.

$$R_{SNS} = \frac{L \times f_{SW} \times V_{CL}}{\left(V_{O} - V_{IN}\right) \times 3 \times D + L \times f_{SW} \times I_{LIM}}$$

$$R_{SNS} = \frac{33 \times 0.5 \times 0.5}{\left(40 - 9\right) \times 3 \times 0.78 + 33 \times 0.5 \times 3}$$
(36)

where

The closest 5% value is 100 m $\Omega$ . Power dissipation in R<sub>SNS</sub> can be estimated by calculating the average current. The worst-case average current through R<sub>SNS</sub> occurs at minimum input voltage/maximum duty cycle and can be calculated with Equation 38 and Equation 39.

$$P_{CS} = \left[ \left( \frac{I_0}{1 - D} \right)^2 \times R_{SNS} \right] \times D$$
(38)
$$P_{CS} = \left[ (0.5 / 0.22)^2 \times 0.1 \right] \times 0.78 = 0.4 \text{ W}$$
(39)

For this example, a 0.1  $\Omega$  ±1%, thick-film chip resistor in a 1210 case size rated to 0.5 W is used.

With R<sub>SNS</sub> selected, R<sub>S2</sub> can be determined using Equation 40 and Equation 41.

$$R_{S2} = \frac{V_{CL} - I_{ILIM} \times R_{SNS}}{45\mu \times D} - 2000 - R_{S1}$$
(40)

$$R_{S2} = \frac{0.5 - 3 \times 0.1}{45\mu \times 0.78} - 2000 - 100 = 3598\Omega$$
(41)

The closest 1% tolerance value is 3.57 k $\Omega$ .

#### 8.2.2.10 Control Loop Compensation

The LM5022 uses peak current-mode PWM control to correct changes in output voltage due to line and load transients. Peak current-mode provides inherent cycle-by-cycle current limiting, improved line transient response, and easier control loop compensation.

The control loop is comprised of two parts. The first is the power stage, which consists of the pulse width modulator, output filter, and the load. The second part is the error amplifier, which is an op-amp configured as an inverting amplifier. Figure 17 shows the regulator control loop components.





Figure 17. Power Stage and Error Amplifier

One popular method for selecting the compensation components is to create Bode plots of gain and phase for the power stage and error amplifier. Combined, they make the overall bandwidth and phase margin of the regulator easy to determine. Software tools such as Excel, MathCAD, and Matlab are useful for observing how changes in compensation or the power stage affect system gain and phase.

The power stage in a CCM peak current mode boost converter consists of the DC gain,  $A_{PS}$ , a single low-frequency pole,  $f_{LFP}$ , the ESR zero,  $f_{ZESR}$ , a right-half plane zero,  $f_{RHP}$ , and a double pole resulting from the sampling of the peak current. The power stage transfer function (also called the control-to-output transfer function) can be written with Equation 42, Equation 43, and Equation 44.

$$G_{PS} = A_{PS} \times \frac{\left(1 + \frac{s}{\omega_{ZESR}}\right) \left(1 - \frac{s}{\omega_{RHP}}\right)}{\left(1 + \frac{s}{\omega_{LEP}}\right) \left(1 + \frac{s}{Q_n \times \omega_n} + \frac{s^2}{\omega_n^2}\right)}$$

where

• the DC gain is defined as:

$$A_{PS} = \frac{(1 - D) \times R_{C}}{2 \times R_{SNS}}$$

where

$$R_0 = V_0 / I_0$$

(42)

(43) (44)



The system ESR zero is calculated with Equation 45.

$$\omega_{ZESR} = \frac{1}{R_{C} \times C_{O}}$$
(45)

The low-frequency pole is calculated with Equation 46.

$$\omega_{\text{LEP}} = \frac{1}{0.5 \times (R_{\text{O}} + \text{ESR}) \times C_{\text{O}}}$$
(46)

The right-half plane zero is calculated with Equation 47.

$$\omega_{\text{RHP}} = \frac{R_{\text{O}} \times \left(\frac{V_{\text{IN}}}{V_{\text{O}}}\right)^2}{L}$$
(47)

The sampling double-pole quality factor is calculated with Equation 48.

$$Q_{n} = \frac{1}{\pi \left[ -D + 0.5 + (1 - D) \frac{S_{e}}{S_{n}} \right]}$$
(48)

The sampling double corner frequency is calculated with Equation 49.

 $\omega_{\rm n} = \pi \times f_{\rm SW} \tag{49}$ 

The natural inductor current slope is calculated with Equation 50.

$$S_{n} = R_{SNS} \times V_{IN} / L$$
(50)

The external ramp slope is calculated with Equation 51.

$$S_{e} = 45 \,\mu A \times (2000 + R_{S1} + R_{S2})] \times f_{SW}$$
(51)

In Equation 43, DC gain is highest when input voltage and output current are at the maximum. In this the example those conditions are  $V_{IN} = 16$  V and  $I_O = 500$  mA.

DC gain is 44 dB. The low-frequency pole  $f_P = \omega_P/2\pi$  is at 423 Hz, the ESR zero  $f_Z = \omega_Z/2\pi$  is at 5.6 MHz, and the right-half plane zero  $f_{RHP} = \omega_{RHP}/2\pi$  is at 61 kHz. The sampling double-pole occurs at one-half of the switching frequency. Proper selection of slope compensation (through  $R_{S2}$ ) is most evident the sampling double pole. A well-selected  $R_{S2}$  value eliminates peaking in the gain and reduces the rate of change of the phase lag. Gain and phase plots for the power stage are shown in Figure 18 and Figure 19.



Figure 18. Power Stage Gain and Phase



Figure 19. Power Stage Gain and Phase

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The single pole causes a rolloff in the gain of -20 dB/decade at lower frequency. The combination of the RHP zero and sampling double pole maintain the slope out to beyond the switching frequency. The phase tends towards  $-90^{\circ}$  at lower frequency but then increases to  $-180^{\circ}$  and beyond from the RHP zero and the sampling double pole. The effect of the ESR zero is not seen because its frequency is several decades above the switching frequency. The combination of increasing gain and decreasing phase makes converters with RHP zeroes difficult to compensate. Setting the overall control loop bandwidth to 1/3 to 1/10 of the RHP zero frequency minimizes these negative effects, but requires a compromise in the control loop bandwidth. If this loop were left uncompensated, the bandwidth would be 89 kHz and the phase margin  $-54^{\circ}$ . The converter would oscillate, and therefore is compensated using the error amplifier and a few passive components.

The transfer function of the compensation block ( $G_{EA}$ ) can be derived by treating the error amplifier as an inverting op-amp with input impedance  $Z_I$  and feedback impedance  $Z_F$ . The majority of applications require a Type II, or two-pole one-zero amplifier, shown in Figure 17. The LaPlace domain transfer function for this Type II network is given by Equation 52.

$$G_{EA} = \frac{Z_F}{Z_1} = \frac{1}{R_{FB2}(C1+C2)} \times \frac{s \times R1 \times C2 + 1}{s \left(\frac{s \times R1 \times C1 \times C2}{C1+C2} + 1\right)}$$

(52)

Many techniques exist for selecting the compensation component values. The following method is based upon setting the mid-band gain of the error amplifier transfer function first and then positioning the compensation zero and pole:

- 1. Determine the desired control loop bandwidth: The control loop bandwidth ( $f_{0dB}$ ) is the point at which the total control loop gain (H = G<sub>PS</sub> × G<sub>EA</sub>) is equal to 0 dB. For this example, a low bandwidth of 10 kHz, or approximately 1/6th of the RHP zero frequency, is chosen because of the wide variation in input voltage.
- 2. Determine the gain of the power stage at  $f_{OdB}$ : This value, A, can be read graphically from the gain plot of  $G_{PS}$  or calculated by replacing the 's' terms in  $G_{PS}$  with '2  $\pi f_{OdB}$ '. For this example, the gain at 10 kHz is approximately 16 dB.
- 3. Calculate the negative of A and convert it to a linear gain: By setting the mid-band gain of the error amplifier to the negative of the power stage gain at  $f_{0dB}$ , the control loop gain equals 0 dB at that frequency. For this example, -16 dB = 0.15 V/V.
- 4. Select the resistance of the top feedback divider resistor  $R_{FB2}$ : This value is arbitrary, however selecting a resistance between 10 k $\Omega$  and 100 k $\Omega$  leads to practical values of R1, C1, and C2. For this example,  $R_{FB2} = 20 \text{ k}\Omega \text{ 1\%}$ .
- 5. Set Equation 55:

$$R1 = A \times R_{FB2}$$

For this example:  $R1 = 0.15 \times 20000 = 3 \text{ k}\Omega$ 

- 6. Select a frequency for the compensation zero,  $f_{Z1}$ : The suggested placement for this zero is at the low-frequency pole of the power stage,  $f_{LFP} = \omega LFP / 2\pi$ . For this example,  $f_{Z1} = f_{LFP} = 423$  Hz
- 7. Set Equation 54.

$$C2 = \frac{1}{2\pi \times R1 \times f_{Z1}}$$
(54)

For this example, C2 = 125 nF

- 8. Select a frequency for the compensation pole,  $f_{P1}$ : The suggested placement for this pole is at one-fifth of the switching frequency. For this example,  $f_{P1} = 100 \text{ kHz}$
- 9. Set Equation 55.

$$C1 = \frac{C2}{2\pi \times C2 \times R1 \times f_{P1} - 1}$$

For this example, C1 = 530 pF

00

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(55)

(53)



Plug the closest 1% tolerance values for R<sub>FB2</sub> and R1, then the closest 10% values for C1 and C2 into G<sub>EA</sub> and model the error amp: The open-loop gain and bandwidth of the LM5022's internal error amplifier are 75 dB and 4 MHz, respectively. Their effect on G<sub>EA</sub> can be modeled using Equation 56:

$$OPG = \frac{2\pi \times GBW}{s + \frac{2\pi \times GBW}{A_{DC}}}$$

(56)

(57)

 $A_{DC}$  is a linear gain, the linear equivalent of 75 dB is approximately 5600 V/V. C1 = 560 pF 10%, C2 = 120 nF 10%, R1 = 3.01 k\Omega 1%

11. Plot or evaluate the actual error amplifier transfer function:

$$G_{EA-ACTUAL} = \frac{G_{EA} \times OPG}{1 + G_{EA} \times OPG}$$



Figure 20. Overall Loop Gain and Phase



Figure 21. Overall Loop Gain and Phase

12. Plot or evaluate the complete control loop transfer function: The complete control loop transfer function is obtained by multiplying the power stage and error amplifier functions together. The bandwidth and phase margin can then be read graphically or evaluated numerically. The bandwidth of this example circuit at V<sub>IN</sub> = 16 V is 10.5 kHz with a phase margin of 66°.

LM5022 JAJSAO5I – JANUARY 2007 – REVISED DECEMBER 2017

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13. Re-evaluate at the corners of input voltage and output current: Boost converters exhibit significant change in their loop response when V<sub>IN</sub> and I<sub>O</sub> change. With the compensation fixed, the total control loop gain and phase must be checked to ensure a minimum phase margin of 45° over both line and load.

#### 8.2.2.11 Efficiency Calculations

A reasonable estimation for the efficiency of a boost regulator controlled by the LM5022 can be obtained by adding together the loss is each current carrying element and using Equation 58.

$$\eta = \frac{P_{O}}{P_{O} + P_{\text{total-loss}}}$$
(58)

The following shows an efficiency calculation to complement the circuit design. Output power for this circuit is 40 V  $\times$  0.5 A = 20 W. Input voltage is assumed to be 13.8 V, and the calculations used assume that the converter runs in CCM. Duty cycle for V<sub>IN</sub> = 13.8 V is 66%, and the average inductor current is 1.5 A.

#### 8.2.2.11.1 Chip Operating Loss

This term accounts for the current drawn at the VIN pin. This current,  $I_{IN}$ , drives the logic circuitry and the power MOSFETs. The gate driving loss term from MOSFET is included in the chip operating loss. For the LM5022,  $I_{IN}$  is equal to the steady-state operating current,  $I_{CC}$ , plus the MOSFET driving current,  $I_{GC}$ . Power is lost as this current passes through the internal linear regulator of the LM5022 in Equation 59.

$$I_{GC} = Q_G \times f_{SW} I_{GC} = 27 \text{ nC} \times 500 \text{ kHz} = 13.5 \text{ mA}$$
(59)

I<sub>CC</sub> is typically 3.5 mA (taken from *Electrical Characteristics*). Chip operating loss is then calculated with Equation 60.

$$P_{Q} = V_{IN} \times (I_{Q} + I_{GC}) P_{Q} = 13.8 \times (3.5 \text{ m} + 13.5 \text{m}) = 235 \text{ mW}$$
(60)

#### 8.2.2.11.2 MOSFET Switching Loss

 $P_{SW} = 0.5 \times V_{IN} \times I_L \times (t_R + t_F) \times f_{SW} P_{SW} = 0.5 \times 13.8 \times 1.5 \times (10 \text{ ns} + 12 \text{ ns}) \times 5 \times 10^5 = 114 \text{ mW}$ (61)

#### 8.2.2.11.3 MOSFET and R<sub>SNS</sub> Conduction Loss

$$P_{\rm C} = D \times (I_{\rm L}^2 \times (R_{\rm DSON} \times 1.3 + R_{\rm SNS})) P_{\rm C} = 0.66 \times (1.5^2 \times (0.029 + 0.1)) = 192 \text{ mW}$$
(62)

#### 8.2.2.11.4 Output Diode Loss

The average output diode current is equal to  $I_O$  or 0.5 A. The estimated forward drop ( $V_D$ ) is 0.5 V. The output diode loss is Equation 63.

$$P_{D1} = I_0 \times V_D P_{D1} = 0.5 \times 0.5 = 0.25 W$$
(63)

#### 8.2.2.11.5 Input Capacitor Loss

This term represents the loss as input ripple current passes through the ESR of the input capacitor bank. In this equation 'n' is the number of capacitors in parallel. The 4.7- $\mu$ F input capacitors selected have a combined ESR of approximately 1.5 m $\Omega$ , and  $\Delta i_{L}$  for a 13.8-V input is 0.55 A in Equation 64 and Equation 65.

$$P_{CIN} = \frac{I_{IN-RMS}^2 \times ESR}{n}$$
(64)

$$I_{\text{IN-RMS}} = 0.29 \times \Delta i_{\text{L}} = 0.29 \times 0.55 = 0.16 \text{ A P}_{\text{CIN}} = [0.16^2 \times 0.0015] / 2 = 0.02 \text{ mW} \text{ (negligible)}$$
(65)

#### 8.2.2.11.6 Output Capacitor Loss

This term is calculated using the same method as the input capacitor loss, substituting the output capacitor RMS current for  $V_{IN} = 13.8$  V. The combined ESR of the output capacitors is also approximately 1.5 m $\Omega$  in Equation 66.

$$I_{O-RMS} = 1.13 \times 1.5 \times (0.66 \times 0.34)^{0.5} = 0.8 \text{ A P}_{CO} = [0.8 \times 0.0015] / 2 = 0.6 \text{ mW}$$
(66)



#### 8.2.2.11.7 Boost Inductor Loss

The typical DCR of the selected inductor is 40 m $\Omega$  in Equation 67.

$$P_{DCR} = I_{L}^{2} \times DCR P_{DCR} = 1.5^{2} \times 0.04 = 90 \text{ mW}$$

Core loss in the inductor is estimated to be equal to the DCR loss, adding an additional 90 mW to the total inductor loss.

#### 8.2.2.11.8 Total Loss

 $P_{LOSS}$  = Sum of All Loss Terms = 972 mW

#### 8.2.2.11.9 Efficiency

 $\eta = 20 / (20 + 0.972) = 95\%$ 

#### 8.2.3 Application Curves



(67)

(68)

(69)

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LM5022 JAJSAO5I – JANUARY 2007 – REVISED DECEMBER 2017

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### 9 Power Supply Recommendations

LM5022 is a power management device. The power supply for the device can be any DC voltage source within the specified input range.



### 10 Layout

### **10.1 Layout Guidelines**

To produce an optimal power solution with the LM5022, good layout and design of the PCB are as critical as component selection. The following are the several guidelines to create a good layout of the PCB, as based on Figure 14:

- 1. Using a low-ESR ceramic capacitor, place  $C_{\text{INX}}$  as close as possible to the VIN and GND pins of the LM5022.
- 2. Using a low-ESR ceramic capacitor, place  $C_{OX}$  close to the load as possible of the LM5022.
- 3. Using a low-ESR ceramic capacitor, place  $C_F$  close to the VCC and GND pins of the LM5022.
- 4. Minimize the loop area formed by the output capacitor connections  $(C_{o1}, C_{o2})$  by D1 and  $R_{sns}$ . Make sure the cathode of D1 and  $R_{sns}$  are positioned next to each other, and place  $C_{o1}(+)$  and  $C_{o1}(-)$  close to D1 cathode and  $R_{sns}(-)$  respectively.
- 5. R<sub>sns</sub>(+) must be connected to the CS pin with a separate trace made as short as possible. This trace must be routed away from the inductor and the switch node (where D1, Q1, and L1 connect).
- 6. Minimize the trace length to the FB pin by positioning  $R_{FB1}$  and  $R_{FB2}$  close to the LM5022.
- 7. Route the VOUT sense path away from noisy node and connect it as close as possible to the positive side of  $C_{\text{OX}}$ .

### 10.1.1 Filter Capacitors

The low-value ceramic filter capacitors are most effective when the inductance of the current loops that they filter is minimized. Place  $C_{INX}$  as close as possible to the VIN and GND pins of the LM5022. Place  $C_{OX}$  close to the load, and  $C_F$  next to the VCC and GND pins of the LM5022.

### 10.1.2 Sense Lines

The top of  $R_{SNS}$  must be connected to the CS pin with a separate trace made as short as possible. Route this trace away from the inductor and the switch node (where D1, Q1, and L1 connect). For the voltage loop, keep  $R_{FB1/2}$  close to the LM5022 and run a trace from as close as possible to the positive side of  $C_{OX}$  to  $R_{FB2}$ . As with the CS line, the FB line must be routed away from the inductor and the switch node. These measures minimize the length of high impedance lines and reduce noise pickup.

#### 10.1.3 Compact Layout

Parasitic inductance can be reduced by keeping the power path components close together. As described in *Layout Guidelines*, keep the high slew-rate current loops as tight as possible. Short, thick traces or copper pours (shapes) are best.

The switch node must be just large enough to connect all the components together without excessive heating from the current it carries. The LM5022 (boost converter) operates in two distinct cycles whose high current paths are shown in Figure 29.



Figure 29. Boost Converter Current Loops



### Layout Guidelines (continued)

The dark grey, inner loops represents the high current paths during the MOSFET on-time. The light grey, outer loop represents the high current path during the off-time.

### 10.1.4 Ground Plane and Shape Routing

The diagram of Figure 29 is also useful for analyzing the flow of continuous current versus the flow of pulsating currents. The circuit paths with current flow during both the on-time and off-time are considered to be continuous current, while those that carry current during the on-time or off-time only are pulsating currents. Preference in routing must be given to the pulsating current paths, as these are the portions of the circuit most likely to emit EMI. The ground plane of a PCB is a conductor and return path, and it is susceptible to noise injection just as any other circuit path. The continuous current paths on the ground net can be routed on the system ground plane with less risk of injecting noise into other circuits. The path between the input source, input capacitor and the MOSFET and the path between the output capacitor and the load are examples of continuous current paths. In contrast, the path between the grounded side of the power switch and the negative output capacitor terminal carries a large pulsating current. This path must be routed with a short, thick shape, preferably on the component side of the PCB. Multiple vias in parallel must be used right at the negative pads of the input and output capacitors to connect the component side shapes to the ground plane. Vias must not be placed directly at the grounded side of the MOSFET (or  $R_{SNS}$ ) as they tend to inject noise into the ground plane. A second pulsating current loop that is often ignored but must be kept small is the gate drive loop formed by the OUT and VCC pins, Q1,  $R_{SNS}$ , and capacitor  $C_F$ .

### **10.2 Layout Examples**



Figure 30. Top Layer and Top Overlay



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### Layout Examples (continued)



Figure 31. Bottom Layer

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### 11 デバイスおよびドキュメントのサポート

### 11.1 デバイス・サポート

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### 11.2 ドキュメントのサポート

### 11.2.1 関連資料

関連資料については、以下を参照してください。

『AN-1557 LM5022評価ボード』(SNVA203)

### 11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通 知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の 詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 11.4 コミュニティ・リソース

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### 11.7 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

### 12 メカニカル、パッケージ、および注文情報

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### **PACKAGING INFORMATION**

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
LM5022MM/NOPB	Active	Production	VSSOP (DGS)   10	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5022
LM5022MM/NOPB.A	Active	Production	VSSOP (DGS)   10	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5022
LM5022MM/NOPB.B	Active	Production	VSSOP (DGS)   10	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5022
LM5022MME/NOPB	Active	Production	VSSOP (DGS)   10	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5022
LM5022MME/NOPB.A	Active	Production	VSSOP (DGS)   10	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5022
LM5022MME/NOPB.B	Active	Production	VSSOP (DGS)   10	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5022
LM5022MMX/NOPB	Active	Production	VSSOP (DGS)   10	3500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5022
LM5022MMX/NOPB.A	Active	Production	VSSOP (DGS)   10	3500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5022
LM5022MMX/NOPB.B	Active	Production	VSSOP (DGS)   10	3500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5022

<sup>(1)</sup> **Status:** For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

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23-May-2025

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#### OTHER QUALIFIED VERSIONS OF LM5022 :

• Automotive : LM5022-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



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### TAPE AND REEL INFORMATION





#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5022MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5022MME/NOPB	VSSOP	DGS	10	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5022MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1



## PACKAGE MATERIALS INFORMATION

25-Sep-2024



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5022MM/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM5022MME/NOPB	VSSOP	DGS	10	250	208.0	191.0	35.0
LM5022MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0

## **DGS0010A**



## **PACKAGE OUTLINE**

### VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187, variation BA.



## DGS0010A

## **EXAMPLE BOARD LAYOUT**

### VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

![](_page_37_Figure_4.jpeg)

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

![](_page_37_Picture_8.jpeg)

## DGS0010A

## **EXAMPLE STENCIL DESIGN**

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

![](_page_38_Figure_4.jpeg)

NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

![](_page_38_Picture_8.jpeg)

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