

LM2901B-Q1、LM2901x-Q1 車載用、クワッド コンパレータ

1 特長

- 車載アプリケーション認定済み
- 下記の内容で AEC-Q100 認定済み:
 - デバイス温度グレード 1: 動作時周囲温度範囲 $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
 - デバイス HBM ESD 分類レベル:
 - 「AV」バージョンは Class 1C
 - 他のすべてのバージョンは Class 2
 - デバイス CDM ESD 分類レベル C3
- 「B」デバイスの HBM ESD を 2kV に改善
- シングル電源またはデュアル電源
- 電源電圧に依存しない低い消費電流、コンパレータあたり 200 μA (代表値) (「B」バージョン)
- 低い入力バイアス電流、3.5nA (代表値) (「B」デバイス)
- 低い入力オフセット電流、0.5nA (代表値) (「B」デバイス)
- 低い入力オフセット電圧、 $\pm 0.37\text{mV}$ (代表値) (「B」デバイス)
- 同相入力電圧範囲にグランドを含む
- 差動入力電圧範囲は最大定格電源電圧と同じ $\pm 36\text{V}$
- TTL、MOS、CMOS 互換出力
- SOT のシングルバージョンについては、TL331-Q1 (SLVS969) を参照
- 複数パッケージのデュアルバージョンについては、LM2903x-Q1 (SLCS141) を参照
- 機能安全対応
 - 機能安全システムの設計に役立つ資料を利用可能

2 アプリケーション

- 車載用
 - HEV/EV およびパワートレイン
 - インフォテインメントおよびクラスタ
 - ボディコントロール モジュール

- 産業用
- 電化製品

3 説明

LM2901B-Q1 デバイスは、業界標準の LM2901x-Q1 コンパレータ ファミリの次世代バージョンです。この次世代ファミリは、小さいオフセット電圧、より高い電源電圧への対応などの特長を備え、コストの制約が厳しいアプリケーション向けに大きな価値を提供します。さらに、低消費電流、小さい入力バイアス電流、小さい伝搬遅延、2kV の優れた ESD 特性と、そのまま置き換えることができる利便性を兼ね備えています。

すべてのデバイスは、広い電圧範囲にわたって動作するように設計された 4 つの独立した電圧コンパレータで構成されています。デュアル電源でも、2 つの電源間の差分が 2V $\sim$ 36V の範囲内であり、VCC が入力同相電圧より 1.5V 以上高ければ、動作可能です。出力は、他のオープン コレクタ出力に接続できます。

「V」バージョンは最大 32V で動作し、「B」バージョンは最大 36V で動作します。すべて、AEC-Q100 グレード 1 の温度範囲 $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$ で認定済みです。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
LM2901B-Q1 LM2901-Q1 LM2901A-Q1 LM2901AV-Q1	TSSOP (14)	4.40mm $\times$ 5.00mm
	SOIC (14)	3.91mm $\times$ 8.65mm
LM2901B-Q1	SOT-23 (14) (プレビュー)	4.20 mm $\times$ 2.00mm
	X2QFN (14) (プレビュー)	2.00mm $\times$ 2.00mm
	WQFN (16)	3.00mm $\times$ 3.00 mm

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ファミリ比較表

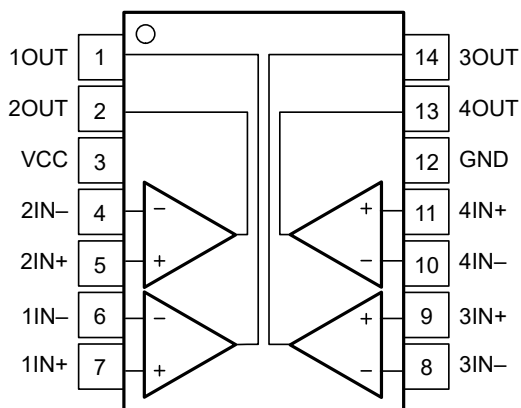
仕様	LM2901B-Q1	LM2901-Q1	LM2901V-Q1	LM2901AV-Q1	単位
電源電圧	2 $\sim$ 36	2 $\sim$ 30	2 $\sim$ 32	2 $\sim$ 32	V
総消費電流 (5V $\sim$ 最大値 36V)	0.6 $\sim$ 0.8	1 $\sim$ 2.5	1 $\sim$ 2.5	1 $\sim$ 2.5	mA
温度範囲	-40 $\sim$ 125	-40 $\sim$ 125	-40 $\sim$ 125	-40 $\sim$ 125	$^{\circ}\text{C}$
静電気放電 (HBM)	2000	2000	2000	2000	V
オフセット電圧 (最大過熱値)	± 5.5	± 15	± 15	± 4	mV
入力バイアス電流 (代表値 / 最大値)	3.5 / 25	25 / 250	25 / 250	25 / 250	nA
応答時間 (代表値)	1	1.3	1.3	1.3	μsec



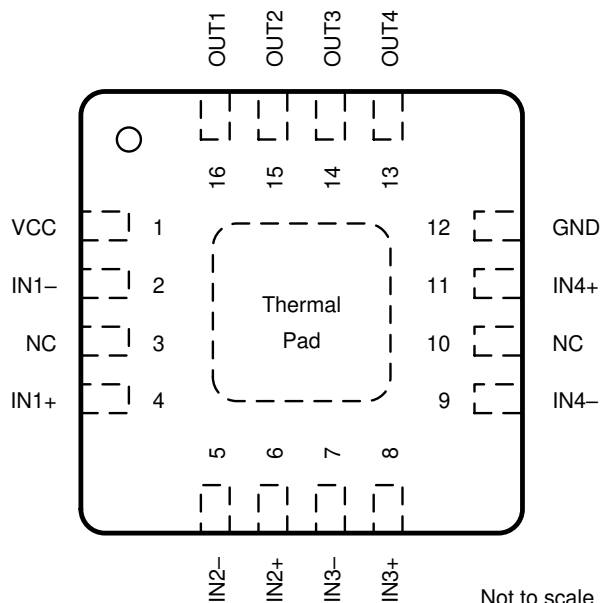
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4 Pin Configuration and Functions

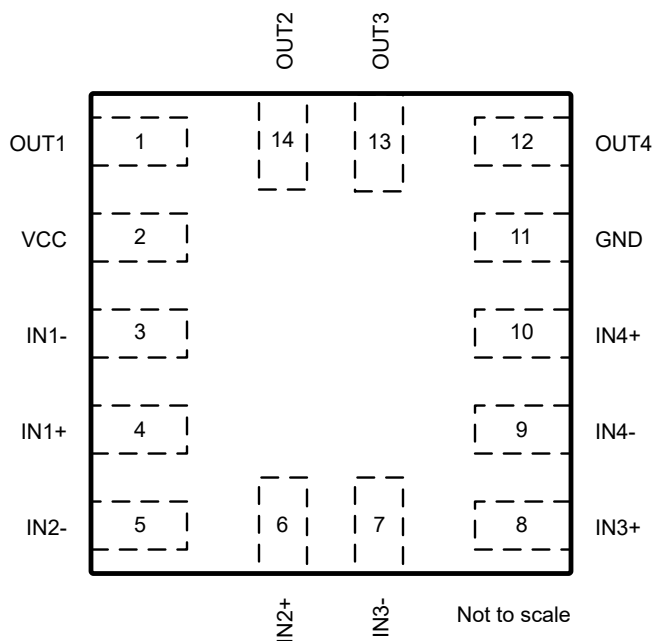


**図 4-1. D, PW and DYY Packages
14-Pin SOIC, TSSOP and SOT-23
Top View**



NOTE: Connect exposed thermal pad directly to GND pin.

**図 4-2. RTE Package
16-Pad WQFN With Exposed Thermal Pad
Top View**



**図 4-3. RUC Package
14-Pad X2QFN
Top View**

表 4-1. Pin Functions

NAME ⁽¹⁾	PIN			I/O	DESCRIPTION
	SOIC, TSSOP, DYY	X2QFN	WQFN		
OUT1 ⁽¹⁾	1	14	16	Output	Output pin of the comparator 2
OUT2 ⁽¹⁾	2	1	15	Output	Output pin of the comparator 1
V _{CC}	3	2	1	—	Positive supply
IN2– ⁽¹⁾	4	3	5	Input	Negative input pin of the comparator 1
IN2+ ⁽¹⁾	5	4	6	Input	Positive input pin of the comparator 1
IN1– ⁽¹⁾	6	5	2	Input	Negative input pin of the comparator 2
IN1+ ⁽¹⁾	7	6	4	Input	Positive input pin of the comparator 2
IN3–	8	7	7	Input	Negative input pin of the comparator 3
IN3+	9	8	8	Input	Positive input pin of the comparator 3
IN4–	10	9	9	Input	Negative input pin of the comparator 4
IN4+	11	10	11	Input	Positive input pin of the comparator 4
GND	12	11	12	—	Negative supply
OUT4	13	12	13	Output	Output pin of the comparator 4
OUT3	14	13	14	Output	Output pin of the comparator 3
NC	—	—	3	—	No Internal Connection - Leave floating or GND
NC	—	—	10	—	No Internal Connection - Leave floating or GND
Thermal Pad	—	—	PAD	—	Connect directly to GND pin

(1) Some manufacturers transpose the names of channels 1 & 2. Electrically the pinouts are identical, just a difference in channel naming convention.

5 Specifications

5.1 Absolute Maximum Ratings for LM2901B-Q1

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage: $V_S = (V+) - (V-)$	-0.3	38	V
Differential input voltage : V_{ID} ⁽²⁾		±38	V
Input pins (IN+, IN-)	-0.3	38	V
Current into input pins (IN+, IN-)		-50	mA
Output pin (OUT)	-0.3	38	V
Output sink current		25	mA
Output short-circuit duration ⁽³⁾		Unlimited	s
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
- (2) Differential voltages are at IN+ with respect to IN-.
- (3) Short circuits from outputs to V+ can cause excessive heating and eventual destruction.

5.2 Absolute Maximum Ratings for LM2901x-Q1

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage, V_{CC} ⁽²⁾		36	V
Differential input voltage, V_{ID} ⁽³⁾		±36	
Input voltage range, V_I (either input)	-0.3	36	
Output voltage, V_O		36	
Output current, I_O		20	mA
Duration of output short circuit to ground ⁽⁴⁾		Unlimited	
Operating virtual junction temperature, T_J		150	°C
Storage temperature, T_{stg}	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings can cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this can affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values, except differential voltages, are with respect to network ground.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

5.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per AEC Q100-011 ⁽¹⁾	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.4 Recommended Operating Conditions for LM2901B-Q1

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: $V_S = (V+) - (V-)$	2	36	V
Ambient temperature, T_A , LM2901B-Q1	–40	125	°C
Input Voltage Range, V_{IVR}	$(V-) - 0.1$	$(V+) - 2.0$	V

5.5 Recommended Operating Conditions for LM2901x-Q1

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	LM2901-Q1	2	30	V
		LM2901V-Q1, LM2901AV-Q1	2	32	
T_A	Ambient temperature		–40	125	°C
I_O	Output current (per comparator)		0	4	mA

5.6 Thermal Information

THERMAL METRIC ⁽¹⁾		All Devices					UNIT
		D (SOIC)	PW (TSSOP)	DDY (SOT-23)	RTE (WQFN)	RUC (X2QFN)	
		14 PINS	14 PINS	14 PINS	16 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.2	136.6		67.6		°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.9	66.6		72.3		
$R_{\theta JB}$	Junction-to-board thermal resistance	67.8	79.8		43.1		
ψ_{JT}	Junction-to-top characterization parameter	28.0	17.8		6.3		
ψ_{JB}	Junction-to-board characterization parameter	67.4	79.3		42.8		
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	-	26.4	-	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report, [SPRA953](#).

5.7 Electrical Characteristics for LM2901B-Q1

$V_S = 5V$, $V_{CM} = (V-)$; $T_A = 25^\circ C$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_S = 5$ to $36V$	-3.5	± 0.37	3.5	mV
		$V_S = 5$ to $36V$, $T_A = -40^\circ C$ to $+125^\circ C$	-5.5		5.5	
I_B	Input bias current			-3.5	-25	nA
		$T_A = -40^\circ C$ to $+125^\circ C$			-50	nA
I_{OS}	Input offset current		-25	± 0.5	25	nA
		$T_A = -40^\circ C$ to $+125^\circ C$	-50		50	nA
V_{CM}	Common mode range ⁽¹⁾	$V_S = 3$ to $36V$	(V-)		(V+) - 1.5	V
		$V_S = 3$ to $36V$, $T_A = -40^\circ C$ to $+125^\circ C$	(V-)		(V+) - 2.0	V
A_{VD}	Large signal differential voltage amplification	$V_S = 15V$, $V_O = 1.4V$ to $11.4V$; $R_L \geq 15k$ to (V+)	50	200		V/mV
V_{OL}	Low level output Voltage {swing from (V-)}	$I_{SINK} \leq 4mA$, $V_{ID} = -1V$		110	400	mV
		$I_{SINK} \leq 4mA$, $V_{ID} = -1V$ $T_A = -40^\circ C$ to $+125^\circ C$			550	mV
I_{OH-LKG}	High-level output leakage current	(V+) = $V_O = 5V$; $V_{ID} = 1V$		0.1	50	nA
		(V+) = $V_O = 36V$; $V_{ID} = 1V$			100	nA
I_{OL}	Low level output current	$V_{OL} = 1.5V$; $V_{ID} = -1V$; $V_S = 5V$	6	21		mA
I_Q	Quiescent current (all comparators)	$V_S = 5V$, no load		0.8	1.2	mA
		$V_S = 36V$, no load, $T_A = -40^\circ C$ to $+125^\circ C$		1	1.6	mA

- (1) When the voltage at either input goes negative by more than 0.3V, the output can be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by $V_{CC} - 2V$. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.

5.8 Switching Characteristics for LM2901B-Q1

$V_S = 5V$, $V_{O_PULLUP} = 5V$, $V_{CM} = V_S/2$, $C_L = 15pF$, $R_L = 5.1k\Omega$, $T_A = 25^\circ C$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{response}$	Propagation delay time, high-to-low; Small scale input signal ⁽¹⁾	Input overdrive = 5mV, Input step = 100mV		1000		ns
$t_{response}$	Propagation delay time, high-to-low; TTL input signal ⁽¹⁾	TTL input with $V_{ref} = 1.4V$		300		ns

- (1) High-to-low and low-to-high refers to the transition at the input.

5.9 Electrical Characteristics for LM2901x-Q1

$V_{CC} = 5V$, at specified free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾		T_A ⁽²⁾	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	$V_{IC} = V_{ICR(min)}$, $V_O = 1.4V$, $V_{CC} = 5V$ to MAX ⁽³⁾	Non A devices	25°C		2	7	mV
			Full range			15	
		A suffix devices	25°C		1	2	
			Full range			4	
I_{IO} Input offset current	$V_O = 1.4V$		25°C		5	50	nA
			Full range			200	
I_{IB} Input bias current	$V_O = 1.4V$		25°C		–25	–250	nA
			Full range			–500	
V_{ICR} Common-mode input-voltage range ⁽⁴⁾			25°C	0	$V_{CC} - 1.5$		V
			Full range	0	$V_{CC} - 2$		
A_{VD} Large-signal differential-voltage amplification	$V_{CC} = 15V$, $V_O = 1.4V$ to $11.4V$, $R_L \geq 15k\Omega$ to V_{CC}		25°C	25	100		V/mV
I_{OH} High-level output current	$V_{ID} = 1V$	$V_{OH} = 5V$	25°C		0.1	50	nA
		$V_{OH} = V_{CC}$ MAX ⁽³⁾	Full range			1	μA
V_{OL} Low-level output voltage	$V_{ID} = -1V$	$I_{OL} = 4mA$	25°C		150	400	mV
			Full range			700	
I_{OL} Low-level output current	$V_{ID} = -1V$	$V_{OL} = 1.5V$	25°C	6	16		mA
I_{CC} Supply current (four comparators)	$V_O = 2.5V$, No load	$V_{CC} = 5V$	25°C		0.8	2	
		$V_{CC} = MAX$ ⁽³⁾			1	2.5	

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.

(2) Full range (MIN to MAX) is $-40^\circ C$ to $125^\circ C$. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.

(3) V_{CC} MAX = 30V for non-V devices and 32V for V-suffix devices.

(4) The voltage at either the input or common mode can not be allowed to negative by more than 0.3V. The upper end of the common-mode voltage range is $V_{CC+} - 1.5V$; however, one input can exceed V_{CC} , and the comparator can provide a proper output state as long as the other input remains in the common-mode range. Either or both inputs can go to 30V without damage.

5.10 Switching Characteristics for LM2901x-Q1

$V_{CC} = 5V$, $T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time ⁽²⁾	R_L connected to 5V through 5.1k Ω , $C_L = 15pF$ ⁽¹⁾	100mV input step with 5mV overdrive		1.3		μs
		TTL-level input step		0.3		

(1) C_L includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4V.

5.11 Typical Characteristics

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $R_{\text{PULLUP}} = 5.1\text{k}$, $C_L = 15\text{pF}$, $V_{\text{CM}} = 0\text{V}$, $V_{\text{UNDERDRIVE}} = 100\text{mV}$, $V_{\text{OVERDRIVE}} = 100\text{mV}$ unless otherwise noted.

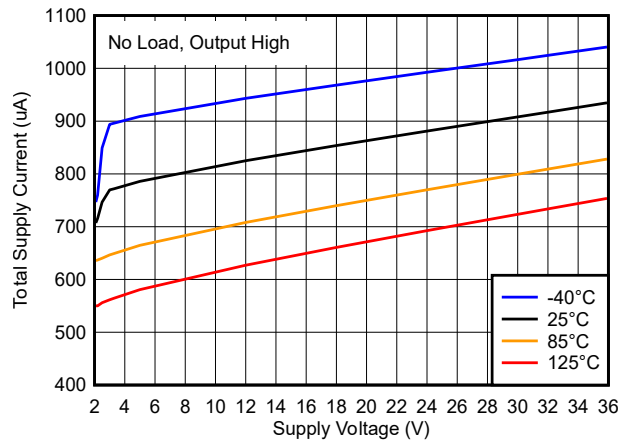


Figure 5-1. Total Supply Current vs. Supply Voltage

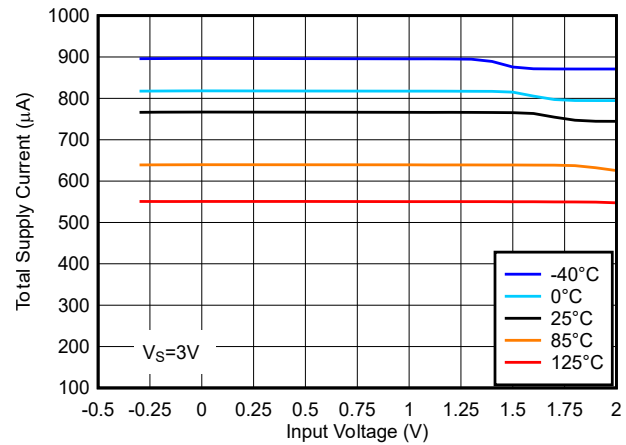


Figure 5-2. Total Supply Current vs. Input Voltage at 3V

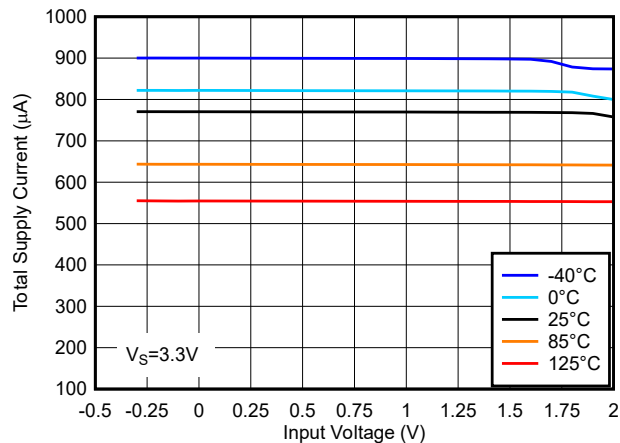


Figure 5-3. Total Supply Current vs. Input Voltage at 3.3V

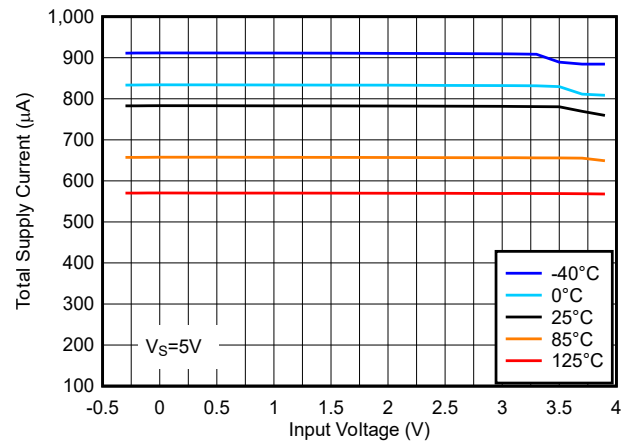


Figure 5-4. Total Supply Current vs. Input Voltage at 5V

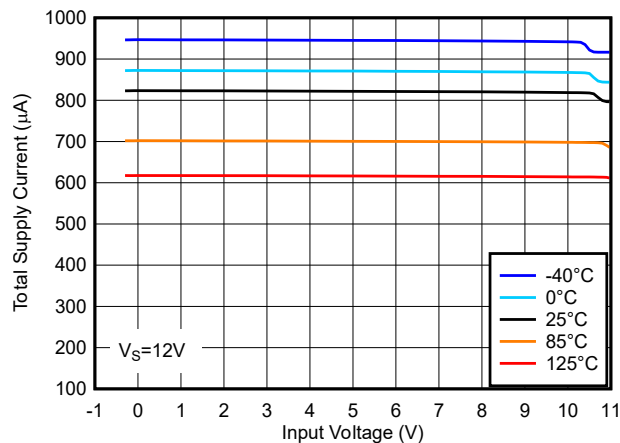


Figure 5-5. Total Supply Current vs. Input Voltage at 12V

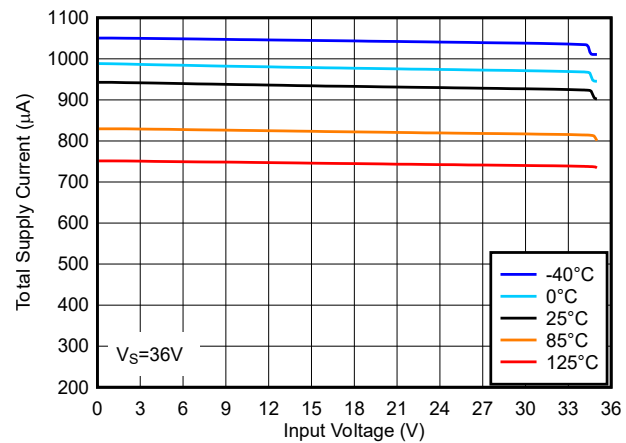
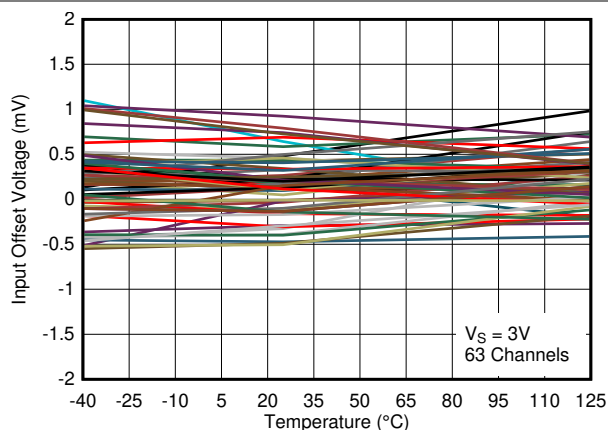


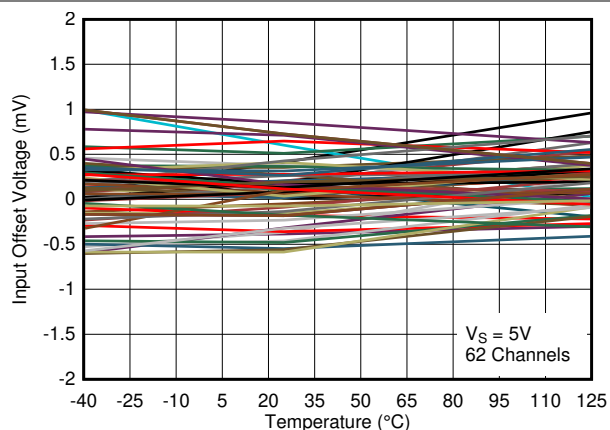
Figure 5-6. Total Supply Current vs. Input Voltage at 36V

5.11 Typical Characteristics (continued)

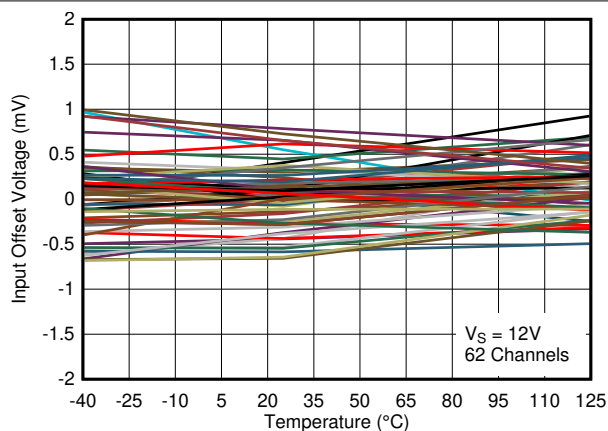
$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $R_{\text{PULLUP}} = 5.1\text{k}$, $C_L = 15\text{pF}$, $V_{\text{CM}} = 0\text{V}$, $V_{\text{UNDERDRIVE}} = 100\text{mV}$, $V_{\text{OVERDRIVE}} = 100\text{mV}$ unless otherwise noted.



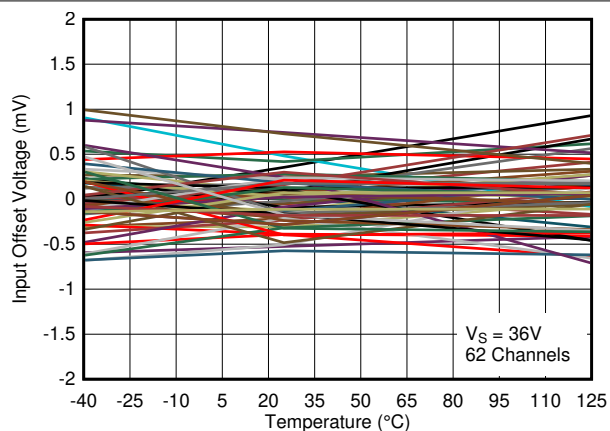
5-7. Input Offset Voltage vs. Temperature at 3V



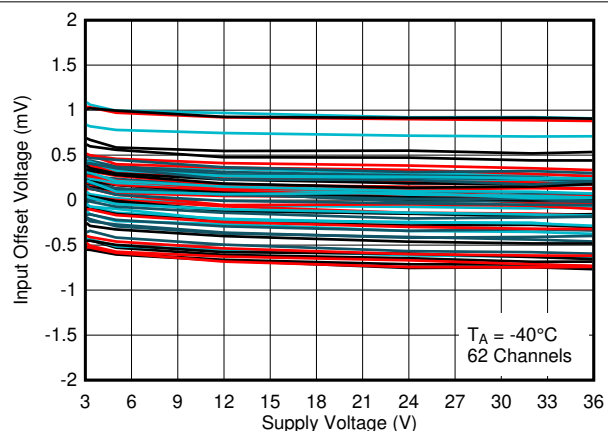
5-8. Input Offset Voltage vs. Temperature at 5V



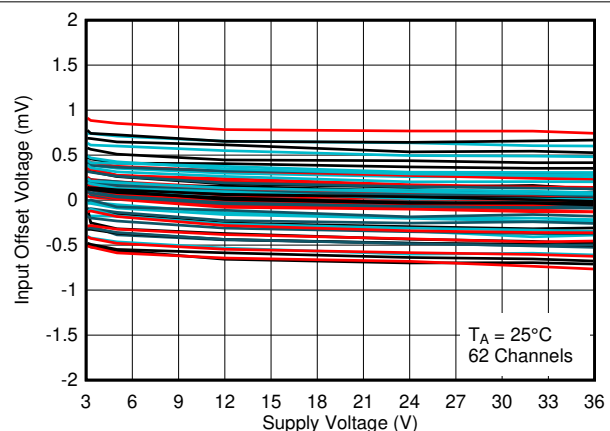
5-9. Input Offset Voltage vs. Temperature at 12V



5-10. Input Offset Voltage vs. Temperature at 36V



5-11. Input Offset Voltage vs. Supply Voltage at -40°C



5-12. Input Offset Voltage vs. Supply Voltage at 25°C

5.11 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $R_{\text{PULLUP}} = 5.1\text{k}$, $C_L = 15\text{pF}$, $V_{\text{CM}} = 0\text{V}$, $V_{\text{UNDERDRIVE}} = 100\text{mV}$, $V_{\text{OVERDRIVE}} = 100\text{mV}$ unless otherwise noted.

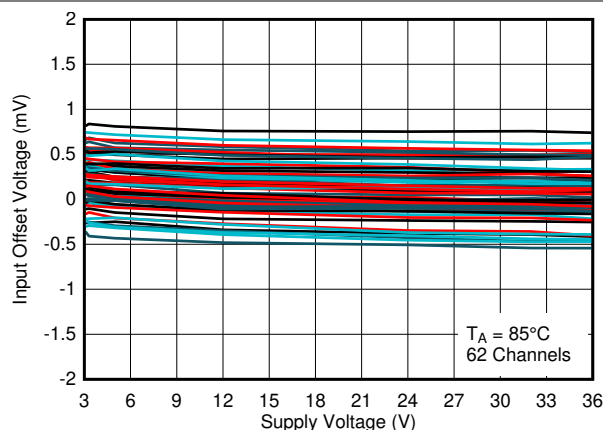


FIG 5-13. Input Offset Voltage vs. Supply Voltage at 85°C

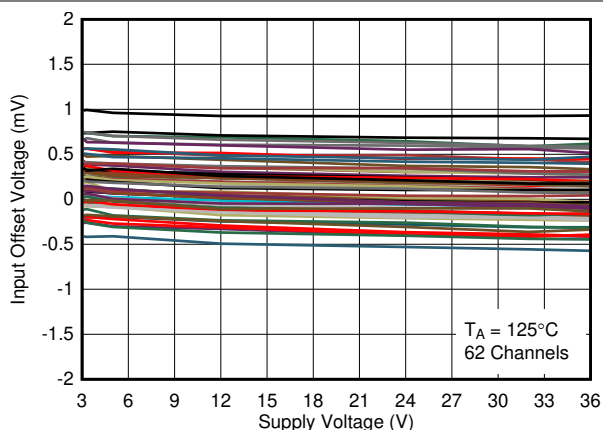


FIG 5-14. Input Offset Voltage vs. Supply Voltage at 125°C

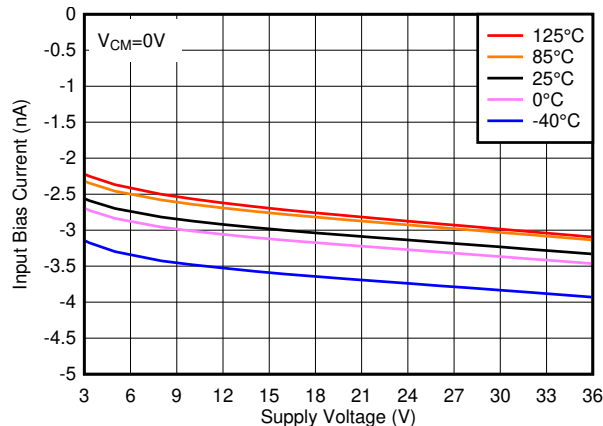


FIG 5-15. Input Bias Current vs. Supply Voltage

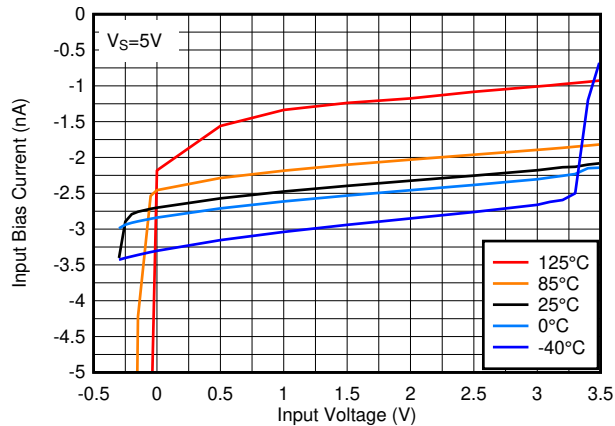


FIG 5-16. Input Bias Current vs. Input Voltage at 5V

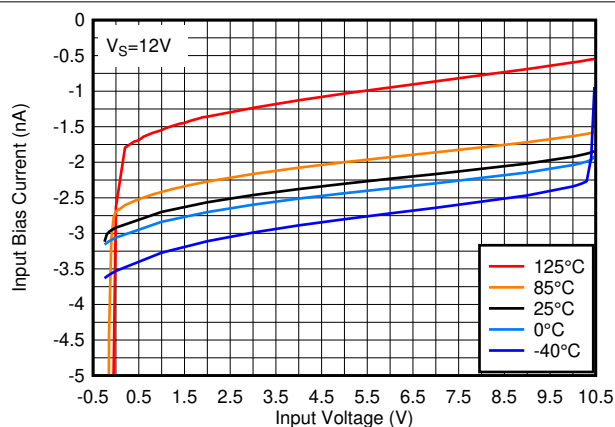


FIG 5-17. Input Bias Current vs. Input Voltage at 12V

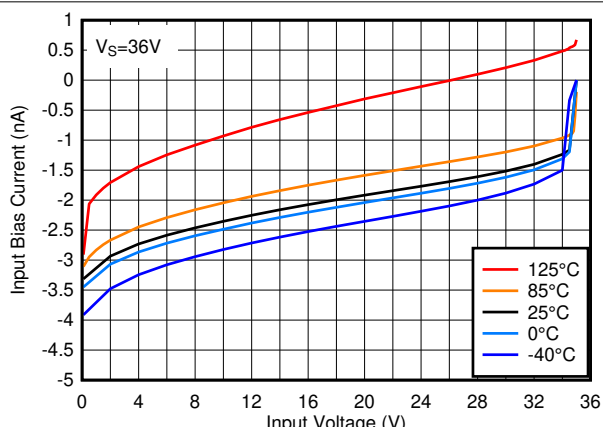


FIG 5-18. Input Bias Current vs. Input Voltage at 36V

5.11 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $R_{\text{PULLUP}} = 5.1\text{k}$, $C_L = 15\text{pF}$, $V_{\text{CM}} = 0\text{V}$, $V_{\text{UNDERDRIVE}} = 100\text{mV}$, $V_{\text{OVERDRIVE}} = 100\text{mV}$ unless otherwise noted.

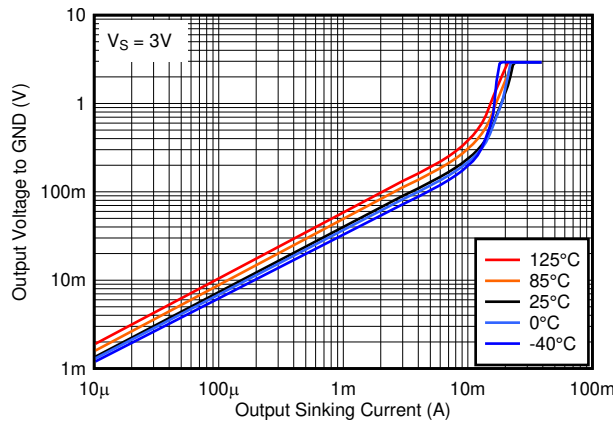


FIG 5-19. Output Low Voltage vs. Output Sinking Current at 3V

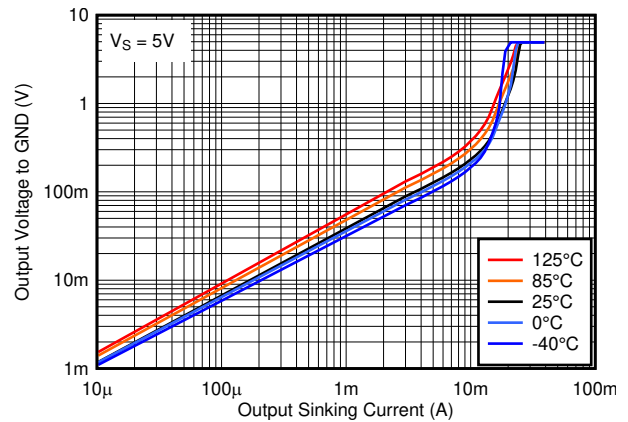


FIG 5-20. Output Low Voltage vs. Output Sinking Current at 5V

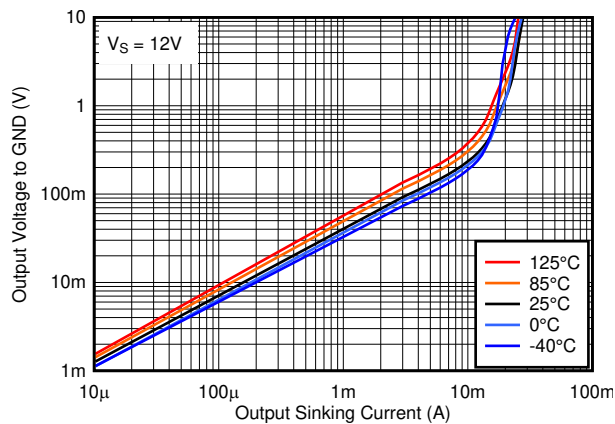


FIG 5-21. Output Low Voltage vs. Output Sinking Current at 12V

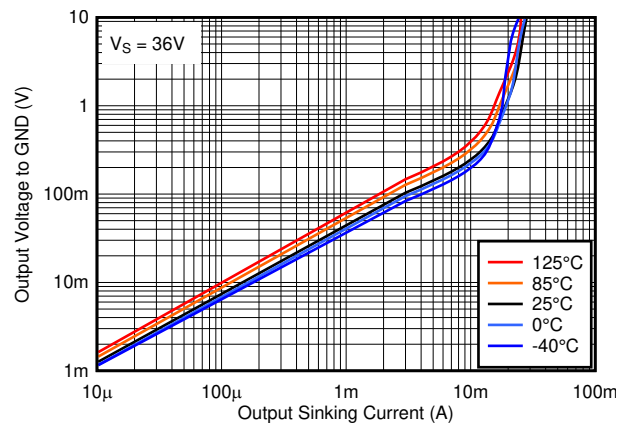


FIG 5-22. Output Low Voltage vs. Output Sinking Current at 36V

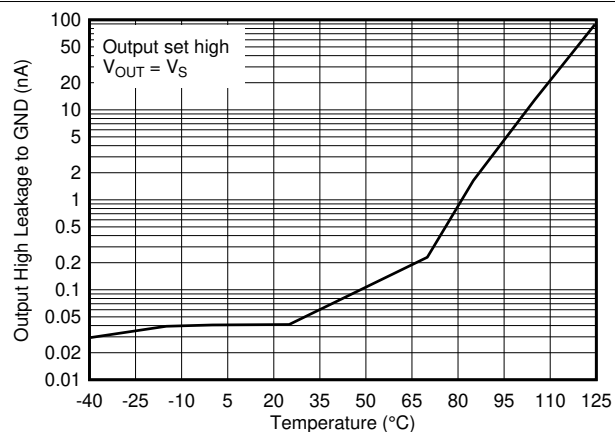


FIG 5-23. Output High Leakage Current vs. Temperature at 5V

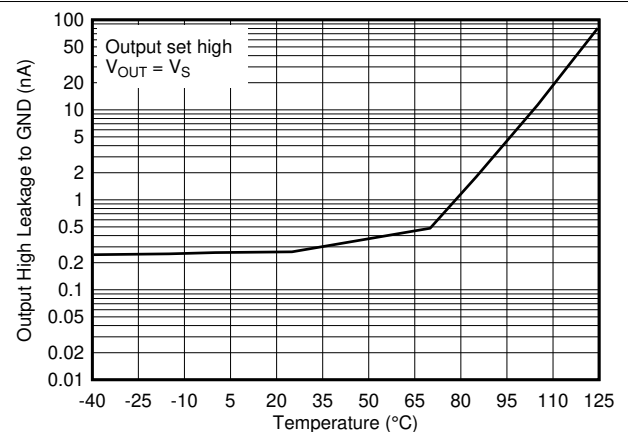


FIG 5-24. Output High Leakage Current vs. Temperature at 36V

5.11 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $R_{\text{PULLUP}} = 5.1\text{k}$, $C_L = 15\text{pF}$, $V_{\text{CM}} = 0\text{V}$, $V_{\text{UNDERDRIVE}} = 100\text{mV}$, $V_{\text{OVERDRIVE}} = 100\text{mV}$ unless otherwise noted.

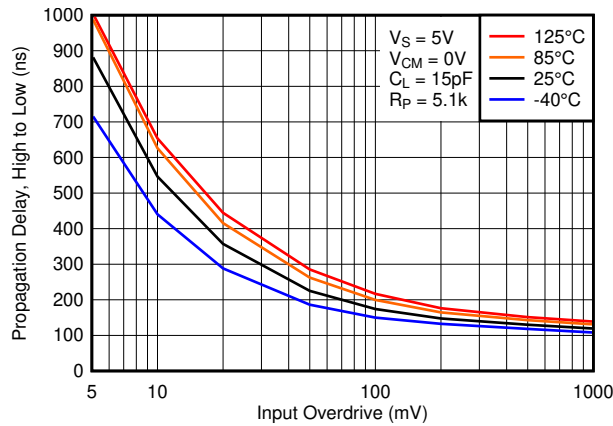


FIG 5-25. High to Low Propagation Delay vs. Input Overdrive Voltage, 5V

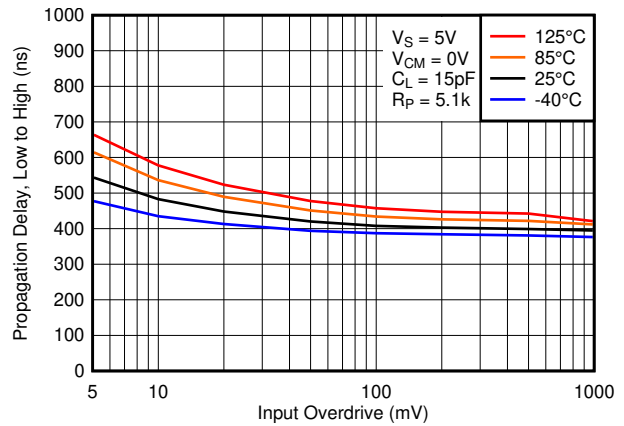


FIG 5-26. Low to High Propagation Delay vs. Input Overdrive Voltage, 5V

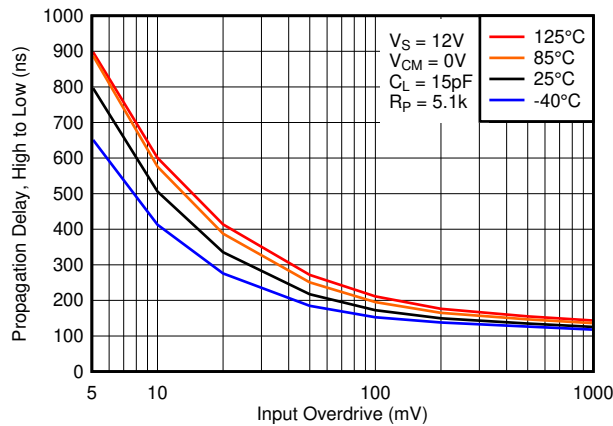


FIG 5-27. High to Low Propagation Delay vs. Input Overdrive Voltage, 12V

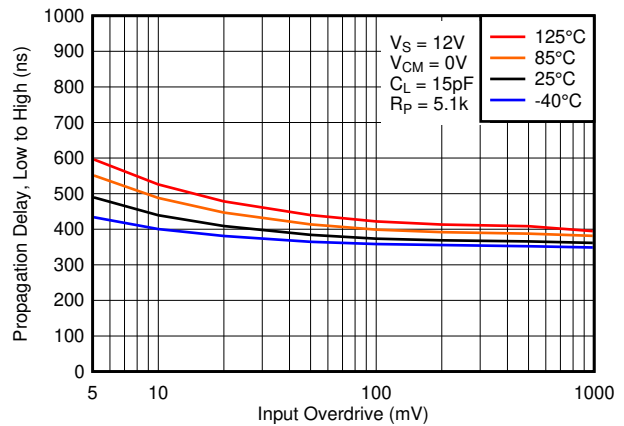


FIG 5-28. Low to High Propagation Delay vs. Input Overdrive Voltage, 12V

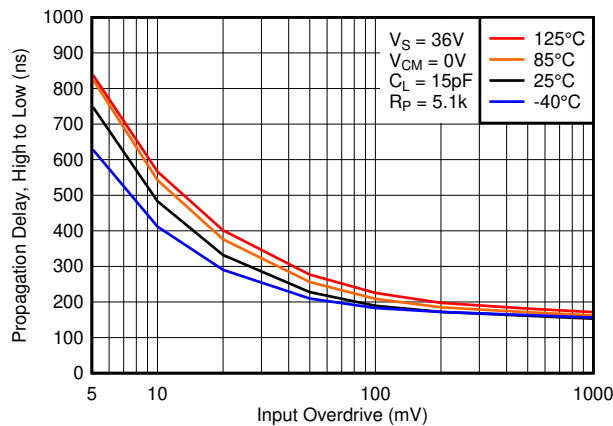


FIG 5-29. High to Low Propagation Delay vs. Input Overdrive Voltage, 36V

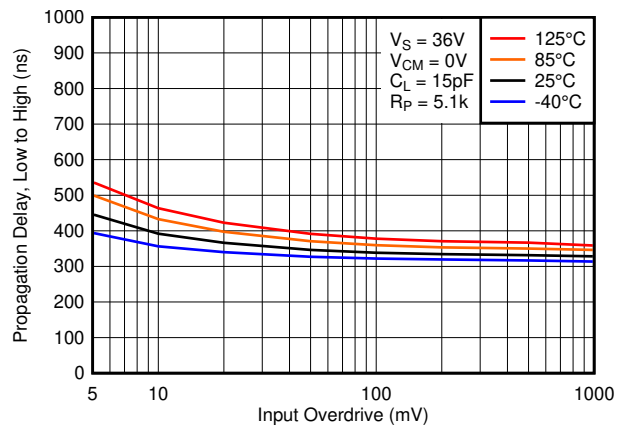


FIG 5-30. Low to High Propagation Delay vs. Input Overdrive Voltage, 36V

5.11 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $R_{\text{PULLUP}} = 5.1\text{k}$, $C_L = 15\text{pF}$, $V_{\text{CM}} = 0\text{V}$, $V_{\text{UNDERDRIVE}} = 100\text{mV}$, $V_{\text{OVERDRIVE}} = 100\text{mV}$ unless otherwise noted.

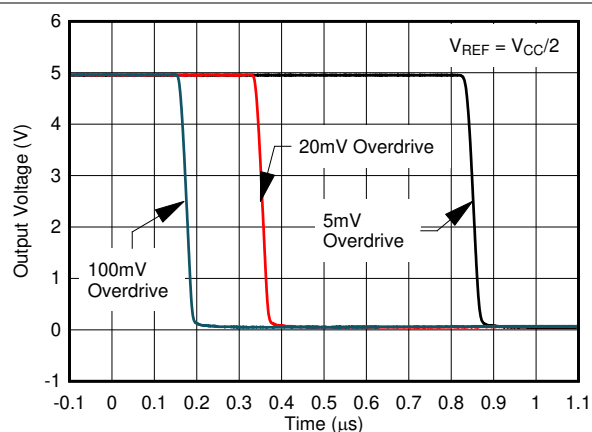


FIG 5-31. Response Time for Various Overdrives, High-to-Low Transition

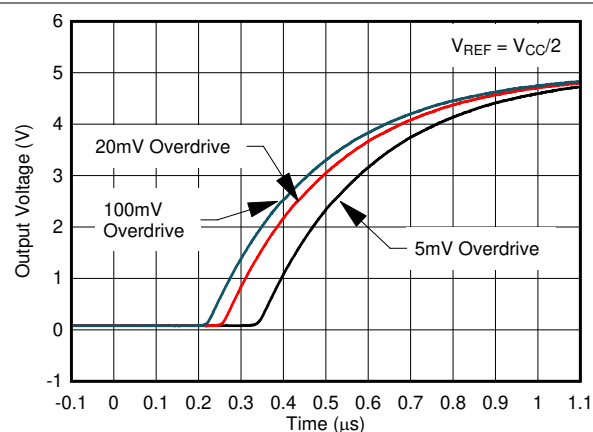


FIG 5-32. Response Time for Various Overdrives, Low-to-High Transition

6 Detailed Description

6.1 Overview

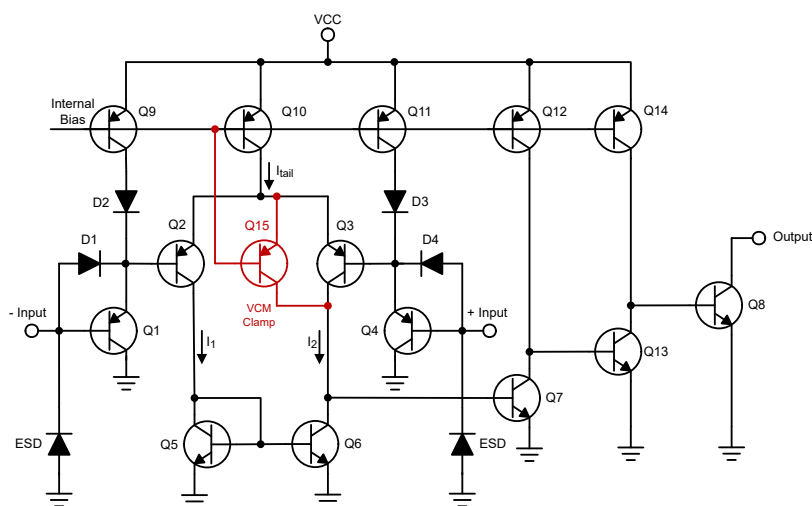
The LM2901-Q1 family is a quad comparator with the ability to operate up to 36V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to its very wide supply voltages range (2V to 36V), low I_q and fast response.

This device is AEC-Q100 qualified and can operate over a wide temperature range of -40°C to 125°C .

The open-drain output allows the user to configure the output's logic low voltage (V_{OL}) and can be utilized to enable the comparator to be used in AND functionality.

The "B" versions add dedicated ESD protections on all the pins for improved ESD performance as well as improved negative input voltage handling. Please see Application Note [SNOAA35](#) for more information

6.2 Functional Block Diagram Schematic (Each Comparator)



6.3 Feature Description

The comparator consists of a PNP darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing the comparator to accurately function from ground to $V_{CC} - 2\text{V}$ over temperature. On the non-B devices, a clamp was added around Q3 to mimic the both inputs above input voltage range behavior of the original classic silicon.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN sinks current when the negative input voltage is higher than the positive input voltage and the offset voltage. The V_{OL} is resistive and scales with the output current. Please see the "Output Low Voltage vs. Output Sinking Current" graphs for V_{OL} values with respect to the output current.

6.4 Device Functional Modes

6.4.1 Voltage Comparison

The LM2901-Q1 family of devices operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputs a logic low or high impedance (logic high with pullup) based on the input differential polarity.

7 Application and Implementation

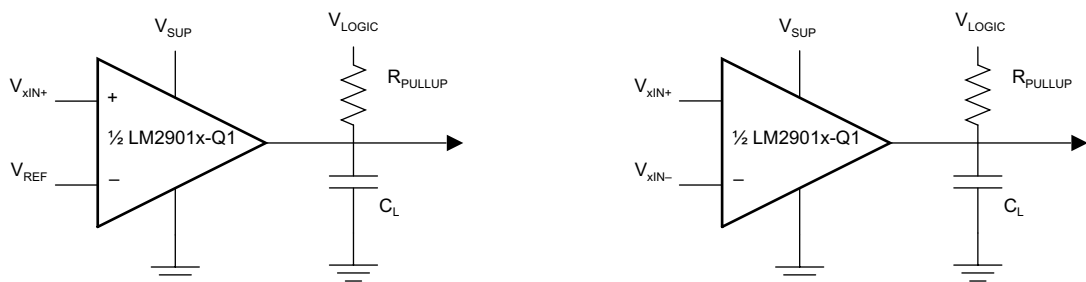
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7.1 Application Information

LM2901-Q1 family is typically used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LM2901-Q1 an excellent choice for level shifting to a higher or lower voltage.

7.2 Typical Application



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図 7-1. Single-Ended and Differential Comparator Configurations

7.2.1 Design Requirements

For this design example, use the parameters listed in 表 7-1 as the input parameters.

表 7-1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	0V to $V_{SUP} - 1.5V$
Supply voltage	2V to 36V
Logic supply voltage	2V to 36V
Output current (R_{PULLUP})	1 μA to 20mA
Input overdrive voltage	100mV
Reference voltage	2.5V
Load capacitance (C_L)	15pF

7.2.2 Detailed Design Procedure

7.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken into account. If temperature operation is above or below 25°C the V_{ICR} can range from 0V to $V_{CC} - 2.0V$. This limits the input voltage range to as high as $V_{CC} - 2.0V$ and as low as 0V. Operation outside of this range can yield incorrect comparisons.

Below is a list of input voltage situation and the outcomes:

1. When both IN- and IN+ are both within the common mode range:

- a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
 - b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
 3. When IN+ is higher than common mode and IN- is within common mode, the output is high impedance and the output transistor is not conducting
 4. When IN- and IN+ are both higher than common mode, see Section 2 of [Application Design Guidelines for LM339, LM393, TL331 Family Comparators Including the New B-versions](#).

7.2.2.2 Minimum Overdrive Voltage

The overdrive voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison the overdrive voltage (V_{OD}) must be higher than the input offset voltage (V_{IO}). The overdrive voltage can also determine the response time of the comparator, with the response time decreasing as the overdrive increases. [Figure 7-2](#) and [Figure 7-3](#) show positive and negative response times with respect to overdrive voltage.

7.2.2.3 Output and Drive Current

Output current is determined by the load/pull-up resistance and logic/pull-up voltage. The output current produces a output low voltage (V_{OL}) which is proportional to the output current. Use [Figure 5-19](#), [Figure 5-20](#), and [Figure 5-21](#) to determine V_{OL} based on the output current.

The output current can also effect the transient response. More is explained in the next section.

7.2.2.4 Response Time

The transient response can be determined by the load capacitance (C_L), load or pullup resistance (R_{PULLUP}), and equivalent collector-emitter resistance (R_{CE}).

Use [Equation 1](#) and [Equation 2](#) to calculate the approximate values of the rise time (t_r) and fall time (t_f).

$$t_P \approx R_{PULLUP} \times C_L \quad (1)$$

$$t_N \approx R_{CE} \times C_L \quad (2)$$

To find the value of R_{CE} , use the slope of [Figure 5-31](#) in the linear region at the desired temperature, or divide V_{OL} by I_O .

7.2.3 Application Curves

The following curves were generated with 5V on V_{CC} and V_{LOGIC} , $R_{PULLUP} = 5.1k\Omega$, and 50pF scope probe.

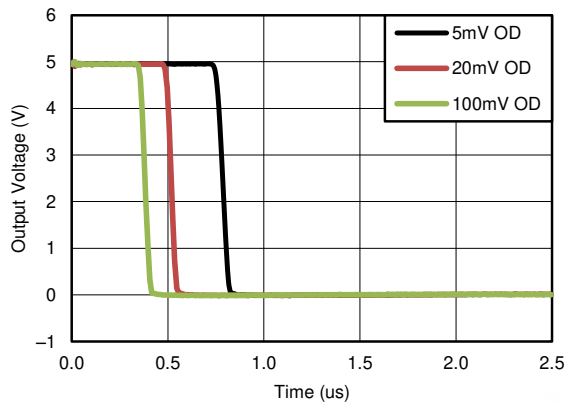


図 7-2. Response Time for Various Overdrives
Negative Transition

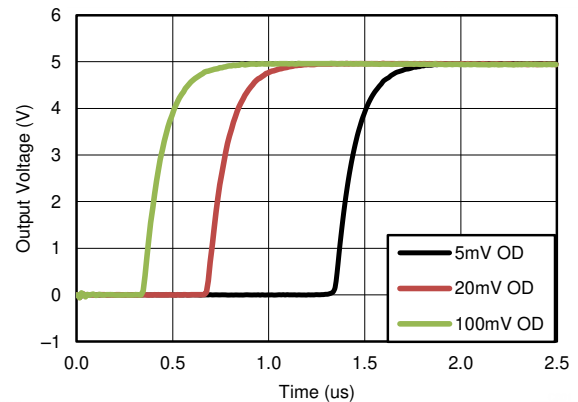


図 7-3. Response Time for Various Overdrives
Positive Transition

7.2.4 アプリケーション情報に関する免責事項

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7.3 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, TI recommends using a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can take away from some of the input common mode range of the comparator and create an inaccurate comparison.

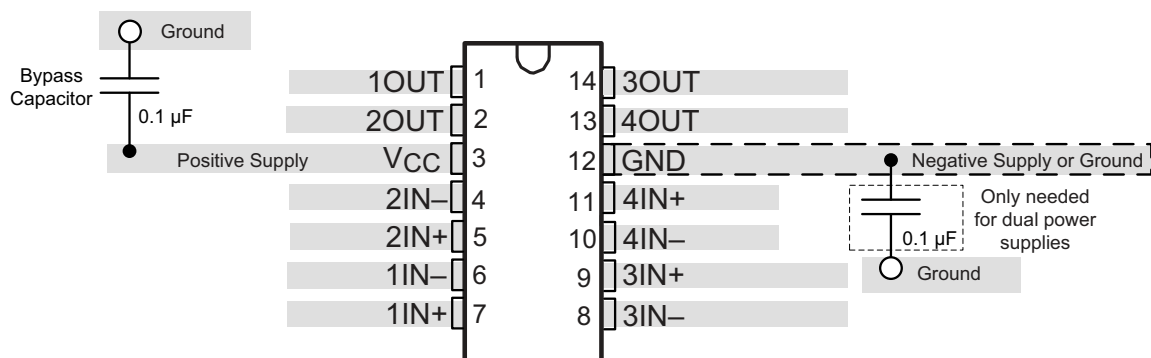
7.4 Layout

7.4.1 Layout Guidelines

For accurate comparator applications without hysteresis maintaining a stable power supply with minimized noise and glitches is critical. Best practice is to add a bypass capacitor between the supply voltage and ground. This can be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the GND pin and system ground.

Minimize coupling between outputs and inverting inputs to prevent output oscillations. Do not run output and inverting input traces in parallel unless there is a V_{CC} or GND trace between output and inverting input traces to reduce coupling. When series resistance is added to inputs, place resistor close to the device.

7.4.2 Layout Example



☒ 7-4. LM2901x-Q1 Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

TL331-Q1 *Single Differential Comparator*, [SLVS969](#)

8.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM2901-Q1	Click here	Click here	Click here	Click here	Click here
LM2901V-Q1	Click here	Click here	Click here	Click here	Click here
LM2901AV-Q1	Click here	Click here	Click here	Click here	Click here
LM2901B-Q1	Click here	Click here	Click here	Click here	Click here

8.3 Trademarks

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8.4 静電気放電に関する注意事項



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8.5 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (March 2023) to Revision H (May 2025)	Page
• Updated <i>Thermal Information</i> table.....	5
• Removed legacy device <i>Thermal</i> and <i>ESD Tables</i>	5
• Removed legacy device graphs.....	9
• Fixed duplicated Fig 5-4 graph.....	9
• Updated Functional Block Diagram and renamed to Schematic and updated Description text to include clamp.....	15

Changes from Revision F (May 2021) to Revision G (March 2023)	Page
• 最初のページの「特長」と「概要」のテキストを「B」バージョンに更新.....	1
• 最初のページの CDM ESD 分類を更新.....	1
• 最初のページに「ファミリ比較」表を追加.....	1
• Added "B" device description, electrical tables, graphs and pinouts throughout.....	5

Changes from Revision E (January 2015) to Revision F (May 2021)	Page
• 最初のページの HBM ESD 分類を更新.....	1
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
• Changed incorrect text in Apps Section Feature Description.....	15
• Changed incorrect Layout Example pinout.....	19

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2901AVQDRG4Q1	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 125	2901AVQ
LM2901AVQDRQ1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901AVQ
LM2901AVQDRQ1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901AVQ
LM2901AVQPWRG4Q1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901AVQ
LM2901AVQPWRG4Q1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901AVQ
LM2901AVQPWRQ1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901AVQ
LM2901AVQPWRQ1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901AVQ
LM2901BQDRQ1	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901BQ
LM2901BQDRQ1.A	Active	Production	SOIC (D) 14	3000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901BQ
LM2901BQPWRQ1	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901BQ
LM2901BQPWRQ1.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901BQ
LM2901BWRTERQ1	Active	Production	WQFN (RTE) 16	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901BQ
LM2901BWRTERQ1.A	Active	Production	WQFN (RTE) 16	5000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901BQ
LM2901QDRG4Q1	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 125	2901Q1
LM2901QDRQ1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901Q1
LM2901QDRQ1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901Q1
LM2901QPWRG4Q1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901Q1
LM2901QPWRG4Q1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901Q1
LM2901QPWRQ1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901Q1
LM2901QPWRQ1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901Q1
LM2901VQDRG4Q1	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 125	2901VQ1
LM2901VQDRQ1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901VQ1
LM2901VQDRQ1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901VQ1
LM2901VQPWRG4Q1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2901Q1, 2901VQ)
LM2901VQPWRG4Q1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2901Q1, 2901VQ)
LM2901VQPWRQ1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901VQ
LM2901VQPWRQ1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901VQ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM2901-Q1, LM2901AV-Q1, LM2901B-Q1, LM2901V-Q1 :

- Catalog : [LM2901](#), [LM2901AV](#), [LM2901B](#), [LM2901V](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

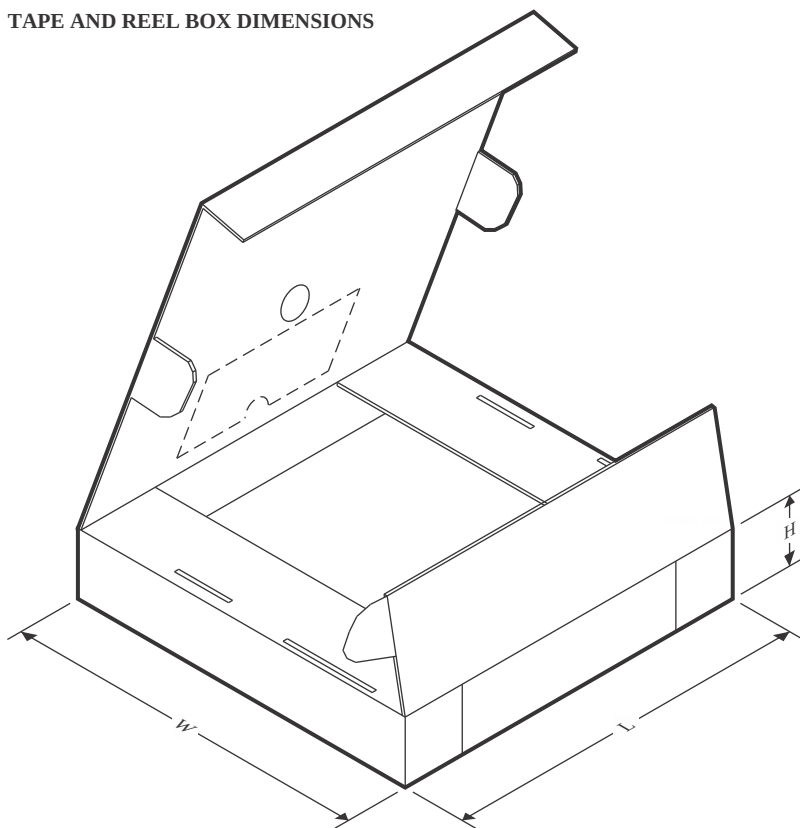
TAPE AND REEL INFORMATION



*All dimensions are nominal

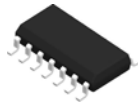
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2901AVQDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901AVQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901AVQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901AVQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901BQDRQ1	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901BQPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901BWRTERQ1	WQFN	RTE	16	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM2901QDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901VQDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901VQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901VQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901VQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

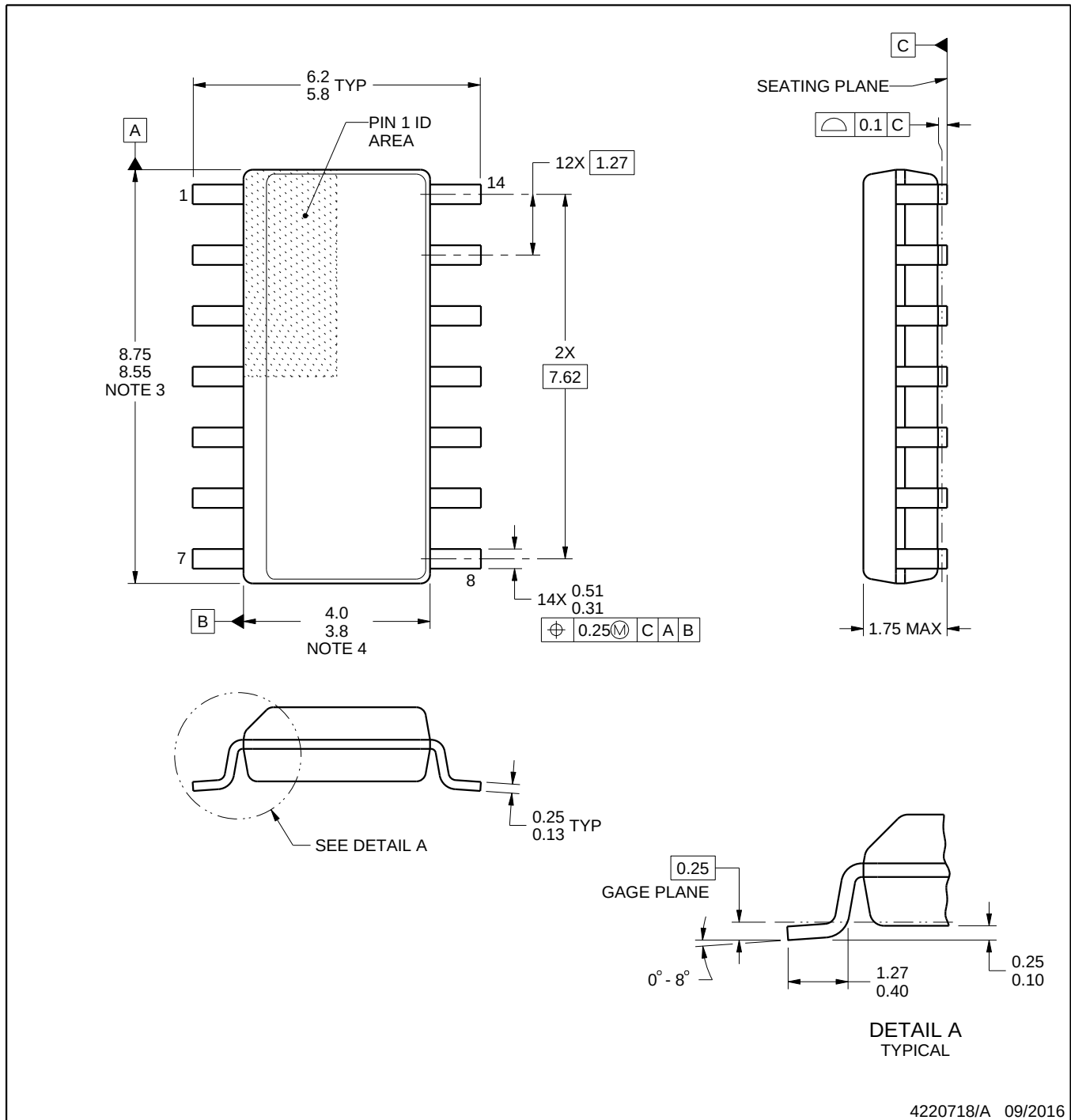


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2901AVQDRQ1	SOIC	D	14	2500	353.0	353.0	32.0
LM2901AVQPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901AVQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901AVQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901BQDRQ1	SOIC	D	14	3000	353.0	353.0	32.0
LM2901BQPWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0
LM2901BWRTERQ1	WQFN	RTE	16	5000	367.0	367.0	35.0
LM2901QDRQ1	SOIC	D	14	2500	353.0	353.0	32.0
LM2901QPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901VQDRQ1	SOIC	D	14	2500	353.0	353.0	32.0
LM2901VQPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901VQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901VQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

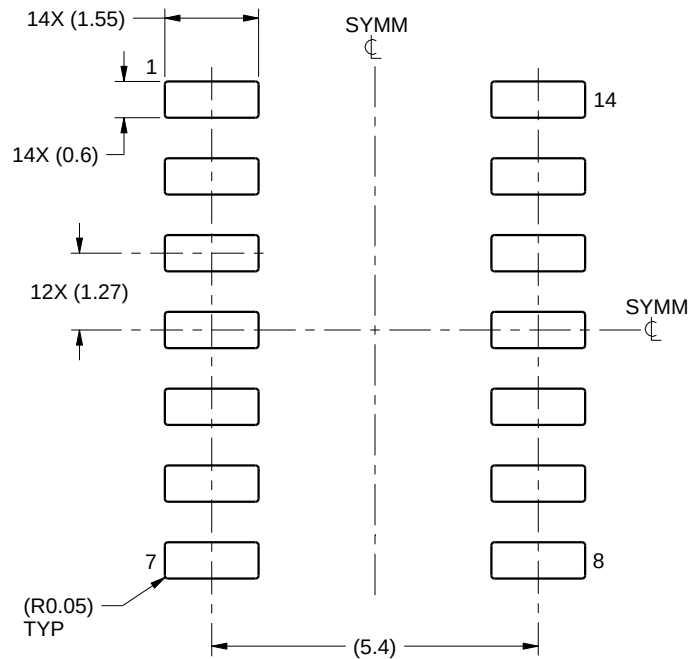
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

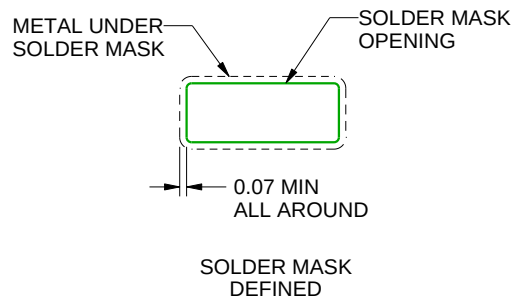
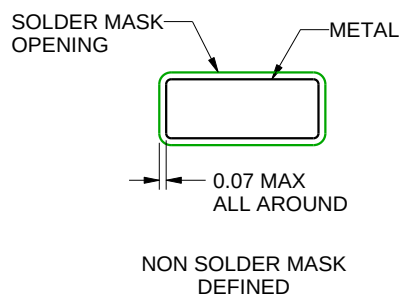
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

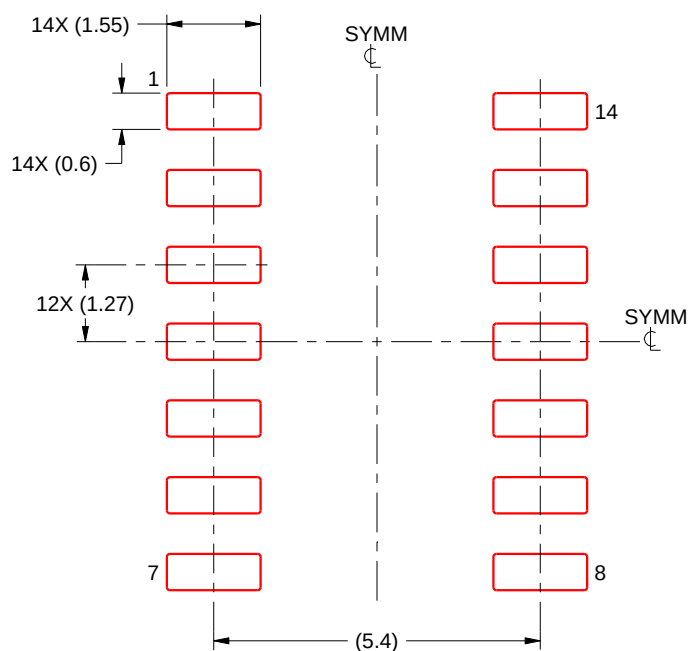
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

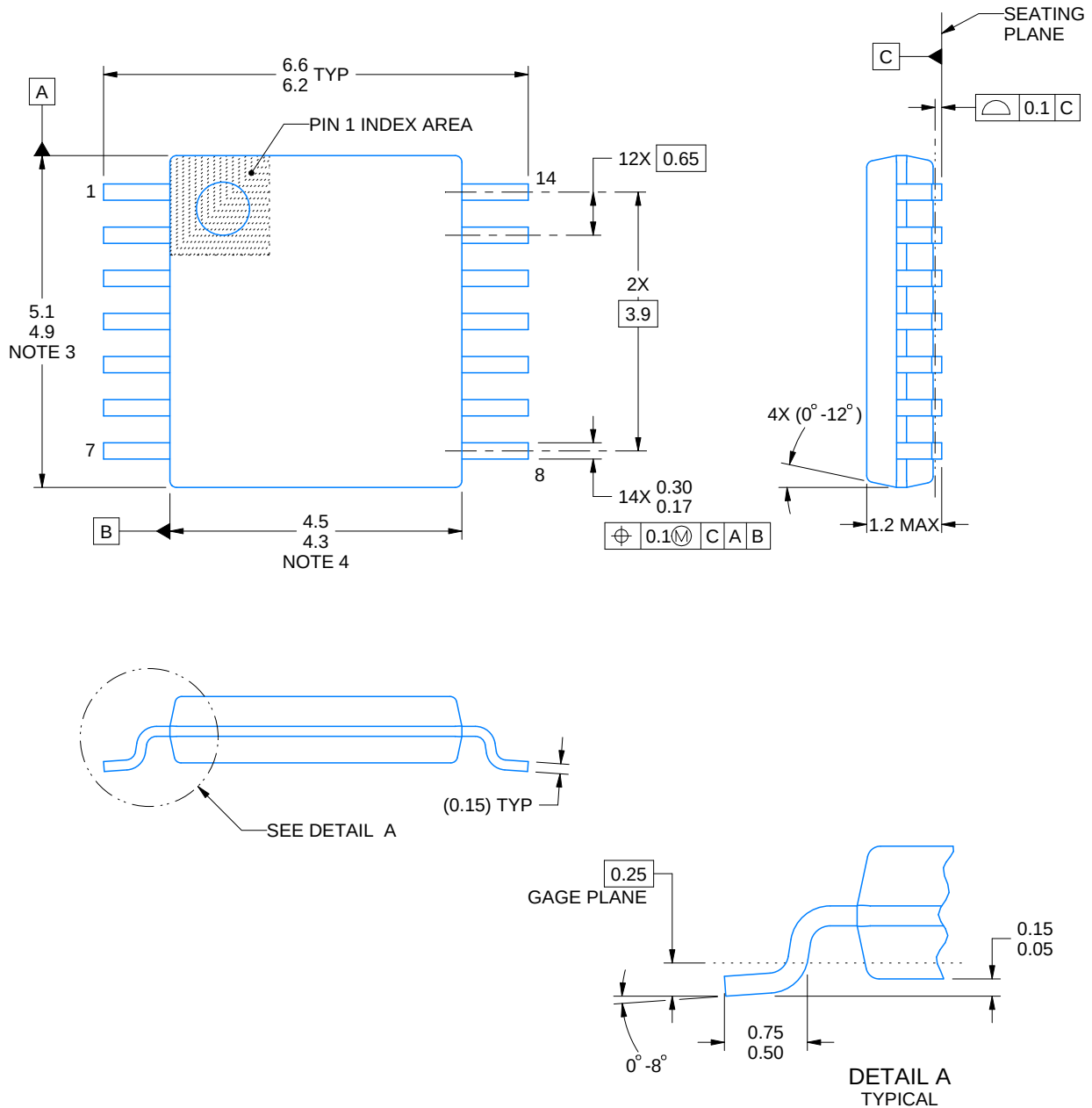
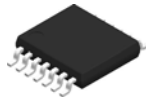


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220202/B 12/2023

NOTES:

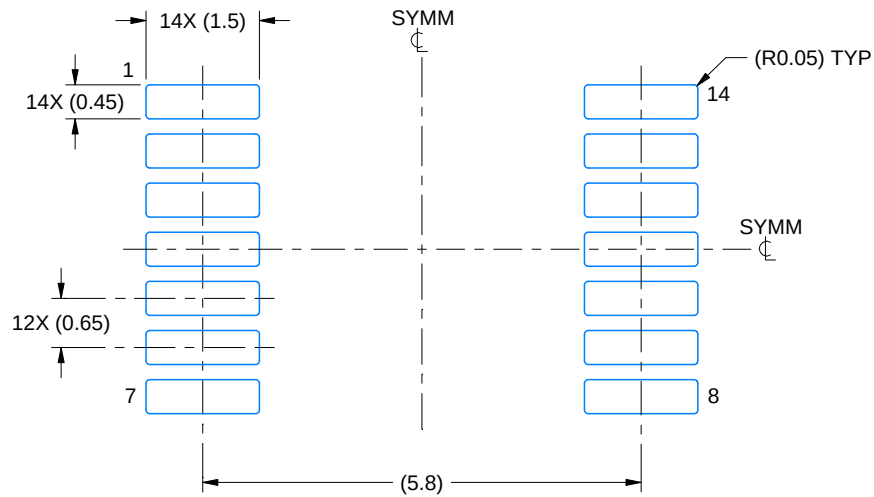
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

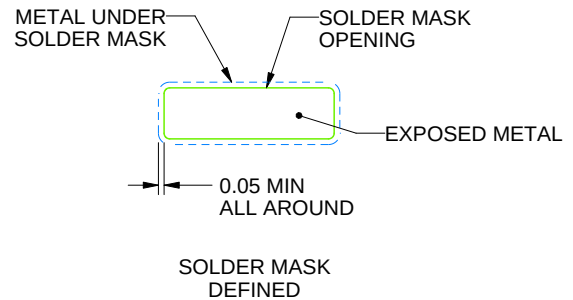
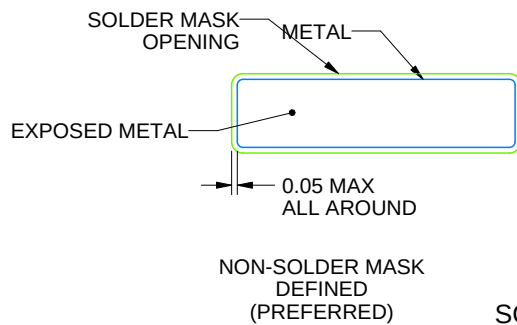
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

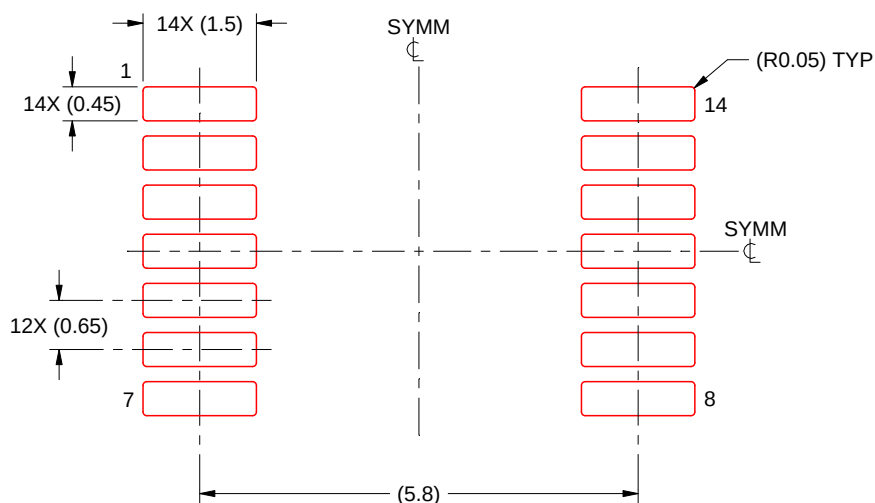
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

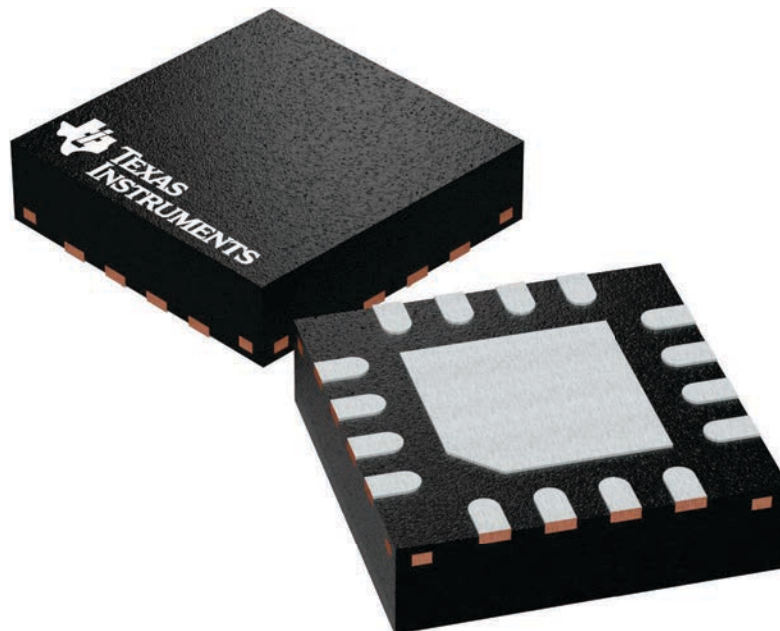
RTE 16

WQFN - 0.8 mm max height

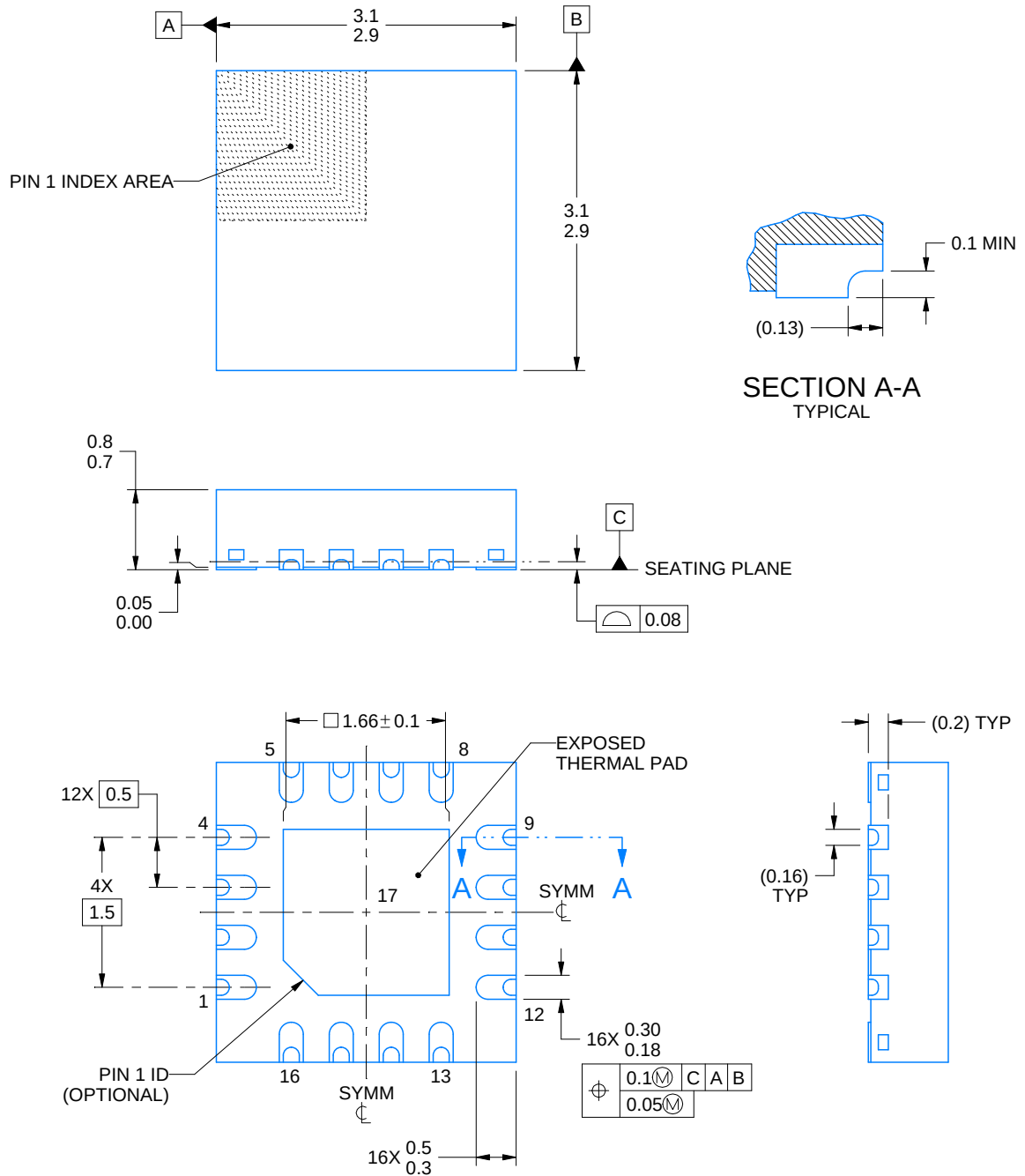
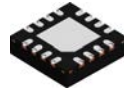
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225944/A



4224938/C 03/2022

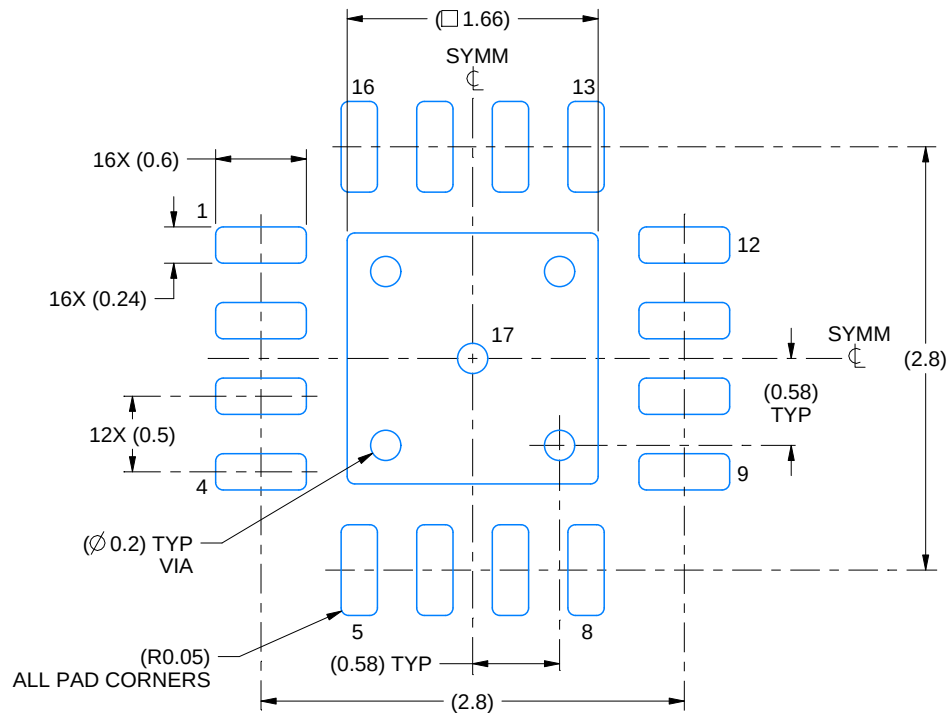
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

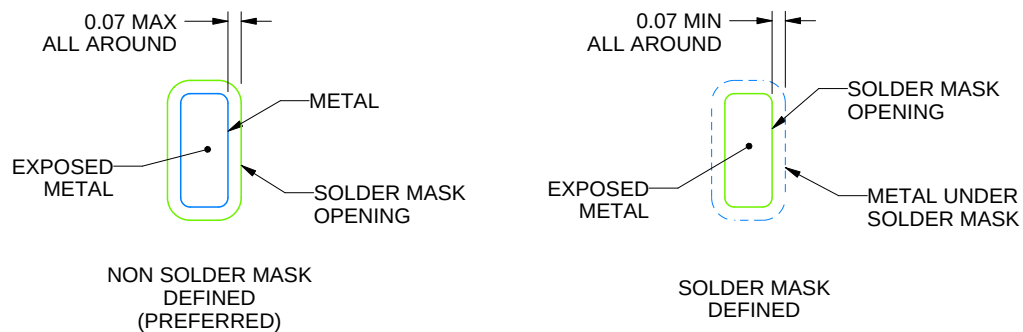
RTE0016K

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4224938/C 03/2022

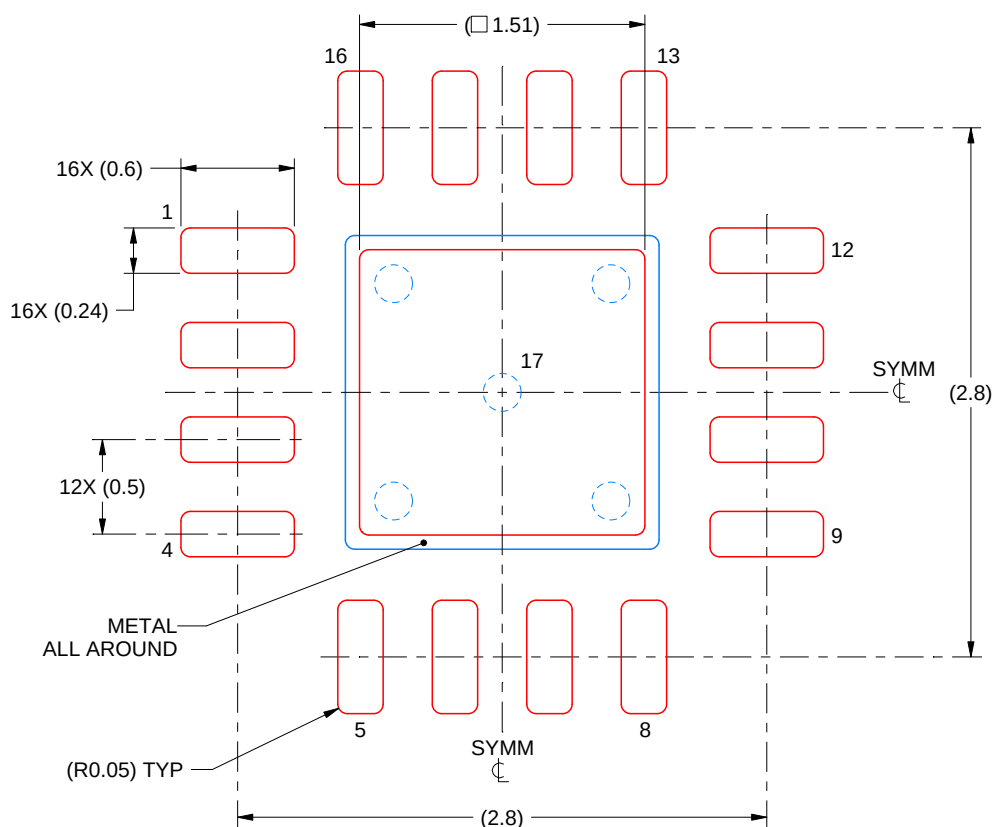
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RTE0016K

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224938/C 03/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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