LM27402 DCR電流センシング搭載の高性能同期整流降圧コントローラ

1 特長

- 3V～20Vの広い入力電圧範囲
- インダクタDCRまたはシャント抵抗ベースの過電流保護
- 0.6V基準電圧、-40℃～125℃の接合部温度範囲全体にわたって±1%のFB精度
- 200kHz～1.2MHzのスイッチング周波数
- 出力電圧は最大で入力電圧の95%
- 大電流MOSFETドライバを内蔵
- 内部のVDDバイアス電源LDOサブレギュレータ
- 外部クロック同期
- 外付けコンデンサによりソフトスタートを設定可能
- プリバイアス付きスタートアップ機能
- 電源トラッキング
- ライン・フィードフォワード付きの電圧モード制御
- オープン・ドレインのパワー・グッド・インジケータ
- ヒステリシス機能付きの高精度イネーブル
- 16ピンのHTSSOPおよびWQFNパッケージ
- WEBENCH® Power Designerにより、LM27402を使用するカスタム設計を作成

2 アプリケーション

- FPGAおよびASIC用の大電流、低電圧電源
- 汎用の大電流降圧コンバータ
- DC/DCコンバータおよびPOLモジュール
- テレコム、データコム、ネットワーク、分散電源アーキテクチャ
- 暗号通貨のマイニング(Bitcoin、Ethereum、Litecoin)

3 概要

LM27402は電圧モード、同期整流、DC/DC降圧型コントローラで、無損失のインダクタDCR電流センシング能力があります。インダクタの電流を検出することで、抵抗性のパワートレイン素子の追加が不要なため、全体の効率が向上し、正確で連続的な電流センシングが容易になります。0.6V ±1%の基準電圧により、高い精度と低電圧の出力を実現しています。LM27402の動作入力電圧範囲は3V～20Vで、広範な入力レールに適しています。

LM27402の電圧モード制御ループには入力電圧フィード・フォワードが組み込まれており、入力電圧の範囲全体にわたって安定性を維持します。スイッチング周波数は200kHz～1.2MHzの範囲で設定可能です。

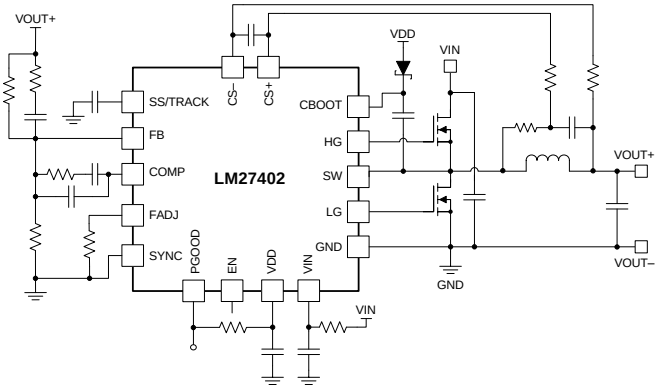
大電流のデュアル内蔵MOSFETドライバは、大きなQ_G、低い$R_{DS(on)}$のパワーMOSFETをサポートします。パワー・グッド・インジケータにより、電源レールのシーケンシングおよび出力のフォルト検出が可能です。可変の外部ソフトスタートにより、スタートアップ時に突入電流が制限され、単調性の出力制御が行われます。他の機能として、他の電源の外部トラッキング、内蔵のLDOバイアス電源、同期機能があります。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM27402	WQFN (16)	4.00mm×4.00mm
	HTSSOP (16)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーション回路



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision J (July 2015) から **Revision K** に変更 **Page**

- 「アプリケーション」に「暗号通貨のマイニング(Bitcoin、Ethereum、Litecoin)」を追加、WEBENCHのリンクを 追加 ... 1

Revision I (March 2013) から **Revision J** に変更 **Page**

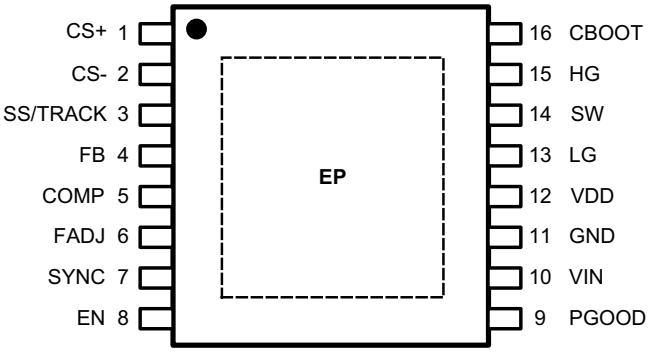
- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1

Revision H (March 2013) から **Revision I** に変更 **Page**

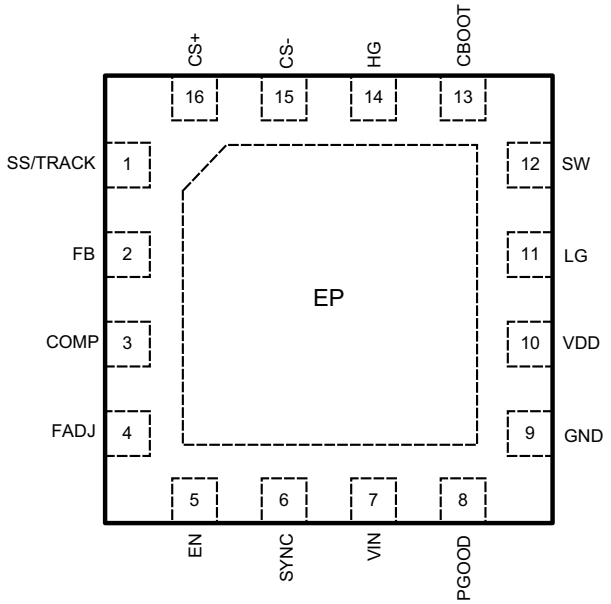
- Changed layout of National Semiconductor Data Sheet to TI format ... 36

5 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP
Top View



RUM Package
16-Pin WQFN
Top View



Pin Functions

PIN			I/O(1)	DESCRIPTION
NAME	HTSSOP	WQFN		
CBOOT	16	13	P	High-side gate driver supply rail. Connect a 100-nF ceramic capacitor from CBOOT to SW and a Schottky diode from VDD to CBOOT.
COMP	5	3	O	Output of the internal error amplifier. The COMP voltage is compared to an internally generated ramp at the PWM comparator to establish the duty cycle command.
CS+	1	16	I	Current sense positive input. This pin is the noninverting input to the current-sense comparator.
CS–	2	15	I	Current sense negative input. This pin is the inverting input to the current-sense comparator. 10-µA of nominal offset current is provided for adjustable current limit setpoint.
EN	8	5	I	LM27402 enable pin. Apply a voltage typically higher than 1.17 V to EN and the LM27402 will begin to switch if VIN and VDD have exceeded their UVLO thresholds. A hysteresis of 100 mV on EN provides noise immunity. EN is internally tied to VDD through a 2-µA pullup current source. EN must not exceed the voltage on VDD.
FADJ	6	4	I	Frequency adjust input. The switching frequency is programmable between 200 kHz and 1.2 MHz by connecting a resistor between FADJ and GND.
FB	4	2	I	Feedback input. Inverting input to the error amplifier to set the output voltage and compensate the voltage-mode control loop.
GND	11	9	G	Common ground connection. This pin provides the power and signal return connections for analog functions, including low-side MOSFET gate return, soft-start capacitor, and frequency adjust resistor.
HG	15	14	O	High-side MOSFET gate drive output.
LG	13	11	O	Low-side MOSFET gate drive output.
PGOOD	9	8	O	Power Good monitor output. This open-drain output goes low during overcurrent, short-circuit, UVLO, output overvoltage and undervoltage, overtemperature, or when the output is not regulated (such as an output prebias). An external pullup resistor to VDD or to an external rail is required. Included is a 20-µs deglitch filter. The PGOOD voltage should not exceed 5.5 V.

(1) P= Power, G = Ground, I = Input, O = Output

Pin Functions (continued)

PIN			I/O(1)	DESCRIPTION
NAME	HTSSOP	WQFN		
SS/TRACK	3	1	I/O	Soft-start or tracking input. A start-up rate is defined with the use of an external soft-start capacitor from SS/TRACK to GND. A +3-µA current source charges the soft-start capacitor to set the output voltage rise time during start-up. SS/TRACK can also be controlled with an external voltage source for tracking applications. SS/TRACK voltage must not exceed the voltage on VDD.
SW	14	12	P	Power stage switch-node connection and return path for the high-side gate driver.
SYNC	7	6	I	Frequency synchronization input. Apply an external clock signal to SYNC to set the switching frequency. The SYNC frequency must be greater than the frequency set by the FADJ pin. If the signal is not present, the switching frequency will decrease to the frequency set by the FADJ resistor. SYNC must not exceed the voltage on VDD and must be tied to GND if not used.
VDD	12	10	P	Internal sub-regulated 4.5-V bias supply. VDD is used to supply the voltage on CBOOT to facilitate high-side MOSFET switching. Connect a 1-µF ceramic capacitor from VDD to GND as close as possible to the LM27402. VDD cannot be connected to a separate voltage rail. However, VDD can be connected to VIN to provide increased gate drive only if $V_{IN} \leq 5.5$ V. Use A 1-Ω, 1-µF input filter for increased noise rejection.
VIN	10	7	P	Input voltage supply rail with an operating range is 3 V to 20 V. This input is used to provide the feedforward modulation for output voltage control and for generating the internal bias supply voltage. Decouple VIN to GND locally with a 1-µF ceramic capacitor. For better noise rejection, connect to the power stage input rail with an RC filter.
EP	–	–	P	Exposed pad. Connect this pad to the PCB GND plane using multiple thermal vias.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
VIN, CS+, CS–, SW to GND	–0.3	22	V
SW to GND less than 20ns Transients	–3	22	V
VDD, PGOOD to GND	–0.3	6	V
EN, SYNC, SS/TRACK, FADJ, COMP, FB, LG to GND	–0.3	V_{VDD}	V
CBOOT to GND	–0.3	24	V
CBOOT to SW	–0.3	6	V
CS+ to CS–	–2	2	V
Operating Junction Temperature	–40	150	°C
Lead Temperature (Soldering, 10 sec)		260	°C
Storage Temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Unless otherwise specified, voltages are from the indicated pins to GND.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor to each pin.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
VIN(1)	VDD powered by internal LDO	3.0	20	V
	VDD tied to VIN	3.0	5.5	
VDD		2.2	5.5	V
SS/TRACK, SYNC, EN		0	V_{VDD}	V
PGOOD		0	5.5	V
Junction Temperature		–40	125	°C

(1) VDD is the output of an internal linear regulator. Under normal operating conditions where VIN is greater than 5.5 V, VDD must not be connected to any external voltage source. In an application where VIN is between 3.0 V and 5.5 V, connecting VIN to VDD maximizes the bias supply rail voltage. In order to have better noise rejection under these conditions, a 1-Ω and 1-µF RC input filter to VDD may be used.

6.4 Thermal Information

THERMAL METRIC(1)		LM27402		UNIT
		RUM (WQFN)	PWP (HTSSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.3(2)	39.8(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.7	25.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.9	18.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.0	18.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.3	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Tested on a four layer JEDEC board. Four vias are provided under the WQFN exposed pad and nine vias are provided under the HTSSOP exposed pad.

6.5 Electrical Characteristics

Unless otherwise stated, the following conditions apply: V_{VIN} = 12 V. Limits in standard type are for T_J = 25°C only. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATIONAL SPECIFICATIONS						
I_Q	Quiescent Current	V_{FB} = 0.6 V (not switching), T_J = 25°C		4.5		mA
		V_{FB} = 0.6 V (not switching), T_J = –40°C to +125°C			6	
I_{QSD}	Quiescent Current In Shutdown	V_{EN} = 0 V, T_J = 25°C		25		µA
		V_{EN} = 0 V, T_J = –40°C to +125°C			45	
UVLO						
UVLO	Input Under Voltage Lockout	V_{VIN} Rising, V_{VDD} Rising, T_J = 25°C		2.9		V
		V_{VIN} Rising, V_{VDD} Rising, T_J = –40°C to +125°C	2.7		2.99	
$UVLO_{HYS}$	UVLO Hysteresis	V_{VIN} Falling, V_{VDD} Falling		300		mV
REFERENCE						
V_{FB}	Feedback Voltage	T_J = 25°C		0.600		V
		T_J = –40°C to +125°C	0.594		0.606	
I_{FB}	Feedback Pin Bias Current	V_{FB} = 0.65 V	–50	0	50	nA

Electrical Characteristics (continued)

Unless otherwise stated, the following conditions apply: V_{VIN} = 12 V. Limits in standard type are for T_J = 25°C only. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING						
F_{SW}	Switching Frequency	R_{FADJ} = 4.12 kΩ, T_J = 25°C		1150		kHz
		R_{FADJ} = 4.12 kΩ, T_J = –40°C to +125°C	950		1350	
		R_{FADJ} = 20 kΩ, T_J = 25°C		500		kHz
		R_{FADJ} = 4.12 kΩ, T_J = –40°C to +125°C	400	0	600	
		R_{FADJ} = 95.3 kΩ, T_J = 25°C		214		kHz
		R_{FADJ} = 4.12 kΩ, T_J = –40°C to +125°C	175		265	
D_{MAX}	Maximum Duty Cycle	F_{SW} = 300 kHz, T_J = 25°C		95%		
		F_{SW} = 300 kHz, T_J = –40°C to +125°C	93%			
VDD SUB-REGULATOR						
V_{DD}	Sub-Regulator Output Voltage	I_{DD} = 25 mA, T_J = 25°C		4.5		V
		I_{DD} = 25 mA, T_J = –40°C to +125°C	4		5	
ERROR AMPLIFIER						
BW_{-3dB}	Open Loop Bandwidth			2		MHz
A_{VOL}	Error Amp DC Gain			50		dB
V_{SLEW_RISE}	Error Amplifier Rising Slew Rate	V_{FB} = 0.5 V		5		V/µs
V_{SLEW_FALL}	Error Amplifier Falling Slew Rate	V_{FB} = 0.7 V		3		V/µs
I_{SOURCE}	COMP Source Current	V_{FB} = 0.5 V	8	12		mA
I_{SINK}	COMP Sink Current	V_{FB} = 0.7 V	4	12		mA
V_{COMP_MAX}	Max COMP Voltage	V_{FB} = 0.5 V		3.1		V
V_{COMP_MIN}	Min COMP Voltage	V_{FB} = 0.7 V		0.5		V
OVER CURRENT						
V_{OFFSET}	Comparator Voltage Offset	T_J = 25°C		0		mV
		T_J = –40°C to +125°C	–5		5	
I_{CS-}	Current Limit Offset Current	V_{CS-} = 5 V, T_J = 25°C		10		µA
		V_{CS-} = 5 V, T_J = –40°C to +125°C	9.5		10.5	
GATE DRIVE						
R_{DSON1}	High-Side FET Driver pullup On Resistance	$V_{CBOOT} – V_{SW}$ = 4.7 V, I_{HG} = +100 mA		1.7		Ω
R_{DSON2}	High-Side FET Driver pulldown On Resistance	$V_{CBOOT} – V_{SW}$ = 4.7 V, I_{HG} = –100 mA		1.2		Ω
R_{DSON3}	Low-Side FET Driver pullup On Resistance	V_{VDD} = 4.7 V, I_{LG} = +100 mA		1.7		Ω
R_{DSON4}	Low-Side FET Driver pulldown On Resistance	V_{VDD} = 4.7 V, I_{LG} = –100 mA		1		Ω
SOFT-START						
I_{SS}	Soft-Start Source Current	$V_{SS/TRACK}$ = 0 V, T_J = 25°C		3		µA
		$V_{SS/TRACK}$ = 0 V, T_J = –40°C to +125°C	2		4	
R_{SS_PD}	Soft-Start pulldown Resistance	$V_{SS/TRACK}$ = 0.6 V		288		Ω

Electrical Characteristics (continued)

Unless otherwise stated, the following conditions apply: V_{VIN} = 12 V. Limits in standard type are for T_J = 25°C only. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWERGOOD						
I_{PGS}	PGOOD Low Sink Current	V_{PGOOD} = 0.2 V, V_{FB} = 0.75 V, T_J = 25°C	60			µA
		V_{PGOOD} = 0.2 V, V_{FB} = 0.75 V, T_J = –40°C to +125°C	0	100		
I_{PGL}	PGOOD Leakage Current	V_{PGOOD} = 5 V		1	10	µA
O_{VT}	Overvoltage Threshold	V_{FB} Rising, T_J = 25°C		117%		
		V_{FB} Rising, T_J = –40°C to +125°C	114%		120%	
O_{VT_HYS}	O_{VT} Hysteresis	V_{FB} Falling		2%		
U_{VT}	Undervoltage Threshold	V_{FB} Rising , T_J = 25°C		94%		
		V_{FB} Rising, T_J = –40°C to +125°C	91%		97%	
U_{VT_HYS}	U_{VT} Hysteresis	V_{FB} Falling		3%		
ENABLE						
V_{EN}	Enable Logic High Threshold	V_{EN} Rising, T_J = 25°C		1.17		V
		V_{EN} Rising, T_J = –40°C to +125°C	1.10		1.24	
V_{EN_HYS}	Enable Hysteresis	V_{EN} Falling		100		mV
I_{EN}	Enable Pin pullup Current	V_{EN} = 0 V		2		µA
FREQUENCY SYNCHRONIZATION						
V_{LH_SYNC}	SYNC Pin Logic High	V_{VDD} = 4.7 V, T_J = –40°C to +125°C	2.0			V
V_{LL_SYNC}	SYNC Pin Logic Low	V_{VDD} = 4.7 V, T_J = –40°C to +125°C			0.8	V
$SYNC_{FSW\_L}$	Minimum Clock Sync Frequency	T_J = –40°C to +125°C	200			kHz
$SYNC_{FSW\_H}$	Maximum Clock Sync Frequency	T_J = –40°C to +125°C			1200	kHz
THERMAL SHUTDOWN						
T_{SHD}	Thermal Shutdown	Temperature Rising		165		°C
T_{SHD_HYS}	Thermal Shutdown Hysteresis	Temperature Falling		15		°C

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
SOFT-START						
T_{SS_INT}	Internal Soft-Start Time			1.28		ms
POWERGOOD						
$T_{DEGLITCH}$	Deglitch Time	V_{PGOOD} Rising and Falling		20		µs

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING						
T_{OFF_MIN}	Minimum Off Time	V_{FB} = 0.5 V, T_J = 25°C		165		ns
		V_{FB} = 0.5 V, T_J = –40°C to +125°C	125	5	205	
GATE DRIVE						
T_{DT}	Deadtime Timeout	F_{SW} = 500 kHz		40		ns

6.8 Typical Performance Characteristics

Unless otherwise stated, all data sheet curves were recorded using *Example Circuit 1*. V_{IN} = 12 V.

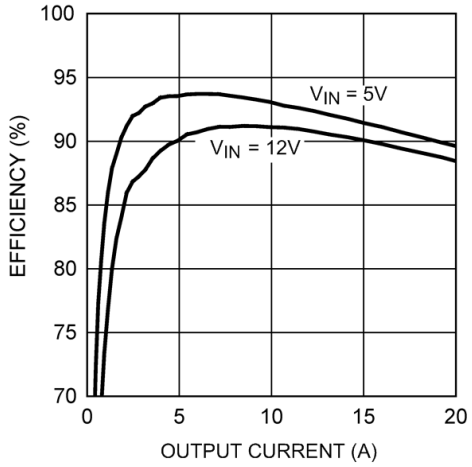


Figure 1. Efficiency (V_{out} = 1.5 V)

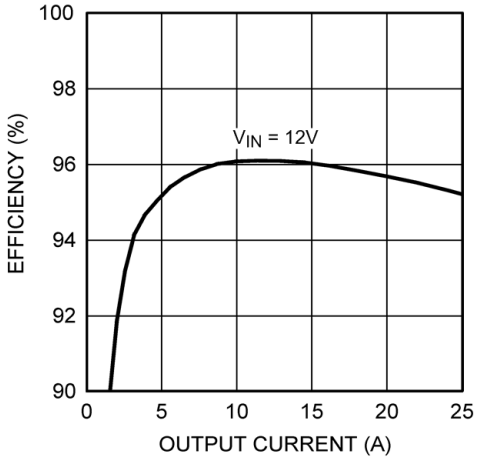


Figure 2. Efficiency (V_{out} = 5 V, *Example Circuit 2*)

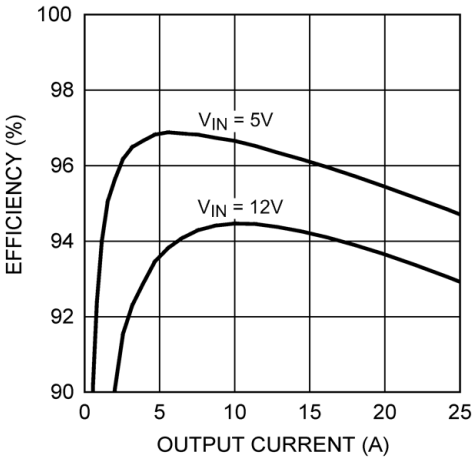


Figure 3. Efficiency (V_{out} = 3.3 V, *Example Circuit 2*)

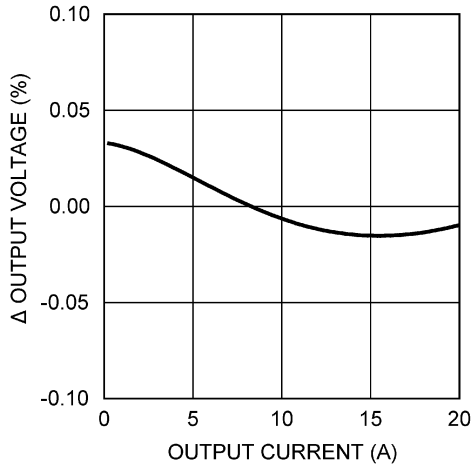


Figure 4. Load Regulation (V_{out} = 1.5 V)

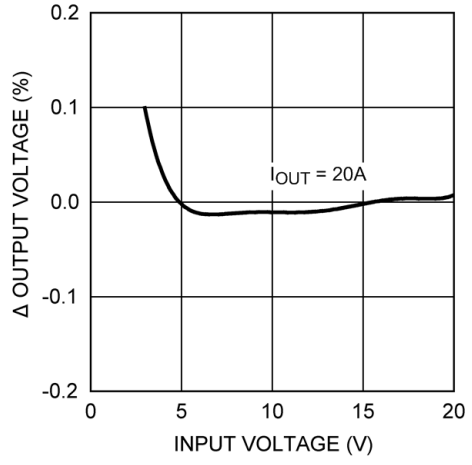


Figure 5. Line Regulation (V_{out} = 1.5 V)

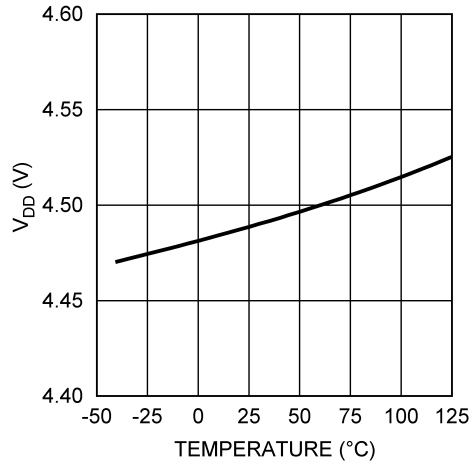


Figure 6. VDD Voltage vs Temperature (I_{VDD} = 25 mA)

Typical Performance Characteristics (continued)

Unless otherwise stated, all data sheet curves were recorded using *Example Circuit 1*. V_{IN} = 12 V.

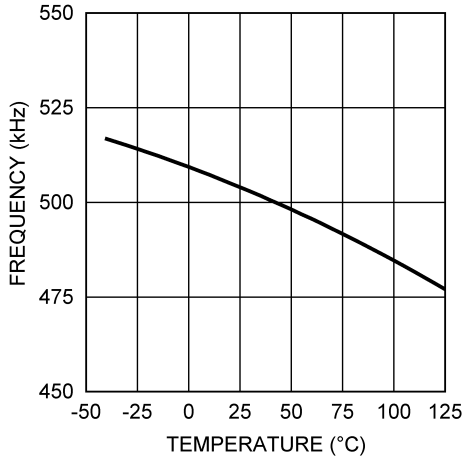


Figure 7. Frequency vs Temperature (R_{FADJ} = 20 kΩ)

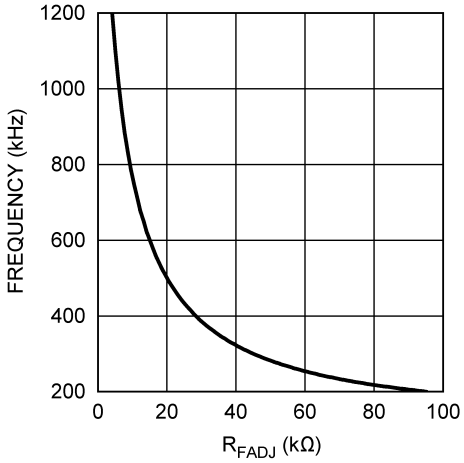


Figure 8. Frequency vs R_{FADJ}

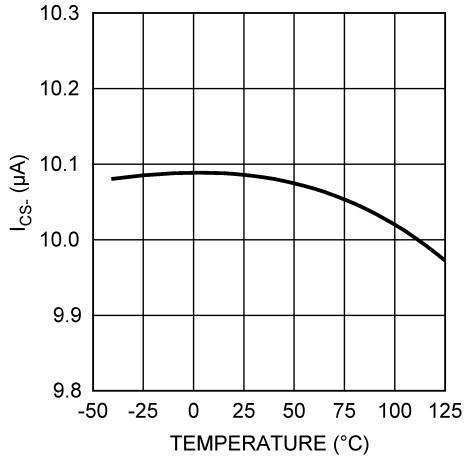


Figure 9. CS– Current Source vs Temperature

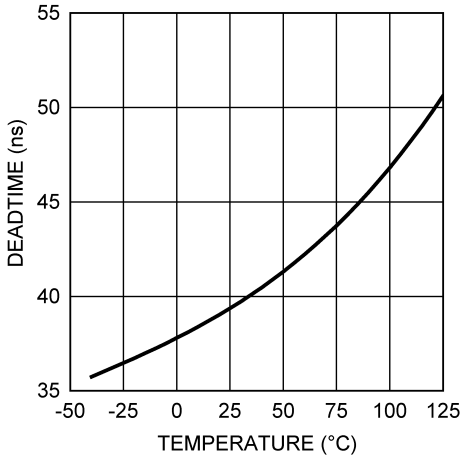


Figure 10. Deadtime vs Temperature

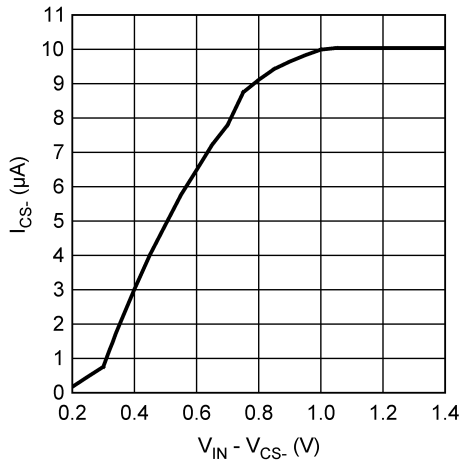
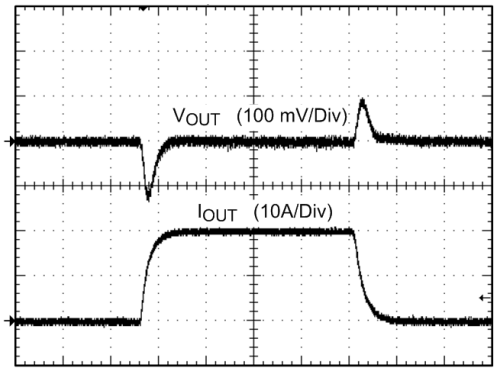


Figure 11. CS– Current Source Compliance Voltage

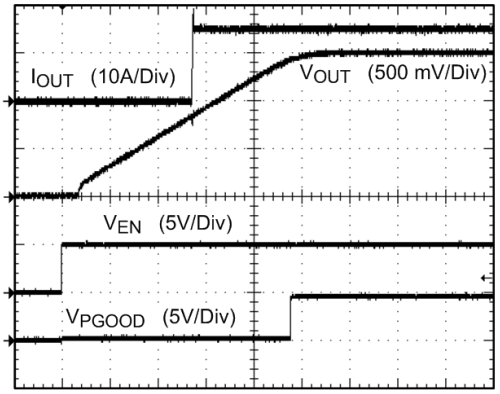


Horizontal Scale: 100 µs/DIV

Figure 12. Load Transient

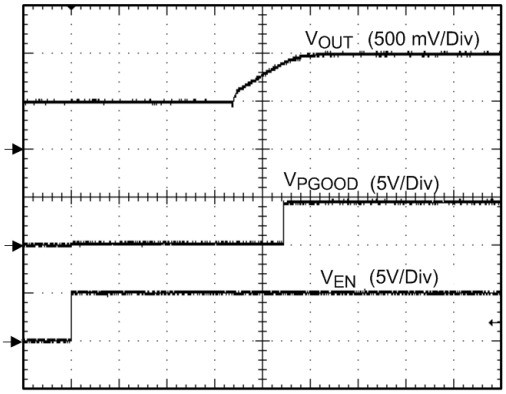
Typical Performance Characteristics (continued)

Unless otherwise stated, all data sheet curves were recorded using *Example Circuit 1*. V_{IN} = 12 V.



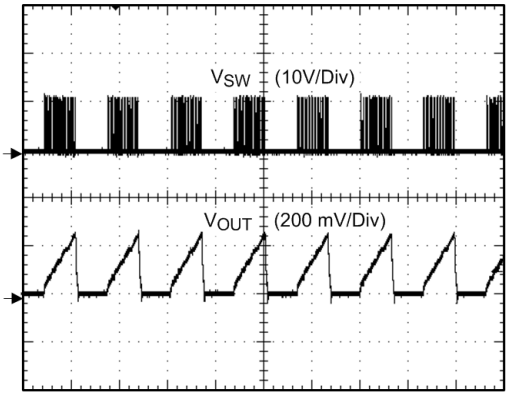
Horizontal Scale: 2 ms/DIV

Figure 13. Start-up Waveforms



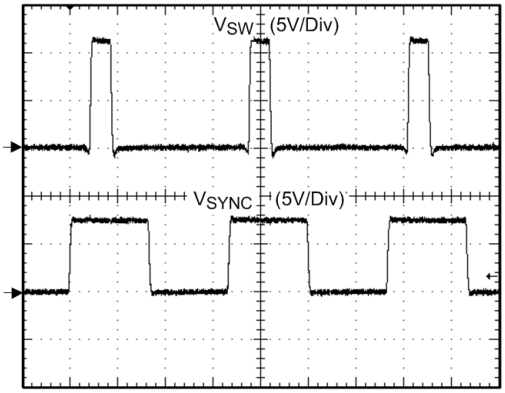
Horizontal Scale: 2 ms/DIV

Figure 14. Pre-Bias Start-up



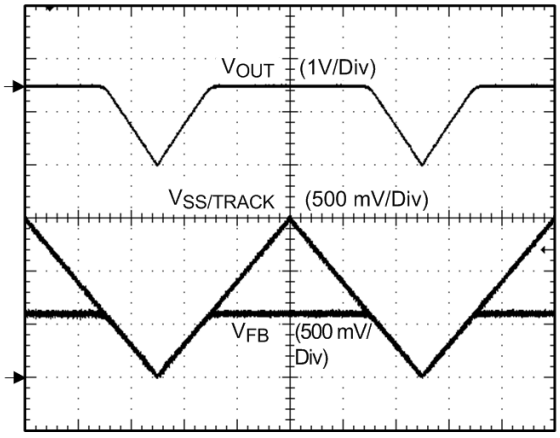
Horizontal Scale: 2 ms/DIV

Figure 15. OCP Hiccup



Horizontal Scale: 400 ns/DIV

Figure 16. Frequency Synchronization



Horizontal Scale: 2 ms/DIV

Figure 17. Tracking

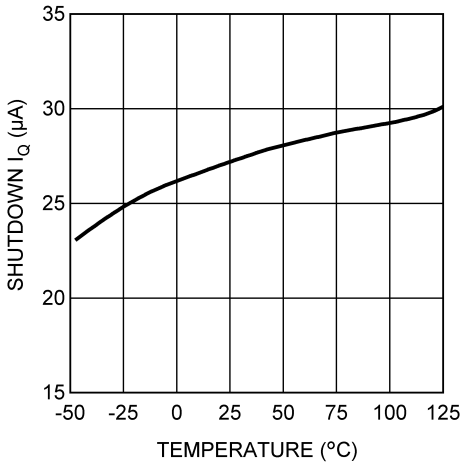


Figure 18. Shutdown Quiescent Current vs Temperature

Typical Performance Characteristics (continued)

Unless otherwise stated, all data sheet curves were recorded using *Example Circuit 1*. V_{IN} = 12 V.

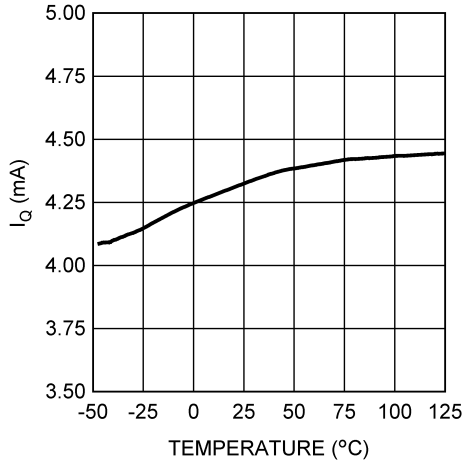


Figure 19. Quiescent Current vs Temperature

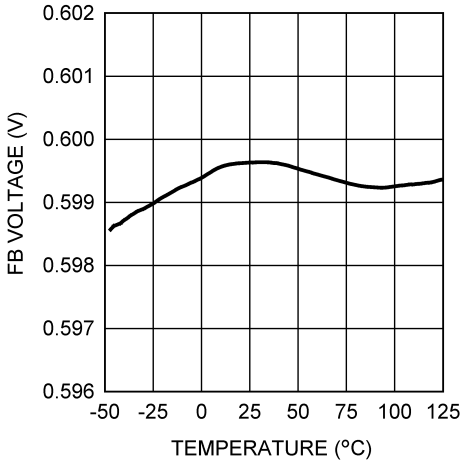


Figure 20. Feedback Voltage vs Temperature

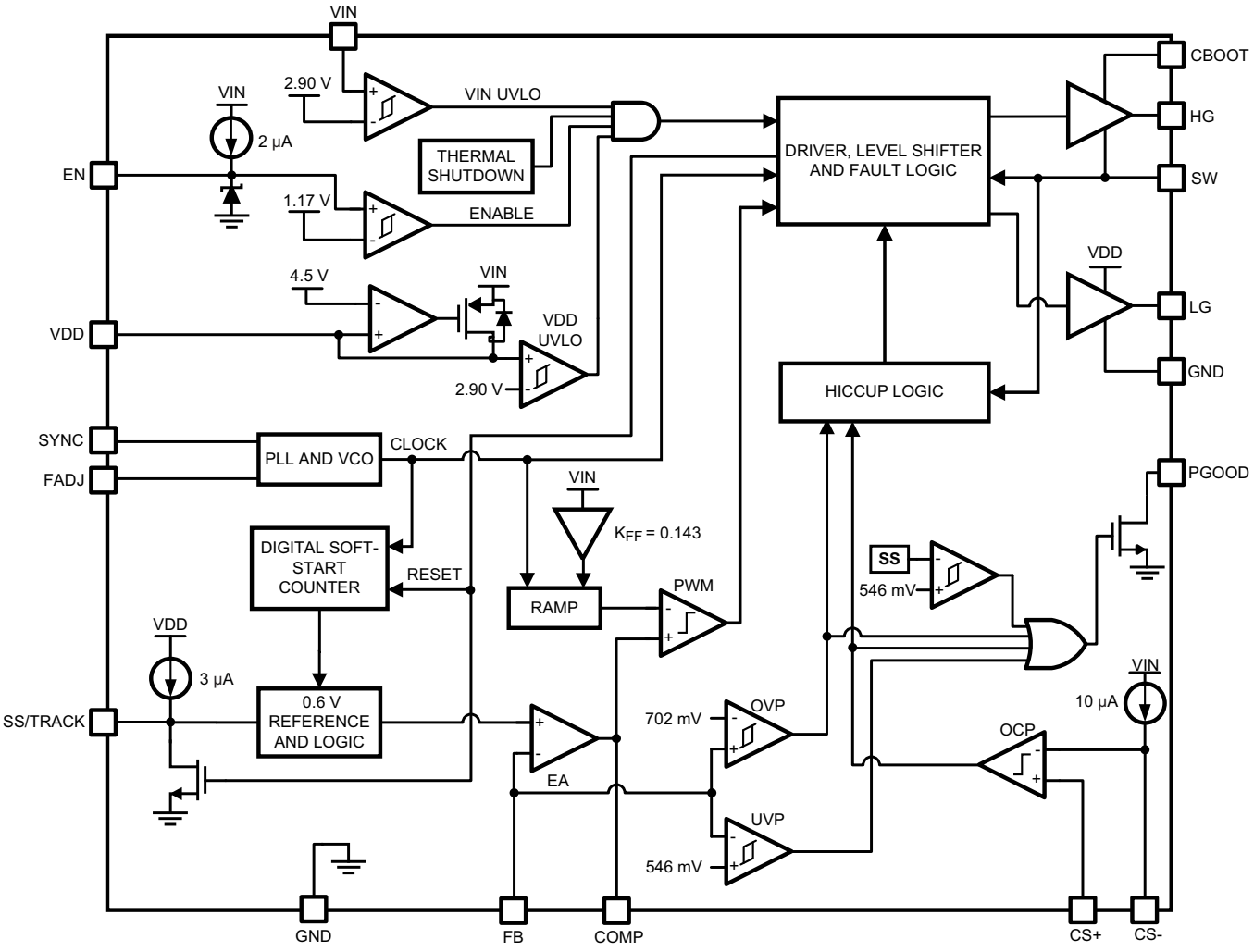
7 Detailed Description

7.1 Overview

The LM27402 is a feature-rich, easy-to-use, single-phase, synchronous PWM DC/Dc step-down controller capable of providing an ultrahigh current output for demanding POL applications. An input voltage range of 3 V to 20 V is compatible with a wide range of intermediate bus system rails and battery chemistries, especially 3.3-V, 5-V, and 12-V inputs. The output voltage is adjustable from 0.6 V to as high as 95% of the input voltage, with better than ±1% feedback system regulation accuracy over the full junction temperature range. With an adjustable inductor DCR based current limit setpoint, ferrite and composite cored inductors with low DCR and small footprint can be specified to maximize efficiency and reduce power loss. High-current gate drivers with adaptive deadtime are used for the high-side and low-side power MOSFETs to provide further efficiency gains.

The LM27402 employs a voltage-mode control loop with input voltage feedforward to accurately regulate the output voltage over substantial load, line, and temperature ranges. The switching frequency is programmable between 200 kHz and 1.2 MHz through a resistor or an external synchronization signal. The LM27402 is available in thermally-enhanced WQFN-16 and HTSSOP-16 packages with 0.65-mm lead pitch. The device offers high levels of integration by including MOSFET gate drivers, a low dropout (LDO) bias supply regulator, and comprehensive fault protection features to enable highly flexible, reliable, energy-efficient, and high density regulator solutions. Multiple fault conditions are accommodated, including overvoltage, undervoltage, overcurrent, and overtemperature.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Wide Input Voltage Range

The LM27402 operating input voltage range is from 3 V to 20 V. The device is intended for POL conversions from 3.3-V, 5-V, and 12-V unregulated, semiregulated and fully regulated supply rails. It is also suitable for connection to intermediate bus converters with output rails centered at 12 V and 9.6 V (derived from 4:1 and 5:1 primary-secondary transformer step-downs in nonregulated full-bridge converter topologies) and voltage levels intrinsic to a wide variety of battery chemistries.

The LM27402 uses an internal LDO subregulator to provide a 4.5-V bias rail for the gate drive and control circuits (assuming the input voltage is higher than 4.5 V plus the necessary subregulator dropout specification). Naturally, it can be more favorable to connect VDD directly to the input during low input voltage operation (V_{VIN} < 5.5 V). In summary, connecting VDD to VIN during low input voltage operation provides a greater gate drive voltage level and thus an inherent efficiency benefit. However, by virtue of the low subregulator dropout voltage, this VDD to VIN connection is not mandatory, thus enabling input ranges from 3 V up to 20 V.

In general, the subregulator is rated to drive the two internal gate driver stages in addition to the quiescent current associated with the operation of the LM27402. VDD and VIN pins of the LM27402 can be tied together if the input voltage is ensured not to exceed 5.5 V (absolute maximum 6 V). This connection bypasses the internal LDO bias regulator and eliminates the LDO dropout voltage and power dissipation. An RC filter from the input rail to the VIN pin, for example 2.2 Ω and 1 µF, presents supplementary filtering at the VIN pin. Low gate threshold voltage MOSFETs are recommended for this configuration.

7.3.2 UVLO

An undervoltage lockout is built into the LM27402 that allows the device to only switch if the input voltage (VIN) and the internal sub-regulated voltage (VDD) both exceed 2.9 V. A UVLO hysteresis of 300 mV on both VDD and VIN prevents power-on and -off anomalies related to input voltage deviations.

7.3.3 Precision Enable

The EN pin of the LM27402 allows the output to be toggled on and off and is a precision analog input. When the EN voltage exceeds 1.17 V, the controller initiates the soft-start sequence as long as the input voltage and sub-regulated voltage have exceeded their UVLO thresholds of 2.9 V. The EN pin has an absolute maximum voltage rating of 6.0 V and should not exceed the voltage on VDD. There is an internal 2 µA pullup current source connected to the EN pin. If EN is open, the LM27402 turns on automatically if VIN and VDD exceed 2.9 V. If the EN voltage is held below 0.8 V, the LM27402 enters a deep shutdown state where the internal bias circuitry is off. The quiescent current is approximately 35 µA in deep shutdown. The EN pin has 100 mV of hysteresis to reject noise and allow the pin to be resistively coupled to the input voltage or sequenced with other rails.

7.3.4 Soft-Start and Voltage Tracking

When the EN pin exceeds 1.17 V and both VIN and VDD exceed their UVLO thresholds, the LM27402 begins charging the output linearly to the voltage level dictated by the feedback resistor network. The soft-start time is set by connecting a capacitor from SS/TRACK to GND. After EN exceeds 1.17 V, an internal 3-µA current source begins to linearly charge the soft-start capacitor. Soft-start allows the user to limit inrush currents related to high output capacitance and output slew rate. If a soft-start capacitor is not used, the LM27402 defaults to a digitally-controlled star-tup time of 1.28 ms. The SS/TRACK pin can also be used to ratiometrically or coincidentally track an external voltage source. See the *Setting the Soft-Start Time* and *Tracking* sections for more information.

7.3.5 Output Voltage Setpoint and Accuracy

The reference voltage seen at the FB pin is set at 0.6 V, and a feedback system accuracy of ±1% over the full junction temperature range is met. Junction temperature range for the LM27402 is –40°C to +125°C. While somewhat dependent on frequency and load current levels, the LM27402 is generally capable of providing output voltages in the range of 0.6 V to a maximum of greater than 90% VIN. The dc output voltage during normal operation is set by the feedback resistor network connected to VOUT.

Feature Description (continued)

7.3.6 Voltage-Mode Control

The LM27402 incorporates a voltage-mode control loop implementation with input voltage feedforward to eliminate the input voltage dependence of the PWM modulator gain. This configuration allows the controller to maintain stability throughout the entire input voltage operating range and provides for optimal response to input voltage transient disturbances. The constant gain provided by the controller greatly simplifies feedback loop design because loop characteristics remain constant as the input voltage changes, unlike a buck converter without voltage feedforward. An increase in input voltage is matched by a concomitant increase in ramp voltage amplitude to maintain constant modulator gain. The input voltage feedforward gain, k_{FF}, is 1/7, equivalent to the ramp amplitude divided by the input voltage, V_{RAMP}/V_{IN}. See the *Control Loop Compensation* section for more detail.

7.3.7 Power Good

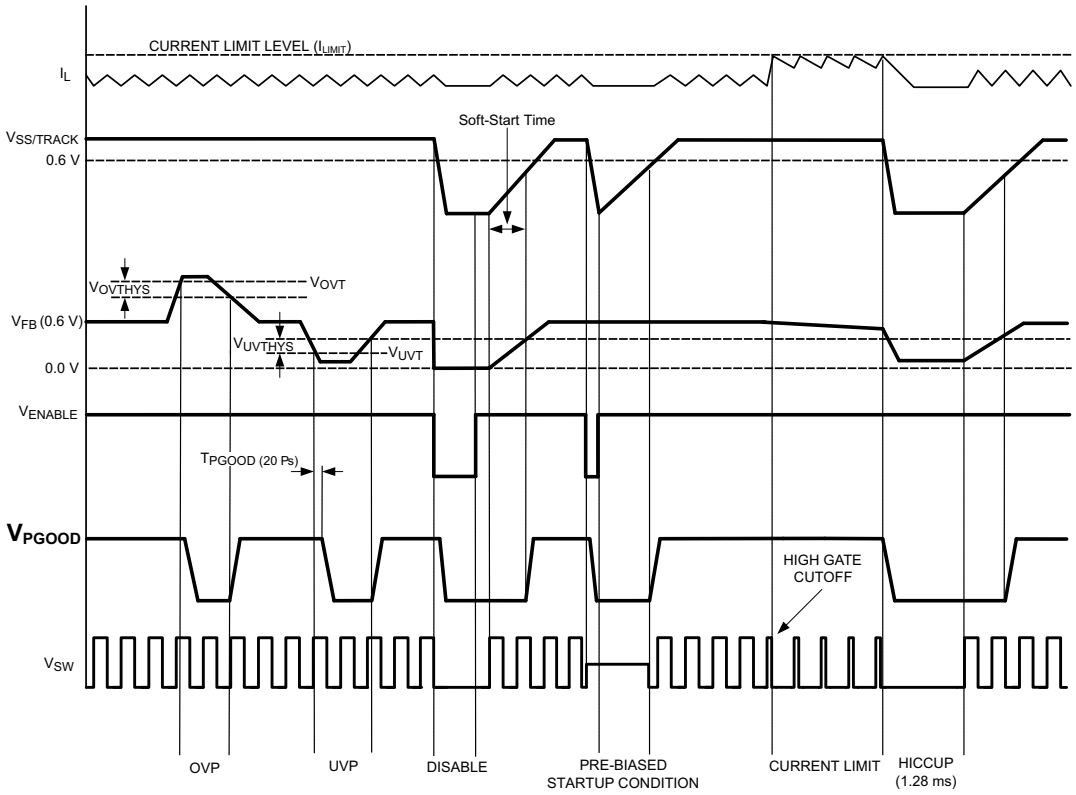


Figure 21. Power Good Behavior

The PGOOD flag of the LM27402 is used to signal when the output is out of regulation or during nonregulated pre-biased conditions. This means that current limit, UVLO, overvoltage threshold, undervoltage threshold, or a non-regulated output will cause the PGOOD pin to pull low. To prevent glitches to PGOOD, a 20-µs deglitch filter is built into the LM27402. Figure 21 illustrates when the PGOOD flag is asserted low.

7.3.8 Inductor-DCR-Based Overcurrent Protection

The LM27402 exploits the filter inductor DCR (DC resistance) to detect overcurrent events. This technique enables lossless and continuous monitoring of the output current using an RC sense network in parallel with the inductor. DCR current sensing allows the system designer to use inductors specified with tight tolerance DCRs to improve the current limit setpoint accuracy. A DC current limit setpoint accuracy within the range of 10% to 20% is achieved using inductors with low DCR tolerances.

Feature Description (continued)

7.3.9 Current Sensing

As mentioned, the LM27402 implements a lossless inductor DCR lossless current sense scheme designed to provide both accurate overload (current limit) and short-circuit protection. Figure 22 shows the popular inductor DCR current sense method. Figure 23 shows an implementation with current shunt resistor, R_{ISNS}.

Components R_S and C_S in Figure 22 create a low-pass filter across the inductor to enable differential sensing of the inductor DCR voltage drop. When R_SC_S is equal to L/R_{DCR}, the voltage developed across the sense capacitor, C_S, is a replica of the voltage waveform of the inductor DCR. Choose the capacitance of C_S greater than 0.1 µF to maintain low impedance of the sense network, thus reducing the susceptibility of noise pickup from the switch node.

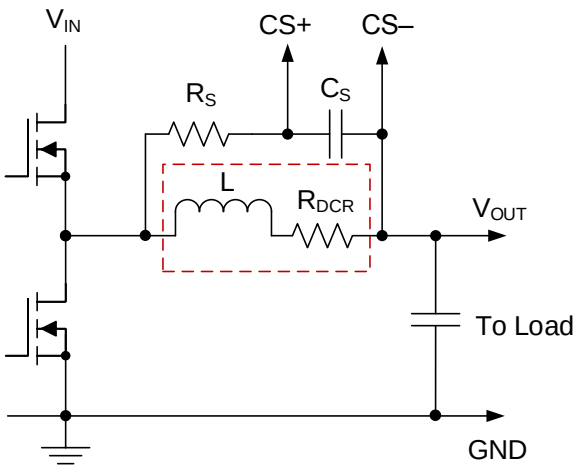


Figure 22. Current Sensing Using Inductor DCR

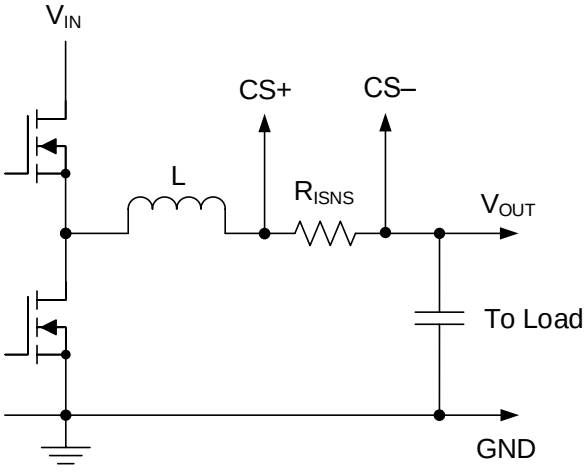


Figure 23. Current Sensing Using Shunt Resistor

Note that the inductor DCR is shown schematically as a discrete element in Figure 22. With power inductors selected to provide lowest possible DCR to minimize power losses, the typical DCR ranges from 0.4 mΩ to 4 mΩ. Then, given a load current of 25 A, the voltage presented across the CS+ and CS– pins ranges between 10 mV and 100 mV.

A current sense (or current shunt) resistor in series with the inductor can also be implemented at lower output current levels to provide accurate overcurrent protection, see Figure 23. Burdened by the unavoidable efficiency penalty and/or additional cost implications, this configuration is not usually implemented in high-current applications (except where OCP setpoint accuracy and stability over the operating temperature range are critical specifications).

7.3.10 Power MOSFET Gate Drivers

The LM27402 gate driver impedances are low enough to perform effectively in high output current applications where large die-size or paralleled MOSFETs with correspondingly large gate charge, Q_G, are used. Measured at V_{VDD} = 4.7 V, the LM27402's low-side driver has a low impedance pulldown path of 1 Ω to minimize the effect of dv/dt induced turn-on, particularly with low gate-threshold voltage MOSFETs. Similarly, the high-side driver has 1.7-Ω and 1.2-Ω pull-up and pulldown impedances, respectively, for faster switching transition times, lower switching loss, and greater efficiency.

Furthermore, there is a proprietary adaptive deadtime control on both switching edges to prevent shoot-through and cross-conduction, minimize body diode conduction time, and reduce body diode reverse recovery related losses. The LM27402 is fully compatible with discrete NexFET™ Power Block MOSFETs from TI.

7.3.11 Pre-Bias Start-up

In certain applications, the output may acquire a pre-bias voltage before the LM27402 is powered on or enabled. Pre-biased conditions are managed by preventing switching until the soft-start (SS/TRACK) voltage exceeds the feedback (FB) voltage. When $V_{SS/TRACK}$ exceeds V_{FB}, the LM27402 begins to switch synchronously and regulate the output voltage.

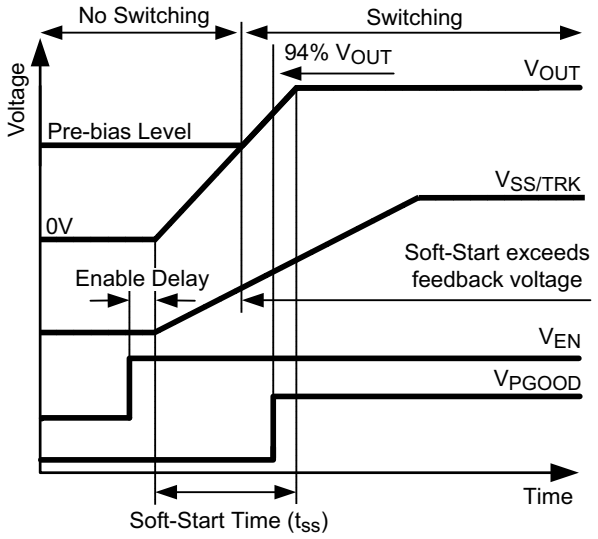


Figure 24. Pre-Bias Start-up

Prohibiting switching during a pre-biased start-up condition prevents the output from forcing parasitic paths in the system application to conduct excessive current. The LM27402 does not switch if the output is pre-biased to a voltage higher than the nominally-set output voltage.

7.4 Device Functional Modes

7.4.1 Fault Conditions

Overcurrent, overtemperature, output undervoltage, and overvoltage protection features are included in the LM27402.

7.4.1.1 Thermal Protection

Internal thermal shutdown is provided to protect the controller in the event that the maximum junction temperature of approximately 165°C has been exceeded. Both the high-side and low-side power MOSFETs are turned off during this condition. During a thermal fault condition, PGOOD is held at logic zero.

7.4.1.2 Current Limit

The LM27402 may enter two states when a current limit event is detected. If a current limit condition has occurred, the high-side power MOSFET is immediately turned off until the next switching cycle. This is considered the first current limit state and provides an immediate response to any current limit event. During the first state, an internal counter begins to record the number of overcurrent events. The counter is reset if 32 consecutive switching cycles occur with no current limit events detected. If five overcurrent events are detected within 32 switching cycles, the LM27402 then enters into a hiccup mode state. During hiccup mode, the LM27402 enters shutdown for 1.28 ms and then attempt to restart again. When transitioning into hiccup mode, the high-side MOSFET is turned off and the low-side MOSFET is turned on. As the inductor current reaches zero subsequent to the overcurrent event, the low-side MOSFET is turned off and the switch-node becomes high impedance to prepare for the next start-up sequence. The soft-start capacitor is discharged through an internal pulldown FET to reinitialize the start-up sequence. To illustrate how the LM27402 behaves during current limit faults, an overcurrent scenario is illustrated in Figure 25.

Device Functional Modes (continued)

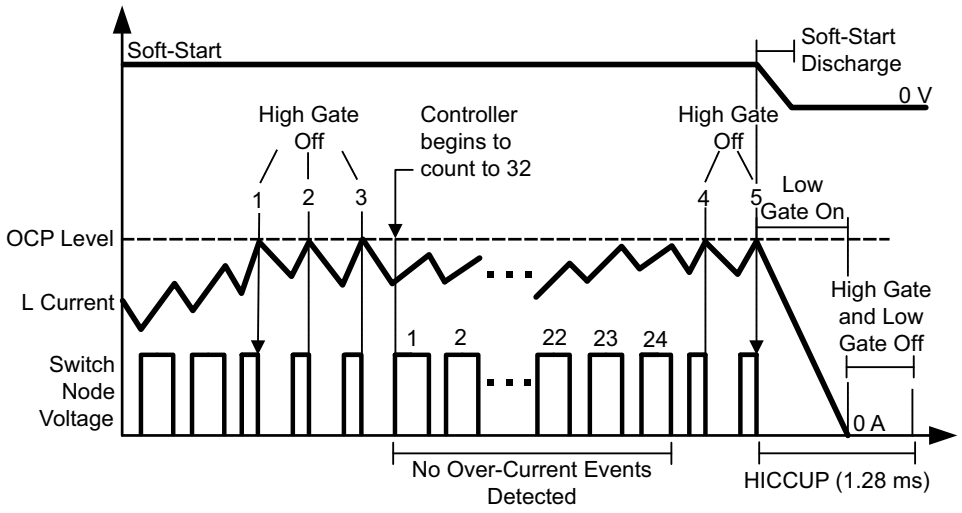


Figure 25. Current Limit Timing Diagram

In the example shown in Figure 25, the LM27402 immediately turns off the high-side MOSFET when an overcurrent event is detected. After the third overcurrent event is detected, 24 switching cycles occur before the fourth overcurrent pulse is detected. Because the current limit logic does not count 32 switching cycles between two overcurrent events, the internal current limit counter is not reset and continues counting until the LM27402 enters hiccup mode. The soft-start capacitor is then discharged to initialize start-up and a wait period of 1.28 ms occurs.

7.4.1.3 Negative Current Limit

To prevent excess negative current, the LM27402 implements a negative current limit through the low-side MOSFET. Negative current limit is only enabled when an output overvoltage event is detected. Should such an overvoltage fault occur, the low-side MOSFET turns off if the SW voltage exceeds a positive 100 mV during the low-side MOSFET conduction time, thereby protecting the power stage from excessive negative current.

7.4.1.4 Undervoltage Threshold (UVT)

The FB pin is also monitored for an output voltage excursion below the nominal level. However, if the UVT comparator is tripped, no action occurs on the normal switching cycles. The UVT signal is used solely as a valid condition for the Power Good flag to transition low. When the FB voltage exceeds 94% of the reference voltage, the Power Good flag transitions high. Conversely, the Power Good flag transitions low when the FB voltage is less than 91% of the reference.

7.4.1.5 Overvoltage Threshold (OVT)

When the FB voltage exceeds 117% of the reference voltage, the Power Good flag transitions low after a 20-µs deglitch. The control loop attempts to bring the output voltage back to the nominal setpoint. Conversely, when the FB voltage goes below 115% of the reference, the Power Good flag is allowed to transition high. Negative current-limit detection is activated when the regulator is in an OV condition. See the *Negative Current Limit* section for more details.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Converter Design

As with any DC/Dc converter, numerous tradeoffs are required to optimize the design for efficiency, size, or performance. Such tradeoffs are highlighted throughout the following discussion. To facilitate component selection, the circuit shown in Figure 26 may be used as a reference. Unless otherwise indicated, all formulae assume units of Amps (A) for current, Farads (F) for capacitance, Henries (H) for inductance and Volts (V) for voltage.

Figure 26 shows R_F and C_F acting as an RC filter to the VIN pin of the LM27402. The filter is used to attenuate voltage ripple that may exist on the input rail particularly during high output currents. The recommended values of R_F and C_F are 2.2 Ω and 1 µF, respectively. There is a practical limit to the size of R_F as it can cause a large voltage drop if large operating bias currents are present. The VIN pin of the LM27402 must not exceed 150 mV difference from the input voltage rail (V_{IN}).

Equation 1 is used to calculate for any buck converter is duty ratio:

$$D = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{\eta} \tag{1}$$

Due to the resistive powertrain losses, the duty ratio will increase based on the overall efficiency, η. Calculation of η can be found in the *Power Loss and Efficiency Calculations* section of this data sheet.

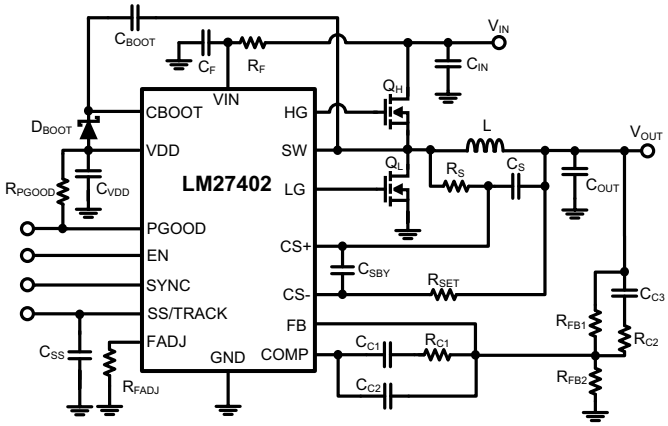


Figure 26. Typical Application Circuit

Application Information (continued)

8.1.2 Inductor Selection (L)

The inductor value is determined based on the operating frequency, load current, ripple current, and duty ratio. The selected inductor must have a saturation current rating greater than the peak current limit of the LM27402. To optimize the performance, the inductance is typically selected such that the ripple current, ΔI_L, is between 20% and 40% of the rated output current. Figure 27 illustrates the switch voltage and inductor ripple current waveforms. Once the nominal input voltage, output voltage, operating frequency, and desired ripple current are known, the minimum inductance value can be calculated by Equation 2:

$$L_{MIN} = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}} \quad (2)$$

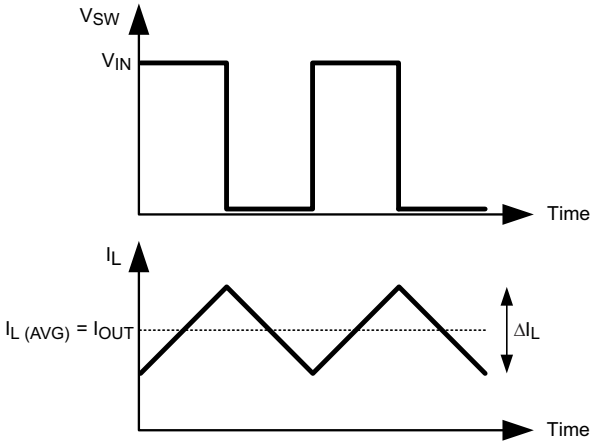


Figure 27. Switch Voltage and Inductor Current Waveforms

The peak inductor current at maximum load, $I_{OUT} + \Delta I_L / 2$, should be kept adequately below the peak current limit setpoint of the device.

8.1.3 Output Capacitor Selection (C_{OUT})

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a source of charge for transient load events. A wide range of output capacitors may be used with the LM27402 that provide excellent performance, including ceramic, tantalum, or electrolytic type chemistries. Typically, ceramic capacitors provide extremely low ESR to reduce the output ripple voltage and noise spikes, while tantalum and electrolytic capacitors provide a large bulk capacitance in a small size for transient loading events. When selecting the output capacitance, the two performance characteristics to consider are output voltage ripple and transient response. The output voltage ripple is approximated by Equation 3:

$$\Delta V_{OUT} = \Delta I_L \times \sqrt{R_{ESR}^2 + \left(\frac{1}{8 \times f_{SW} \times C_{OUT}}\right)^2} \quad (3)$$

where ΔV_{OUT} is the amount of peak-to-peak voltage ripple at the power supply output, R_{ESR} is the equivalent series resistance of the output capacitor, f_{SW} is the switching frequency, and C_{OUT} is the output capacitance used in the design. The tolerable output ripple amplitude is application specific; however a general recommendation is to keep the output ripple less than 1% of the rated output voltage. Note that ceramic capacitors are sometimes preferred because they have very low ESR; however, depending on package and voltage rating of the capacitor, the effective in-circuit capacitance can drop significantly with applied voltage and operating temperature.

Application Information (continued)

The output capacitor also affects the output voltage deviation during a load current transient. The peak output voltage deviation is dependent on many factors such as output capacitance, output capacitor ESR, filter inductance, control loop bandwidth, powertrain parasitics, and so on. Given sufficient control loop bandwidth, a good approximation of the output voltage deviation is seen in Equation 4:

$$\Delta V_{TR} = \frac{L \times \Delta I_O^2}{2 \times C_{OUT} \times V_L} + \frac{R_{ESR}^2 \times C_{OUT} \times V_L}{2 \times L} \quad (4)$$

ΔV_{TR} is the transient output voltage deviation, ΔI_{OUT} is the load current step change and L is the filter inductance. V_L is the minimum inductor voltage, which is duty ratio dependent.

$V_L = V_{OUT}$, if D ≤ 0.5,

$V_L = V_{IN} - V_{OUT}$, if D > 0.5

For a desired ΔV_{TR}, a minimum output capacitance is found by Equation 5:

$$C_{OUT} \geq \frac{L \times \Delta I_{OUT}^2}{\Delta V_{TR} \times V_L} \times \frac{1}{1 + \sqrt{1 - \left(\frac{R_{ESR} \times \Delta I_{OUT}}{\Delta V_{TR}}\right)^2}} \quad (5)$$

8.1.4 Input Capacitor Selection (C_{IN})

Input capacitors are necessary to limit the input ripple voltage while supplying much of the switch current during the high-side MOSFET on-time. It is generally recommended to use ceramic capacitors at the input as they provide both a low impedance and a high RMS current rating. It is important to choose a stable dielectric for the ceramic capacitor such as X5R or X7R. A quality dielectric provides better temperature performance and also avoids the DC voltage derating inherent with Y5V capacitors. Place the input capacitor as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET. Non-ceramic input capacitors must be selected for RMS current rating, minimum ripple voltage, and to provide damping. A good approximation for the required ripple current rating is given by the relationship of Equation 6:

$$I_{CIN\_RMS} \approx I_{OUT} \times \sqrt{D \times (1 - D)} \quad (6)$$

The highest requirement for RMS current rating occurs for D = 0.5. When D = 0.5, the RMS ripple current rating of the input capacitor must be greater than half the output current. Low ESR ceramic capacitors can be placed in parallel with higher valued bulk capacitors to provide optimized input filtering for the regulator. The input voltage ripple is calculated using Equation 7:

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{C_{IN} \times f_{SW}} + \left(I_{OUT} + \frac{\Delta I_L}{2}\right) \times R_{ESR\_CIN} \quad (7)$$

The minimum amount of input capacitance as a function of desired input voltage ripple is estimated using Equation 8:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{\left(\Delta V_{IN} - \left(I_{OUT} + \frac{\Delta I_L}{2}\right) \times R_{ESR\_CIN}\right) \times f_{SW}} \quad (8)$$

8.1.5 Using Precision Enable

If enable (EN) is not controlled directly, the LM27402 can be pre-programmed to turn on at an input voltage higher than the UVLO voltage. This is done with an external resistor divider from VIN to EN and EN to GND as shown in Figure 28.

Application Information (continued)

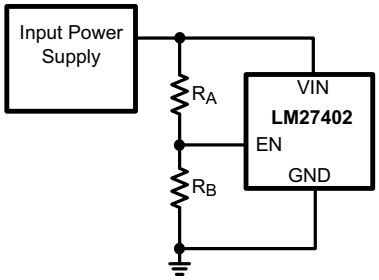


Figure 28. Enable Sequencing

The resistor values of R_A and R_B are relatively sized to allow the EN pin to reach the precision enable threshold voltage at the appropriate input supply voltage. With the enable current source considered, the equation to solve for R_A is Equation 9:

$$R_A = \frac{R_B(V_{IN} - 1.17V)}{1.17V - I_{EN} \times R_B} \quad (9)$$

where R_A is the resistor from VIN to EN, R_B is the resistor from EN to GND, I_{EN} is the internal enable pull-up current (2 µA) and 1.17 V is the fixed precision enable threshold voltage. Typical values for R_B range from 10 kΩ to 100 kΩ.

8.1.6 Setting the Soft-Start Time

Adding a soft-start capacitor reduces inrush currents and provides a monotonic start-up. The soft-start capacitance is calculated by Equation 10:

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{0.6V} \quad (10)$$

As shown, the C_{SS} capacitance is set by the desired soft-start time t_{ss}, the soft-start current I_{ss} (3 µA) and the nominal feedback (FB) voltage level of 0.6 V. If V_{VIN} and V_{VDD} are above their UVLO voltage levels (2.9 V) and EN is above the precision enable threshold (1.17 V), the soft-start sequence begins. The LM27402 defaults to a minimum start-up time of 1.28 ms when a soft-start capacitor is not connected. In other words, the LM27402 will not start-up faster than 1.28 ms. The soft-start capacitor is discharged when enable is cycled, during UVLO, OTP, or when the LM27402 enters hiccup mode from an overcurrent event.

There is a delay between EN transitioning above 1.17 V and the beginning of the soft-start sequence. The delay allows the LM27402 to initialize its internal circuitry. Once the output has charged to 94% of the nominal output voltage and SS/TRACK has exceeded 564 mV, the PGOOD indicator transitions high as illustrated in Figure 29.

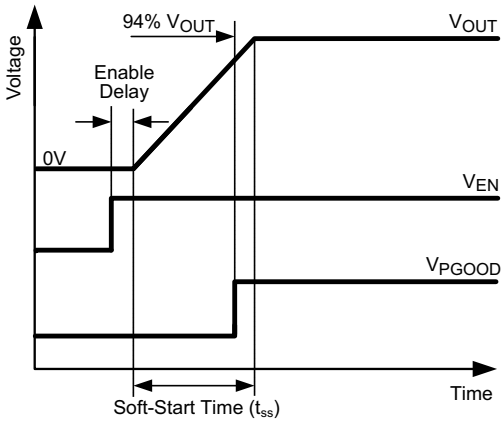


Figure 29. Soft-Start Timing

Application Information (continued)

8.1.7 Tracking

The SS/TRACK pin also functions as a tracking pin when external power supply tracking is needed. Tracking is achieved by simply dividing down the external supply voltage with a simple resistor network shown in Figure 30. With the correct resistor divider configuration, the LM27402 can track an external voltage source to obtain a coincident or ratiometric start-up behavior.

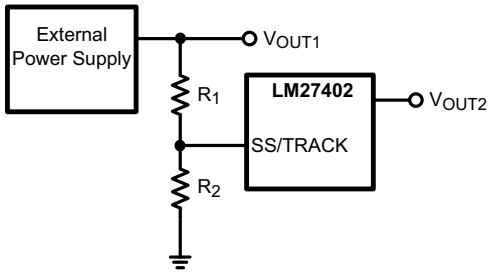


Figure 30. Tracking an External Power Supply

Because the soft-start charging current I_{SS} is sourced from the SS/TRACK pin, the size of R_2 must be less than 10 kΩ to minimize errors in the tracking output. Once a value for R_2 is selected, calculate the value for R_1 using the appropriate equation in Figure 31 to give the desired start-up sequence. Figure 31 shows two common start-up sequences; the upper waveform shows a coincidental start-up while the lower waveform illustrates a ratiometric start-up. A coincidental configuration provides a robust start-up sequence for certain applications because it avoids turning on any parasitic conduction paths that may exist between loads. A ratiometric configuration is preferred in applications where both supplies need to be at the final steady-state voltage at the same time.

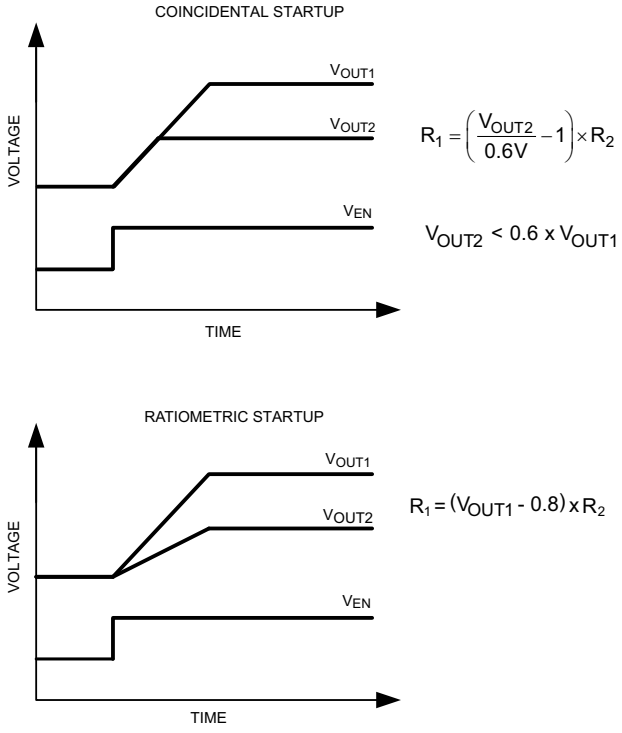


Figure 31. Tracking Start-up Sequences

Similar to the soft-start function, the fastest possible startup time is 1.28 ms regardless of the rise time of the tracking voltage. When using the track feature, the final voltage seen by the SS/TRACK pin should exceed 0.8 V to provide sufficient overdrive and transient immunity.

Application Information (continued)

8.1.8 Setting the Switching Frequency

There are two options for setting the switching frequency of the LM27402. The frequency is adjusted by an external resistor from FADJ to GND, or the user can synchronize the LM27402 to an external clock signal using SYNC. The LM27402 only synchronizes to frequencies above the frequency set by the R_{FADJ} resistor. The clock signal must range from less than 0.8 V to greater than 2.0 V to ensure proper operation. If the clock signal ceases, the switching frequency reduces to the free-running frequency set by the FADJ resistor. The frequency range is 200 kHz to 1.2 MHz. The sync-in clock can synchronize at a maximum of 400 kHz above the frequency set by the resistor. To find the resistance needed for a given frequency, use the following equation: (f_{SW} (kHz), R_{FADJ} (kΩ))

$$R_{FADJ} = \frac{100}{\frac{f_{SW}}{100} - 1} - 5 \tag{11}$$

8.1.9 Setting the Current Limit Threshold

As mentioned in the *Current Sensing* section, the LM27402 exploits the filter inductor DCR to detect overcurrent events. If desired, the user can employ inductors with low tolerance DCR to increase the accuracy of the current limit threshold. The most common circuit arrangement for sensing the inductor DCR voltage is shown in Figure 32.

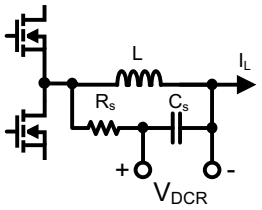


Figure 32. Inductor DCR Current Sensing Circuit

The most accurate sensing of the differential voltage across the inductor DCR is achieved by matching the time constant of the R_SC_S sense filter with the inductor's L/R_{DCR} time constant. If the time constants are matched, the voltage across the capacitor follows the voltage across the DCR. A typical range of capacitance used in the R_SC_S network is 100 nF to 1µF. The equation to match the time constants is:

$$R_SC_S = \frac{L}{R_{DCR}} \tag{12}$$

Adjust the current limit threshold to any level with a single resistor from the current limit comparator to the output voltage pin. Use the circuit in Figure 33 to set the current limit.

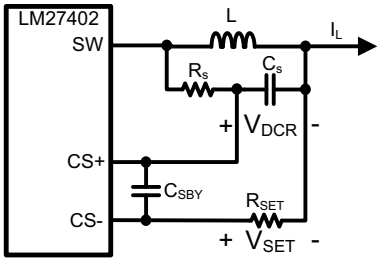


Figure 33. Adjusting the Current Limit Setpoint

Application Information (continued)

Because the voltage across the inductor DCR follows the current through the inductor, the device trips at the peak of the inductor current. Capacitor C_{SBY} shown in Figure 33 filters the input to the current sense comparator. A working range for this capacitance is 47 pF to 100 pF. The equation to set the resistor value of R_{SET} is:

$$R_{SET} = \frac{I_{LIMIT} R_{DCR}}{I_{cs-}} \tag{13}$$

I_{LIMIT} is the desired current limit level, R_{DCR} is the rated DC resistance of the inductor and I_{cs-} is the 10 µA current source flowing out of the CS– pin. To aid in high frequency common-mode rejection, a series resistor, R_{CS}, of same resistance as R_{SET}, is optionally added to the CS+ signal path.

The internal current source I_{CS-} is powered from the input voltage rail, V_{IN}. The minimum voltage required to drive that current source is 1 V from V_{IN} to V_{OUT}. If a low-dropout condition occurs where $V_{IN} - V_{OUT} < 1$ V, the LM27402 may prematurely initiate hiccup mode. There are multiple options to avoid this situation. The first option is to enable the LM27402 after the input voltage has risen 1 V above the nominal output voltage as seen in Figure 28. The second option is to lower the comparator common-mode voltage shown in Figure 34 such that the I_{CS-} current source has enough headroom voltage.

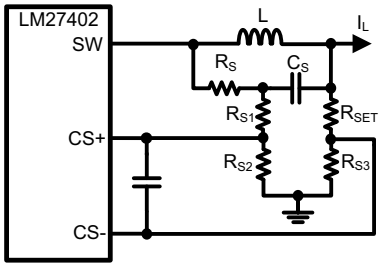


Figure 34. Common Mode Voltage Resistor Divider Network

Refer to *AN-2060 LM27402 Current Limit Application Circuits* (SNVA441) for design guidelines to adjust the common-mode voltage of the current sense comparator.

8.1.10 Control Loop Compensation

The LM27402 voltage mode control system incorporates input voltage feedforward to eliminate the input voltage dependence of the PWM modulator gain. Input voltage feedforward is essential for stability across the entire input voltage range and makes it easier for the designer to select the compensation and power train components. The following describes how to set the output voltage and obtain the open-loop transfer function.

During steady state operation, the DC output voltage is set by the feedback resistor network between V_{OUT}, FB and GND. The FB voltage is nominally 0.6 V ±1%. The equation describing the output voltage is:

$$V_{OUT} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} 0.6V \tag{14}$$

A good starting value for R_{FB1} is 20 kΩ. If an output voltage of 0.6 V is required, R_{FB2} must not be used.

There are three main blocks of a voltage-mode buck switcher that the power supply designer needs to consider when designing the control system: power train, PWM modulator, and compensator. A diagram representing the control loop is shown in Figure 35.

Application Information (continued)

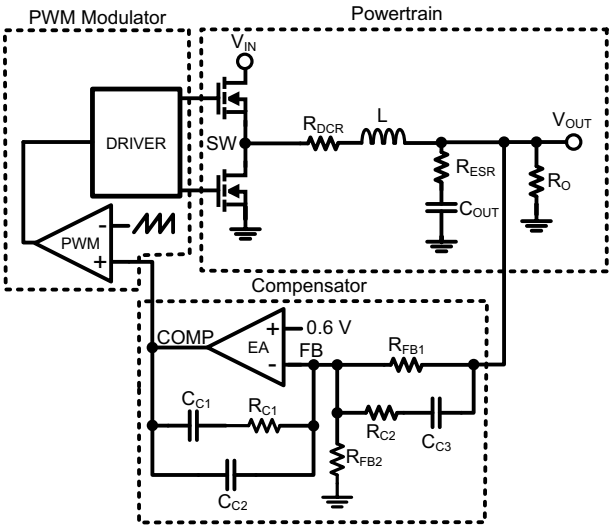


Figure 35. Control Loop Schematic Diagram

The power train consists of the filter inductor (L) with DCR (R_{DCR}), output capacitor (C_{OUT}) with ESR (effective series resistance R_{ESR}), and effective load resistance (R_O). The error amplifier (EA) regulates the feedback (FB) voltage to 0.6V. The passive compensation components around the error amplifier establish system stability. Type-III compensation is shown in Figure 35. The PWM modulator establishes the duty cycle command by comparing the error amplifier output (COMP) with an internally generated ramp set at the switching frequency.

The modulator gain, power train and compensator transfer functions must be taken into consideration when obtaining the total open-loop transfer function. The PWM modulator adds a DC gain component to the open-loop transfer function. In a basic voltage-mode system, the PWM gain varies with input voltage. However the LM27402 internal voltage feedforward circuitry maintains a constant PWM gain of 7:

$$G_{PWM} = \frac{1}{k_{FF}} = 7 \tag{15}$$

The power train transfer function includes the filter inductor and its DCR, output capacitor with ESR, and load resistance. The inductor and capacitor create two complex poles at a frequency described by:

$$f_{LC} = \frac{1}{2\pi}\sqrt{\frac{R_O + R_{DCR}}{LC_{OUT}(R_O + R_{ESR})}} \tag{16}$$

A left half plane zero is created by the output capacitor ESR located at a frequency described by:

$$f_{ESR} = \frac{1}{2\pi C_{OUT} R_{ESR}} \tag{17}$$

The complete power train transfer function is:

$$G_P(s) = \frac{1 + \frac{s}{2\pi f_{ESR}}}{1 + \frac{s}{Q_O 2\pi f_{LC}} + \left(\frac{s}{2\pi f_{LC}}\right)^2} \tag{18}$$

Figure 36 shows the bode plot of the above transfer function.

Application Information (continued)

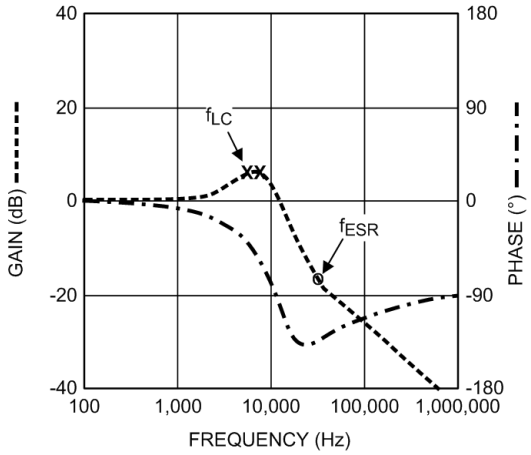


Figure 36. Powertrain Bode Plot

The complex poles (f_{LC}) created by the filter inductor and output capacitor cause a 180° phase shift as seen in Figure 36. The phase is boosted back up to -90° by virtue of the output capacitor ESR zero. The phase shift caused by the complex poles must be compensated to stabilize the loop response. The compensation network shown around the error amplifier in Figure 35 creates two poles, two zeros and a pole at the origin. Placing these poles and zeros at the correct frequencies optimizes the loop response. The compensator transfer function is:

$$G_{EA}(s) = K_m \frac{\left(\frac{2\pi f_{Z1}}{s} + 1\right)\left(\frac{s}{2\pi f_{Z2}} + 1\right)}{\left(\frac{s}{2\pi f_{P1}} + 1\right)\left(\frac{s}{2\pi f_{P2}} + 1\right)} \quad (19)$$

The pole located at the origin provides high DC gain to maximize DC load regulation performance. The other two poles and two zeros are strategically located to stabilize the voltage-mode loop depending on the power stage complex poles and damping characteristic, Q. Figure 37 illustrates a typical compensation transfer function.

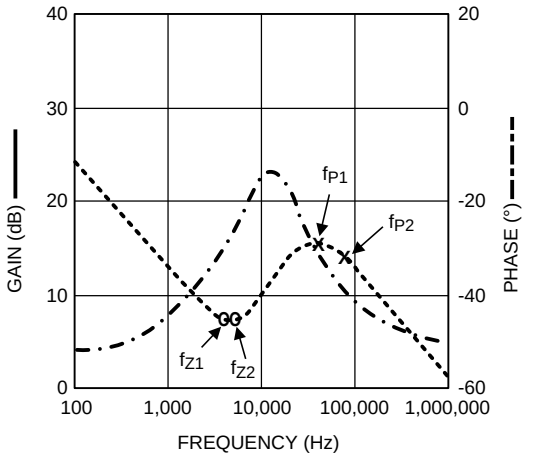


Figure 37. Type-III Compensation Network Bode Plot

K_m is the mid-band gain of the compensator and is estimated by:

$$K_m = \frac{f_C \, k_{FF}}{f_{LC}} \quad (20)$$

Application Information (continued)

f_C is the desired crossover frequency and is normally selected between one tenth and one fifth of the switching frequency, f_{SW}. The next set of equations show pole and zero locations expressed in terms of the components in the compensator feedback loop.

$$f_{Z1} = \frac{1}{2\pi R_{C1} C_{C1}} \quad f_{Z2} = \frac{1}{2\pi (R_{C2} + R_{FB1}) C_{C3}}$$

$$f_{P1} = \frac{1}{2\pi R_{C2} C_{C3}} \quad f_{P2} = \frac{C_{C1} + C_{C2}}{2\pi R_{C1} C_{C1} C_{C2}} \quad K_m = \frac{R_{C1}}{R_{FB1}} \tag{21}$$

Depending on Q, the complex double pole causes an increase in gain at the LC resonant frequency and a precipitous drop in phase. To compensate for the phase drop, it is common practice to place both compensator zeros created by the Type-III compensation network at or slightly below the LC double pole frequency. The other two poles are located beyond this point. One pole is located at the zero caused by the output capacitor ESR and the other pole is placed at half the switching frequency to roll off the higher frequency response.

$$f_{Z1} = f_{Z2} = f_{LC}$$

$$f_{P1} = f_{ESR}$$

$$f_{P2} = \frac{f_{SW}}{2} \tag{22}$$

Conservative values for the compensation components are found by using the following equations.

$$R_{C1} = R_{FB1} K_m$$

$$C_{C1} = \frac{1}{2\pi f_{LC} R_{C1}}$$

$$R_{C2} = \frac{R_{FB1} f_{LC}}{f_{ESR} - f_{LC}}$$

$$C_{C3} = \frac{1}{2\pi f_{ESR} R_{C2}}$$

$$C_{C2} = \frac{C_{C1}}{\pi f_{SW} R_{C1} C_{C1} - 1} \tag{23}$$

Once the compensation components are fixed, create a Bode plot of the loop response using all three transfer functions. Figure 38 provides an illustration of the loop response.

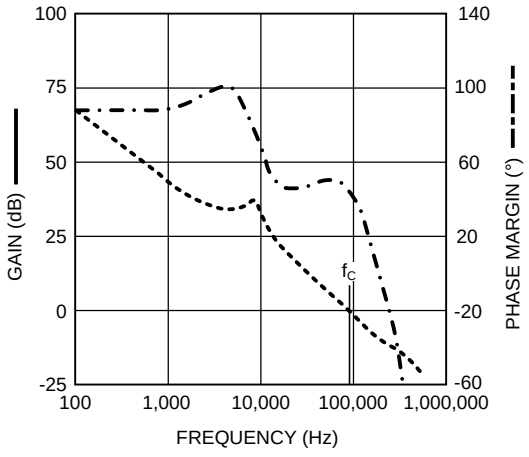


Figure 38. Loop Response

Application Information (continued)

It is important to always verify the stability by either observing the load transient response or by using a network analyzer. A phase margin between 45° and 70° is usually desired for voltage-mode controlled systems. Excessive phase margin causes slow system response to load transients whereas low phase margin is indicated by an oscillatory load transient response. If the peak voltage deviation is larger than desired, increase f_C and recalculate the compensation components. If this amounts to a reduction in phase margin, the remaining option is to increase output capacitance.

8.1.11 MOSFET Gate Drivers

To drive large power MOSFETs with high gate charge, the LM27402 includes low impedance high-side and low-side gate drivers that source and sink high current for fast transition times and increased efficiency. The high-side gate driver is powered from a bootstrap circuit, whereas the low-side driver is powered by the VDD rail as shown in Figure 39.

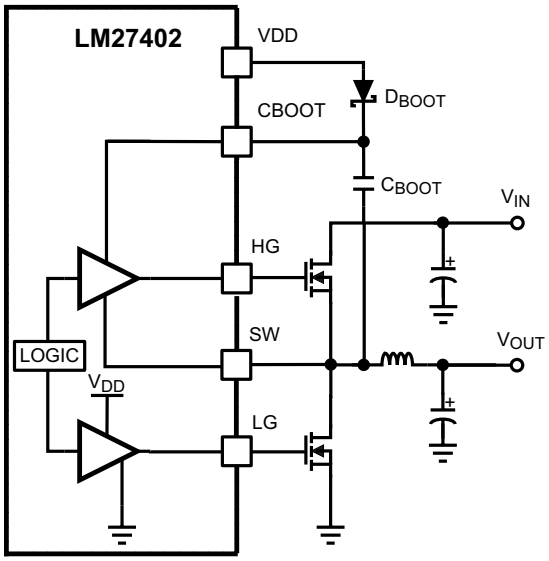


Figure 39. High-Side and Low-Side MOSFET Gate Drivers

The circuit in Figure 39 effectively supplies close to the VDD voltage (4.5 V) between the gate and the source of the high-side MOSFET during the on time. Use a Schottky diode for D_{BOOT} with sufficient reverse voltage rating and continuous current rating. The average current through the boot diode depends on the gate charge of the high-side MOSFET and the switching frequency. It is calculated using Equation 24.

$$I_{DBOOT} = f_{SW} Q_{GHS} \tag{24}$$

I_{DBOOT} is the average current through the D_{BOOT} diode, f_{SW} is the switching frequency and Q_{GHS} is the gate charge of the high-side MOSFET. If the input voltage is below 5.5 V, it is recommended to connect VDD to the input supply of the LM27402 through a 1-Ω resistor as shown in Figure 40. This increases the gate voltage amplitude of both the low-side and high-side MOSFETs, thus reducing $R_{DS(on)}$.

Application Information (continued)

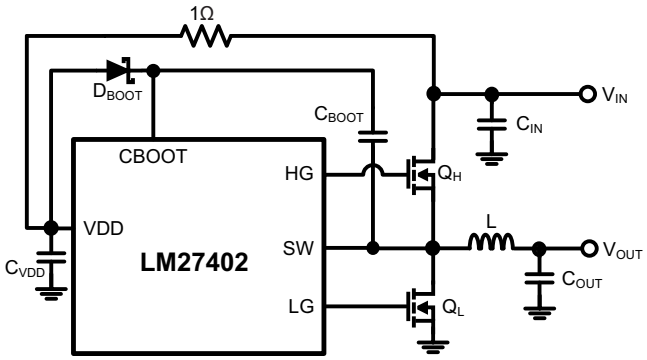


Figure 40. Tie V_{DD} to V_{IN} when VIN ≤ 5.5V

8.1.12 Power Loss and Efficiency Calculations

The overall efficiency of a buck regulator is simply the ratio of output power to input power. Although power losses are found in almost every component of a buck regulator, the following sections present equations detailing components with the highest relative power loss.

8.1.12.1 Power MOSFETs

Selecting the correct power MOSFET for a design is important to the overall operation of the circuit. If inappropriate MOSFETs are selected for the application, it may result in poor efficiency, high temperature issues, shoot-through and other impairments. It is important to calculate the power dissipation for each MOSFET at the maximum output current and ensure that the maximum allowable power dissipation is not exceeded. MOSFET data sheets must also specify a junction-to-ambient thermal resistance (θ_{JA}), and the temperature rise is estimated from this specification.

Both high-side and low-side MOSFETs contribute significant loss to the system relative to the other components. The high-side MOSFET contributes transition switching loss, conduction loss and gate charge loss. The low-side MOSFET also contributes conduction and gate charge loss, and the body diode of the MOSFET causes deadtime conduction loss and reverse recovery loss that must also be considered. The transition losses for the low-side MOSFET are insignificant and usually ignored.

8.1.12.2 High-Side Power MOSFET

The next set of equations are used to calculate the losses associated with the high-side MOSFET.

$$P_{CND\_HS} \approx I_{OUT}^2 \times R_{DS(ON)\_HS} \times D \times 1.3$$

$$P_{SW\_HS} = \frac{V_{IN} \times I_{OUT} \times f_{SW} \times (tr+tf)}{2}$$

$$P_{TOT\_HS} = P_{CND\_HS} + P_{SW\_HS} \quad (25)$$

P_{CND_HS} is the conduction loss of the high-side MOSFET during the D interval. this equation includes a self heating coefficient of 1.3 to approximate the effects of the $R_{DS(on)}$ temperature coefficient. $R_{DS(ON)\_HS}$ is the drain to source resistance, I_{OUT} is the output current and D is the duty ratio. P_{SW_HS} is the switching power loss during the high-side MOSFET transition time. V_{IN} is the input voltage, f_{SW} is the switching frequency, and t_r and t_f are the rise and fall times of the switch-node voltage, respectively. P_{TOT_HS} is the total power dissipation of the high-side MOSFET.

The gate charge of the high-side MOSFET greatly affects the turn-on transition time, and therefore efficiency. Furthermore, consider the ratio of switching loss to conduction loss associated with the high-side MOSFET. If the duty ratio is small and the input voltage is high, it is beneficial to tradeoff Q_G for higher $R_{DS(on)}$ to avoid high switching losses relative to conduction losses. If the duty ratio is large and the input voltage is low, then a lower $R_{DS(on)}$ MOSFET in tandem with a higher Q_G may result in less power dissipation.

Application Information (continued)

8.1.12.3 Low-Side Power MOSFET

The next set of equations are used to calculate the losses due to the low-side MOSFET.

$$P_{CND\_LS} \approx I_{OUT}^2 \times R_{DS(ON)\_LS} \times (1\text{-}D) \times 1.3$$
$$P_D = T_{deadtime} \times f_{SW} \times I_{OUT} \times V_{FD}$$
$$P_{RR} = Q_{RR} \times f_{SW} \times V_{IN}$$
$$P_{TOT\_LS} = P_{CND\_LS} + P_D + P_{RR} \quad (26)$$

P_{CND_LS} is the conduction loss of the low-side MOSFET during the 1-D cycle and $R_{DS(ON)\_LS}$ is its on-state resistance. P_D is the deadtime power loss due to the body diode drop of the low-side MOSFET. $T_{deadtime}$ is the total deadtime. P_{RR} is the reverse recovery charge power loss. Q_{RR} is the total reverse recovery charge typically specified in the MOSFET datasheet. P_{TOT_LS} is the total power dissipation of the low-side MOSFET.

8.1.12.4 Gate-Charge Loss

A finite amount of gate charge is required in order to switch the high-side and low-side power MOSFETs. This gate charge is continually charging the MOSFET gates during every switching cycle and appears as a constant current flowing to the controller from the input supply. The next equation describes the power loss due to the gate charge.

$$P_{QG} = V_{IN} \times (Q_{GHS} + Q_{GLS}) \times f_{SW} \quad (27)$$

P_{QG} is the total gate charge power loss, Q_{GHS} and Q_{GLS} are the respective high-side and low-side MOSFET gate charges found in the MOSFET datasheets, V_{IN} is the input voltage, and f_{SW} is the switching frequency.

8.1.12.5 Input and Output Capacitor ESR Losses

Both the input and output capacitors are subject to steady state AC current and must be taken into consideration when calculating power losses. The next equation shown is the input capacitor ESR power loss.

$$P_{IN\_CAP} = I_{CIN\_RMS}^2 \times R_{ESR\_CIN} \quad (28)$$

The input capacitor power loss equation includes the effective series resistance or R_{ESR_IN} of the input capacitor. The power loss due to the ESR of the output capacitor is:

$$P_{OUT\_CAP} = \frac{\Delta I_L^2}{12} \times R_{ESR} \quad (29)$$

The output capacitor power loss equation includes the peak-to-peak inductor current, ΔI_L, and the effective series resistance or R_{ESR} of the output capacitor.

8.1.12.6 Inductor Losses

The losses due to the inductor are caused primarily by its DCR. The next equation calculates the inductor DCR power loss.

$$P_{DCR} = I_{RMS}^2 \times R_{DCR} \times 1.2 \quad (30)$$

P_{DCR} is the total power loss of the Inductor. A self-heating coefficient of 1.2 is included in this equation to approximate the effects of the copper temperature coefficient approximately equal to 3900ppm/°C. R_{DCR} is the inductor DC resistance.

Application Information (continued)

8.1.12.7 Controller Losses

The controller loss remains constant and typically contributes a very small loss of power. The quiescent current is the main factor in terms of power loss attributed to the controller and it remains constant at 4 mA. The quiescent current power loss equation is:

$$P_{IQ} = V_{IN} \times I_Q \tag{31}$$

The controller I_Q power loss equation includes the I_Q current (4 mA) and the input voltage V_{IN}.

It is also important to calculate the power dissipated in the controller itself due to the gate charge component of current flowing from VIN to VDD. This can cause the controller to operate at an elevated temperature given the power dissipation of the LDO pass device. The next equation calculates the power dissipated by the internal LDO.

$$P_{LDO} = (V_{VIN} - 4.5) \times (Q_{GLS}+Q_{GHS}) \times f_{SW} \tag{32}$$

P_{LDO} is the power dissipated in the LDO, Q_{GHS} and Q_{GLS} are the high-side and low-side MOSFET gate charges, respectively.

8.1.12.8 Overall Efficiency

After calculating the losses, the efficiency is thus calculated using:

$$\eta\ (\%) = \frac{P_{OUT}}{P_{OUT}+ P_{LOSS}} \times 100$$

$$P_{LOSS} = P_{TOT\_HS} + P_{TOT\_LS} + P_{QG} + P_{DCR} + P_{IN\_CAP} + P_{OUT\_CAP} + P_{IQ}$$

$$P_{OUT} = V_{OUT} \times I_{OUT} \tag{33}$$

8.2 Typical Applications

8.2.1 Example Circuit 1

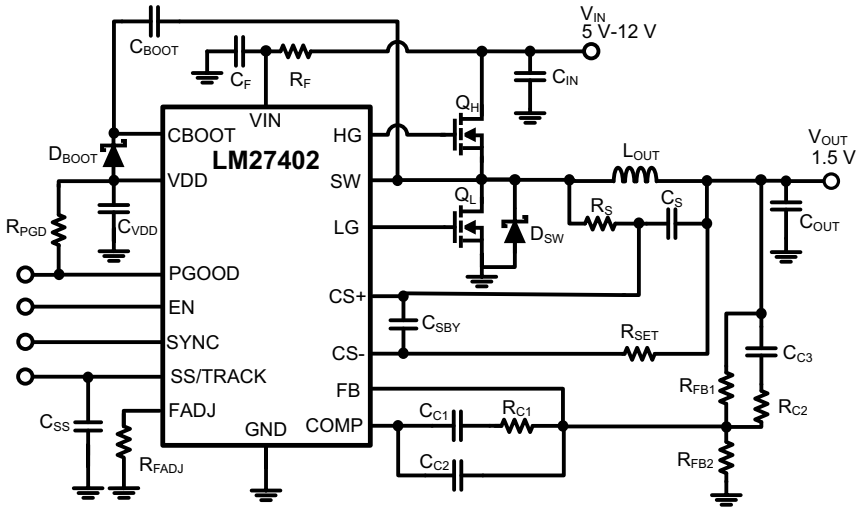


Figure 41. 4.5-V to 20-V Input, 1.5-V Output at 20 A, 300-kHz Switching Frequency

8.2.1.1 Design Requirements

The schematic diagram of a 20-A buck regulator is given in Figure 41 and its BOM is listed in Table 1. In this example, the target full-load efficiency is 88% at 12-V input voltage. Output voltage is adjusted simply by changing R_{FB2}. The free-running switching frequency is set to 300 kHz by resistor R_{FADJ}. The output voltage soft-start time is 10 ms.

8.2.1.2 Detailed Design Procedure

The design procedure for an LM27402-based converter for a given application is streamlined by using the *LM27402 Quick-Start Design Tool* available as a free download, or by availing of TI's WEBENCH® Designer online software. Such tools are complemented by the availability of the LM27402 evaluation module (EVM) design as well as numerous LM27402 reference designs populated in TI Designs™ reference design library.

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM27402 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

Typical Applications (continued)

The current limit setpoint in this design is set at 25 A at 25°C, based on resistor R_{SET} and the inductor DCR of 2.34 mΩ. Of course, the current limit setpoint must always be selected such that the operating current level does not exceed the saturation current specification of the chosen inductor. The component values for the DCR sense network (R_S and C_S in Figure 41) are chosen based on setting the R_SC_S product approximately equal to L/R_{DCR}, as recommended in the *Setting the Current Limit Threshold* section. The MOSFETs are chosen for both lowest conduction and switching power loss, as discussed in detail in the *Power MOSFETs* section.

Table 1. Bill of Materials

DESIGNATOR	TYPE	PARAMETERS	PART NUMBER	QTY	MANUFACTURER
U1	IC	Synchronous Buck Voltage-Mode PWM Controller	LM27402	1	TI
C_{BOOT}	Capacitor	0.22 µF, Ceramic, X7R, 25 V, 10%	GRM188R71E224KA88D	1	Murata
C_{C1}	Capacitor	3.9 nF, Ceramic, X7R, 50 V, 10%	GRM188R71H392KA01D	1	Murata
C_{C2}	Capacitor	150 pF, Ceramic, C0G, 50 V, 5%	GRM1885C1H151JA01D	1	Murata
C_{C3}	Capacitor	820 pF, Ceramic, C0G, 50 V, 5%	GRM1885C1H821JA01D	1	Murata
C_{VDD}	Capacitor	1 µF, Ceramic, X5R, 25 V, 10%	GRM188R61E105KA12D	1	Murata
C_F	Capacitor	1 µF, Ceramic, X5R, 25 V, 10%	GRM188R61E105KA12D	1	Murata
C_{IN}	Capacitor	22 µF, Ceramic, X5R, 25 V, 10%	GRM32ER61E226KE15L	5	Murata
C_{OUT}	Capacitor	100 µF, Ceramic, X5R, 6.3 V, 20%	C1210C107M9PACTU	4	Kemet
C_S	Capacitor	0.22 µF, Ceramic, X7R, 25 V, 10%	GRM188R71E224KA88D	1	Murata
C_{SS}	Capacitor	47 nF, Ceramic, X7R, 16 V, 10%	GRM188R71C473KA01D	1	Murata
C_{SBY}	Capacitor	100 pF, Ceramic, C0G, 50 V, 5%	GRM1885C1H101JA01D	1	Murata
D_{BOOT}	Diode	Schottky Diode, Average I = 100 mA, Max Surge I = 750 mA	CMOSH-3	1	Central Semi
D_{SW}	Diode	Schottky Diode, Average I = 3A, Max Surge I = 80A	CMSH3-40M	1	Central Semi
L_{OUT}	Inductor	0.68 µH, 2.34 mΩ	IHLP5050CEERR68M06	1	Vishay
Q_L	N-CH MOSFET	30 V, 60 A, 43.5 nC, $R_{DS(on)}$ at 4.5 V = 1.85 mΩ	Si7192DP	1	Vishay
Q_H	N-CH MOSFET	25 V, 40 A, 13 nC, $R_{DS(on)}$ at 4.5 V = 6.2 mΩ	SiR436DP	1	Vishay
R_{C1}	Resistor	8.06 kΩ, 1%, 0.1 W	CRCW06038k06FKEA	1	Vishay
R_{C2}	Resistor	261 Ω, 1%, 0.1 W	CRCW0603261RFKEA	1	Vishay
R_{FADJ}	Resistor	45.3 kΩ, 1%, 0.1 W	CRCW060345K3FKEA	1	Vishay
R_{FB1}	Resistor	20.0 kΩ, 1%, 0.1 W	CRCW060320K0FKEA	1	Vishay
R_{FB2}	Resistor	13.3 kΩ, 1%, 0.1 W	CRCW060320K0FKEA	1	Vishay
R_F	Resistor	2.2 Ω, 5%, 0.1 W	CRCW06032R20JNEA	1	Vishay
R_{PGD}	Resistor	51.1 kΩ, 5%, 0.1 W	CRCW060351K1JNEA	1	Vishay
R_S	Resistor	1.3 kΩ, 1%, 0.1 W	CRCW06031K30FKEA	1	Vishay
R_{SET}	Resistor	6.34 kΩ, 1%, 0.1 W	CRCW06036K34FKEA	1	Vishay

8.2.1.3 Application Curves

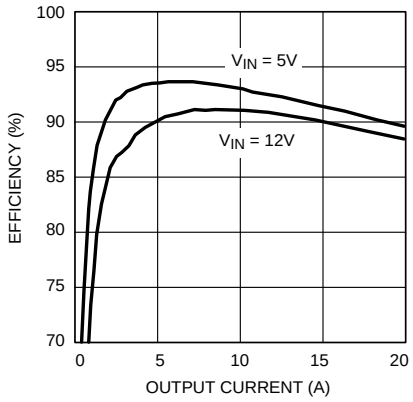


Figure 42. Converter Efficiency vs Output Current

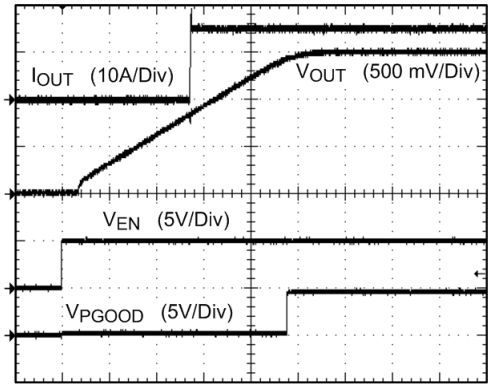


Figure 43. Start-up Characteristic with EN Stepped High, 15-A Electronic Load (2 ms/div)

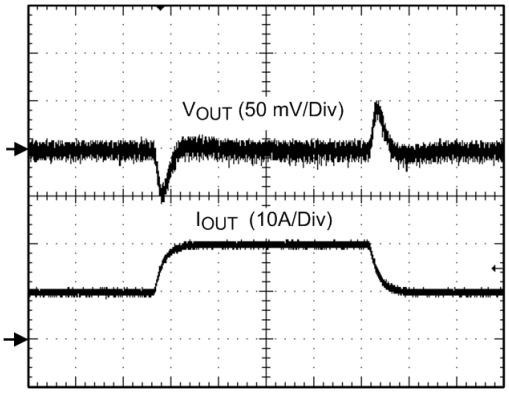


Figure 44. 10-A to 20-A Load Transient (100 µs/div)

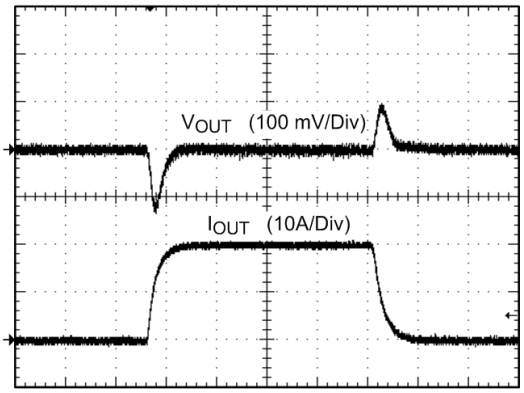


Figure 45. 0-A to 20-A Load Transient (100 µs/div)

8.2.2 Example Circuit 2

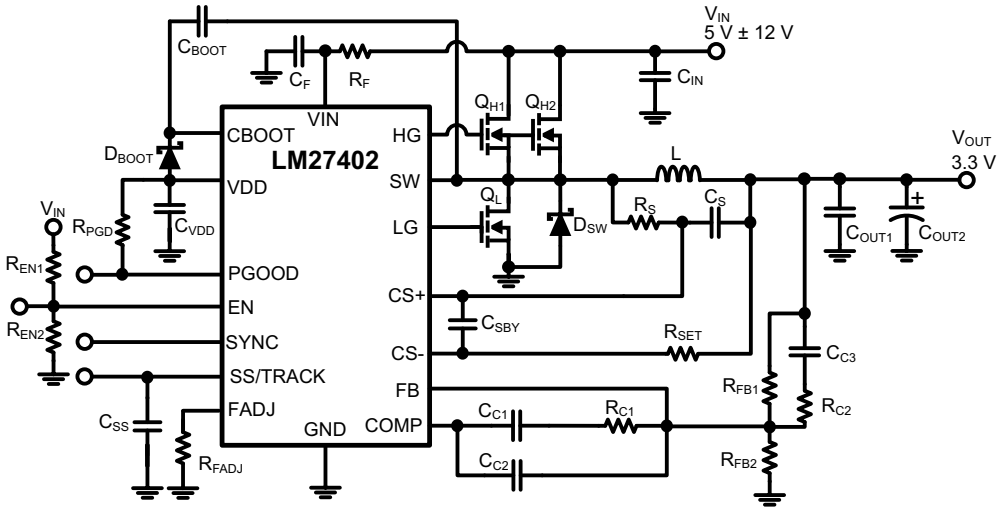


Figure 46. 5-V to 12-V Input Voltage Range, 3.3-V Output, 25-A Output Current, 300-kHz Switching Frequency

Table 2. Bill Of Materials

DESIGNATOR	TYPE	PARAMETERS	PART NUMBER	QTY	MANUFACTURER
U1	IC	Synchronous Buck Voltage-Mode PWM Controller	LM27402	1	TI
C_{BOOT}	Capacitor	0.22 µF, Ceramic, X7R, 25 V, 10%	GRM188R71E224KA88D	1	Murata
C_{C1}	Capacitor	1200 pF, Ceramic, COG, 50 V, 5%	GRM1885C1H122JA01D	1	Murata
C_{C2}	Capacitor	56 pF, Ceramic, COG, 50 V, 5%	GRM1885C1H560JA01D	1	Murata
C_{C3}	Capacitor	820 pF, Ceramic, COG, 50 V, 5%	GRM1885C1H821JA01D	1	Murata
C_{VDD}	Capacitor	1 µF, Ceramic, X5R, 25 V, 10%	GRM188R61E105KA12D	1	Murata
C_F	Capacitor	1 µF, Ceramic, X5R, 25 V, 10%	GRM188R61E105KA12D	1	Murata
C_{IN}	Capacitor	22 µF, Ceramic, X5R, 25 V, 10%	GRM32ER61E226KE15L	5	Murata
$C_{OUT\ 1}$	Capacitor	100 µF, Ceramic, X5R, 6.3 V, 20%	C1210C107M9PACTU	1	Kemet
C_{OUT2}	Capacitor	330 µF, POSCAP, 6.3 V, 20%	6TPE1330MIL	1	Sanyo
C_S	Capacitor	0.22 µF, Ceramic, X7R, 25 V, 10%	GRM188R71E224KA88D	1	Murata
C_{SS}	Capacitor	47000 pF, Ceramic, X7R, 16 V, 10%	GRM188R71E473KA01D	1	Murata
C_{SBY}	Capacitor	100 pF, Ceramic, C0G, 50 V, 5%	GRM1885C1H101JA01D	1	Murata
D_{BOOT}	Diode	Schottky Diode, Average I = 100 mA, Max Surge I = 750 mA	CMOSH-3	1	Central Semi
D_{SW}	Diode	Schottky Diode, Average I = 3 A, Max Surge I = 80A	CMSH3-40M	1	Central Semi
L_{OUT}	Inductor	1 µH, 0.9 mΩ	SER2010-102ML	1	Coilcraft
Q_L	N-CH MOSFET	30 V, 60 A, 43.5 nC, $R_{DS(on)}$ at 4.5V = 1.85 mΩ	Si7192DP	1	Vishay
$Q_{H(1,2)}$	N-CH MOSFET	25 V, 50 A, 20 nC, $R_{DS(on)}$ at 4.5V = 3.4 mΩ	SiR892DP	1	Vishay
R_{C1}	Resistor	18.7 kΩ, 1%, 0.1 W	CRCW060318K7FKEA	1	Vishay
R_{C2}	Resistor	4.75 kΩ, 1%, 0.1 W	CRCW06034K75FKEA	1	Vishay
R_{FADJ}	Resistor	45.3 kΩ, 1%, 0.1 W	CRCW060345K3FKEA	1	Vishay
R_{FB1}	Resistor	20.0 kΩ, 1%, 0.1 W	CRCW060320K0FKEA	1	Vishay
R_{FB2}	Resistor	4.42 kΩ, 1%, 0.1 W	CRCW06034K42FKEA	1	Vishay
R_F	Resistor	2.2Ω, 5%, 0.1 W	CRCW06032R20JNEA	1	Vishay
R_{PGD}	Resistor	51.1 kΩ, 5%, 0.1 W	CRCW060351K1JNEA	1	Vishay
R_S	Resistor	4.12 kΩ, 1%, 0.1 W	CRCW06034K12FKEA	1	Vishay
R_{SET}	Resistor	4.53 kΩ, 1%, 0.1 W	CRCW06034K53FKEA	1	Vishay

8.2.3 Example Circuit 3

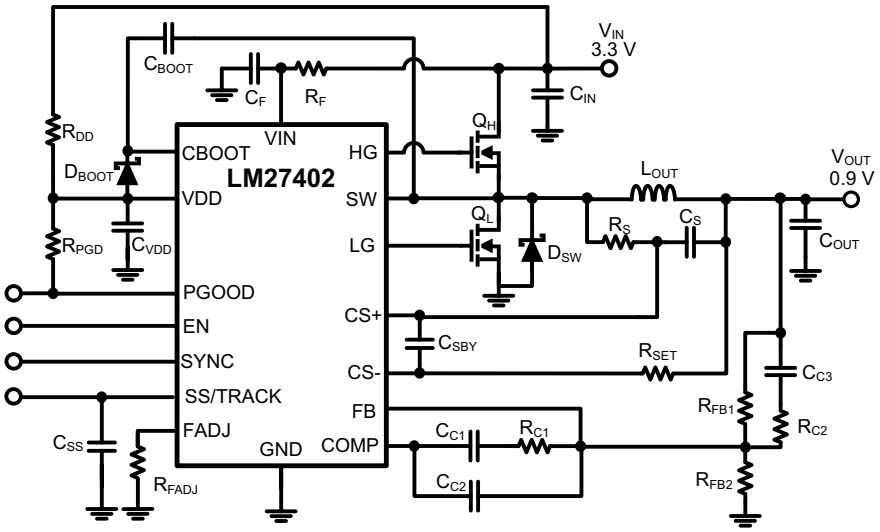


Figure 47. 3.3-V Input voltage, 0.9-V Output Voltage, 20-A Output Current, 500-kHz Switching Frequency

Table 3. Bill Of Materials

DESIGNATOR	TYPE	PARAMETERS	PART NUMBER	QTY	MANUFACTURER
U1	IC	Synchronous Buck Voltage-Mode PWM Controller	LM27402	1	TI
C_{BOOT}	Capacitor	0.22 µF, Ceramic, X7R, 25 V, 10%	GRM188R71E224KA88D	1	Murata
C_{C1}	Capacitor	820 pF, Ceramic, COG, 50 V, 5%	GRM1885C1H821JA01D	1	Murata
C_{C2}	Capacitor	68 pF, Ceramic, COG, 50 V, 5%	GRM1885C1H680JA01D	1	Murata
C_{C3}	Capacitor	390 pF, Ceramic, COG, 50 V, 5%	GRM1885C1H391JA01D	1	Murata
C_{VDD}	Capacitor	1 µF, Ceramic, X5R, 25 V, 10%	GRM188R61E105KA12D	1	Murata
C_F	Capacitor	1 µF, Ceramic, X5R, 25 V, 10%	GRM188R61E105KA12D	1	Murata
C_{IN}	Capacitor	22 µF, Ceramic, X5R, 25 V, 10%	C2012X5R0J226M	5	TDK
C_{OUT}	Capacitor	100 µF, Ceramic, X5R, 6.3 V, 20%	JMK316BJ107ML	3	Taiyo Yuden
C_S	Capacitor	0.22 µF, Ceramic, X7R, 25 V, 10%	GRM188R71E224KA88D	1	Murata
C_{SS}	Capacitor	22000 pF, Ceramic, X7R, 16 V, 10%	GRM188R71E223KA01D	1	Murata
C_{SBY}	Capacitor	68 pF, Ceramic, C0G, 50 V, 5%	GRM1885C1H680JA01D	1	Murata
D_{BOOT}	Diode	Schottky Diode, Average I = 100 mA, Max Surge I = 750 mA	CMOSH-3	1	Central Semi
D_{SW}	Diode	Schottky Diode, Average I = 3A, Max Surge I = 80 A	CMSH3-40M	1	Central Semi
L_{OUT}	Inductor	0.33 µH, 1.4 mΩ	RL-8250-1.4-R33M	1	Renco
Q_L	N-Ch MOSFET	20 V, 100 A, 64 nC, $R_{DS(on)}$ at 4.5 V = 1.6 mΩ	BSC019N02KS	1	Infineon
Q_H	N-Ch MOSFET	20 V, 100 A, 40 nC, $R_{DS(on)}$ at 4.5 V = 2.1 mΩ	BSC026N02KS	1	Infineon
R_{C1}	Resistor	10.0 kΩ, 1%, 0.1 W	CRCW060310K0FKEA	1	Vishay
R_{C2}	Resistor	150Ω, 1%, 0.1 W	CRCW0603150RFKEA	1	Vishay
R_{DD}	Resistor	1Ω, 5%, 0.1 W	CRCW06031R00JNEA	1	Vishay
R_{FADJ}	Resistor	20.0 kΩ, 1%, 0.1 W	CRCW060320K0FKEA	1	Vishay
R_{FB1}	Resistor	20.0 kΩ, 1%, 0.1 W	CRCW060320K0FKEA	1	Vishay
R_{FB2}	Resistor	40.2 kΩ, 1%, 0.1 W	CRCW060340K2FKEA	1	Vishay
R_F	Resistor	2.2 Ω, 5%, 0.1 W	CRCW06032R20JNEA	1	Vishay
R_{PGD}	Resistor	51.1 kΩ, 5%, 0.1 W	CRCW060351K1JNEA	1	Vishay
R_S	Resistor	1.07 kΩ, 1%, 0.1 W	CRCW06031K07FKEA	1	Vishay
R_{SET}	Resistor	5.11 kΩ, 1%, 0. W	CRCW06035K11FKEA	1	Vishay

9 Power Supply Recommendations

The LM27402 PWM controller is designed to operate from an input voltage supply range between 3 V and 20 V. If the input supply is located more than a few inches from the LM27402-based converter, additional bulk capacitance may be required in addition to ceramic bypass capacitance. Given the negative incremental input impedance of a buck converter, a bulk electrolytic component provides damping to reduce effects of input line parasitic inductance resonating with high-Q ceramic capacitors.

10 Layout

10.1 Layout Guidelines

Careful PCB design and layout are important in a high current, fast switching circuit (with high current and voltage slew rates) to assure appropriate device operation and design robustness. As expected, certain issues must be considered before designing a PCB layout using the LM27402. The main switching loop of the power stage is denoted by 1 in Figure 48. The buck converter topology means that particularly high di/dt current will flow in loop 1, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing its effective loop area. For loop 2 however, the di/dt through inductor L_F and capacitor C_{OUT} is naturally limited by the inductor. Keeping the area of loop 2 small is not nearly as important as that of loop 1. Also important are the gate drive loops of the low-side and high-side MOSFETs, denoted by 3 and 4, respectively, in Figure 48.

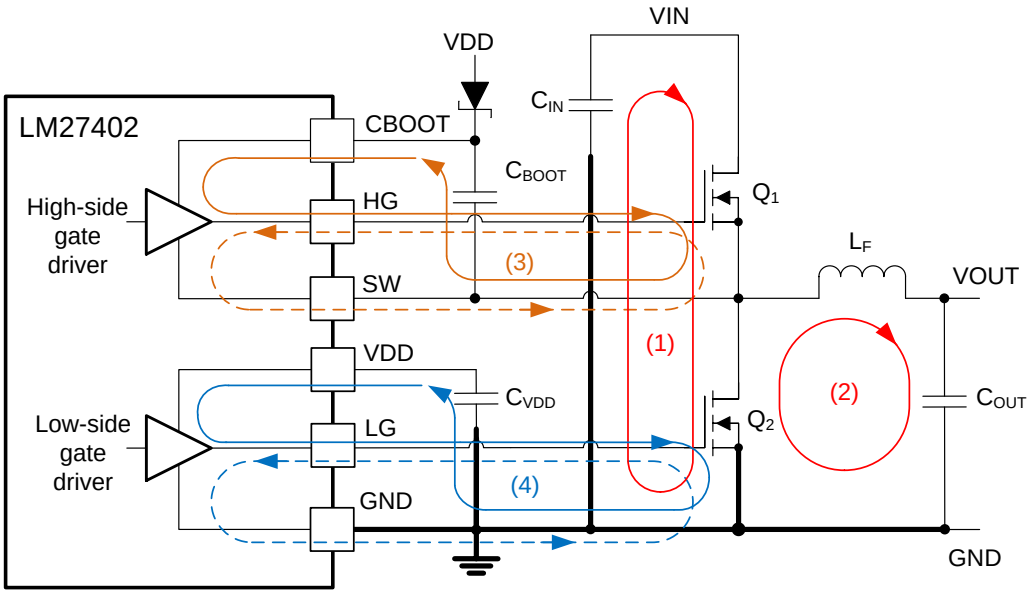


Figure 48. DC/Dc Converter Ground System With Power Stage and Gate Drive Circuit Switching Loops

10.1.1 Power Stage Layout

1. Input capacitor(s), output capacitor(s) and MOSFETs are the constituent components in the power stage of a buck regulator and are typically placed on the top side of the PCB (solder side). Leveraging any system-level airflow, the benefits of convective heat transfer are thus maximized. In a two-sided PCB layout, small-signal components are typically placed on the bottom side (component side). At least one inner plane must be inserted, connected to ground, in order to shield and isolate the small-signal traces from noisy power traces and lines.
2. The DC/Dc converter has several high-current loops. Minimize the area of these loops in order to suppress generated switching noise and parasitic loop inductance and optimize switching performance.
   – Loop 1: The most important loop to minimize the area of is the path from the input capacitor(s) through the high- and low-side MOSFETs, and back to the capacitor(s) through the ground connection. Connect the input capacitor(s) negative terminal close to the source of the low-side MOSFET (at ground). Similarly, connect the input capacitor(s) positive terminal close to the drain of the high-side MOSFET (at VIN). Refer to loop 1 of Figure 48.

Layout Guidelines (continued)

   – Loop 2. The second important loop is the path from the low-side MOSFET through inductor and output capacitor(s), and back to source of the low-side MOSFET through ground. Connect source of the low-side MOSFET and negative terminal of the output capacitor(s) at ground as close as possible. Refer to loop 2 of Figure 48.

3. The PCB trace defined as SW node, which connects to the source of the high-side (control) MOSFET, the drain of the low-side (synchronous) MOSFET and the high-voltage side of the inductor, must be short and wide. However, the SW connection is a source of injected EMI and thus must not be too large.
4. Follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.
5. The SW pin connects to the switch node of the power conversion stage, and it acts as the return path for the high-side gate driver. The parasitic inductance inherent to loop 1 in Figure 48 and the output capacitance (C_{OSS}) of both power MOSFETs form a resonant circuit that induces high frequency (>100 MHz) ringing on the SW node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. Ensure that the peak ringing amplitude does not exceed the absolute maximum rating limit for the SW pin. In many cases, a series resistor and capacitor snubber network connected from the SW node to GND damps the ringing and decreases the peak amplitude. Provide provisions for snubber network components in the printed circuit board layout. If testing reveals that the ringing amplitude at the SW pin is excessive, then include snubber components.

10.1.2 Gate Drive Layout

The LM27402 high- and low-side gate drivers incorporate short propagation delays, adaptive deadtime control and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turn-on and turn-off transitions of the power MOSFETs. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled.

Minimization of stray/parasitic loop inductance is key to optimizing gate drive switching performance, whether it be series gate inductance that resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) that provides a negative feedback component opposing the gate drive command, thereby increasing MOSFET switching times. The following loops are important:

- Loop 3: high-side MOSFET, Q_1. During the high-side MOSFET turn on, high current flows from the boot capacitor through the gate driver and high-side MOSFET, and back to negative terminal of the boot capacitor through the SW connection. Conversely, to turn off the high-side MOSFET, high current flows from gate of the high-side MOSFET through the gate driver and SW, and back to source of the high-side MOSFET through the SW trace. Refer to loop 3 of Figure 48.
- Loop 4: low-side MOSFET, Q_2. During the low-side MOSFET turn on, high current flows from VDD decoupling capacitor through the gate driver and low-side MOSFET, and back to negative terminal of the capacitor through ground. Conversely, to turn off the low-side MOSFET, high current flows from gate of the low-side MOSFET through the gate driver and GND, and back to source of the low-side MOSFET through ground. Refer to loop 4 of Figure 48.

The following circuit layout guidelines are strongly recommended when designing with high-speed MOSFET gate drive circuits.

1. Connections from gate driver outputs, HG and LG, to the respective gate of the high-side or low-side MOSFET should be as short as possible to reduce series parasitic inductance. Use 0.65 mm (25 mils) or wider traces. Use via(s), if necessary, of at least 0.5 mm (20 mils) diameter along these traces. Route HG and SW gate traces as a differential pair from the LM27403 to the high-side MOSFET, taking advantage of flux cancellation.
2. Minimize the current loop path from the VDD and CBOOT pins through their respective capacitors as these provide the high instantaneous current to charge the MOSFET gate capacitances. Specifically, locate the bootstrap capacitor, C_{BOOT}, close to the LM27402's CBOOT and SW pins to minimize the area of loop 3 associated with the high-side driver. Similarly, locate the VDD capacitor, C_{VDD}, close to the LM27402's VDD and GND pins to minimize the area of loop 4 associated with the low-side driver.
3. Placing a 2-Ω to 10-Ω BOOT resistor in series with the BOOT capacitor slows down the high-side MOSFET turn-on transition, serving to reduce the voltage ringing and peak amplitude at the SW node at the expense of increased MOSFET turn-on power loss.

Layout Guidelines (continued)

10.1.3 Controller Layout

Components related to the analog and feedback signals, current limit setting and temperature sense are considered in the following:

1. In general, separate power and signal traces, and use a ground plane to provide noise shielding.
2. Place all sensitive analog traces and components such as COMP, FB, FADJ, and SS/TRACK away from high-voltage switching nodes such as SW, HG, LG or CBOOT. Use internal layer(s) as ground plane(s). Pay particular attention to shielding the feedback (FB) trace from power traces and components.
3. The upper feedback resistor can be connected directly to the output voltage sense point at the load device or the bulk capacitor at the converter side. This connections can be used for the purpose of remote sensing at the downstream load; however, care must be taken to route the trace to prevent noise coupling from noisy nets.
4. Connect the OCP setpoint resistor from CS– pin to VOUT and make the connections as close as possible to the LM27402. The trace from the CS– pin to the resistor must avoid coupling to a high-voltage switching node. Similar precautions apply if a resistor is tied to the CS+ pin.
5. Minimize the current loop from the VDD and VIN pins through their respective decoupling capacitors to the GND pin. In other words, locate these capacitors as close as possible to the LM27402.

10.1.4 Thermal Design and Layout

The useful operating temperature range of a PWM controller with integrated gate drivers and bias supply LDO regulator is greatly affected by:

- Average gate drive current requirements of the power MOSFETs
- Switching frequency
- Operating input voltage (affecting LDO voltage drop and hence its power dissipation)
- Thermal characteristics of the package and operating environment

In order for a PWM controller to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The LM27402 controller is available in small 4-mm × 4-mm WQFN-24 (RUM) and 4.4-mm × 5-mm HTSSOP-16 (PWP) PowerPAD™ packages to cover a range of application requirements. The thermal metrics of these packages are summarized in the *Thermal Information* section of this datasheet. For detailed information regarding the thermal information table, please refer to *IC Package Thermal Metrics*, SPRA953, application report.

Both package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. While the exposed pad of the LM27402's package is not directly connected to any leads of the package, it is thermally connected to the substrate of the device (ground). This allows a significant improvement in heat-sinking, and it becomes imperative that the PCB is designed with thermal lands, thermal vias, and a ground plane to complete the heat removal subsystem. The LM27402's exposed pad is soldered to the ground-connected copper land on the PCB directly underneath the device package, reducing the thermal resistance to a very low value.

Numerous vias with a 0.3-mm diameter connected from the thermal land to the internal/solder-side ground plane(s) are vital to help dissipation. In a multi-layer PCB design, a solid ground plane is typically placed on the PCB layer below the power components. Not only does this provide a plane for the power stage currents to flow but it also represents a thermally conductive path away from the heat generating devices.

The thermal characteristics of the MOSFETs also are significant. The high-side MOSFET's drain pad is normally connected to a VIN plane for heat-sinking. The low-side MOSFET's drain pad is tied to the SW plane, but the SW plane area is purposely kept relatively small to mitigate EMI concerns.

10.2 Layout Example

Figure 49 and Figure 50 show an example PCB layout based on the LM27402 20A EVM design. For more details, please see the *LM27402 Evaluation Board User's Guide*, SNVA406.

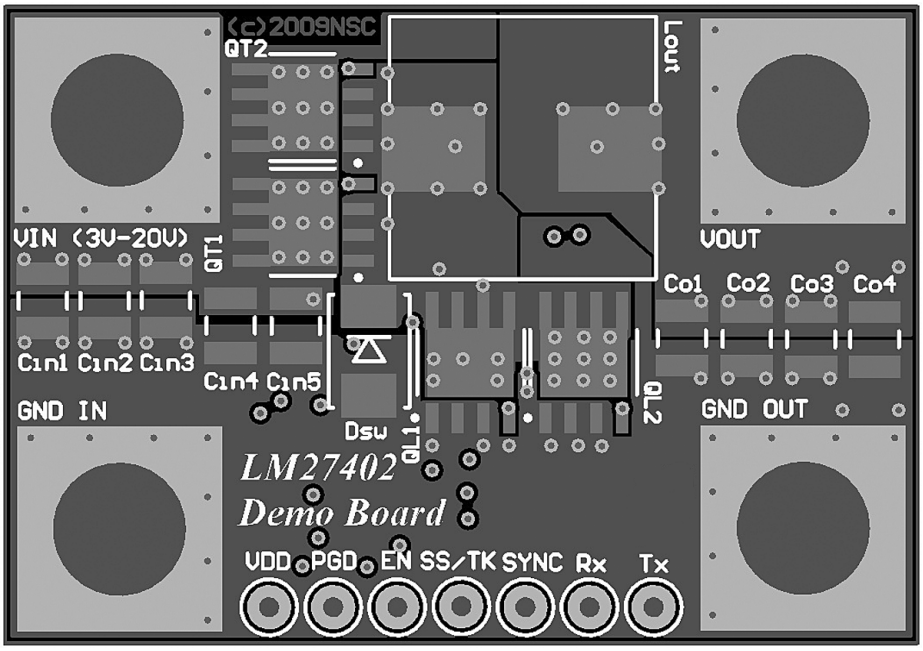


Figure 49. LM27402 PCB Layout – Top Layer

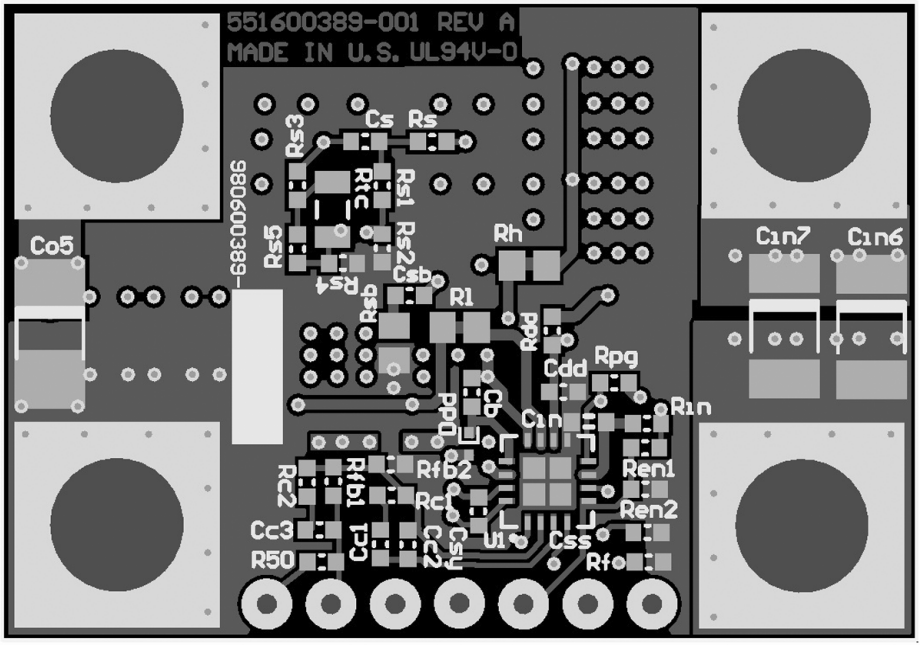


Figure 50. LM27402 PCB Layout – Bottom Layer

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

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11.1.2 開発サポート

11.1.2.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、LM27402デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

- WEBENCH http://www.ti.com/webench
- TI NexFET™パワー・ブロック・モジュールCSD87330Q3D
- *LM27402デザイン・ツール*
- TI Designs

11.2 ドキュメントのサポート

11.2.1 関連資料

- *『LM27402 EVMユーザー・ガイド』*、SNVA406
- *『LM27402 電流制限アプリケーション回路』*、SNVA441
- *『ポイント・オブ・ロード・レギュレータ用、スタートアップ電流可変の6/4ビットVIDプログラム可能電流DAC』*、SNVS822

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

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WEBENCH is a registered trademark of Texas Instruments.
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11.6 静電気放電に関する注意事項

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM27402MH/NOPB	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-	L27402 MH
LM27402MH/NOPB.A	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L27402 MH
LM27402MHX/NOPB	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-	L27402 MH
LM27402MHX/NOPB.A	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L27402 MH
LM27402SQ/NOPB	Active	Production	WQFN (RUM) | 16	1000 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	27402S
LM27402SQ/NOPB.A	Active	Production	WQFN (RUM) | 16	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	27402S
LM27402SQX/NOPB	Active	Production	WQFN (RUM) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	27402S
LM27402SQX/NOPB.A	Active	Production	WQFN (RUM) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	27402S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

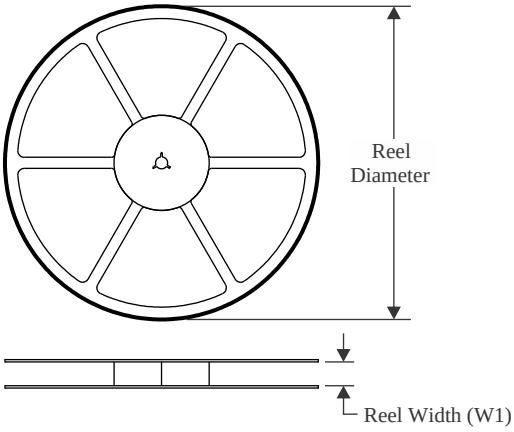
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

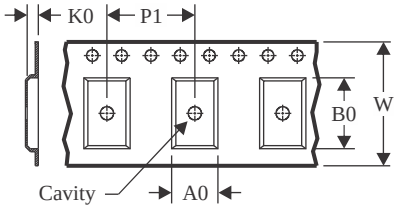
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

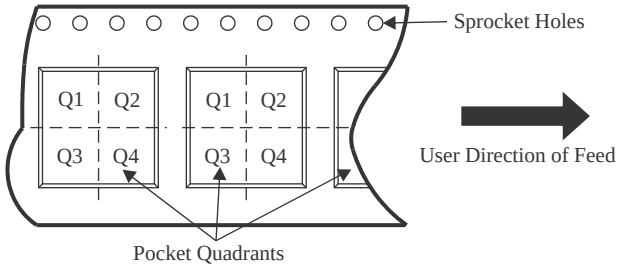


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

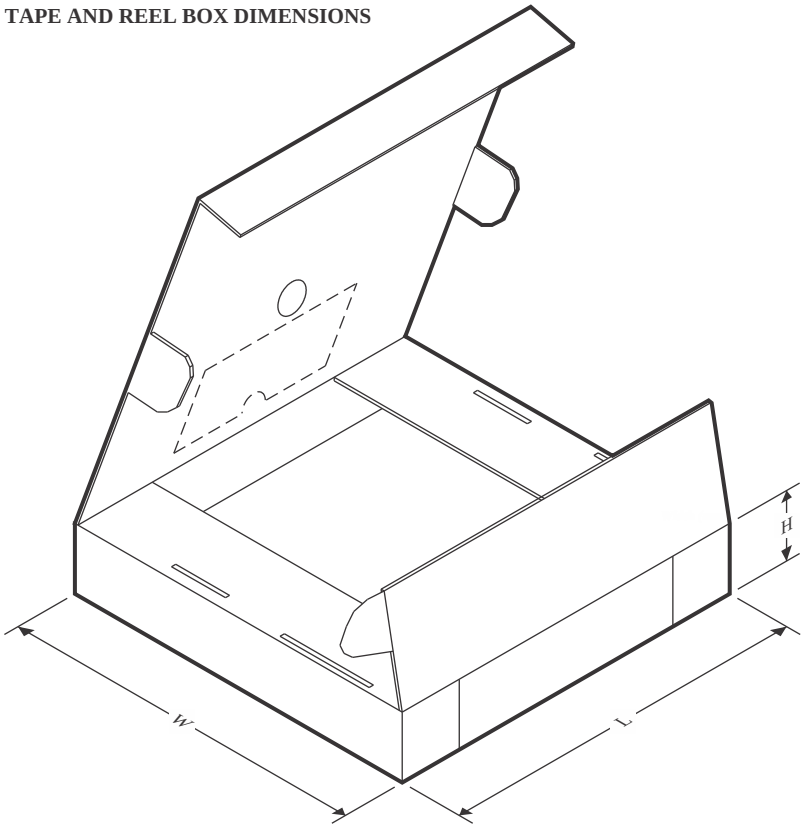
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM27402MHX/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM27402SQ/NOPB	WQFN	RUM	16	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM27402SQX/NOPB	WQFN	RUM	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

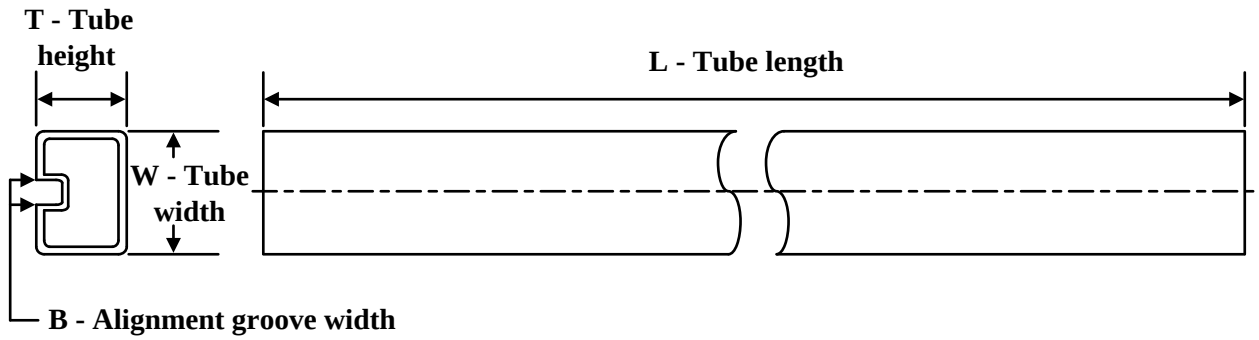
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM27402MHX/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0
LM27402SQ/NOPB	WQFN	RUM	16	1000	210.0	185.0	35.0
LM27402SQX/NOPB	WQFN	RUM	16	4500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

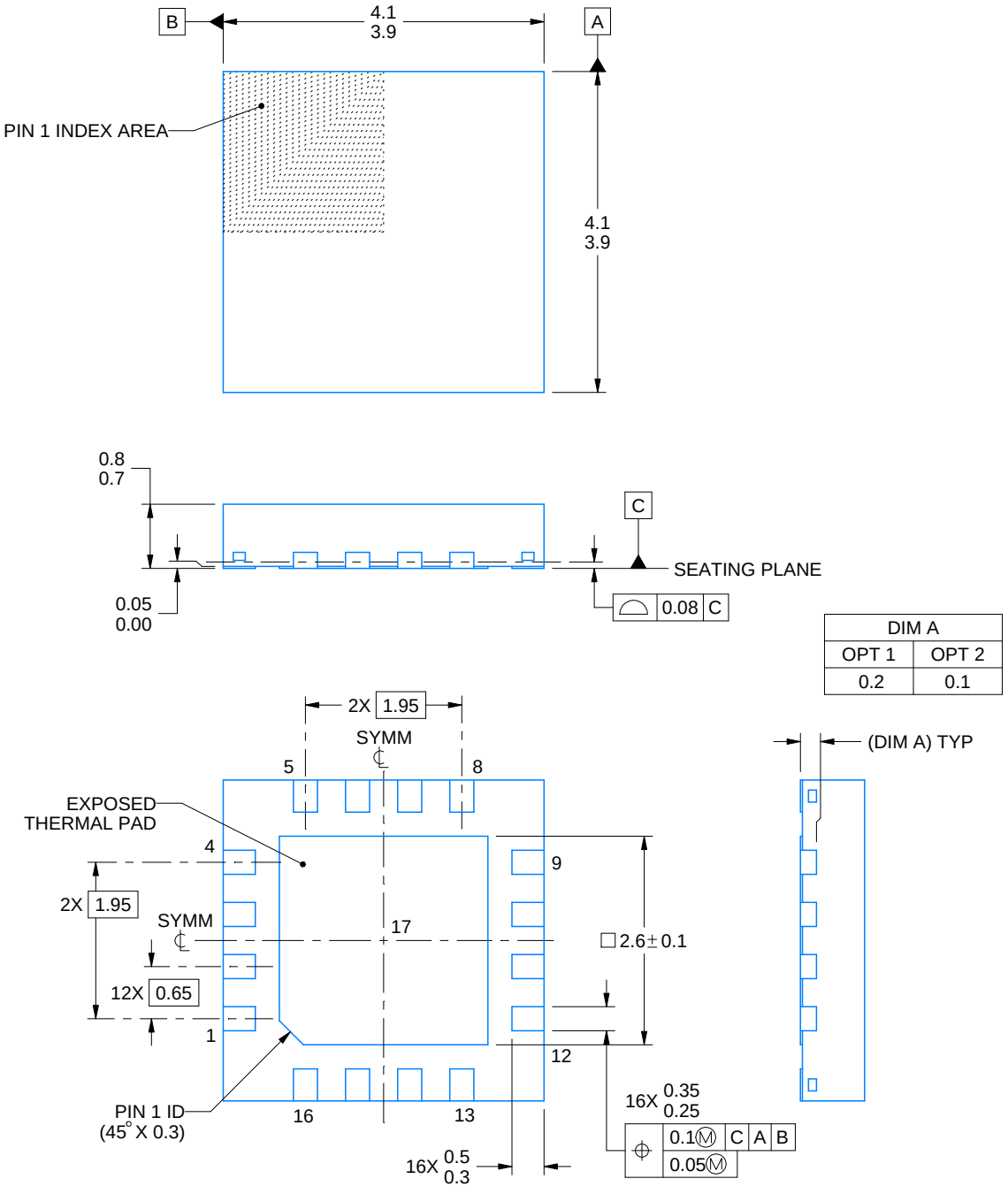
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM27402MH/NOPB	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM27402MH/NOPB.A	PWP	HTSSOP	16	92	495	8	2514.6	4.06

RUM0016A

PACKAGE OUTLINE

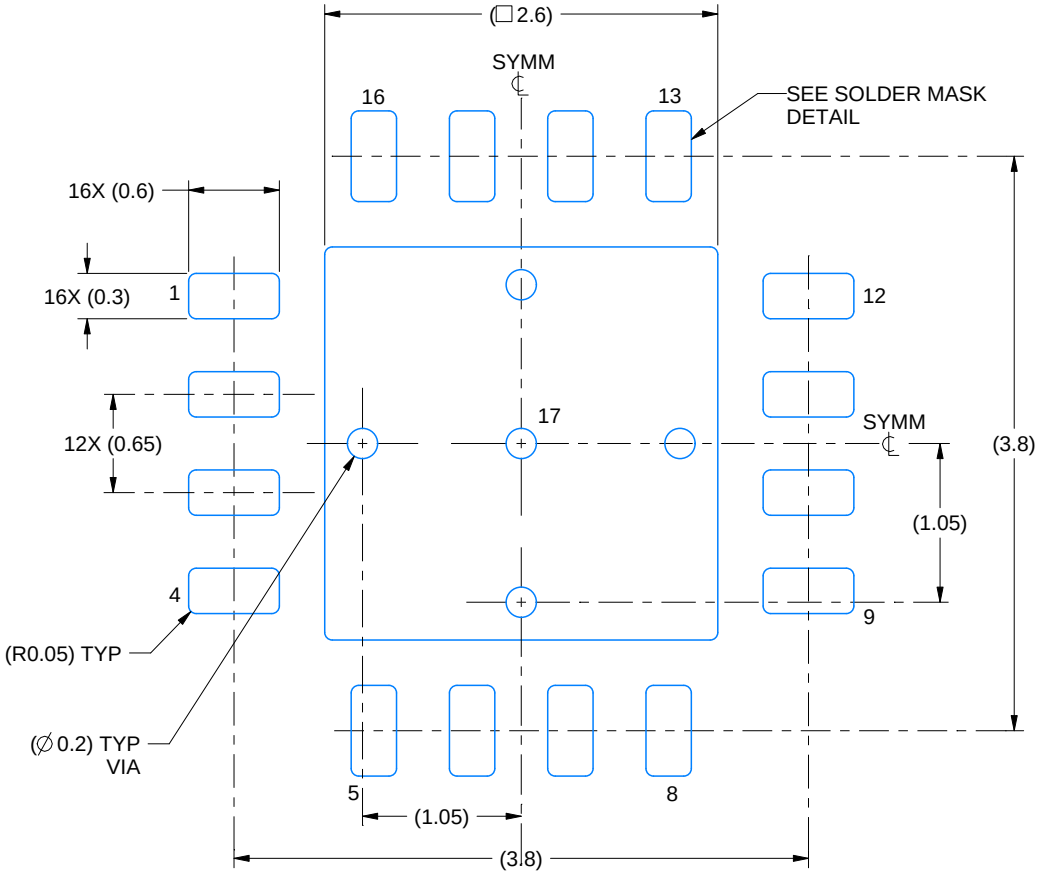
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

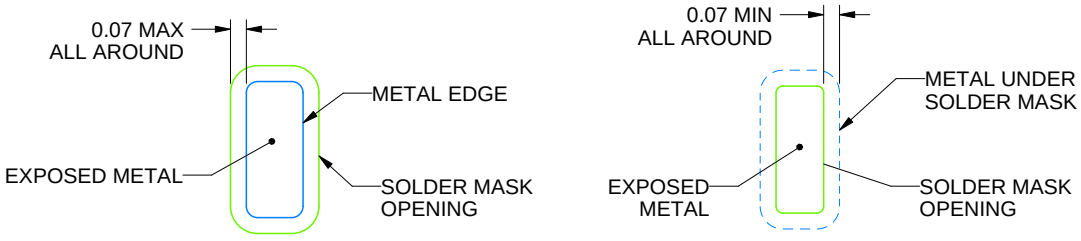


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214998/A 11/2021

NOTES: (continued)

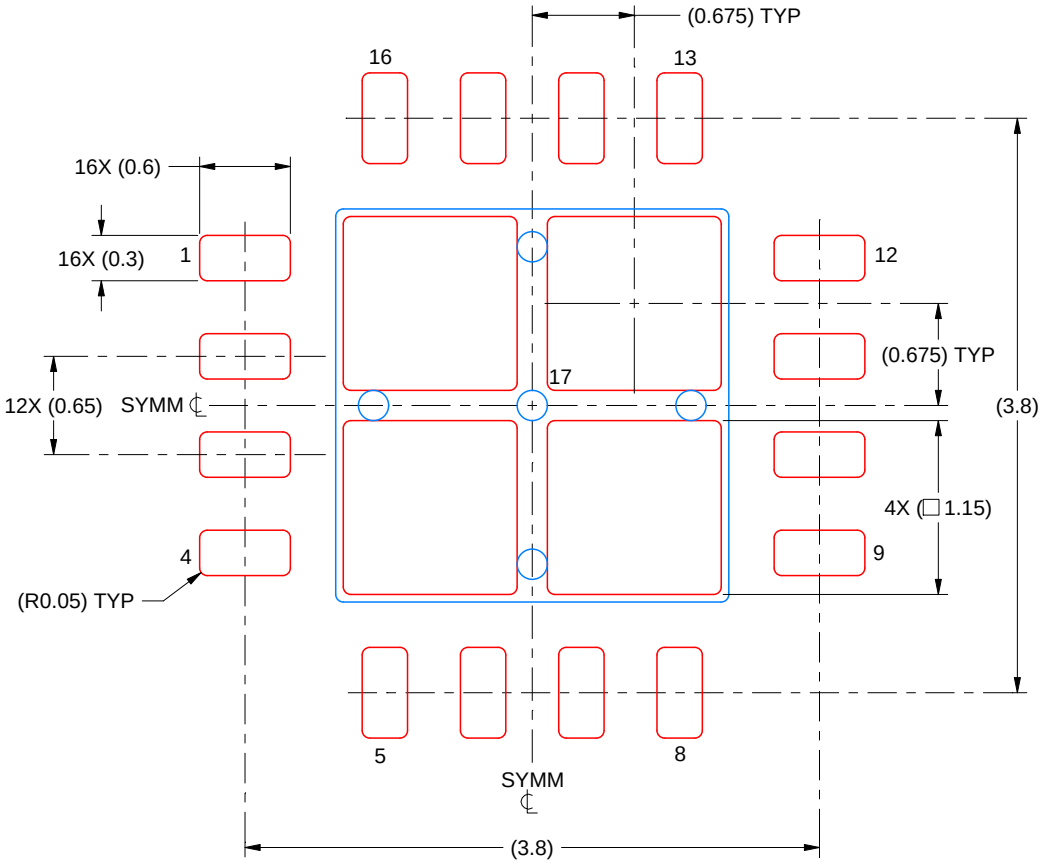
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUM0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



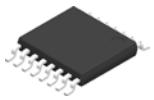
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4214998/A 11/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

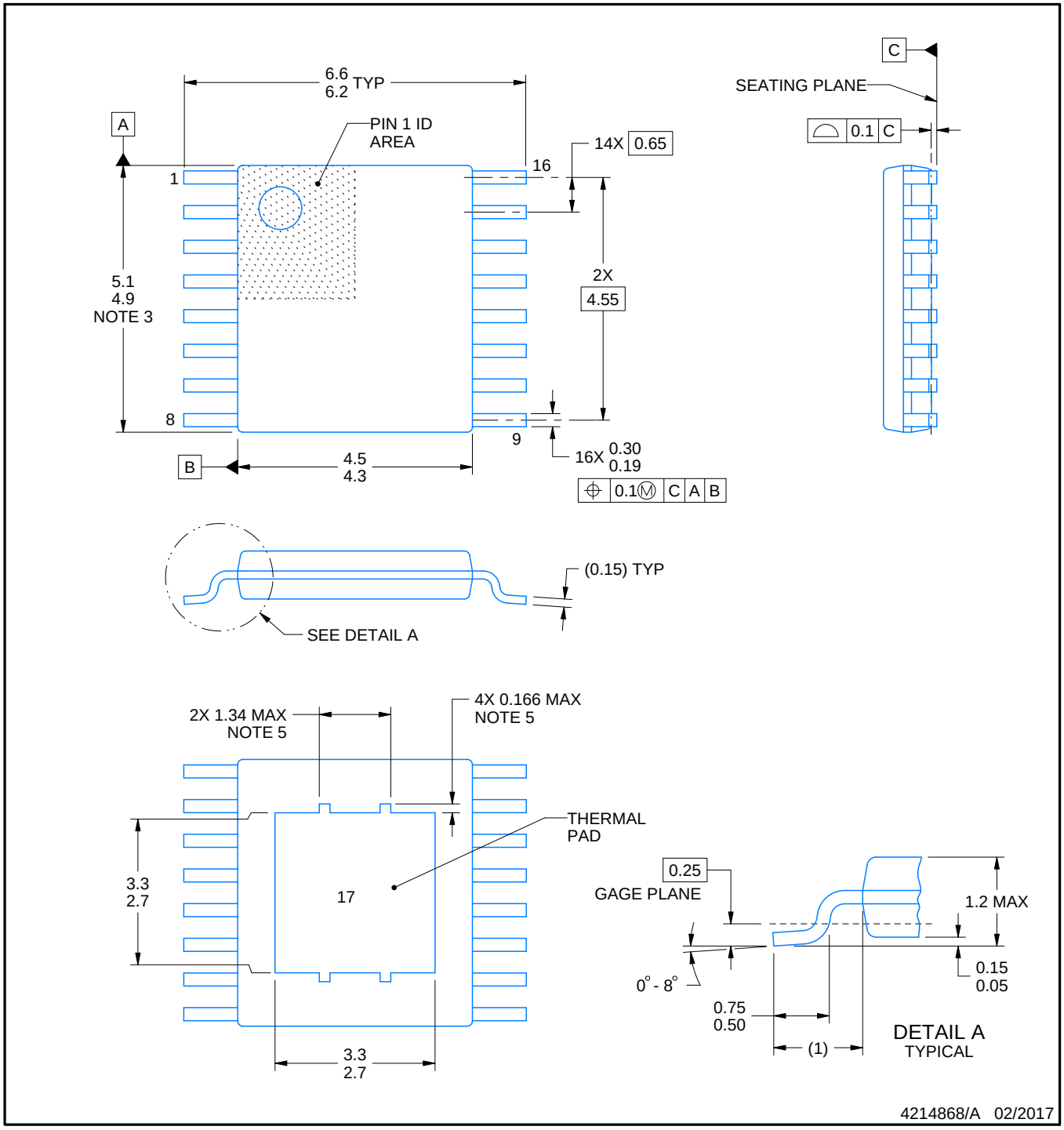


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

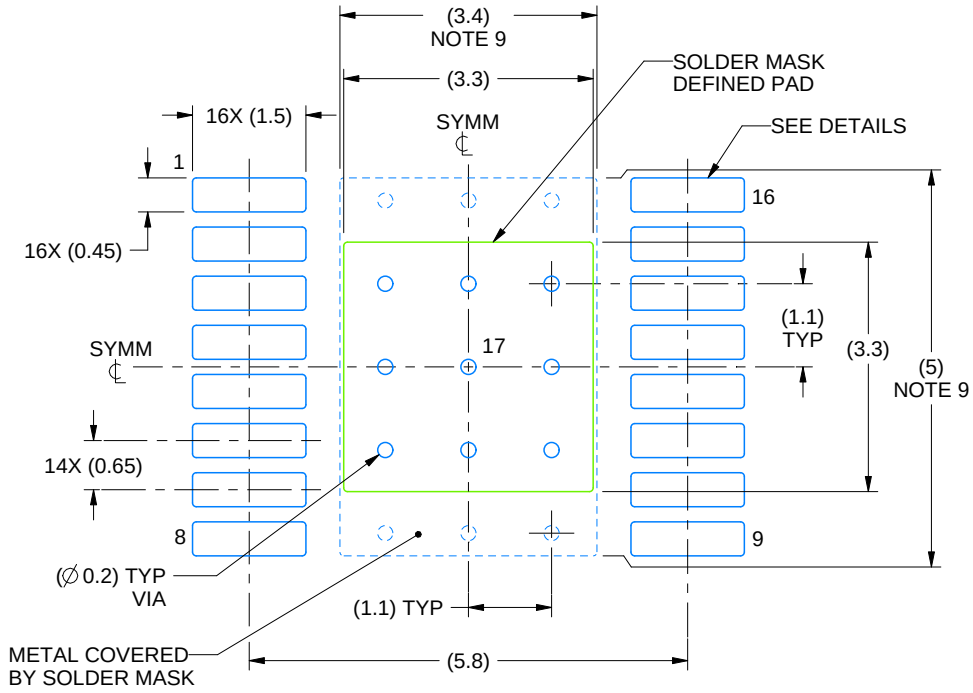
PLASTIC SMALL OUTLINE



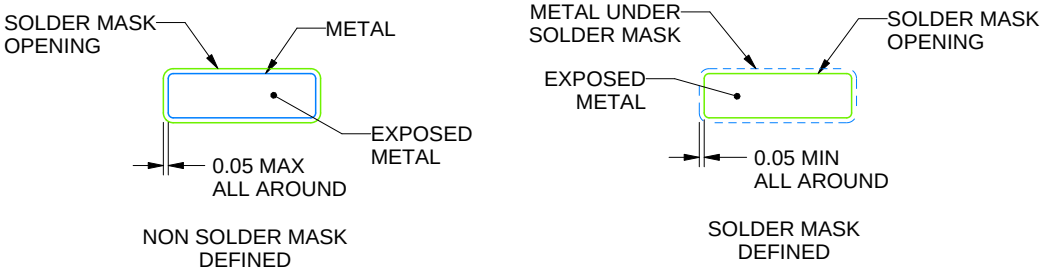
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

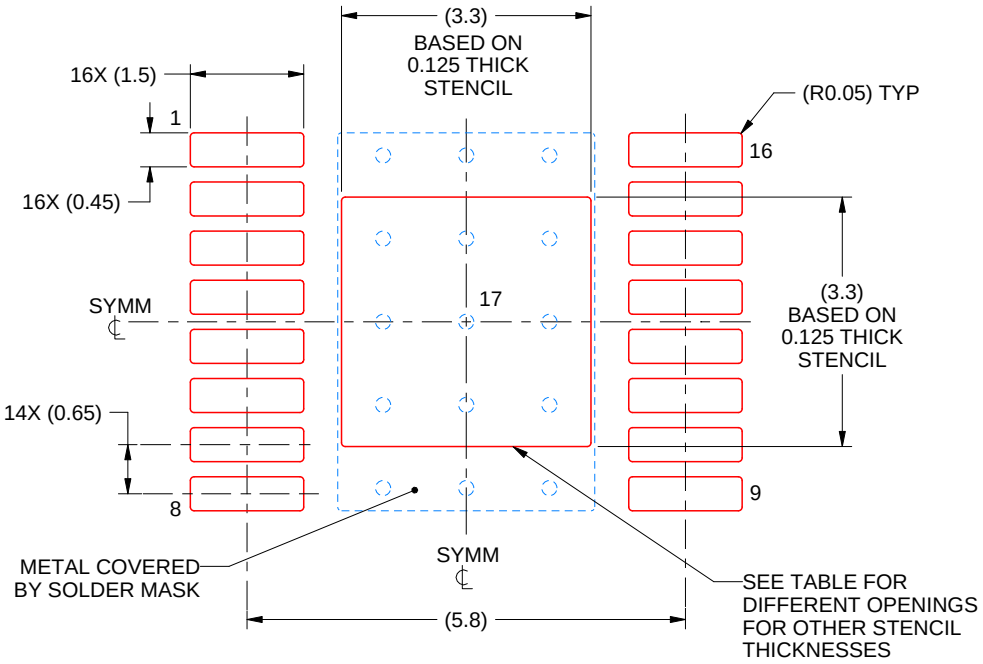


SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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最終更新日：2025 年 10 月