IWR2243 76～81GHz シングルチップ FMCW トランシーバ

1 特長

- FMCW トランシーバ
  - PLL、トランスミッタ、レシーバ、ベースバンド、ADC を内蔵
  - 76～81GHz 帯で使用可能帯域幅 5GHz
  - 4 つの受信チャネル
  - 3 つの送信チャネル
  - フラクショナル N PLL を使用した超高精度のチャープ・エンジン
  - TX 出力：13dBm
  - RX ノイズ指数：13dB
  - 1MHz での位相ノイズ：
    - -96dBc/Hz (76～77GHz)
    - -94dBc/Hz (77～81GHz)
- 較正および自己テストを内蔵
  - 内蔵ファームウェア (ROM)
  - 周波数および温度の自己較正システム
- ホスト・インターフェイス
  - SPI または I2C により外部プロセッサと通信可能な制御インターフェイス
  - MIPI D-PHY および CSI2 v1.1 を介した外部プロセッサとのデータ・インターフェイス
  - フォルト・レポート用の割り込み
- 機能安全準拠
  - 機能安全アプリケーション向けに開発
  - SIL 3 までの IEC 61508 機能安全システム設計に役立つ資料を入手可能
  - SIL-2 までのハードウェア安全度
  - 安全関連認証
    - TUV SUD により IEC 61508 認証済み (SIL 2 まで)
- IWR2243 の高度な機能
  - 内蔵された自己監視機能によりホスト・プロセッサの関与を限定
  - 複素ベースバンド・アーキテクチャ
  - 複数のデバイスをカスケード接続することで、チャネルの増設が可能
  - 干渉検出機能を内蔵
- パワー・マネージメント
  - 内蔵 LDO ネットワークにより PSRR の向上を実現
  - I/O は 3.3V/1.8V のデュアル電圧に対応
- クロック・ソース
  - 40MHz の外部駆動クロック (方形波 / 正弦波) をサポート
  - 負荷コンデンサ付きの 40MHz 水晶振動子接続をサポート
- ハードウェア設計が簡単
  - 組み立てが簡単で低コストの PCB を設計できる 0.65mm ピッチ、161 ピン、10.4mm × 10.4mm のフリップ・チップ BGA パッケージ
  - 小さなソリューション・サイズ
- 接合部温度範囲：–40℃～105℃

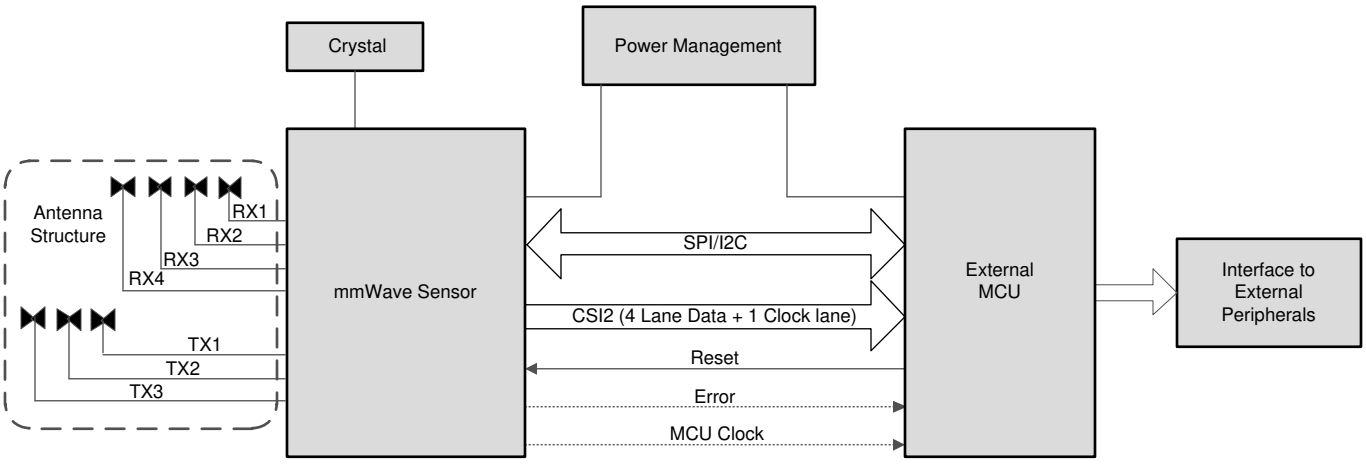


図 1-1. 産業用アプリケーション用レーダー・センサ

2 アプリケーション

- 距離、速度、角度測定向け産業用センサ
- ロボット
- 交通監視
- セキュリティと監視
- ファクトリ・オートメーションの安全保護
- カスケード構成によるイメージング・レーダー

3 概要

IWR2243 は、76～81GHz 帯で動作可能な統合型シングルチップ FMCW トランシーバです。このデバイスは、超小型のフォーム・ファクタで、かつてないレベルの統合を実現しています。IWR2243 は、低消費電力で自己監視機能を備えた超高精度の産業用レーダー・システムに最適なソリューションです。

IWR2243 は、レーダー・センサの実装を簡素化する自己完結型 FMCW トランシーバ・シングルチップ・ソリューションです。テキサス・インスツルメンツの低消費電力 45nm RFCMOS プロセスで製造され、PLL および ADC コンバータを内蔵する 3TX / 4RX システムのモノリシック実装を実現しています。プログラミング・モデルを変更するだけで、さまざまなセンサを実装でき、マルチモード・センサの実装においては動的再構成にも対応します。IWR2243 デバイスは、カスケード形式で複数のデバイスの接続をサポートしています。これにより角度分解能が向上し、高性能レーダー・センサの開発に対応できます。

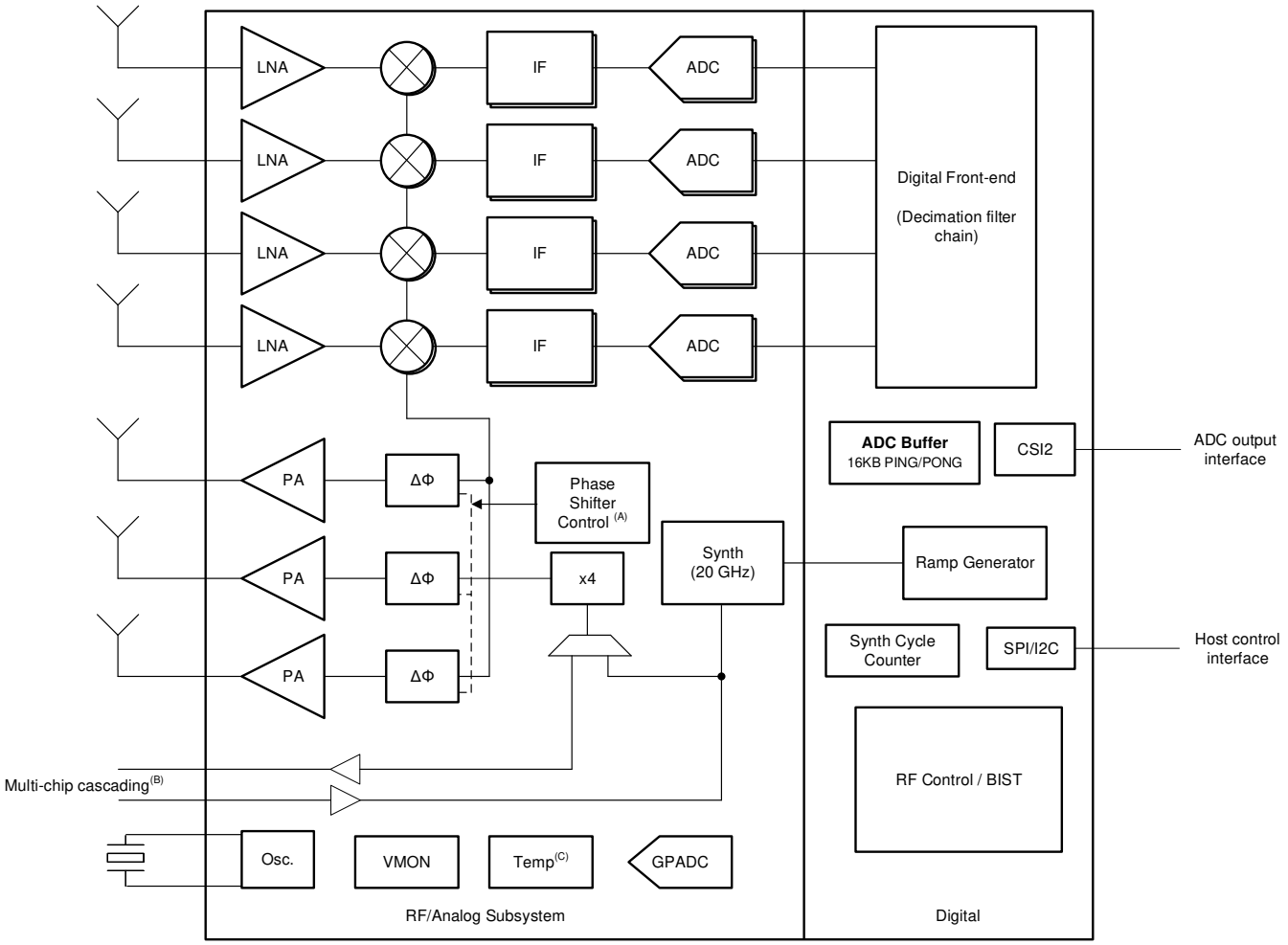
また本デバイスは、リファレンス・ハードウェア・デザイン、ソフトウェア・ドライバ、構成例、API ガイド、ユーザー・マニュアルを含む完全なプラットフォーム・ソリューションとして提供されています。

製品情報

部品番号 (1)	パッケージ	本体サイズ
IWR2243APBGABL (トレイ)	FCBGA (161)	10.4mm × 10.4mm
IWR2243APBGABLR (リール)	FCBGA (161)	10.4mm × 10.4mm

(1) 詳細については、セクション 13、「メカニカル、パッケージ、および注文情報」を参照してください。

4 機能ブロック図



A. 位相シフト制御:
   - 0° / 180° BPM
   - 0° / 180° BPM、分解能 5.625° の制御を選択可能 (IWR2243 および IWR1843)

B. マルチチップのカスケード機能が使用可能

C. 内部温度センサの精度は ±7℃です。

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5 Revision History

DATE	REVISION	NOTES
October 2021	*	Initial Release

6 Device Comparison

表 6-1. Device Features Comparison

FUNCTION		IWR2243P	IWR6843	IWR1843	IWR1642	IWR1443
Number of receivers		4	4	4	4	4
Number of transmitters		3(1)	3(1)	3(1)	2	3
RF frequency range		76 to 81 GHz	60 to 64 GHz	76 to 81 GHz	76 to 81 GHz	76 to 81 GHz
On-chip memory		—	1.75MB	2MB	1.5MB	576KB
Max I/F (Intermediate Frequency) (MHz)		20	10	10	5	15
Max real sampling rate (Msps)		45	25	25	12.5	37.5
Max complex sampling rate (Msps)		22.5	12.5	12.5	6.25	18.75
Functioanl Safety-Compliance		SIL-2	SIL-2	SIL-2 Targeted	—	—
Non-Functional safety variant		—	Yes	Yes	Yes	Yes
Processors						
MCU (R4F)		—	Yes	Yes	Yes	Yes
DSP (C674x)		—	Yes	Yes	Yes	—
Peripherals						
Serial Peripheral Interface (SPI) ports		1	2	2	2	1
Quad Serial Peripheral Interface (QSPI)		Yes	Yes	Yes	Yes	Yes
Inter-Integrated Circuit (I^2C) interface		1	1	1	1	1
Controller Area Network (DCAN) interface		—	—	Yes	Yes	Yes
Controller Area Network (CAN-FD) interface		—	Yes	Yes	—	—
Trace		—	Yes	Yes	Yes	—
PWM		—	Yes	Yes	Yes	—
Hardware In Loop (HIL/DMM)		—	Yes	Yes	Yes	—
GPADC		Yes	Yes	Yes	Yes	Yes
LVDS/Debug (2)		Yes	Yes	Yes	Yes	Yes
CSI2		Yes	—	—	—	Yes
Hardware accelerator		—	Yes	Yes	—	Yes
1-V bypass mode		Yes	Yes	Yes	Yes	Yes
Cascade (20 GHz Sync)		Yes	—	—	—	—
JTAG		—	Yes	Yes	Yes	Yes
Per chirp configurable Tx phase shifter		Yes	—	Yes	—	—
Product status	Product Preview (PP), Advance Information (AI), or Production Data (PD)	PD(3)	PD(3)	PD(3)	PD(3)	PD(3)

(1) 3 Tx Simultaneous operation is supported only with 1-V LDO bypass and PA LDO disable mode. In this mode, the 1-V supply needs to be fed on the VOUT PA pin.
(2) LVDS Interface is not a production Interface and is only used for debug
(3) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

6.1 Related Products

For information about other devices in this family of products or related products see the links that follow.

mmWave Sensors	TI's mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for industrial applications.
mmWave IWR	The Texas Instruments IWRxxxx family of mmWave Sensors are highly integrated and built on RFCMOS technology operating in 76- to 81-GHz or 60- to 64-GHz frequency band. The devices have a closed-loop PLL for precise and linear chirp synthesis, includes a built-in radio processor (BIST) for RF calibration and safety monitoring. The devices have a very small-form factor, low power consumption, and are highly accurate. Industrial applications from long range to ultra short range can be realized using these devices.

7 Terminal Configuration and Functions

7.1 Pin Diagram

図 7-1 shows the pin locations for the 161-pin FCBGA package. 図 7-2, 図 7-3, 図 7-4, and 図 7-5 show the same pins, but split into four quadrants.

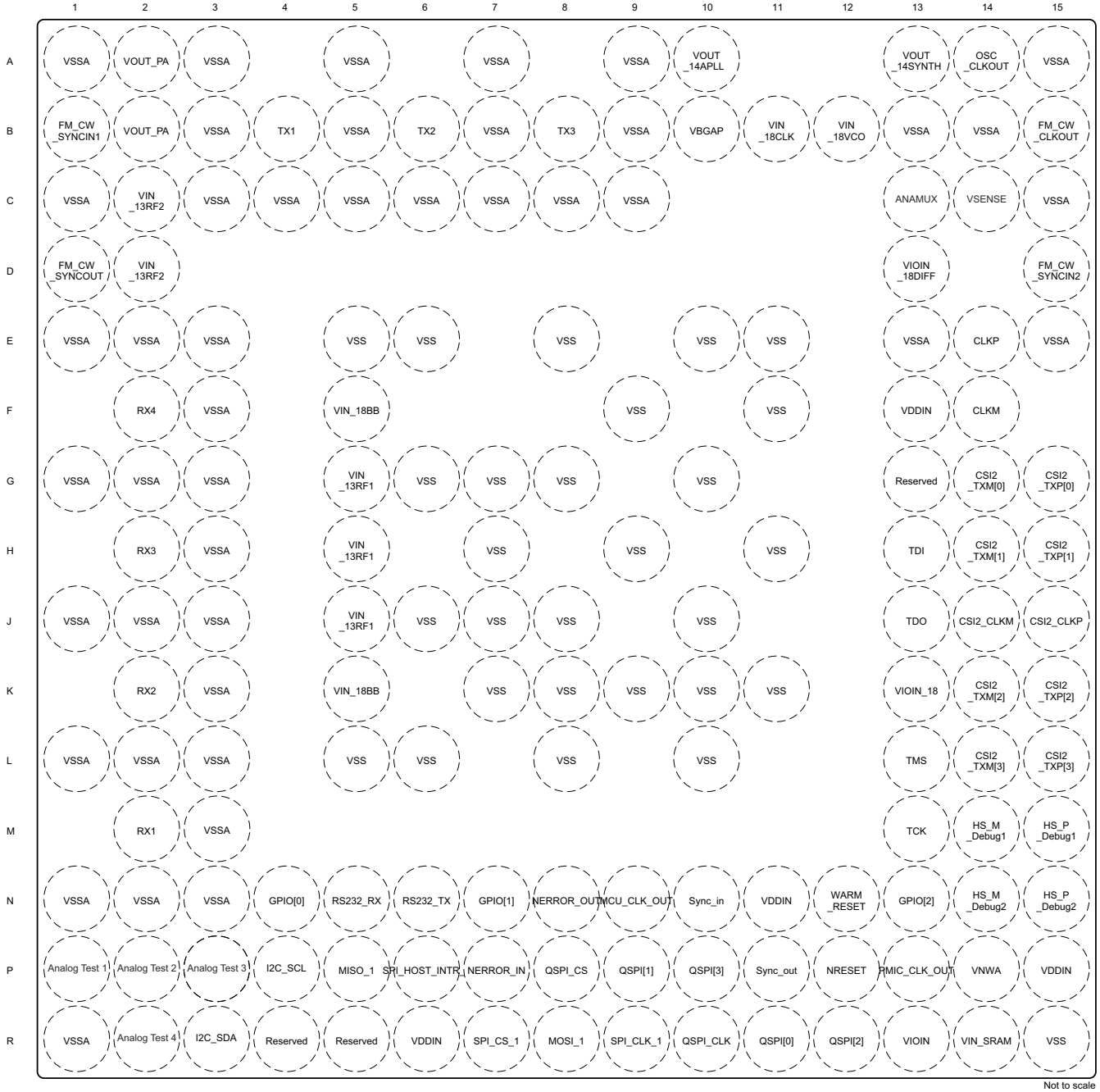


図 7-1. Pin Diagram

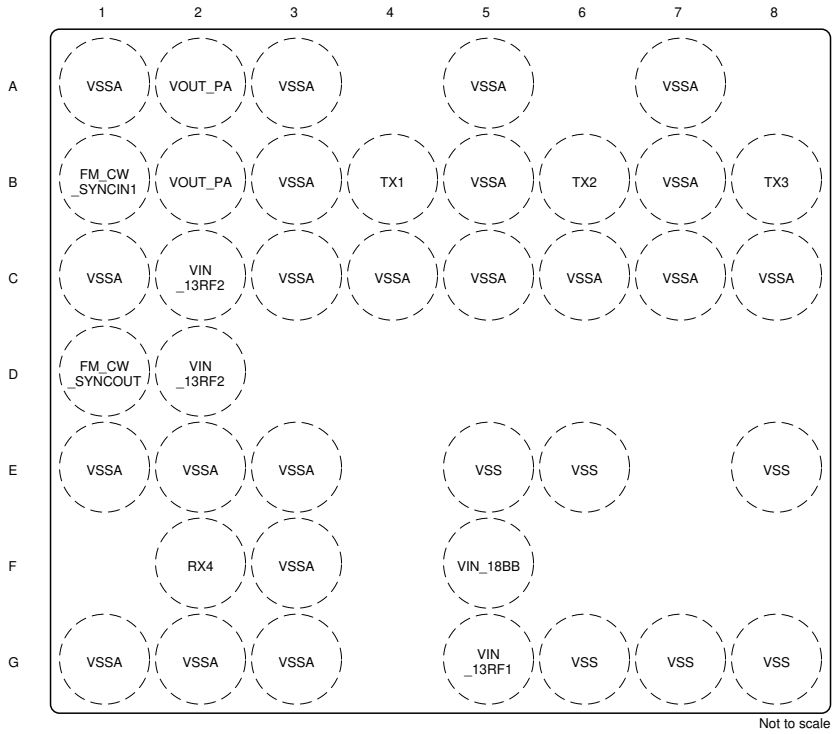


図 7-2. Top Left Quadrant

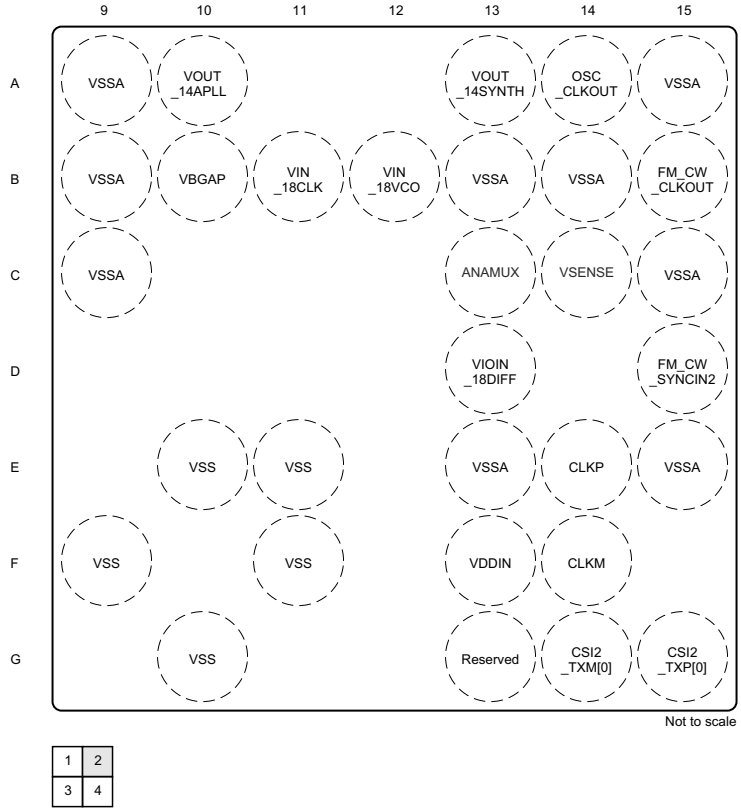


図 7-3. Top Right Quadrant

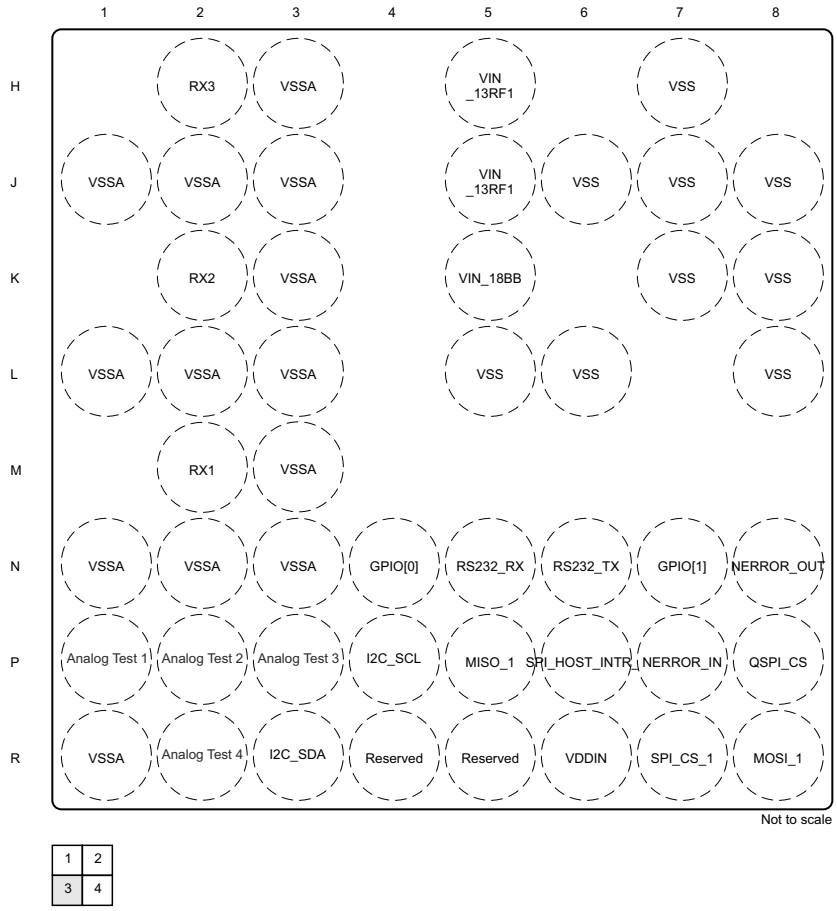


図 7-4. Bottom Left Quadrant

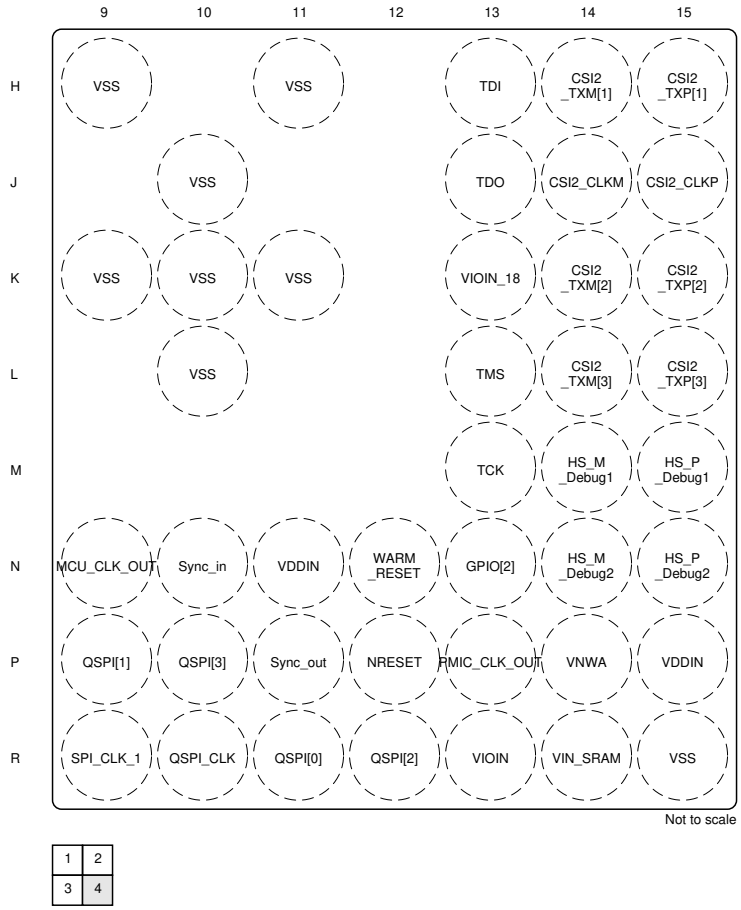


図 7-5. Bottom Right Quadrant

7.2 Signal Descriptions

表 7-1 lists the pins by function and describes that function.

注

All IO pins of the device (except NERROR IN, NERROR_OUT, and WARM_RESET) are non-failsafe; hence, care needs to be taken that they are not driven externally without the VIO supply being present to the device.

表 7-1. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS(1)	DESCRIPTION
Transmitters	TX1	B4	O	—	Single-ended transmitter1 o/p
	TX2	B6	O	—	Single-ended transmitter2 o/p
	TX3	B8	O	—	Single-ended transmitter3 o/p
Receivers	RX1	M2	I	—	Single-ended receiver1 i/p
	RX2	K2	I	—	Single-ended receiver2 i/p
	RX3	H2	I	—	Single-ended receiver3 i/p
	RX4	F2	I	—	Single-ended receiver4 i/p
CSI2 TX	CSI2_TXP[0]	G15	O	—	Differential data Out – Lane 0 (for CSI and LVDS debug interface)
	CSI2_TXM[0]	G14	O	—	
	CSI2_CLKP	J15	O	—	Differential clock Out (for CSI and LVDS debug interface)
	CSI2_CLKM	J14	O	—	
	CSI2_TXP[1]	H15	O	—	Differential data Out – Lane 1 (for CSI and LVDS debug interface)
	CSI2_TXM[1]	H14	O	—	
	CSI2_TXP[2]	K15	O	—	Differential data Out – Lane 2 (for CSI and LVDS debug interface)
	CSI2_TXM[2]	K14	O	—	
	CSI2_TXP[3]	L15	O	—	Differential data Out – Lane 3 (for CSI and LVDS debug interface)
	CSI2_TXM[3]	L14	O	—	
	HS_DEBUG1_P	M15	O	—	Differential debug port 1 (for LVDS debug interface)
	HS_DEBUG1_M	M14	O	—	
	HS_DEBUG2_P	N15	O	—	Differential debug port 2 (for LVDS debug interface)
	HS_DEBUG2_M	N14	O	—	
Chip-to-chip cascading synchronization signals	FM_CW_CLKOUT	B15	O	—	20-GHz single-ended output. Modulated waveform
	FM_CW_SYNCOUT	D1			
	FM_CW_SYNCIN1	B1	I	—	20-GHz single-ended input. Only one of these pins should be used. Multiple instances for layout flexibility.
	FM_CW_SYNCIN2	D15			
Reference clock	OSC_CLKOUT	A14	O	—	Reference clock output from clocking subsystem after cleanup PLL. Can be used by secondary chip in multichip cascading
System synchronization	SYNC_OUT	P11	O	Pull Down	Low-frequency frame synchronization signal output. Can be used by secondary chip in multichip cascading
	SYNC_IN	N10	I	Pull Down	Low-frequency frame synchronization signal input. This signal could also be used as a hardware trigger for frame start

表 7-1. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS[1]	DESCRIPTION
SPI control interface from external MCU (default peripheral mode)	SPI_CS_1	R7	I	Pull Up	SPI chip select
	SPI_CLK_1	R9	I	Pull Down	SPI clock
	MOSI_1	R8	I	Pull Up	SPI data input
	MISO_1	P5	O	Pull Up	SPI data output
	SPI_HOST_INTR_1	P6	O	Pull Down	SPI interrupt to host
Reserved	RESERVED	R4, R5		—	Reserved. For debug purposes, it is recommended to have test points on these pins.
Reset	NRESET	P12	I	—	Power on reset for chip. Active low. The NRESET needs to be pulled low for a minimum of 20 µsec to ensure proper device reset.
	WARM_RESET[2]	N12	O	Open Drain	Open-drain fail-safe warm reset signal. Can be used as a status signal that the device is going through reset.
Sense on Power	SOP2	P13	I	—	The SOP pins are driven externally (weak drive) and the mmWave device senses the state of these pins during bootup to decide the bootup mode. After boot the same pins have other functionality. [SOP2 SOP1 SOP0] = [0 0 1] -> Functional SPI mode [SOP2 SOP1 SOP0] = [1 0 1] -> Flashing mode [SOP2 SOP1 SOP0] = [0 1 1] -> debug mode [SOP2 SOP1 SOP0] = [1 1 1] -> Functional I2C mode
	SOP1	P11	I	—	
	SOP0	J13	I	—	
Safety	NERROR_OUT	N8	O	Open Drain	Open-drain fail-safe output signal. Connected to PMIC/Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset.
	NERROR_IN	P7	I	Open Drain	Fail-safe input to the device. Error output from any other device can be concentrated in the error signaling monitor module inside the device and appropriate action can be taken by firmware
JTAG	TMS	L13	I	Pull Up	JTAG port for TI internal development. For debug purposes, it is recommended to have test points on these pins.
	TCK	M13	I	Pull Down	
	TDI	H13	I	Pull Up	
	TDO	J13	O	—	
Reference oscillator	CLKP	E14	I	—	In XTAL mode: Differential port for reference crystal In External clock mode: Single ended input reference clock port (Output CLKM is grounded in this case)
	CLKM	F14	O	—	
Band-gap voltage	VBGAP	B10	O	—	

表 7-1. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS(1)	DESCRIPTION
Power supply	VDDIN	F13,N11,P15,R6	POW	—	1.2-V digital power supply
	VIN_SRAM	R14	POW	—	1.2-V power rail for internal SRAM
	VNWA	P14	POW	—	1.2-V power rail for SRAM array back bias
	VIOIN	R13	POW	—	I/O supply (3.3-V or 1.8-V): All CMOS I/Os would operate on this supply.
	VIOIN_18	K13	POW	—	1.8-V supply for CMOS IO
	VIN_18CLK	B11	POW	—	1.8-V supply for clock module
	VIOIN_18DIFF	D13	POW	—	1.8-V supply for CSI2 port
	Reserved	G13	POW	—	No connect
	VIN_13RF1	G5,J5,H5	POW	—	1.3-V Analog and RF supply,VIN_13RF1 and VIN_13RF2 could be shorted on the board
	VIN_13RF2	C2,D2	POW	—	
	VIN_18BB	K5,F5	POW	—	1.8-V Analog baseband power supply
	VIN_18VCO	B12	POW	—	1.8-V RF VCO supply
	VSS	E5,E6,E8,E10,E11,F9,F11,G6,G7,G8,G10,H7,H9,H11,J6,J7,J8,J10,K7,K8,K9,K10,K11,L5,L6,L8,L10,R15	GND	—	Digital ground
	VSSA	A1,A3,A5,A7,A9,A15,B3,B5,B7,B9,B13,B14,C1,C3,C4,C5,C6,C7,C8,C9,C15,E1,E2,E3,E13,E15,F3,G1,G2,G3,H3,J1,J2,J3,K3,L1,L2,L3,M3,N1,N2,N3,R1	GND	—	Analog ground
Internal LDO output/inputs	VOUT_14APLL	A10	O	—	
	VOUT_14SYNTH	A13	O	—	
	VOUT_PA	A2,B2	IO	—	When internal PA LDO is used this pin provides the output voltage of the LDO. When the internal PA LDO is bypassed and disabled 1V supply should be fed on this pin. This is mandatory in 3TX simultaneous use case.
External clock out	PMIC_CLK_OUT	P13	O	—	Dithered clock input to PMIC
	MCU_CLK_OUT	N9	O	—	Programmable clock given out to external MCU or the processor
General-purpose I/Os	GPIO[0]	N4	IO	Pull Down	General-purpose IOs. These pins are also used to set the I2C address incase of functional I2C mode. GPIO[2:0] -> 0x000 -> I2C address 0x28 GPIO[2:0] -> 0x001 -> I2C address 0x29 GPIO[2:0] -> 0x111 -> I2C address 0x2F It is recommended that the GPIO[0] signal is connected to the host processor digital pin for debug. For proper operations, the host processor needs to be able to drive a pulse on this pin.
	GPIO[1]	N7	IO	Pull Down	
	GPIO[2]	N13	IO	Pull Down	

表 7-1. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS(1)	DESCRIPTION
I2C interface from external MCU (target mode)	I2C_SDA	R3	IO	Open Drain	I2C data I2C clock The host interface of I2C is selected by booting the device in SOP mode 7 [111]. The I2C address is selected using the GPIO[2:0] pins.
	I2C_SCL	P4	I	Open Drain	
QSPI for Serial Flash	QSPI_CS	P8	O	Pull Up	Chip-select output from the device. Device is a controller connected to serial flash peripheral.
	QSPI_CLK	R10	O	Pull Down	Clock output from the device. Device is a controller connected to serial flash peripheral.
	QSPI[0]	R11	IO	Pull Down	Data IN/OUT
	QSPI[1]	P9	IO	Pull Down	Data IN/OUT
	QSPI[2]	R12	IO	Pull Up	Data IN/OUT
	QSPI[3]	P10	IO	Pull Up	Data IN/OUT
Flash programming and RS232 UART	RS232_TX	N6	O	Pull Down	UART pins for programming external flash For debug purposes, it is recommended to have test points on these pins.
	RS232_RX	N5	I	Pull Up	
GPADC (Test and Debug output for preproduction phase. Can be pinned out on production hardware for field debug)	Analog Test1 / ADC1	P1	IO	—	ADC channel 1(3)
	Analog Test2 / ADC2	P2	IO	—	ADC channel 2(3)
	Analog Test3 / ADC3	P3	IO	—	ADC channel 3(3)
	Analog Test4 / ADC4	R2	IO	—	ADC channel 4(3)
	ANAMUX / ADC5	C13	IO	—	ADC channel 5(3)
	VSENSE / ADC6	C14	IO	—	ADC channel 6(3)

(1) Status of PULL structures associated with the IO after device POWER UP.
(2) For IWR2243, WARM_RESET can be used as an output only pin for status indication.
(3) For details, see セクション 9.4.2

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETERS		MIN	MAX	UNIT
VDDIN	1.2 V digital power supply	–0.5	1.4	V
VIN_SRAM	1.2 V power rail for internal SRAM	–0.5	1.4	V
VNWA	1.2 V power rail for SRAM array back bias	–0.5	1.4	V
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	–0.5	3.8	V
VIOIN_18	1.8 V supply for CMOS IO	–0.5	2	V
VIN_18CLK	1.8 V supply for clock module	–0.5	2	V
VIOIN_18DIFF	1.8 V supply for CSI2 port	–0.5	2	V
VIN_13RF1	1.3 V Analog and RF supply, VIN_13RF1 and VIN_13RF2 could be shorted on the board.	–0.5	1.45	V
VIN_13RF2				
VIN_13RF1	1-V Internal LDO bypass mode. Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed.	–0.5	1.4	V
VIN_13RF2				
VIN_18BB	1.8-V Analog baseband power supply	–0.5	2	V
VIN_18VCO supply	1.8-V RF VCO supply	–0.5	2	V
RX1-4	Externally applied power on RF inputs		10	dBm
TX1-4	Externally applied power on RF outputs(3)		10	dBm
Input and output voltage range	Dual-voltage LVCMOS inputs, 3.3 V or 1.8 V (Steady State)	–0.3V	VIOIN + 0.3	V
	Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8 V (Transient Overshoot/Undershoot) or external oscillator input		VIOIN + 20% up to 20% of signal period	
CLKP, CLKM	Input ports for reference crystal	–0.5	2	V
Clamp current	Input or Output Voltages 0.3 V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O.	–20	20	mA
T_J	Operating junction temperature range	–40	105	°C
T_{STG}	Storage temperature range after soldered onto PC board	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) This value is for an externally applied signal level on the TX. Additionally, a reflection coefficient up to Gamma= 1 can be applied on the TX output.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) (1)	±1000	V
		Charged-device model (CDM)(2)	±250	

(1) ANSI/ESDA/JEDEC JS-001 specification.
(2) ANSI/ESDA/JEDEC JS-002 specification.

8.3 Power-On Hours (POH)

JUNCTION TEMPERATURE (T_j)	OPERATING CONDITION	NOMINAL CVDD VOLTAGE (V)	POWER-ON HOURS [POH] (HOURS)(1)
90% at 85°C T_j 10% at 105°C T_j	50% Duty Cycle	1.2	80,000
100% at 85°C T_j			100,000

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

8.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDIN	1.2 V digital power supply	1.14	1.2	1.32	V
VIN_SRAM	1.2 V power rail for internal SRAM	1.14	1.2	1.32	V
VNWA	1.2 V power rail for SRAM array back bias	1.14	1.2	1.32	V
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	3.135	3.3	3.465	V
		1.71	1.8	1.89	
VIOIN_18	1.8 V supply for CMOS IO	1.71	1.8	1.9	V
VIN_18CLK	1.8 V supply for clock module	1.71	1.8	1.9	V
VIOIN_18DIFF	1.8 V supply for CSI2 port	1.71	1.8	1.9	V
VIN_13RF1	1.3 V Analog and RF supply. VIN_13RF1 and VIN_13RF2 could be shorted on the board	1.23	1.3	1.36	V
VIN_13RF2					
VIN_13RF1 (1-V Internal LDO bypass mode)		0.95	1	1.05	V
VIN_13RF2 (1-V Internal LDO bypass mode)					
VIN18BB	1.8-V Analog baseband power supply	1.71	1.8	1.9	V
VIN_18VCO	1.8V RF VCO supply	1.71	1.8	1.9	V
V_{IH}	Voltage Input High (1.8 V mode)	1.17			V
	Voltage Input High (3.3 V mode)	2.25			
V_{IL}	Voltage Input Low (1.8 V mode)			0.3*VIOIN	V
	Voltage Input Low (3.3 V mode)			0.62	
V_{OH}	High-level output threshold (I_{OH} = 6 mA)	VIOIN – 450			mV
V_{OL}	Low-level output threshold (I_{OL} = 6 mA)			450	mV
NRESET SOP[2:0]	V_{IL} (1.8V Mode)			0.45	V
	V_{IH} (1.8V Mode)	0.96			
	V_{IL} (3.3V Mode)			0.65	
	V_{IH} (3.3V Mode)	1.57			
T_J	Operating junction temperature range	-40		105	℃

8.5 Power Supply Specifications

表 8-1 describes the four rails from an external power supply block of the IWR2243 device.

表 8-1. Power Supply Rails Characteristics

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOS IN THE DEVICE
1.8 V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, CSI2	Input: VIN_18VCO, VIN18CLK, VIN_18BB, VIOIN_18DIFF, VIOIN_18IO LDO Output: VOUT_14SYNTH, VOUT_14APLL
1.3 V (or 1 V in internal LDO bypass mode)(1)	Power Amplifier, Low Noise Amplifier, Mixers and LO Distribution	Input: VIN_13RF2, VIN_13RF1 LDO Output: VOUT_PA
3.3 V (or 1.8 V for 1.8 V I/O mode)	Digital I/Os	Input VIOIN
1.2 V	Core Digital and SRAMs	Input: VDDIN, VIN_SRAM

(1) Three simultaneous transmitter operation is supported only in 1-V LDO bypass and PA LDO disable mode. In this mode 1V supply needs to be fed on the VOUT PA pin.

The 1.3V (1.0V) and 1.8V power supply ripple specifications mentioned in 表 8-2 are defined to meet a target spur level of –105dBc (RF Pin = –15dBm) at the RX. The spur and ripple levels have a dB to dB relationship, for example, a 1dB increase in supply ripple leads to a ~1dB increase in spur level. Values quoted are rms levels for a sinusoidal input applied at the specified frequency.

表 8-2. Ripple Specifications

FREQUENCY (kHz)	RF RAIL		VCO/IF RAIL
	1.0 V (INTERNAL LDO BYPASS) (μV_{RMS})	1.3 V (μV_{RMS})	1.8 V (μV_{RMS})
137.5	7	648	83
275	5	76	21
550	3	22	11
1100	2	4	6
2200	11	82	13
4400	13	93	19
6600	22	117	29

8.6 Power Consumption Summary

表 8-3 and 表 8-4 summarize the power consumption at the power terminals.

表 8-3. Maximum Current Ratings at Power Terminals

PARAMETER(2)	SUPPLY NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
Current consumption	VDDIN, VIN_SRAM, VNWA	Total current drawn by all nodes driven by 1.2V rail			850	mA
	VIN_13RF1, VIN_13RF2	Total current drawn by all nodes driven by 1.3V (or 1V in LDO Bypass mode) rail when 3 transmitters are used (1)			2500	
	VIOIN_18, VIN_18CLK, VIOIN_18DIFF, VIN_18BB, VIN_18VCO	Total current drawn by all nodes driven by 1.8V rail			850	
	VIOIN	Total current drawn by all nodes driven by 3.3V rail			50	

(1) Three transmitters can simultaneously be deployed in the IWR2243 device with 1V / LDO bypass and PA LDO disable mode. In this mode 1V supply needs to be fed on the VOUT PA pin. For a 2Tx use case, the peak 1V supply current goes up to 2000 mA.
(2) The specified current values are at typical supply voltage level.

表 8-4. Average Power Consumption at Power Terminals

PARAMETER	CONDITION		DESCRIPTION	MIN	TYP	MAX	UNIT
Average power consumption in single chip mode.	1.0-V internal LDO bypass mode	1TX, 4RX	The frame is set to 50% duty cycle. 4lane CSI interface is enabled at 600Mbps for ADC data transfer		1.42		W
		2TX, 4RX			1.62		
		3TX, 4RX			1.82		
Average power consumption in Cascade mode for Primary sensor.	1.0-V internal LDO bypass mode	3TX, 4RX	The frame is set to 50% duty cycle. 4lane CSI interface is enabled at 600Mbps for ADC data transfer		1.97		W
Average power consumption in Cascade mode for Secondary sensor.	1.0-V internal LDO bypass mode	3TX, 4RX	The frame is set to 50% duty cycle. 4lane CSI interface is enabled at 600Mbps for ADC data transfer		1.85		W

8.7 RF Specification

over recommended operating conditions and with run time calibrations enabled (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Receiver	Noise figure			13		dB
	1-dB compression point (Out Of Band)(1)			–9		dBm
	Maximum gain			52		dB
	Gain range			20		dB
	Gain step size			2		dB
	Image Rejection Ratio (IMRR)			30		dB
	IF bandwidth(2)				20	MHz
	ADC sampling rate (Real/ Complex 2x)				45	Msps
	ADC sampling rate (Complex 1x)				22.5	Msps
	ADC resolution			12		Bits
	Return loss (S11)			<–10		dB
	Gain mismatch variation (over temperature)			±0.5		dB
	Phase mismatch variation (over temperature)			±3		°
	In-band IIP2	RX gain = 30dB IF = 1.5, 2 MHz at -12 dBFS		16		dBm
	Out-of-band IIP2	RX gain = 24dB IF = 10 KHz at -10 dBm, 1.9 MHz at -30 dBm		24		dBm
	Idle Channel Spurs			–90		dBFS
Transmitter	Output power			13		dBm
	Phase shifter accuracy			±5		°
	Amplitude noise			–145		dBc/Hz
Clock subsystem	Frequency range		76		81	GHz
	Ramp rate				266(3)	MHz/µs
	Phase noise at 1-MHz offset	76 to 78 GHz (VCO1)(4)		–96		dBc/Hz
		76 to 81 GHz (VCO2)		–94		
20 GHz SYNC OUT signal (FM_CW_CLKOUT and FM_CW_SYNCOUT)	Frequency range		19		20.25	GHz
	Output power at the pin		3	7	10	dBm
	Return loss			–9		dB
	Impedance			50		Ω
20 GHz SYNC IN signal (FM_CW_SYNCIN)	Frequency range		19		20.25	GHz
	Input power at the pin		-6		7(5)	dBm
	Return loss			–10		dB
	Impedance			50		Ω

(1) 1-dB Compression Point (Out Of Band) is measured by feeding a continuous wave tone below the lowest HPF cut-off frequency (10 kHz).

(2) The analog IF stages include high-pass filtering, with two independently configurable first-order high-pass corner frequencies. The set of available HPF corners is summarized as follows:

Available HPF Corner Frequencies (kHz)	
HPF1	HPF2
175,235,350,700	350, 700, 1400, 2800

The filtering performed by the digital baseband chain is targeted to provide:

- Less than ±0.5 dB pass-band ripple/droop, and
- Better than 60 dB anti-aliasing attenuation for any frequency that can alias back into the pass-band.

(3) The max ramp rate depends on the PLL bandwidth configuration set using the"AWR_APLL_SYNTH_BW_CONTROL_SB" API. For more details, see the mmWave Interface Control Document.
(4) The phase noise numbers use the following configuration: SYNTH ICP TRIM = 3 , SYNTH RZ TRIM = 8 , and APLL ICP TRIM = 0x26.
(5) At 105°C T_J, the max input level recommended is 3 dBm

図 8-1 shows variations of noise figure and in-band P1dB parameters with respect to receiver gain programmed.

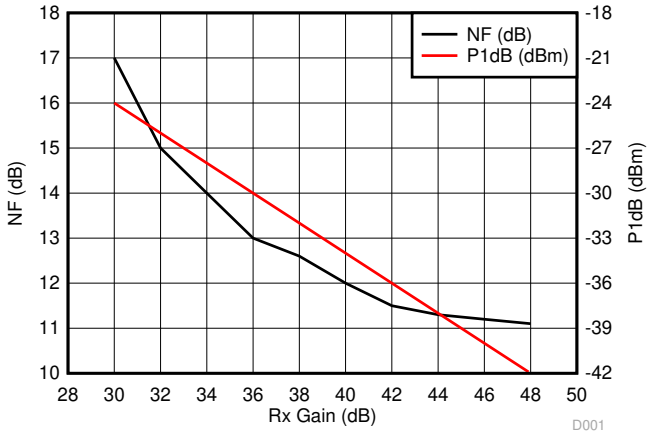


図 8-1. Noise Figure, In-band P1dB vs Receiver Gain

8.8 Thermal Resistance Characteristics for FCBGA Package [ABL0161]

THERMAL METRICS(1)		°C/W(2) (3)
$R\Theta_{JC}$	Junction-to-case	5
$R\Theta_{JB}$	Junction-to-board	5.9
$R\Theta_{JA}$	Junction-to-free air	21.6
$R\Theta_{JMA}$	Junction-to-moving air	15.3(4)
Psi_{JT}	Junction-to-package top	0.69
Psi_{JB}	Junction-to-board	5.8

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.
(3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(4) Air flow = 1 m/s

8.9 Timing and Switching Characteristics

8.9.1 Power Supply Sequencing and Reset Timing

The IWR2243 device expects all external voltage rails and SOP lines to be stable before reset is deasserted. 図 8-2 describes the device wake-up sequence.

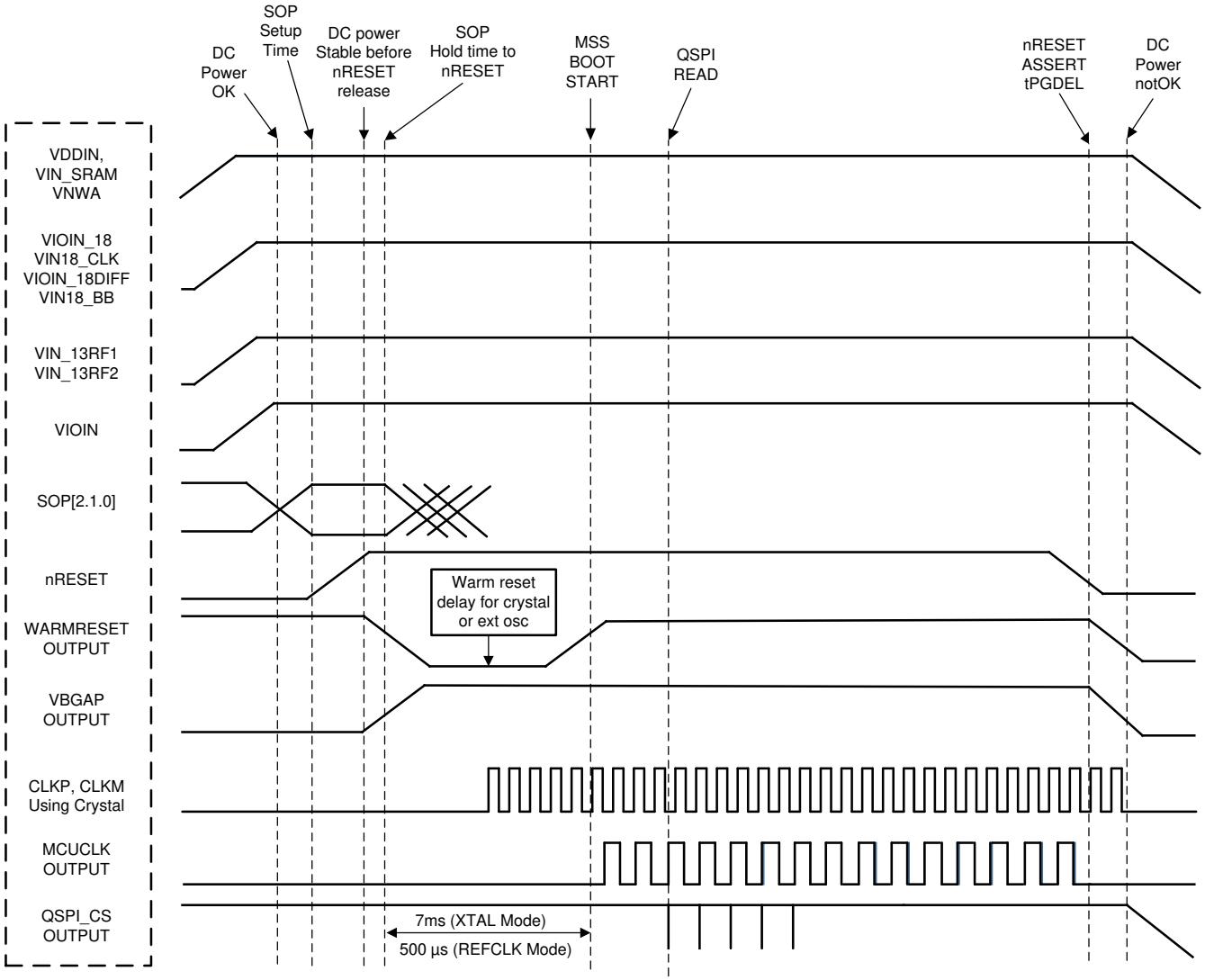


図 8-2. Device Wake-up Sequence

8.9.2 Synchronized Frame Triggering

The IWR2243 device supports a hardware based mechanism to trigger radar frames. An external host can pulse the SYNC_IN signal to start radar frames. The typical time difference between the rising edge of the external pulse and the frame transmission on air (Tlag) is about 160 ns. There is also an additional programmable delay that the user can set to control the frame start time.

The periodicity of the external SYNC_IN pulse should be always greater than the programmed frame periodic in the frame configurations in all instances.

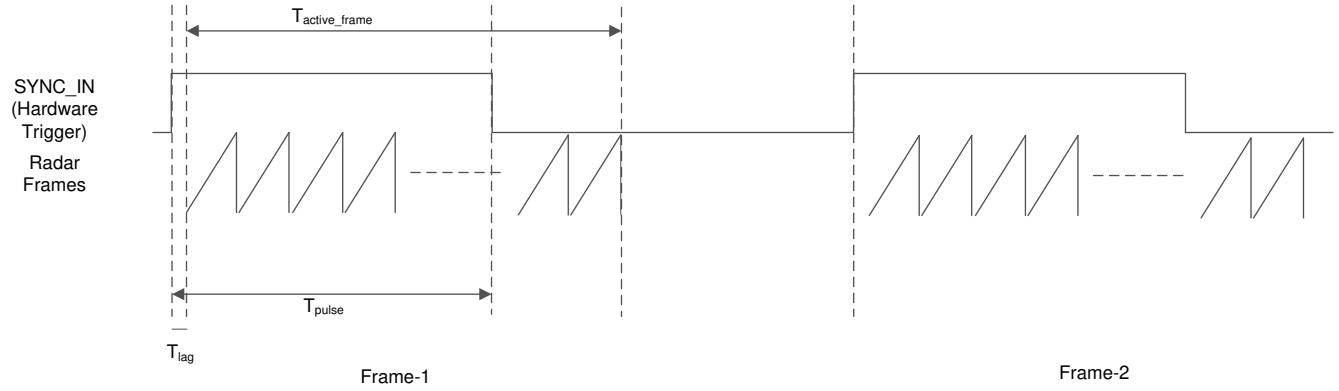


図 8-3. Sync In Hardware Trigger

表 8-5. Frame Trigger Timing

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T_{active_frame}	Active frame duration	User defined		ns
T_{pulse}		25	4000	

8.9.3 Input Clocks and Oscillators

8.9.3.1 Clock Specifications

An external crystal is connected to the device pins. 図 8-4 shows the crystal implementation.

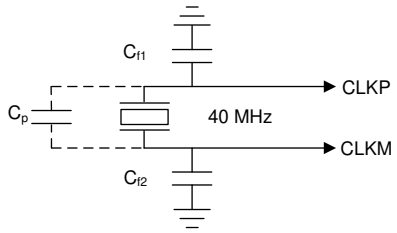


図 8-4. Crystal Implementation

注

The load capacitors, C_{f1} and C_{f2} in 図 8-4, should be chosen such that 式 1 is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins.Note that Cf1 and Cf2 include the parasitic capacitances due to PCB routing.

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \quad (1)$$

表 8-6 lists the electrical characteristics of the clock crystal.

表 8-6. Crystal Electrical Characteristics (Oscillator Mode)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_P	Parallel resonance crystal frequency		40		MHz
C_L	Crystal load capacitance	5	8	12	pF
ESR	Crystal ESR			50	Ω
Temperature range	Expected temperature range of operation	–40		105	°C
Frequency tolerance	Crystal frequency tolerance(1) (2)	-200		200	ppm
Drive level			50	200	µW

(1) The crystal manufacturer's specification must satisfy this requirement.
(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.

In the case where an external clock is used as the clock resource, the signal is fed to the CLKP pin only; CLKM is grounded. The phase noise requirement is very important when a 40-MHz clock is fed externally. 表 8-7 lists the electrical characteristics of the external clock signal.

表 8-7. External Clock Mode Specifications

PARAMETER		SPECIFICATION			UNIT
		MIN	TYP	MAX	
Input Clock: External AC-coupled sine wave or DC-coupled square wave Phase Noise referred to 40 MHz	Frequency		40		MHz
	AC-Amplitude	700		1200	mV (pp)
	DC-$t_{rise/fall}$			10	ns
	Phase Noise at 1 kHz			–132	dBc/Hz
	Phase Noise at 10 kHz			–143	dBc/Hz
	Phase Noise at 100 kHz			–152	dBc/Hz
	Phase Noise at 1 MHz			–153	dBc/Hz
	Duty Cycle	35		65	%
	Freq Tolerance	–50		50	ppm
Input clock requirements for the Secondary device in Cascade mode (assuming the 20Ghz clock is provided from the Primary device)	Phase Noise at 10 kHz			-127	dBc/Hz
	Phase Noise at 100 kHz			-137	dBc/Hz
	Phase Noise at 1 MHz			-147	dBc/Hz
	Period jitter @40Mhz			1.75	ps rms
	Spur levels (sum of all spurs)			-52	dBc

8.9.4 Multibuffered / Standard Serial Peripheral Interface (MibSPI)

8.9.4.1 Peripheral Description

The MibSPI/SPI is a high-speed synchronous serial input/output port that allows a serial bit stream to be shifted into and out of the device at a programmed bit-transfer rate. The MibSPI/SPI is normally used for communication between the microcontroller and external peripherals or another microcontroller.

セクション 8.9.4.1.2 and セクション 8.9.4.1.3 assume the operating conditions stated in セクション 8.9.4.1.1, セクション 8.9.4.1.2, セクション 8.9.4.1.3, and 図 8-5 describe the timing and switching characteristics of the MibSPI.

8.9.4.1.1 SPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

8.9.4.1.2 SPI Peripheral Mode Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPICLK	25			ns
2	$t_{w(SPCH)S}$	Pulse duration, SPICLK high	10			ns
3	$t_{w(SPCL)S}$	Pulse duration, SPICLK low	10			ns
4	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low			10	ns
5	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low	2			ns

8.9.4.1.3 SPI Peripheral Mode Timing Requirements (SPICLK = input, SPISIMO = input, and SPISOMI = output)

NO.			MIN	TYP	MAX	UNIT
6	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high	3			ns
7	$t_{h(SPCH-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK high	1			ns

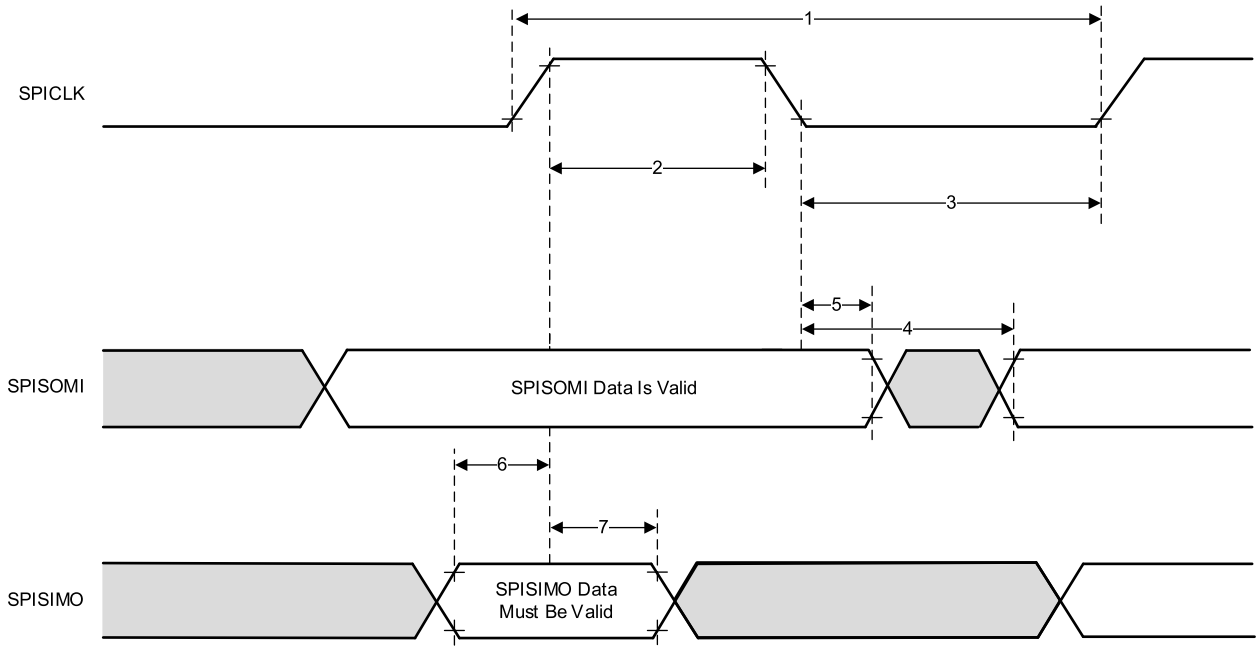


図 8-5. SPI Peripheral Mode External Timing

8.9.4.2 Typical Interface Protocol Diagram (Peripheral Mode)

1. Host should ensure that there is a delay of at least two SPI clocks between CS going low and start of SPI clock.
2. Host should ensure that CS is toggled for every 16 bits of transfer through SPI.

図 8-6 shows the SPI communication timing of the typical interface protocol.

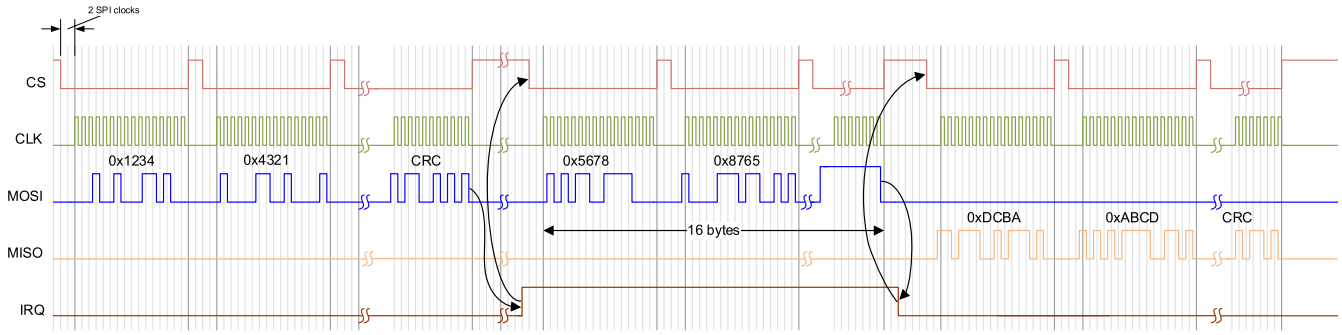


図 8-6. SPI Communication

8.9.5 Inter-Integrated Circuit Interface (I2C)

The inter-integrated circuit (I2C) module is a multi-controller communication module providing an interface between devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an I^{2}C-bus™. This module will support any target or controller I2C compatible device.

The I2C has the following features:

- Compliance to the Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
  - Bit/Byte format transfer
  - 7-bit and 10-bit device addressing modes
  - General call
  - START byte
  - Multi-Controller transmitter/ target receiver mode
  - Multi-Controller receiver/ target transmitter mode
  - Combined controller transmit/receive and receive/transmit mode
  - Transfer rates of 100 kbps
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

注

This I2C module does not support:

- High-speed (HS) mode
- C-bus compatibility mode
- The combined format in 10-bit address mode (the I2C sends the target address second byte every time it sends the target address first byte)

8.9.5.1 I2C Timing Requirements

	(1)	STANDARD MODE		UNIT
		MIN	MAX	
$t_{c(SCL)}$	Cycle time, SCL	10		µs
$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		µs
$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		µs
$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		µs
$t_{w(SCLH)}$	Pulse duration, SCL high	4		µs
$t_{su(SDA-SCLH)}$	Setup time, SDA valid before SCL high	250		µs
$t_{h(SCLL-SDA)}$	Hold time, SDA valid after SCL low	0	3.45(1)	µs
$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		µs
$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		µs
$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			ns
C_b (2) (3)	Capacitive load for each bus line		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) The maximum th(SDA-SCLL) for I2C bus devices has only to be met if the device does not stretch the low period (tw(SCLL)) of the SCL signal.
(3) C_b = total capacitance of one bus line in pF.

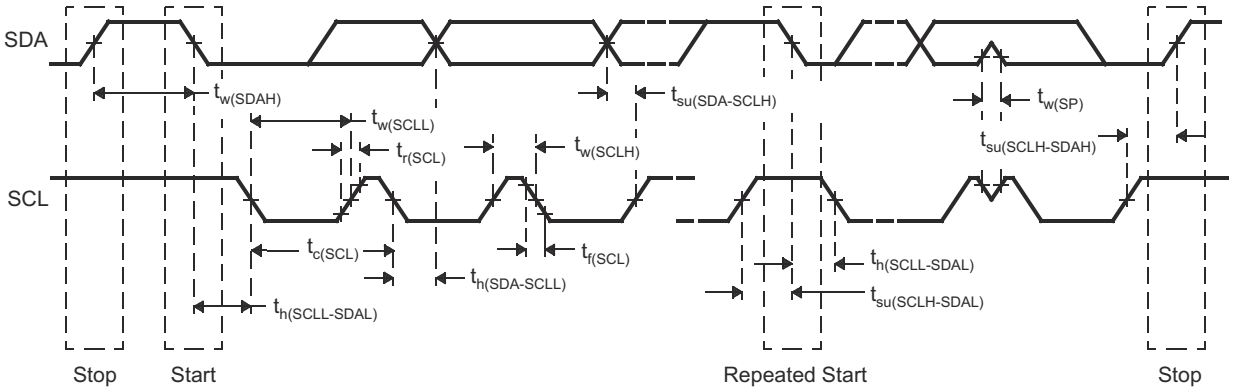


図 8-7. I2C Timing Diagram

注

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum th(SDA-SCLL) has only to be met if the device does not stretch the LOW period (tw(SCLL)) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-SCLH)}$.

8.9.6 Quad Serial Peripheral Interface (QSPI)

The quad serial peripheral interface (QSPI™) module is a kind of SPI module that allows single, dual, or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. The QSPI works as a controller only. The QSPI in the device is primarily intended for fast booting from quad-SPI flash memories.

The QSPI supports the following features:

- Programmable clock divider
- Six-pin interface
- Programmable length (from 1 to 128 bits) of the words transferred
- Programmable number (from 1 to 4096) of the words transferred
- Support for 3-, 4-, or 6-pin SPI interface
- Optional interrupt generation on word or frame (number of words) completion
- Programmable delay between chip select activation and output data from 0 to 3 QSPI clock cycles

Timing Requirements for QSPI Input (Read) Timings and QSPI Switching Characteristics assume the operating conditions stated in QSPI Timing Conditions.

8.9.6.1 QSPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

8.9.6.2 Timing Requirements for QSPI Input (Read) Timings

		MIN(1) (2)	TYP	MAX	UNIT
$t_{su(D-SCLK)}$	Setup time, d[3:0] valid before falling sclk edge (Q12)	7.3			ns
$t_{h(SCLK-D)}$	Hold time, d[3:0] valid after falling sclk edge (Q13)	1.5			ns
$t_{su(D-SCLK)}$	Setup time, final d[3:0] bit valid before final falling sclk edge	7.3 – P(3)			ns
$t_{h(SCLK-D)}$	Hold time, final d[3:0] bit valid after final falling sclk edge	1.5 + P(3)			ns

(1) Clock Mode 0 (clk polarity = 0 ; clk phase = 0) is the mode of operation.
(2) The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.
(3) P = SCLK period in ns.

8.9.6.3 QSPI Switching Characteristics

NO.	PARAMETER(1) (2) (3)		MIN	TYP	MAX	UNIT
Q1	$t_{c(SCLK)}$	Cycle time, sclk	25			ns
Q2	$t_{w(SCLKL)}$	Pulse duration, sclk low	0.5*P – 3			ns
Q3	$t_{w(SCLKH)}$	Pulse duration, sclk high	0.5*P – 3			ns
Q4	$t_{d(CS-SCLK)}$	Delay time, sclk falling edge to cs active edge	–M*P – 1		–M*P + 2.5	ns
Q5	$t_{d(SCLK-CS)}$	Delay time, sclk falling edge to cs inactive edge	N*P – 1		N*P + 2.5	ns
Q6	$t_{d(SCLK-D1)}$	Delay time, sclk falling edge to d[0] transition	–3.5		7	ns
Q7	$t_{ena(CS-D1LZ)}$	Enable time, cs active edge to d[0] driven (lo-z)	–P – 4		–P +1	ns
Q8	$t_{dis(CS-D1Z)}$	Disable time, cs active edge to d[0] tri-stated (hi-z)	–P – 4		–P +1	ns
Q9	$t_{d(SCLK-D1)}$	Delay time, sclk first falling edge to first d[1] transition (for PHA = 0 only)	–3.5 – P		7 – P	ns

(1) The Y parameter is defined as follows: If DCLK_DIV is 0 or ODD then, Y equals 0.5. If DCLK_DIV is EVEN then, Y equals (DCLK_DIV/2) / (DCLK_DIV+1). For best performance, it is recommended to use a DCLK_DIV of 0 or ODD to minimize the duty cycle distortion. The HSDIVIDER on CLKOUTX2_H13 output of DPLL_PER can be used to achieve the desired clock divider ratio. All required details about clock division factor DCLK_DIV can be found in the device-specific Technical Reference Manual.
(2) P = SCLK period in ns.
(3) M = QSPI_SPI_DC_REG.DDx + 1, N = 2

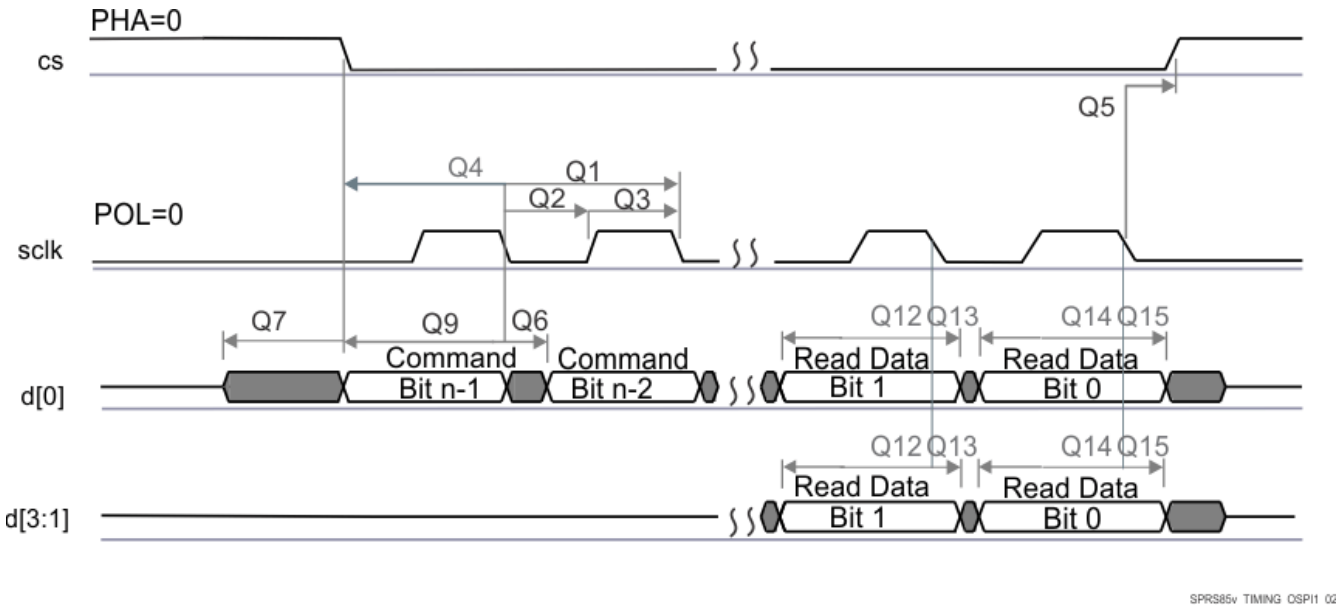


図 8-8. QSPI Read (Clock Mode 0)

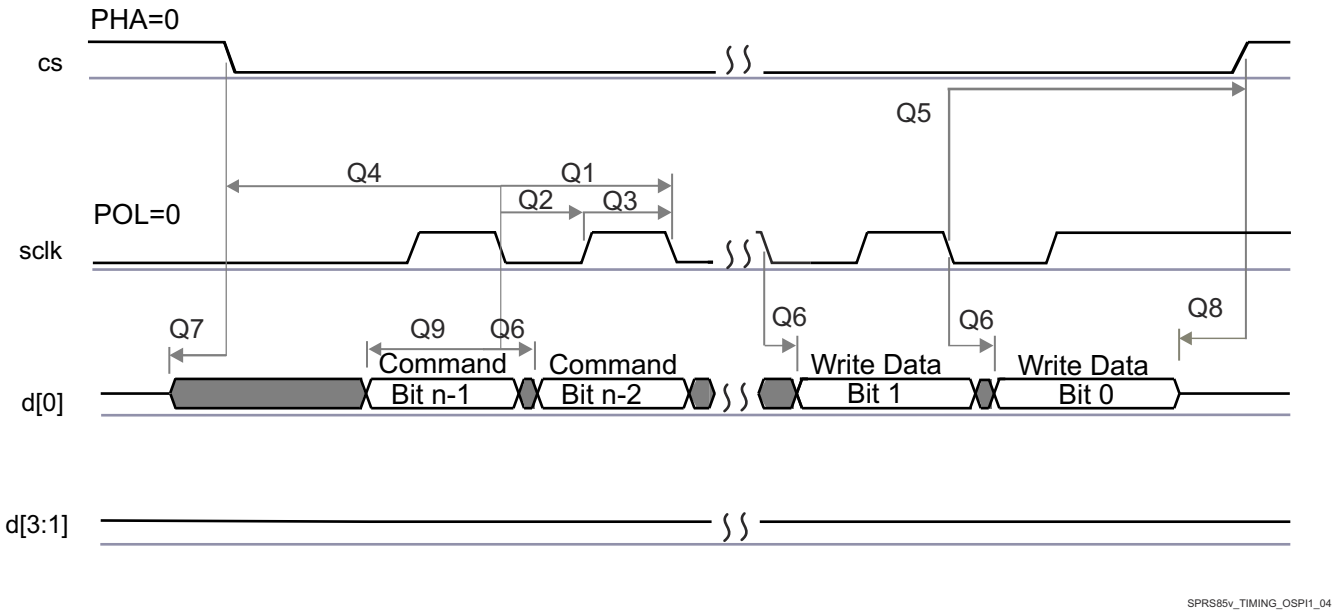


図 8-9. QSPI Write (Clock Mode 0)

8.9.7 LVDS Interface Configuration

The IWR2243 supports seven differential LVDS IOs/Lanes to support debug where raw ADC data could be extracted. The lane configuration supported is four Data lanes (LVDS_TXP/M), one Bit Clock lane (LVDS_CLKP/M) one Frame clock lane (LVDS_FRCLKP/M). The LVDS interface supports the following data rates:

- 900 Mbps (450 MHz DDR Clock)
- 600 Mbps (300 MHz DDR Clock)
- 450 Mbps (225 MHz DDR Clock)
- 400 Mbps (200 MHz DDR Clock)
- 300 Mbps (150 MHz DDR Clock)
- 225 Mbps (112.5 MHz DDR Clock)
- 150 Mbps (75 MHz DDR Clock)

Note that the bit clock is in DDR format and hence the numbers of toggles in the clock is equivalent to data.

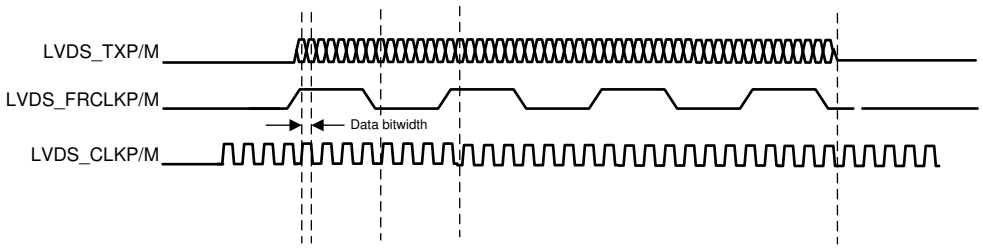


図 8-10. LVDS Interface Lane Configuration And Relative Timings

8.9.7.1 LVDS Interface Timings

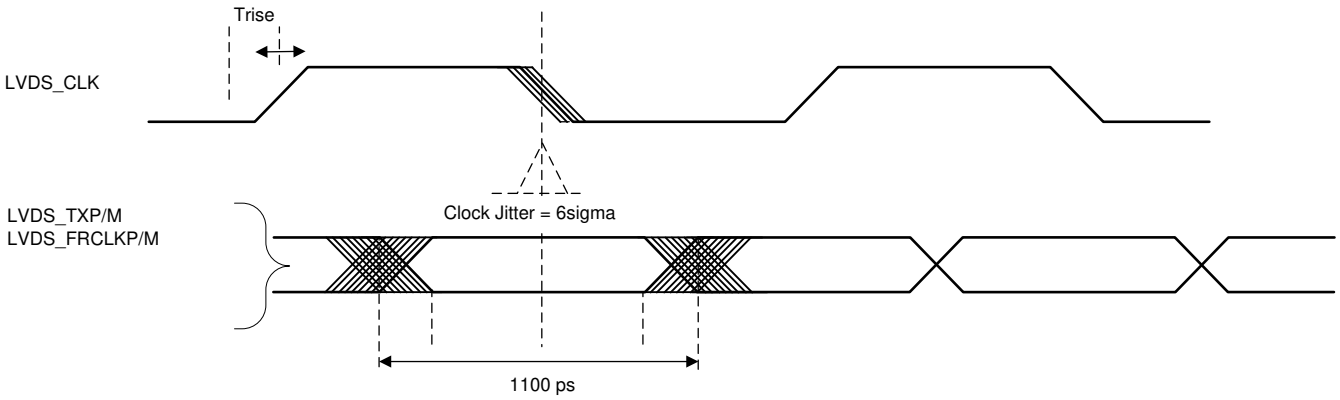


図 8-11. Timing Parameters

表 8-8. LVDS Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty Cycle Requirements	max 1 pF lumped capacitive load on LVDS lanes	48%		52%	
Output Differential Voltage	peak-to-peak single-ended with 100 Ω resistive load between differential pairs	250		450	mV
Output Offset Voltage		1125		1275	mV
Trise and Tfall	20%-80%, 900 Mbps		330		ps
Jitter (pk-pk)	900 Mbps		80		ps

8.9.8 General-Purpose Input/Output

セクション 8.9.8.1 lists the switching characteristics of output timing relative to load capacitance.

8.9.8.1 Switching Characteristics for Output Timing versus Load Capacitance (C_L)

PARAMETER(1)		TEST CONDITIONS	VIOIN = 1.8V	VIOIN = 3.3V	UNIT
t_r	Max rise time	C_L = 20 pF	2.8	3.0	ns
		C_L = 50 pF	6.4	6.9	
		C_L = 75 pF	9.4	10.2	
t_f	Max fall time	C_L = 20 pF	2.8	2.8	ns
		C_L = 50 pF	6.4	6.6	
		C_L = 75 pF	9.4	9.8	

(1) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

8.9.9 Camera Serial Interface (CSI)

The CSI is a MIPI D-PHY compliant interface for connecting this device to a camera receiver module. This interface is made of four differential lanes; each lane is configurable for carrying data or clock. The polarity of each wire of a lane is also configurable. セクション 8.9.9.1, 図 8-12, 図 8-13, and 図 8-14 describe the clock and data timing of the CSI.The clock is always ON once the CSI IP is enabled. Hence it remains in HS mode.

8.9.9.1 CSI Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
HPTX						
$HSTX_{DBR}$	Data bit rate	(1/2/4 data lane PHY)	150		600	Mbps
f_{CLK}	DDR clock frequency	(1/2/4 data lane PHY)	75		300	MHz
$\Delta_{VCMTX(LF)}$	Common-level variation		–50		50	mV
t_R and t_F	20% to 80% rise time and fall time				0.3	UI
LPTX DRIVER						
t_{EOT}	Time from start of THS-TRAIL period to start of LP-11 state				105 + 12*UI	ns
DATA-CLOCK Timing Specification						
UINOM	Nominal Unit Interval		1.67		13.33	ns
UIINST,MIN	Minimum instantaneous Unit Interval		1.131			ns
TSKEW[TX]	Data to clock skew measured at transmitter		–0.15		0.15	UIINST, MIN
CSI2 TIMING SPECIFICATION						
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter before any associated data lane beginning the transition from LP to HS mode.		8			ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the clock lane LP-00 line state immediately before the HS-0 line state starting the HS transmission.		38		95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state before starting the clock.		300			ns
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLKTRAIL}$, to the start of the LP-11 state following a HS burst.				105 ns + 12*UI	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the data lane LP-00 line state immediately before the HS-0 line state starting the HS transmission		40 + 4*UI		85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.		145 ns + 10*UI			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.		100			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst		max(8*UI, 60 ns + 4*UI)			ns
T_{LPX}	TXXXransmitted length of any low-power state period		50			ns

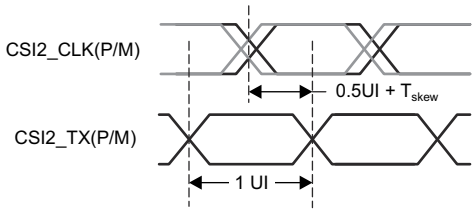


図 8-12. Clock and Data Timing in HS Transmission

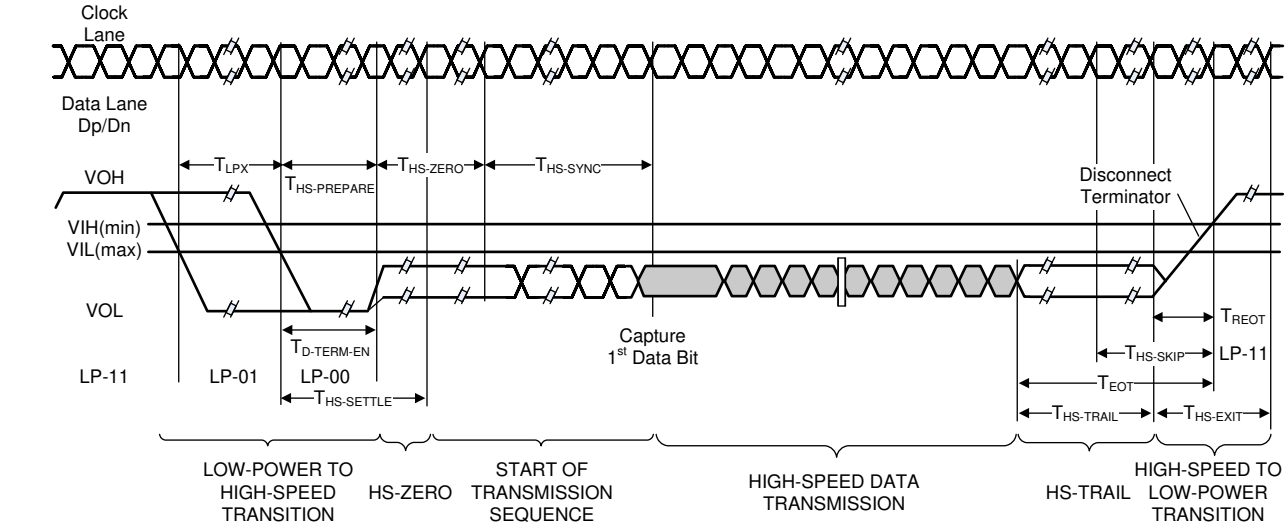
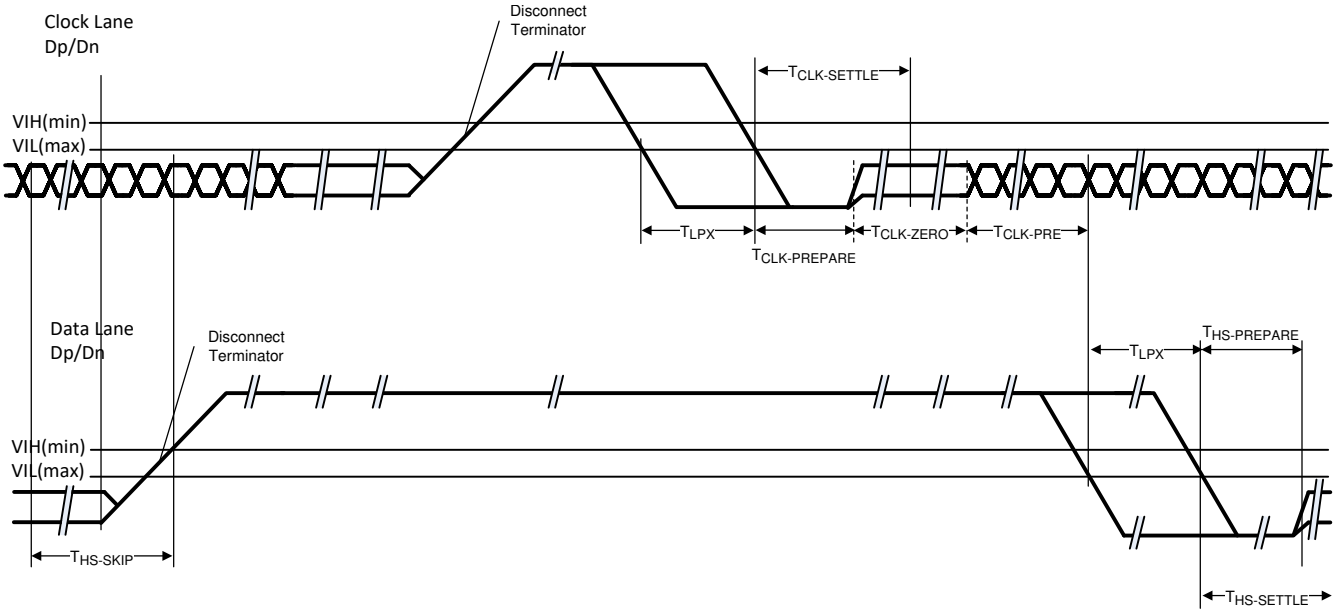


図 8-13. High-Speed Data Transmission Burst



A. The HS to LP transition of the CLK does not actually take place since the CLK is always ON in HS mode.

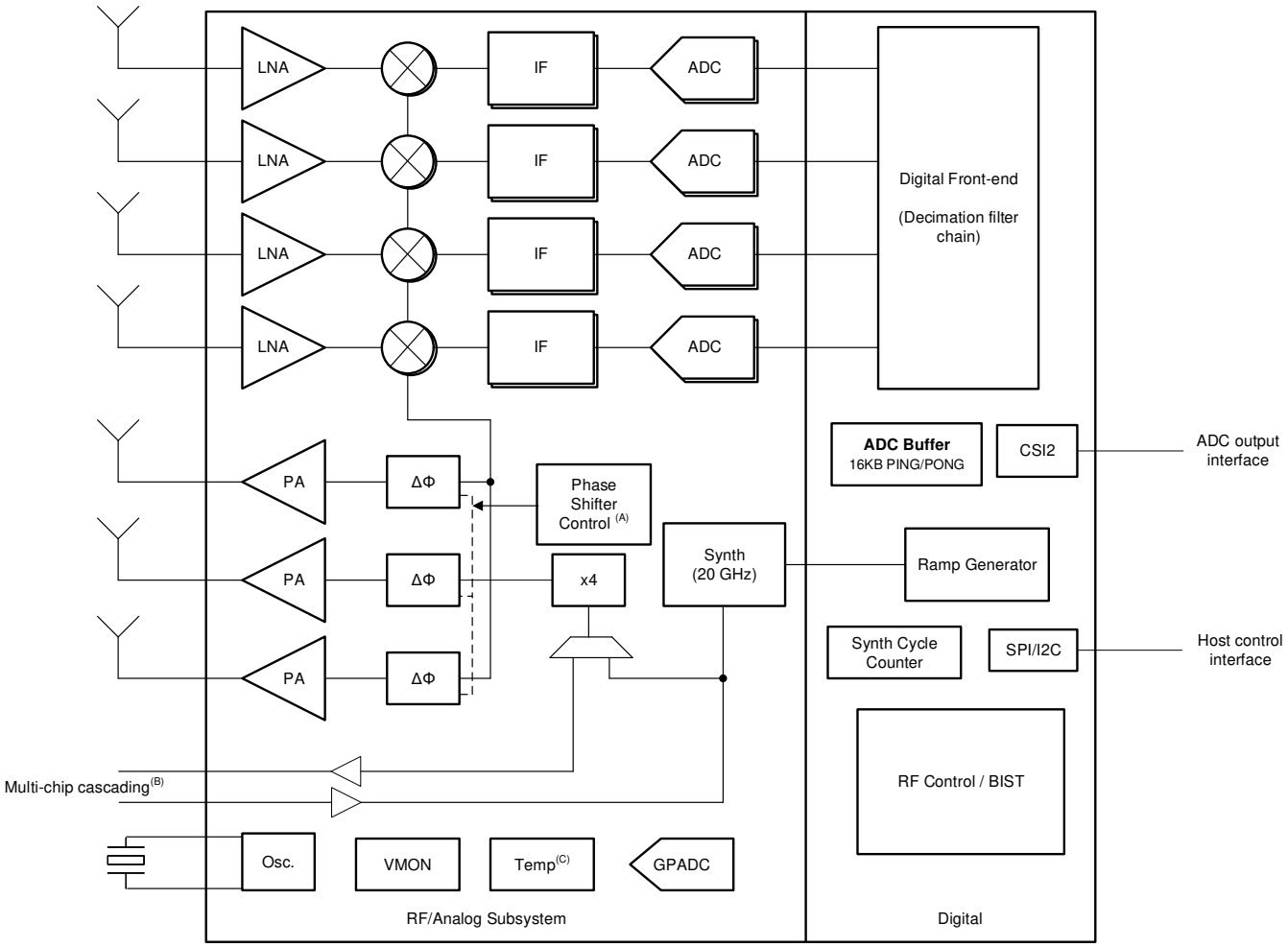
図 8-14. Switching the Clock Lane Between Clock Transmission and Low-Power Mode

9 Detailed Description

9.1 Overview

The IWR2243 device is a single-chip highly integrated 77-GHz transceiver and front end that includes three transmit and four receive chains. It is an ideal solution for low power, self-monitored, ultra-accurate radar systems in the industrial space. The IWR2243 device has an extremely small form factor and provides ultra-high resolution with very low power consumption. This device, when used with the TDA3X or TDA2X, offers higher levels of performance and flexibility through a programmable digital signal processor (DSP).

9.2 Functional Block Diagram



A. Phase Shift Control
- 0° / 180° BPM
- 0° / 180° BPM and 5.625° resolution control option for IWR2243, and IWR1843

B. Internal temperature sensor accuracy is ± 7 °C.

9.3 Subsystems

9.3.1 RF and Analog Subsystem

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The three transmit channels can be operated simultaneously for transmit beamforming purpose as required; whereas the four receive channels can all be operated simultaneously.

The IWR2243 device supports simultaneous operation of 3 transmitters.

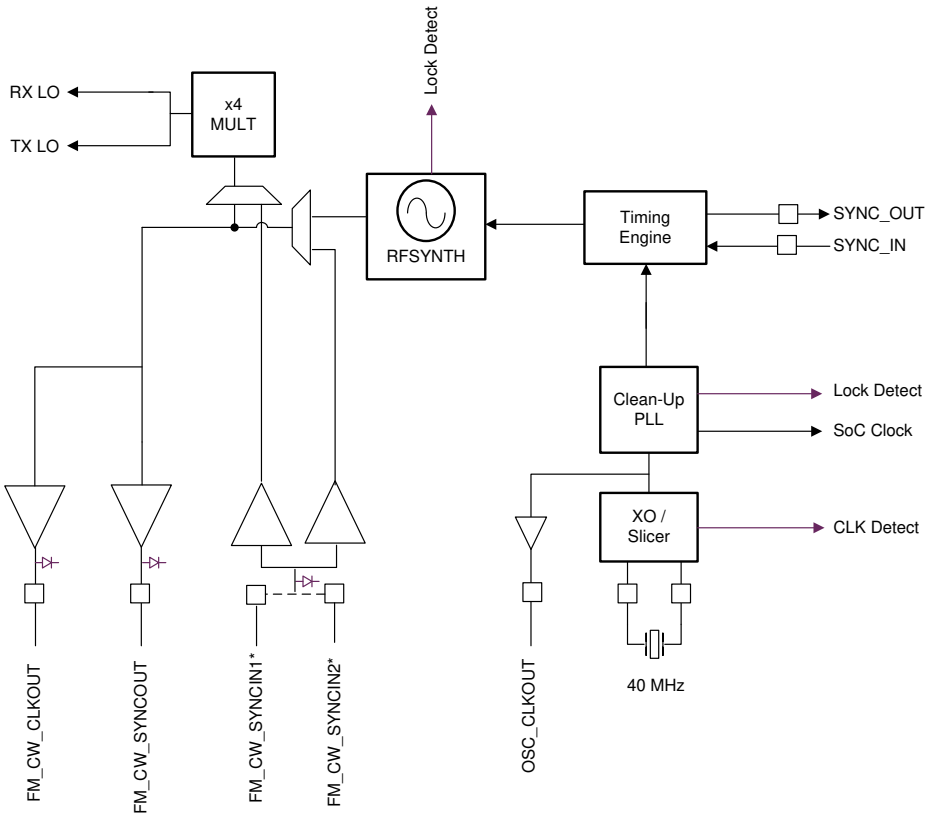
9.3.1.1 Clock Subsystem

The IWR2243 clock subsystem generates 76 to 81 GHz from an input reference of 40-MHz crystal. It has a built-in oscillator circuit followed by a clean-up PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X4 multiplier to create the required frequency in the 76 to 81 GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation.

The output of the RF synthesizer is available at the device pin boundary for multichip cascaded configuration. The clean-up PLL also provides a reference clock for the host processor after system wakeup.

The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

図 9-1 describes the clock subsystem.



* These pins are 20GHz LO input pins. Connect LO to one pin while grounding the other pin.

図 9-1. Clock Subsystem

9.3.1.2 Transmit Subsystem

The IWR2243 transmit subsystem consists of three parallel transmit chains, each with independent phase and amplitude control. All three transmitters can be used simultaneously or in time-multiplexed fashion. The device supports binary phase modulation for MIMO radar and interference mitigation. For IWR2243, additional phase shifters are associated with Tx channels, and these can programmed on a per chirp basis.

Each transmit chain can deliver a maximum of 13 dBm at the antenna port on the PCB. The transmit chains also support programmable backoff for system optimization.

図 9-2 describes the transmit subsystem.

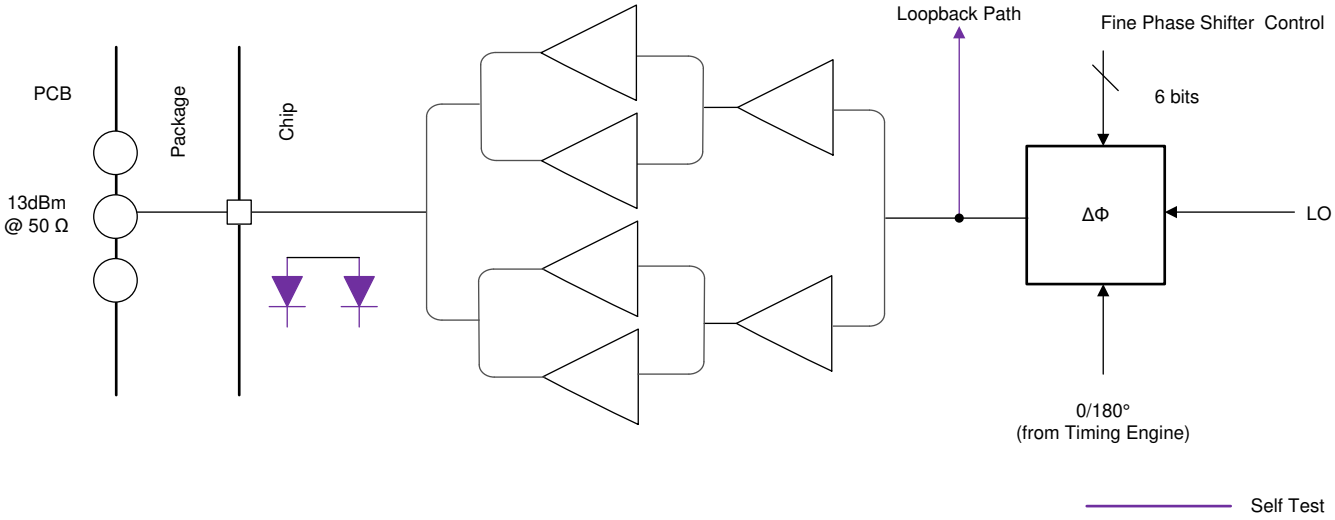


図 9-2. Transmit Subsystem (Per Channel)

9.3.1.3 Receive Subsystem

The IWR2243 receive subsystem consists of four parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, ADC conversion, and decimation. All four receive channels can be operational at the same time an individual power-down option is also available for system optimization.

Unlike conventional real-only receivers, the IWR2243 device supports a complex baseband architecture, which uses quadrature mixer and dual IF and ADC chains to provide complex I and Q outputs for each receiver channel. The IWR2243 is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies above 175 kHz and can support bandwidths up to 20 MHz.

図 9-3 describes the receive subsystem.

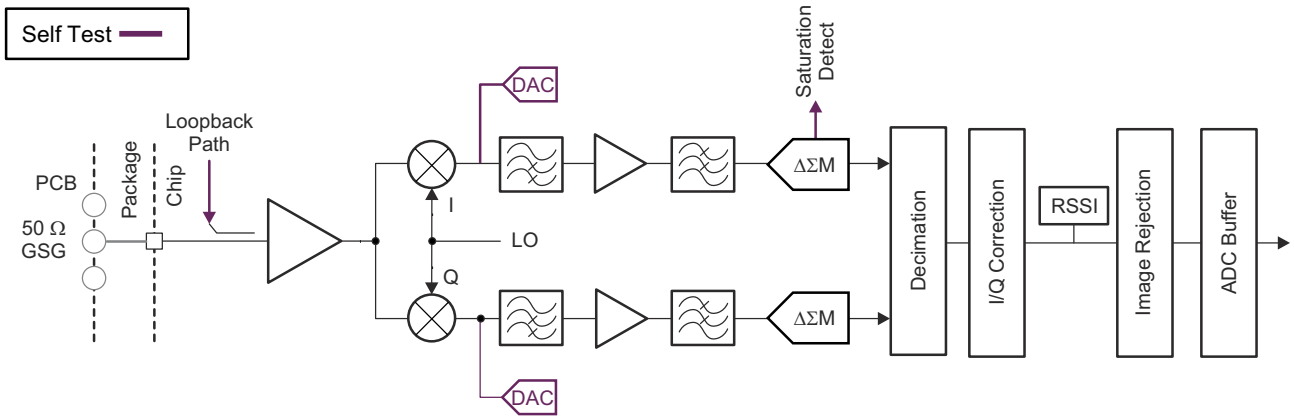


図 9-3. Receive Subsystem (Per Channel)

9.3.2 Host Interface

The IWR2243 device communicates with the host radar processor over the following main interfaces:

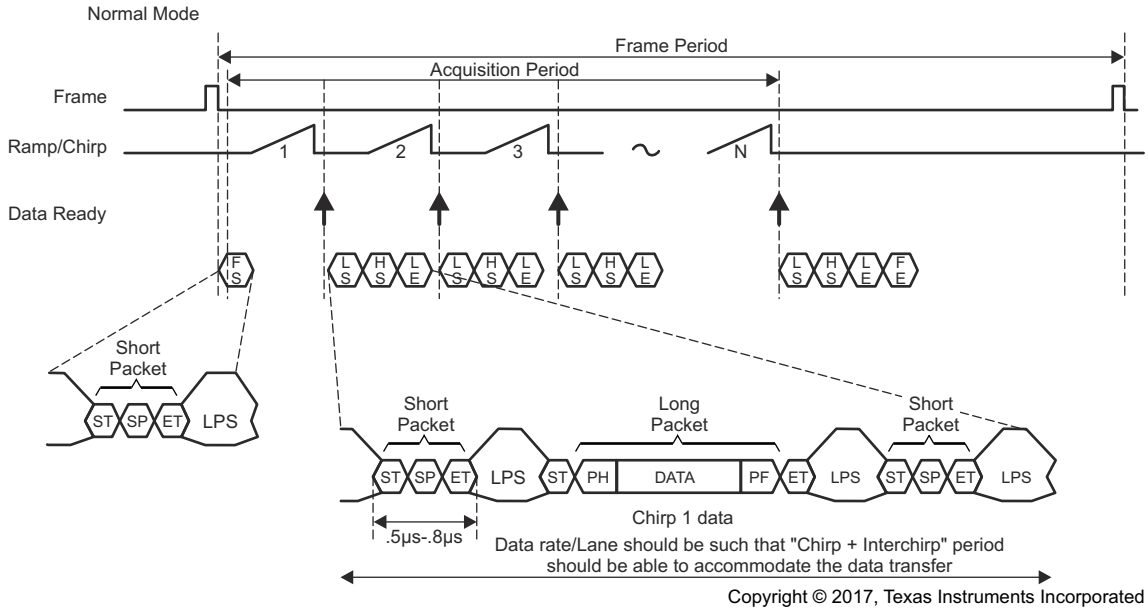
- Reference Clock – Reference clock available for host processor after device wakeup
- Control – 4-port standard SPI (peripheral or I2C) for host control along with HOST INTR pin for async events.. All radio control commands (and response) flow through this interface.
- Data – High-speed serial port following the MIPI CSI2 format. Four data and one clock lane (all differential). Data from different receive channels can be multiplexed on a single data lane to optimize board routing. This is a unidirectional interface used for data transfer only.
- Reset – Active-low reset for device wakeup from host
- Out-of-band interrupt
- Error – Used for notifying the host in case the radio controller detects a fault

9.4 Other Subsystems

9.4.1 ADC Data Format Over CSI2 Interface

The IWR2243 device uses MIPI D-PHY / CSI2-based format to transfer the raw ADC samples to the external MCU. This is shown in 図 9-4.

- Supports four data lanes
- CSI-2 data rate scalable from 150 Mbps to 600 Mbps per lane
- Virtual channel based
- CRC generation



Frame **S**tart – CSi2 VSYNC Start Short Packet
Line **S**tart – CSI2 HSYNC Start Short Packet
Line **E**nd – CSI2 HSYNC End Short Packet
Frame **E**nd – CSi2 VSYNC End Short Packet

図 9-4. CSI-2 Transmission Format

The data payload is constructed with the following three types of information:

- Chirp profile information
- The actual chirp number
- ADC data corresponding to chirps of all four channels
  - Interleaved fashion
- Chirp quality data (configurable)

The payload is then split across the four physical data lanes and transmitted to the receiving D-PHY. The data packet packing format is shown in 図 9-5

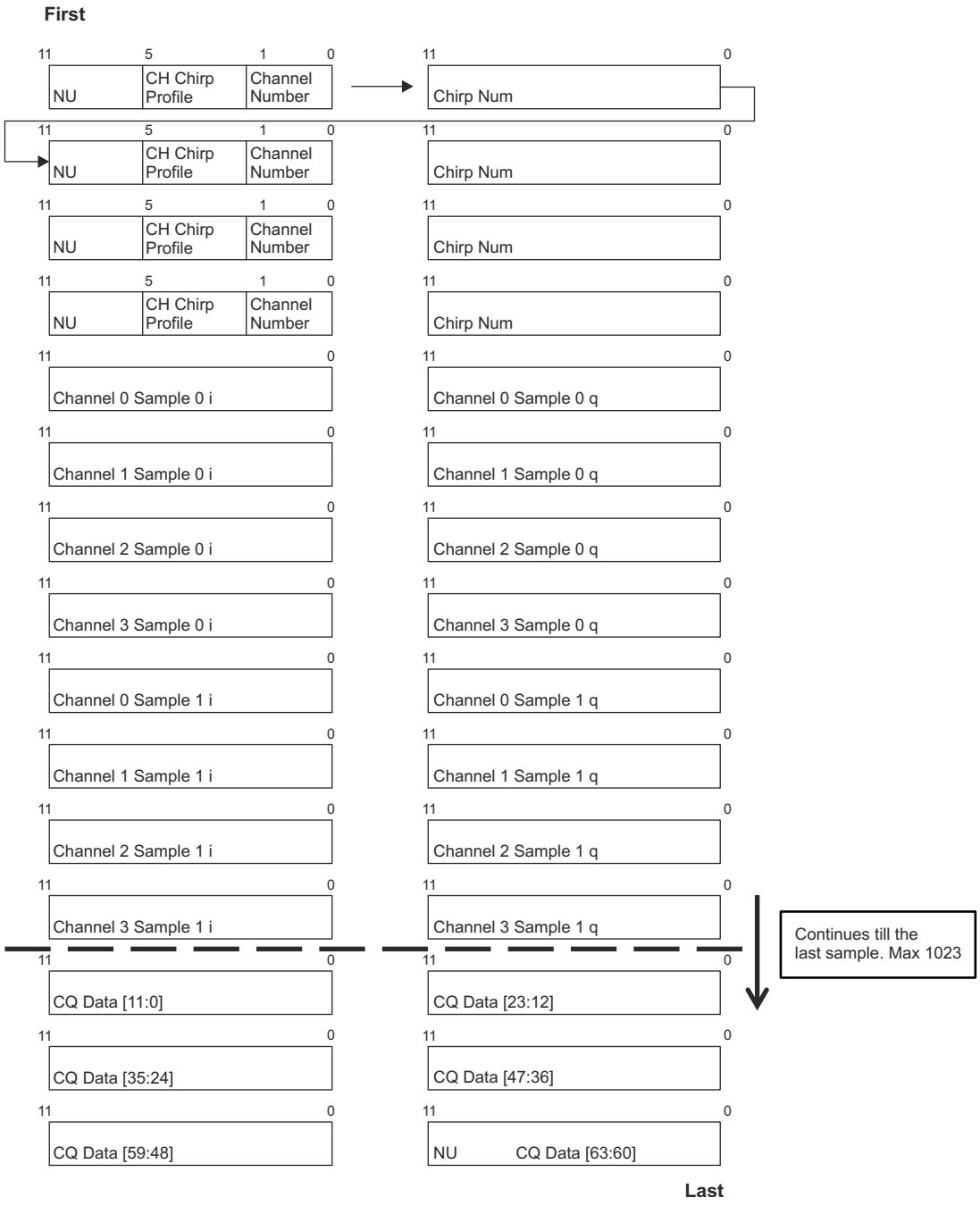


図 9-5. Data Packet Packing Format for 12-Bit Complex Configuration

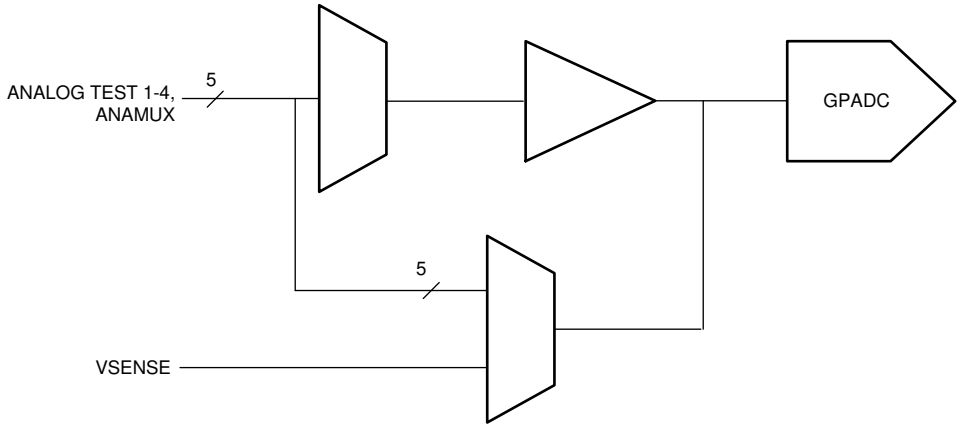
9.4.2 ADC Channels (Service) for User Application

The device includes provision for an ADC service for user application, where the GPADC engine present inside the device can be used to measure up to six external voltages. The ADC1, ADC2, ADC3, ADC4, ADC5, and ADC6 pins are used for this purpose.

- ADC itself is controlled by TI firmware running inside the BIST subsystem and access to it for customer's external voltage monitoring purpose is via 'monitoring API' calls routed to the BIST subsystem. This API could be linked with the user application running on the MSS R4F.
- BIST subsystem firmware will internally schedule these measurements along with other RF and Analog monitoring operations. The API allows configuring the settling time (number of ADC samples to skip) and number of consecutive samples to take. At the end of a frame, the minimum, maximum and average of the readings will be reported for each of the monitored voltages.

GPADC Specifications:

- 625 Ksps SAR ADC
- 0 to 1.8V input range
- 10-bit resolution
- For 5 out of the 6 inputs, an optional internal buffer is available. Without the buffer, the ADC has a switched capacitor input load modeled with 5pF of sampling capacitance and 12pF parasitic capacitance (GPADC channel 6, the internal buffer is not available).



A. GPADC structures are used for measuring the output of internal temperature sensors. The accuracy of these measurements is ±7°C.

図 9-6. ADC Path

9.4.2.1 GPADC Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TYP	UNIT
ADC supply	1.8	V
ADC unbuffered input voltage range	0 – 1.8	V
ADC buffered input voltage range(1)	0.4 – 1.3	V
ADC resolution	10	bits
ADC offset error	±5	LSB
ADC gain error	±5	LSB
ADC DNL	–1/+2.5	LSB
ADC INL	±2.5	LSB
ADC sample rate(2)	625	Ksps
ADC sampling time(2)	400	ns
ADC internal cap	10	pF
ADC buffer input capacitance	2	pF
ADC input leakage current	3	uA

(1) Outside of given range, the buffer output will become nonlinear.
(2) ADC itself is controlled by TI firmware running inside the BIST subsystem. For more details please refer to the API calls.

10 Monitoring and Diagnostic Mechanisms

Below is the list given for the main monitoring and diagnostic mechanisms available in the Functional Safety-Compliant IWR2243 device.

MSS R4F is the processor used for running TI's Functional Firmware stored in the ROM that helps in the execution of the API calls issued by the host processor. (It is not a customer programmable core)

表 10-1. Monitoring and Diagnostic Mechanisms for IWR2243

S No	Feature	Description
1	Boot time LBIST For MSS R4F Core and associated VIM	IWR2243 architecture supports hardware logic BIST (LBIST) engine self-test Controller (STC). This logic is used to provide a very high diagnostic coverage (>90%) on the MSS R4F CPU core and Vectored Interrupt Module (VIM) at a transistor level. LBIST for the CPU and VIM are triggered by the bootloader.
2	Boot time PBIST for MSS R4F TCM Memories	MSS R4F has three Tightly coupled Memories (TCM) memories TCMA, TCMB0 and TCMB1. IWR2243 architecture supports a hardware programmable memory BIST (PBIST) engine. This logic is used to provide a very high diagnostic coverage (March-13n) on the implemented MSS R4F TCMs at a transistor level. PBIST for TCM memories is triggered by Bootloader at the boot time . CPU stays there in while loop and does not proceed further if a fault is identified.
3	End to End ECC for MSS R4F TCM Memories	TCMs diagnostic is supported by Single error correction double error detection (SECDED) ECC diagnostic. An 8-bit code word is used to store the ECC data as calculated over the 64-bit data bus. ECC evaluation is done by the ECC control logic inside the CPU. This scheme provides end-to-end diagnostics on the transmissions between CPU and TCM. CPU is configured to have predetermined response (Ignore or Abort generation) to single and double bit error conditions.
4	MSS R4F TCM bit multiplexing	Logical TCM word and its associated ECC code is split and stored in two physical SRAM banks. This scheme provides an inherent diagnostic mechanism for address decode failures in the physical SRAM banks. Faults in the bank addressing are detected by the CPU as an ECC fault.Further, bit multiplexing scheme implemented such that the bits accessed to generate a logical (CPU) word are not physically adjacent. This scheme helps to reduce the probability of physical multi-bit faults resulting in logical multi-bit faults; rather they manifest as multiple single bit faults. As the SECDED TCM ECC can correct a single bit fault in a logical word, this scheme improves the usefulness of the TCM ECC diagnostic.
5	Clock Monitor	IWR2243 architecture supports Three Digital Clock Comparators (DCCs) and an internal RCOSC. Dual functionality is provided by these modules – Clock detection and Clock Monitoring. DCCint is used to check the availability/range of Reference clock at boot otherwise the device is moved into limp mode (Device still boots but on 10MHz RCOSC clock source. This provides debug capability). DCCint is only used by boot loader during boot time. It is disabled once the APLL is enabled and locked. DCC1 is dedicated for APLL lock detection monitoring, comparing the APLL output divided version with the Reference input clock of the device. Initially (before configuring APLL), DCC1 is used by bootloader to identify the precise frequency of reference input clock against the internal RCOSC clock source. Failure detection for DCC1 would cause the device to go into limp mode. Clock Compare module (CCC) module is used to compare the APLL divided down frequency with reference clock (XTAL). Failure detection is indicated by the nERROR OUT signal.
6	RTI/WD for MSS R4F	Internal watchdog is enabled by the bootloader in a windowed watchdog (DWWD) mode.. Watchdog expiry issues an internal warm reset and nERROR OUT signal to the host.
7	MPU for MSS R4F	Cortex-R4F CPU includes an MPU. The MPU logic can be used to provide spatial separation of software tasks in the device memory. Cortex-R4F MPU supports 12 regions. It is expected that the operating system controls the MPU and changes the MPU settings based on the needs of each task. A violation of a configured memory protection policy results in a CPU abort.
8	PBIST for Peripheral interface SRAMs - SPI, I2C	IWR2243 architecture supports a hardware programmable memory BIST (PBIST) engine for Peripheral SRAMs as well. PBIST for peripheral SRAM memories is triggered by the bootloader. The PBIST tests are destructive to memory contents, and as such are typically run only at boot time. . Any fault detected by the PBIST results in an error indicated in PBIST and boot status response message.

表 10-1. Monitoring and Diagnostic Mechanisms for IWR2243 (continued)

S No	Feature	Description
9	ECC for Peripheral interface SRAMs – SPI, I2C	Peripheral interface SRAMs diagnostic is supported by Single error correction double error detection (SECDED) ECC diagnostic. When a single or double bit error is detected the error is indicated by nERROR (double bit error) or via SPI message (single bit error).
10	Cyclic Redundancy Check – Main SS	Cyclic Redundancy Check (CRC) module is available for the Main SS. The firmware uses this feature for data transfer checks in mailbox and SPI communication.
11	MPU for DMAs	IWR2243 architecture supports MPUs on Main SS DMAs. The firmware uses this for stack protection.
12	Boot time LBIST For BIST R4F Core and associated VIM	IWR2243 architecture supports hardware logic BIST (LBIST) even for BIST R4F core and associated VIM module. This logic provides very high diagnostic coverage (>90%) on the BIST R4F CPU core and VIM. This is triggered by MSS R4F boot loader at boot time and it does not proceed further if the fault is detected.
13	Boot time PBIST for BIST R4F TCM Memories	IWR2243 architecture supports a hardware programmable memory BIST (PBIST) engine for BIST R4F TCMs which provide a very high diagnostic coverage (March-13n) on the BIST R4F TCMs. PBIST is triggered at the power up of the BIST R4F.
14	End to End ECC for BIST R4F TCM Memories	BIST R4F TCMs diagnostic is supported by Single error correction double error detection (SECDED) ECC diagnostic. Single bit error is communicated to the BIST R4FCPU while double bit error is communicated to MSS R4F as an interrupt which sends a async event to the host.
15	BIST R4F TCM bit multiplexing	Logical TCM word and its associated ECC code is split and stored in two physical SRAM banks. This scheme provides an inherent diagnostic mechanism for address decode failures in the physical SRAM banks and helps to reduce the probability of physical multi-bit faults resulting in logical multi-bit faults.
16	Temperature Sensors	IWR2243 architecture supports various temperature sensors all across the device (next to power hungry modules such as PAs, DSP etc) which is monitored during the inter-frame period.(1)
17	Tx Power Monitors	IWR2243 architecture supports power detectors at the Tx output.(2)
18	Error Signaling Error Output	When a diagnostic detects a fault, the error must be indicated. The IWR2243 architecture provides aggregation of fault indication from internal monitoring/diagnostic mechanisms using nERROR signaling or async event over SPI interface.
19	Synthesizer (Chirp) frequency monitor	Monitors Synthesizer's frequency ramp by counting (divided-down) clock cycles and comparing to ideal frequency ramp. Excess frequency errors above a certain threshold, if any, are detected and reported.
20	Ball break detection for TX ports (TX Ball break monitor)	IWR2243 architecture supports a ball break detection mechanism based on Impedance measurement at the TX output(s) to detect and report any large deviations that can indicate a ball break. Monitoring is done by TIs code running on BIST R4F and failure is reported to the host. It is completely up to customer SW to decide on the appropriate action based on the message from BIST R4F.
21	RX loopback test	Built-in TX to RX loopback to enable detection of failures in the RX path(s), including Gain, inter-RX balance, etc.
22	IF loopback test	Built-in IF (square wave) test tone input to monitor IF filter's frequency response and detect failure.
23	RX saturation detect	Provision to detect ADC saturation due to excessive incoming signal level and/or interference.

(1) Monitoring is done by the TI's code running on BIST R4F. There are two modes in which it could be configured to report the temperature sensed via API by customer application.
   a. Report the temperature sensed after every N frames
   b. Report the condition once the temperature crosses programmed threshold.

   It is completely up to customer SW to decide on the appropriate action based on the message from BIST R4Fvia Mailbox.

(2) Monitoring is done by the TI's code running on BIST R4F.
   There are two modes in which it could be configured to report the detected output power via API by customer application.
   a. Report the power detected after every N frames
   b. Report the condition once the output power degrades by more than configured threshold from the configured.

It is completely up to customer SW to decide on the appropriate action based on the message from BIST R4F.

11 Applications, Implementation, and Layout

注

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

Application information can be found on IWR Application web page.

11.2 Imaging Radar using Cascade Configuration

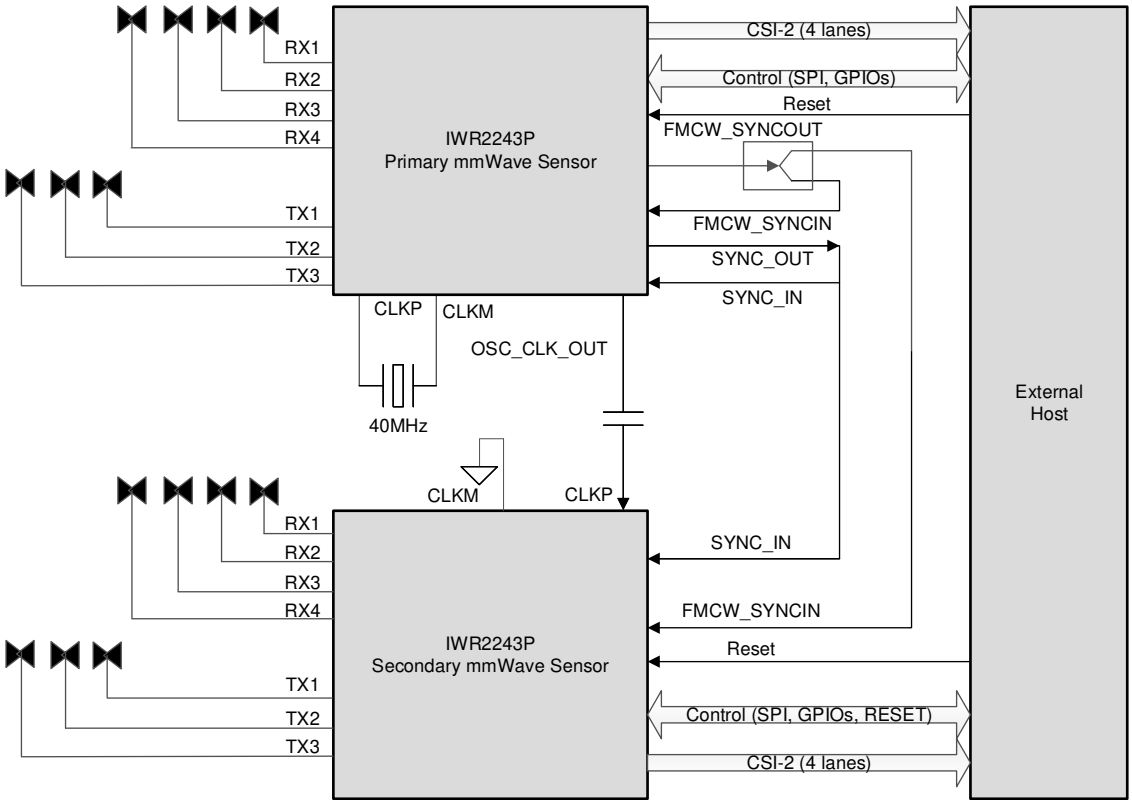


図 11-1. Imaging Radar using Cascade Configuration

11.3 Reference Schematic

図 11-2 shows the reference schematic for the IWR2243 device.

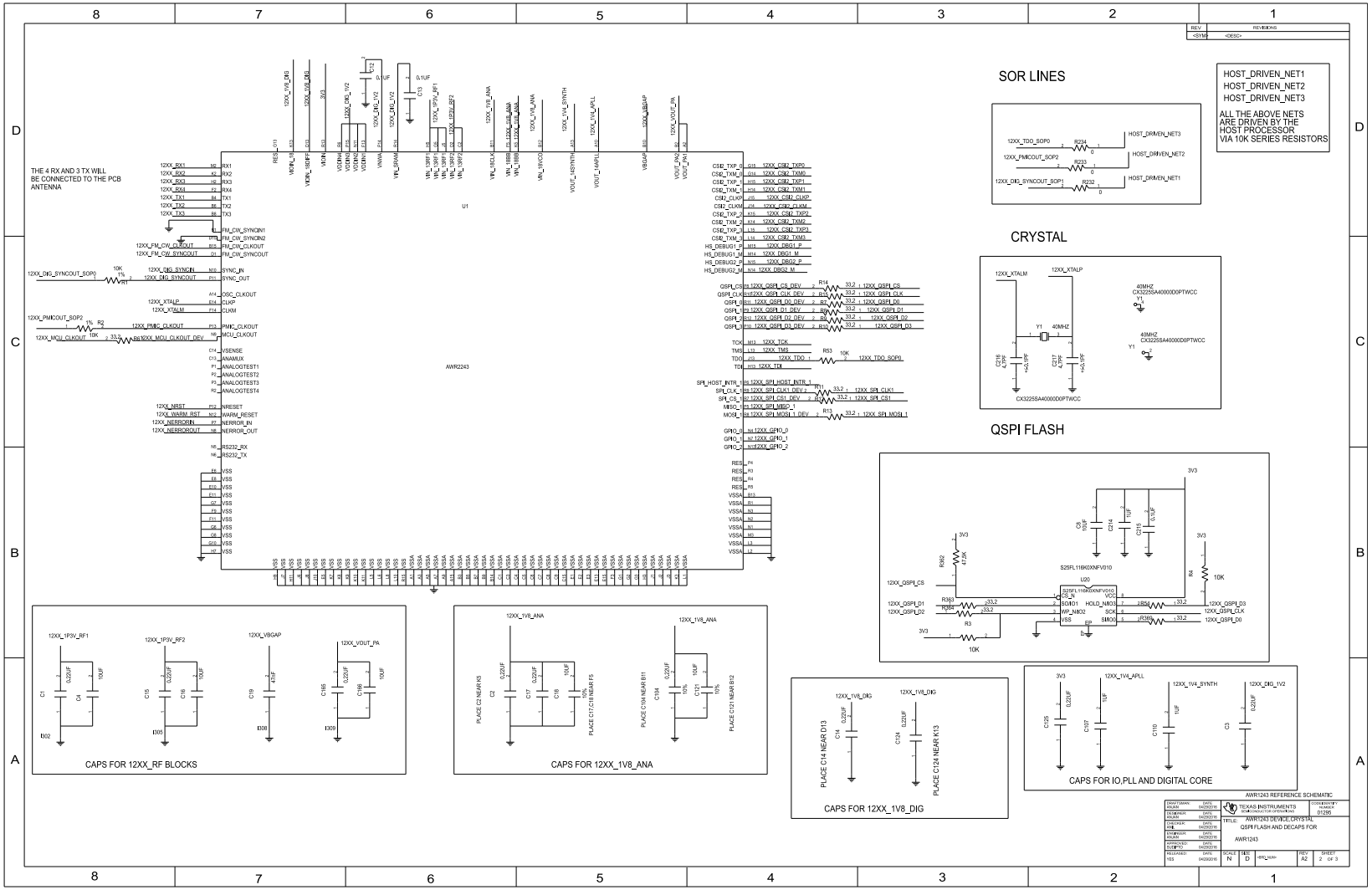


図 11-2. IWR2243 Reference Schematic

11.4 Layout

The top layer routing, top layer closeup, and bottom layer routing are shown in 図 11-3, 図 11-4, and 図 11-5, respectively.

11.4.1 Layout Guidelines

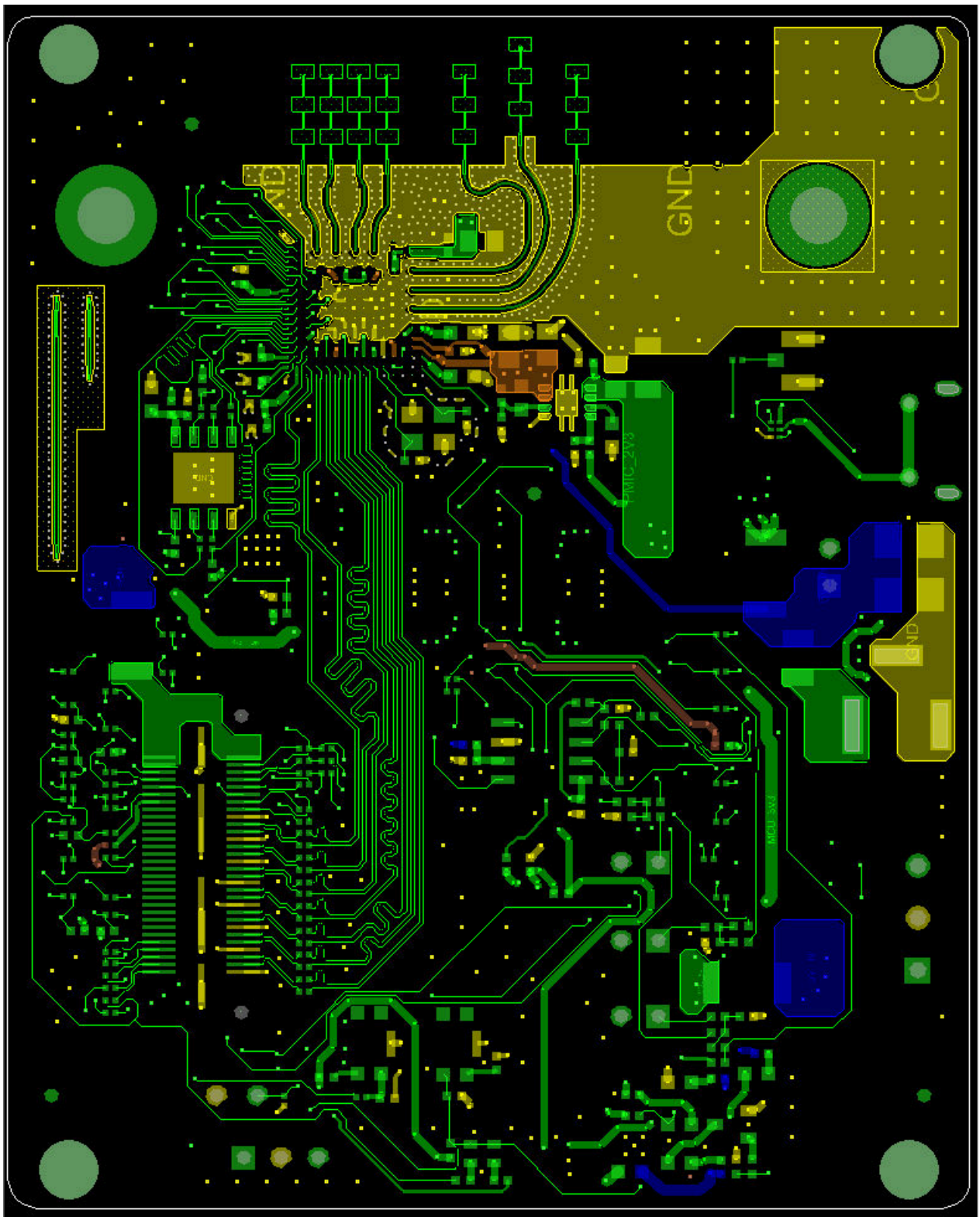


図 11-3. Top Layer Routing

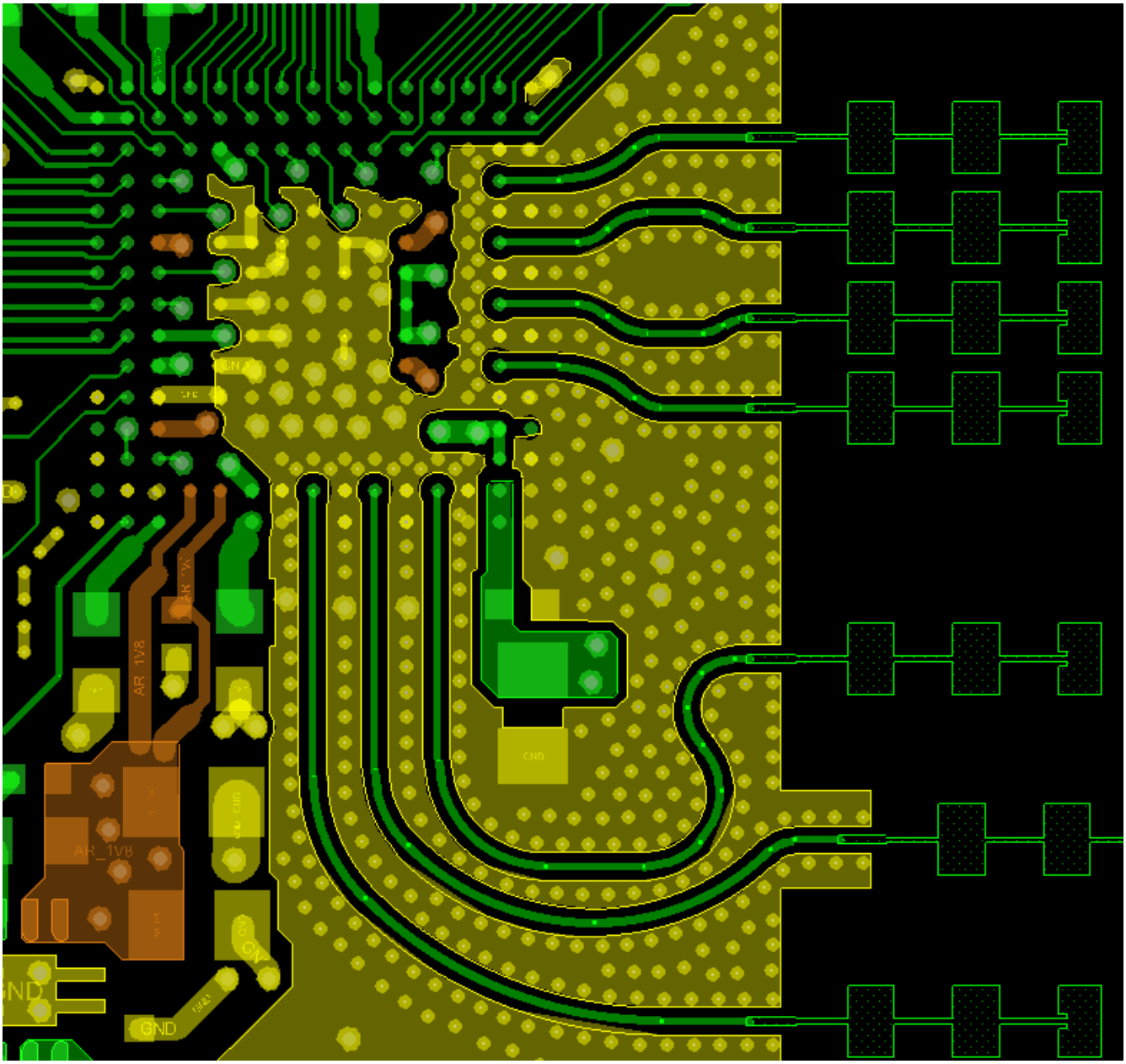


図 11-4. Top Layer Routing Closeup

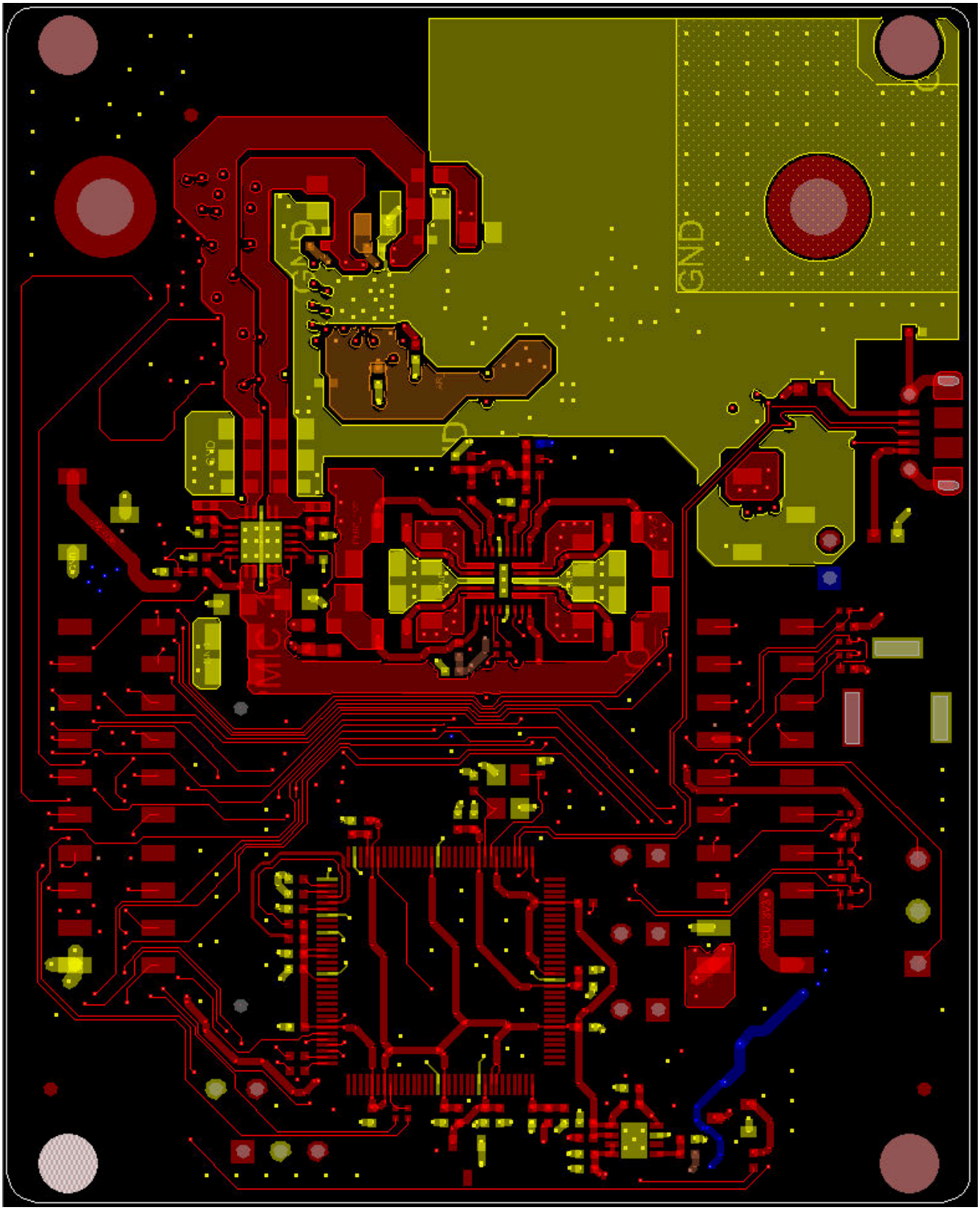
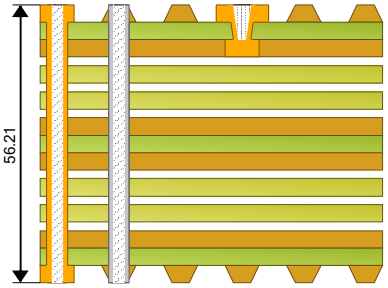


図 11-5. Bottom Layer Routing

11.4.2 Stackup Details



Layer	Stack up	Description	Type	Base Thickness	Processed Thickness	εr	Copper Coverage
1				0.689	2.067		100.000
		Rogers 4835 4mil coreH/1 Low Pro	Rogers 4835	4.000	4.000	3.480	
2				1.260	1.260		73.000
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.830	3.700	
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.830	3.700	
3				1.260	1.260		69.000
		Iteq IT180A 28 mil core 1/1	FR4	28.000	28.000	4.280	
4				1.260	1.260		48.000
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.691	3.700	
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.691	3.700	
5				1.260	1.260		72.000
		Iteq IT180A 4 mil core 1/H	FR4	4.000	4.000	3.790	
6				0.689	2.067		100.000

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions follow.

12.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *IWR2243*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ABL0161), the temperature range (for example, blank is the default commercial temperature range). 図 12-1 provides a legend for reading the complete device name for any *IWR2243* device.

For orderable part numbers of *IWR2243* devices in the ABL0161 package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the XWR2243 Device Errata.

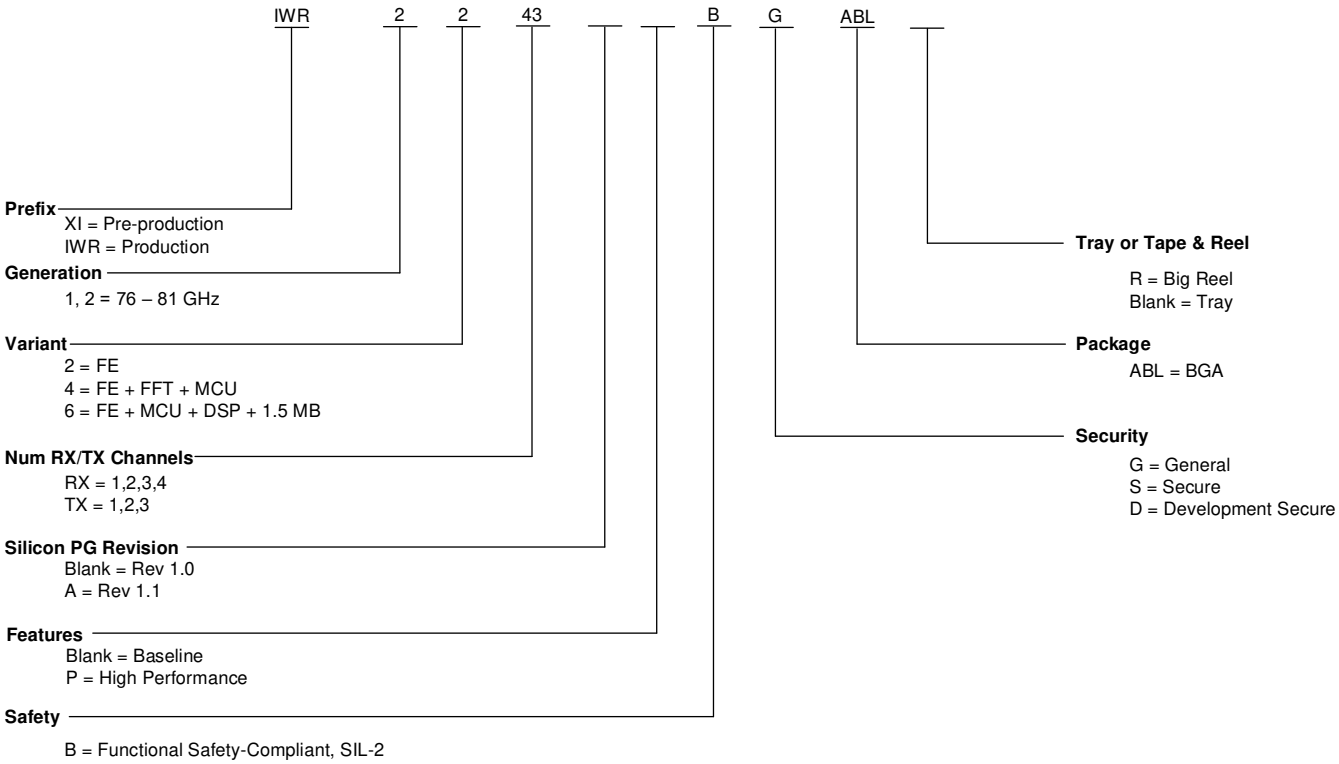


図 12-1. Device Nomenclature

12.2 Tools and Software

Development Tools

XWR2243 Cascade Application Note Describes TI's cascaded mmWave radar system.

Models

XWR2243 BSDL Model Boundary scan database of testable input and output pins for IEEE 1149.1 of the specific device.

12.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the DSP, related peripherals, and other technical collateral follows.

Errata

XWR2243 Device Errata Silicon Revisions 1.0 and 1.1

Describes known advisories, limitations, and cautions on silicon and provides workarounds.

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12.8 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

13.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

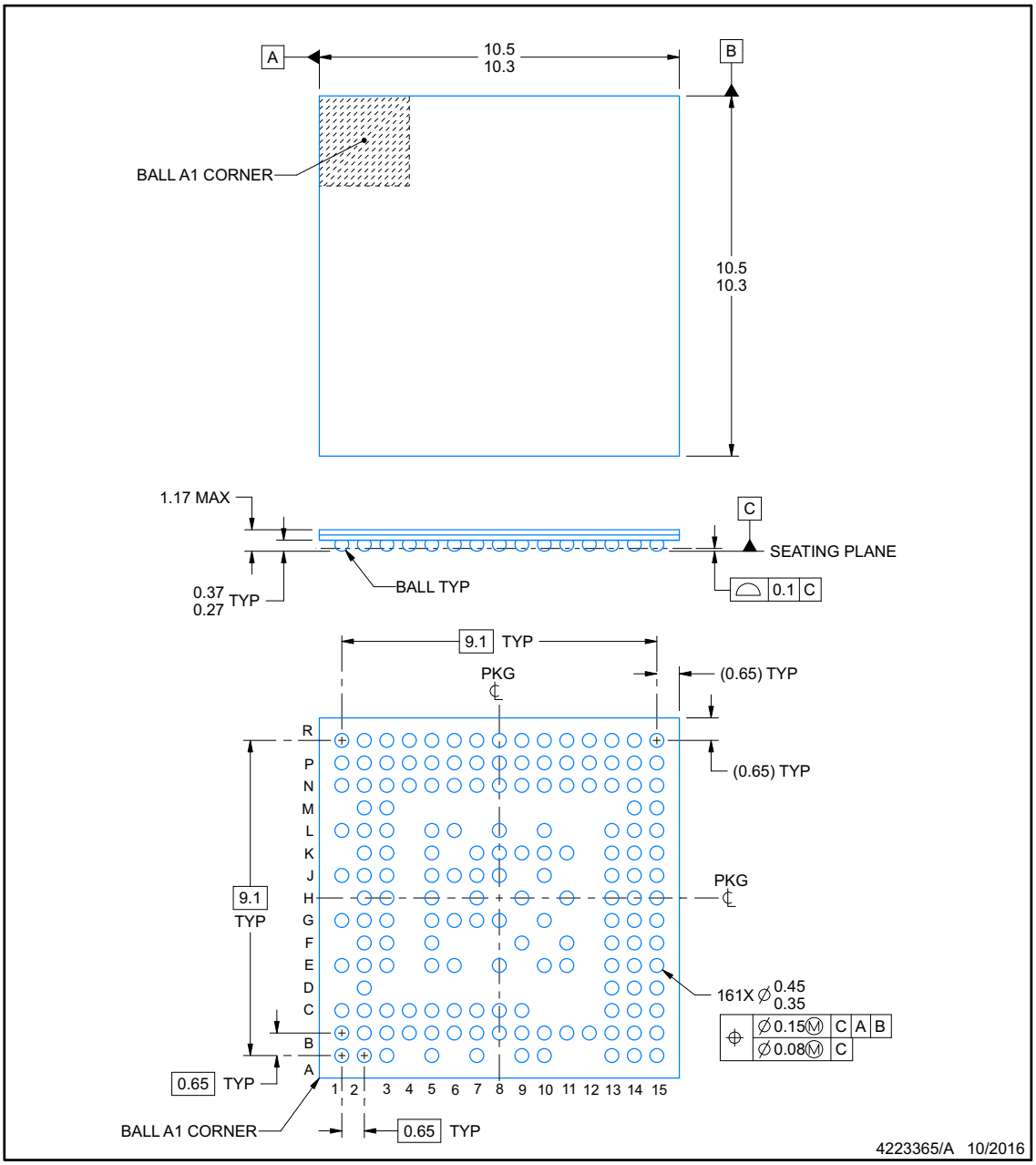
注意
The following package information is subject to change without notice.

PACKAGE OUTLINE

ABL0161B

FCBGA - 1.17 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

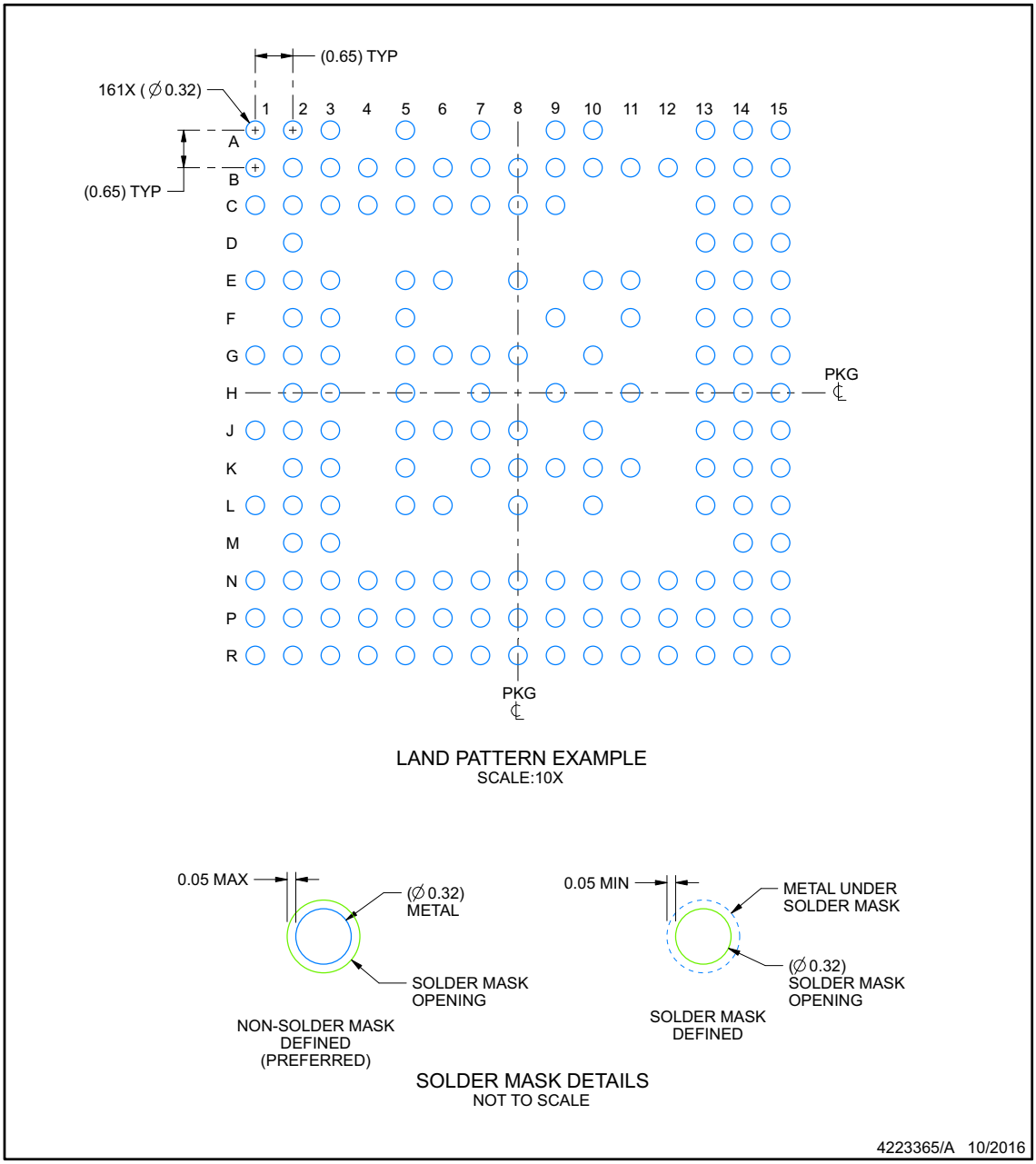
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

ABL0161B

FCBGA - 1.17 mm max height

PLASTIC BALL GRID ARRAY



NOTES: (continued)

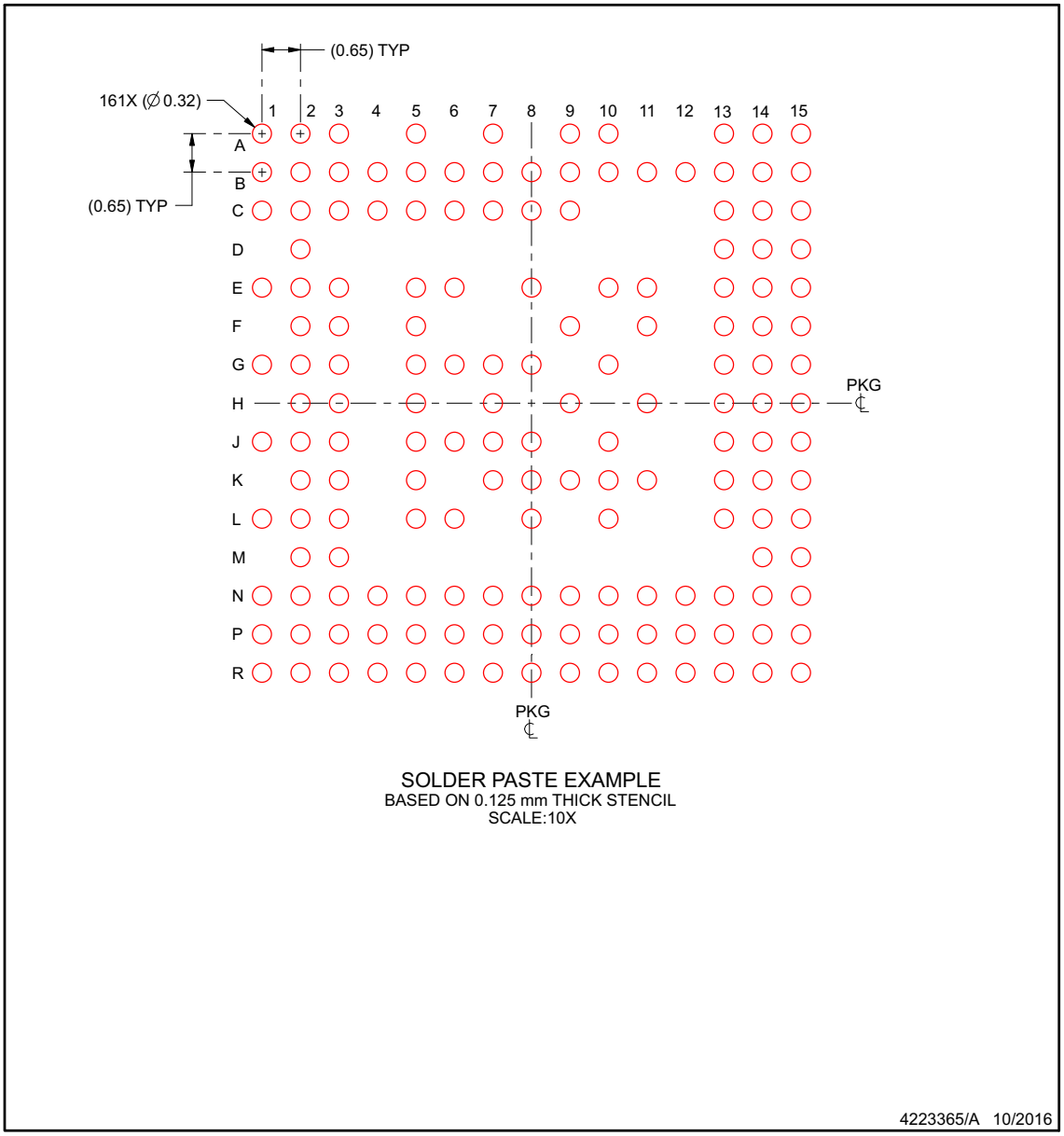
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ABL0161B

FCBGA - 1.17 mm max height

PLASTIC BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
IWR2243APBGABL	Active	Production	FCCSP (ABL) | 161	176 | JEDEC TRAY (5+1)	-	Call TI	Level-3-260C-168 HR	-40 to 105	IWR2243P BG 583A
IWR2243APBGABL.B	Active	Production	FCCSP (ABL) | 161	176 | JEDEC TRAY (5+1)	-	Call TI	Level-3-260C-168 HR	-40 to 105	IWR2243P BG 583A
IWR2243APBGABLR	Active	Production	FCCSP (ABL) | 161	1000 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 105	IWR2243P BG 583A
IWR2243APBGABLR.B	Active	Production	FCCSP (ABL) | 161	1000 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 105	IWR2243P BG 583A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

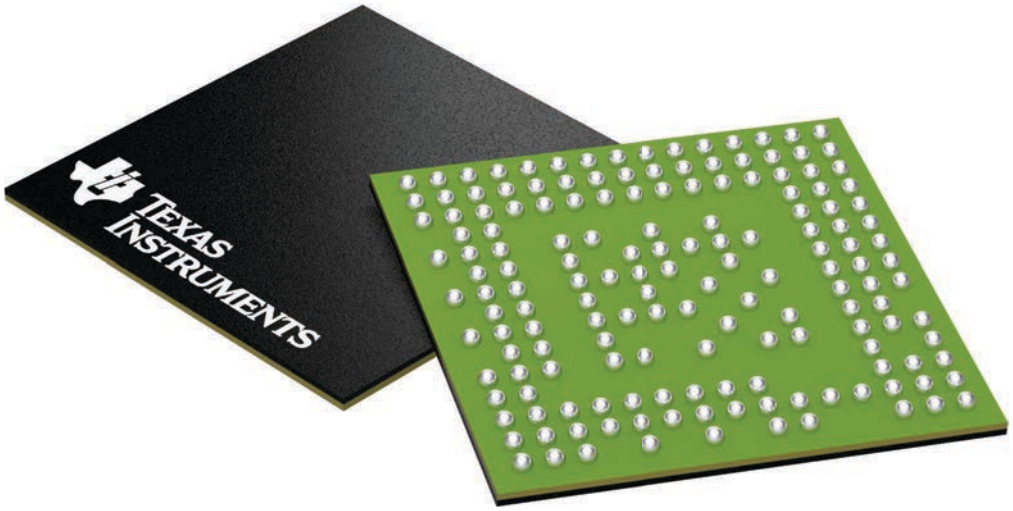
ABL 161

FCBGA - 1.17 mm max height

10.4 x 10.4, 0.65 mm pitch

PLASTIC BALL GRID ARRAY

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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