ISOS141-SEP 放射線耐性、高速 4 チャネル・デジタル・アイソレータ

1 特長

- 放射線耐性
  - 総照射線量 (TID) 耐性 (ELDRS フリー) = 30krad (Si)
  - TID RLAT/RHA = 30krad(Si)
  - シングル・イベント・ラッチアップ (SEL) 耐性:LET = 43MeV·cm^2/mg (125℃)
  - シングル・イベント誘電体破壊 (SEDR) 耐性: 43MeV·cm^2/mg (V_{DC} = 500V)
- 宇宙用強化プラスチック (宇宙用 EP)
  - NASA ASTM E595 アウトガス仕様に適合
  - VID (Vendor Item Drawing) V62/21610
  - ミリタリー温度範囲 (-55℃～125℃)
  - 単一のウェハー製造施設
  - 単一のアセンブリ / テスト施設
  - 金ボンド・ワイヤ、NiPdAu リード仕上げ
  - ウェハー・ロットをトレース可能
  - 長期にわたる製品ライフ・サイクル
  - 長期にわたる製品変更通知
- 600V_{RMS} の連続動作電圧
- セクション 6.7:
  - DIN VDE V 0884-11:2017-01
  - UL 1577 部品認定プログラム
- 100Mbps のデータ・レート
- 広い電源電圧範囲:2.25V～5.5V
- 2.25V/5.5V レベル変換
- デフォルト出力は *Low*
- 低消費電力:1.5mA/チャネル (標準値、1Mbps 時)
- 小さい伝搬遅延時間:10.7ns (標準値、電源電圧 5V 時)
- 小さいチャネル間スキュー 4ns 以下 (電源電圧 5V 時)
- CMTI:±100kV/µs (標準値)
- システム・レベルの ESD、EFT、サージ、磁気耐性
- 小型 QSOP (DBQ-16) パッケージ

2 アプリケーション

- 低軌道 (LEO) 衛星用途
- 信号の絶縁 (RS-422、RS-485、CAN、SPI)
- ゲート・ドライバの絶縁または GaN DC/DC コンバータの帰還の絶縁
- 宇宙グレード絶縁型 DC/DC モジュール
- 宇宙船向けバッテリ管理システム (BMS)
- 衛星推進向け電源ユニット (PPU)
- 発射装置と着陸装置の各種システム
- 通信ペイロード
- レーダー画像処理ペイロード

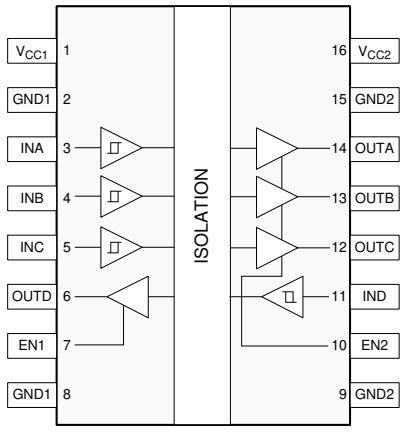
3 概要

ISOS141-SEP 放射線耐性デバイスは、小型の 16 ピン QSOP パッケージに封止された高性能 4 チャネル・デジタル・アイソレータです。それぞれの絶縁チャネルにはロジック入力および出力バッファがあり、二重の容量性二酸化ケイ素 (SiO_2) 絶縁バリアによって分離されています。このデバイスは、100Mbps の高いデータ・レート、10.7ns の小さい伝搬遅延、4ns の小さいチャネル間スキューという特長によって低軌道 (LEO) 衛星用途に対応します。ISOS141-SEP デバイスは 3 つの順方向チャネルと 1 つの逆方向チャネルを備えており、入力電力または信号が失われた場合のデフォルト出力は Low です。マルチマスタ駆動アプリケーションのために、または消費電力を低減するために、イネーブル・ピンを使って各出力を高インピーダンスにすることができます。

ISOS141-SEP は、CMOS または LVCMOS デジタル I/O を絶縁すると同時に、高い電磁気耐性と低い放射を低消費電力で実現します。本デバイスは、革新的なチップ設計により、100kV/µs という優れた同相過渡耐性を備えているため、システム・レベルの ESD、EFT、サージを軽減できます。また、放射のコンプライアンスに簡単に対応できます。

製品情報

部品番号	パッケージ	本体サイズ (公称)
ISOS141FDBQSEP 30krad(Si) RLAT/RHA	16 ピン QSOP (DBQ)	4.90mm × 3.90mm
ISOS141FDBQTSEP 30krad(Si) RLAT/RHA		



V_{CCI} = 入力電源、V_{CC2} = 出力電源
GND1 = 入力グランド、GND2 = 出力グランド

概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
May 2021	*	Initial release.

5 Pin Configuration and Functions

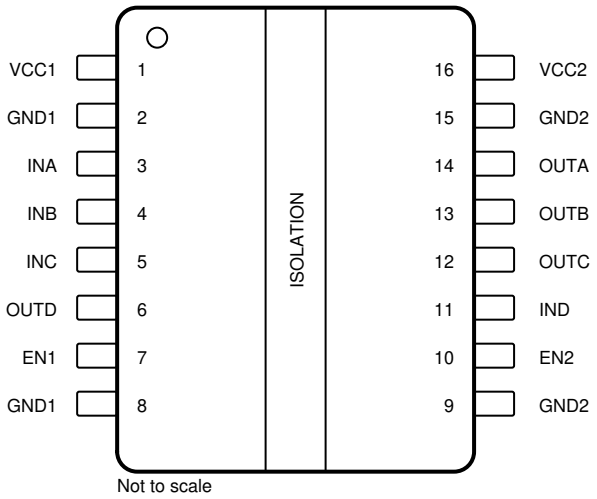


図 5-1. ISOS141-SEP DBQ Package 16-pin QSOP Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	Number		
EN1	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2	—	Ground connection for V_{CC1}
	8		
GND2	9	—	Ground connection for V_{CC2}
	15		
INA	3	I	Input, channel A
INB	4	I	Input, channel B
INC	5	I	Input, channel C
IND	11	I	Input, channel D
OUTA	14	O	Output, channel A
OUTB	13	O	Output, channel B
OUTC	12	O	Output, channel C
OUTD	6	O	Output, channel D
V_{CC1}	1	—	Power supply, side 1
V_{CC2}	16	—	Power supply, side 2

6 Specifications

6.1 Absolute Maximum Ratings

See(1)

		MIN	MAX	UNIT
Supply voltage ((2))	V_{CC1}, V_{CC2}	-0.5	6	V
Voltage at INx, OUTx, ENx	V	-0.5	V_{CCX} + 0.5 ((3))	V
Output current	Io	-15	15	mA
Temperature	Operating junction temperature, T_J		150	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test(3) (4)	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC1} , V_{CC2} (1)	Supply Voltage		2.25		5.5	V
Vcc (UVLO+)	UVLO threshold when supply voltage is rising			2	2.25	V
Vcc (UVLO-)	UVLO threshold when supply voltage is falling		1.7	1.8		V
Vhys (UVLO)	Supply voltage UVLO hysteresis		100	200		mV
V_{IH}	High level Input voltage		0.7 x V_{CCI} ((2))		V_{CCI}	V
V_{IL}	Low level Input voltage		0		0.3 x V_{CCI}	V
I_{OH}	High level output current	V_{CCO} = 5 V ((2))	-4			mA
		V_{CCO} = 3.3 V	-2			mA
		V_{CCO} = 2.5 V	-1			mA
I_{OL}	Low level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	mA
		V_{CCO} = 2.5 V			1	mA
DR	Data Rate		0		100	Mbps
T_A	Ambient temperature		-55	25	125	°C

(1) V_{CC1} and V_{CC2} can be set independent of one another
(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

6.4 Thermal Information

THERMAL METRIC[(1)]		ISOS141 DBQ (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISOS141						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 50-MHz 50% duty cycle square wave			200	mW
P_{D1}	Maximum power dissipation (side-1)				75	mW
P_{D2}	Maximum power dissipation (side-2)				125	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			DBQ-16	
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>3.7	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	>3.7	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-III	
DIN VDE V 0884-11:2017-01 (2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	848	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test See 図 10-7	600	V_{RMS}
		DC voltage	848	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification)	4000	V_{PK}
q_{pd}	Apparent charge(4)	Method a, After Input-output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b; At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 x sin (2πft), f = 1 MHz	~1	pF
R_{IO}	Isolation resistance(5)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		55/125/21	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *basic electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

VDE	UL
Certifying according to DIN VDE V 0884-11:2017-01	Certifying according to UL 1577 Component Recognition Program
Maximum transient isolation voltage, 4242 V_{PK} (DBQ-16); Maximum repetitive peak isolation voltage, 848 V_{PK} (DBQ-16); Maximum surge isolation voltage, 4000 V_{PK} (DBQ-16)	Single protection, 3000 V_{RMS}
Basic certificate: planned	File number: planned

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DBQ-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ =109°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C See 図 6-1			209	mA
		$R_{\theta JA}$ = 109°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C See 図 6-1			319	mA
		$R_{\theta JA}$ = 109°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C See 図 6-1			417	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 109°C/W, T_J = 150°C, T_A = 25°C See 図 6-2			1147	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -4 mA; See 図 8-1	V_{CCO} - 0.4 ((1))			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See 図 8-1			0.4	V
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V; See 図 8-4	85	100		kV/us
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 5 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.10 Supply Current Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISOS141							
Supply current - Disable	EN1 = EN2 = 0 V; V_I = 0 V (ISOS141)		I_{CC1}		1	1.5	mA
			I_{CC2}		0.8	1.1	
	EN1 = EN2 = 0 V; V_I = V_{CCI} ((1))(ISOS141)		I_{CC1}		4.3	6.3	
			I_{CC2}		1.8	2.7	
Supply current - DC signal ((2))	EN1 = EN2 = V_{CCI}; V_I = 0 V (ISOS141)		I_{CC1}		1.5	2.3	
			I_{CC2}		2	3	
	EN1 = EN2 = V_{CCI}; V_I = V_{CCI} (ISOS141)		I_{CC1}		4.8	6.8	
			I_{CC2}		3.2	4.9	
Supply current - AC signal ((3))	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.2	4.6	
			I_{CC2}		2.8	4.1	
		10 Mbps	I_{CC1}		3.7	5.2	
			I_{CC2}		4.2	5.7	
		100 Mbps	I_{CC1}		8.6	11.3	
			I_{CC2}		18	22	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx} and ENx = open
(3) Supply current valid for ENx = V_{CCx}

6.11 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -2mA; See 図 8-1	V_{CCO} - 0.3 ((1))			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA; See 図 8-1			0.3	V
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V; See 図 8-4	85	100		kV/us
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.12 Supply Current Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISOS141							
Supply current - Disable	EN1 = EN2 = 0 V; V_I = 0 V (ISOS141)		I_{CC1}		1	1.5	mA
			I_{CC2}		0.8	1.1	
	EN1 = EN2 = 0 V; V_I = V_{CC1} ((1))(ISOS141)		I_{CC1}		4.3	6.3	
			I_{CC2}		1.9	2.7	
Supply current - DC signal ((2))	EN1 = EN2 = V_{CCI}; V_I = 0 V (ISOS141)		I_{CC1}		1.5	2.3	
			I_{CC2}		2	3	
	EN1 = EN2 = V_{CCI}; V_I = V_{CCI} (ISOS141)		I_{CC1}		4.8	6.8	
			I_{CC2}		3.2	4.9	
Supply current - AC signal ((3))	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.2	4.6	
			I_{CC2}		2.7	4.1	
		10 Mbps	I_{CC1}		3.5	5	
			I_{CC2}		3.7	5.2	
		100 Mbps	I_{CC1}		6.8	9.3	
			I_{CC2}		13.7	16.4	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx} and ENx = open
(3) Supply current valid for ENx = V_{CCx}

6.13 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -1mA; See 図 8-1	V_{CCO} - 0.2 ((1))			V
V_{OL}	Low-level output voltage	I_{OL} = 1mA; See 図 8-1			0.2	V
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V; See 図 8-4	85	100		kV/us
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.14 Supply Current Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISOS141							
Supply current - Disable	EN1 = EN2 = 0 V; V_I = 0 V (ISOS141)		I_{CC1}		1	1.5	mA
			I_{CC2}		0.8	1.1	
	EN1 = EN2 = 0 V; V_I = V_{CC1} ((1))(ISOS141)		I_{CC1}		4.3	6.3	
			I_{CC2}		1.8	2.7	
Supply current - DC signal ((2))	EN1 = EN2 = V_{CCI}; V_I = 0 V (ISOS141)		I_{CC1}		1.4	2.3	
			I_{CC2}		2	3	
	EN1 = EN2 = V_{CCI}; V_I = V_{CCI} (ISOS141)		I_{CC1}		4.7	6.8	
			I_{CC2}		3.2	4.9	
Supply current - AC signal ((3))	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.1	4.6	
			I_{CC2}		2.7	4	
		10 Mbps	I_{CC1}		3.4	4.9	
			I_{CC2}		3.5	4.9	
		100 Mbps	I_{CC1}		5.6	8.3	
			I_{CC2}		10.8	13.8	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx} and ENx = open
(3) Supply current valid for ENx = V_{CCx}

6.15 Switching Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 8-1		10.7	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				4.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.4	ns
t_r	Output signal rise time	See 図 8-1		2.4	3.9	ns
t_f	Output signal fall time			2.4	3.9	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See 図 8-2		9	20	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			9	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISOS141 with F suffix			3	8.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISOS141 with F suffix			7	20	ns
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.7V. See 図 8-3		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.8		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 8-1		11	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				5	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See 図 8-1		1.3	3	ns
t_f	Output signal fall time			1.3	3	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See 図 8-2		17	30	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			17	30	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISOS141 with F suffix			3.2	8.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISOS141 with F suffix			17	30	ns
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.7V. See 図 8-3		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.9		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.17 Switching Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 8-1		12	18.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				5.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.6	ns
t_r	Output signal rise time	See 図 8-1		1	3.5	ns
t_f	Output signal fall time			1	3.5	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See 図 8-2		22	40	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			22	40	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISOS141 with F suffix			3.3	8.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISOS141 with F suffix			18	40	ns
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.7V. See 図 8-3		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.7		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.18 Insulation Characteristics Curves

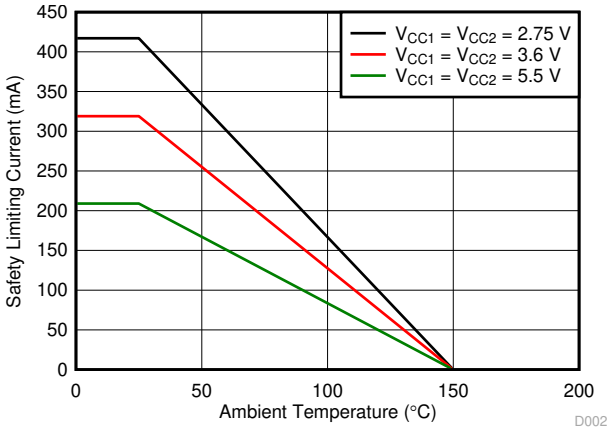


図 6-1. Thermal Derating Curve for Safety Limiting Current for DBQ-16 Package

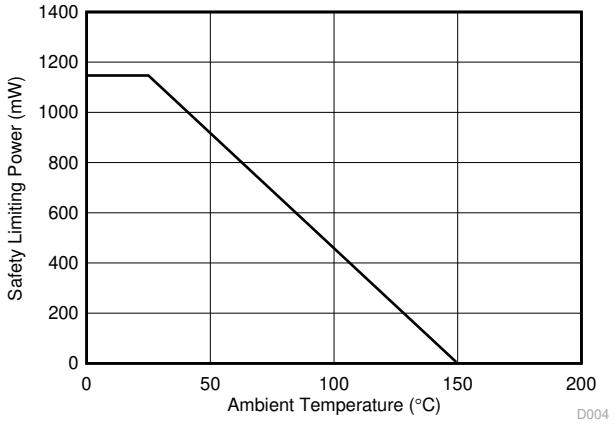
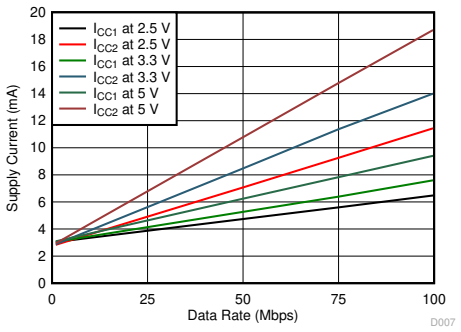


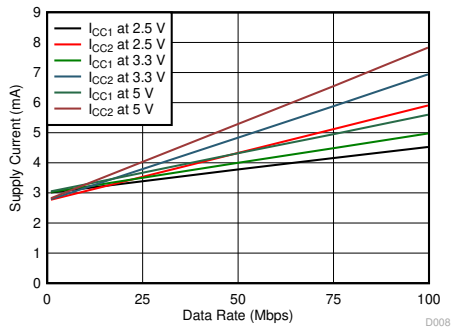
図 6-2. Thermal Derating Curve for Safety Limiting Power for DBQ-16 Package

6.19 Typical Characteristics



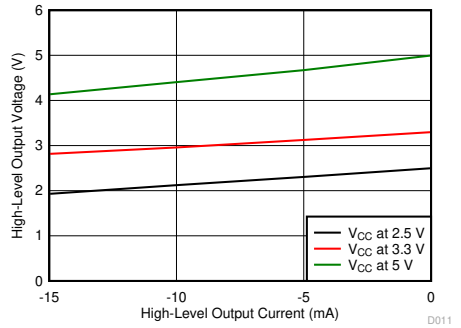
T_A = 25°C C_L = 15 pF

図 6-3. Supply Current vs Data Rate (With 15-pF Load)



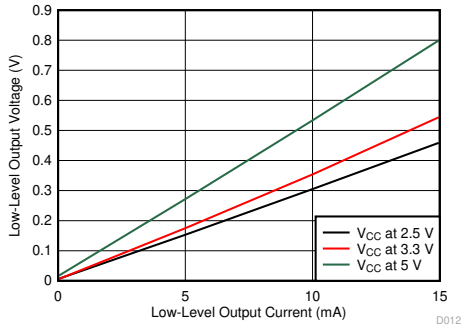
T_A = 25°C C_L = No Load

図 6-4. Supply Current vs Data Rate (With No Load)



T_A = 25°C

図 6-5. High-Level Output Voltage vs High-level Output Current



T_A = 25°C

図 6-6. Low-Level Output Voltage vs Low-Level Output Current

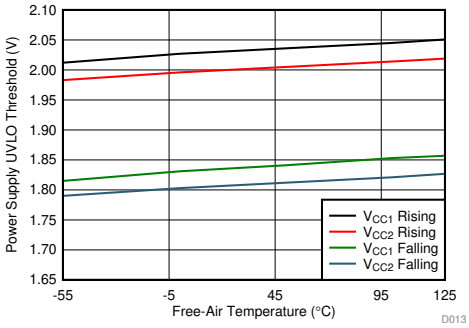


図 6-7. Power Supply Undervoltage Threshold vs Free-Air Temperature

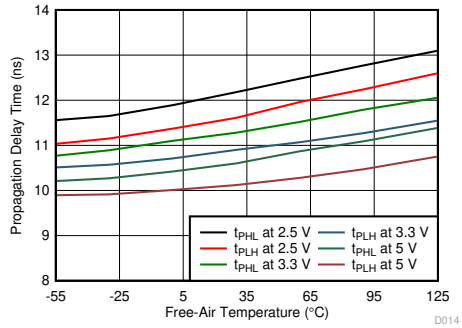
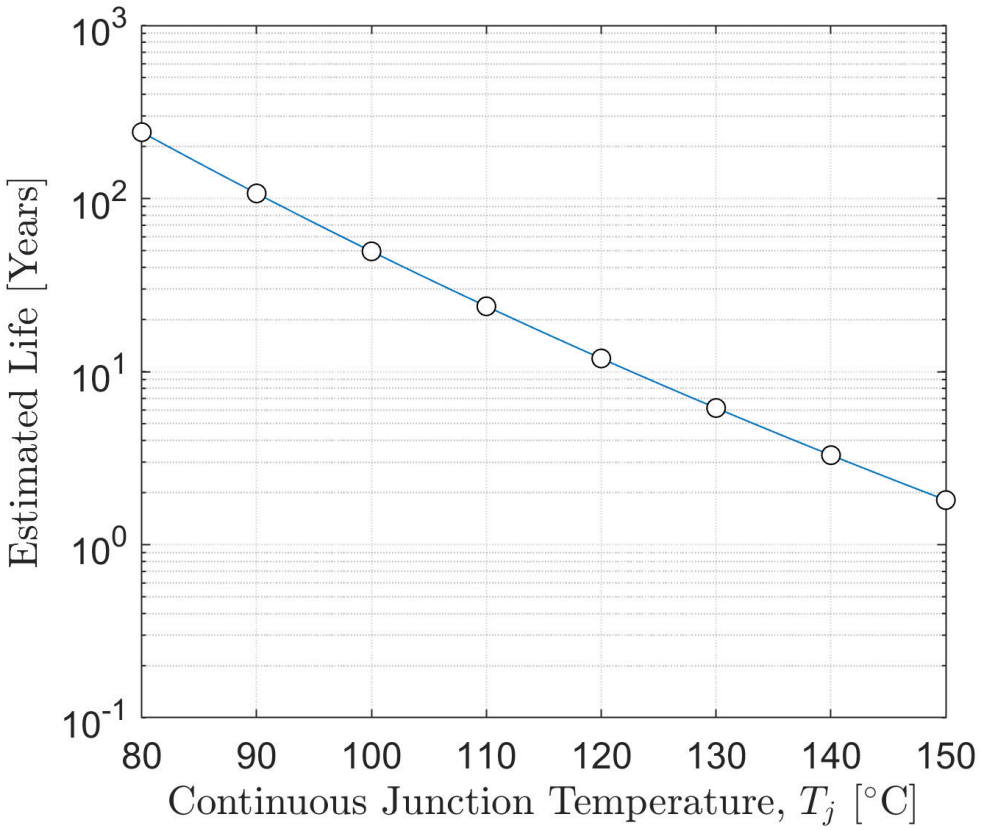


図 6-8. Propagation Delay Time vs Free-Air Temperature

7 Operating Life Deration

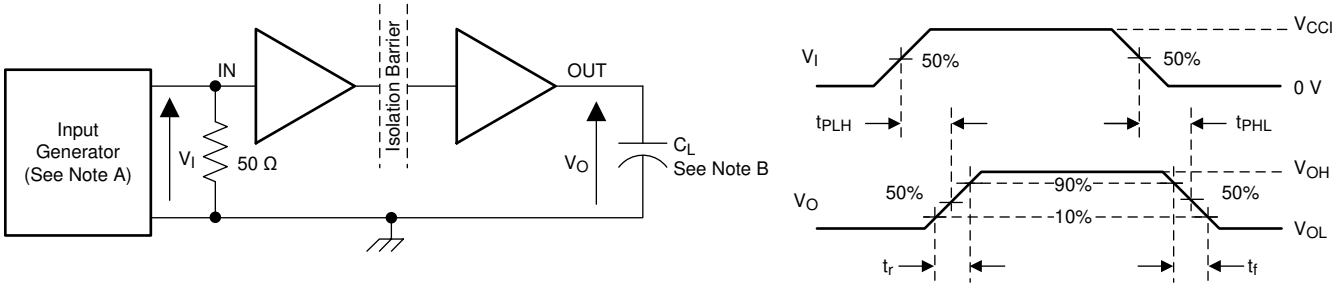
The information in this section is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.



1. Silicon operating life design goal is 100000 power-on hours (POH) at 105 °C junction temperature (does not include package interconnect life).
2. The predicted operating lifetime versus junction temperature is based on reliability modeling using wirebond lifetime as the dominant failure mechanism affecting device wear out for the specific device process and design characteristics.

Wirebond Life Derating Curve

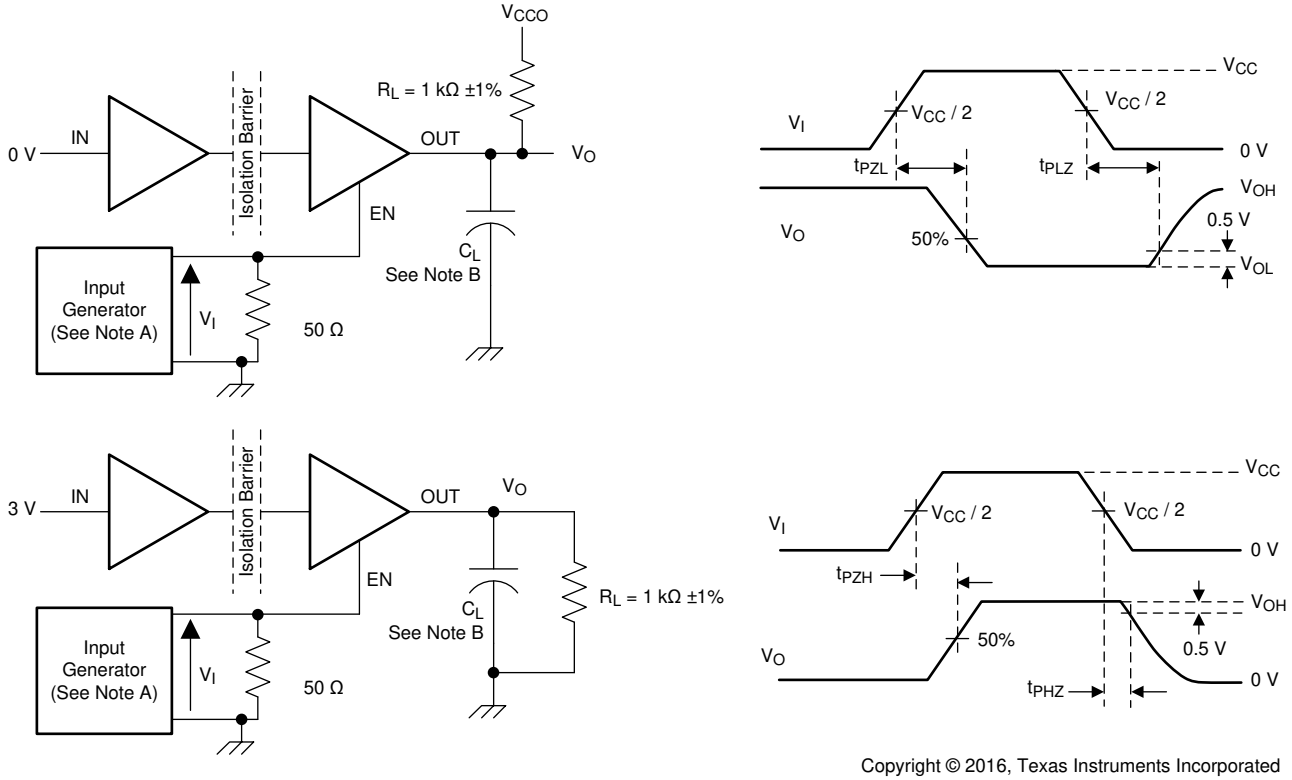
8 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

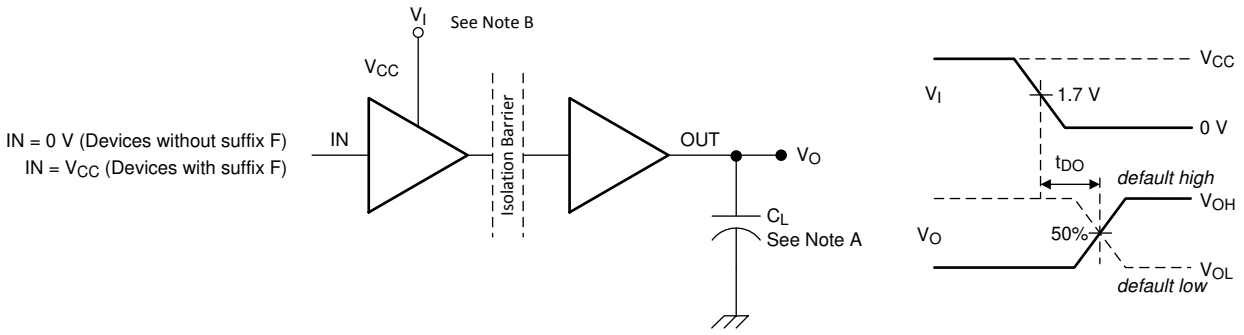
図 8-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

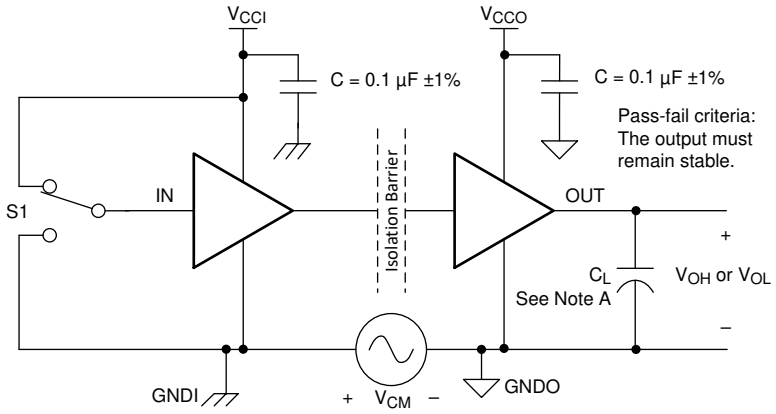
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 8-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.
B. Power Supply Ramp Rate = 10 mV/ns

図 8-3. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 8-4. Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The ISOS141-SEP has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The ISOS141-SEP device also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, 図 9-1, shows a functional block diagram of a typical channel.

9.2 Functional Block Diagram

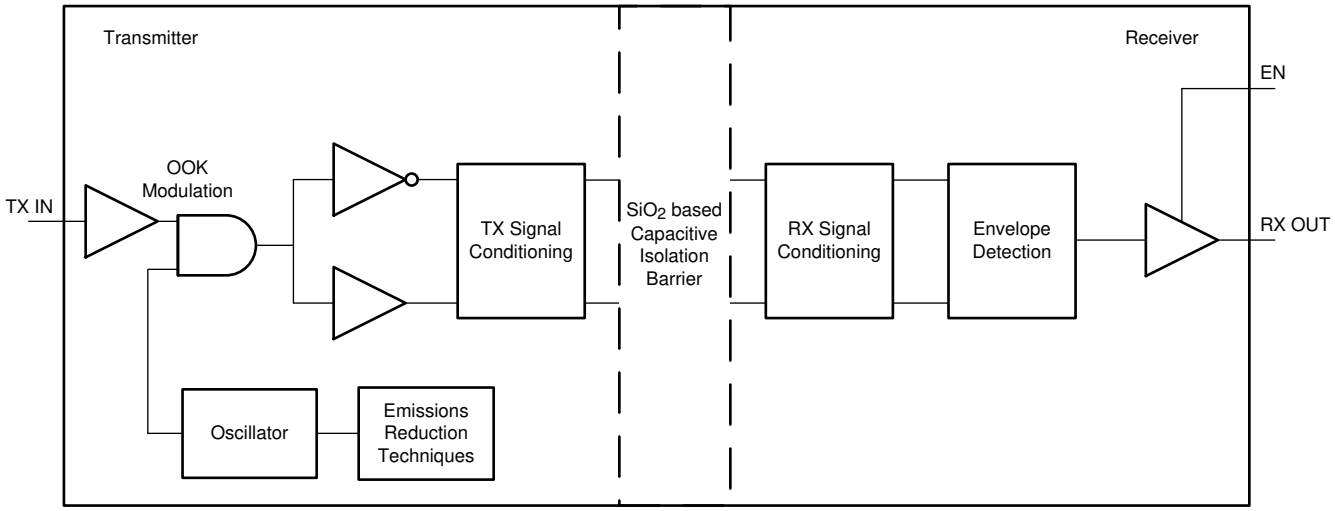


図 9-1. Conceptual Block Diagram of a Digital Capacitive Isolator

図 9-2 shows a conceptual detail of how the ON-OFF keying scheme works.

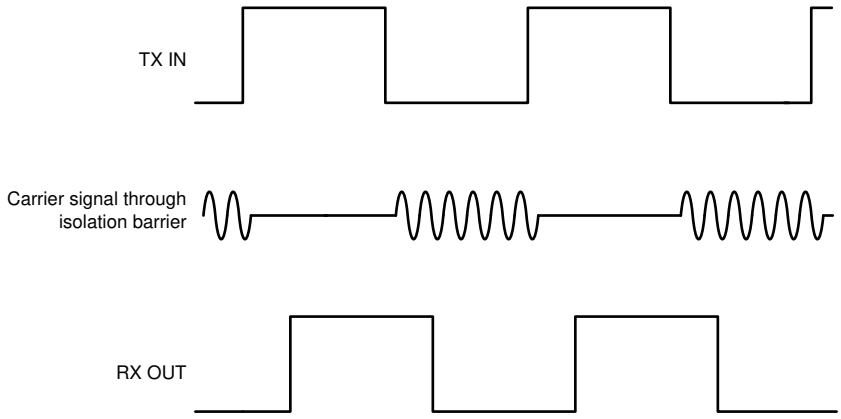


図 9-2. On-Off Keying (OOK) Based Modulation Scheme

9.3 Feature Description

表 9-1 provides an overview of the device features.

表 9-1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION(1)
ISOS141-SEP With F suffix	3 Forward, 1 Reverse	100 Mbps	Low	DBQ-16	3000 V_{RMS} / 4242 V_{PK}

(1) See セクション 6.7 for detailed isolation ratings.

9.3.1 Radiation Tolerance

Total Ionizing Dose (TID)— ISOS141-SEP is a radiation tolerant, TI Space Enhanced Plastic (Space EP) device, and as such it has a Total Ionizing Dose (TID) level specified in the “Device Information” table on the front page. Testing and qualification of these products is done on a wafer level according to MIL-STD-883, Test Method 1019. Radiation Lot Acceptance Testing (RLAT) is performed at the 30-krad TID levels. A TID characterization report is available. Group E TID RLAT data are available with lot shipments as part of the QCI summary reports.

Single-Event Effects (SEE)— one-time SEE characterization was performed according to EIA/JEDEC standard, EIA/JEDEC57 to linear energy transfer (LET) = 43 MeV·cm^2/mg. During testing, no Single-Event Latch-Up (SEL) or Single-Event Dielectric Rupture (SEDR) were observed.

Neutron Displacement Damage (NDD)— ISOS141-SEP was irradiated up to 1 × 10^{12} n/cm^2 . A sample size of 15 units was exposed to radiation testing per MILSTD-883, Method 1017 for Neutron Irradiation.

Radiation Testing and Characterization Reports— are available for all radiation effects described in this section, to find the latest reports go to the ISOS141-SEP Technical Documentation section on TI.com.

9.3.2 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISOS141-SEP device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

9.4 Device Functional Modes

表 9-2 lists the functional modes for the ISOS141-SEP.

表 9-2. Function Table

V_{CCI}	V_{CCO}	INPUT (INx)(2)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of its input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to its default logic state. Default is *Low* for ISOS141-SEP with F suffix.
X	PU	X	L	Z	A low value of output enable causes the outputs to be high-impedance.
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *Low* for ISOS141-SEP with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined(1). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.

(1) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.
(2) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.

9.4.1 Device I/O Schematics

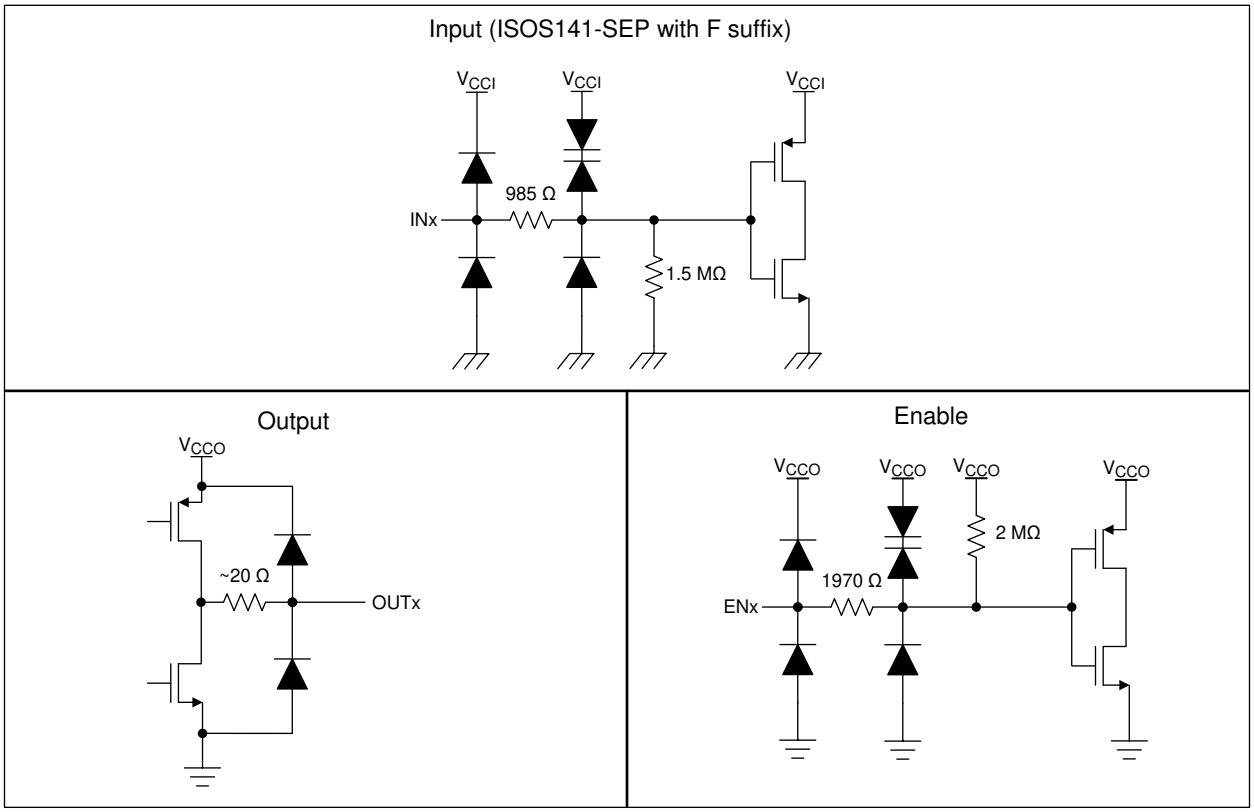


図 9-3. Device I/O Schematics

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ISOS141-SEP four channel digital isolator provides flexibility for multiple use cases in LEO applications. Used in conjunction with isolated power supplies, these devices help prevent noise currents on data buses, such as UART, SPI, RS-485, RS-232, and CAN from damaging sensitive circuitry. It can also be used to isolate multiple static signals in a system to provide additional redundancy and robustness. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard.

Additionally, this digital isolator can be used as a logic-level translator in addition to providing isolation. Since an isolation barrier separates the two sides, each side can be sourced independently with any voltage within recommended operating conditions. The supply voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. As an example, it is possible to supply ISOS141-SEP V_{CC1} with 3.3 V (which is within 2.25 V to 5.5 V) and V_{CC2} with 5V (which is also within 2.25 V to 5.5 V).

10.2 Typical Application

図 10-1 shows ISOS141-SEP in the GaN half bridge circuit being used to isolate PWM signals from the half-bridge controller on the primary side to the half-bridge gate driver on the secondary side to achieve higher efficiency through synchronous rectification.

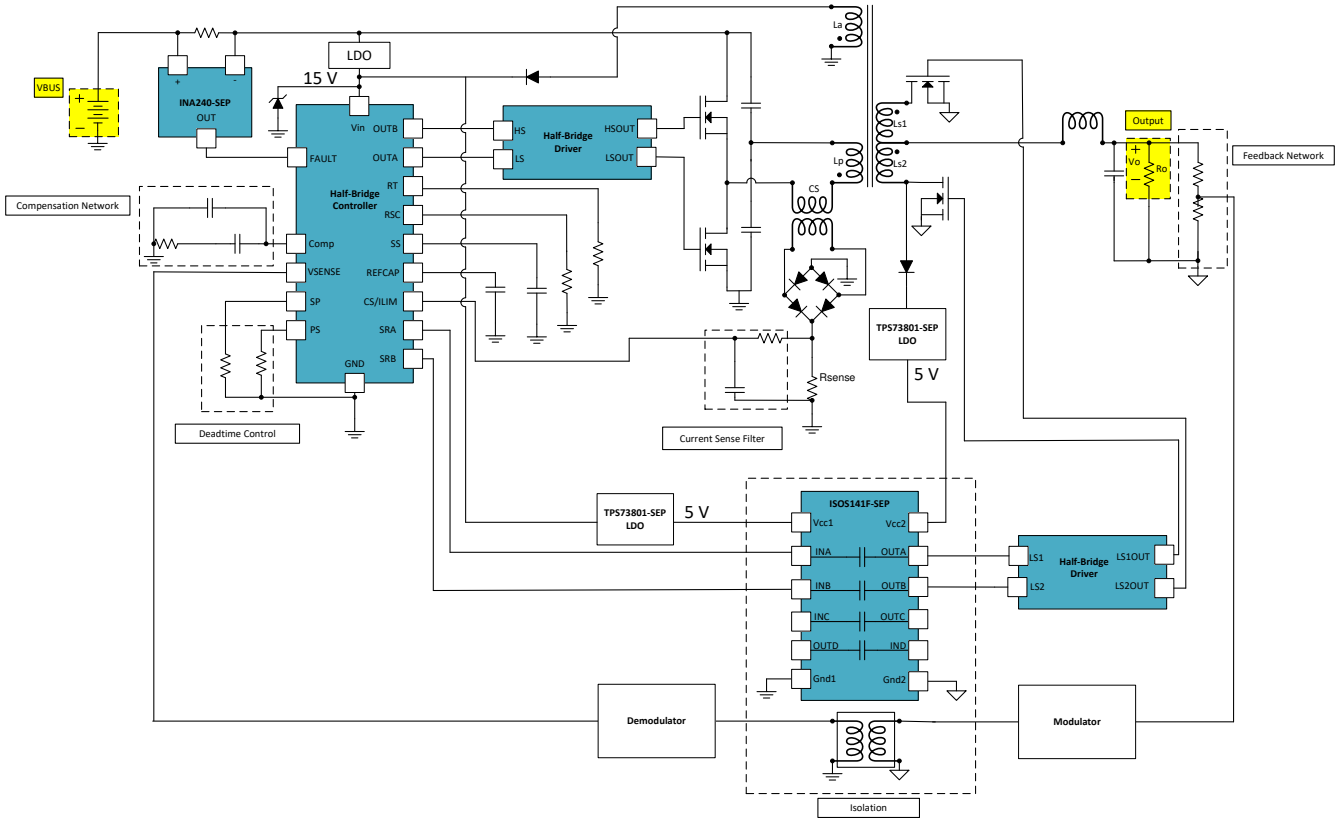


図 10-1. Isolated 75V to 5V 50W GaN-Based Half-Bridge Topology

10.2.1 Design Requirements

To design with these devices, use the parameters listed in 表 10-1.

表 10-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

10.2.2 Detailed Design Procedure

The ISOS141-SEP device only require two external bypass capacitors to operate.

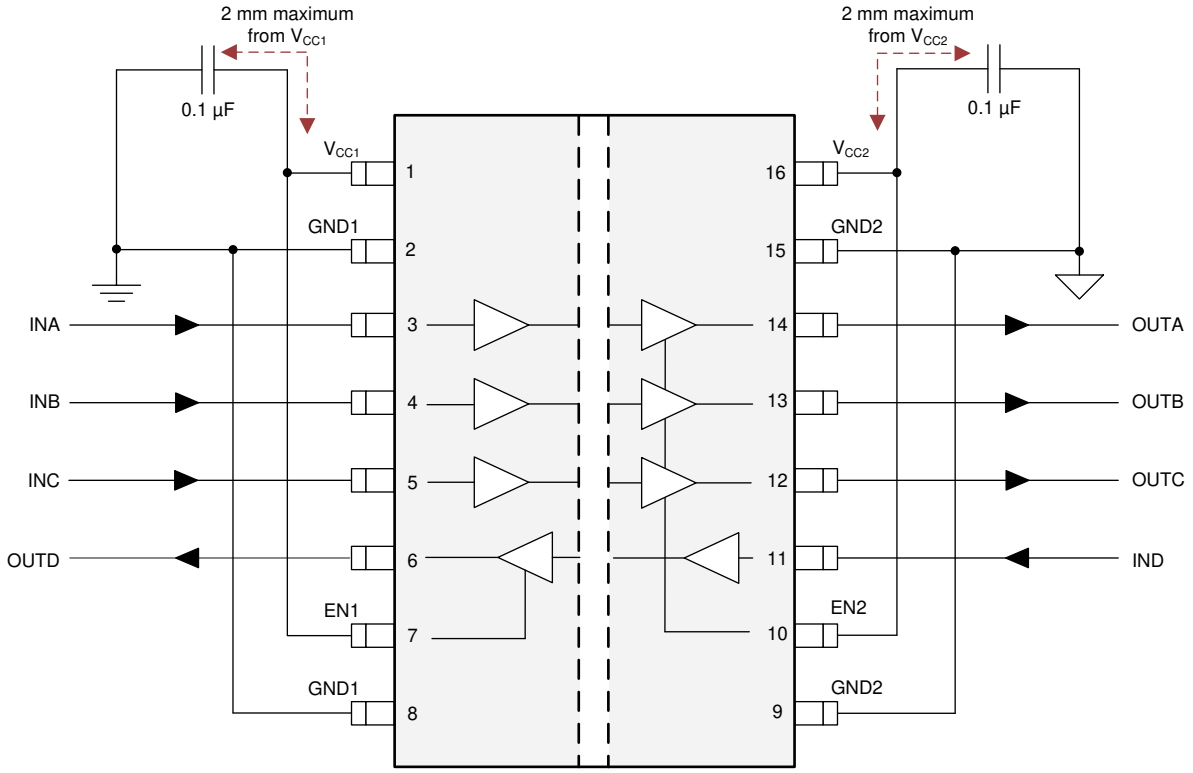


図 10-2. Typical ISOS141-SEP Circuit Hook-up

10.2.3 Application Curve

The following typical eye diagrams of the ISOS141-SEP device indicates low jitter and wide open eye at the maximum data rate of 100 Mbps.

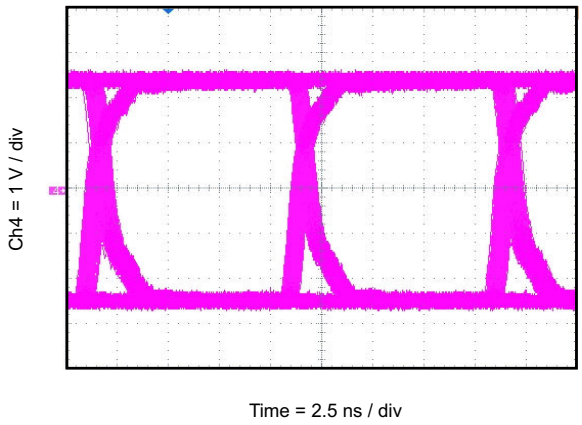


図 10-3. Eye Diagram at 100 Mbps PRBS 2^{16} – 1, 5 V and 25°C

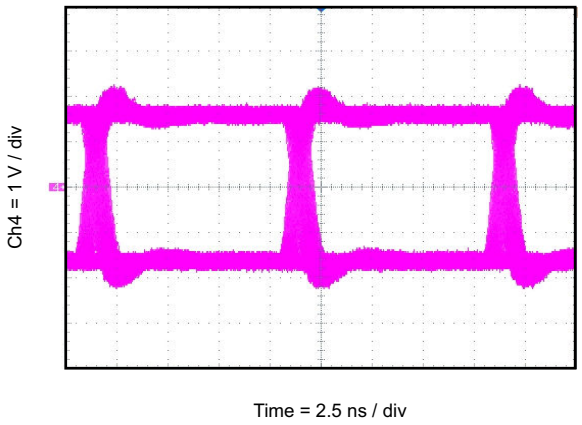


図 10-4. Eye Diagram at 100 Mbps PRBS 2^{16} – 1, 3.3 V and 25°C

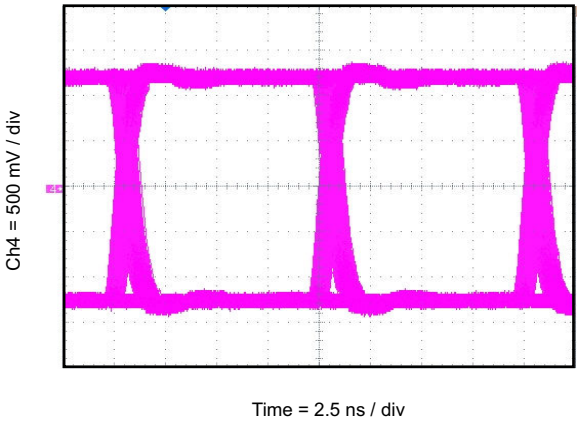


図 10-5. Eye Diagram at 100 Mbps PRBS 2^{16} – 1, 2.5 V and 25°C

10.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See 図 10-6 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

図 10-7 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the insulation withstand capability of DBQ-16 package is 600 V_{RMS} with a lifetime of >1000 years as illustrated in 図 10-7. Factors, such as package size, pollution degree, and material group can limit the working voltage of a component.

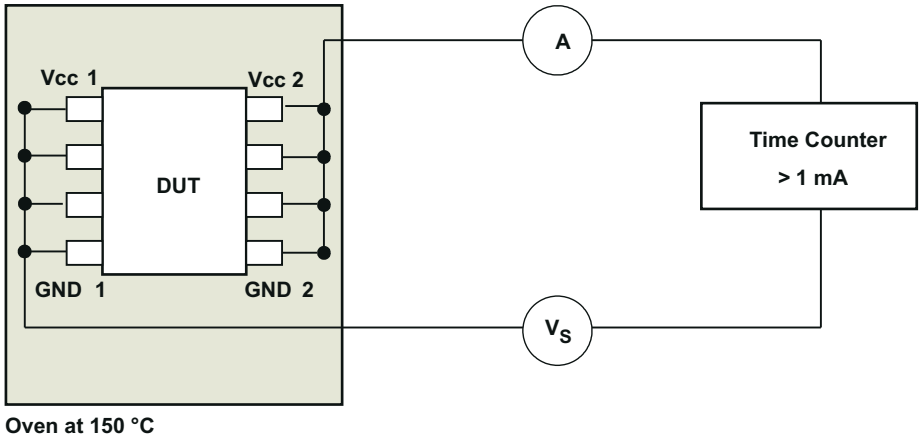


図 10-6. Test Setup for Insulation Lifetime Measurement

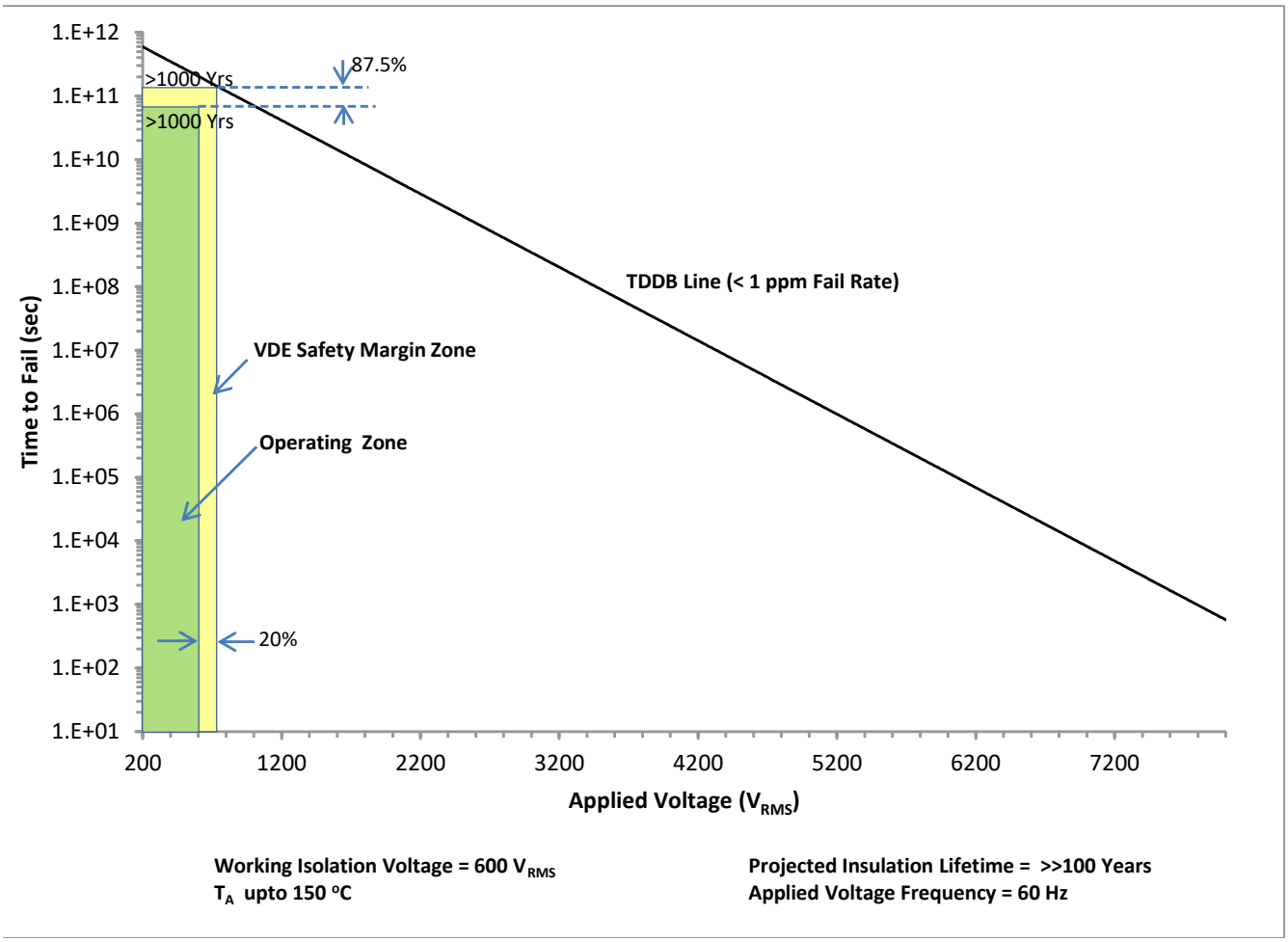


図 10-7. Insulation Lifetime Projection Data

11 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible.

12 Layout

12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 図 12-1). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

12.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

12.2 Layout Example

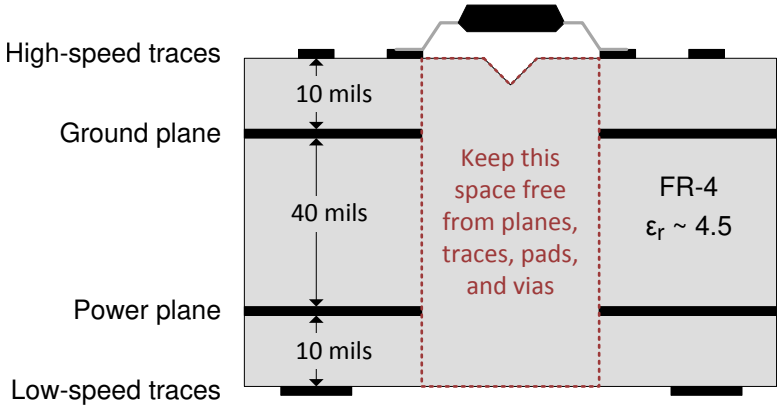


図 12-1. Layout Example Schematic

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Radiation hardened 3.3V CAN transceiver in space enhanced plastic package with standby mode* datasheet
- Texas Instruments, *Radiation hardened RS-422 dual differential drivers and receivers in space Enhanced Plastic* datasheet
- Texas Instruments, *Radiation-hardened, 2.2-V to 20-V, 1-A low-noise adjustable output LDO in Space Enhanced Plastic* datasheet
- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems* application report

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

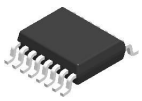
13.3 Community Resources

13.4 Trademarks

すべての商標は、それぞれの所有者に帰属します。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

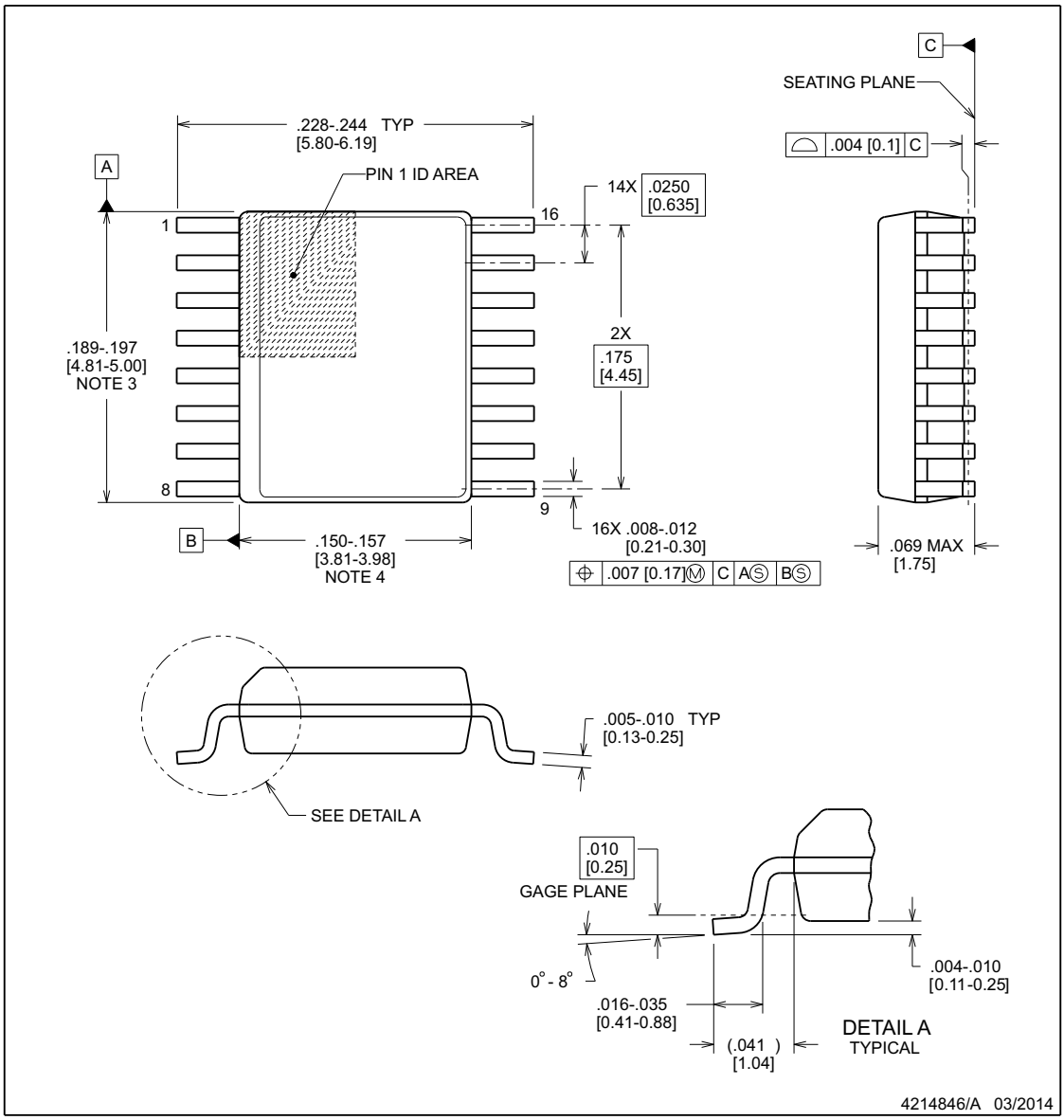


PACKAGE OUTLINE

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



NOTES:

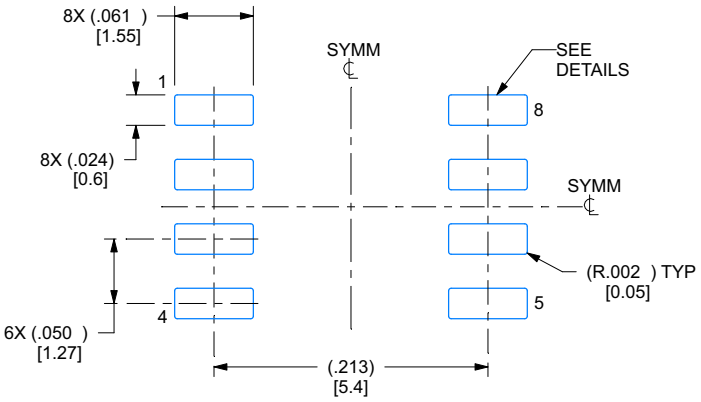
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

EXAMPLE BOARD LAYOUT

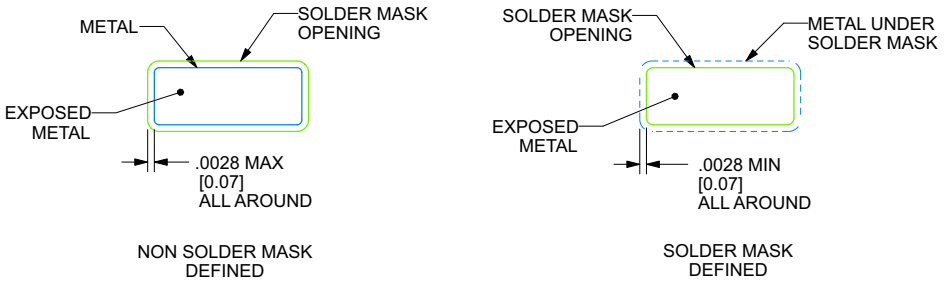
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

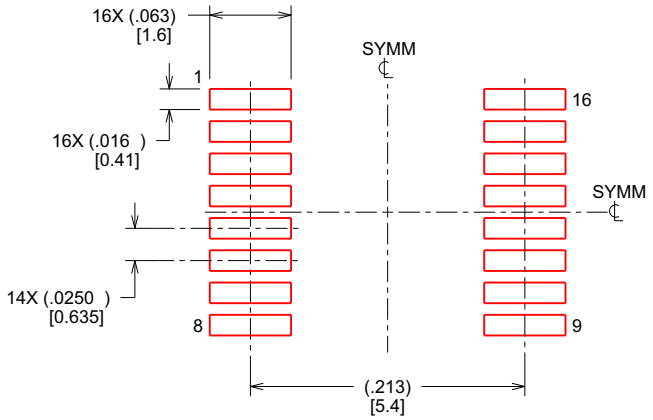
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A — **SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISOS141FDBQSEP	Active	Production	SSOP (DBQ) | 16	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	141FSE
ISOS141FDBQTSEP	Active	Production	SSOP (DBQ) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	141FSE
V62/21610-01XE	Active	Production	SSOP (DBQ) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	141FSE
V62/21610-01XE-T	Active	Production	SSOP (DBQ) | 16	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	141FSE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

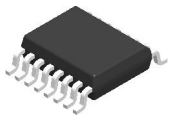
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

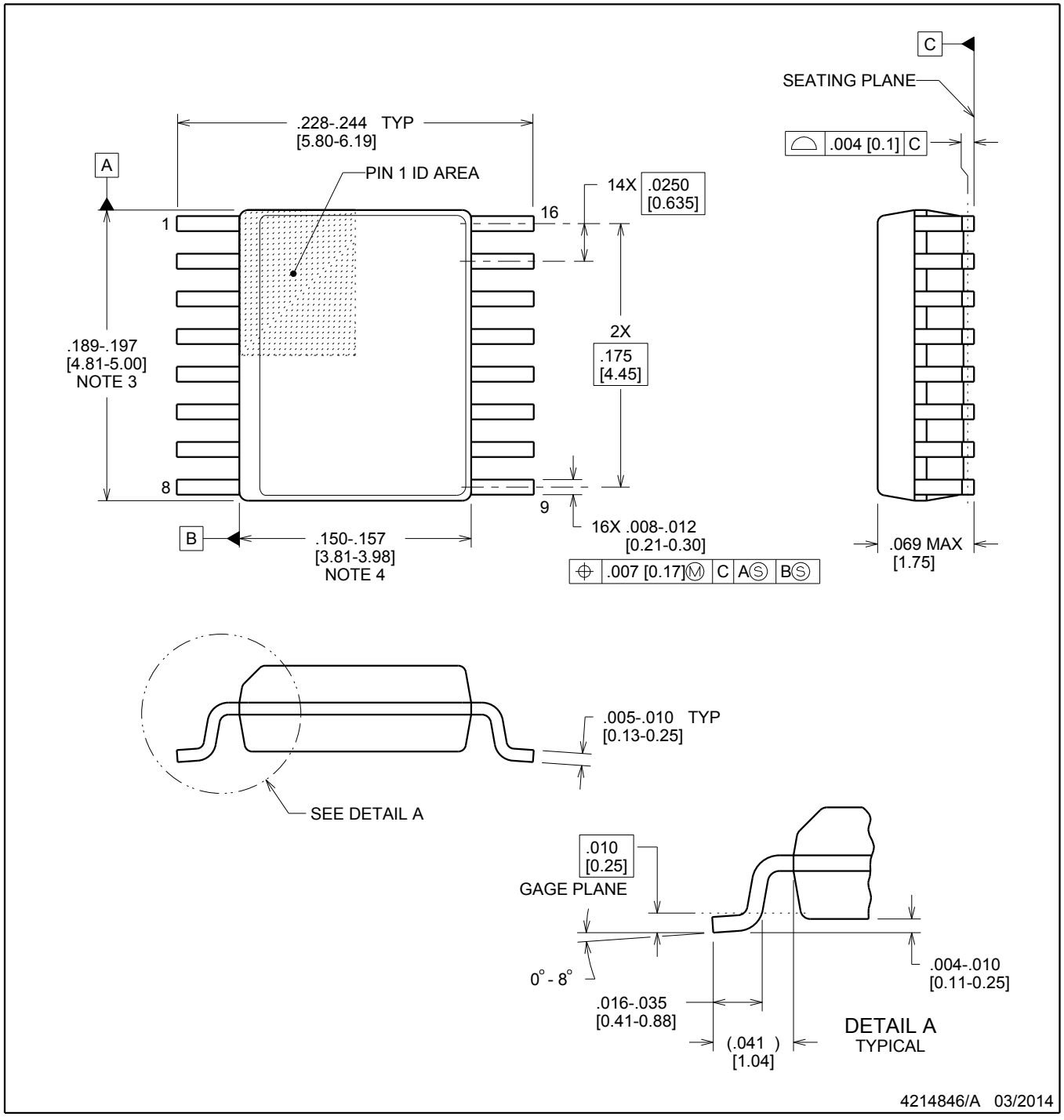


PACKAGE OUTLINE

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



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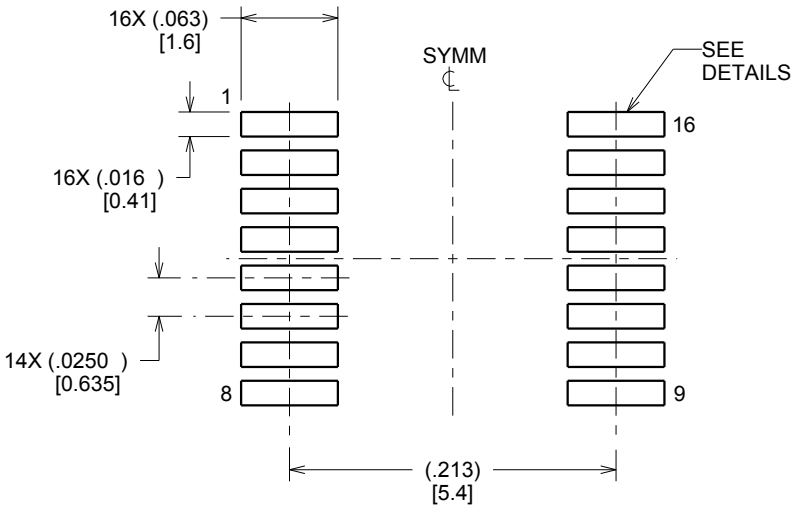
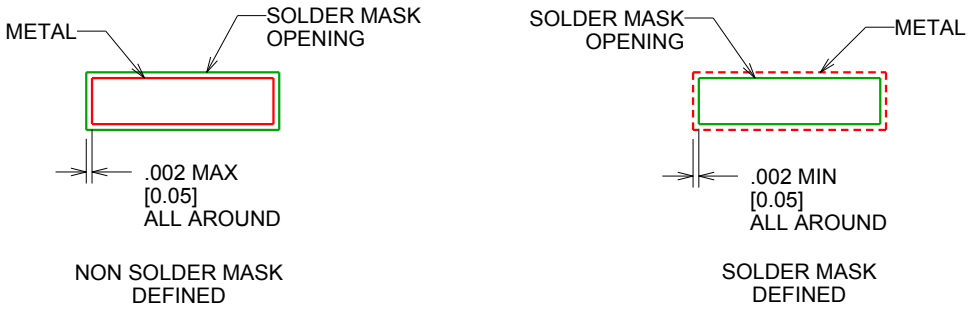


LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

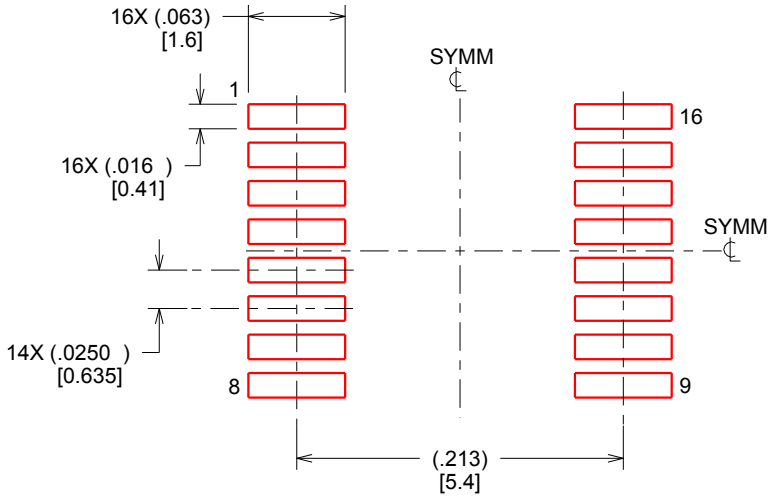
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月