ISO7830x High-Performance, 8000V_{PK} Reinforced Triple Digital Isolators

1 Features

- Signaling Rate: Up to 100Mbps
- Wide Supply Range: 2.25V to 5.5V
- 2.25V to 5.5V Level Translation
- Wide Temperature Range: –55°C to 125°C
- Low Power Consumption, Typical 1.6mA per Channel at 1Mbps
- Low Propagation Delay: 11ns Typical (5V Supplies)
- Industry leading CMTI (min): ±100kV/μs
- Robust Electromagnetic Compatibility (EMC)
- System-Level ESD, EFT, and Surge Immunity
- Low Emissions
- Isolation Barrier Life: > 40 Years
- SOIC-16 Wide Body (DW) and Extra-Wide Body (DWW) Package Options
- Safety-Related Certifications:
  - 8000V_{PK} Reinforced Isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 5.7kV_{RMS} Isolation for 1 Minute per UL 1577
  - IEC 61010-1, IEC 62368-1, IEC 60601-1, and GB 4943.1 certifications

2 Applications

- Industrial Automation
- Motor Control
- Power Supplies
- Solar Inverters
- Medical Equipment
- Hybrid Electric Vehicles

3 Description

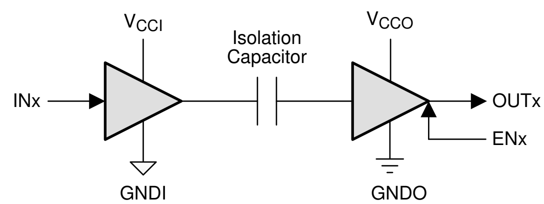
The ISO7830x device is a high-performance, 3-channel digital isolator with 8000V_{PK} isolation voltage. This device has reinforced isolation certifications according to VDE, CSA, TUV and CQC. The isolator provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os.

Each isolation channel has a logic input and output buffer separated by silicon dioxide (SiO_2) insulation barrier. This device comes with enable pins which can be used to put the respective outputs in high impedance for multi-master driving applications and to reduce power consumption. The ISO7830x device has three forward and no reverse-direction channels. If the input power or signal is lost, the default output is *high* for the ISO7830 device and *low* for the ISO7830F device. See *Section 7.4* for further details.

Used in conjunction with isolated power supplies, this device helps prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through remarkable chip design and layout techniques, electromagnetic compatibility of ISO7830x has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. ISO7830x is available in a 16-pin SOIC wide-body (DW) and extra-wide body (DWW) packages.

Package Information

PART NUMBER	PACKAGE	PACKAGE SIZE
ISO7830 ISO7830F	DW (16, SOIC)	10.30mm × 7.50mm
	DWW (16, SOIC)	10.30mm × 14.0mm



V_{CCI} and GNDI are supply and ground connections respectively for the input channels.
V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

Simplified Schematic

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4 Pin Configuration and Functions

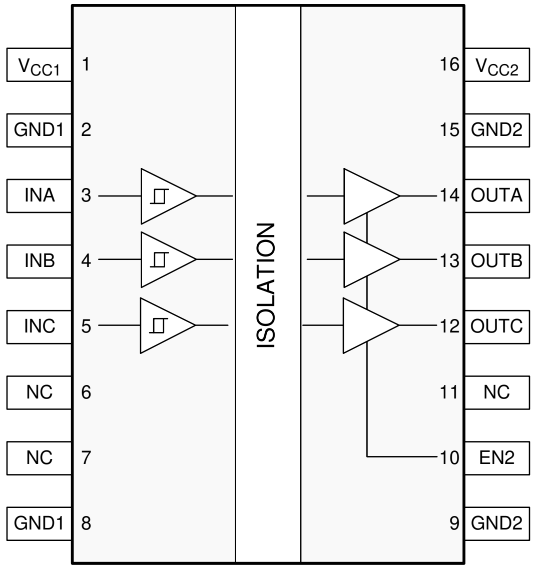


Figure 4-1. DW and DWW Packages 16-Pin SOIC Top View

Pin Functions

PIN		Type[1]	DESCRIPTION
NAME	NO.		
EN2	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2, 8	—	Ground connection for V_{CC1}
GND2	9, 15	—	Ground connection for V_{CC2}
INA	3	I	Input, channel A
INB	4	I	Input, channel B
INC	5	I	Input, channel C
OUTA	14	O	Output, channel A
OUTB	13	O	Output, channel B
OUTC	12	O	Output, channel C
NC	6, 7, 11	—	Not connected
V_{CC1}	1	—	Power supply, side 1
V_{CC2}	16	—	Power supply, side 2

(1) I = Input, O = Output

5 Specifications

5.1 Absolute Maximum Ratings

See [(1)]

		MIN	MAX	UNIT
V_{CC1} V_{CC2}	Supply voltage[(2)]	–0.5	6	V
V	Voltage at INx, OUTx, or EN2x	–0.5	V_{CCx} + 0.5[(3)]	V
I_O	Output current	–15	15	mA
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6V

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
I_{OH}	High-level output current	V_{CCO} [(1)] = 5V	–4			mA
		V_{CCO} [(1)] = 3.3V	–2			
		V_{CCO} [(1)] = 2.5V	–1			
I_{OL}	Low-level output current	V_{CCO} [(1)] = 5V			4	mA
		V_{CCO} [(1)] = 3.3V			2	
		V_{CCO} [(1)] = 2.5V			1	
V_{IH}	High-level input voltage		0.7 × V_{CCI} [(1)]		V_{CCI} [(1)]	V
V_{IL}	Low-level input voltage		0		0.3 × V_{CCI} [(1)]	V
DR	Signaling rate		0		100	Mbps
T_A	Ambient temperature		–55	25	125	°C

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

5.4 Thermal Information

THERMAL METRIC[(1)]		ISO7830		UNIT
		DW (SOIC)	DWW (SOIC)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.1	83.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	43.8	45.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.7	54.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.0	17.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	45.2	53.3	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Power Rating

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF, input a 50MHz 50% duty cycle square wave			150	mW
P_{D1}	Maximum power dissipation by side-1				25	mW
P_{D2}	Maximum power dissipation by side-2				125	mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATION		UNIT
			DW	DWW	
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	>8	>14.5	mm
		Shortest terminal-to-terminal distance through air (typical)		15.0	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	>8	>14.5	mm
		Shortest terminal-to-terminal distance across the package surface (typical)		15.0	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	>21	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	>600	V
	Material group		I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ $600V_{RMS}$	I–IV	I–IV	
		Rated mains voltage ≤ $1000V_{RMS}$	I–III	I–IV	
DIN EN IEC 60747-17 (VDE 0884-17) [2]					
V_{IORM}	Maximum repetitive peak isolation voltage		2121	2828	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); Time dependent dielectric breakdown (TDDB) Test, see Figure 5-1 and Figure 5-2	1500	2000	V_{RMS}
		DC voltage	2121	2828	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1s (100% production)	8000	8000	V_{PK}
V_{IMP}	Maximum impulse voltage [3]	Tested in air, 1.2/50μs waveform per IEC 62368-1	9800	9800	V_{PK}
V_{IOSM}	Maximum surge isolation voltage [4]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-μs waveform per IEC 62368-1	12800	12800	V_{PK}
q_{pd}	Apparent charge [5]	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IOTM} = 2545V_{PK}$ (DW) and $3394V_{PK}$ (DWW), t_m = 10s	≤5	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM} = 3394V_{PK}$ (DW) and $4525V_{PK}$ (DWW), t_m = 10s	≤5	≤5	
		Method b: At routine test (100% production); $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)	≤5	≤5	
C_{IO}	Barrier capacitance, input to output[6]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1MHz	2	2	pF
R_{IO}	Isolation resistance, input to output [6]	V_{IO} = 500V, T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500V at T_S = 150°C	$>10^{9}$	$>10^{9}$	
	Pollution degree		2	2	
	Climatic category		55/125/21	55/125/21	
UL 1577					
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5700V_{RMS}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6840V_{RMS}$, t = 1s (100% production)	5700	5700	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-terminal device.

5.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1 and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1	Certified according to EN 61010-1 and EN 62368-1
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716	Client ID number: 77311

5.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 81.1°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C, see Figure 5-3			280	mA
		$R_{\theta JA}$ = 81.1°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C, see Figure 5-3			428	
		$R_{\theta JA}$ = 81.1°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C, see Figure 5-3			560	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 81.1°C/W, T_J = 150°C, T_A = 25°C, see Figure 5-5			1541	mW
T_S	Maximum safety temperature				150	°C
DWW PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 83.4°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C, see Figure 5-4			273	mA
		$R_{\theta JA}$ = 83.4°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C, see Figure 5-4			416	
		$R_{\theta JA}$ = 83.4°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C, see Figure 5-4			545	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 83.4°C/W, T_J = 150°C, T_A = 25°C, see Figure 5-6			1499	mW
T_S	Maximum safety temperature				150	°C

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Section 5.4* is that of a device installed on a high-K test board for leaded surface mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

5.9 Electrical Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4mA; see Figure 6-1	V_{CCO} (1) – 0.4	V_{CCO} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4mA; see Figure 6-1		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI} (1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} at INx or EN2			10	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx or EN2	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0V, V_{CM} = 1500V; see Figure 6-4	100			kV/µs
C_I	Input capacitance (2)	V_I = V_{CC} / 2 + 0.4 × sin (2πft), f = 1MHz, V_{CC} = 5V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) Measured from input pin to ground.

5.10 Supply Current Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - disable	EN2 = 0V, V_I = 0V (Devices with suffix F), V_I = V_{CCI} (Devices without suffix F)		I_{CC1}		1.1	1.8	mA
			I_{CC2}		0.4	0.6	
	EN2 = 0V, V_I = V_{CCI} (Devices with suffix F), V_I = 0V (Devices without suffix F)		I_{CC1}		4.6	6.6	
			I_{CC2}		0.4	0.6	
Supply current - DC signal	V_I = 0V (Devices with suffix F), V_I = V_{CCI} (Devices without suffix F)		I_{CC1}		1.1	2	
			I_{CC2}		1.7	2.7	
	V_I = V_{CCI} (Devices with suffix F), V_I = 0V (Devices without suffix F)		I_{CC1}		4.6	6.8	
			I_{CC2}		1.9	2.8	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		2.8	4.4	
			I_{CC2}		1.9	3	
		10Mbps	I_{CC1}		2.9	4.4	
			I_{CC2}		3.3	4.6	
		100Mbps	I_{CC1}		3.9	4.9	
			I_{CC2}		17.5	20.8	

5.11 Electrical Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2mA; see Figure 6-1	V_{CCO} [(1)] – 0.4	V_{CCO} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2mA; see Figure 6-1		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI} [(1)]			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} at INx or EN2			10	μA
I_{IL}	Low-level input current	V_{IL} = 0V at INx or EN2	–10			μA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0V, V_{CM} = 1500V; see Figure 6-4	100			kV/μs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

5.12 Supply Current Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - disable	EN2 = 0V, V_I = 0V (Devices with suffix F), V_I = V_{CCI} (Devices without suffix F)		I_{CC1}		1.1	1.8	mA
			I_{CC2}		0.3	0.6	
	EN2 = 0V, V_I = V_{CCI} (Devices with suffix F), V_I = 0V (Devices without suffix F)		I_{CC1}		4.6	6.6	
			I_{CC2}		0.3	0.6	
Supply current - DC signal	V_I = 0V (Devices with suffix F), V_I = V_{CCI} (Devices without suffix F)		I_{CC1}		1.1	2	
			I_{CC2}		1.7	2.6	
	V_I = V_{CCI} (Devices with suffix F), V_I = 0V (Devices without suffix F)		I_{CC1}		4.6	6.8	
			I_{CC2}		1.9	2.8	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		2.8	4.4	
			I_{CC2}		1.9	2.9	
		10Mbps	I_{CC1}		2.9	4.4	
			I_{CC2}		2.9	4.1	
		100Mbps	I_{CC1}		3.5	4.8	
			I_{CC2}		13.2	16	

5.13 Electrical Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1mA; see Figure 6-1	V_{CCO} [(1)] – 0.4	V_{CCO} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 1mA; see Figure 6-1		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI} [(1)]			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} at INx or EN2			10	μA
I_{IL}	Low-level input current	V_{IL} = 0V at INx or EN2	–10			μA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0V, V_{CM} = 1500V; see Figure 6-4	100			kV/μs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

5.14 Supply Current Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - disable	EN2 = 0V, V_I = 0V (Devices with suffix F), V_I = V_{CCI} (Devices without suffix F)		I_{CC1}		1.1	1.8	mA
			I_{CC2}		0.3	0.6	
	EN2 = 0V, V_I = V_{CCI} (Devices with suffix F), V_I = 0V (Devices without suffix F)		I_{CC1}		4.6	6.6	
			I_{CC2}		0.3	0.6	
Supply current - DC signal	V_I = 0V (Devices with suffix F), V_I = V_{CCI} (Devices without suffix F)		I_{CC1}		1.1	2	
			I_{CC2}		1.7	2.6	
	V_I = V_{CCI} (Devices with suffix F), V_I = 0V (Devices without suffix F)		I_{CC1}		4.6	6.8	
			I_{CC2}		1.8	2.8	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		2.8	4.4	
			I_{CC2}		1.8	2.9	
		10Mbps	I_{CC1}		2.9	4.4	
			I_{CC2}		2.6	3.7	
		100Mbps	I_{CC1}		3.4	4.7	
			I_{CC2}		10.3	12.7	

5.15 Switching Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 6-1	6	11	16	ns
PWD	Pulse width distortion(1) $\|t_{PHL} – t_{PLH}\|$			0.55	4.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			2.5	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See Figure 6-1		1.7	3.9	ns
t_f	Output signal fall time			1.9	3.9	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 6-2		12	20	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			12	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7830			10	20	ns
	Enable propagation delay, high impedance-to-high output for ISO7830F			2	2.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7830			2	2.5	μs
	Enable propagation delay, high impedance-to-low output for ISO7830F			10	20	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See Figure 6-3		0.2	9	μs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100Mbps		0.90		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.16 Switching Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 6-1	6	10.8	16	ns
PWD	Pulse width distortion(1) $\|t_{PHL} – t_{PLH}\|$			0.7	4.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			2.2	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See Figure 6-1		0.8	3	ns
t_f	Output signal fall time			0.8	3	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 6-2		17	32	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			17	32	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7830			17	32	ns
	Enable propagation delay, high impedance-to-high output forISO7830F			2	2.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7830			2	2.5	μs
	Enable propagation delay, high impedance-to-low output for ISO7830F			17	32	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See Figure 6-3		0.2	9	μs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100Mbps		0.91		ns

(1) Also known as pulse skew.

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

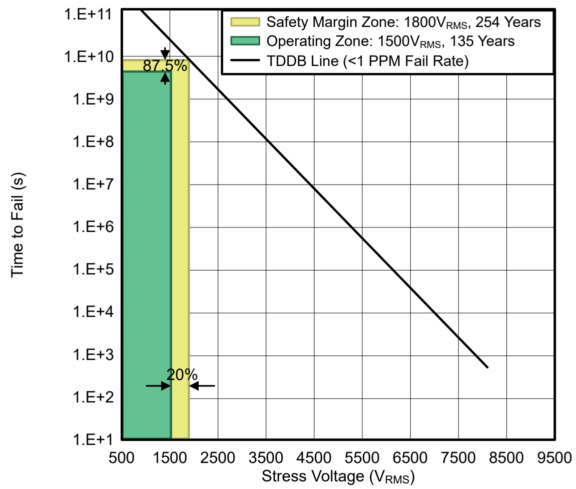
5.17 Switching Characteristics—2.5V Supply

$V_{CC1} = V_{CC2} = 2.5V \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 6-1	7.5	11.7	17.5	ns
PWD	Pulse width distortion[1] $\|t_{PHL} – t_{PLH}\|$			0.66	4.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time[2]	Same-direction Channels			2.2	ns
$t_{sk(pp)}$	Part-to-part skew time[3]				4.5	ns
t_r	Output signal rise time	See Figure 6-1		1	3.5	ns
t_f	Output signal fall time			1.2	3.5	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 6-2		22	45	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			22	45	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7830			18	45	ns
	Enable propagation delay, high impedance-to-high output for ISO7830F			2	2.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7830			2	2.5	μs
	Enable propagation delay, high impedance-to-low output for ISO7830F			18	45	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See Figure 6-3		0.2	9	μs
t_{ie}	Time interval error	$2^{16} – 1$ PRBS data at 100Mbps		0.91		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.18 Insulation Characteristics Curves



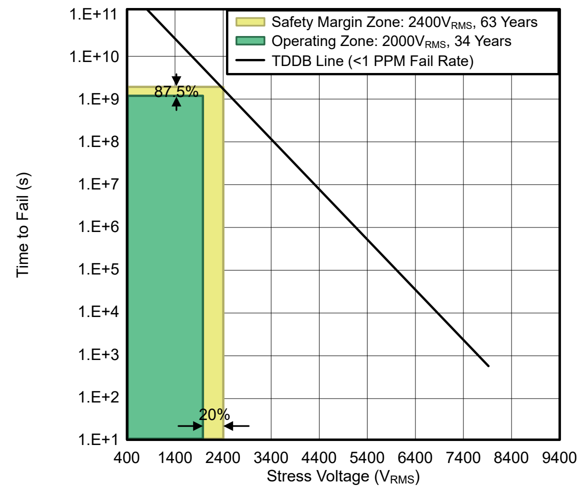
T_A up to 150°C

Operating lifetime = 135 years

Stress-voltage frequency = 60Hz

Isolation working voltage = $1500V_{RMS}$

Figure 5-1. Reinforced Isolation Capacitor Lifetime Projection for Devices in DW Package



T_A up to 150°C

Operating lifetime = 34 years

Stress-voltage frequency = 60Hz

Isolation working voltage = $2000V_{RMS}$

Figure 5-2. Reinforced Isolation Capacitor Lifetime Projection for Devices in DWW Package

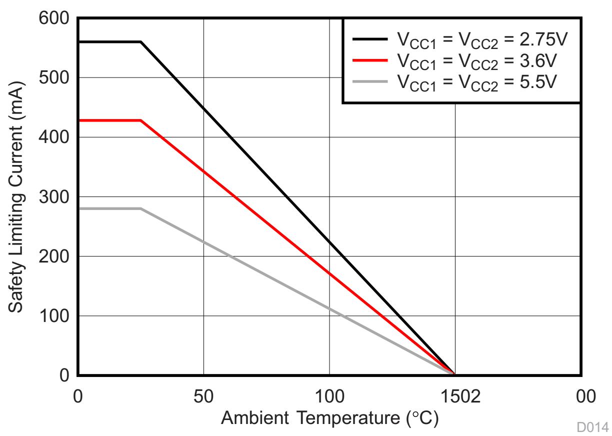


Figure 5-3. Thermal Derating Curve for Safety Limiting Current for DW Package

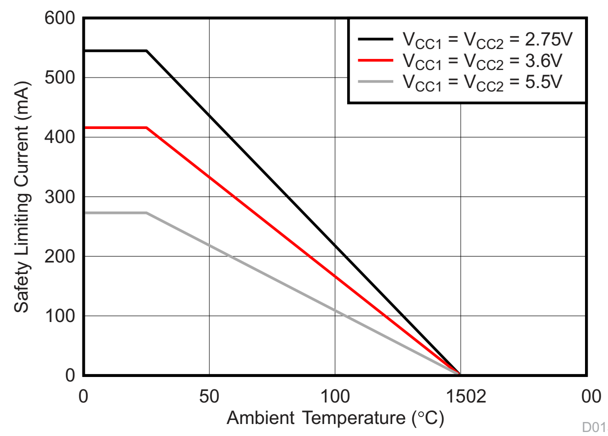


Figure 5-4. Thermal Derating Curve for Safety Limiting Current for DWW Package

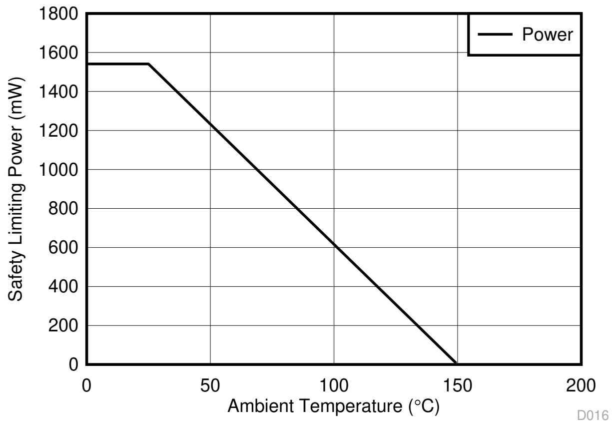


Figure 5-5. Thermal Derating Curve for Safety Limiting Power for DW Package

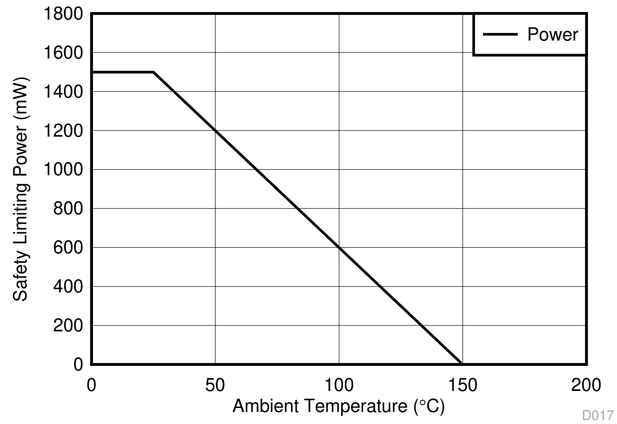
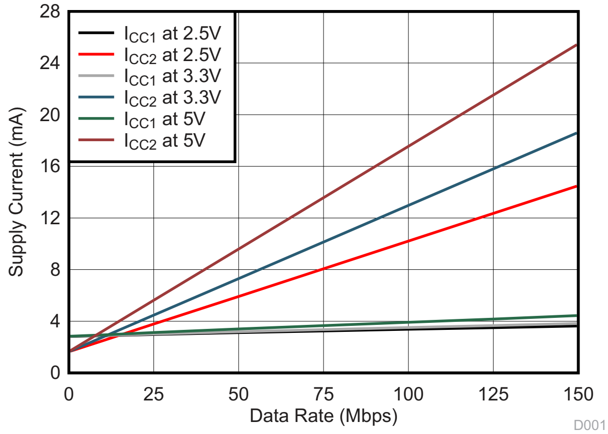


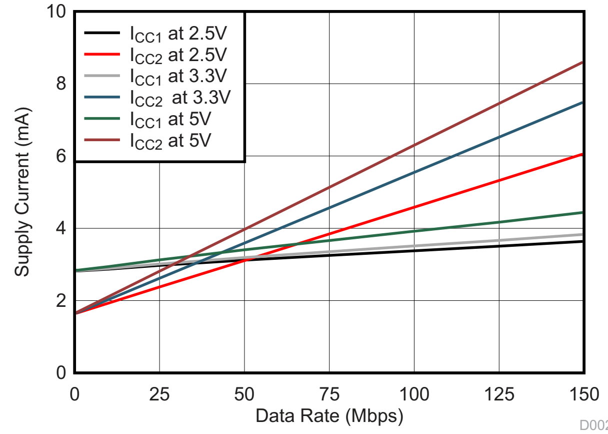
Figure 5-6. Thermal Derating Curve for Safety Limiting Power for DWW Package

5.19 Typical Characteristics



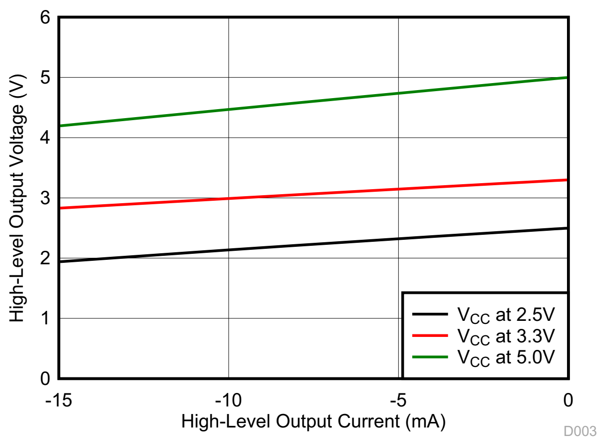
T_A = 25°C C_L = 15pF

Figure 5-7. Supply Current vs Data Rate (With 15pF Load)



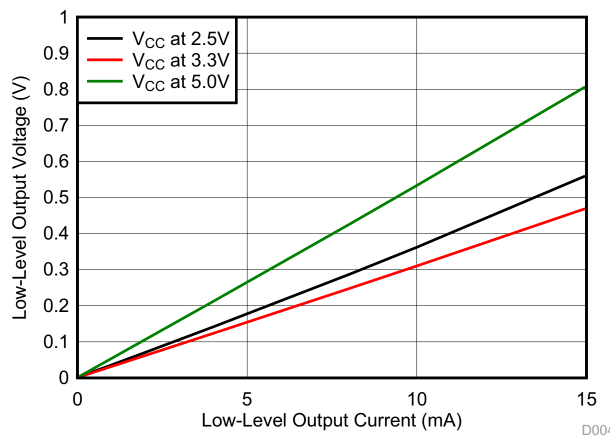
T_A = 25°C C_L = No Load

Figure 5-8. Supply Current vs Data Rate (With No Load)



T_A = 25°C

Figure 5-9. High-Level Output Voltage vs High-level Output Current



T_A = 25°C

Figure 5-10. Low-Level Output Voltage vs Low-Level Output Current

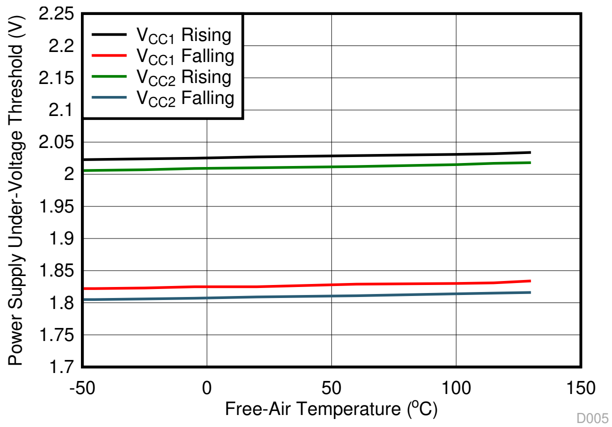


Figure 5-11. Power Supply Undervoltage Threshold vs Free-Air Temperature

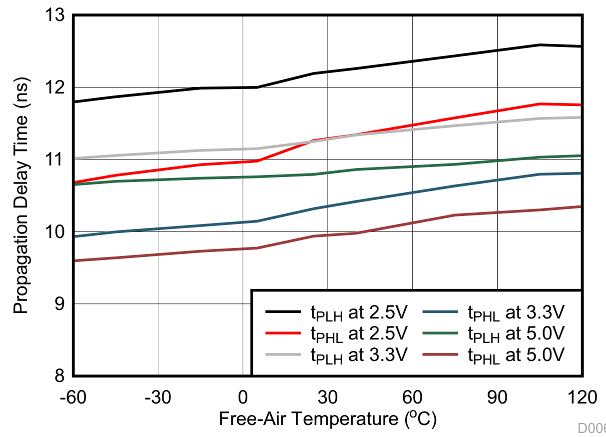
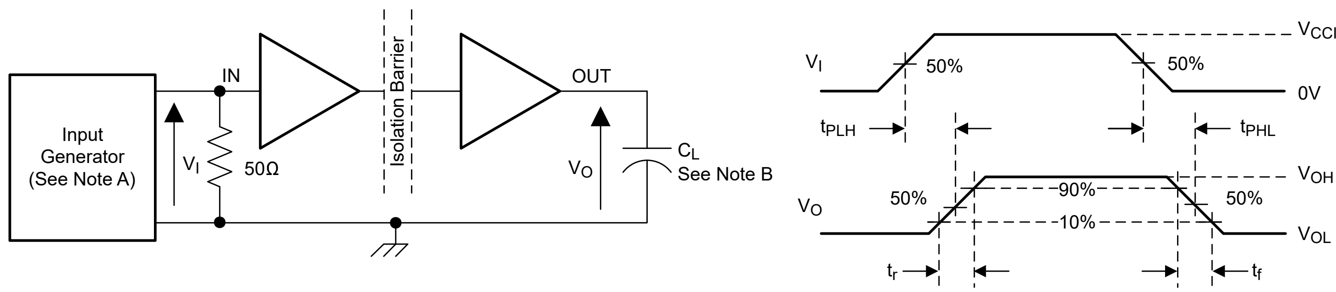


Figure 5-12. Propagation Delay Time vs Free-Air Temperature

6 Parameter Measurement Information

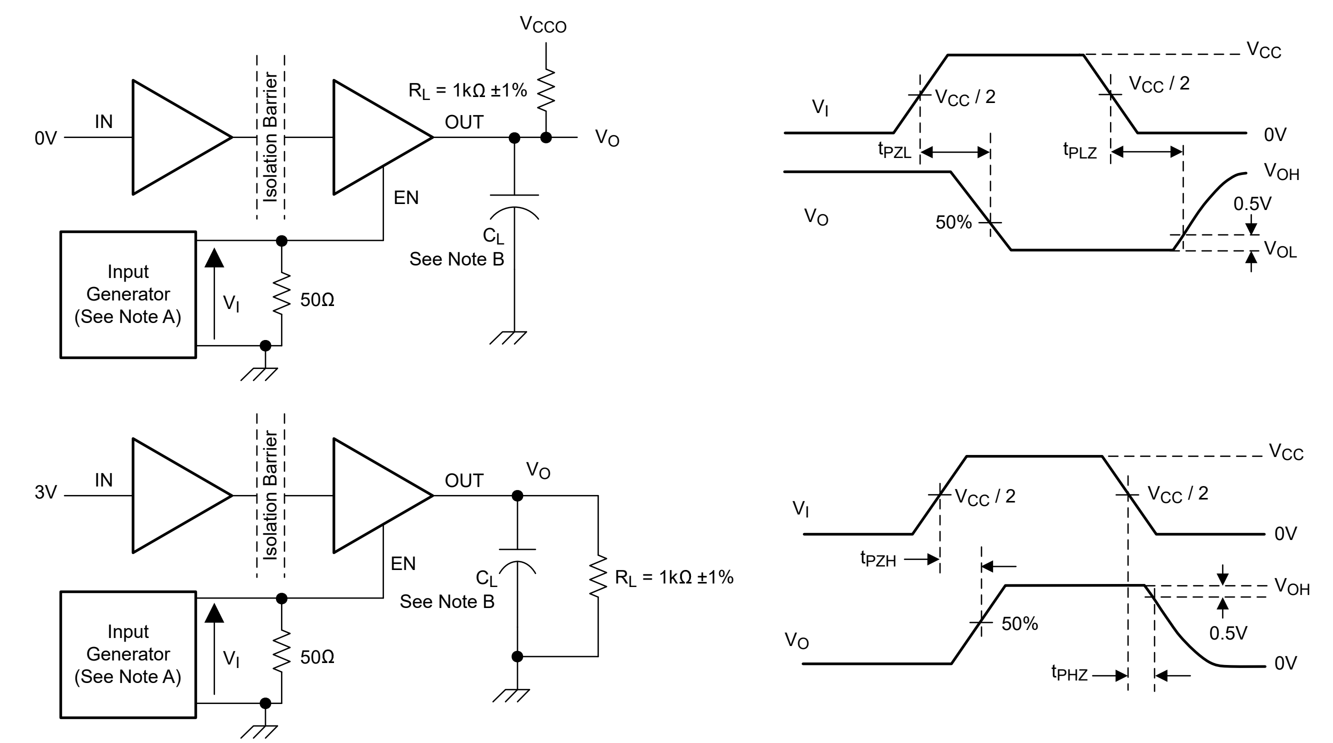
6.1 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω. At the input, 50Ω resistor is required to terminate Input Generator signal. The 50Ω resistor is not needed in actual application.

B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

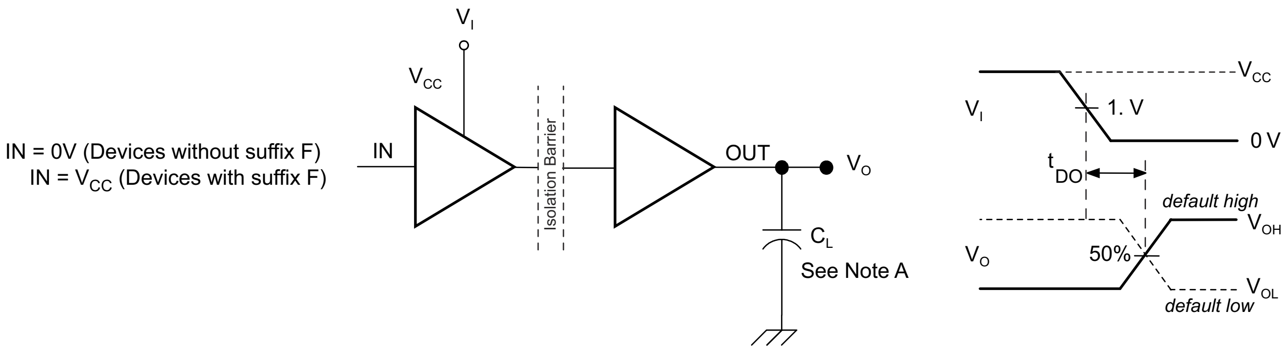
Figure 6-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω.

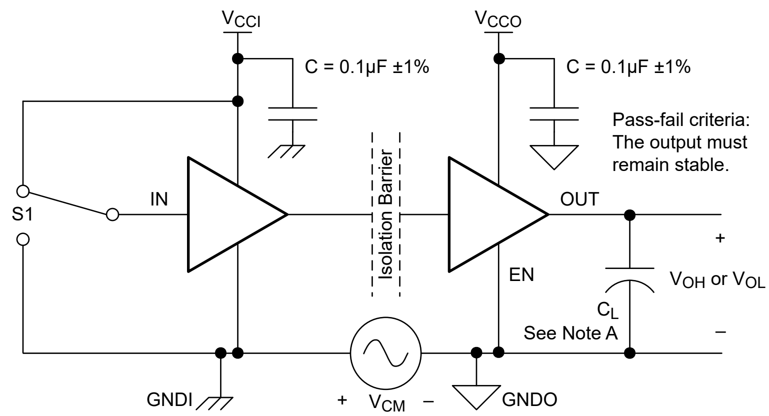
B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-3. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-4. Common-Mode Transient Immunity Test Circuit

7 Detailed Description

7.1 Overview

The ISO7830x device has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the EN pin is low then the output goes to high impedance. The ISO7830x device also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions because of the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 7-1, shows a functional block diagram of a typical channel.

7.2 Functional Block Diagram

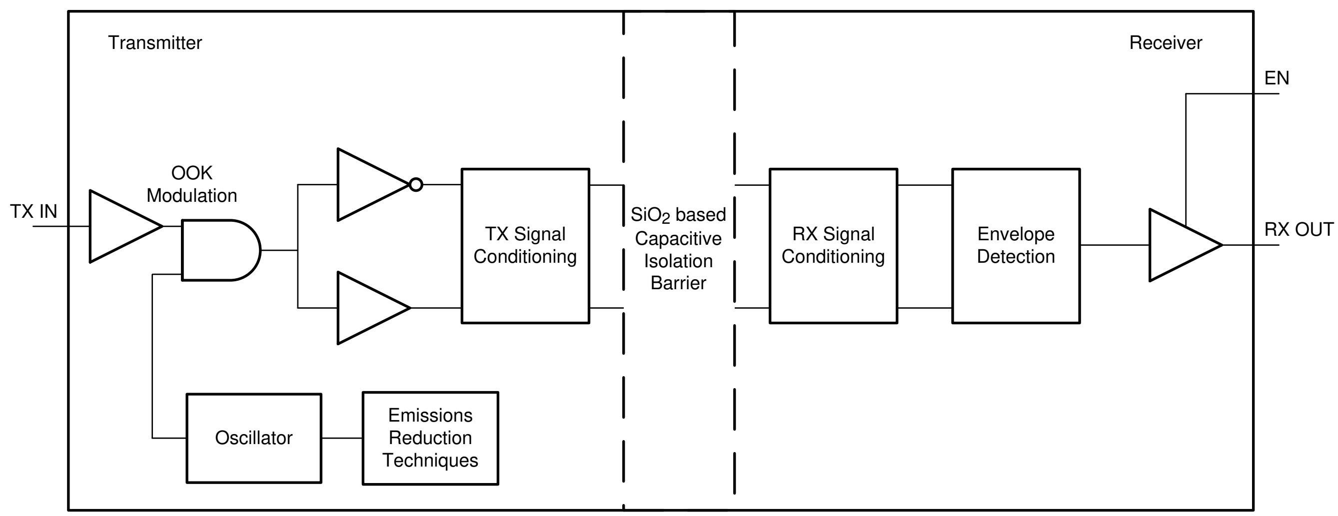


Figure 7-1. Conceptual Block Diagram of a Digital Capacitive Isolator

Figure 7-2 shows a conceptual detail of how the ON-OFF keying scheme works.

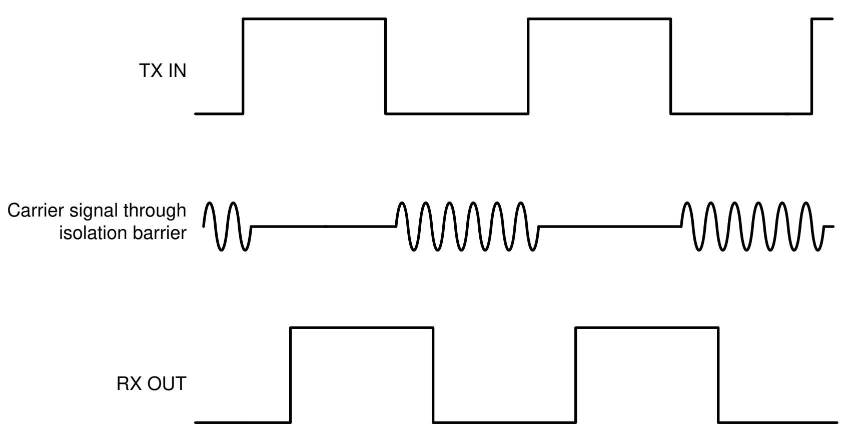


Figure 7-2. On-Off Keying (OOK) Based Modulation Scheme

7.3 Feature Description

Table 7-1 provides an overview of the device features.

Table 7-1. Device Features

PART NUMBER	CHANNEL DIRECTION	RATED ISOLATION	MAXIMUM DATA RATE	DEFAULT OUTPUT
ISO7830	3 Forward, 0 Reverse	$5700V_{RMS}$ / $8000V_{PK}$ (1)	100Mbps	High
ISO7830F	3 Forward, 0 Reverse	$5700V_{RMS}$ / $8000V_{PK}$ (1)	100Mbps	Low

(1) See the *Section 5.7* section for detailed isolation ratings.

7.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7830x device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by providing purely differential internal operation.

7.4 Device Functional Modes

Table 7-2 lists the ISO7830x functional modes.

Table 7-2. Function Table

V_{CCI}	V_{CCO}	INPUT (INx)[2]	OUTPUT ENABLE (EN2)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of the input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to the default logic state. Default is High for ISO7830 and Low for ISO7830F
X	PU	X	L	Z	A low value of output enable causes the outputs to be high-impedance
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is High for ISO7830 and Low for ISO7830F When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output state is undetermined [1]. When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input

(1) The outputs are in undetermined state when 1.7V < V_{CCI}, V_{CCO} < 2.25V.
(2) A strongly driven input signal can weakly power the floating V_{CC} using an internal protection diode and cause undetermined output.

7.4.1 Device I/O Schematics

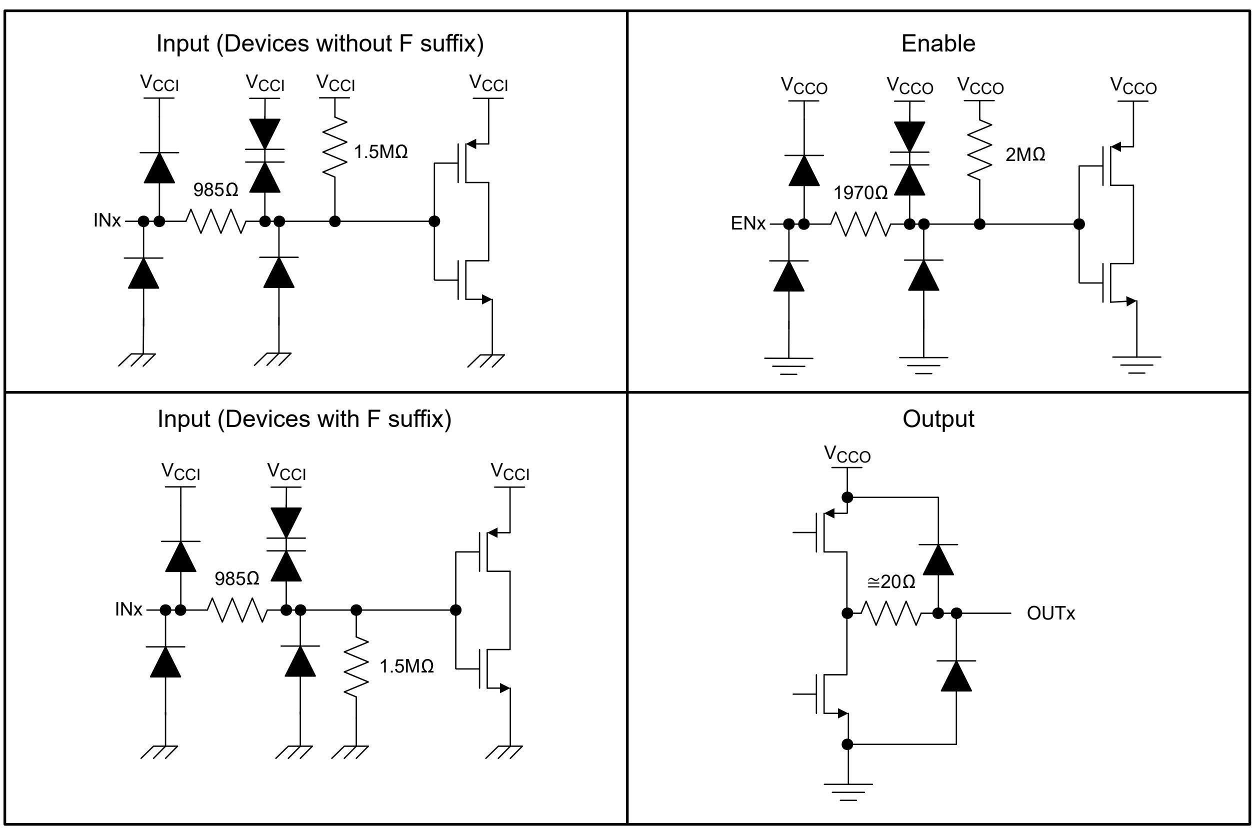


Figure 7-3. Device I/O Schematics

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ISO7830x device is a high-performance, triple-channel digital isolator with 5.7kV$_{RMS}$ isolation voltage. The device comes with enable pin which can be used to put the outputs in high impedance for multi-master driving applications and reduce power consumption. The ISO7830x device uses single-ended CMOS-logic switching technology. The supply voltage range is from 2.25V to 5.5V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

ISO7830F can be used with Texas Instruments' mixed signal micro-controller, gate driver, transformer driver and voltage regulator to create an isolated MOSFET/ IGBT drive circuit. Figure 8-1 shows an implementation of isolated dual channel gate driver

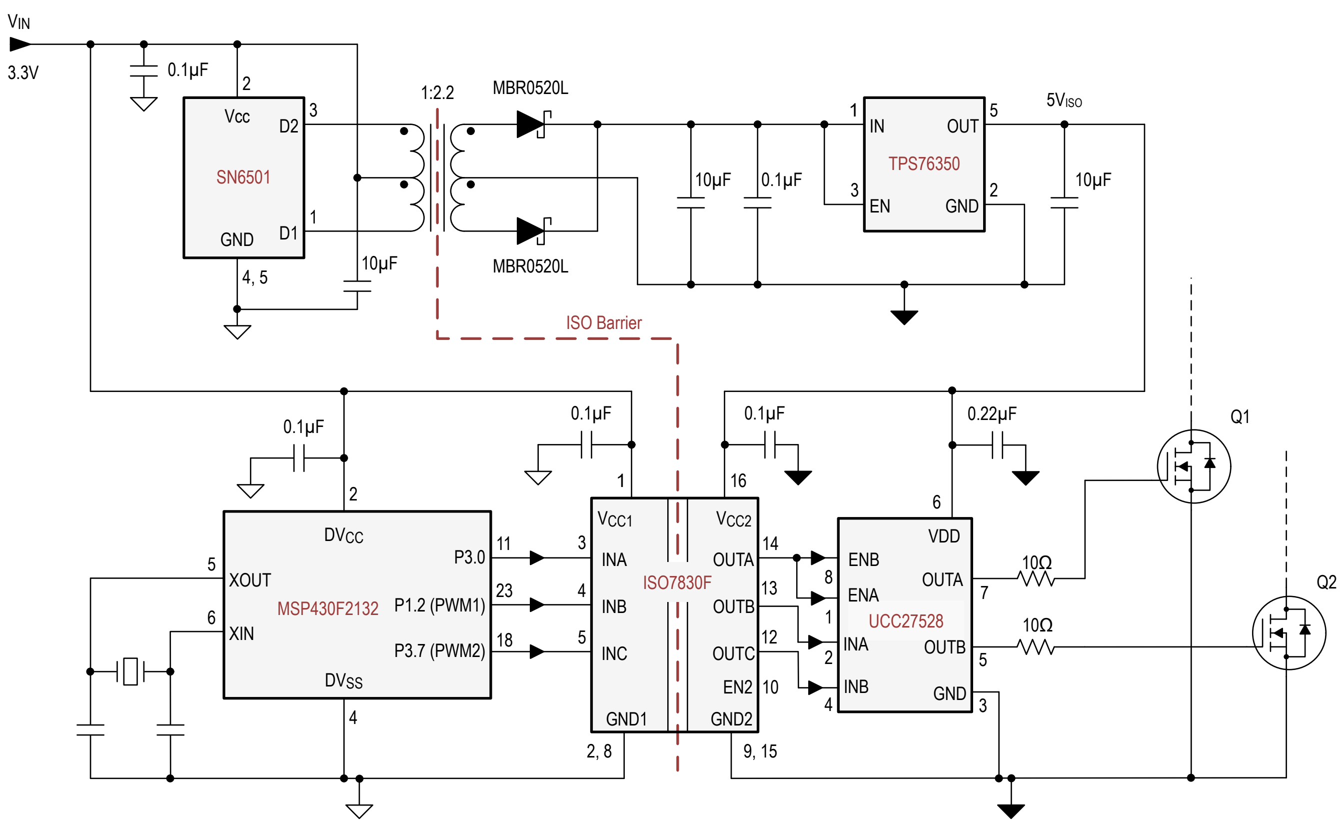


Figure 8-1. Isolated Dual MOSFET / IGBT Gate Drive Circuit

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage	2.25V to 5.5V
Decoupling capacitor between V_{CC1} and GND1	0.1µF
Decoupling capacitor from V_{CC2} and GND2	0.1µF

8.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, ISO7830x only requires two external bypass capacitors to operate.

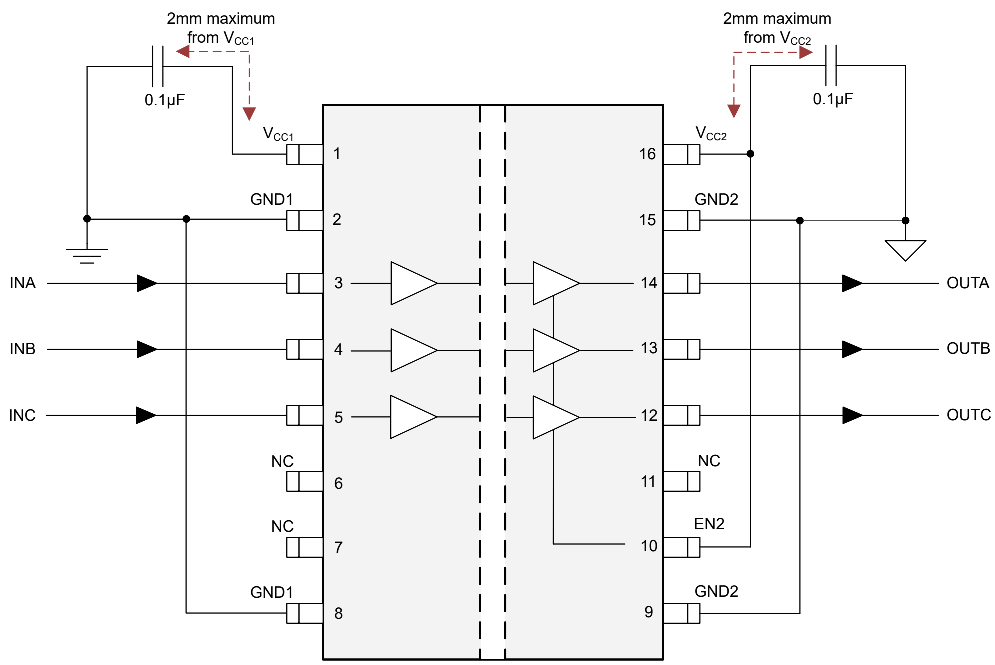


Figure 8-2. Typical ISO7830 Circuit Hook-up

8.2.3 Application Curve

The following typical eye diagram of the ISO7830x device indicates low jitter and wide open eye at the maximum data rate of 100Mbps.

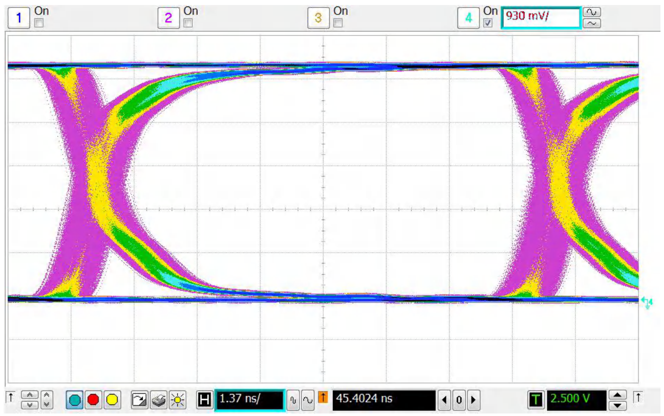


Figure 8-3. Eye Diagram at 100Mbps PRBS, 5V and 25°C

8.3 Power Supply Recommendations

To help provide reliable operation at data rates and supply voltages, a 0.1µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0).

8.4 Layout

8.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 8-4). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see the application note, *Digital Isolator Design Guide* (SLLA284).

8.4.1.1 PCB Material

For digital circuit boards operating at less than 150Mbps (or rise and fall times greater than 1ns) and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

8.4.2 Layout Example

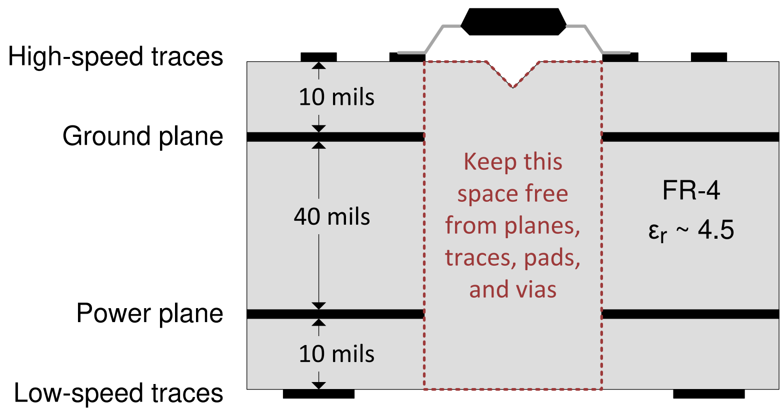


Figure 8-4. Layout Example Schematic

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

1. Texas Instruments, *Digital Isolator Design Guide*, application note
2. Texas Instruments, *Isolation Glossary*, application note
3. Texas Instruments, *SN6501Transformer Driver for Isolated Power Supplies*, data sheet
4. Texas Instruments, UCC27528 Dual 5-A High-Speed Low-Side Gate Driver Based on CMOS Input Threshold LogicCMOS Input Threshold Logic, data sheet
5. Texas Instruments, TPS76350 Low-Power 150-mA Low-Dropout Linear Regulators, data sheet
6. Texas Instruments, MSP430F2132 Mixed Signal Microcontroller, data sheet

9.1.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7830	Click here	Click here	Click here	Click here	Click here
ISO7830F	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2016) to Revision C (July 2025)	Page
• Updated the number format for tables, figures, and cross-references throughout the document	1
• Added 15mm(typ) creepage/clearance to *Insulation Specifications* table	6

Changes from Revision A (September 2015) to Revision B (June 2016)	Page
• Changed *Section 1* From: Low Power Consumption, Typical 2.4mA per Channel at 1Mbps To: Low Power Consumption, Typical 1.6 mA per Channel at 1Mbps	1
• Changed the isolation barrier life from > 25 years to > 40 years in the *Section 1* section	1
• Changed *Section 1* From: Safety and Regulatory Approvals To: Safety-Related Certifications	1
• Updated the status of the certifications throughout the document	1
• Added the extra-wide body package (16 pin SOIC [DWW]) option	1
• Deleted EN1 from the pin out drawing in the *Pin Configuration and Functions* section. Replaced references of ENx with EN2	3
• Changed pin V_{CC1} description From: Power supply, V_{CC1} To: Power supply, side 1 in the *PIN Functions* table	3
• Changed pin V_{CC2} description From: Power supply, V_{CC2} To: Power supply, side 2 in the *PIN Functions* table	3
• Moved Junction temperature From *Section 5.3* To *Section 5.1*	4
• Changed the values for the DW package in the *Thermal Information* table	5
• Changed the maximum power dissipation values for side 1 (40 to 25) and side 2 (110 to 125) in the *Power Rating* table	5
• Moved *Insulation Characteristics* to the *Specifications* section	6
• Changed C_{IO} Specification From: 2pF To: ≅1 pF	6
• Added the climatic category parameter to the *Insulation Characteristics* table	6
• Moved *Section 5.7* to the *Section 5* section	7
• Moved *Section 5.8* to the *Section 5* section	7
• Changed the test conditions and values for the DW package in the *Safety Limiting Values* table	7
• Changed V_{CCO} to V_{CCI} in the minimum value for the input threshold voltage hysteresis parameter in the electrical characteristics tables	8
• Added the V_{CM} test condition to the CMTI parameter in the electrical characteristics tables. Also updated the minimum value from 70 to 100 and deleted the maximum value of 100	8
• Changed t_{fs} To: t_{DO} in *Section 5.15*	11
• Changed t_{fs} To: t_{DO} in *Section 5.16*	11
• Changed t_{fs} To: t_{DO} in *Section 5.17*	12
• Added the lifetime projection graphs for DW and DWW packages to the *Insulation Characteristics Curves* section	13
• Changed the thermal derating curves in the *Safety Limiting Values* section	13
• Changed 2.7V To: 1.7V, fs high To: default high, and fs low To: default low in Figure 6-3	17
• Changed Figure 8-1	22

Changes from Revision * (July 2015) to Revision A (September 2015)	Page
• Changed From: 1-page Product Preview To: Production data sheet	1

11 Mechanical, Packaging, and Orderable Information

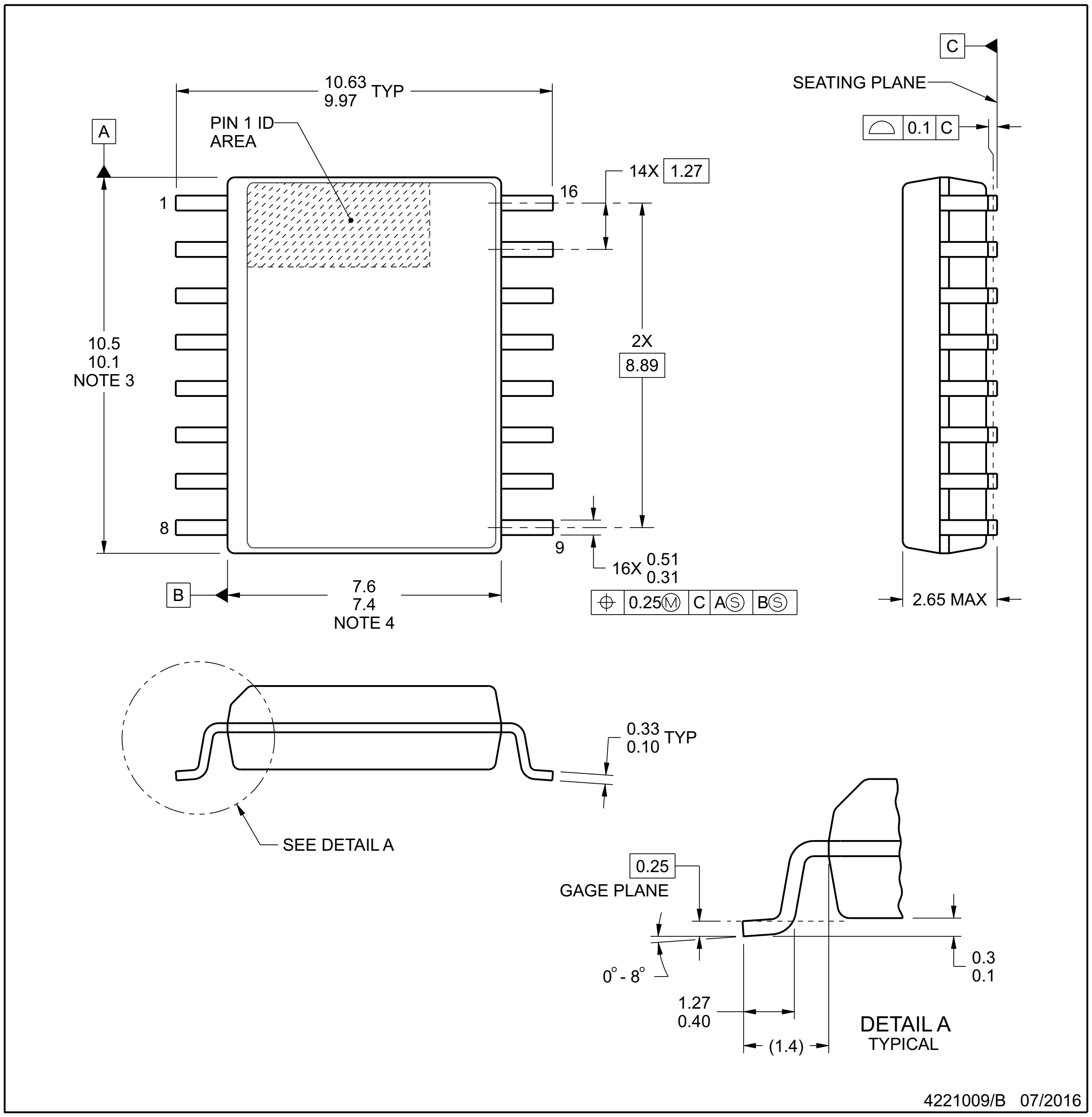
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



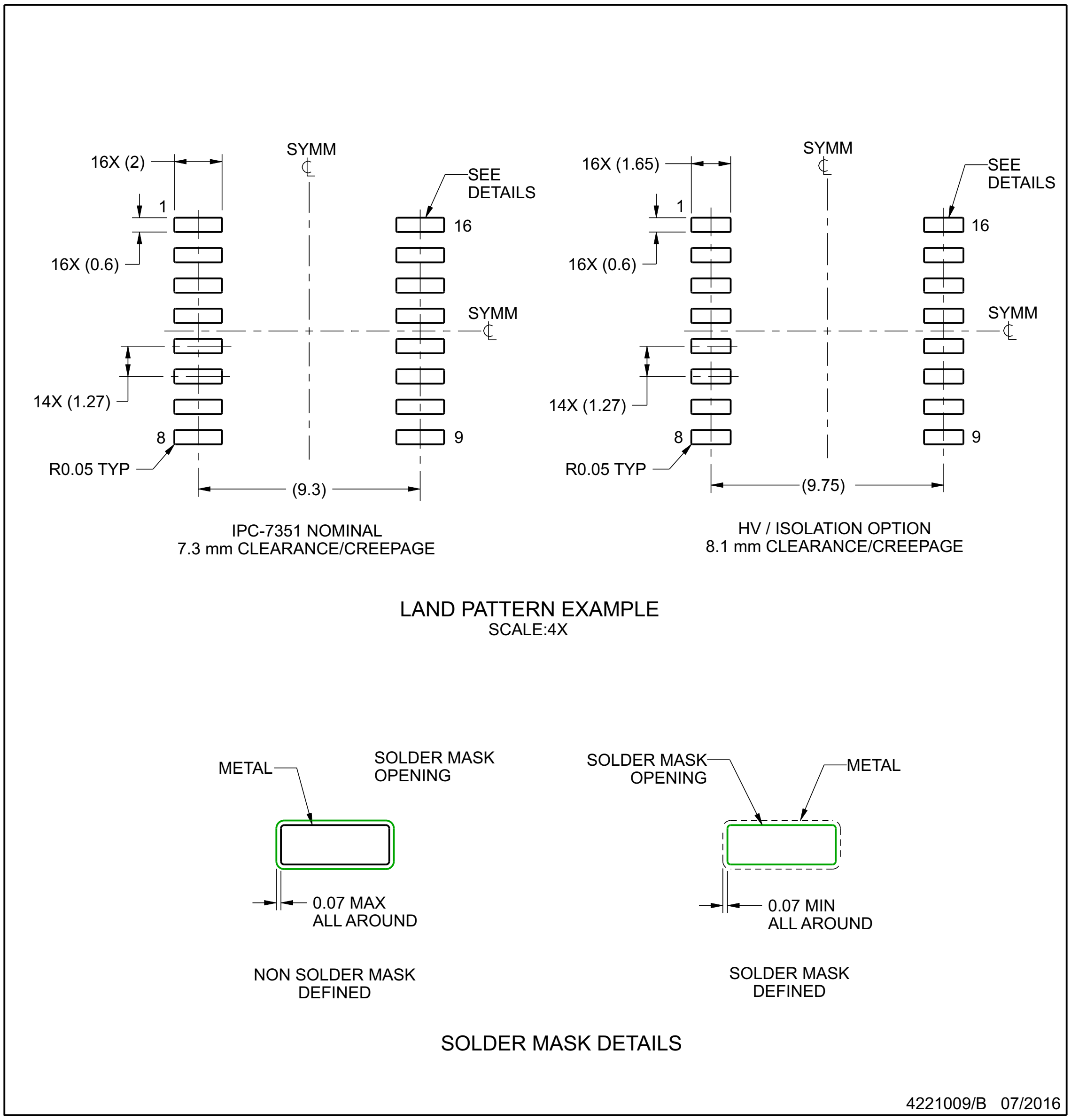
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016B SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

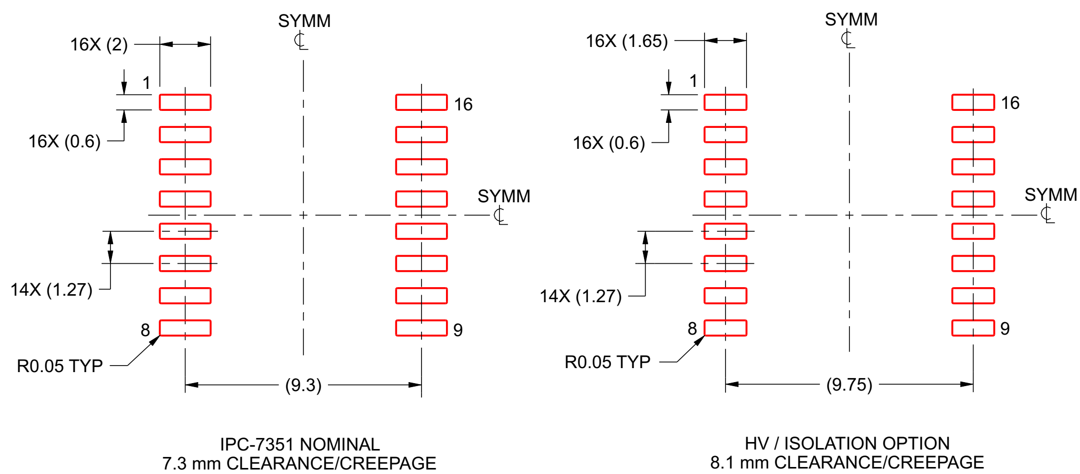
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

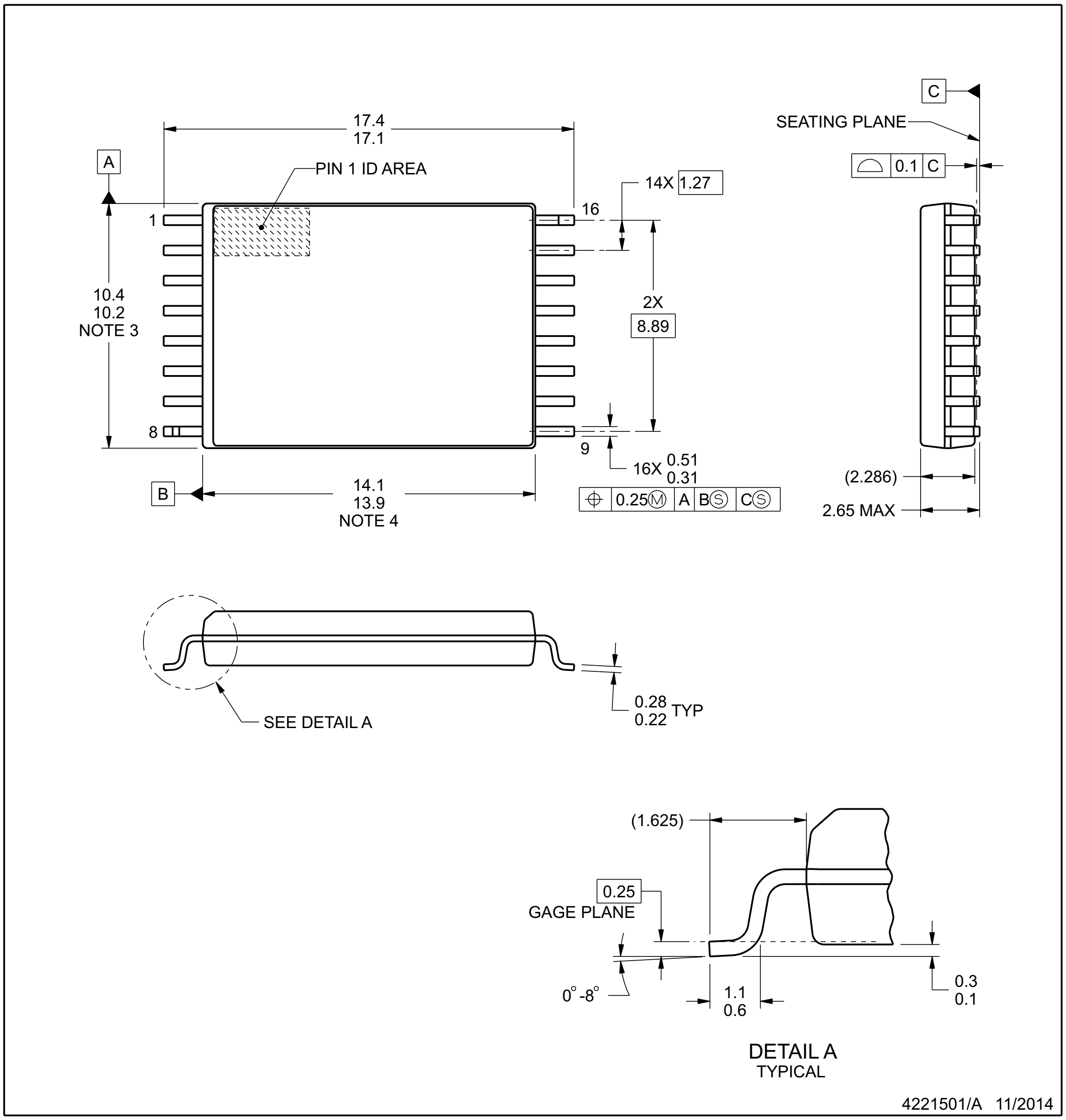
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DWW0016A

SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE



NOTES:

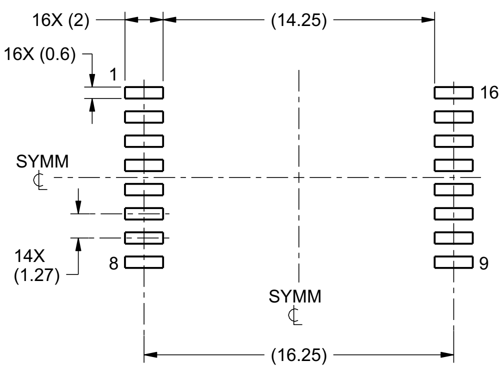
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

EXAMPLE BOARD LAYOUT

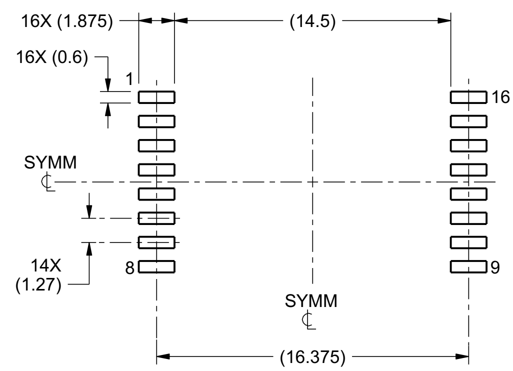
DWW0016A

SOIC - 2.65 mm max height

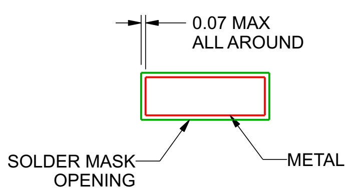
PLASTIC SMALL OUTLINE



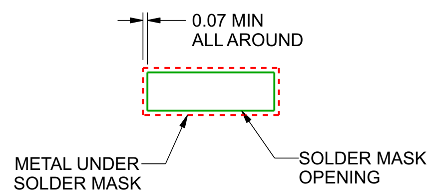
LAND PATTERN EXAMPLE
STANDARD
SCALE:3X



LAND PATTERN EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
SCALE:3X



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221501/A 11/2014

NOTES: (continued)

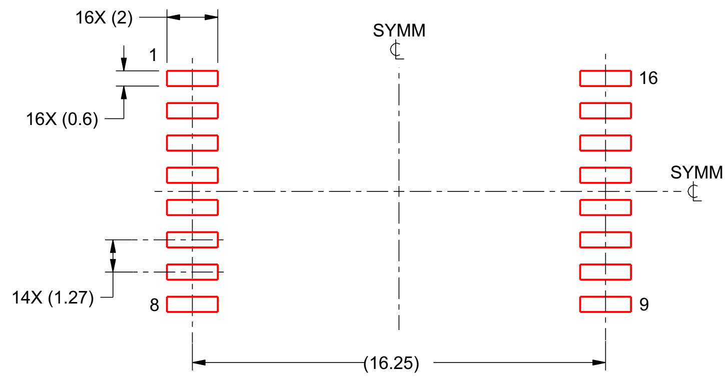
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

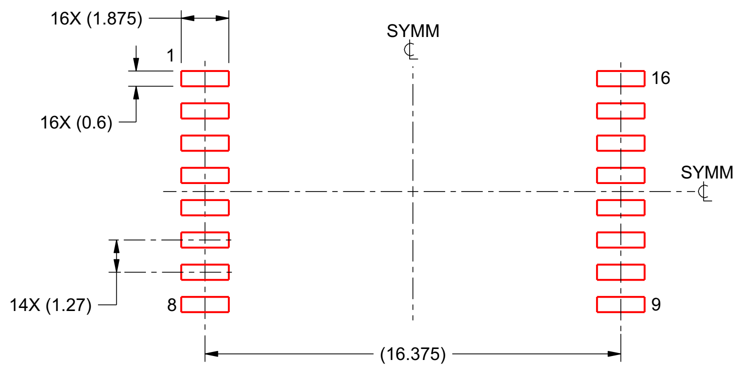
DWW0016A

SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
STANDARD
BASED ON 0.125 mm THICK STENCIL
SCALE:4X



SOLDER PASTE EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221501/A 11/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7830DW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830
ISO7830DW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830
ISO7830DW.B	Active	Production	SOIC (DW) | 16	40 | TUBE	-	Call TI	Call TI	-55 to 125	
ISO7830DWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830
ISO7830DWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830
ISO7830DWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7830DWW	Active	Production	SOIC (DWW) | 16	45 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830
ISO7830DWW.A	Active	Production	SOIC (DWW) | 16	45 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830
ISO7830DWW.B	Active	Production	SOIC (DWW) | 16	45 | TUBE	-	Call TI	Call TI	-55 to 125	
ISO7830DWWR	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830
ISO7830DWWR.A	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830
ISO7830DWWR.B	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7830FDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830F
ISO7830FDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830F
ISO7830FDW.B	Active	Production	SOIC (DW) | 16	40 | TUBE	-	Call TI	Call TI	-55 to 125	
ISO7830FDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830F
ISO7830FDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830F
ISO7830FDWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7830FDWW	Active	Production	SOIC (DWW) | 16	45 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830F
ISO7830FDWW.A	Active	Production	SOIC (DWW) | 16	45 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830F
ISO7830FDWW.B	Active	Production	SOIC (DWW) | 16	45 | TUBE	-	Call TI	Call TI	-55 to 125	
ISO7830FDWWR	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830F
ISO7830FDWWR.A	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830F
ISO7830FDWWR.B	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	-	Call TI	Call TI	-55 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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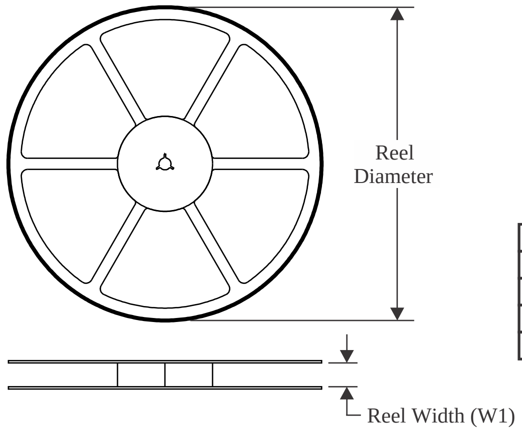
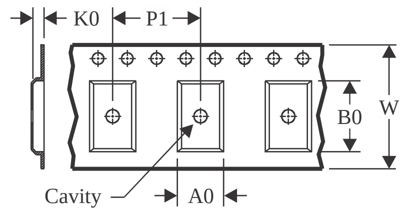
TAPE AND REEL INFORMATION

REEL DIMENSIONS

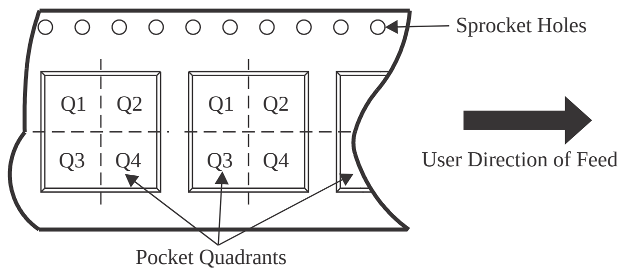


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

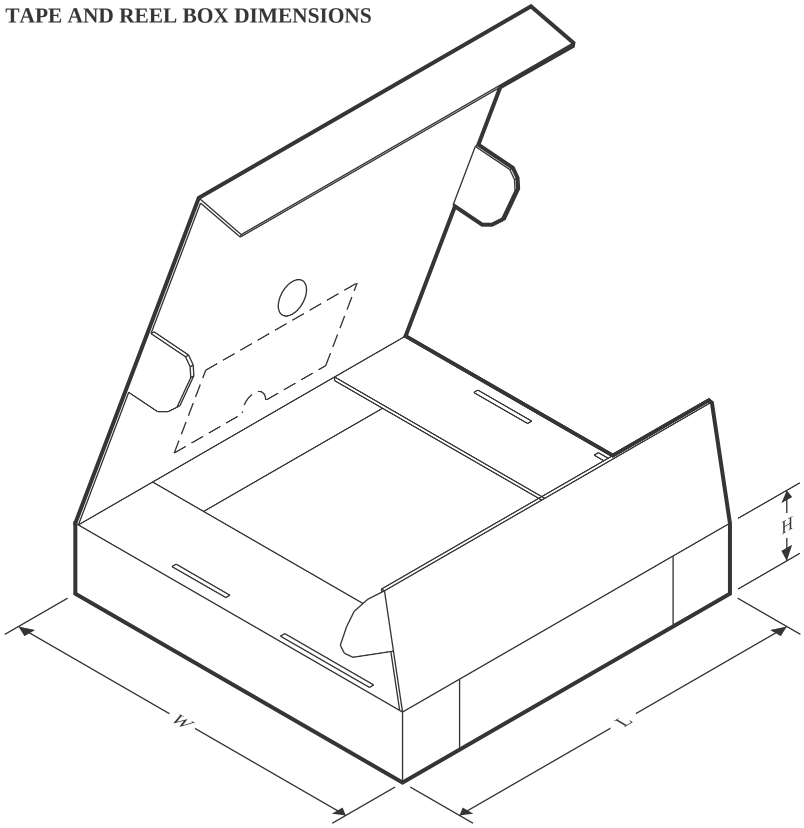
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7830DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7830DWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1
ISO7830FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7830FDWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1

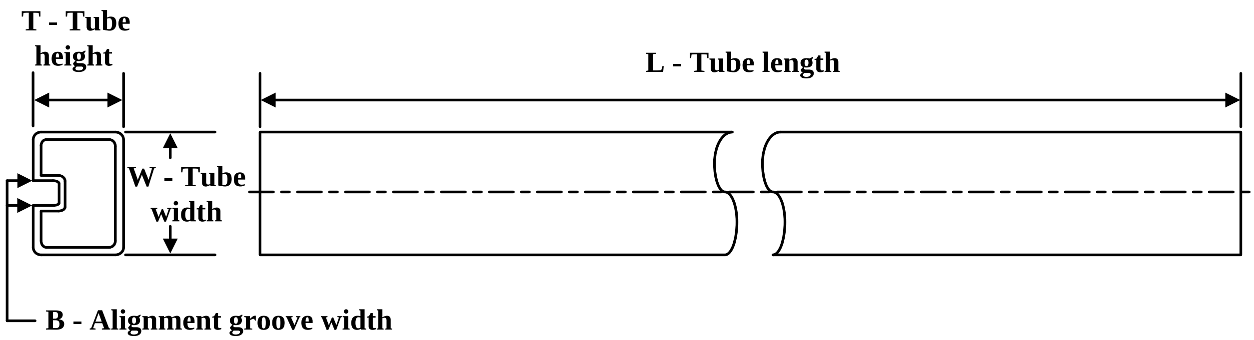
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7830DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7830DWWR	SOIC	DWW	16	1000	350.0	350.0	43.0
ISO7830FDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7830FDWWR	SOIC	DWW	16	1000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7830DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7830DW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7830DWW	DWW	SOIC	16	45	507	20	5000	9
ISO7830DWW.A	DWW	SOIC	16	45	507	20	5000	9
ISO7830FDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7830FDW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7830FDWW	DWW	SOIC	16	45	507	20	5000	9
ISO7830FDWW.A	DWW	SOIC	16	45	507	20	5000	9