低消費電力デュアル・デジタル・アイソレータ

1 特長

- **車載アプリケーションに対応**
- **次の結果で AEC-Q100 認定済み**
  - デバイス温度グレード 1:動作時周囲温度範囲 -40°C～+125°C
  - デバイス HBM ESD 分類レベル H3A
  - デバイス CDM ESD 分類レベル C4
- **伝搬遅延時間：20ns 未満**
- **低消費電力**
- **安全および規制当局の承認**
  - VDE 準拠で 4242V_{PK} の絶縁、UL 1577 準拠で 2.5kVrms の絶縁、IEC 60950-1 および IEC 61010-1 最終機器標準に従い CSA 認定済み
- **50kV/μs (標準値) の過渡耐性**
- **3.3V～5V の電源およびロジック・レベルで動作**

2 アプリケーション

- **次の分野におけるフォトカプラの代替**
  - サーボ制御インターフェイス
  - モータ制御
  - 電源
  - バッテリ・パック

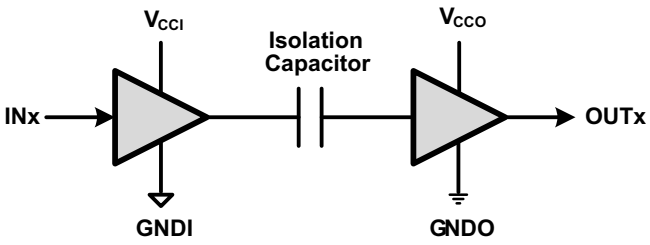
3 概要

ISO7421E-Q1 は、UL 準拠で最大 2.5KVrms、1 分間の二重ガルバニック絶縁を提供します。このデジタル・アイソレータは双方向構成の 2 つの絶縁チャネルを備えています。それぞれの絶縁チャネルにはロジック入力および出力バッファがあり、二酸化ケイ素 (SiO_2) の絶縁バリアによって分離されています。これらのデバイスを絶縁型電源と組み合わせて使用すると、データ・バスや他の回路上のノイズ電流がローカル・グランドに入り込んでノイズに敏感な回路に干渉または損傷を与えることを防止できます。

これらのデバイスは TTL 入力スレッショルドを使用し、3.3V または 5V、または任意の組み合わせの 2 つの電源電圧を必要とします。3.3V 電源を供給するとき、すべての入力は 5V 許容です。

注:ISO7421E-Q1 は、最大 50Mbps の信号速度で動作が規定されています。これらのデバイスは応答時間が短いため、ほとんどの場合、非常に短いパルス幅でデータを送信できます。入力パルス幅が 20ns 未満の場合は、スプリアス信号を除去するために、必要に応じて外部フィルタ処理を設計に追加してください。

概略回路図

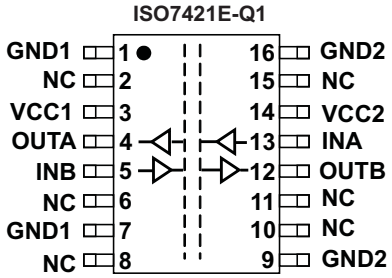


(1) V_{CCI}および GNDI は、それぞれ入力チャネルの電源およびグランド接続です。

(2) V_{CCO}および GNDO は、それぞれ出力チャネルの電源およびグランド接続です。

4 Pin Configuration and Functions

16-Pin SSOP
Top View



NC = No Internal Connection

Table 1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	ISO7421E-Q1		
INA	13	I	Input, channel A
INB	5	–	Input, channel B
GND1	1, 7	–	Ground connection for V_{CC1}
GND2	9, 16	O	Ground connection for V_{CC2}
OUTA	4	O	Output, channel A
OUTB	12	–	Output, channel B
V_{CC1}	14	–	Power supply, V_{CC1}
V_{CC2}	14	-	Power supply, V_{CC2}
NC	2, 6, 8, 10, 11, 15		No Connect Pin

4.1 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

4.1 Device Function Table

INPUT SIDE V_{CC} (V_{CCI})(1)	OUTPUT SIDE V_{CC} (V_{CCO})(1)	INPUT (IN)(1)	OUTPUT (OUT)(1)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

(1) PU = Powered Up (V_{CC} ≥ 3.15V); PD = Powered Down (V_{CC} ≤ 2.4V); X = Irrelevant; H = High Level; L = Low Level

4.2 Available Options

PRODUCT	RATED T_A	MARKED AS	ORDERING NUMBER
ISO7421E-Q1	–40°C to 125°C	ISO7421EQ	ISO7421EQDWRQ1

5 Absolute Maximum Ratings(1)

					VALUE		UNIT
					MIN	MAX	
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}				–0.5	6	V
V_I	Voltage at IN, OUT				–0.5	V_{CC} + 0.5(3)	V
I_O	Output Current					±15	mA
ESD	Electrostatic discharge	Human Body Model	AEC-Q100 Classification Level H3A	All pins		4	kV
		Charged Device Model	AEC-Q100 Classification Level C4			1	kV
T_J	Maximum junction temperature					150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings(1) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.
(3) Maximum voltage must not exceed 6 V. A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.

6 Thermal Information

THERMAL METRIC(1)		ISO7421E-Q1 DW (16 Pins)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	79.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	44.6	
θ_{JB}	Junction-to-board thermal resistance	51.2	
ψ_{JT}	Junction-to-top characterization parameter	18.0	
ψ_{JB}	Junction-to-board characterization parameter	42.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	
P_D	Device power dissipation, Vcc1 = Vcc2 = 5.25 V, T_J = 150°C, C_L = 15 pF, Input a 0.5 MHz 50% duty cycle square wave	42	mW

(1) 従来および新しい熱測定値の詳細については、『*Semiconductor and IC Package Thermal Metrics*』アプリケーション・レポート (SPRA953)を参照してください。

7 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage - 3.3V Operation	3.15	3.3	3.45	V
	Supply voltage - 5V Operation	4.75	5	5.25	
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level output voltage	2		V_{CC}	V
V_{IL}	Low-level output voltage	0		0.8	V
T_A	Ambient Temperature	-40		125	°C
T_J (1)	Junction temperature	–40		136	°C
$1/t_{ui}$	Signaling rate	0		50	Mbps
t_{ui}	Input pulse duration	1			µs

(1) To maintain the recommended operating conditions for T_J, see the *Package Thermal Characteristics* table and the *Icc Equations* section of this data sheet

8 Electrical Characteristics

V_{CC1} and V_{CC2} at 5 V ± 5%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; See 図 1		V_{CC} –0.8	4.6		V
		I_{OH} = –20 µA; See 図 1		V_{CC} –0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See 図 1			0.2	0.4	V
		I_{OL} = 20 µA; See 図 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; See 図 3		25	50		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V		2.3	3.6	mA
I_{CC2}			AC Input: C_L = 15 pF		2.3	3.6	
I_{CC1}		10 Mbps	C_L = 15 pF		2.9	4.5	
I_{CC2}					2.9	4.5	
I_{CC1}		25 Mbps			4.3	6	
I_{CC2}					4.3	6	
I_{CC1}		50 Mbps			6	9.1	
I_{CC2}					6	9.1	

9 Switching Characteristics

V_{CC1} and V_{CC2} at 5 V ± 5%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 1		9	14	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.3	3.7	ns
$t_{sk(pp)}$	Part-to-part skew time				4.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time				3.6	ns
t_r	Output signal rise time	See 図 1		1		ns
t_f	Output signal fall time			1		ns
t_{fs}	Fail-safe output delay time from input power loss	See 図 2		6		µs

(1) Also known as pulse skew.

10 Electrical Characteristics

V_{CC1} at 5 V ± 5%, V_{CC2} at 3.3 V ± 5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; See 図 1	5-V side	V_{CC} –0.8	4.6		V
			3.3-V side	V_{CC} –0.4	3		
		I_{OH} = –20 µA; See 図 1		V_{CC} –0.1	V_{CC}		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See 図 1			0.2	0.4	V
		I_{OL} = 20 µA; See 図 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; See 図 3		25	40		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V		2.3	3.6	mA
I_{CC2}			AC Input: C_L = 15 pF		1.8	2.8	
I_{CC1}		10 Mbps	C_L = 15 pF		2.9	4.5	
I_{CC2}					2.2	3.2	
I_{CC1}		25 Mbps			4.3	6	
I_{CC2}					2.8	4.1	
I_{CC1}		50 Mbps			6	9.1	
I_{CC2}					3.8	5.8	

11 Switching Characteristics

V_{CC1} at 5 V ± 5%, V_{CC2} at 3.3 V ± 5%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 1		10	17	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	5.6	ns
$t_{sk(pp)}$	Part-to-part skew time				6.3	ns
$t_{sk(o)}$	Channel-to-channel output skew time				4	ns
t_r	Output signal rise time	See 図 1		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See 図 2		6		µs

(1) Also known as pulse skew.

12 Electrical Characteristics

V_{CC1} at 3.3 V ± 5%, V_{CC2} at 5 V ± 5%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; See 図 1	5-V side	V_{CC} –0.8	4.6		V
			3.3-V side	V_{CC} –0.4	3		
		I_{OH} = –20 µA; See 図 1		V_{CC} –0.1	V_{CC}		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See 図 1			0.2	0.4	V
		I_{OL} = 20 µA; See 図 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; See 図 3		25	40		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V		1.8	2.8	mA
I_{CC2}			AC Input: C_L = 15 pF		2.3	3.6	
I_{CC1}		10 Mbps	C_L = 15 pF		2.2	3.2	
I_{CC2}					2.9	4.5	
I_{CC1}		25 Mbps			2.8	4.1	
I_{CC2}					4.3	6	
I_{CC1}		50 Mbps			3.8	5.8	
I_{CC2}					6	9.1	

13 Switching Characteristics

V_{CC1} at 3.3 V ± 5%, V_{CC2} at 5 V ± 5%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 1		10	17	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	4	ns
$t_{sk(pp)}$	Part-to-part skew time				8.5	ns
$t_{sk(o)}$	Channel-to-channel output skew time				4	ns
t_r	Output signal rise time	See 図 1		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See 図 2		6		µs

(1) Also known as pulse skew.

14 Electrical Characteristics

V_{CC1} and V_{CC2} at 3.3 V ± 5%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; See 図 1		V_{CC} –0.4	3		V
		I_{OH} = –20 µA; See 図 1		V_{CC} –0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See 図 1			0.2	0.4	V
		I_{OL} = 20 µA; See 図 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}					µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; See 図 3		25	40		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V		1.8	2.8	mA
I_{CC2}			AC Input: C_L = 15 pF		1.8	2.8	
I_{CC1}		10 Mbps	C_L = 15 pF		2.2	3.2	
I_{CC2}					2.2	3.2	
I_{CC1}		25 Mbps			2.8	4.1	
I_{CC2}					2.8	4.1	
I_{CC1}		50 Mbps			3.8	5.8	
I_{CC2}					3.8	5.8	

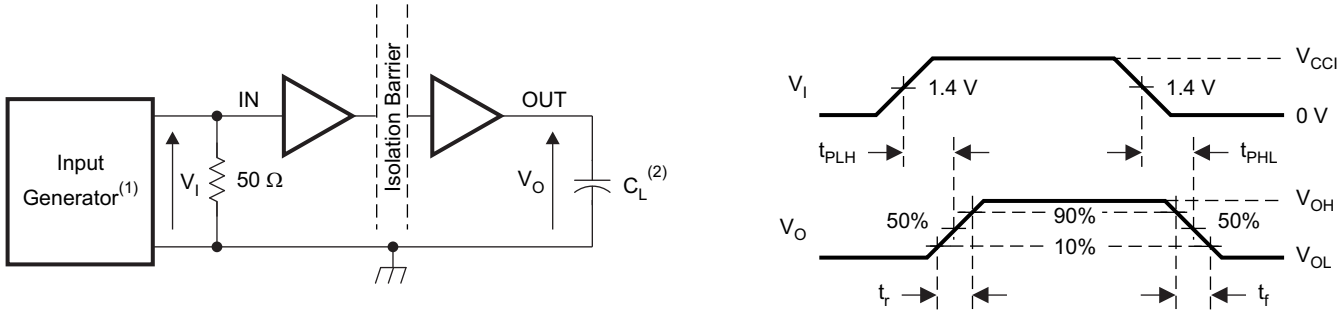
15 Switching Characteristics

V_{CC1} and V_{CC2} at 3.3 V ± 5%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 1		12	20	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			1	5	ns
$t_{sk(pp)}$	Part-to-part skew time				6.8	ns
$t_{sk(o)}$	Channel-to-channel output skew time				5.5	ns
t_r	Output signal rise time	See 図 1		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See 図 2		6		µs

(1) Also known as pulse skew.

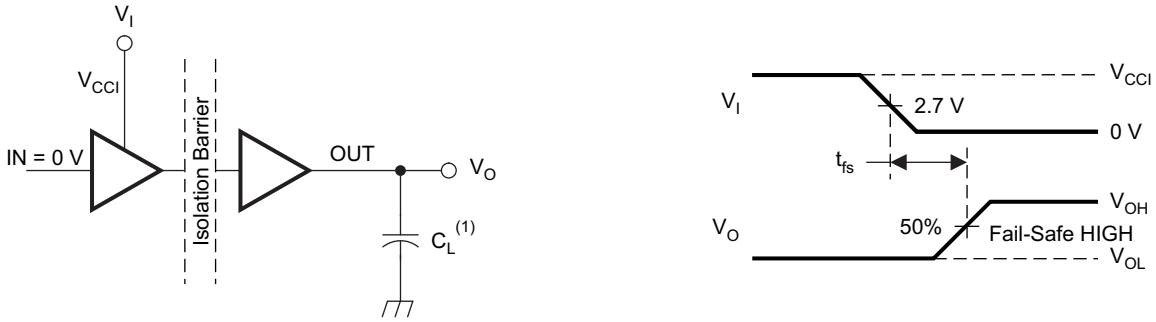
16 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω.

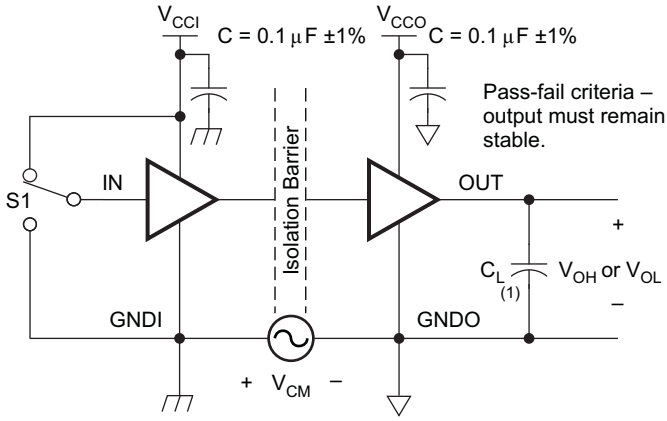
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 1. Switching Characteristic Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 2. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 3. Common-Mode Transient Immunity Test Circuit

17 Device Information

17.1 Package Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air	7.6			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface	7.6			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN EN 60112 (VDE 0303-11)	≥400			V
	Minimum internal gap (Internal Clearance)	Distance through the insulation	0.014			mm
R_{IO}	Isolation resistance, input to output(1)	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device		$>10^{12}$		Ω
C_{IO}	Barrier capacitance input to output(1)	V_{IO} = 0.4 sin(2πft), f = 1 MHz		2		pF
C_I	Input capacitance to ground(2)	$V_I = V_{CC}/2$ + 0.4 sin(2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

注

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance

Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

17.2 IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic Isolation Group	Material Group	II
Installation Classification	Rated mains voltages <= 150 Vrms	I - IV
	Rated mains voltages <= 300 Vrms	I - IV
	Rated mains voltages <= 400 Vrms	I - III

17.3 Insulation Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		1414	Vpeak
V_{PR}	Input to output test voltage	Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM}$ x 1.6, t = 10 s, Partial discharge < 5 pC	2262	Vpeak
		After Input/Output Safety Test Subgroup 2/3, $V_{PR} = V_{IORM}$ x 1.2, t = 10 s, Partial discharge < 5 pC	1697	
		Method b1, $V_{PR} = V_{IORM}$ x 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC	2651	
V_{IOTM}	Transient overvoltage	t = 60 sec (qualification)	4242	Vpeak
V_{ISO}	Isolation voltage per UL	$V_{TEST} = V_{ISO}$, t = 60 sec (qualification)	2500	Vrms
		V_{TEST} = 1.2 x V_{ISO}, t = 1 sec (100% production)	3000	
R_S	Insulation resistance	V_{TEST} = 500 V at T_S = 150°C	$>10^9$	Ω
	Pollution degree		2	

17.4 Regulatory Information

VDE	CSA	UL
Certified according to DIN VDE V 0884-11:2017-01	Approved according to IEC 60950-1 and IEC 61010-1	Recognized under UL 1577 Component Recognition Program
Certificate Number: 40047657	Master Contract Number: 220991	File Number: E181974

17.5 IEC Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Is	Safety input, output, or supply current	θ_{JA} =212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			112	mA
		θ_{JA} =212°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C			171	
Ts	Maximum Case Temperature				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

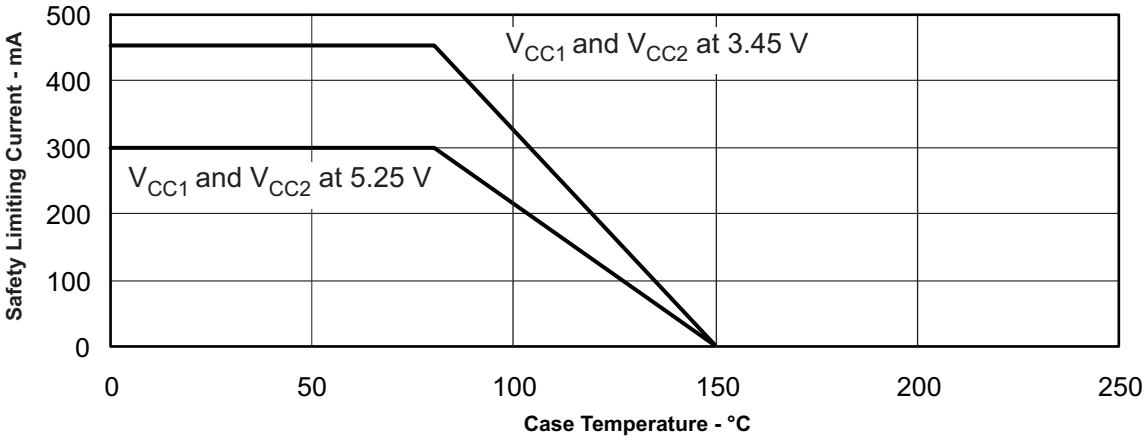


図 4. DW-16 Theta-JC Thermal Derating Curve per IEC 60747-5-2

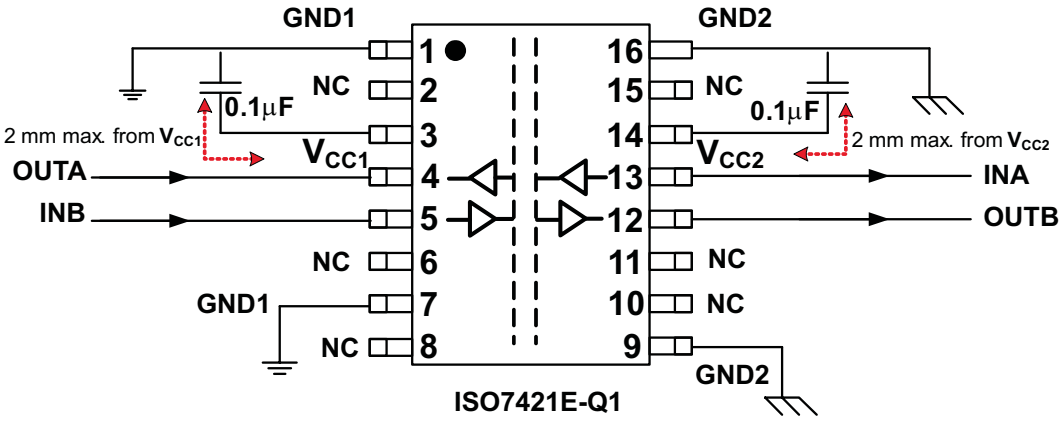


図 5. Typical ISO7421E-Q1 Application Circuit

17.6 Equivalent Input And Output Schematic Diagrams

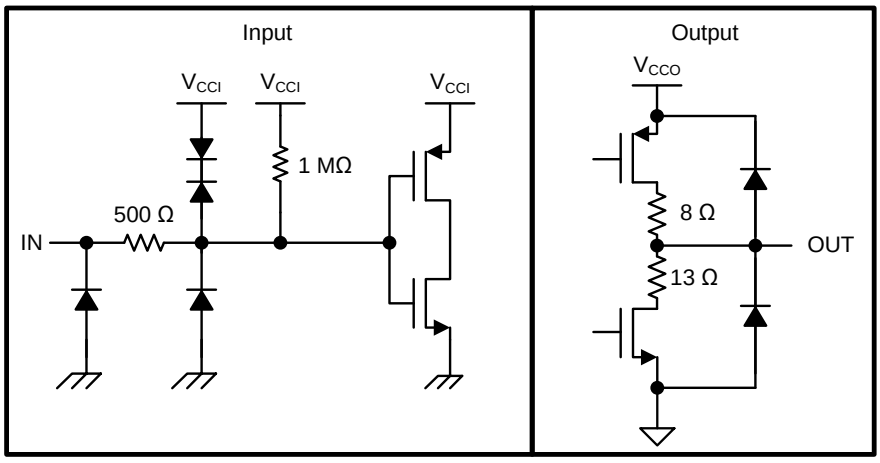


図 6. I/O Schematic

18 Typical Characteristics

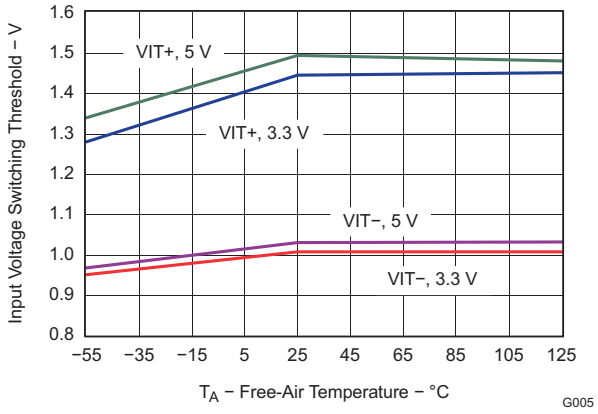


図 7. Input Voltage Switching Threshold Vs Free-air Temperature

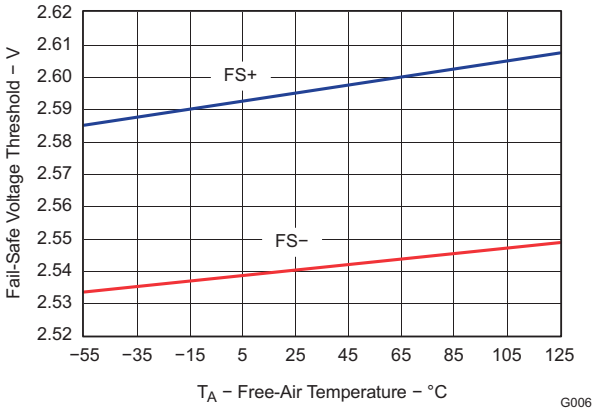


図 8. Fail-safe Voltage Threshold Vs Free-air Temperature

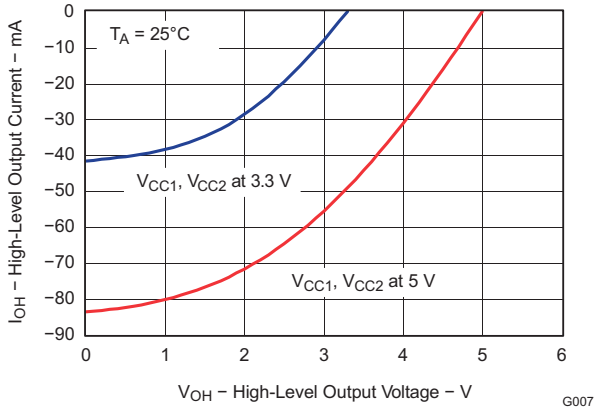


図 9. High-level Output Current Vs High-level Output Voltage

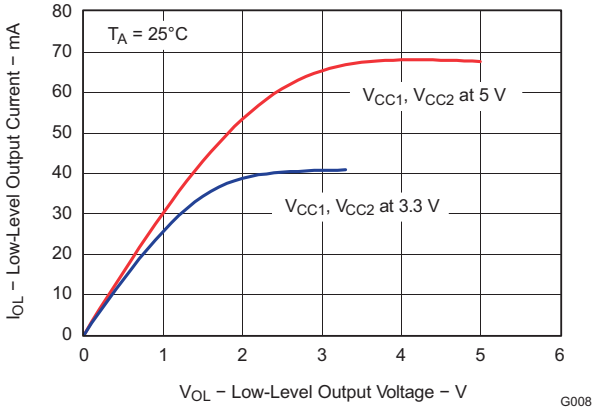


図 10. Low-level Output Current Vs Low-level Output Voltage

19 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

から変更 Revision B (May 2012) to Revision C **Page**

- 「特長」の箇条書き項目「広い周囲温度範囲: -40°C ~ 125°C」を削除、重複エントリであるため 1
- 「特長」の箇条書き項目を「最大 4kV ピークの絶縁、UL 1577 準拠で 2.5kVrms、IEC/VDE および CSA 認定、IEC 60950-1、IEC 61010-1 最終機器標準認定。 すべての認定は申請中です」から、「VDE 準拠で 4242V_{PK} の絶縁、UL 1577 準拠で 2.5kVrms の絶縁、IEC 60950-1 および IEC 61010-1 最終機器標準に従い CSA 認定済み」に変更 1
- 「ISO7421E-Q1 は...二重ガルバニック絶縁...」から「ISO7421E-Q1 は...ガルバニック絶縁...」に、「概要」セクションを変更 1
- デバイスの概略回路図を追加 1
- Changed column titles From:"INPUT SIDE (VCC)" To:"INPUT SIDE V_{CC} (V_{CCI})" and From:"OUTPUT SIDE (VCC)" To:"OUTPUT SIDE V_{CC} (V_{CCO})" in Device Function Table 3
- Changed MAX VALUE for V_I From: "6 V" To: "V_{CC} + 0.5 V" 3
- Added : "Maximum voltage must not exceed 6 V. A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output." 3
- Deleted Supply Current parameters with V_{CC1} and V_{CC2} at 5 V ± 5% for ISO7420x in Electrical Characteristics table since ISO7420x is not included in the data sheet. 5
- Deleted Supply Current parameters with V_{CC1} at 5 V ± 5%, V_{CC2} at 3.3 V ± 5% for ISO7420x in Electrical Characteristics table since ISO7420x is not included in the data sheet. 6
- Deleted Supply Current parameters with V_{CC1} at 3.3 V ± 5%, V_{CC2} at 5 V ± 5% for ISO7420x in Electrical Characteristics table since ISO7420x is not included in the data sheet. 7
- Deleted Supply Current parameters with V_{CC1} and V_{CC2} at 3.3 V ± 5% for ISO7420x in Electrical Characteristics table since ISO7420x is not included in the data sheet. 8
- Changed V_{CC1} to V_{CCI} and Vcc/2 to 50% in 図 1 9
- Changed Vcc1 to V_{CCI} and IN From:"0V or V_{CC1}" To:"0 V" in 図 2 9
- Corrected 'Ground' symbols on both sides of the Isolation Barrier in 図 3 9
- Changed MIN specification for Clearance or L(I01) From: "8.34 mm" To:"7.6 mm" in Package Characteristics table. 10
- Changed MIN specification for Creepage or L(I02) From: "8.1 mm" To:"7.6 mm" in Package Characteristics table. 10
- Changed CTI TEST CONDITIONS From: " DIN IEC 60112 / VDE 0303 Part 1" To: "DIN EN 60112 (VDE 0303-11)" 10
- Added "V_{TEST} = 1.2 x V_{ISO}" to V_{ISO} parameter TEST CONDITIONS in Insulation Characteristics table 11
- Changed VDE standard name From: "IEC 60747-5-2" To:"DIN VDE V 0884-11:2017-01" and document reference From:"File Number: Pending" To:"Certificate Number: 40047657" respectively in Regulatory Information table..... 11
- Changed CSA standard reference From:"Approved under CSA Component Acceptance Notice" To:"Approved according to IEC 60950-1 and IEC 61010-1" and document reference From: "File Number: pending" To:"Master Contract Number: 220991" respectively in Regulatory Information table..... 11
- Changed UL standard reference From:"1577" To:"UL 1577" in Regulatory Information table. 11
- Changed ground symbol of 'Output' to differentiate it from 'Input' in 図 6 12

から変更 Revision A (March 2012) to Revision B **Page**

- 信号速度の情報を 1 から 50Mbps に変更 1
- Changed Signaling rate max value from 1 to 50 Mbps, centered 0 in the min column. 4
- Replaced Supply Current section with marked up table from commercial datasheet SLLSE45, changed 8.5 max value to 9.1. 5
- Replaced Supply Current section with marked up table from commercial datasheet SLLSE45, changed 8.5 max value to 9.1 and changed 5.5 max value to 5.8. 6
- Replaced Supply Current section with marked up table from commercial datasheet SLLSE45, changed 5.5 max value to 5.8 and changed 8.5 max value to 9.1. 7
- Replaced Supply Current section with marked up table from commercial datasheet SLLSE45, changed 5.5 max value to 5.8. 8

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7421EQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7421EQ
ISO7421EQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7421EQ
ISO7421EQDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7421EQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF ISO7421E-Q1 :

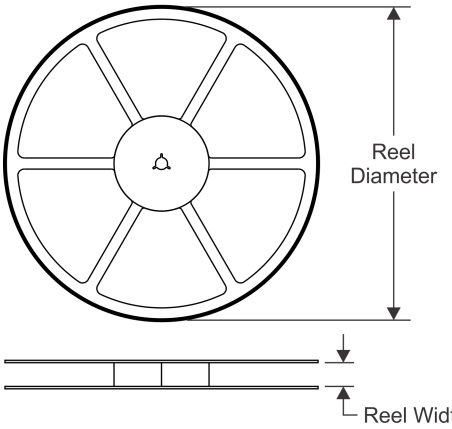
- Catalog : ISO7421E

NOTE: Qualified Version Definitions:

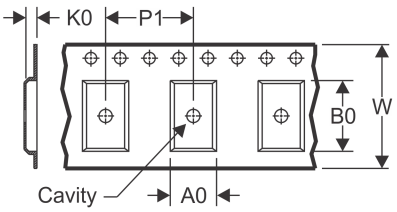
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

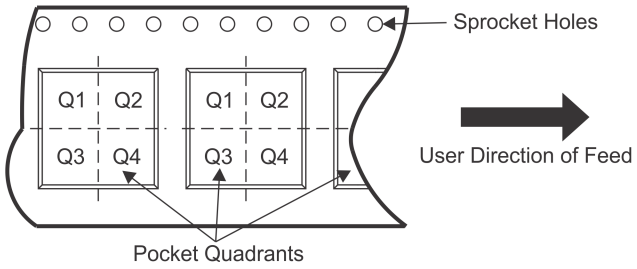


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

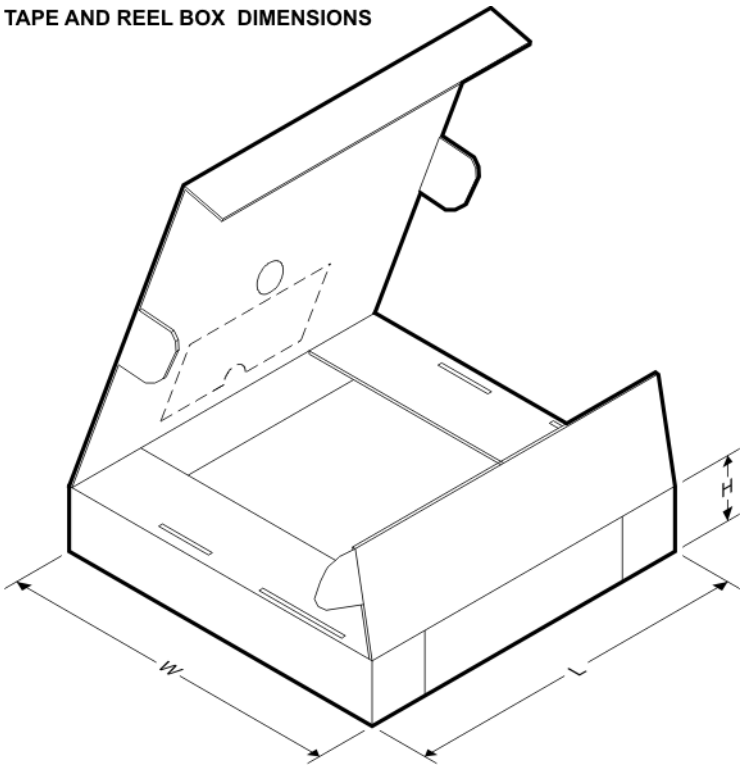
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7421EQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7421EQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

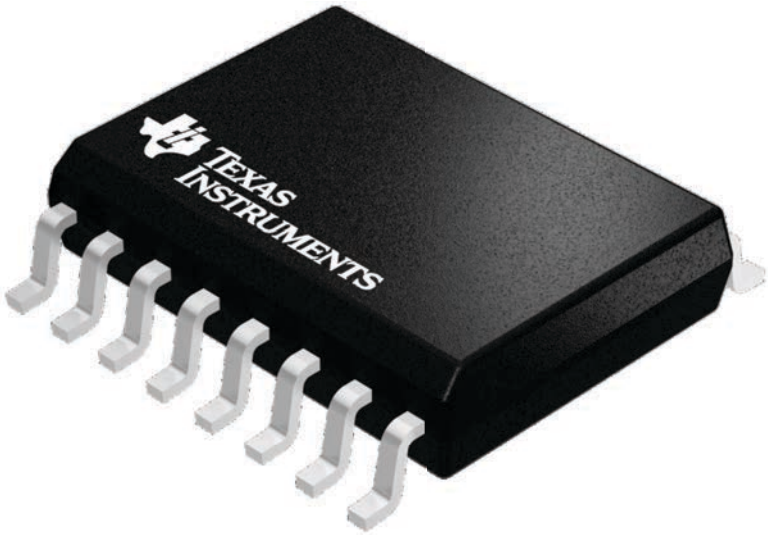
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

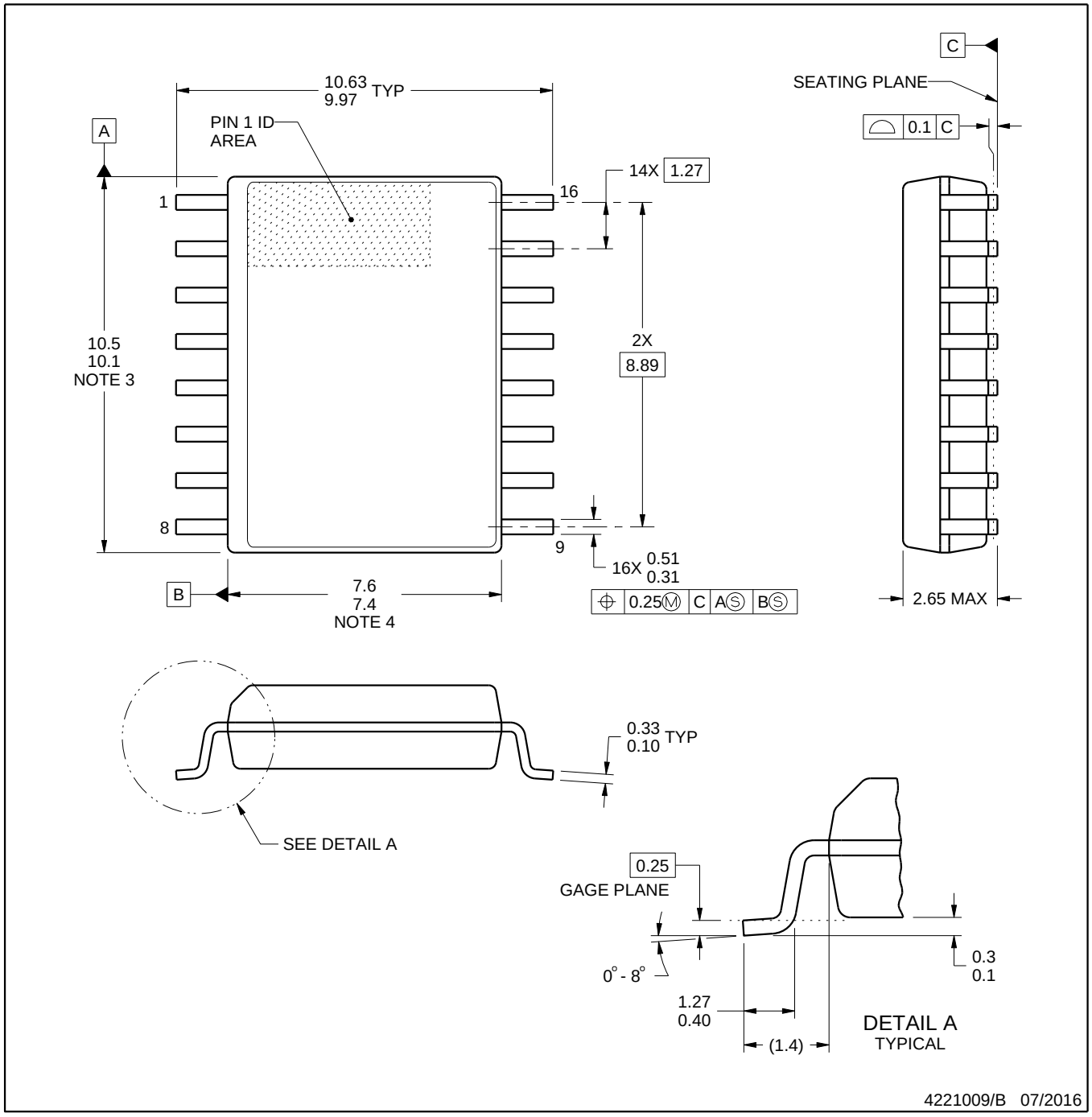
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



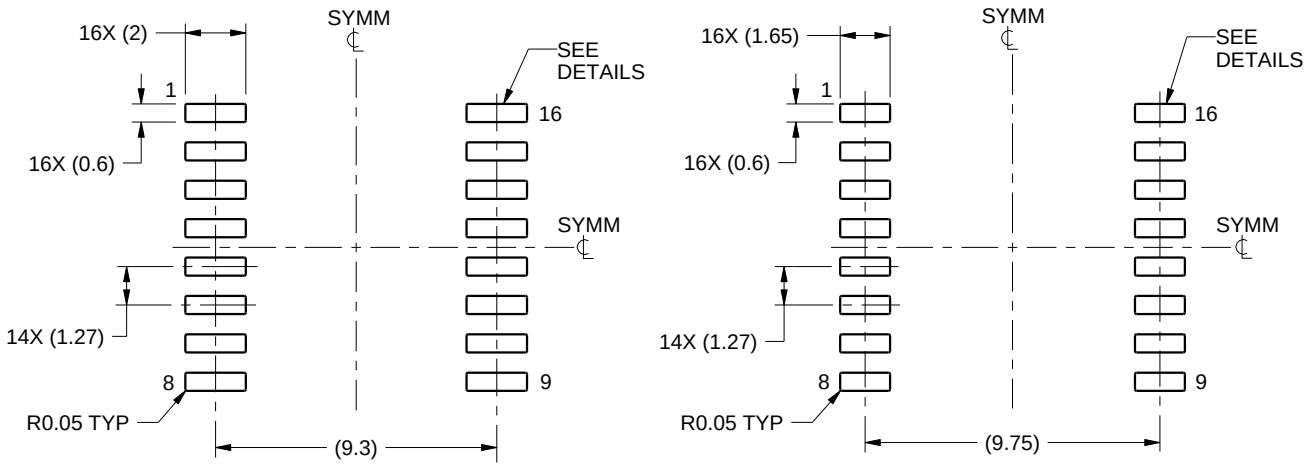
4224780/A

SOIC



NOTES:

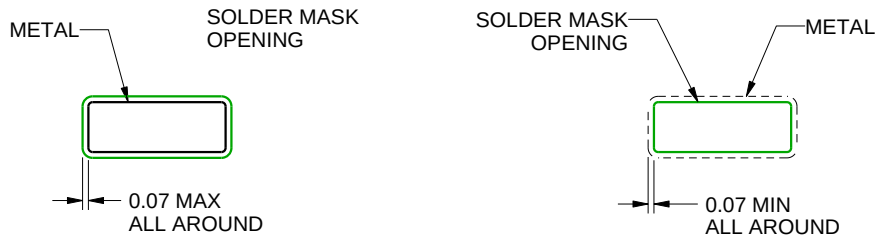
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

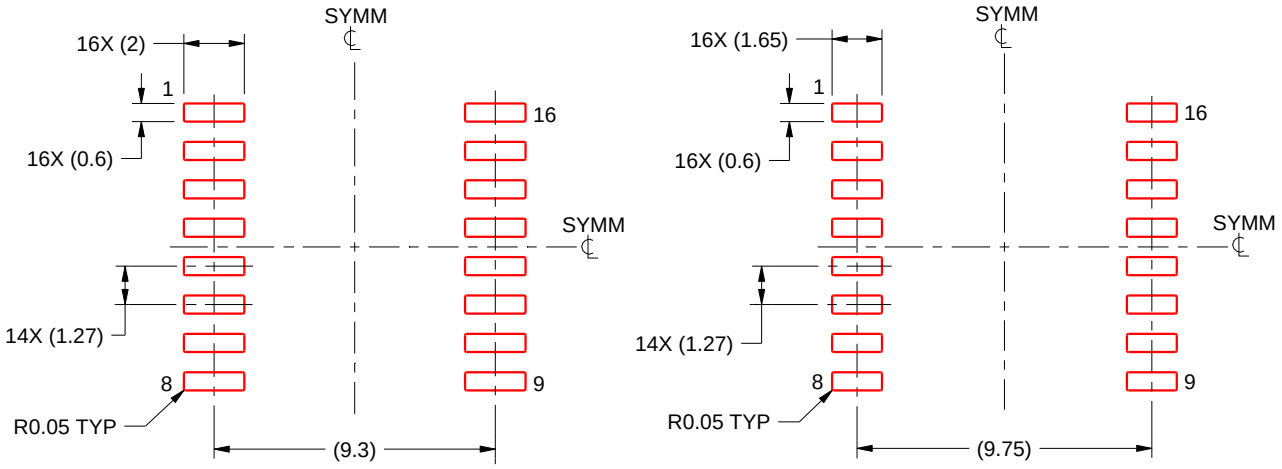
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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