1-Mbps QUAD DIGITAL ISOLATORS

Check for Samples: ISO7241A-EP

FEATURES

- 4000-V_{peak} Isolation, 560-V_{peak} V_{IORM}
  - UL 1577 , IEC 60747-5-2 (VDE 0884, Rev 2), IEC 61010-1, IEC 60950-1 and CSA Approved
- 4-kV ESD Protection
- Operates With 3.3-V or 5-V Supplies
- Typical 25-Year Life at Rated Working Voltage (See Application Note (SLLA197) and Figure 10)
- High Electromagnetic Immunity (See Application Report (SLLA181))

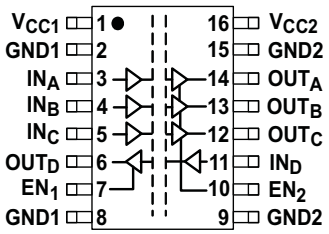
APPLICATIONS

- Industrial Fieldbus
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military (–55°C/125°C) Temperature Range(1)
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

ISO7241A
(TOP VIEW)



(1) Additional temperature ranges available - contact factory

DESCRIPTION

See the Product Notification section. The ISO7241A is a quad-channel digital isolator with multiple channel configurations and output enable functions. This device has logic input and output buffers separated by TI's silicon dioxide (SiO_2) isolation barrier. Used in conjunction with isolated power supplies, this device blocks high voltage, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

The ISO7241A has three channels the same direction and one channel in opposition.

This device has TTL input thresholds and a noise-filter at the input that prevents transient pulses from being passed to the output of the device.

A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state. (See ISO7240CF (SLLS869) or contact TI for a logic low failsafe option).

The ISO7241A may be powered from either 3.3-V or 5-V supplies on either side in any 3.3-V / 3.3-V, 5-V / 5-V, 5-V / 3.3-V, or 3.3-V / 5-V combination. Note that the signal input pins are 5-V tolerant regardless of the voltage supply level being used.

This device is characterized for operation over the ambient temperature range of –55°C to 125°C.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTION DIAGRAM

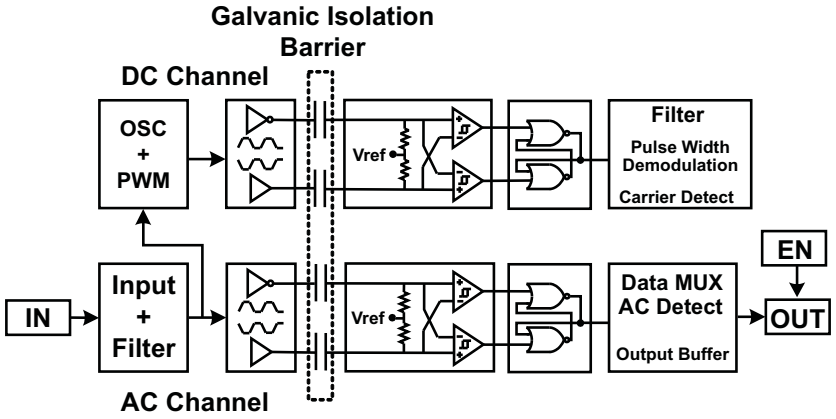


Table 1. Device Function Table(1)

INPUT V_{CC}	OUTPUT V_{CC}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z

(1) PU = Powered Up; PD = Powered Down ; X = Irrelevant; H = High Level; L = Low Level

Table 2. ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	DW	Reel	ISO7241AMDWREP	ISO7241AM

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

ABSOLUTE MAXIMUM RATINGS(1)

					VALUE	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}				–0.5 to 6	V
V_I	Voltage at IN, OUT, EN				–0.5 to 6	V
I_O	Output current				±15	mA
ESD	Electrostatic discharge	Human Body Model	JEDEC Standard 22, Test Method A114-C.01	All pins	±4	kV
		Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101		±1	
		Machine Model	ANSI/ESDS5.2-1996		±200	V
T_J	Maximum junction temperature				170	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage(1), V_{CC1}, V_{CC2}	3.15		5.5	V
I_{OH}	High-level output current			4	mA
I_{OL}	Low-level output current	–4			mA
t_{ui}	Input pulse width	1			µs
$1/t_{ui}$	Signaling rate	0		1000	kbps
V_{IH}	High-level input voltage (IN) (EN on all devices)	2		V_{CC}	V
V_{IL}	Low-level input voltage (IN) (EN on all devices)	0		0.8	V
T_J	Junction temperature			150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification			1000	A/m

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V[1] OPERATION

, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{CC1}	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6.5	11	mA
	1 Mbps					
I_{CC2}	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		13	20	mA
	1 Mbps			13	20	
ELECTRICAL CHARACTERISTICS						
I_{OFF}	Sleep mode output current	EN at 0 V, Single channel		0		µA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.8			V
		I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 1			0.4	V
		I_{OL} = 20 µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current		–10			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		2		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 4	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 1	40		95	ns
PWD	Pulse-width distortion[1] $\lvert t_{PHL} - t_{PLH} \rvert$				10	
$t_{sk(o)}$	Channel-to-channel output skew [2]				2	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		12		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			6.5	11	mA
	1 Mbps						
I_{CC2}	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			8	13	mA
	1 Mbps				8	13	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current	EN at 0 V, Single channel			0		µA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 1	(5-V side)	V_{CC} – 0.8			V
		I_{OH} = –20 µA, See Figure 1		V_{CC} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 1				0.4	V
		I_{OL} = 20 µA, See Figure 1				0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current	IN from 0 V to V_{CC}				10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)			2		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 4		25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 1	40		100	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				11	
$t_{sk(o)}$	Channel-to-channel output skew (2)				3	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		18		µs

(1) Also known as pulse skew
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3-V, V_{CC2} at 5-V[1] OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			4	7	mA
	1 Mbps				4	7	
I_{CC2}	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			13	20	mA
	1 Mbps				13	20	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current	EN at V_{CC}, Single channel			0		µA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 1	(5-V side)	V_{CC} – 0.8			V
		I_{OH} = –20 µA, See Figure 1		V_{CC} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 1				0.4	V
		I_{OL} = 20 µA, See Figure 1				0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current	IN from 0 V to V_{CC}				10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)			2		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 4		25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 3.3-V and V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 1	40		100	ns
PWD	Pulse-width distortion[1] $\lvert t_{PHL} - t_{PLH} \rvert$				11	
$t_{sk(o)}$	Channel-to-channel output skew [2]				2.5	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		12		µs

(1) Also known as pulse skew
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V[1] OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{CC1}	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		4	7	mA
	1 Mbps			4	7	
I_{CC2}	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		8	13	mA
	1 Mbps			8	13	
ELECTRICAL CHARACTERISTICS						
I_{OFF}	Sleep mode output current	EN at 0 V, single channel		0		µA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4			V
		I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 1			0.4	V
		I_{OL} = 20 µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}			10	µA
I_{IL}	Low-level input current		–10			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		2		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 4	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

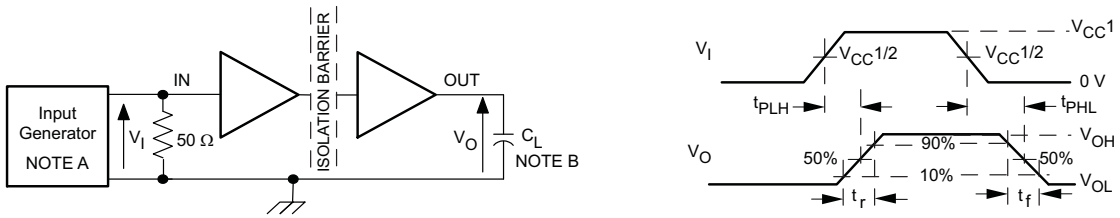
SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 1	45		110	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ [1]				12	
$t_{sk(o)}$	Channel-to-channel output skew [2]				3.5	ns
t_r	Output signal rise time	See Figure 1		2		
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		18		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

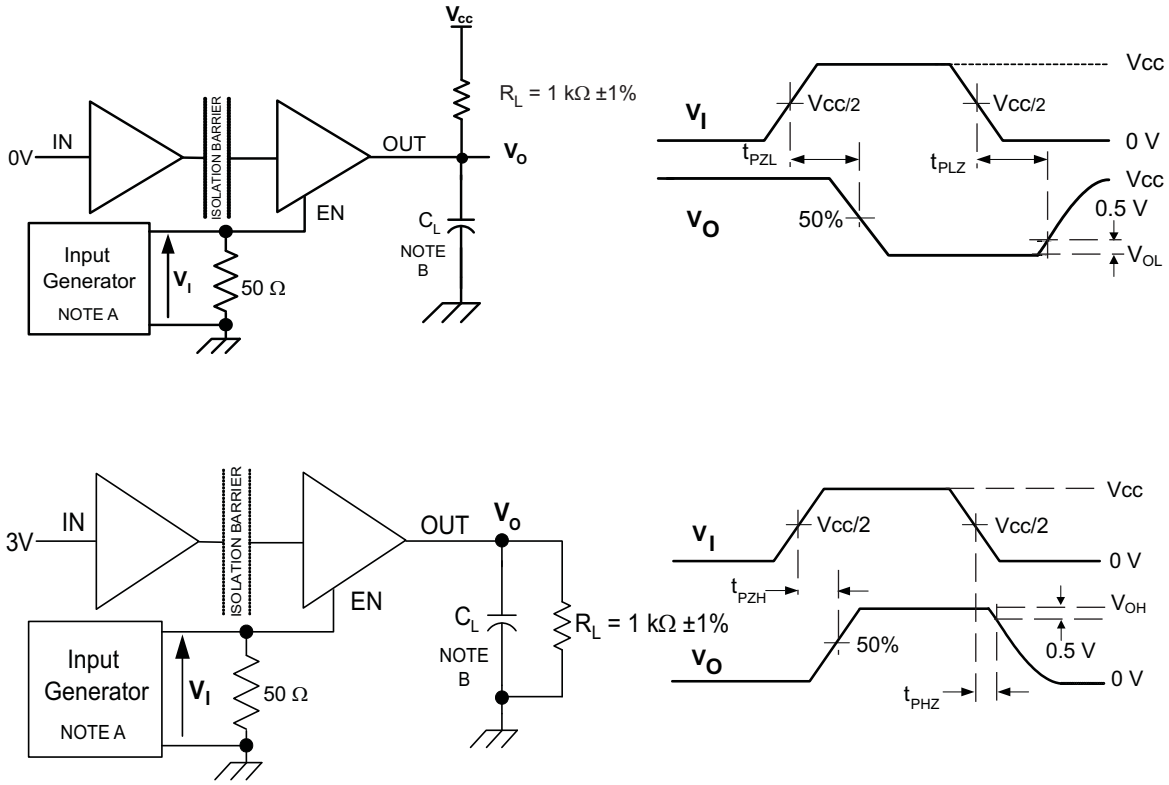
PARAMETER MEASUREMENT INFORMATION



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms

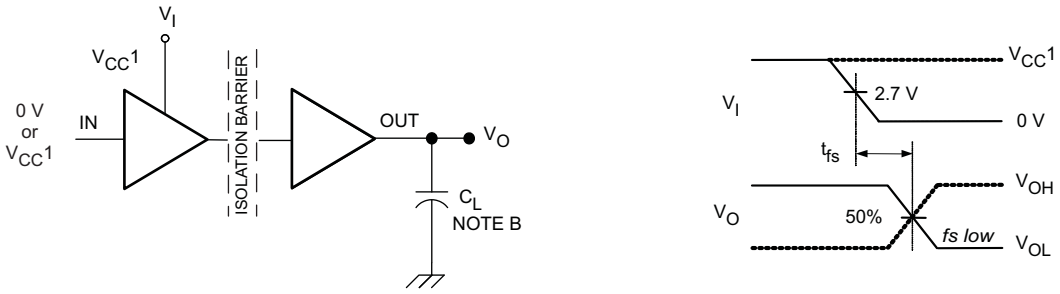


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

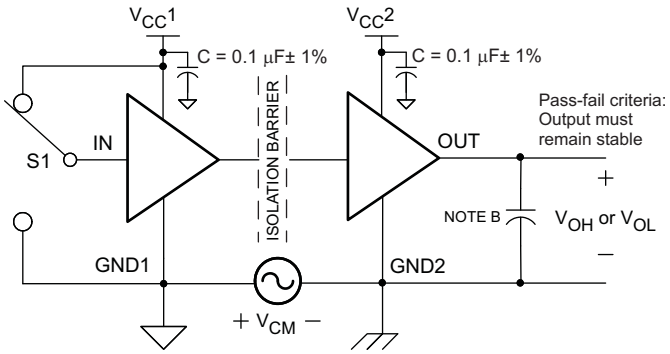
PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

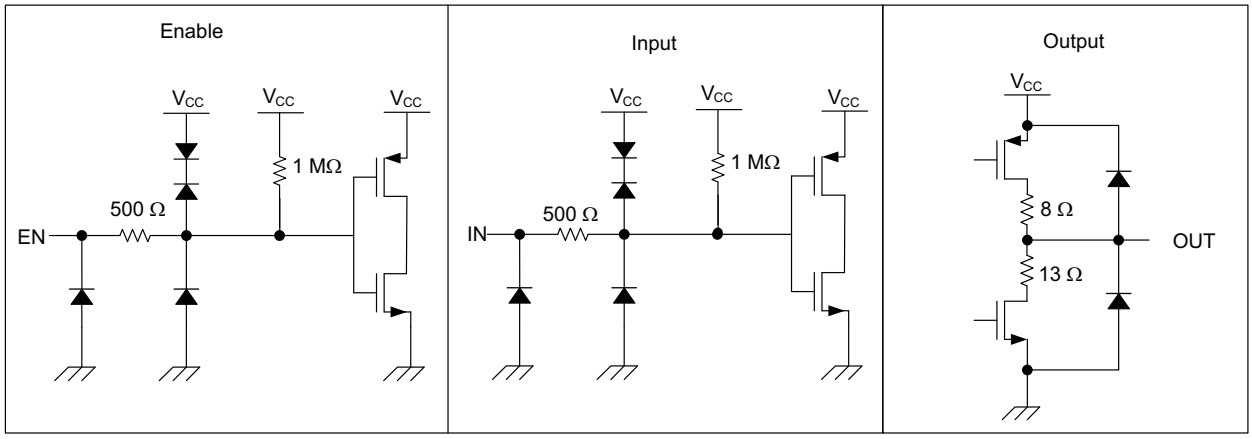
Figure 4. Common-Mode Transient Immunity Test Circuit and Voltage Waveform

DEVICE INFORMATION

PACKAGE CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	8.34			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	8.1			mm
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device		$>10^{12}$		Ω
C_{IO}	Barrier capacitance Input to output	V_I = 0.4 sin (4E6πt)		2		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)		2		pF

DEVICE I/O SCHEMATICS



REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program(1)
File Number: 40016131	File Number: 1698195	File Number: E181974

(1) Production tested ≥ 3000 Vrms for 1 second in accordance with UL 1577.

THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air	Low-K Thermal Resistance(1)		168		°C/W
		High-K Thermal Resistance		96.1		
θ_{JB}	Junction-to-Board Thermal Resistance			61		°C/W
θ_{JC}	Junction-to-Case Thermal Resistance			48		°C/W
P_D	Device Power Dissipation	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 50% duty cycle square wave			220	mW

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

TYPICAL CHARACTERISTIC CURVES

INPUT VOLTAGE THRESHOLD vs FREE-AIR TEMPERATURE

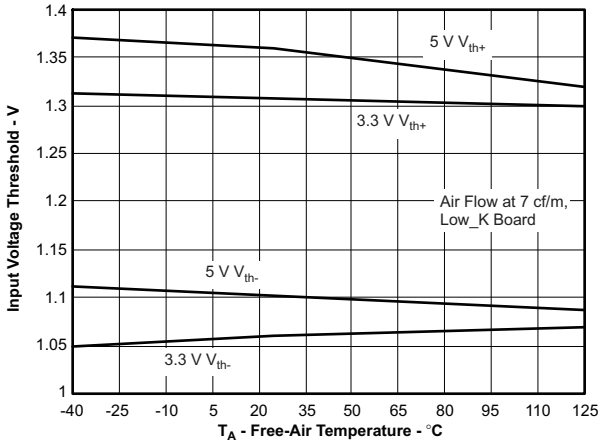


Figure 5.

V_{CC1} FAILSAFE THRESHOLD vs FREE-AIR TEMPERATURE

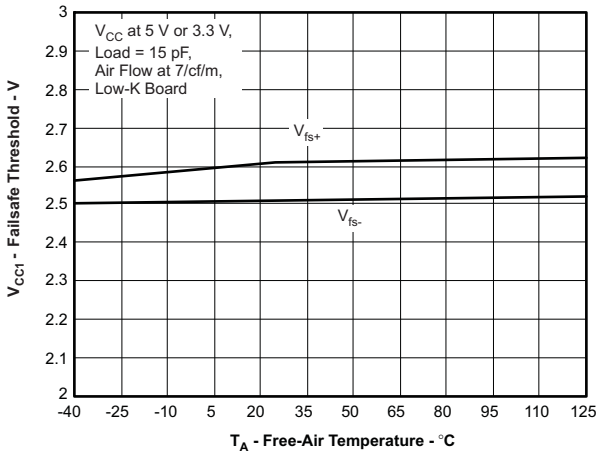


Figure 6.

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

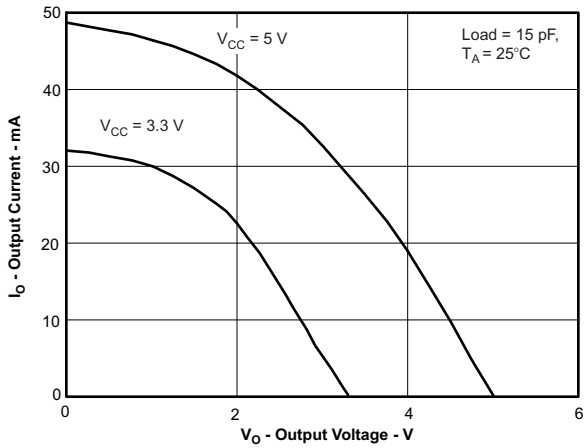


Figure 7.

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

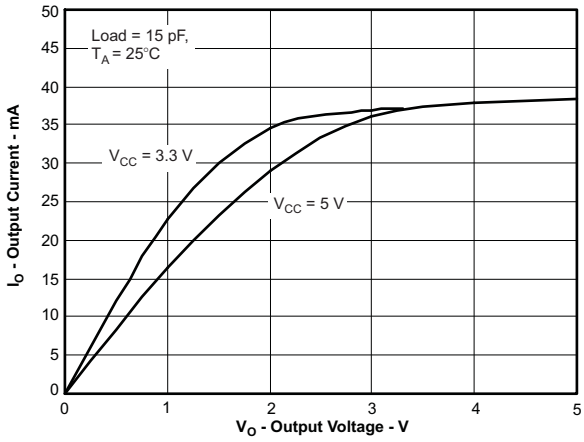


Figure 8.

APPLICATION INFORMATION

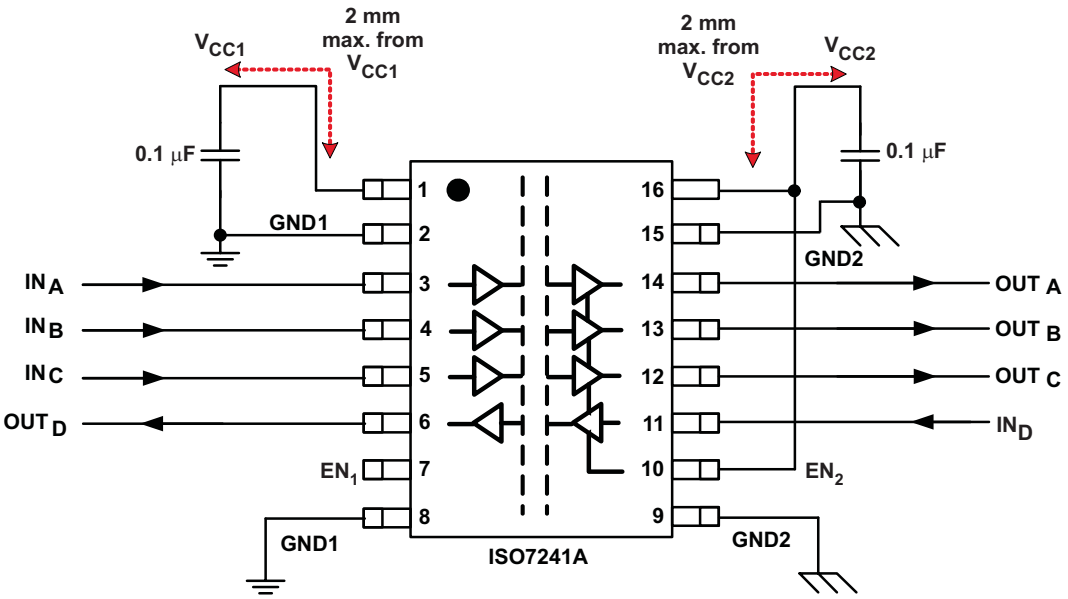


Figure 9. Typical Application Circuit

LIFE EXPECTANCY vs. WORKING VOLTAGE

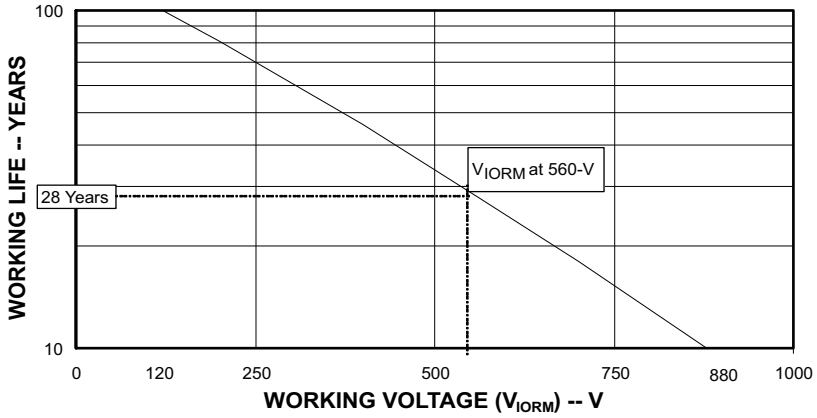


Figure 10. Time-Dependant Dielectric Breakdown Testing Results

PRODUCT NOTIFICATION

An ISO7241A anomaly occurs when a negative-going pulse below the specified 1-µs minimum bit width is input to the device. The output locks in a logic-low condition until the next rising edge occurs after a 1-µs period.

Positive noise edges in pulses of less than the minimum specified 1 µs have no effect on the device, and are properly filtered.

To prevent noise from interfering with ISO7241A performance, it is recommended that an appropriately sized capacitor be placed on each input of the device

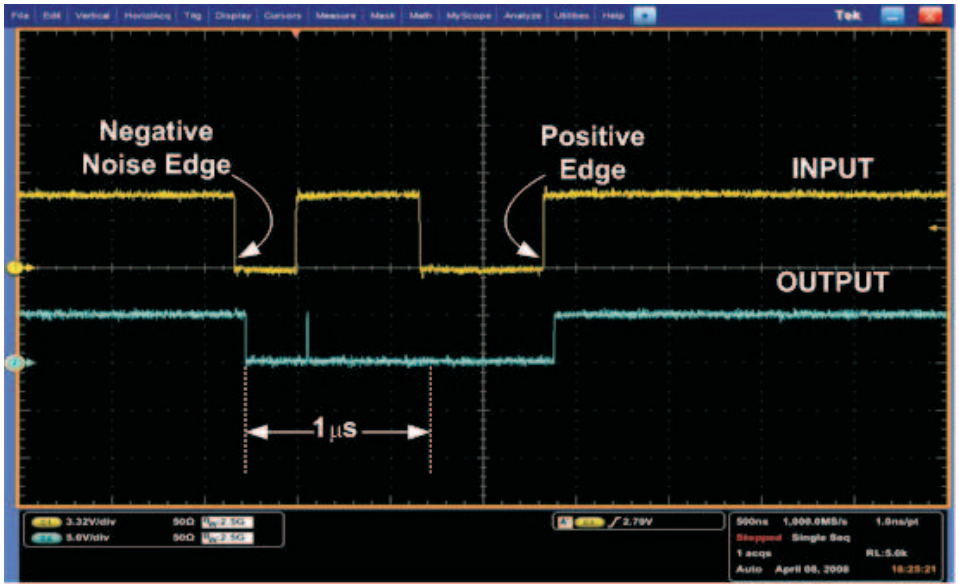


Figure 11. ISO7241A Anomaly

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7241AMDWREP	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7241AM
ISO7241AMDWREP.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7241AM
V62/10606-01XE	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7241AM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

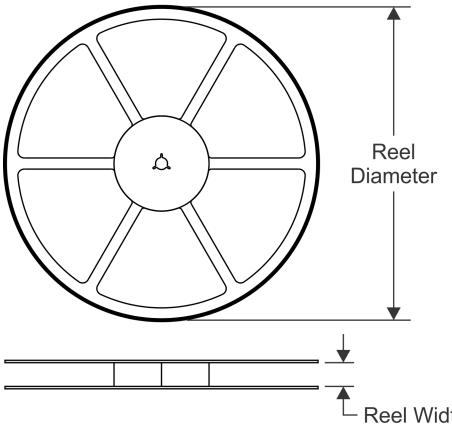
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

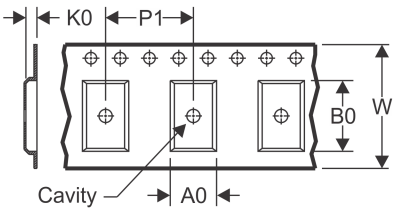
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

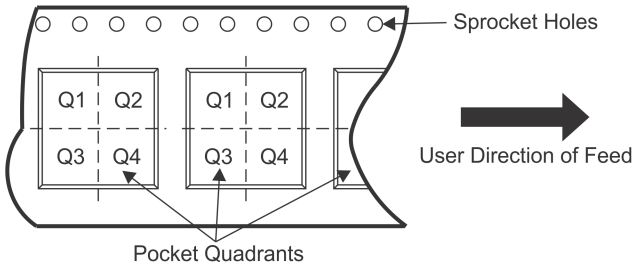


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

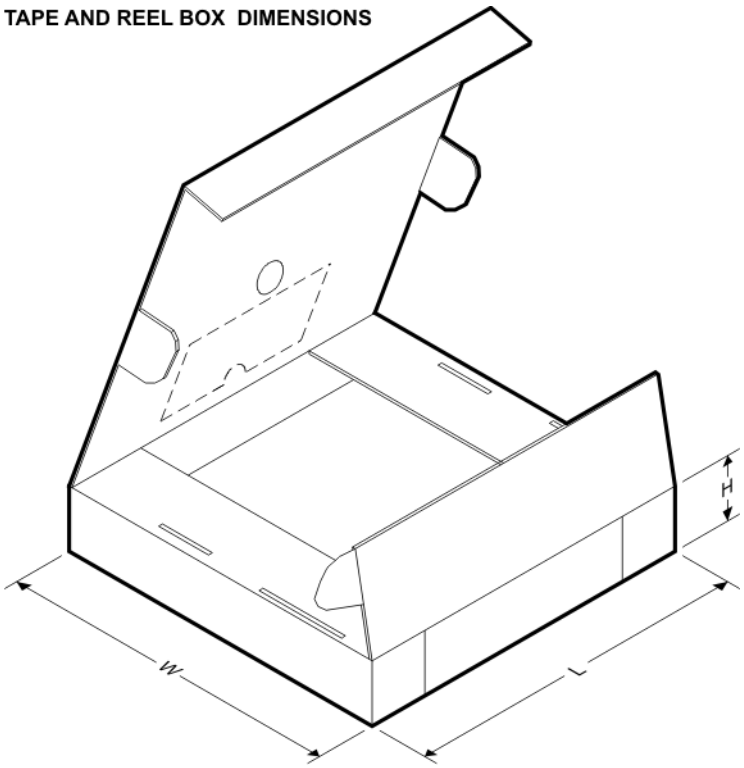
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7241AMDWREP	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7241AMDWREP	SOIC	DW	16	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

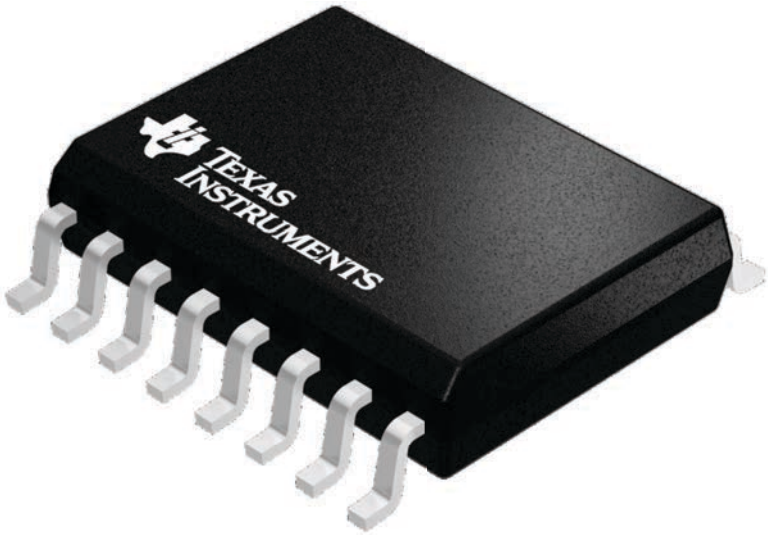
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

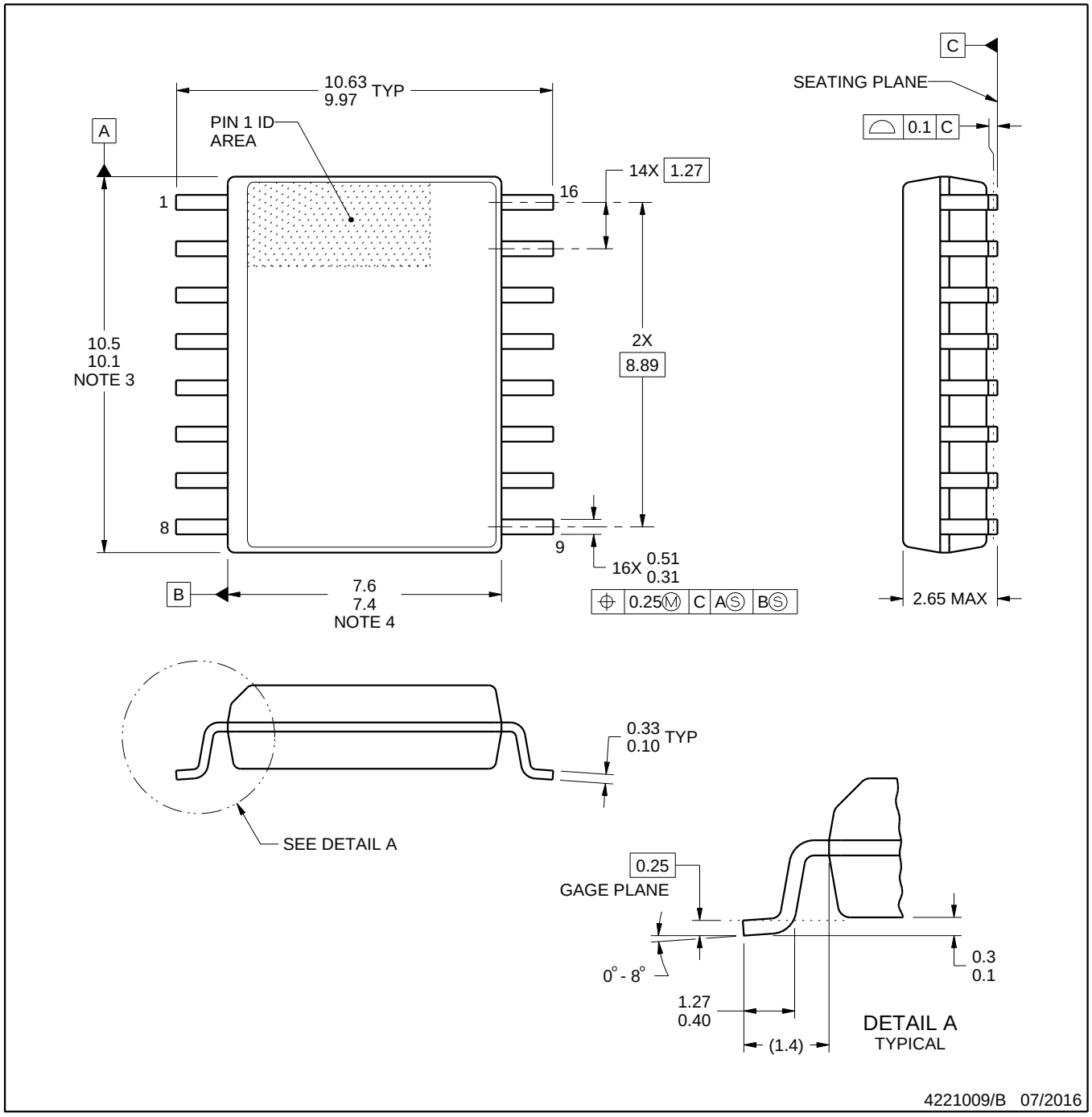
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



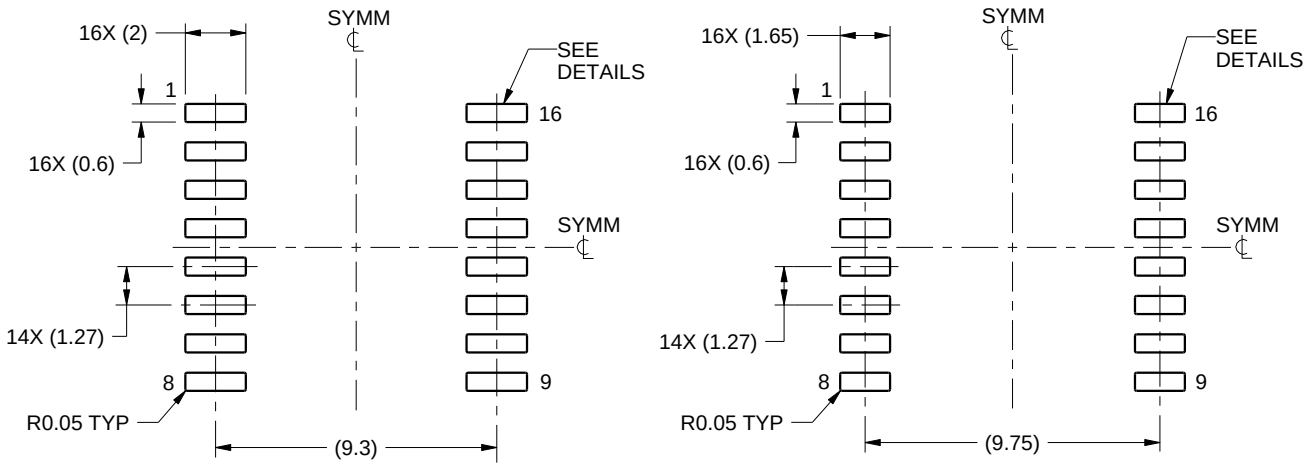
4224780/A

SOIC



NOTES:

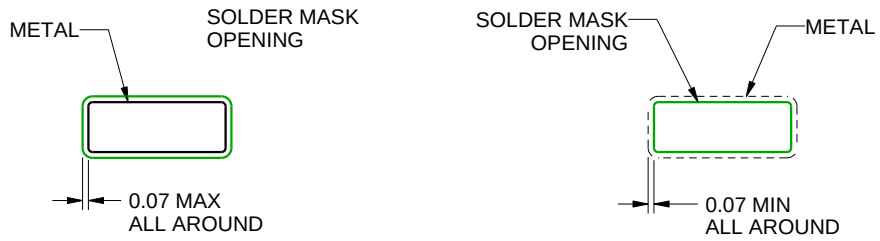
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

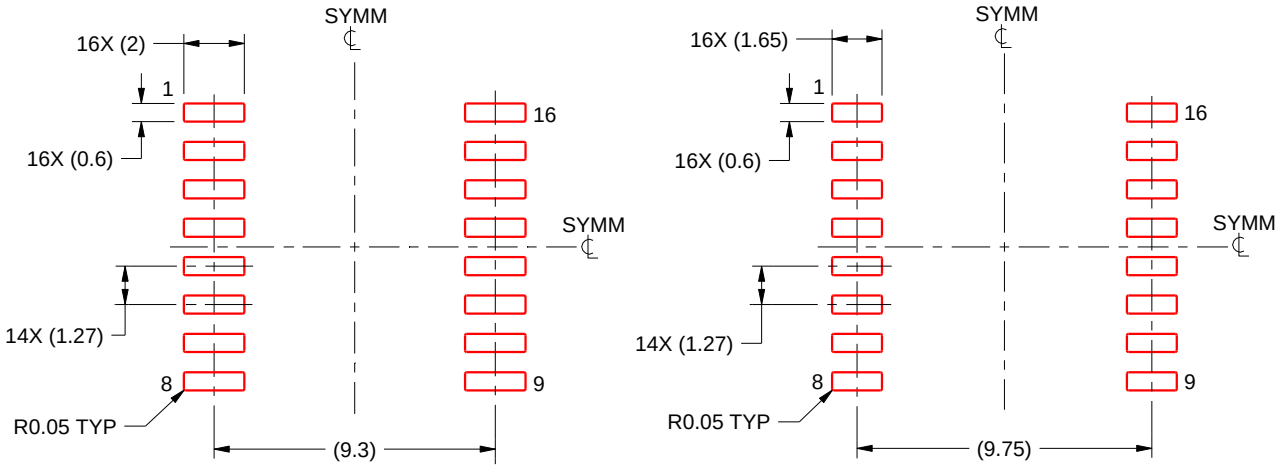
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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