ISO723xx 高速、トリプル チャネル デジタル アイソレータ

1 特長

- 25Mbps と 150Mbps の信号速度オプション
  - 低いチャネル間の出力スキュー:
    最大値 1ns
  - 低いパルス幅歪み (PWD):
    最大値 2ns
  - 低ジッタ成分:150Mbps で標準値 1ns
- 定格動作電圧で標準寿命 25 年
  (「絶縁寿命予測」を参照)
- ESD 保護:4kV
- 3.3V または 5V の電源で動作
- 3.3V から 5V への電圧レベル変換
- 高い電磁界耐性
  (アプリケーションノート『ISO72x デジタル アイソレータの磁界耐性』』を参照)
- -40℃～125℃ の動作範囲
- 安全関連認証 :
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 部品認定プログラム
  - IEC 61010-1 証明書、IEC 62368-1 証明書

2 アプリケーション

- ファクトリ オートメーション
  - Modbus
  - Profibus™
  - DeviceNet™ データバス
- コンピュータ ペリフェラル インターフェイス
- サーボ制御インターフェイス
- データ アクイジション

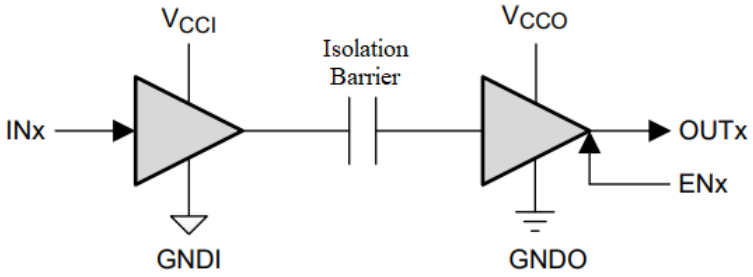
3 概要

ISO7230 および ISO7231 は、それぞれ複数のチャネル構成と出力イネーブル機能を備えたトリプル チャネルのデジタル アイソレータです。これらのデバイスは、テキサス インスツルメンツ独自の二酸化ケイ素 (SiO_2) 絶縁バリアで分離されたロジック入出力バッファを備えています。これらのデバイスを絶縁型電源と組み合わせて使用すると、高電圧がブロックされ、グランドが絶縁されます。また、データ バスや他の回路で発生したノイズ電流がローカル グランドに入り込み、ノイズに敏感な回路に干渉または損傷を与えることを防止します。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)	パッケージ サイズ(2)
ISO7230C ISO7231C ISO7231M	DW (SOIC、16)	10.30mm × 7.50mm	10.30mm × 10.30mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



A. V_{CCI} および GNDI は、それぞれ入力チャネルの電源およびグランド接続です。
B. V_{CCO} および GNDO は、それぞれ出力チャネルの電源およびグランド接続です。

概略回路図

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4 Device Comparison Table

PRODUCT	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION	ISOLATION RATING
ISO7230C	25 Mbps	≅1.5 V (TTL) (CMOS compatible)	3/0	4000 V_{PK}, 2500 V_{RMS}
ISO7231C	25 Mbps	≅1.5 V (TTL) (CMOS compatible)	2/1	
ISO7231M	150 Mbps	V_{CC}/2 (CMOS)		

5 Pin Configuration and Functions

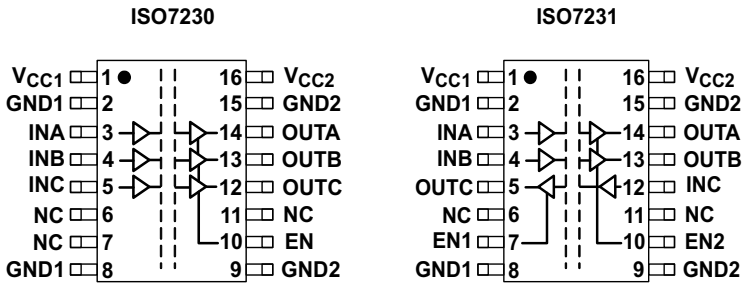


図 5-1. DW Package 16-Pin SOIC Top View

表 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	ISO7230	ISO7231		
EN	10	—	I	Enable, channel A, B, and C
EN1	—	7	I	Enable, channel C
EN2	—	10	I	Enable, channel A and B
GND1	2, 8	2, 8	—	Ground connection for V_{CC1}
GND2	9, 15	9. 15	—	Ground connection for V_{CC2}
INA	3	3	I	Input, channel A
INB	4	4	I	Input, channel B
INC	5	12	I	Input, channel C
NC	6, 7, 11	6, 11	—	Not connected
OUTA	14	14	O	Output, channel A
OUTB	13	13	O	Output, channel B
OUTC	12	5	O	Output, channel C
V_{CC1}	1	1	—	Power supply, V_{CC1}
V_{CC2}	16	16	—	Power supply, V_{CC2}

(1) I = Input; O = Output

6 Specifications

6.1 Absolute Maximum Ratings

See(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}	–0.5	6	V
V_I	Voltage at INx, OUTx, ENx	–0.5	V_{CC} + 0.5(3)	V
I_O	Output current	–15	15	mA
T_J	Maximum junction temperature		170	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC(1)		ISO7230C, ISO7231C, ISO7231M DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	168	°C/W
		68.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.4 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}		3.15		5.5	V
I_{OH}	High-level output current		–4			mA
I_{OL}	Low-level output current				4	mA
t_{ui}	Input pulse width(1)	ISO723xC	40			ns
t_{ui}	Input pulse width(1)	ISO723xM	6.67	5		ns
$1/t_{ui}$	Signaling rate(1)	ISO723xC	0	30	25	Mbps
$1/t_{ui}$	Signaling rate(1)	ISO723xM	0	200	150	Mbps
V_{IH}	High-level input voltage	ISO723xM	0.7 x V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage	ISO723xM	0		0.3 x V_{CC}	V
V_{IH}	High-level input voltage	ISO723xC	2		5.5	V

			MIN	NOM	MAX	UNIT
V_{IL}	Low-level input voltage	ISO723xC	0		0.8	V
T_A	Ambient temperature		-40	25	125	
T_J	Junction temperature				150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

(1) Typical signaling rate and Input pulse width are measured at ideal conditions at 25°C.
(2) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.
For the 2.8-V operation, V_{CC1} or V_{CC2} is specified at 2.8 V.

6.5 Power Ratings

over operating free-air temperature range (unless otherwise noted)

PARAMETER		ISO7230C, ISO7231C, ISO7231M	UNIT
		DW (SOIC)	
		16 PINS	
P_D	Device power dissipation, V_{CC1} = V_{CC2} = 5.5 V, TJ = 150C, C_L = 15 pF, D Input a 50% duty cycle, 25-Mbps square wave	220	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.008	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	400	V
	Material group		II	
	Overvoltage category	Rated mains voltage ≤150 V_{RMS}	I-IV	
		Rated mains voltage ≤300 V_{RMS}	I-III	
		Rated mains voltage ≤400 V_{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17):(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t= 1 s (100% production)	4000	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM} , t_m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.3 × V_{IORM}, t_m = 10 s	≤5	
		Method b: At routine test (100% production); Vini = 1.2 x VIOTM, tini = 1s; Vpd(m) = 1.5 x VIORM, tm = 1s (method b1) or Vpd(m) = Vini, tm = tini (method b2)	≤5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 x sin (2πft), f = 1 MHz	1	pF
R_{IO}	Isolation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 2500 V_{RMS}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO} = 3000 V_{RMS}, t = 1 s (100% production)	2500	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the

isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

(2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Apparent charge is electrical discharge caused by a partial discharge (pd).

(4) All pins on each side of the barrier tied together creating a two-terminal device

6.7 Safety-Related Certifications

VDE	CSA	UL
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 62368-1	Plan to certify according to UL 1577 Component Recognition Program
Certificate planned	Certificate planned	Certificate planned

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C, see セクション 6.3			124	mA
		$R_{\theta JA}$ = 212°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C, see セクション 6.3			190	
T_S	Safety temperature				150	°C

(1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7230C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN at 3 V		0.5	1.2	mA
		25 Mbps			3	5	
	ISO7231C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN1 at 3 V, EN2 at 3 V		4.5	7	mA
		25 Mbps			6.5	11	
I_{CC2}	ISO7230C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN at 3 V		9	15	mA
		25 Mbps			10	17	
	ISO7231C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN1 at 3 V, EN2 at 3 V		8	12	mA
		25 Mbps			10.5	16	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		ENx at 0 V, single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See 図 7-1	V_{CCO} – 0.4			V
			I_{OH} = –20 µA, See 図 7-1	V_{CCO} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See 図 7-1			0.4	V
			I_{OL} = 20 µA, See 図 7-1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		INx at V_{CCI}			10	µA
I_{IL}	Low-level input current		INx at 0 V	–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (2πft), f=2MHz		2		pF
CMTI	Common-mode transient immunity		V_I = V_{CCI} or 0 V, See 図 7-4	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

6.10 Electrical Characteristics: V_{CC1} and V_{CC2} at 5-V

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7230C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN at 3 V		1	3	mA
		25 Mbps			7	9.5	
	ISO7231C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN1 at 3 V, EN2 at 3 V		6.5	11	mA
		25 Mbps			11	17	
I_{CC2}	ISO7230C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN at 3 V		15	22	mA
		25 Mbps			17	24	
	ISO7231C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN1 at 3 V, EN2 at 3 V		13	20	mA
		25 Mbps			17.5	27	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		ENx at 0 V, single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See 図 7-1	V_{CCO} – 0.8			V
			I_{OH} = –20 µA, See 図 7-1	V_{CCO} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See 図 7-1			0.4	V
			I_{OL} = 20 µA, See 図 7-1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		INx at V_{CCI}			10	µA
I_{IL}	Low-level input current		INx at 0 V	–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (2πft), f=2MHz		2		pF
CMTI	Common-mode transient immunity		V_I = V_{CCI} or 0 V, See 図 7-4	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

6.11 Electrical Characteristics: V_{CC1} at 3.3-V, V_{CC2} at 5-V

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7230C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN at 3 V			0.5	1.2	mA
		25 Mbps				3	5	
	ISO7231C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN1 at 3 V, EN2 at 3 V			4.5	7	mA
		25 Mbps				6.5	11	
I_{CC2}	ISO7230C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN at 3 V			15	22	mA
		25 Mbps				17	24	
	ISO7231C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN1 at 3 V, EN2 at 3 V			13	20	mA
		25 Mbps				17.5	27	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		ENx at 0 V, Single channel			0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See 図 7-1	ISO7230	V_{CCO} – 0.4			V
				ISO7231 (5-V side)	V_{CCO} – 0.8			
			I_{OH} = –20 µA, See 図 7-1		V_{CCO} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See 図 7-1				0.4	V
			I_{OL} = 20 µA, See 図 7-1				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		INx at V_{CCI}				10	µA
I_{IL}	Low-level input current		INx at 0 V		–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (2πft), f=2MHz			2		pF

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V, See 図 7-4	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

6.12 Electrical Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7230C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN at 3 V			1	3	mA
		25 Mbps				7	9.5	
	ISO7231C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN1 at 3 V, EN2 at 3 V			6.5	11	mA
		25 Mbps				11	17	
I_{CC2}	ISO7230C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN at 3 V			9	15	mA
		25 Mbps				10	17	
	ISO7231C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN1 at 3 V, EN2 at 3 V			8	12	mA
		25 Mbps				10.5	16	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		ENx at 0 V, Single channel			0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See 図 7-1	ISO7230	V_{CCO} – 0.4			V
				ISO7231 (5-V side)	V_{CCO} – 0.8			
			I_{OH} = –20 µA, See 図 7-1		V_{CCO} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See 図 7-1				0.4	V
			I_{OL} = 20 µA, See 図 7-1				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		INx at V_{CCI}				10	µA
I_{IL}	Low-level input current		INx at 0 V		–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (2πft), f=2MHz			2		pF
CMTI	Common-mode transient immunity		V_I = V_{CCI} or 0 V, See 図 7-4		25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

6.13 Switching Characteristics: V_{CC1} and V_{CC2} at 3.3-V

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO723xC	See 図 7-1	25		56	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO723xC	See 図 7-1			4	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO723xM	See 図 7-1	8		34	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO723xM	See 図 7-1		1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO723xC				10	ns
		ISO723xM			0	5	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO723xC			0	3	ns
		ISO723xM			0	1	
t_r	Output signal rise time		See 図 7-1		2.4		ns
t_f	Output signal fall time		See 図 7-1		2.3		ns

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See 図 7-2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output				15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				15	25	
t_{fs}	Failsafe output delay time from input power loss		See 図 7-3		18		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, same polarity input on all channels, See 図 7-5		1		ns

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

6.14 Switching Characteristics: V_{CC1} and V_{CC2} at 5-V

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO723xC	See 図 7-1	18		42	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$					2.5	
t_{PLH}, t_{PHL}	Propagation delay	ISO723xM		8		23	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				1	2	
$t_{sk(pp)}$	Part-to-part skew (2)	ISO723xC				8	ns
		ISO723xM			0	3	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO723xC			0	2	ns
		ISO723xM			0	1	
t_r	Output signal rise time		See 図 7-1		2.4		ns
t_f	Output signal fall time				2.3		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See 図 7-2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output				15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				15	25	
t_{fs}	Failsafe output delay time from input power loss		See 図 7-3		12		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See 図 7-5		1		ns

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

6.15 Switching Characteristics: V_{CC1} at 3.3-V and V_{CC2} at 5-V

, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO723xC	See 図 7-1	22		51	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$					3	
t_{PLH}, t_{PHL}	Propagation delay	ISO723xM		8		30	
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				1	2	

, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{sk(pp)}$	Part-to-part skew (2)	ISO723xC				10	ns
		ISO723xM			0	5	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO723xC			0	2.5	ns
		ISO723xM			0	1	
t_r	Output signal rise time		See 図 7-1		2.4		ns
t_f	Output signal fall time				2.3		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See 図 7-2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output				15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				15	25	
t_{fs}	Failsafe output delay time from input power loss		See 図 7-3		12		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See 図 7-5		1		ns

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

6.16 Switching Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay, low-to-high-level output	ISO723xC	See 図 7-1	20		50	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$					3	
t_{PLH}, t_{PHL}	Propagation delay, low-to-high-level output	ISO723xM		8		29	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				1	2	
$t_{sk(pp)}$	Part-to-part skew (2)	ISO723xC				10	ns
		ISO723xM			0	5	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO723xC			0	2.5	ns
		ISO723xM			0	1	
t_r	Output signal rise time		See 図 7-1		2.4		ns
t_f	Output signal fall time				2.3		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See 図 7-2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output				15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				15	25	
t_{fs}	Failsafe output delay time from input power loss		See 図 7-3		18		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See 図 7-5		1		ns

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

6.17 Typical Characteristics

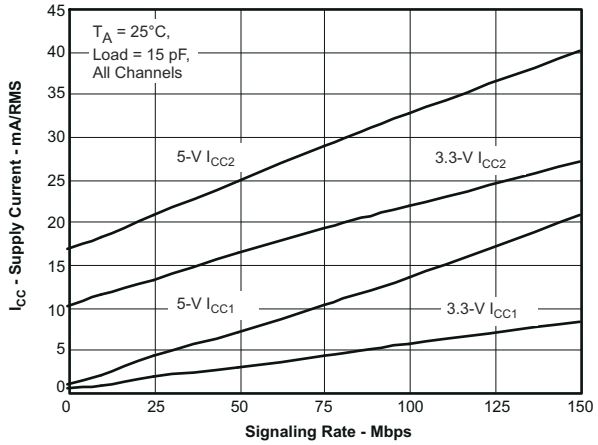


図 6-1. ISO7230C/M RMS Supply Current vs Signaling Rate

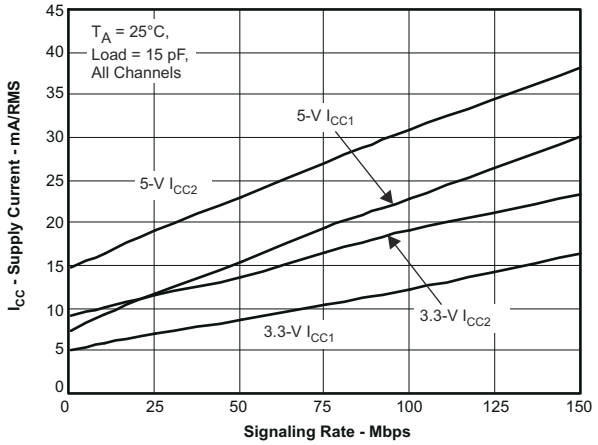


図 6-2. ISO7231C/M RMS Supply Current vs Signaling Rate

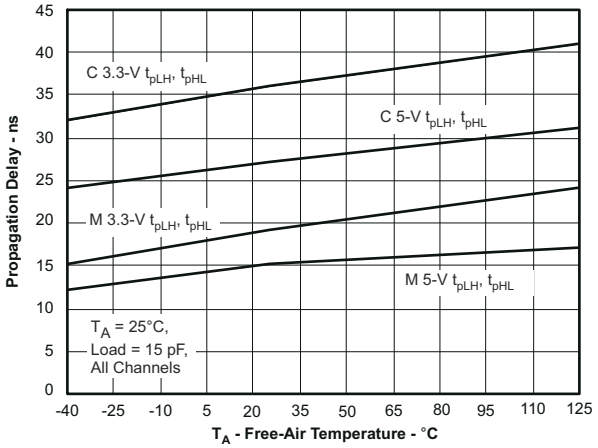


図 6-3. Propagation Delay vs Free-Air Temperature

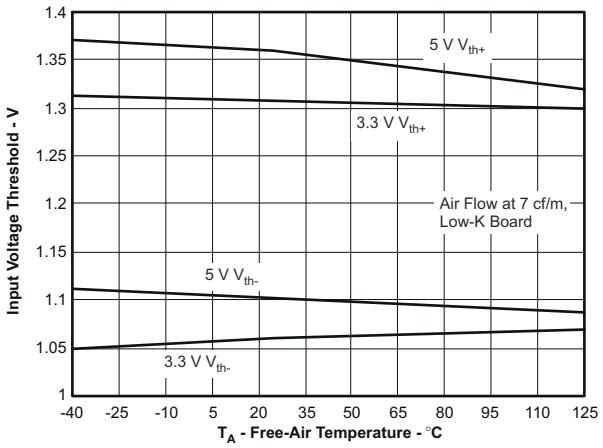


図 6-4. Input Threshold Voltage vs Free-Air Temperature

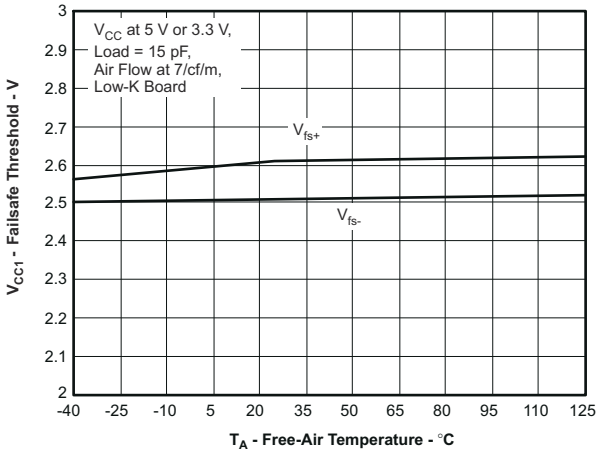


図 6-5. V_{CC1} Fail-Safe Threshold vs Free-Air Temperature

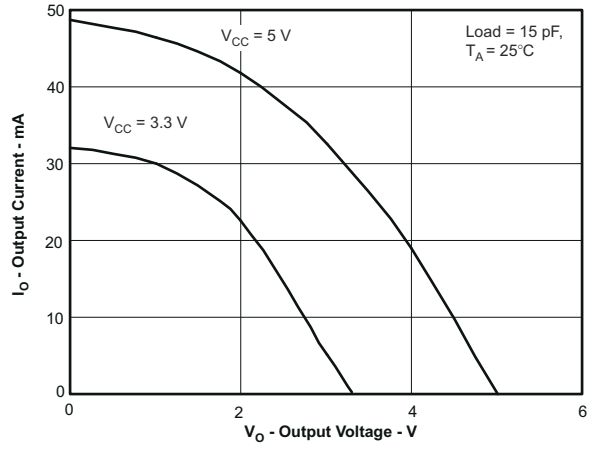


図 6-6. High-Level Output Current vs High-Level Output Voltage

6.17 Typical Characteristics (continued)

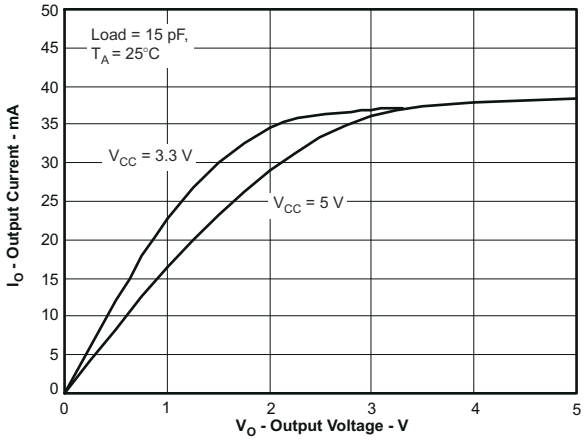
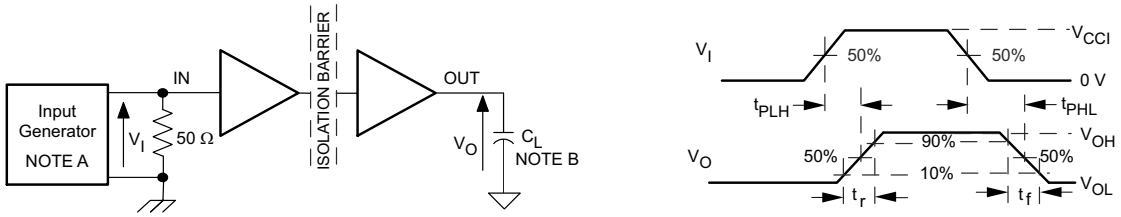


図 6-7. Low-Level Output Current vs Low-Level Output Voltage

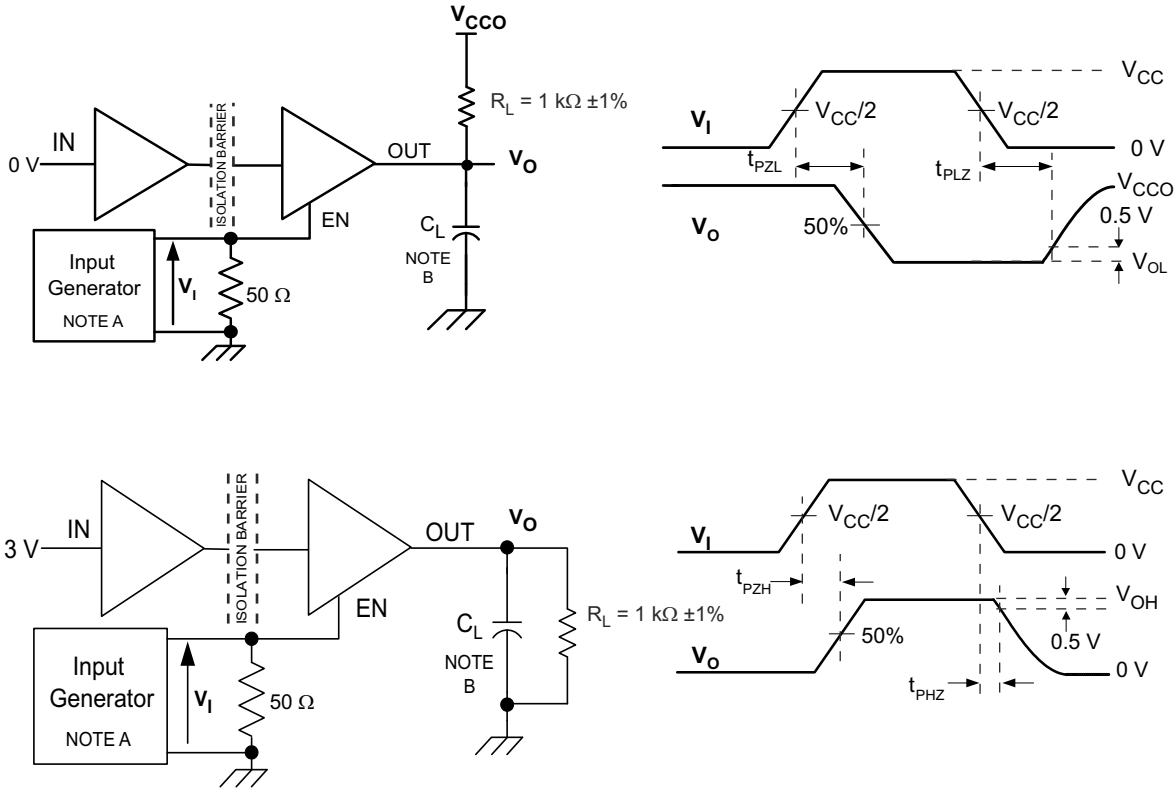
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, tr ≤ 3 ns, tf ≤ 3 ns, ZO = 50 Ω. At the input, a 50-Ω resistor is required to terminate the Input Generator signal. The 50-Ω is not needed in actual application.

B. CL = 15 pF and includes instrumentation and fixture capacitance within ±20%.

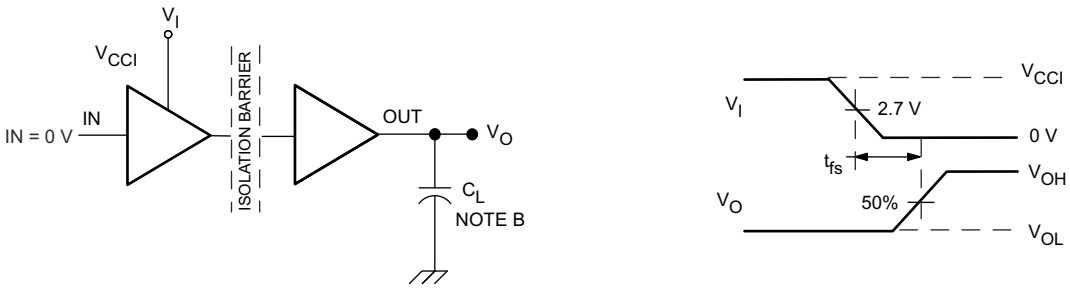
図 7-1. Switching Characteristic Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

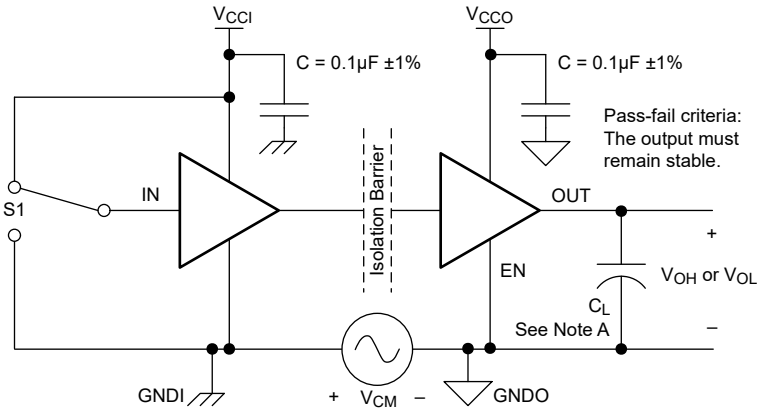
図 7-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

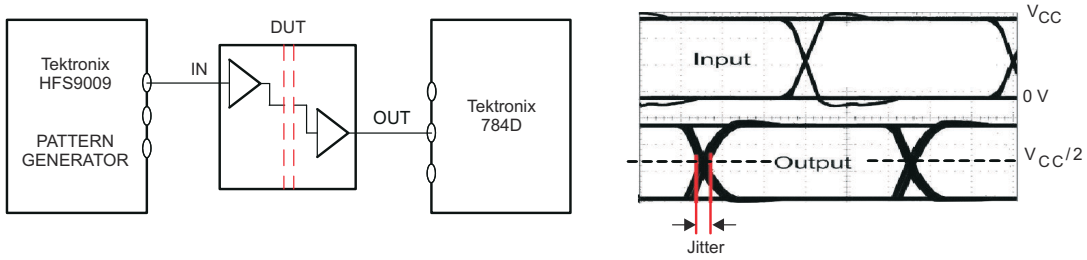
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 7-3. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 7-4. Common-Mode Transient Immunity Test Circuit



PRBS bit pattern run length is 2^{16} – 1. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

図 7-5. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

8 Detailed Description

8.1 Overview

The ISO723x family of devices transmit digital data across a silicon dioxide based isolation barrier. The digital input signal (IN) of the device is sampled by a transmitter and at every data edge the transmitter sends a corresponding differential signal across the isolation barrier. When the input signal is static, the refresh logic periodically sends the necessary differential signal from the transmitter. On the other side of the isolation barrier, the receiver converts the differential signal into a single-ended signal which is output on the OUT pin through a buffer. If the receiver does not receive a data or refresh signal, the timeout logic detects the loss of signal or power from the input side and drives the output to the default level.

8.2 Functional Block Diagram

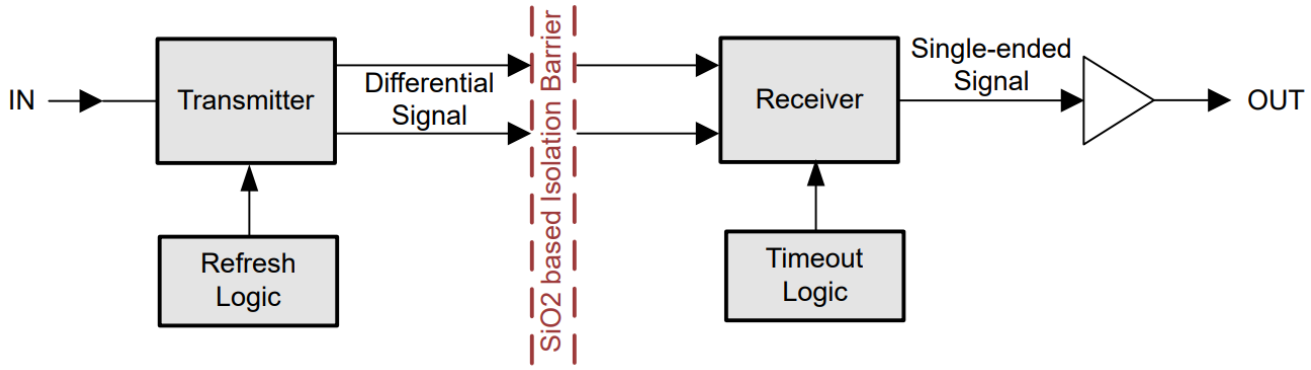


図 8-1. Conceptual Block Diagram of a Digital Isolator

8.3 Feature Description

The ISO724x-Q1 family of devices is available in multiple channel configurations and default output-state options to enable wide variety of application uses. 表 8-1 lists these device features.

表 8-1. Device Features

PRODUCT(1)	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION
ISO7240CF	25 Mbps	≅1.5 V (TTL)	4/0
ISO7241C	25 Mbps	≅1.5 V (TTL)	3/1
ISO7242C	25 Mbps	≅1.5 V (TTL)	2/2

8.4 Device Functional Modes

List of ISO7231C-Q1 functional modes.

表 8-2. Device Function Table ISO7231C-Q1

INPUT V_{CC}	OUTPUT V_{CC}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z
X	PD	X	X	Undetermined

8.4.1 Device I/O Schematics

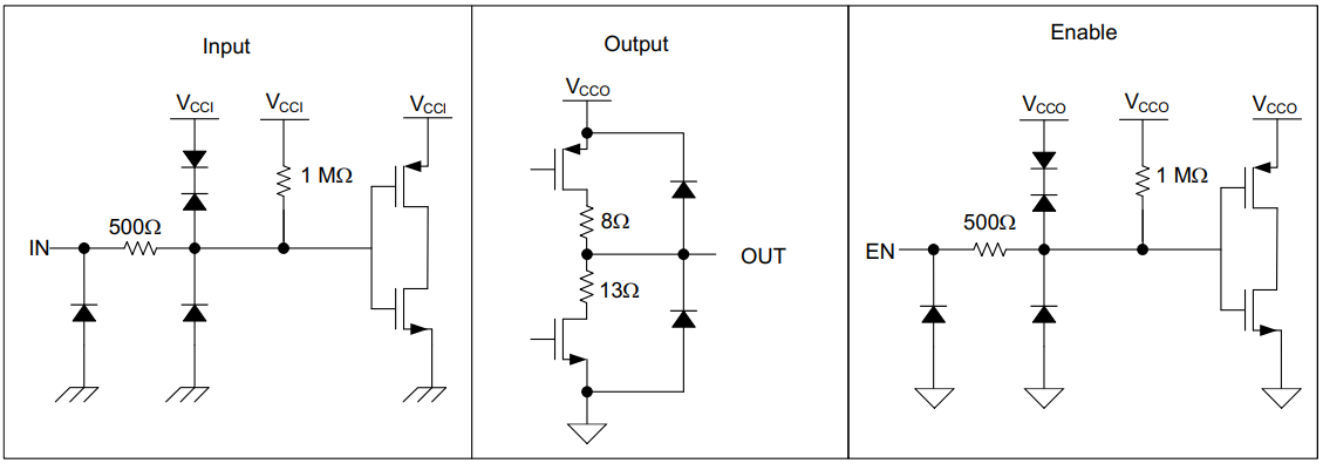


図 8-2. Device I/O Schematics

9 Application and Implementation

注

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9.1 Application Information

ISO723x utilize single-ended TTL or CMOS-logic switching technologies. The supply voltage range is from 3.15 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

ISO7231 combined with Texas Instruments' mixed signal micro-controller, RS-485 transceiver, transformer driver, and voltage regulator can create an isolated RS-485 system as shown in 図 9-1.

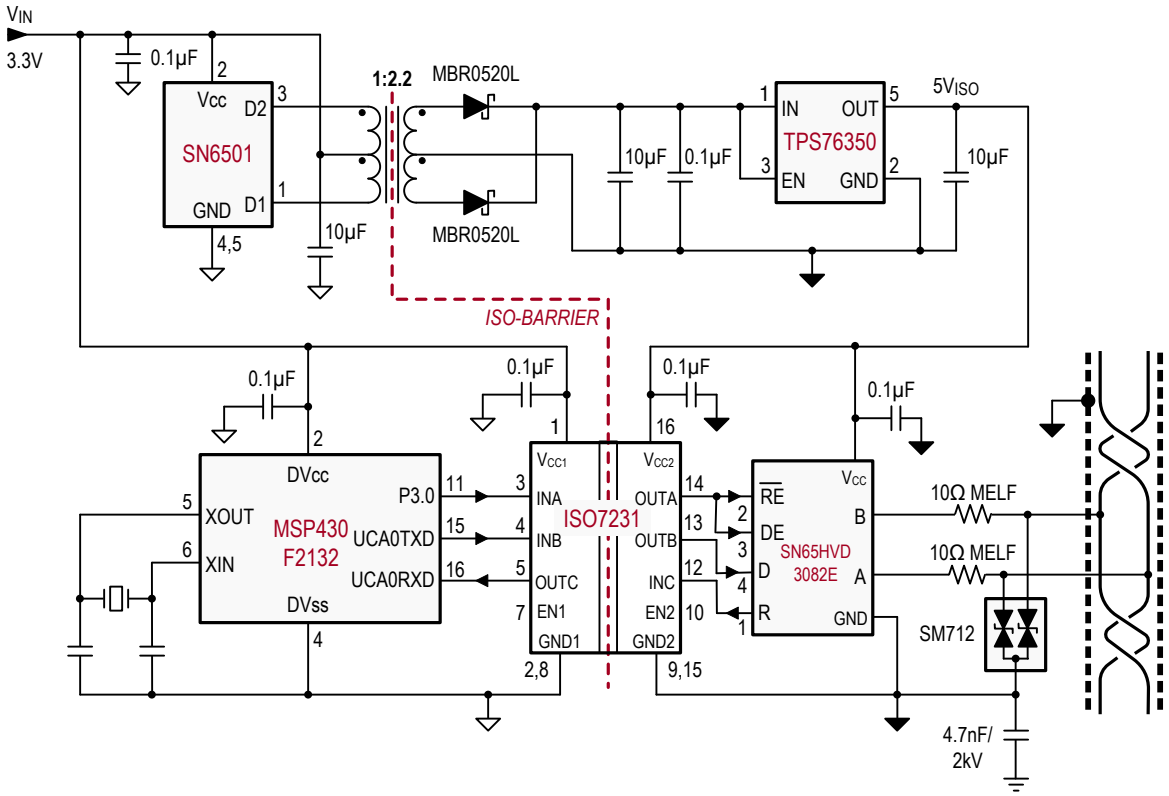

図 9-1. Isolated RS-485 Application Circuit

9.2.1 Design Requirements

Unlike optocouplers, which need external components to improve performance, provide bias, or limit current, ISO723x only needs two external bypass capacitors to operate.

9.2.2 Detailed Design Procedure

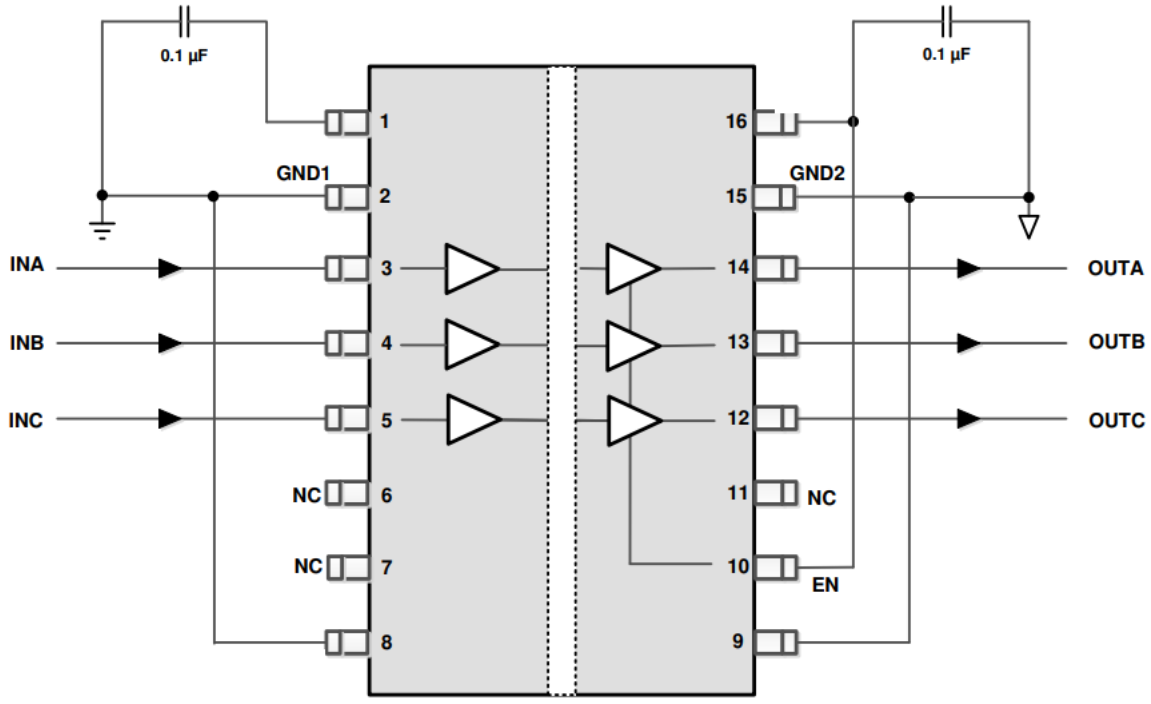

図 9-2. Typical ISO7231-Q1 Circuit Hook-up

9.2.3 Application Performance Plots

9.2.3.1 Insulation Characteristics Curves

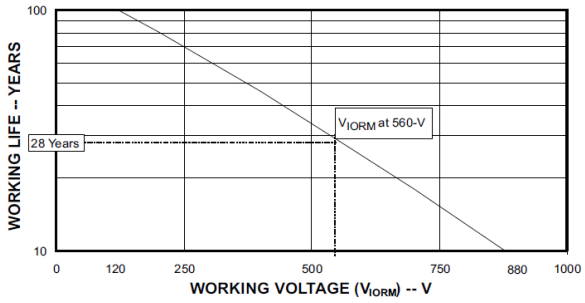

図 9-3. Isolation Lifetime Projection

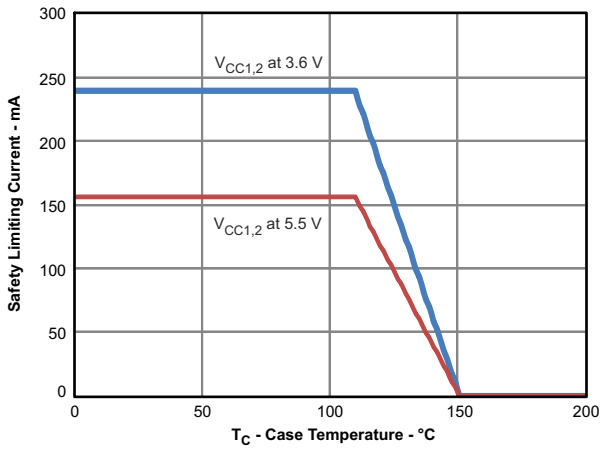

図 9-4. Thermal Derating Curve for Limiting Current per VDE

9.3 Power Supply Recommendations

To provide reliable operation at all data rates and supply voltages, a 0.1 µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments SN6501 data

sheet. For such applications, detailed power supply design and transformer selection recommendations are available in the SN6501 data sheet.

9.4 Layout

9.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 図 9-5). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power/ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly. For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide*.

9.4.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to the lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

9.4.2 Layout Example

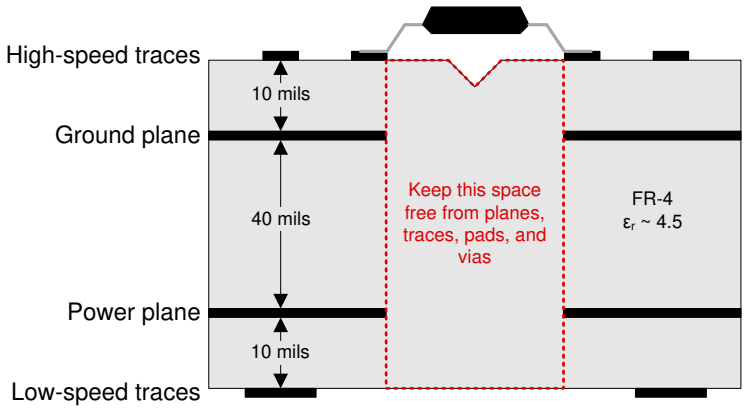

図 9-5. Recommended Layer Stack

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary,* application note
- Texas Instruments, *How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems,* application note
- Texas Instruments, *Digital Isolator Design Guide* application report

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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10.5 静電気放電に関する注意事項

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10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision L (October 2024) to Revision M (February 2025)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• 「*特長*」セクションに、安全関連証明書へのリンクを追加	1

Changes from Revision K (October 2015) to Revision L (October 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• ドキュメント全体で VDE V 0884-11 を DIN VDE 0884-17 に更新	1

- ドキュメント全体を通して容量性絶縁から絶縁バリアに参照を更新 1
- Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations 4
- Updated the *Regulatory Information* table 6
- Updated electrical and switching characteristics to match device performance 6
- Moved the *Insulation Characteristics Curves* to the *Application Curves* section 18

Changes from Revision J (May 2015) to Revision K (October 2015) **Page**

- Added Note 1 to L(I01) and changed the MIN value From: 8.34 To 8 mm in the *Insulation Specifications* table 5
- Added Note 1 to LI02) and changed the MIN value From: 8.1 To 8 mm in the *Insulation Specifications* table 5
- Deleted Note 1 From the *Safety-Related Certifications* table 6
- Changed The ground symbols on the Enable circuit in the Device I/O Schematics images 16

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7230CDW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-40 to 125	ISO7230C
ISO7230CDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7230C
ISO7230CDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7230C
ISO7230CDWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7230C
ISO7230MDW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-40 to 125	ISO7230M
ISO7230MDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7230M
ISO7230MDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7230M
ISO7230MDWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7230M
ISO7231CDW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-40 to 125	ISO7231C
ISO7231CDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231C
ISO7231CDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231C
ISO7231CDWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231C
ISO7231CDWRG4	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231C
ISO7231MDW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-40 to 125	ISO7231M
ISO7231MDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231M
ISO7231MDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231M
ISO7231MDWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231M
ISO7231MDWRG4	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ISO7231C :

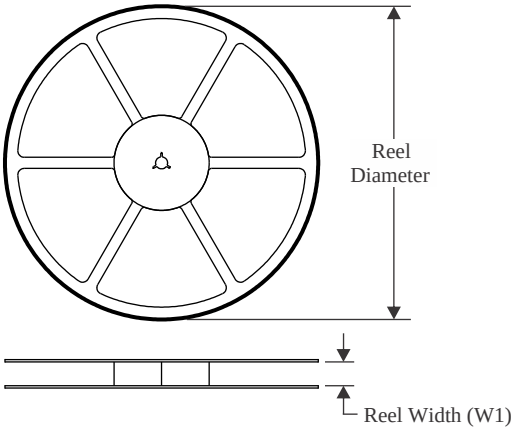
- Automotive : ISO7231C-Q1

NOTE: Qualified Version Definitions:

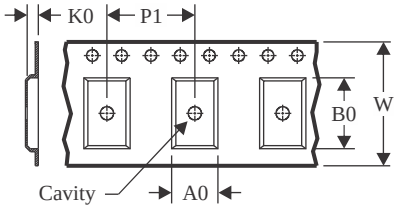
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

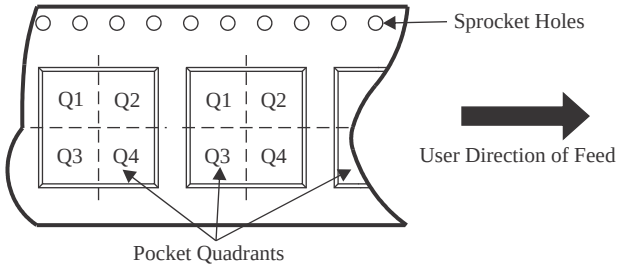


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

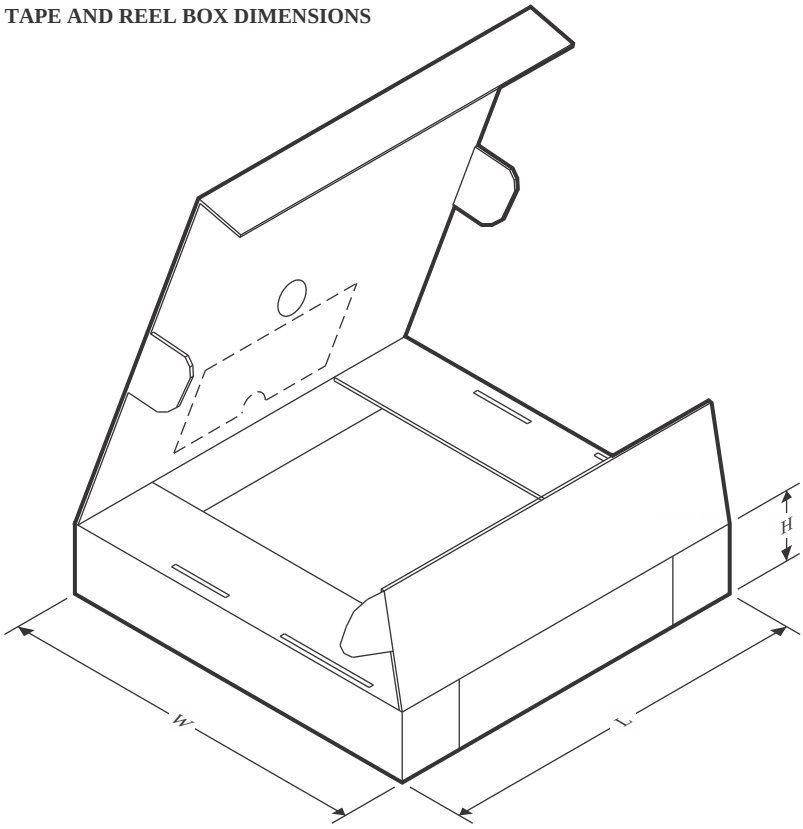
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7230CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7230MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7231CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7231MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7230CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7230MDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7231CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7231MDWR	SOIC	DW	16	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

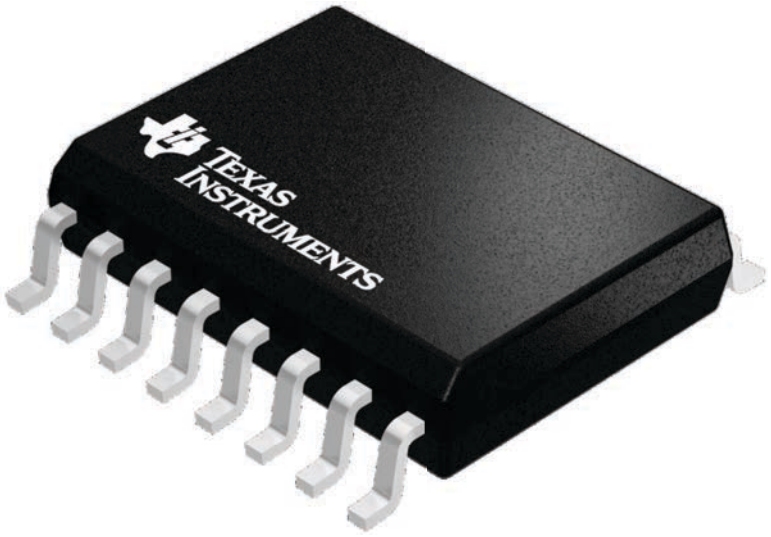
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

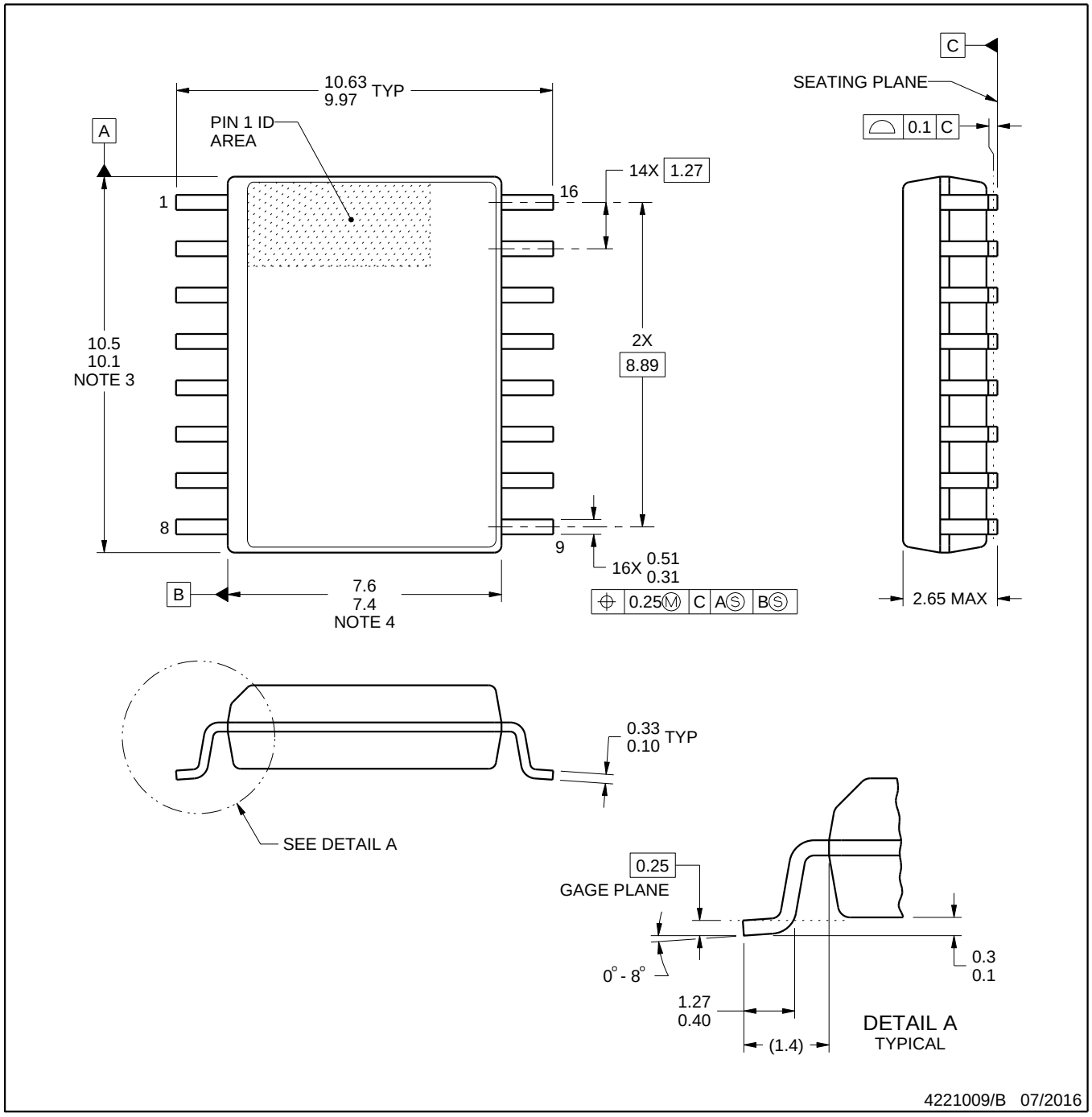
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



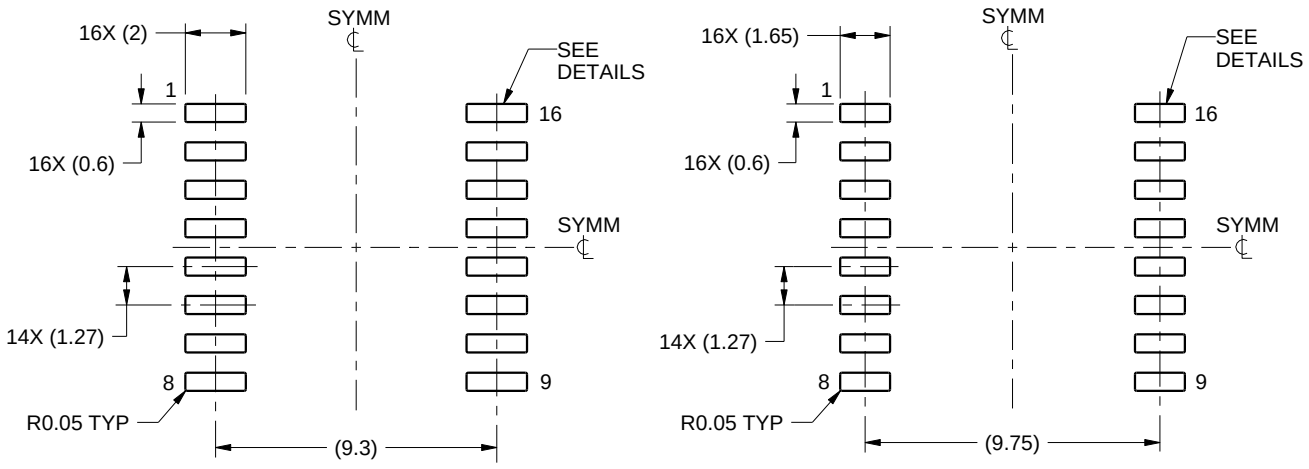
4224780/A

SOIC



NOTES:

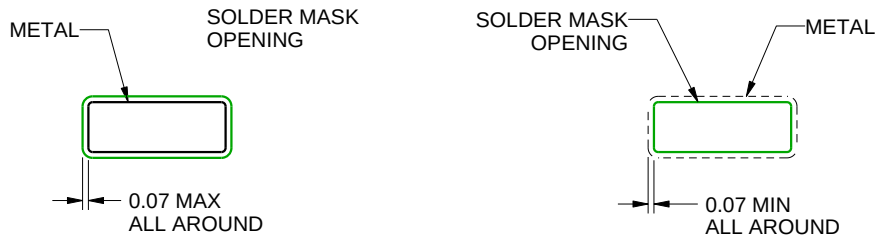
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

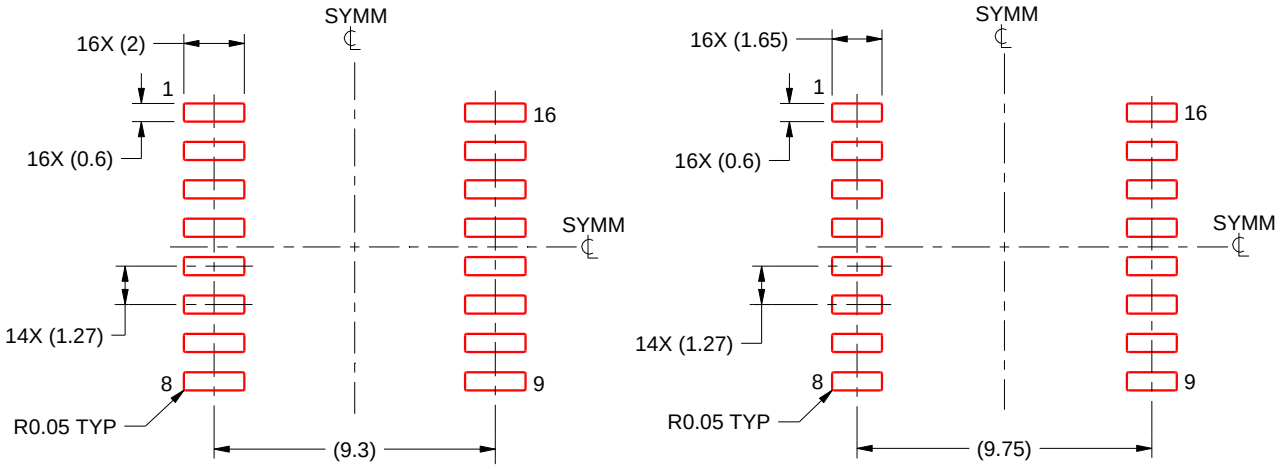
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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