参考資料

ISO5452 高 CMTI 2.5A/5A 絶縁型 IGBT、MOSFET ゲート・ドライバ、分割出力およびアクティブ保護機能搭載

1 特長

- 同相過渡耐圧 (CMTI):50kV/μs (最小値)、100kV/μs (標準値)
  (V_{CM} = 1500V)
- 分割出力により 2.5A のピーク・ソース電流および 5A のピーク・シンク電流を供給
- 短い伝搬遅延:76ns (標準値)、110ns (最大値)
- 2A のアクティブ・ミラー・クランプ
- 出力短絡クランプ
- 短絡時のソフト電源オフ (STO) 機能
- 不飽和化検出時のフォルト・アラームは $\overline{\text{FLT}}$ により通知され、$\overline{\text{RST}}$ によりリセット
- 入出力低電圧誤動作防止 (UVLO):レディ (RDY) ピンによる標示付き
- 低電源またはフローティング入力時の、アクティブ出力プルダウンおよびデフォルト Low 出力
- 入力電源電圧:2.25V～5.5V
- 出力ドライバ供給電圧:15V～30V
- CMOS 互換の入力
- 20ns 未満の入力パルスと過渡ノイズを除去
- 動作温度:-40℃～+125℃ (周囲)
- 絶縁サージ耐久電圧 10000V_{PK}
- 安全関連の認定:
  - 8000V_{PK} V_{IOTM} および 1420V_{PK} V_{IORM} の、DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 準拠の強化絶縁
  - UL1577 準拠で 5700V_{RMS} において 1 分間の絶縁
  - CSA Component Acceptance Notice 5A、IEC-60950-1、および IEC 60601-1 最終機器標準
  - EN 61010-1 および EN 60950-1 準拠の TUV 認定
  - GB4943.1-2011 CQC 認定

2 アプリケーション

- 次のような用途の絶縁型 IGBT および MOSFET ドライブ:
  - 産業用モーター制御ドライブ
  - 産業用電源
  - ソーラー・インバータ
  - HEV および EV の電源モジュール
  - 誘導加熱

3 概要

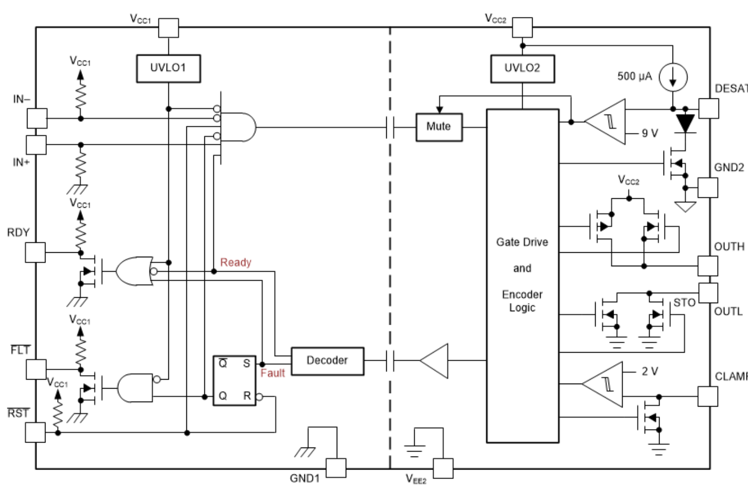
ISO5452 デバイスは、5.7kV_{RMS}、IGBT および MOSFET 用の強化絶縁型ゲート・ドライバで、分割出力の OUTH と OUTL があり、2.5A のソース電流と 5A のシンク電流を供給できます。入力側は、単一の 2.25V～5.5V 電源で動作します。出力側では、最小 15V から最大 30V までの電源電圧範囲が使用できます。
2 つの相補 CMOS 入力により、ゲート・ドライバの出力状態が制御されます。伝搬時間が 76ns と短いため、出力ステージを正確に制御できます。

内部不飽和化 (DESAT) フォルト検出により、IGBT が過電流状況にあることが認識されます。DESAT が検出されると、ミュート・ロジックによりアイソレータの出力がただちにブロックされ、ソフト電源オフ手順が開始されて、OUTH ピンがディセーブルされ、OUTL ピンが 2μs の間 Low になります。
OUTL ピンが、負の方向に最も大きい供給電圧である V_{EE2} との比較で 2V に達すると、ゲート・ドライバ出力が V_{EE2} の電位に強制的に設定され、IGBT はただちにオフになります。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
ISO5452	SOIC (16)	10.30mm × 7.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (January 2017) to Revision C (May 2023)	Page
• Added Additional manufacturing certification pending in the *Safety-Related Certifications* table	8

Changes from Revision A (September 2015) to Revision B (January 2017)	Page
• タイトルを「アクティブ安全機能」から「アクティブ保護機能」に変更	1
• 「特長」の「サージ耐性 10000V_{PK} (IEC 61000-4-5 準拠)」を「絶縁サージ耐久電圧 10000V_{PK}」へ変更	1
• Moved *Insulation Specifications* to the *Specifications* section	7
• Changed R_{IO} Test conditions From: T_S To: T_S = 150°C in *Insulation Specifications*	7
• Moved *Safety-Related Certifications* to the *Specifications* section	8
• Moved *Safety Limiting Values* to the *Specifications* section	8
• Moved *Insulation Characteristics Curves* to the *Specifications*	12
• Added text ", but connecting CLAMP output of the gate driver to the IGBT gate is also not an issue." to *Supply and Active Miller Clamp*	23
• Deleted ground symbol on pin 11 of the *Global Shutdown With Inverting Input Configuration* figure	29
• Deleted ground symbol on pin 11 on the inverting input of the *Auto Reset for Noninverting and Inverting Input Configuration* figure	29

Changes from Revision * (August 2015) to Revision A (September 2015)	Page
• 1 ページの製品プレビューから完全なデータシートへ変更	1
• 「特長」の「同相過渡耐圧 (CMTI):50kV/μs (最小値)、100kV/μs (標準値)..」をリストの先頭に移動	1
• すべての認定のステータスを「完了」に変更	1
• 「機能ブロック図」を変更、ピン OUTL に STO を追加	1
• Changed R_{IO} Test conditions From: 100°C ≤ T_A ≤ max To: 100°C ≤ T_A ≤ 125°C in *Insulation Specifications*	7
• Changed the *Safety-Related Certifications* table	8

5 概要 (続き)

不飽和化がアクティブのとき、絶縁バリアを通してフォルト信号が送信され、入力側の $\overline{FLT}$ 出力が Low になって、アイソレータ入力がブロックされます。ソフト電源オフ期間の間は、ミュート・ロジックがアクティブになります。$\overline{FLT}$ 出力状況はラッチされ、RDY ピンが High に移行した後でのみ、$\overline{RST}$ 入力の Low アクティブ・パルスを使用してリセット可能です。

バイポーラ電源による通常動作時に IGBT がオフになると、出力は V_{EE2} にハード・クランプされます。出力電源がユニポーラの場合、アクティブなミラー・クランプを使用でき、低インピーダンスのパスを通してミラー電流をシンクできるため、高電圧の過渡状況で IGBT が動的にオンになることが防止されます。

ゲート・ドライバの動作準備は、入力側と出力側の電源を監視する 2 つの低電圧誤動作防止回路により制御されます。いずれかの側の電源が不十分な場合は RDY 出力が Low になり、そうでない場合はこの出力が High になります。

ISO5452 は、16 ピンの SOIC パッケージで供給されます。デバイスの動作は、-40℃～+125℃の周囲温度範囲について規定されています。

6 Pin Configuration and Function

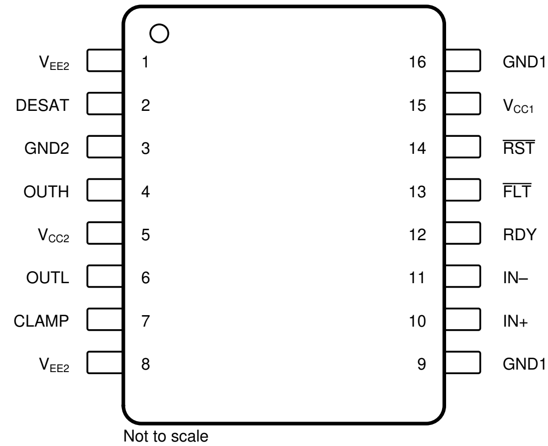


図 6-1. DW Package 16-Pin SOIC Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{EE2}	—	Output negative supply. Connect to GND2 for Unipolar supply application.
2	DESAT	I	Desaturation voltage input
3	GND2	—	Gate drive common. Connect to IGBT emitter.
4	OUTH	O	Positive gate drive voltage output
5	V_{CC2}	—	Most positive output supply potential.
6	OUTL	O	Negative gate drive voltage output
7	CLAMP	O	Miller clamp output
8	V_{EE2}	—	Output negative supply. Connect to GND2 for Unipolar supply application.
9	GND1	—	Input ground
10	IN+	I	Non-inverting gate drive voltage control input
11	IN–	I	Inverting gate drive voltage control input
12	RDY	O	Power-good output, active high when both supplies are good.
13	$\overline{FLT}$	O	Fault output, low-active during DESAT condition
14	$\overline{RST}$	I	Reset input, apply a low pulse to reset fault latch.
15	V_{CC1}	—	Positive input supply (2.25 V to 5.5 V)
16	GND1	—	Input ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CC1}	Supply voltage input side		GND1 – 0.3	6	V
V_{CC2}	Positive supply voltage output side	$(V_{CC2} – GND2)$	–0.3	35	V
V_{EE2}	Negative supply voltage output side	$(V_{EE2} – GND2)$	–17.5	0.3	V
$V_{(SUP2)}$	Total supply output voltage	$(V_{CC2} – V_{EE2})$	–0.3	35	V
$V_{(OUTH)}$	Positive gate driver output voltage		V_{EE2} – 0.3	V_{CC2} + 0.3	V
$V_{(OUTL)}$	Negative gate driver output voltage		V_{EE2} – 0.3	V_{CC2} + 0.3	V
$I_{(OUTH)}$	Gate driver high output current	Gate driver high output current (maximum pulse width = 10 µs, maximum duty cycle = 0.2%)		2.7	A
$I_{(OUTL)}$	Gate driver low output current	Gate driver high output current (maximum pulse width = 10 µs, maximum duty cycle = 0.2%)		5.5	A
$V_{(LIP)}$	Voltage at IN+, IN–, $\overline{FLT}$, RDY, $\overline{RST}$		GND1 - 0.3	V_{CC1} + 0.3	V
$I_{(LOP)}$	Output current of $\overline{FLT}$, RDY			10	mA
$V_{(DESAT)}$	Voltage at DESAT		GND2 - 0.3	V_{CC2} + 0.3	V
$V_{(CLAMP)}$	Clamp voltage		V_{EE2} – 0.3	V_{CC2} + 0.3	V
T_J	Junction temperature		–40	150	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage input side	2.25		5.5	V
V_{CC2}	Positive supply voltage output side $(V_{CC2} – GND2)$	15		30	V
V_{EE2}	Negative supply voltage output side $(V_{EE2} – GND2)$	–15		0	V
$V_{(SUP2)}$	Total supply voltage output side $(V_{CC2} – V_{EE2})$	15		30	V
V_{IH}	High-level input voltage (IN+, IN–, $\overline{RST}$)	0.7 × V_{CC1}		V_{CC1}	V
V_{IL}	Low-level input voltage (IN+, IN–, $\overline{RST}$)	0		0.3 × V_{CC1}	V
t_{UI}	Pulse width at IN+, IN– for full output (C_{LOAD} = 1 nF)	40			ns
t_{RST}	Pulse width at $\overline{RST}$ for resetting fault latch	800			ns
T_A	Ambient temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[(1)]		ISO5452 DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

7.5 Power Ratings

V_{CC1} = 5.5 V, V_{CC2} = 30 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation[(1)]				1255	mW
P_{ID}	Maximum input power dissipation				175	mW
P_{OD}	Maximum output power dissipation				1080	mW

(1) Full chip power dissipation is derated 10.04 mW/°C beyond 25°C ambient temperature. At 125°C ambient temperature, a maximum of 251 mW total power dissipation is allowed. Power dissipation can be optimized depending on ambient temperature and board design, while ensuring that Junction temperature does not exceed 150°C.

7.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	μm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category (according to IEC 60664-1)	Rated Mains Voltage ≤ 300 V_{RMS}	I-IV	
		Rated Mains Voltage ≤ 600 V_{RMS}	I-III	
		Rated Mains Voltage ≤ 1000 V_{RMS}	I-II	
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1420	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage. Time dependent dielectric breakdown (TDDB) Test, see 図 7-1	1000	V_{RMS}
		DC voltage	1420	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification), t = 1 s (100% production)	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50 μs waveform, V_{TEST} = 1.6 × V_{IOSM} = 10000 V_{PK} (qualification)(3)	6250	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM} = 1704 V_{PK}, t_m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM} = 2272 V_{PK}, t_m = 10 s	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)}$ = 1.875× V_{IORM} = 2663 V_{PK}, t_m = 10 s	≤5	
R_{IO}	Isolation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	Ω
		V_{IO} = 500 V at T_S = 150°C	> 10^9	Ω
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 x sin (2πft), f = 1 MHz	~1	pF
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstanding Isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO} = 6840 V_{RMS}, t = 1 s (100% production)	5700	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for basic electrical insulation only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device

7.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 60950-1 (VDE 0805 Teil 1):2011-01	Certified according to CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/ A1:2010/ A12:2011/A2:2013
Reinforced Insulation Maximum Transient isolation voltage, 8000 V_{PK}; Maximum surge isolation voltage, 6250 V_{PK}, Maximum repetitive peak isolation voltage, 1420 V_{PK}	Isolation Rating of 5700 V_{RMS}; Reinforced insulation per CSA 60950- 1- 07+A1+A2 and IEC 60950-1 (2nd Ed.), 800 V_{RMS} max working voltage (pollution degree 2, material group I) ; 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V_{RMS} (354 V_{PK}) max working voltage	Single Protection, 5700 V_{RMS}	Reinforced Insulation, Altitude ≤ 5000m, Tropical climate, 400 V_{RMS} maximum working voltage	5700 V_{RMS} Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V_{RMS} 5700 V_{RMS} Reinforced insulation per EN 60950-1:2006/A11:2009/ A1:2010/ A12:2011/A2:2013 up to working voltage of 800 V_{RMS}
Certification completed Certificate number: 40040142	Certification completed Master contract number: 220991	Certification completed File number: E181974	Certification completed Certificate number: CQC16001141761 Additional manufacturing certification pending	Certification completed Client ID number: 77311

7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output or supply current	$R_{\theta JA}$ = 99.6°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see 図 7-2			456	mA
		$R_{\theta JA}$ = 99.6°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see 図 7-2			346	
		$R_{\theta JA}$ = 99.6°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see 図 7-2			228	
		$R_{\theta JA}$ = 99.6°C/W, V_I = 15 V, T_J = 150°C, T_A = 25°C, see 図 7-2			484	
		$R_{\theta JA}$ = 99.6°C/W, V_I = 30 V, T_J = 150°C, T_A = 25°C, see 図 7-2			42	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 99.6°C/W, T_J = 150°C, T_A = 25°C, see 図 7-3			1255(1)	mW
T_S	Safety temperature				150	°C

(1) Input, output, or the sum of input and output power should not exceed this value

The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *セクション 7.4* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

7.9 Electrical Characteristics

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE SUPPLY						
$V_{IT+(UVLO1)}$	Positive-going UVLO1 threshold voltage input side (V_{CC1} – GND1)				2.25	V
$V_{IT-(UVLO1)}$	Negative-going UVLO1 threshold voltage input side (V_{CC1} – GND1)		1.7			V
$V_{HYS(UVLO1)}$	UVLO1 Hysteresis voltage (V_{IT+} – V_{IT-}) input side	T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		0.2		V
$V_{IT+(UVLO2)}$	Positive-going UVLO2 threshold voltage output side (V_{CC2} – GND2)				13	V
		T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		12		
$V_{IT-(UVLO2)}$	Negative-going UVLO2 threshold voltage output side (V_{CC2} – GND2)		9.5			V
		T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		11		
$V_{HYS(UVLO2)}$	UVLO2 Hysteresis voltage (V_{IT+} – V_{IT-}) output side	T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		1		V
I_{Q1}	Input supply quiescent current				4.5	mA
		T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		2.8		
I_{Q2}	Output supply quiescent current				6	mA
		T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		3.6		
LOGIC I/O						
$V_{IT+(IN, \overline{RST})}$	Positive-going input threshold voltage (IN+, IN–, $\overline{\text{RST}}$)				0.7 × V_{CC1}	V
$V_{IT-(IN, \overline{RST})}$	Negative-going input threshold voltage (IN+, IN–, $\overline{\text{RST}}$)		0.3 × V_{CC1}			V
$V_{HYS(IN, \overline{RST})}$	Input hysteresis voltage (IN+, IN–, $\overline{\text{RST}}$)	T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		0.15 × V_{CC1}		V
I_{IH}	High-level input leakage at (IN+) [(1)]	IN+ = V_{CC1}, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		100		µA
I_{IL}	Low-level input leakage at (IN–, $\overline{\text{RST}}$)[(2)]	IN– = GND1, $\overline{\text{RST}}$ = GND1, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		–100		µA
I_{PU}	Pullup current of $\overline{\text{FLT}}$, RDY	$V_{(RDY)}$ = GND1, $V_{(FLT)}$ = GND1, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		100		µA
V_{OL}	Low-level output voltage at $\overline{\text{FLT}}$, RDY	$I_{(FLT)}$ = 5 mA			0.2	V
GATE DRIVER STAGE						
$V_{(OUTPD)}$	Active output pulldown voltage	$I_{(OUTH/L)}$ = 200 mA, V_{CC2} = open			2	V
$V_{(OUTH)}$	High-level output voltage	$I_{(OUTH)}$ = –20 mA	V_{CC2} – 0.5			V
		$I_{(OUTH)}$ = –20 mA, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		V_{CC2} – 0.24		
$V_{(OUTL)}$	Low-level output voltage	$I_{(OUTL)}$ = 20 mA			V_{EE2} + 50	mV
		$I_{(OUTL)}$ = 20 mA, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		V_{EE2} + 13		
$I_{(OUTH)}$	High-level output peak current	IN+ = high, IN– = low, $V_{(OUTH)}$ = V_{CC2} – 15 V	1.5			A
		IN+ = high, IN– = low, $V_{(OUTH)}$ = V_{CC2} – 15 V, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		2.5		
$I_{(OUTL)}$	Low-level output peak current	IN+ = low, IN– = high, $V_{(OUTL)}$ = V_{EE2} + 15 V	3.4			A
		IN+ = low, IN– = high, $V_{(OUTL)}$ = V_{EE2} + 15 V, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		5		
$I_{(OLF)}$	Low level output current during fault condition	T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		130		mA

7.9 Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACTIVE MILLER CLAMP						
$V_{(CLP)}$	Low-level clamp voltage	$I_{(CLP)}$ = 20 mA			V_{EE2} + 0.08	V
		$I_{(CLP)}$ = 20 mA, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		V_{EE2} + 0.015		
$I_{(CLP)}$	Low-level clamp current	$V_{(CLAMP)}$ = V_{EE2} + 2.5 V	1.6		3.3	A
		$V_{(CLAMP)}$ = V_{EE2} + 2.5 V, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		2.5		
$V_{(CLTH)}$	Clamp threshold voltage		1.6		2.5	V
		T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		2.1		
SHORT CIRCUIT CLAMPING						
$V_{(CLP\_OUTH)}$	Clamping voltage (V_{OUTH} – V_{CC2})	IN+ = high, IN– = low, t_{CLP} = 10 µs, $I_{(OUTH)}$ = 500 mA		1.1	1.3	V
		IN+ = high, IN– = low, t_{CLP} = 10 µs, $I_{(OUTH)}$ = 500 mA, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V				
$V_{(CLP\_OUTL)}$	Clamping voltage (V_{OUTL} – V_{CC2})	IN+ = high, IN– = low, t_{CLP} = 10 µs, $I_{(OUTL)}$ = 500 mA		1.3	1.5	V
		IN+ = high, IN– = low, t_{CLP} = 10 µs, $I_{(OUTL)}$ = 500 mA, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V				
$V_{(CLP\_CLAMP)}$	Clamping voltage (V_{CLP} – V_{CC2})	IN+ = high, IN– = low, t_{CLP} = 10 µs, $I_{(CLP)}$ = 500 mA, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		1.3		V
	Clamping voltage at CLAMP	IN+ = High, IN– = Low, $I_{(CLP)}$ = 20 mA			1.1	V
		IN+ = High, IN– = Low, $I_{(CLP)}$ = 20 mA, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		0.7		
$V_{(CLP\_OUTL)}$	Clamping voltage at OUTL (V_{CLP} - V_{CC2})	IN+ = High, IN– = Low, $I_{(OUTL)}$ = 20 mA			1.1	V
		IN+ = High, IN– = Low, $I_{(OUTL)}$ = 20 mA, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		0.7		
DESAT PROTECTION						
$I_{(CHG)}$	Blanking capacitor charge current	$V_{(DESAT)}$ – GND2 = 2 V	0.42		0.58	mA
		$V_{(DESAT)}$ – GND2 = 2 V, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		0.5		
$I_{(DCHG)}$	Blanking capacitor discharge current	$V_{(DESAT)}$ – GND2 = 6 V	9			mA
		$V_{(DESAT)}$ – GND2 = 6 V, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		14		
$V_{(DSTH)}$	DESAT threshold voltage with respect to GND2		8.3		9.5	V
		T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		9		
$V_{(DSL)}$	DESAT voltage with respect to GND2, when OUTH/L is driven low		0.4		1	V

(1) I_{IH} for IN–, $\overline{RST}$ pin is zero as they are pulled high internally.
(2) I_{IL} for IN+ is zero, as it is pulled low internally.

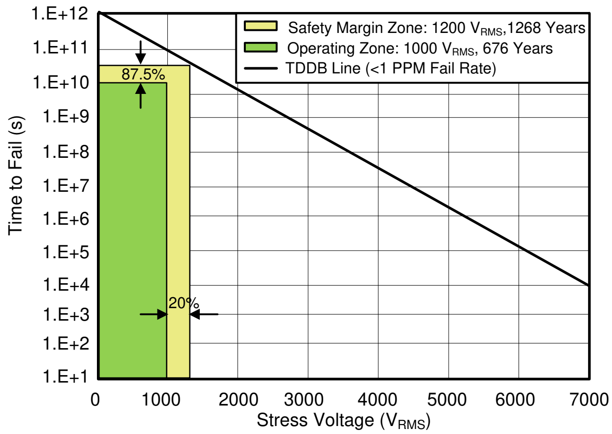
7.10 Switching Characteristics

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time, see 図 8-1, 図 8-2, and 図 8-3	C_{LOAD} = 1 nF	12		35	ns
		C_{LOAD} = 1 nF, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		18		
t_f	Output signal fall time, see 図 8-1, 図 8-2, and 図 8-3	C_{LOAD} = 1 nF	12		37	ns
		C_{LOAD} = 1 nF, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		20		
t_{PLH}, t_{PHL}	Propagation delay, see 図 8-1, 図 8-2, and 図 8-3	C_{LOAD} = 1 nF		76	110	ns
		C_{LOAD} = 1 nF, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V				
t_{sk-p}	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$, see 図 8-1, 図 8-2, and 図 8-3	C_{LOAD} = 1 nF			20	ns
t_{sk-pp}	Part-to-part skew, see 図 8-1, 図 8-2, and 図 8-3	C_{LOAD} = 1 nF			30(1)	ns
t_{GF}	Glitch filter on IN+, IN–, $\overline{RST}$, see 図 8-1, 図 8-2, and 図 8-3	C_{LOAD} = 1 nF	20		40	ns
		C_{LOAD} = 1 nF, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		30		
$t_{DS\,(90\%)}$	DESAT sense to 90% $V_{OUTH/L}$ delay, see 図 8-1, 図 8-2, and 図 8-3	C_{LOAD} = 10 nF			760	ns
		C_{LOAD} = 10 nF, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		553		
$t_{DS\,(10\%)}$	DESAT sense to 10% $V_{OUTH/L}$ delay, see 図 8-1, 図 8-2, and 図 8-3	C_{LOAD} = 10 nF			3.5	µs
		C_{LOAD} = 10 nF, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		2		
$t_{DS\,(GF)}$	DESAT glitch filter delay	C_{LOAD} = 1 nF, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		330		ns
$t_{DS\,(\overline{FLT})}$	DESAT sense to $\overline{FLT}$-low delay, see 図 8-3				1.4	µs
t_{LEB}	Leading edge blanking time, see 図 8-1and 図 8-2		310		480	ns
		T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		400		
$t_{GF(RSTFLT)}$	Glitch filter on $\overline{RST}$ for resetting $\overline{FLT}$		300		800	ns
C_I	Input capacitance(2)	$V_I = V_{CC1} / 2 + 0.4 \times \sin(2\pi ft)$, f = 1 MHz, V_{CC1} = 5 V, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		2		pF
CMTI	Common-mode transient immunity, see 図 8-4	V_{CM} = 1500 V	50			kV/µs
		V_{CM} = 1500 V, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} – GND2 = 15 V, GND2 – V_{EE2} = 8 V		100		

(1) Measured at same supply voltage and temperature condition
(2) Measured from input pin to ground.

7.11 Insulation Characteristics Curves



T_A up to 150°C   Stress-voltage frequency = 60 Hz

図 7-1. Reinforced Isolation Capacitor Lifetime Projection

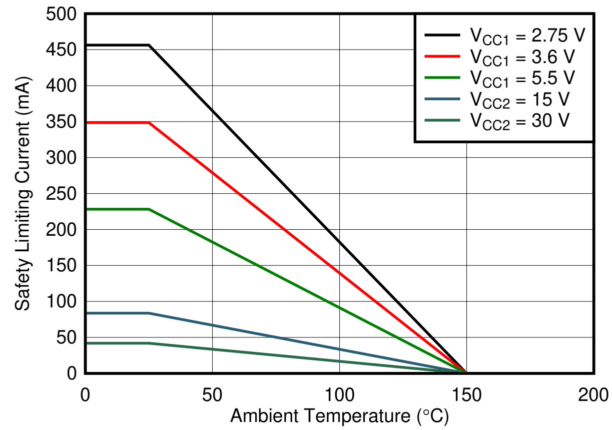


図 7-2. Thermal Derating Curve for Safety Limiting Current per VDE

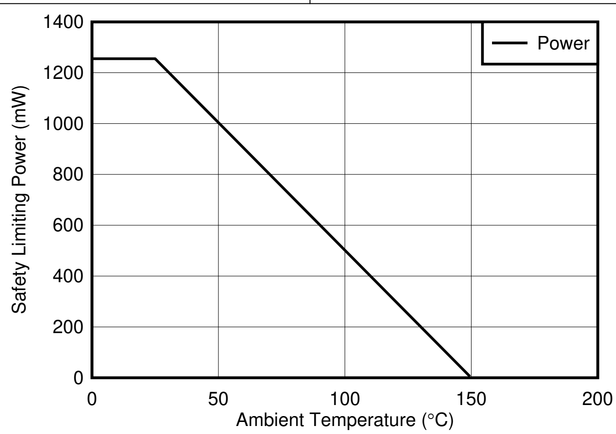


図 7-3. Thermal Derating Curve for Safety Limiting Power per VDE

7.12 Typical Characteristics

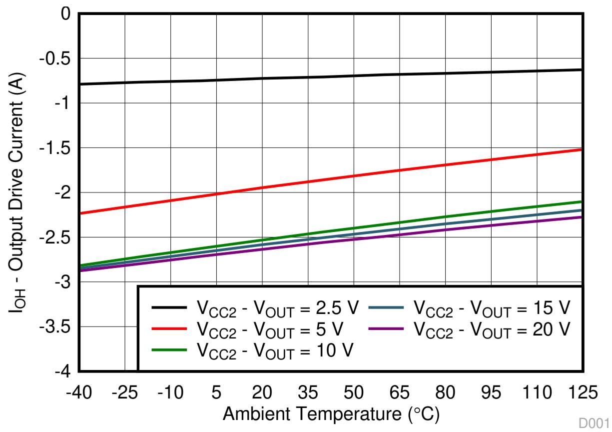


図 7-4. Output High Drive Current vs Temperature

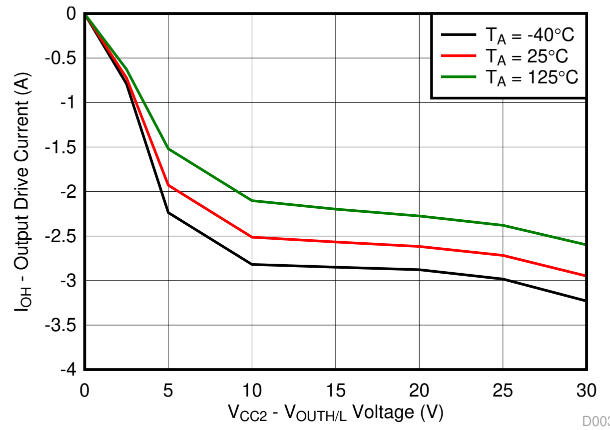


図 7-5. Output High Drive Current vs Output Voltage

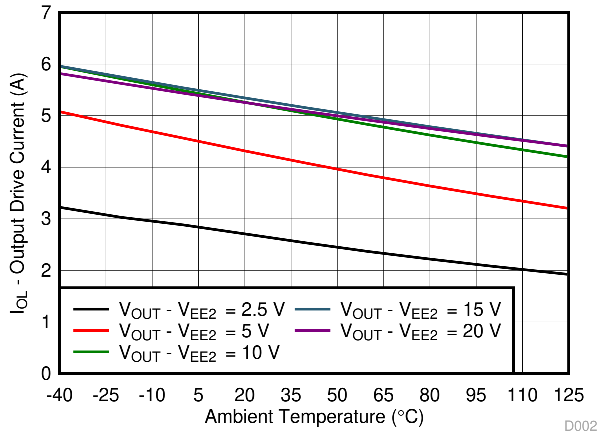


図 7-6. Output Low Drive Current vs Temperature

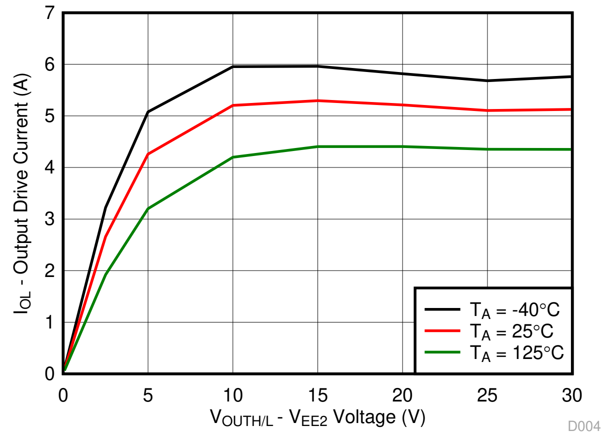
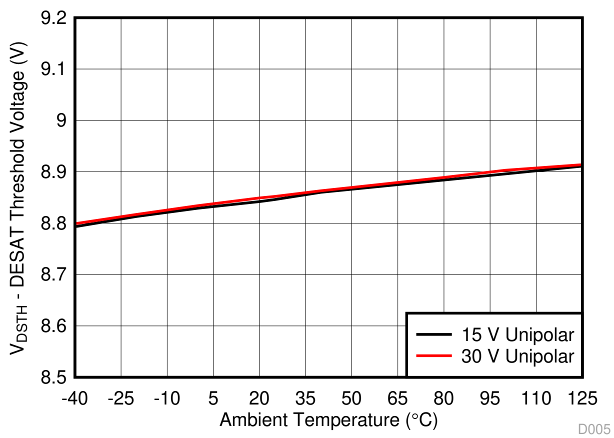


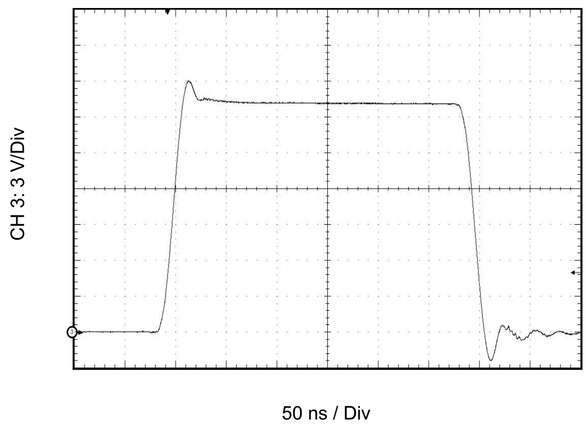
図 7-7. Output Low Drive Current vs Output Voltage



Unipolar: $V_{CC2} – V_{EE2} = V_{CC2} – GND2$

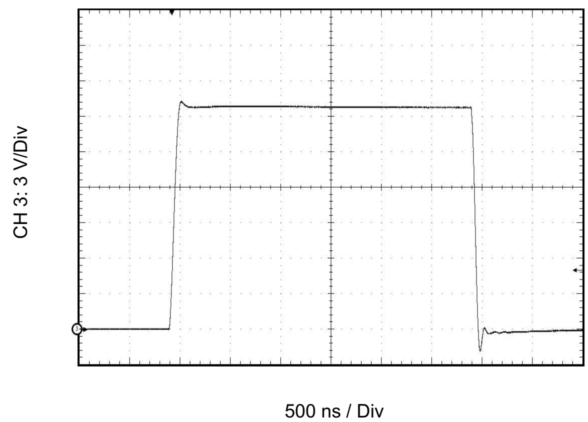
図 7-8. DESAT Threshold Voltage vs Temperature

7.12 Typical Characteristics (continued)



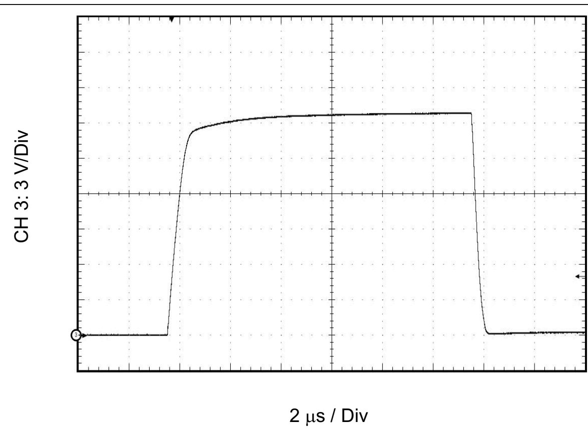
C_L = 1 nF R_{GH} = 0 Ω R_{GL} = 0 Ω
$V_{CC2} – V_{EE2} = V_{CC2}$ – GND2 = 20 V

図 7-9. Output Transient Waveform



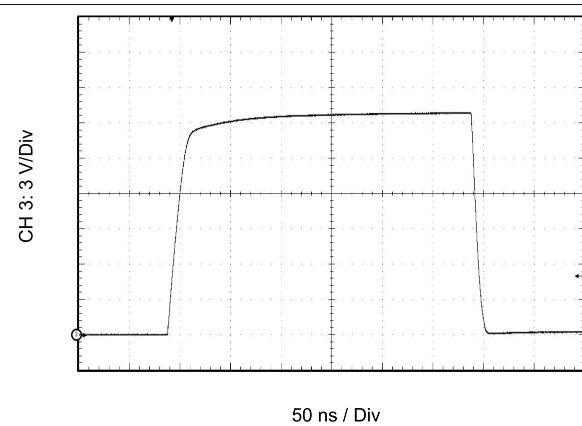
C_L = 10 nF R_{GH} = 0 Ω R_{GL} = 0 Ω
$V_{CC2} – V_{EE2} = V_{CC2}$ – GND2 = 20 V

図 7-10. Output Transient Waveform



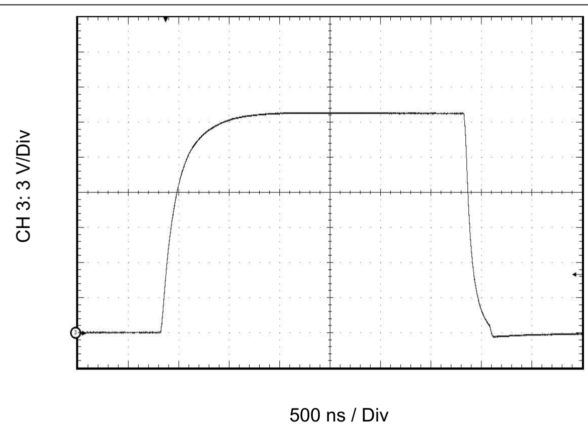
C_L = 100 nF R_{GH} = 0 Ω R_{GL} = 0 Ω
$V_{CC2} – V_{EE2} = V_{CC2}$ – GND2 = 20 V

図 7-11. Output Transient Waveform



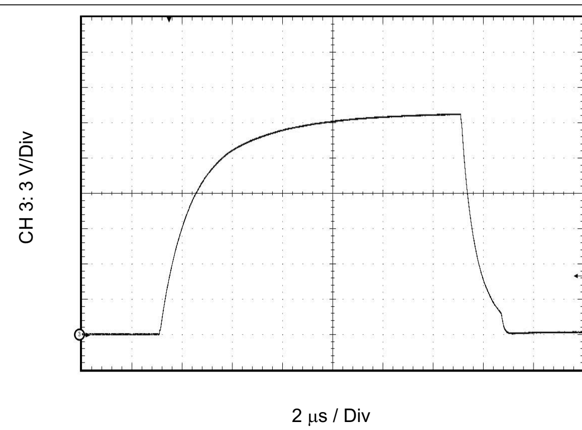
C_L = 1 nF R_{GH} = 10 Ω R_{GL} = 5Ω
$V_{CC2} – V_{EE2} = V_{CC2}$ – GND2 = 20 V

図 7-12. Output Transient Waveform



C_L = 10 nF R_{GH} = 10 Ω R_{GL} = 5Ω
$V_{CC2} – V_{EE2} = V_{CC2}$ – GND2 = 20 V

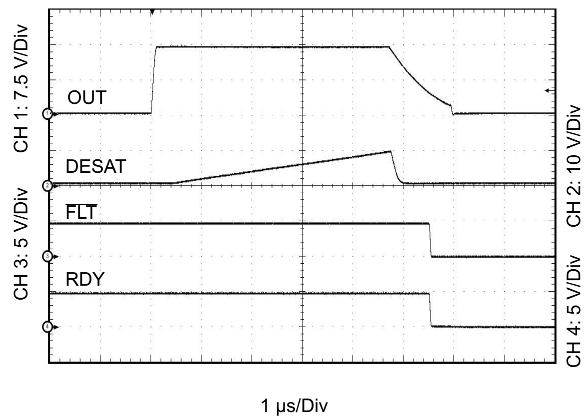
図 7-13. Output Transient Waveform



C_L = 100 nF R_{GH} = 10 Ω R_{GL} = 5Ω
$V_{CC2} – V_{EE2} = V_{CC2}$ – GND2 = 20 V

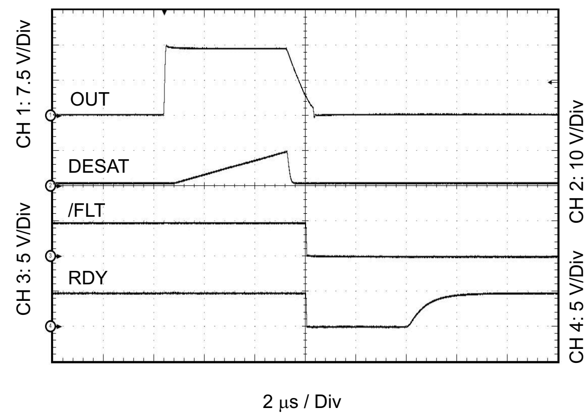
図 7-14. Output Transient Waveform

7.12 Typical Characteristics (continued)



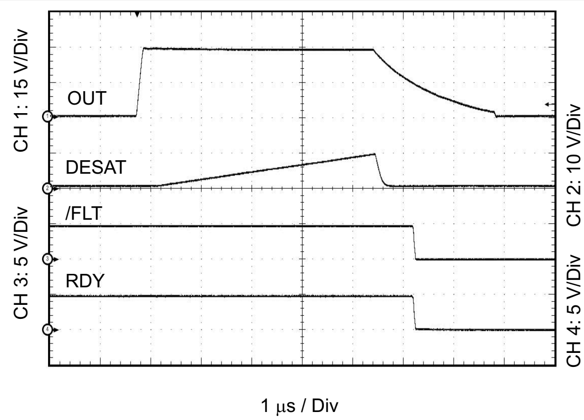
C_L = 10 nF R_{GH} = 0 Ω R_{GL} = 0 Ω
$V_{CC2} – V_{EE2} = V_{CC2}$ – GND2 = 15 V DESAT = 220pF

図 7-15. Output Transient Waveform DESAT, RDY and $\overline{FLT}$



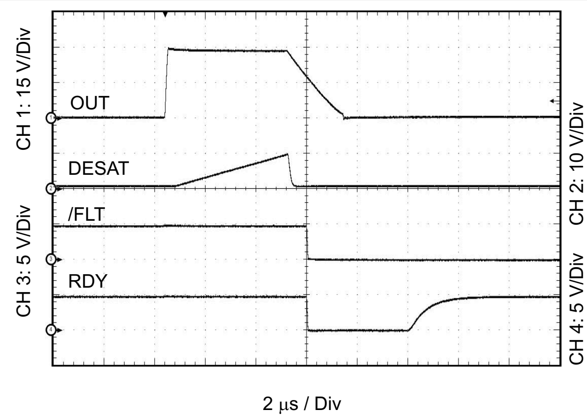
C_L = 10 nF R_{GH} = 0 Ω R_{GL} = 0 Ω
$V_{CC2} – V_{EE2} = V_{CC2}$ – GND2 = 15 V DESAT = 220pF

図 7-16. Output Transient Waveform DESAT, RDY and $\overline{FLT}$



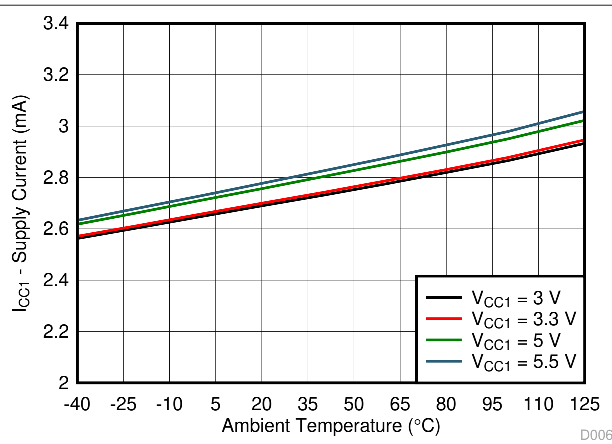
C_L = 10 nF R_{GH} = 0 Ω R_{GL} = 0 Ω
$V_{CC2} – V_{EE2} = V_{CC2}$ – GND2 = 30 V DESAT = 220pF

図 7-17. Output Transient Waveform DESAT, RDY and $\overline{FLT}$



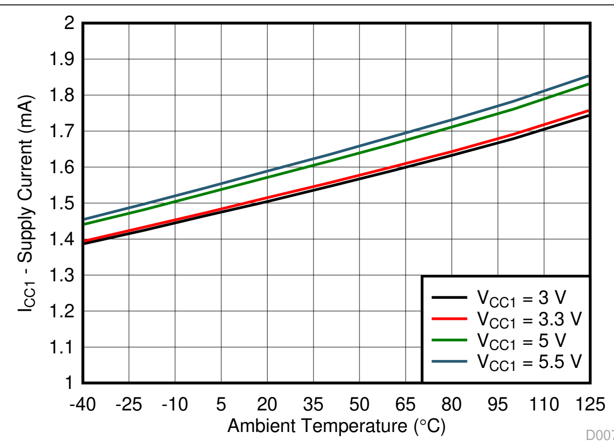
C_L = 10 nF R_{GH} = 0 Ω R_{GL} = 0 Ω
$V_{CC2} – V_{EE2} = V_{CC2}$ – GND2 = 30 V DESAT = 220pF

図 7-18. Output Transient Waveform DESAT, RDY and $\overline{FLT}$



IN+ = High IN– = Low

図 7-19. I_{CC1} Supply Current vs Temperature



IN+ = Low IN– = Low

図 7-20. I_{CC1} Supply Current vs Temperature

7.12 Typical Characteristics (continued)

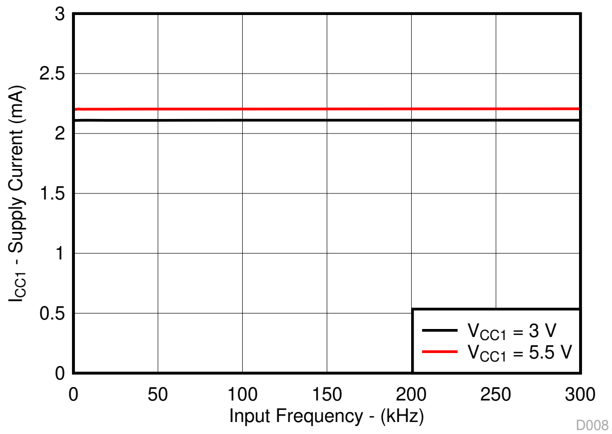
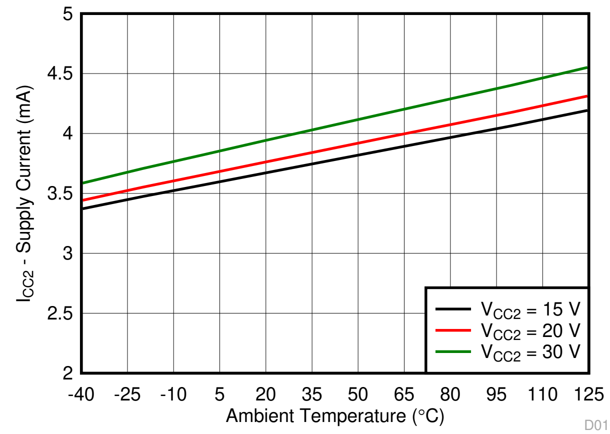
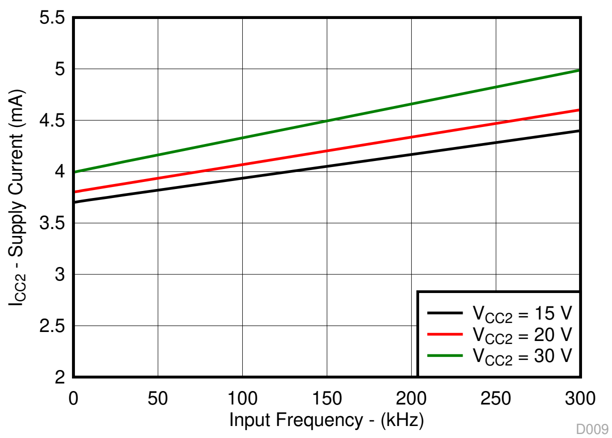


図 7-21. I_{CC1} Supply Current vs Input Frequency



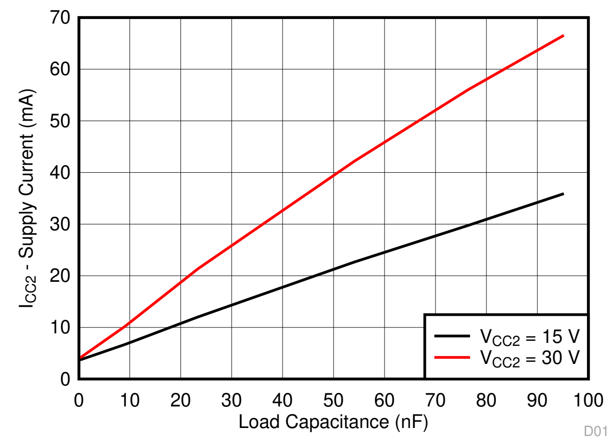
Input frequency = 1 kHz

図 7-22. I_{CC2} Supply Current vs Temperature



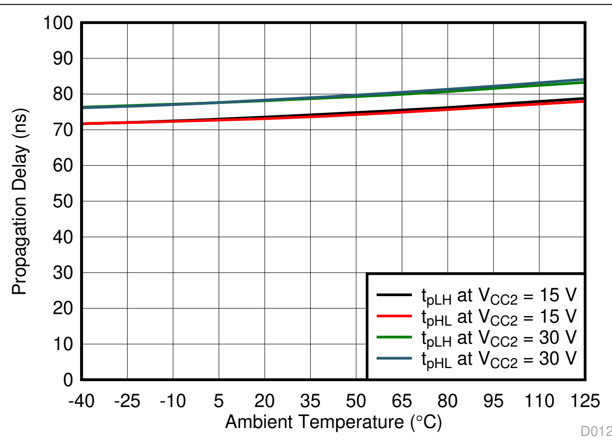
No C_L

図 7-23. I_{CC2} Supply Current vs Input Frequency



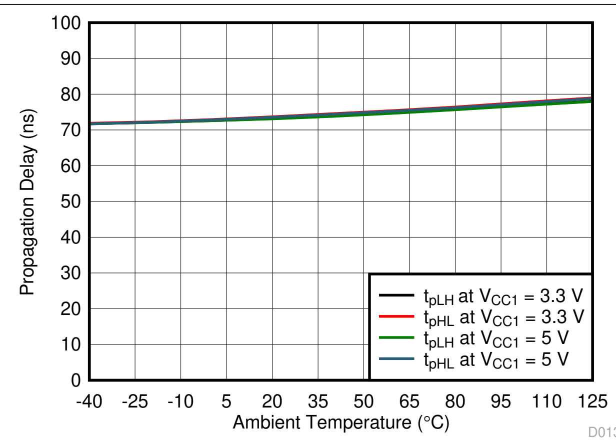
R_{GH} = 10 Ω R_{GL} = 5 Ω, 20 kHz

図 7-24. I_{CC2} Supply Current vs Load Capacitance



C_L = 1 nF R_{GH} = 0 Ω R_{GL} = 0 Ω
V_{CC1} = 5 V

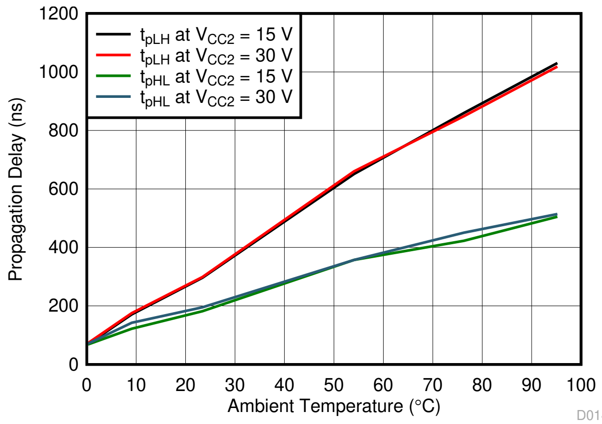
図 7-25. Propagation Delay vs Temperature



C_L = 1 nF R_{GH} = 0 Ω R_{GL} = 0 Ω
V_{CC2} = 15 V

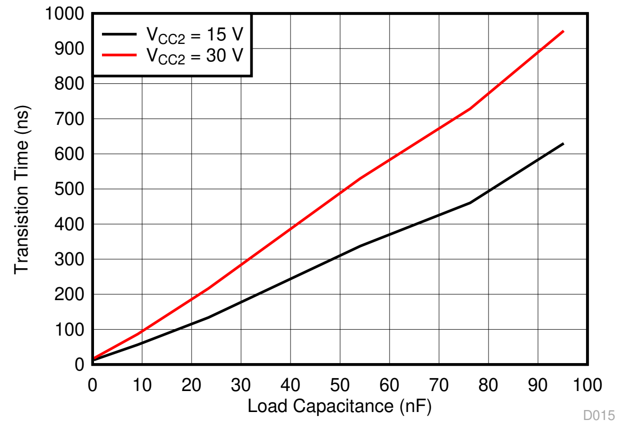
図 7-26. Propagation Delay vs Temperature

7.12 Typical Characteristics (continued)



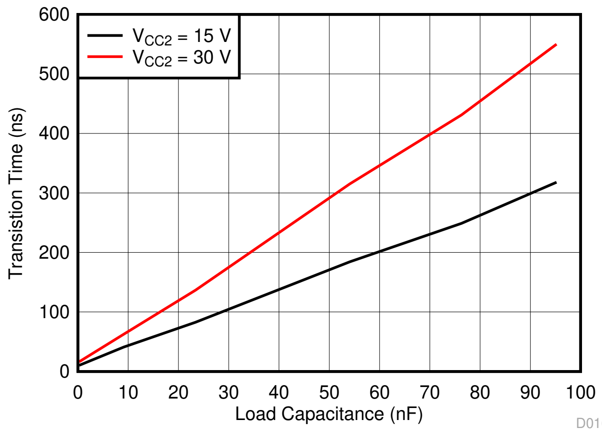
R_{GH} = 10 Ω R_{GL} = 5 Ω V_{CC1} = 5 V

図 7-27. Propagation Delay vs Load Capacitance



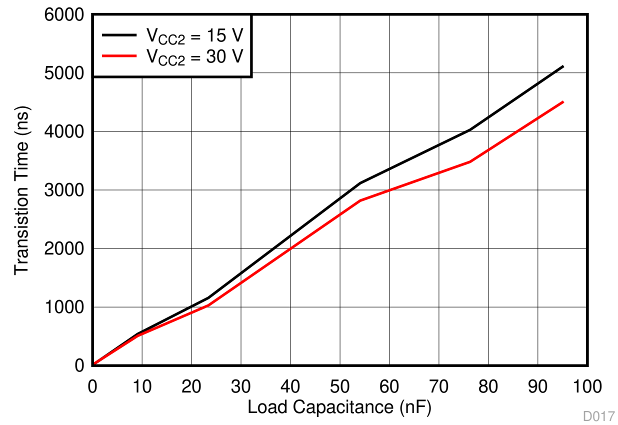
R_{GH} = 0 Ω R_{GL} = 0 Ω V_{CC1} = 5 V

図 7-28. t_r Rise Time vs Load Capacitance



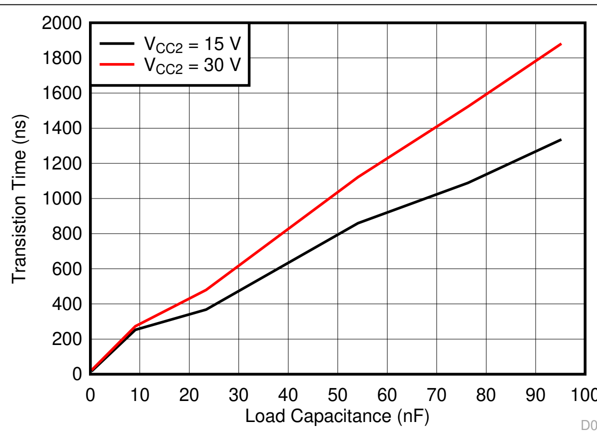
R_{GH} = 0 Ω R_{GL} = 0 Ω V_{CC1} = 5 V

図 7-29. t_f Fall Time v. Load Capacitance



R_{GH} = 10 Ω R_{GL} = 5 Ω V_{CC1} = 5 V

図 7-30. t_r Rise Time vs Load Capacitance



R_{GH} = 10 Ω R_{GL} = 5 Ω V_{CC1} = 5 V

図 7-31. t_f Fall Time vs Load Capacitance

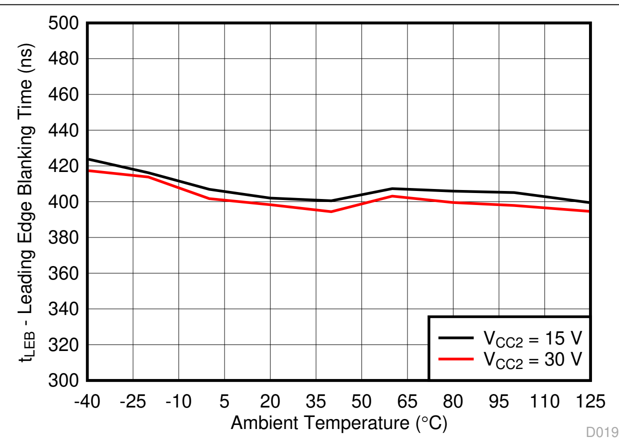
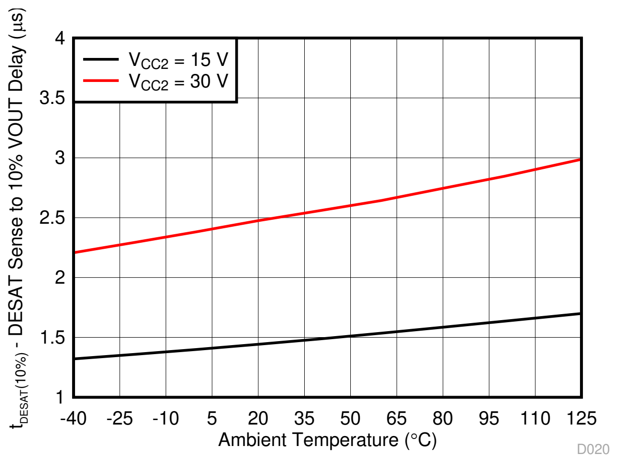


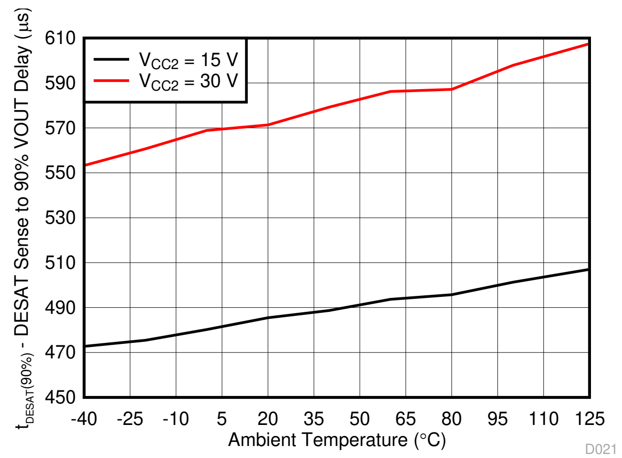
図 7-32. Leading Edge Blanking Time With Temperature

7.12 Typical Characteristics (continued)



C_L = 10 nF R_{GH} = 0 Ω R_{GL} = 0 Ω

図 7-33. DESAT Sense to $V_{OUTH/L}$ 10% Delay vs Temperature



C_L = 10 nF R_{GH} = 0 Ω R_{GL} = 0 Ω

図 7-34. DESAT Sense to $V_{OUTH/L}$ 90% Delay vs Temperature

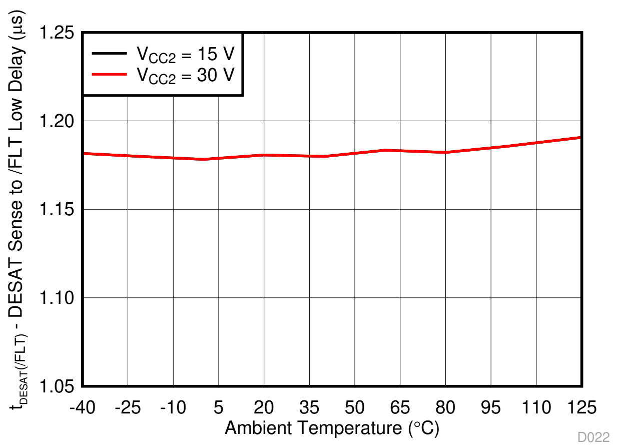


図 7-35. DESAT Sense to Fault Low Delay vs Temperature

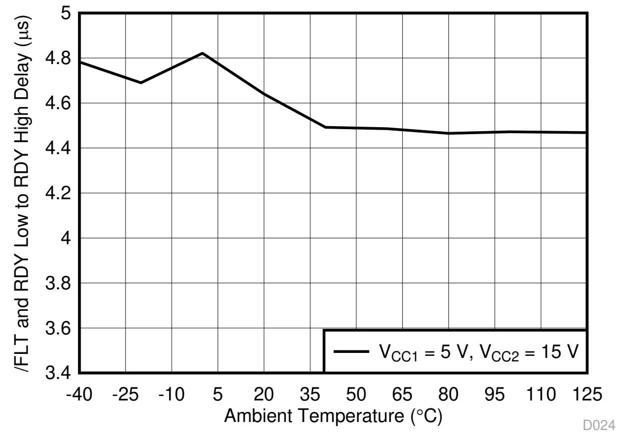


図 7-36. Fault and RDY Low to RDY High Delay vs Temperature

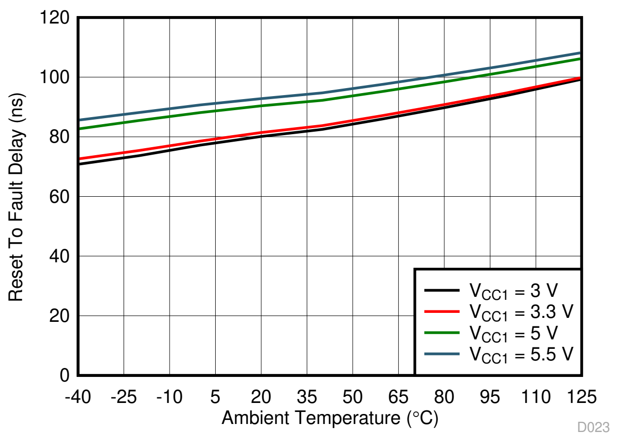


図 7-37. Reset to Fault Delay Across Temperature

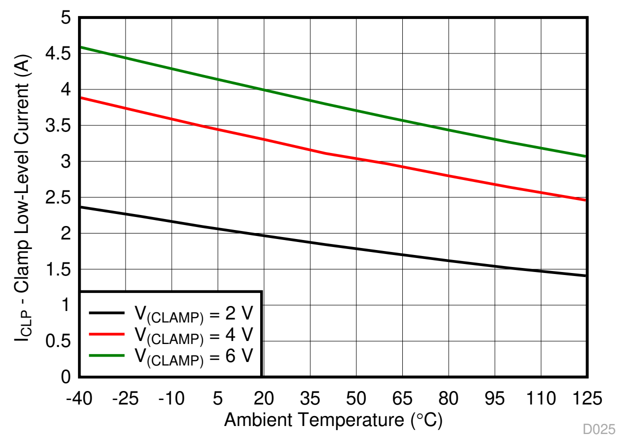


図 7-38. Miller Clamp Current vs Temperature

7.12 Typical Characteristics (continued)

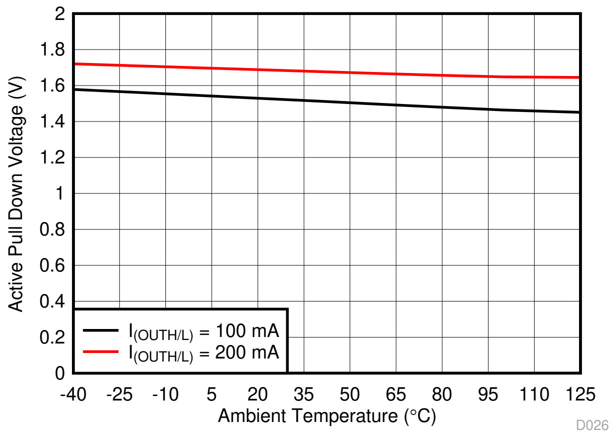


図 7-39. Active Pull Down Voltage vs Temperature

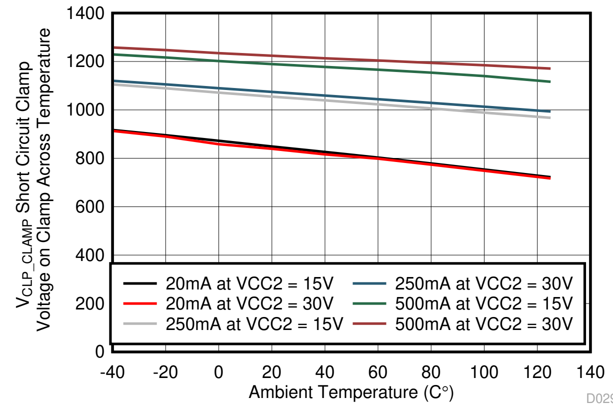


図 7-40. V_{CLP_CLAMP} - Short Circuit Clamp Voltage on Clamp Across Temperature

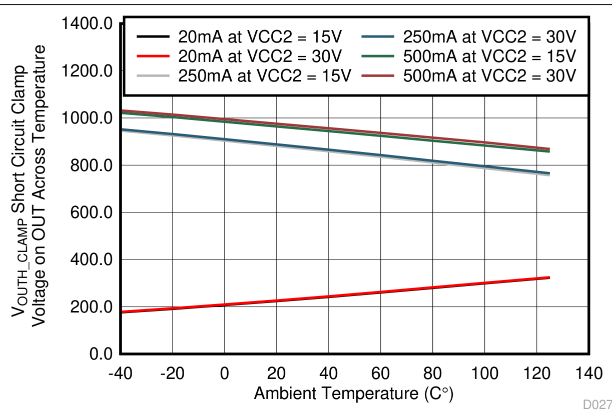


図 7-41. V_{OUTH_CLAMP} - Short Circuit Clamp Voltage on OUTH Across Temperature

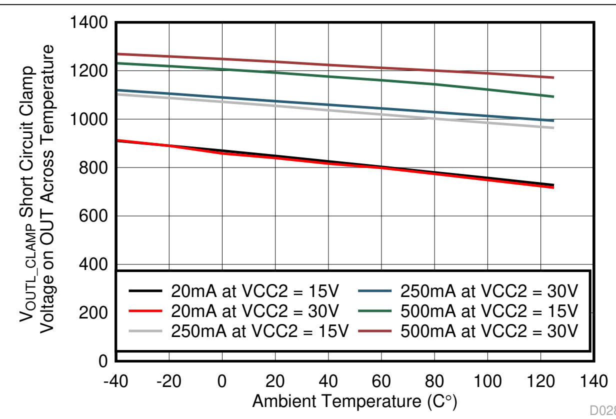
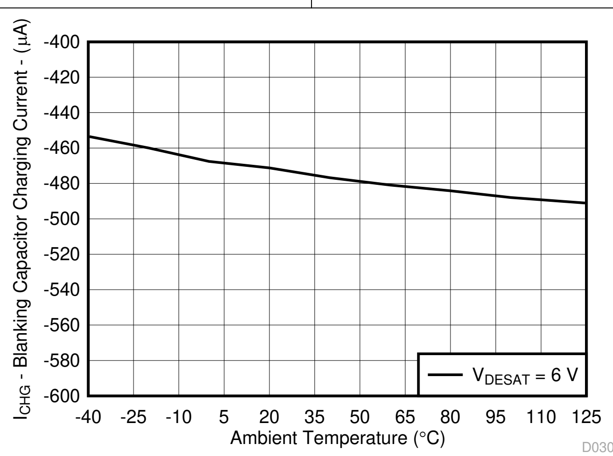


図 7-42. V_{OUTL_CLAMP} - Short Circuit Clamp Voltage on OUTL Across Temperature



V_{CC2} = 15 V DESAT = 6 V

図 7-43. Blanking Capacitor Charging Current vs Temperature

8 Parameter Measurement Information

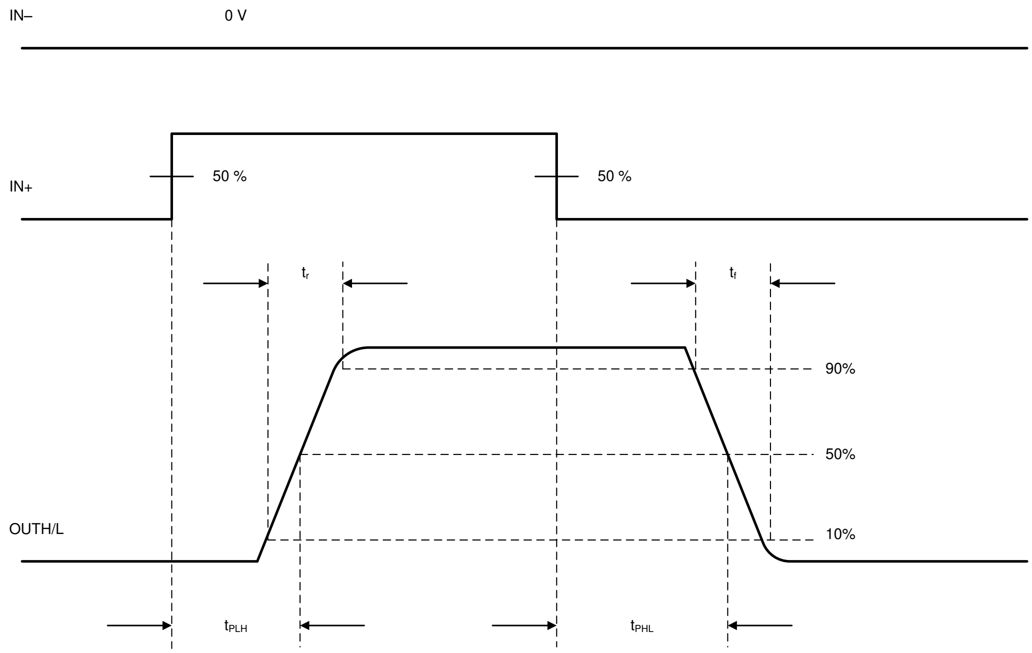


図 8-1. OUTH and OUTL Propagation Delay, Noninverting Configuration

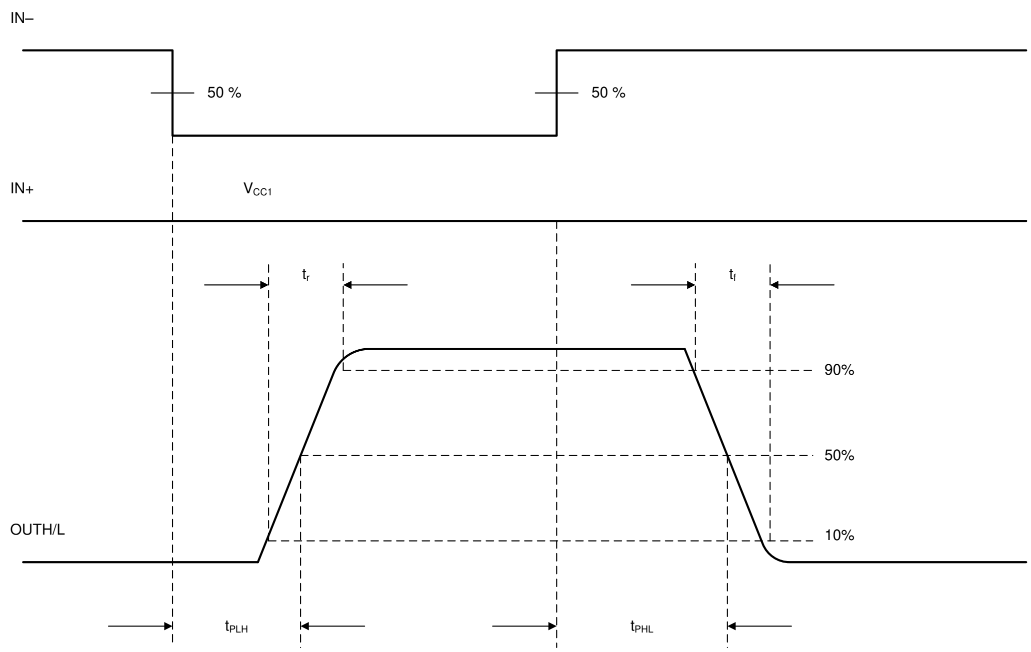


図 8-2. OUTH and OUTL Propagation Delay, Inverting Configuration

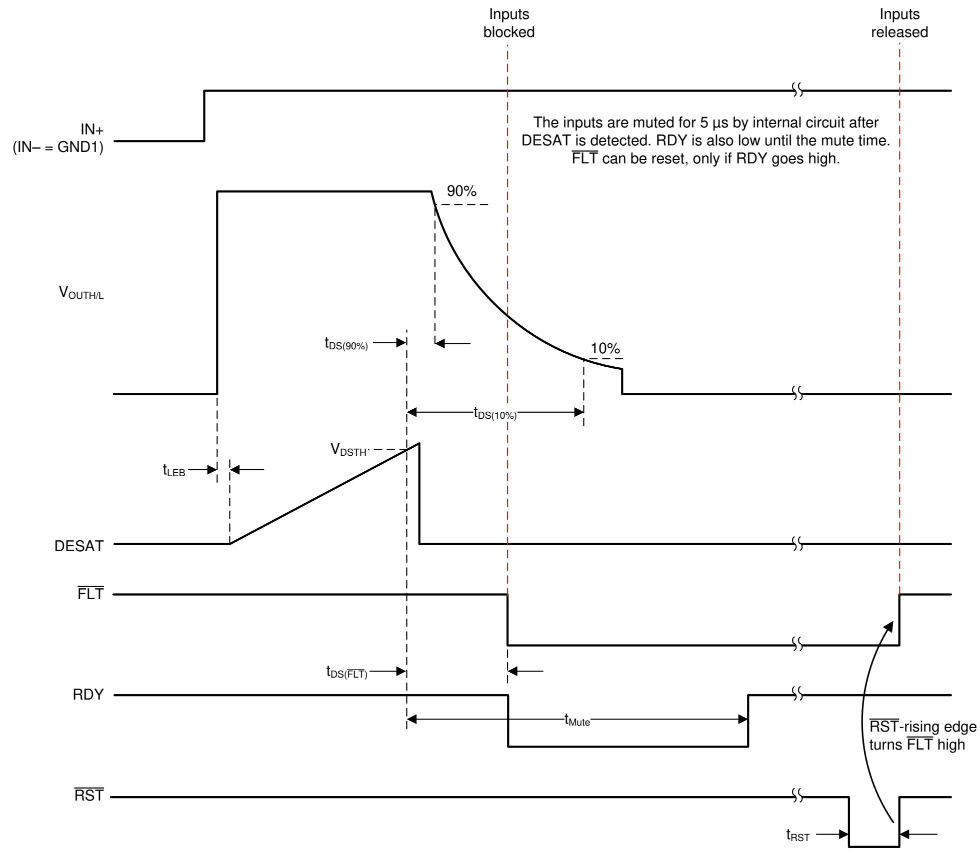


図 8-3. DESAT, OUTH, OUTL, $\overline{FLT}$, $\overline{RST}$ Delay

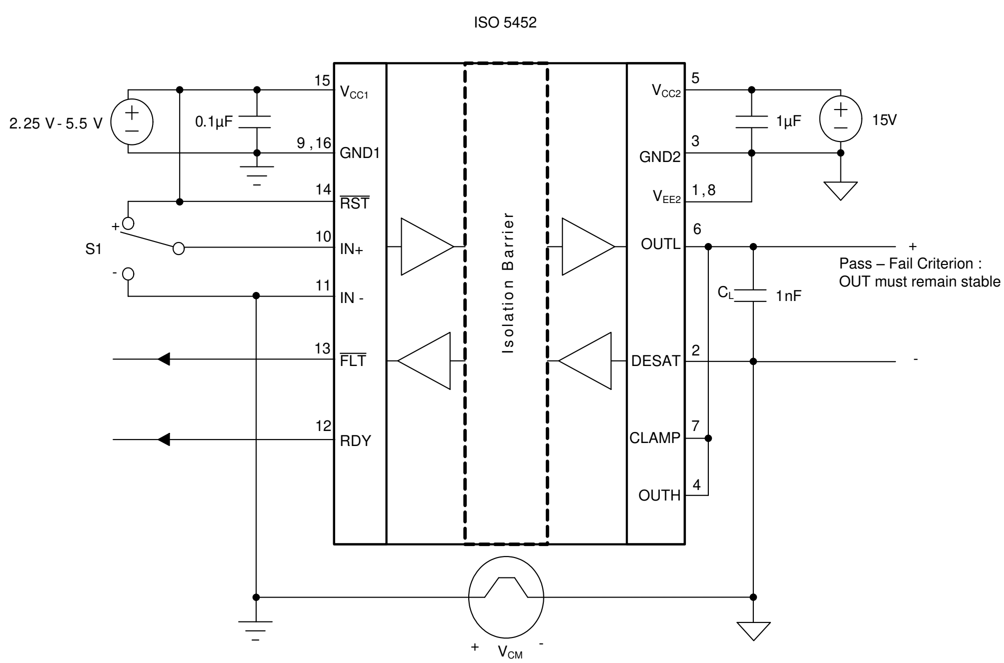


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図 8-4. Common-Mode Transient Immunity Test Circuit

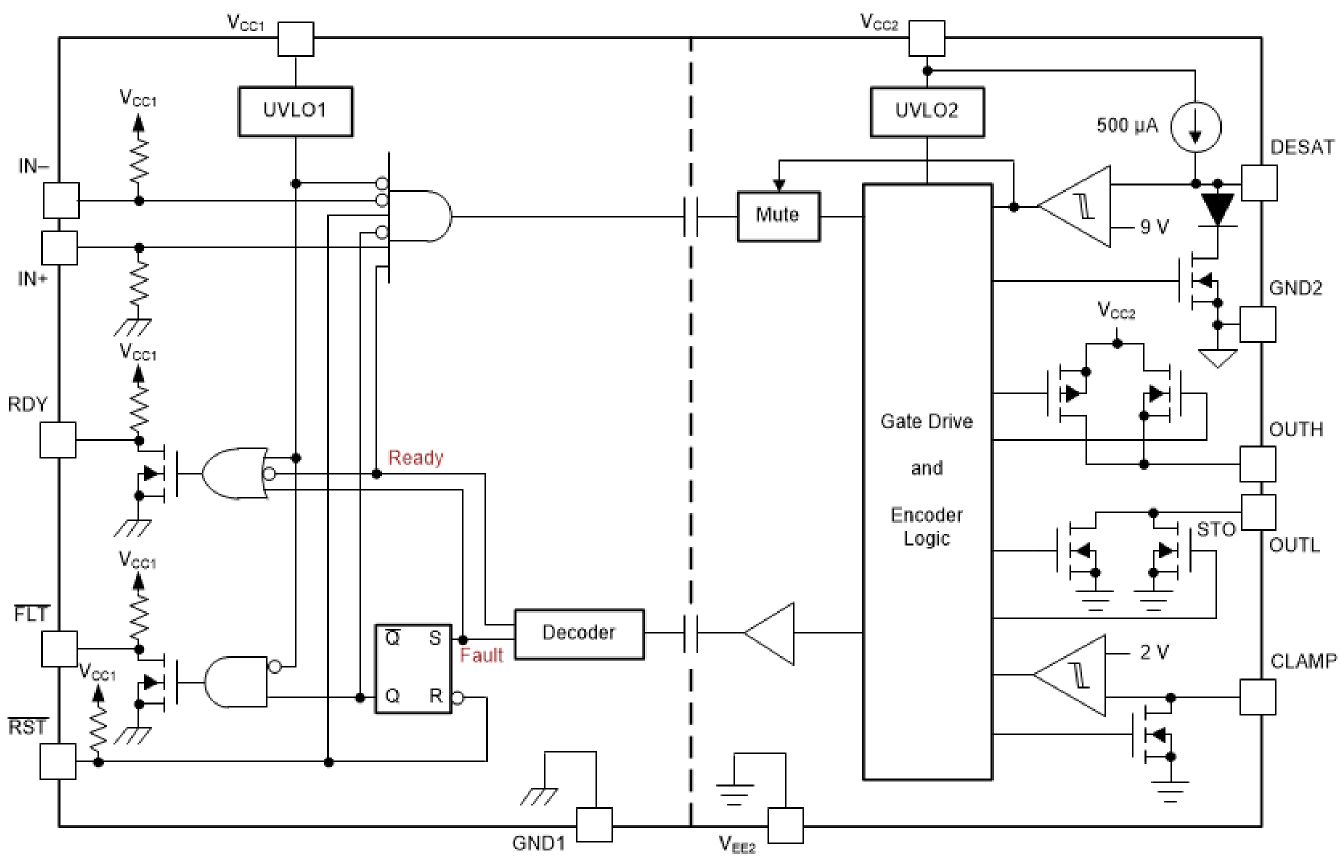
9 Detailed Description

9.1 Overview

The ISO5452 device is an isolated gate driver for IGBTs and MOSFETs. Input CMOS logic and output power stage are separated by a Silicon dioxide (SiO_2) capacitive isolation.

The IO circuitry on the input side interfaces with a microcontroller and consists of gate-drive control and RESET ($\overline{RST}$) inputs, READY (RDY) and FAULT ($\overline{FLT}$) alarm outputs. The power stage consists of power transistors to supply 2.5-A pullup and 5-A pulldown currents to drive the capacitive load of the external power transistors, as well as DESAT detection circuitry to monitor IGBT collector-emitter overvoltage under short-circuit events. The capacitive isolation core consists of transmit circuitry to couple signals across the capacitive isolation barrier, and receive circuitry to convert the resulting low-swing signals into CMOS levels. The ISO5452 device also has undervoltage lockout circuitry to prevent insufficient gate drive to the external IGBT, and active output pulldown feature which ensures that the gate-driver output is held low, if the output supply voltage is absent. The ISO5452 device also has an active Miller clamp function which can be used to prevent parasitic turnon of the external power transistor, because of Miller effect, for unipolar supply operation.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Supply and Active Miller Clamp

The ISO5452 device supports both bipolar and unipolar power supply with active Miller clamp.

For operation with bipolar supplies, the IGBT is turned off with a negative voltage on the gate with respect to the emitter. This prevents the IGBT from unintentionally turning on because of current induced from the collector to the gate because Miller effect. In this condition connecting the CLAMP output of the gate driver to the IGBT gate is not necessary, but connecting the CLAMP output of the gate driver to the IGBT gate is also not an issue. Typical values of V_{CC2} and V_{EE2} for bipolar operation are 15 V and –8 V with respect to GND2.

For operation with unipolar supply, typically, V_{CC2} is connected to 15 V with respect to GND2, and V_{EE2} is connected to GND2. In this use case, the IGBT can turn on because of additional charge from IGBT Miller capacitance caused by a high-voltage slew-rate transition on the IGBT collector. To prevent IGBT from turning on, the CLAMP pin is connected to IGBT gate and Miller current is sinked through a low-impedance CLAMP transistor.

Miller CLAMP is designed for miller current up to 2 A. When the IGBT is turned off and the gate voltage transitions below 2 V and the CLAMP current output is activated.

9.3.2 Active Output Pull-down

The active output pulldown feature ensures that the IGBT gate OUTH/L is clamped to V_{EE2} to ensure safe IGBT off-state, when the output side is not connected to the power supply.

9.3.3 Undervoltage Lockout (UVLO) with Ready (RDY) Pin Indication Output

Undervoltage lockout (UVLO) ensures correct switching of IGBT. The IGBT is turned off, if the supply V_{CC1} drops below $V_{IT-(UVLO1)}$, irrespective of IN+, IN– and RST input until V_{CC1} goes above $V_{IT+(UVLO1)}$.

In similar manner, the IGBT is turned off if the supply V_{CC2} drops below $V_{IT-(UVLO2)}$, irrespective of IN+, IN– and RST input till V_{CC2} goes above $V_{IT+(UVLO2)}$.

The RDY pin indicates status of input and output side UVLO internal protection feature. If either side of device have insufficient supply (V_{CC1} or V_{CC2}), the RDY pin output goes low; otherwise, RDY pin output is high. The RDY pin also serves as an indication to the micro-controller that the device is ready for operation.

9.3.4 Soft Turn-Off, Fault ($\overline{\text{FLT}}$) and Reset ($\overline{\text{RST}}$)

During IGBT overcurrent condition, a mute logic initiates a soft-turn-off procedure which disables OUTH and pulls OUTL to low over a time span of 2 μs. When desaturation is active, a fault signal is sent across the isolation barrier pulling the $\overline{\text{FLT}}$ output at the input side low and blocking the isolator input. Mute logic is activated through the soft-turn-off period. The $\overline{\text{FLT}}$ output condition is latched and can be reset only after RDY goes high, through a low-active pulse at the $\overline{\text{RST}}$ input. $\overline{\text{RST}}$ has an internal filter to reject noise and glitches. By asserting $\overline{\text{RST}}$ for at least the specified minimum duration (800ns), device input logic can be enabled or disabled.

9.3.5 Short Circuit Clamp

Under short-circuit events currents can be induced back into the gate-driver OUTH/L and CLAMP pins because of parasitic Miller capacitance between the IGBT collector and gate terminals. Internal protection diodes on OUTH/L and CLAMP help to sink these currents while clamping the voltages on these pins to values slightly higher than the output side supply.

9.4 Device Functional Modes

For OUTH/L of the ISO5452 device to follow IN+ in normal functional mode, the $\overline{RST}$ and RDY pins must be in the high state. 表 9-1 lists the device functional modes

表 9-1. Function Table(1)

V_{CC1}	V_{CC2}	IN+	IN–	$\overline{RST}$	RDY	OUTH/L
PU	PD	X	X	X	Low	Low
PD	PU	X	X	X	Low	Low
PU	PU	X	X	Low	High	Low
PU	Open	X	X	X	Low	Low
PU	PU	Low	X	X	High	Low
PU	PU	X	High	X	High	Low
PU	PU	High	Low	High	High	High

(1) PU: Power Up (V_{CC1} ≥ 2.25-V, V_{CC2} ≥ 13-V), PD: Power Down (V_{CC1} ≤ 1.7-V, V_{CC2} ≤ 9.5-V), X: Irrelevant

10 Application and Implementation

注

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10.1 Application Information

The ISO5452 device is an isolated gate driver for power semiconductor devices such as IGBTs and MOSFETs. The device is intended for use in applications such as motor control, industrial inverters, and switched mode power supplies. In these applications, sophisticated PWM control signals are required to turn the power devices on and off, which at the system level eventually may determine, for example, the speed, position, and torque of the motor or the output voltage, frequency and phase of the inverter. These control signals are usually the outputs of a micro controller, and are at low voltage levels such as 2.5 V, 3.3 V or 5 V. The gate controls required by the MOSFETs and IGBTs, on the other hand, are in the range of 30 V (using unipolar output supply) to 15 V (using bipolar output supply), and require high current capability to be able to drive the large capacitive loads offered by those power transistors. Not only that, the gate drive must be applied with reference to the emitter of the IGBT (Source for MOSFET), and by construction, the emitter node in a gate drive system may swing between 0 to the DC bus voltage, that can be several 100s of volts in magnitude.

The ISO5452 device is therefore used to level shift the incoming 2.5-V, 3.3-V and 5-V control signals from the microcontroller to the 30 V (using unipolar output supply) to 15 V (using bipolar output supply) drive required by the power transistors while ensuring high-voltage isolation between the driver side and the microcontroller side.

10.2 Typical Applications

図 10-1 shows the typical application of a three-phase inverter using six ISO5452 isolated gate drivers. Three-phase inverters are used for variable-frequency drives to control the operating speed and torque of AC motors and for high power applications such as high-voltage DC (HVDC) power transmission.

The basic three-phase inverter consists of six power switches, and each switch is driven by one SO5452. The switches are driven on and off at high switching frequency with specific patterns to convert DC bus voltage to three-phase AC voltages.

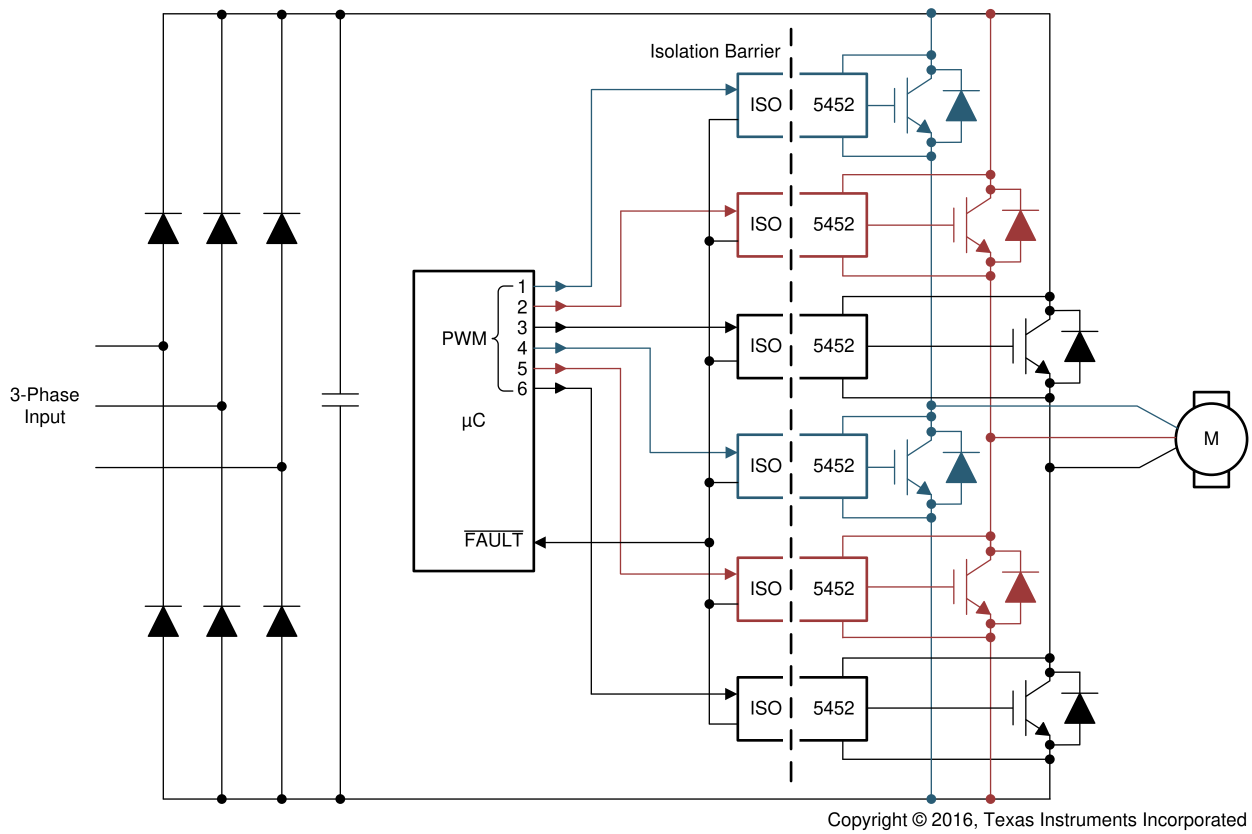


図 10-1. Typical Motor Drive Application

10.2.1 Design Requirements

Unlike optocoupler-based gate drivers which require external current drivers and biasing circuitry to provide the input control signals, the input control to the ISO5452 device is CMOS and can be directly driven by the microcontroller. Other design requirements include decoupling capacitors on the input and output supplies, a pullup resistor on the common drain $\overline{FLT}$ output signal, and a high-voltage protection diode between the IGBT collector and the DESAT input. Further details are explained in the subsequent sections. 表 10-1 shows the allowed range for input and output supply voltage, and the typical current output available from the gate-driver.

表 10-1. Design Parameters

PARAMETER	VALUE
Input supply voltage	2.25 V to 5.5 V
Unipolar output supply voltage (V_{CC2} – GND2 = V_{CC2} – V_{EE2})	15 V to 30 V
Bipolar output supply voltage (V_{CC2} – V_{EE2})	15 V to 30 V
Bipolar output supply voltage (GND2 – V_{EE2})	0 V to 15 V
Output current	2.5 A

10.2.2 Detailed Design Procedure

10.2.2.1 Recommended ISO5452 Application Circuit

The ISO5452 has both, inverting and non-inverting gate control inputs, an active low reset input, and an open-drain fault output suitable for wired-OR applications. The recommended application circuit in 図 10-2 shows a typical gate driver implementation with unipolar output supply and 図 10-3 shows a typical gate driver implementation with bipolar output supply using the ISO5452 device.

A 0.1-µF bypass capacitor, recommended at input supply pin V_{CC1} and 1-µF bypass capacitor, recommended at output supply pin V_{CC2}, provide the large transient currents necessary during a switching transition to ensure reliable operation. The 220-pF blanking capacitor disables DESAT detection during the off-to-on transition of the power device. The DESAT diode (D_{DST}) and the 1-kΩ series resistor are external protection components. The R_G gate resistor limits the gate charge current and indirectly controls the IGBT collector voltage rise and fall times. The open-drain $\overline{\text{FLT}}$ output and RDY output has a passive 10-kΩ pullup resistor. In this application, the IGBT gate driver is disabled when a fault is detected and will not resume switching until the microcontroller applies a reset signal.

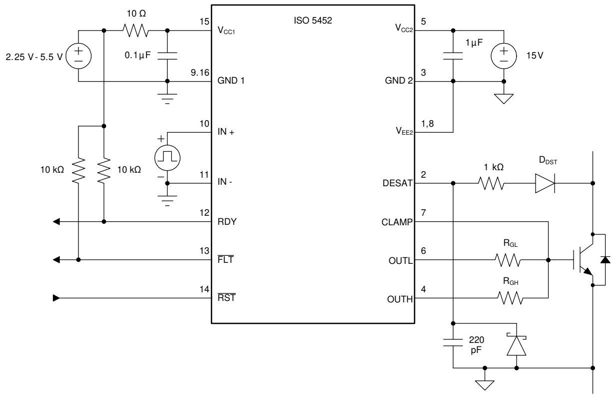


図 10-2. Unipolar Output Supply

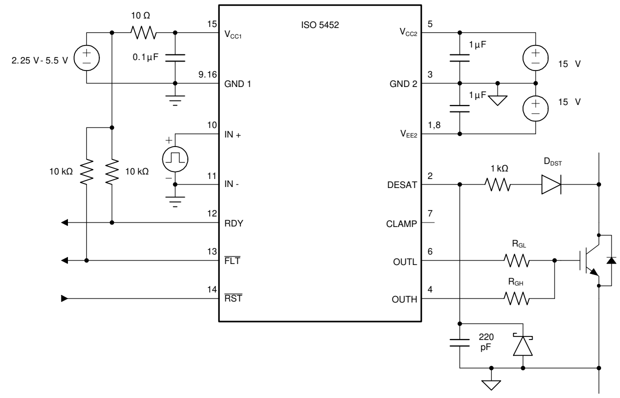


図 10-3. Bipolar Output Supply

10.2.2.2 $\overline{\text{FLT}}$ and RDY Pin Circuitry

A 50-kΩ pullup resistor is internally connected on the $\overline{\text{FLT}}$ and RDY pins. The $\overline{\text{FLT}}$ and RDY pins are an open-drain output. A 10-kΩ pullup resistor can be used to make it faster rise and to provide logic high when $\overline{\text{FLT}}$ and RDY is inactive, as shown in 図 10-4.

Fast common mode transients can inject noise and glitches on $\overline{\text{FLT}}$ and RDY pins because of parasitic coupling. This is dependent on board layout. If required, additional capacitance (100 pF to 300 pF) can be included on the $\overline{\text{FLT}}$ and RDY pins.

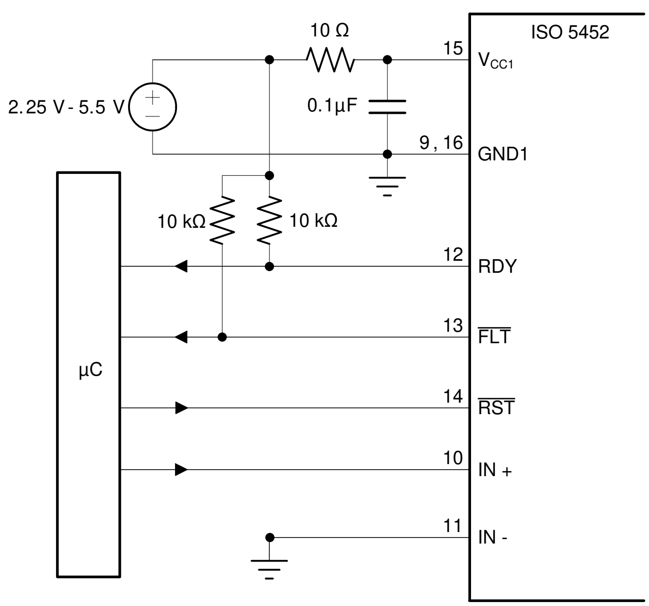


図 10-4. $\overline{\text{FLT}}$ and RDY Pin Circuitry for High CMTI

10.2.2.3 Driving the Control Inputs

The amount of common-mode transient immunity (CMTI) can be curtailed by the capacitive coupling from the high-voltage output circuit to the low-voltage input side of the ISO5452 device. For maximum CMTI performance, the digital control inputs, IN+ and IN–, must be actively driven by standard CMOS, push-pull drive circuits. This type of low-impedance signal source provides active drive signals that prevent unwanted switching of the ISO5452 output under extreme common-mode transient conditions. Passive drive circuits, such as open-drain configurations using pullup resistors, must be avoided. A 20-ns glitch filter can filter a glitch up to 20 ns on IN+ or IN–.

10.2.2.4 Local Shutdown and Reset

In applications with local shutdown and reset, the $\overline{FLT}$ output of each gate driver is polled separately, and the individual reset lines are asserted low independently to reset the motor controller after a fault condition.

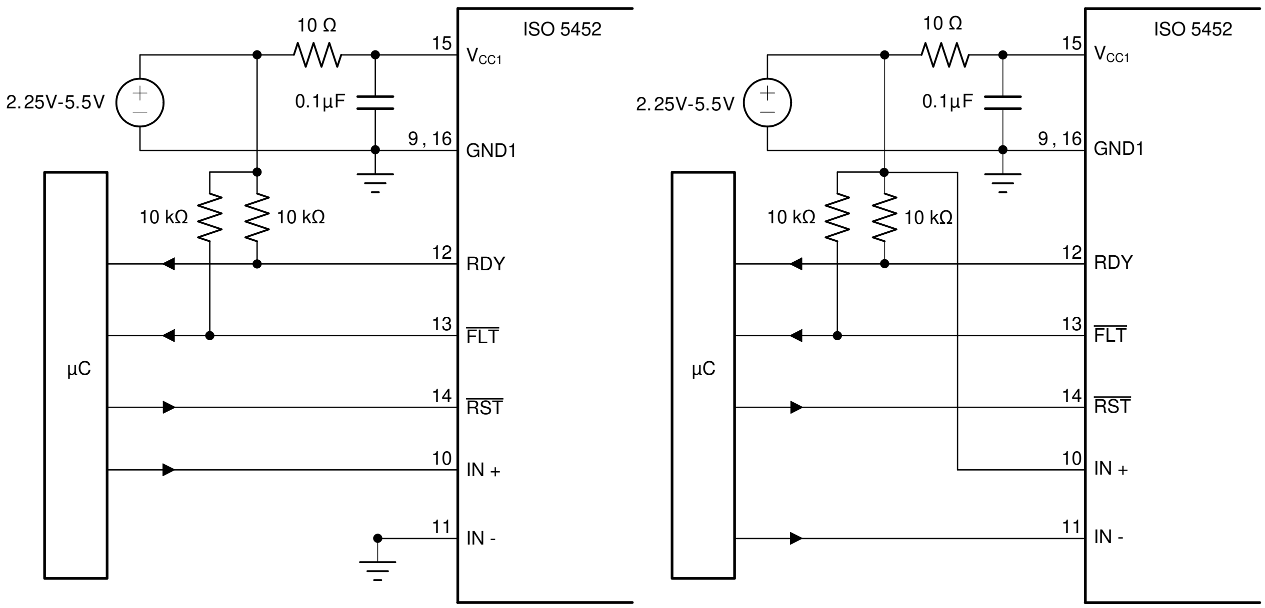


図 10-5. Local Shutdown and Reset for Noninverting (left) and Inverting Input Configuration (right)

10.2.2.5 Global-Shutdown and Reset

When configured for inverting operation, the ISO5452 device can be configured to shutdown automatically in the event of a fault condition by tying the $\overline{FLT}$ output to IN+. For high reliability drives, the open drain $\overline{FLT}$ outputs of multiple ISO5452 devices can be wired together forming a single, common fault bus for interfacing directly to the micro-controller. When any of the six gate drivers of a three-phase inverter detects a fault, the active low $\overline{FLT}$ output disables all six gate drivers simultaneously.

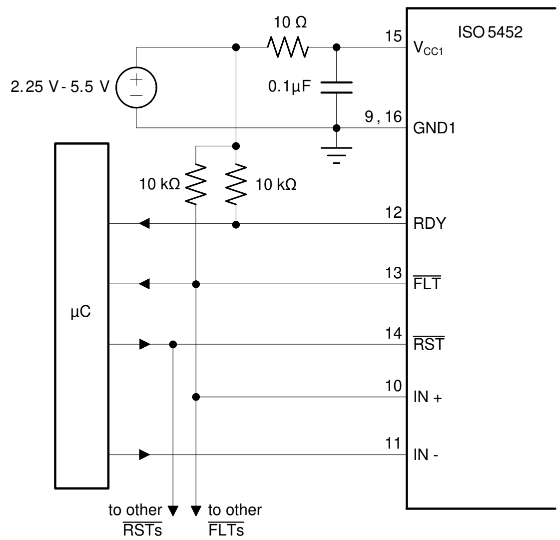


図 10-6. Global Shutdown With Inverting Input Configuration

10.2.2.6 Auto-Reset

In this case, the gate control signal at IN+ is also applied to the $\overline{RST}$ input to reset the fault latch every switching cycle. Incorrect $\overline{RST}$ makes output go low. A fault condition, however, the gate driver remains in the latched fault state until the gate control signal changes to the *gate low* state and resets the fault latch.

If the gate control signal is a continuous PWM signal, the fault latch will always be reset before IN+ goes high again. This configuration protects the IGBT on a cycle by cycle basis and automatically resets before the next *on* cycle.

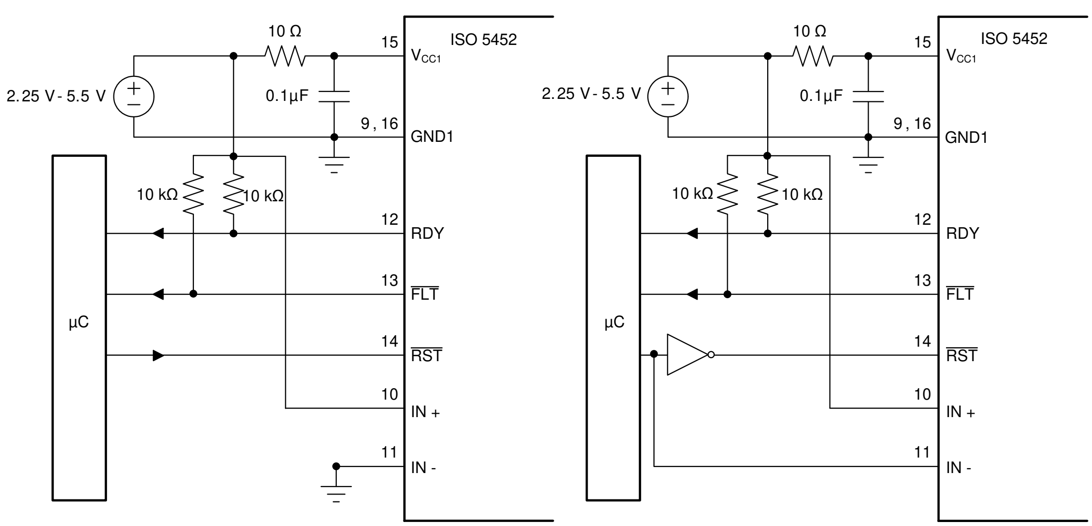


図 10-7. Auto Reset for Noninverting and Inverting Input Configuration

10.2.2.7 DESAT Pin Protection

Switching inductive loads causes large instantaneous forward voltage transients across the freewheeling diodes of IGBTs. These transients result in large negative voltage spikes on the DESAT pin which draw substantial current out of the device. To limit this current below damaging levels, a 100-Ω to 1-kΩ resistor is connected in series with the DESAT diode.

Further protection is possible through an optional Schottky diode, whose low forward voltage assures clamping of the DESAT input to GND2 potential at low voltage levels.

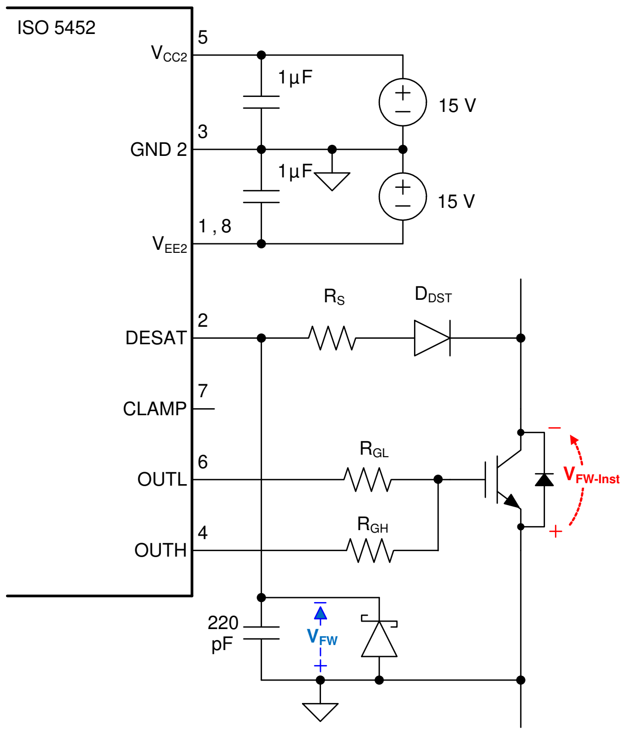


図 10-8. DESAT Pin Protection with Series Resistor and Schottky Diode

10.2.2.8 DESAT Diode and DESAT Threshold

The DESAT function of the diode is used to conduct forward current, allowing sensing of the saturated collector-to-emitter voltage of the IGBT, $V_{(DESAT)}$, (when the IGBT is on) and to block high voltages (when the IGBT is off). During the short transition time when the IGBT is switching, a commonly a high dV_{CE}/dt voltage ramp rate occurs across the IGBT. This results in a charging current $I_{CHARGE} = C_{(D\text{-}DESAT)} \times d_{VCE}/dt$, charging the blanking capacitor. $C_{(D\text{-}DESAT)}$ is the diode capacitance at DESAT.

To minimize this current and avoid false DESAT triggering, fast switching diodes with low capacitance are recommended. As the diode capacitance builds a voltage divider with the blanking capacitor, large collector voltage transients appear at DESAT attenuated by the ratio of 1+ $C_{(BLANK)} / C_{(D\text{-}DESAT)}$.

Because the sum of the DESAT diode forward-voltage and the IGBT collector-emitter voltage make up the voltage at the DESAT-pin, $V_F + V_{CE} = V_{(DESAT)}$, the V_{CE} level, which triggers a fault condition, can be modified by adding multiple DESAT diodes in series as shown in 式 1.

$$V_{CE\text{-}FAULT(TH)} = 9\ \text{V} - n \times V_F \tag{1}$$

where

- *n* is the number of DESAT diodes

When using two diodes instead of one, diodes with half the required maximum reverse-voltage rating may be chosen.

10.2.2.9 Determining the Maximum Available, Dynamic Output Power, $P_{OD\text{-}max}$

The ISO5452 maximum allowed total power consumption of P_D = 251 mW consists of the total input power, P_{ID}, the total output power, P_{OD}, and the output power under load, P_{OL}:

$$P_D = P_{ID} + P_{OD} + P_{OL} \tag{2}$$

With:

$$P_{ID} = V_{CC1\text{-}max} \times I_{CC1\text{-}max} = 5.5\ \text{V} \times 4.5\ \text{mA} = 24.75\ \text{mW} \tag{3}$$

and:

$$P_{OD} = (V_{CC2} - V_{EE2}) \times I_{CC2\text{-}max} = (15\text{V} - (-8\text{V})) \times 6\ \text{mA} = 138\ \text{mW} \tag{4}$$

then:

$$P_{OL} = P_D - P_{ID} - P_{OD} = 251\ \text{mW} - 24.75\ \text{mW} - 138\ \text{mW} = 88.25\ \text{mW} \tag{5}$$

In comparison to P_{OL}, the actual dynamic output power under worst case condition, $P_{OL\text{-}WC}$, depends on a variety of parameters:

$$P_{OL\text{-}WC} = 0.5 \times f_{INP} \times Q_G \times (V_{CC2} - V_{EE2}) \times \left(\frac{r_{on\text{-}max}}{r_{on\text{-}max} + R_G} + \frac{r_{off\text{-}max}}{r_{off\text{-}max} + R_G} \right) \tag{6}$$

where

- f_{INP} = signal frequency at the control input IN+
- Q_G = power device gate charge
- V_{CC2} = positive output supply with respect to GND2
- V_{EE2} = negative output supply with respect to GND2
- $r_{on\text{-}max}$ = worst case output resistance in the on-state: 4 Ω
- $r_{off\text{-}max}$ = worst case output resistance in the off-state: 2.5 Ω
- R_G = gate resistor

When R_G is determined, 式 6 is to be used to verify whether $P_{OL\text{-}WC} < P_{OL}$. 図 10-9 shows a simplified output stage model for calculating $P_{OL\text{-}WC}$.

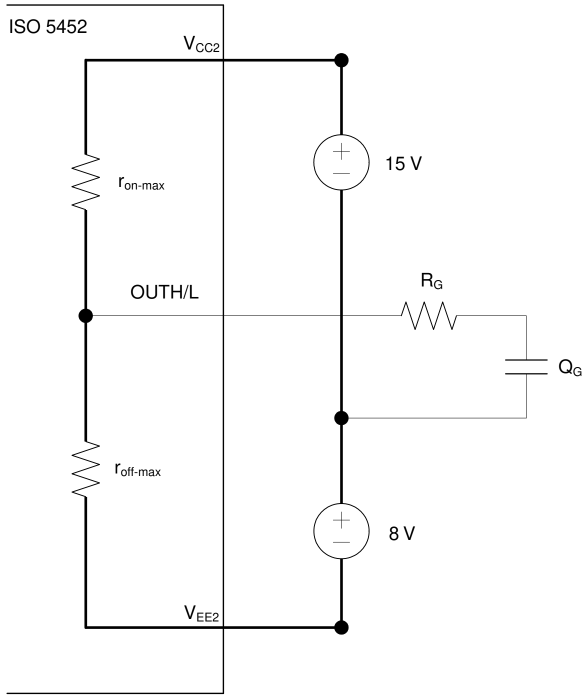


図 10-9. Simplified Output Model for Calculating $P_{OL\text{-}WC}$

10.2.2.10 Example

This examples considers an IGBT drive with the following parameters:

$$I_{ON\text{-}PK} = 2\text{ A},\ Q_G = 650\text{ nC},\ f_{INP} = 20\text{ kHz},\ V_{CC2} = 15\text{V},\ V_{EE2} = –8\text{ V} \tag{7}$$

Apply the value of the gate resistor R_G = 10 Ω.

Then, calculating the worst-case output power consumption as a function of R_G, using 式 6 $r_{on\text{-}max}$ = worst case output resistance in the on-state: 4 Ω, $r_{off\text{-}max}$ = worst case output resistance in the off-state: 2.5 Ω, R_G = gate resistor yields

$$P_{OL\text{-}WC} = 0.5 \times 20\text{ kHz} \times 650\text{ nC} \times \left(15\text{ V} - (-8\text{ V})\right) \times \left(\frac{4\ \Omega}{4\ \Omega + 10\ \Omega} + \frac{2.5\ \Omega}{2.5\ \Omega + 10\ \Omega}\right) = 72.61\text{ mW} \tag{8}$$

Because $P_{OL\text{-}WC}$ = 72.61 mW is less than the calculated maximum of P_{OL} = 88.25 mW, the resistor value of R_G = 10 Ω is suitable for this application.

10.2.2.11 Higher Output Current Using an External Current Buffer

To increase the IGBT gate drive current, a non-inverting current buffer (such as the npn/pnp buffer shown in 図 10-10) may be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for currents up to 8 A, the D44VH10/ D45VH10 pair for up to 15 A maximum.

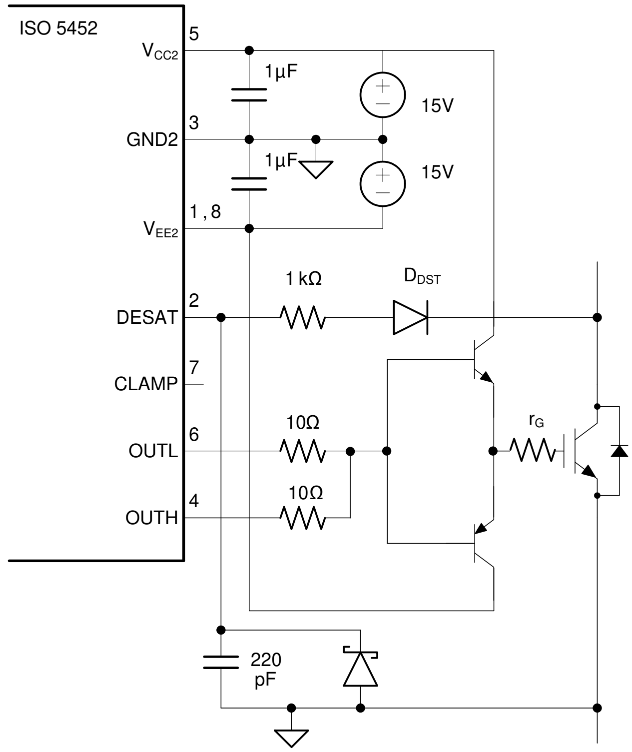
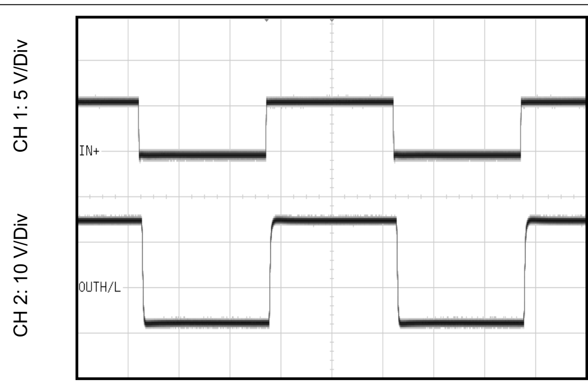


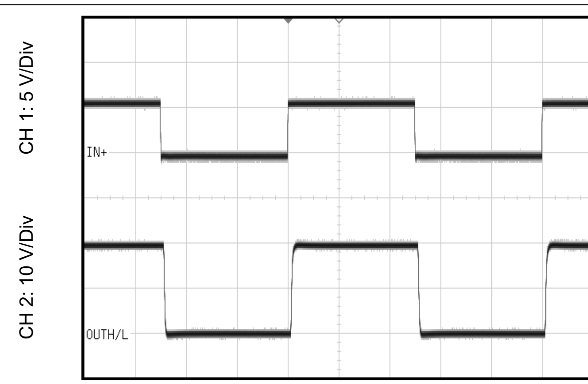
図 10-10. Current Buffer for Increased Drive Current

10.2.3 Application Curves



C_L = 1 nF R_{GH} = 10 Ω R_{GL} = 10 Ω
V_{CC2} – GND2 = 15 V GND2 – V_{EE2} = 8 V
(V_{CC2} – V_{EE2} = 23 V)

図 10-11. Normal Operation - Bipolar Supply



C_L = 1 nF R_{GH} = 10 Ω R_{GL} = 10 Ω
V_{CC2} – V_{EE2} = V_{CC2} – GND2 = 20 V

図 10-12. Normal Operation - Unipolar Supply

11 Power Supply Recommendations

To help ensure reliable operation at all data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at the input supply pin, V_{CC1}, and 1-µF bypass capacitor is recommended at the output supply pin, V_{CC2}. The capacitors should be placed as close to the supply pins as possible. The recommended placement of capacitors is 2-mm (maximum) from input and output power supply pin (V_{CC1} and V_{CC2}).

12 Layout

12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 図 12-1). Layer stacking should be in the following order (top-to-bottom): high-current or sensitive signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-current or sensitive traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the gate driver and the microcontroller and power transistors. Gate driver control input, gate driver output OUTH and OUTL, and DESAT should be routed in the top layer.
- Placing a solid ground plane next to the sensitive signal layer provides an excellent low-inductance path for the return current flow. On the driver side, use GND2 as the ground plane.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch^2. On the gate-driver V_{EE2} and V_{CC2} can be used as power planes. They can share the same layer on the PCB as long as they are not connected together.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

For detailed layout recommendations, see the *Digital Isolator Design Guide* (SLLA284).

12.2 Layout Example

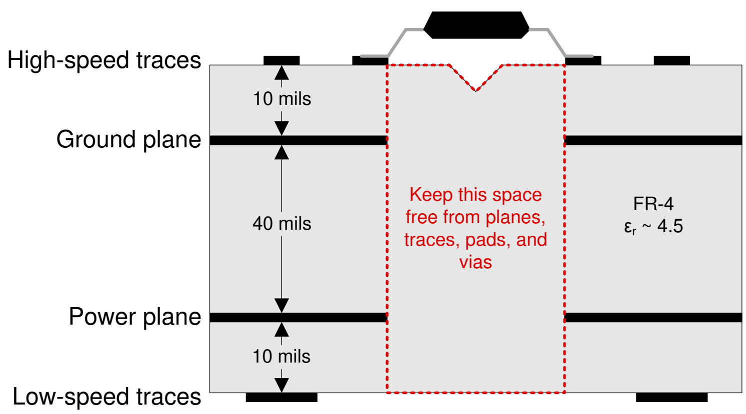


図 12-1. Recommended Layer Stack

12.3 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

13 Device and Documentation Support

13.1 Device Support

13.1.1 サード・パーティ製品に関する免責事項

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13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- *ISO5852S Evaluation Module (EVM) User's Guide*
- *Digital Isolator Design Guide*
- *Isolation Glossary*

13.3 ドキュメントの更新通知を受け取る方法

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13.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO5452DW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-40 to 125	ISO5452
ISO5452DWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO5452
ISO5452DWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO5452
ISO5452DWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO5452

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ISO5452 :

- Automotive : ISO5452-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265