ISO3086T 絶縁型 5V RS-485 トランシーバ、統合型トランス・ドライバ付き

1 特長

- TIA/EIA-485 を満たすか上回る
- 信号速度：最高 20Mbps
- 1/8 単位負荷 - 1 個のバスに最大 256 個のノード
- サーマル・シャットダウン保護機能
- 標準効率 > 60% (I_{LOAD} = 100mA) - SLUU469 を参照してください
- 7pF の低バス容量 (代表値)
- 50kV/μs の代表的な過渡耐性
- バスの開放、短絡、またはアイドル時のフェイル・セーフを備えるレシーバ
- ロジック入力は 5V 許容
- バス・ピン ESD 保護
  - バス・ピンと GND2 の間で 11kV HBM
  - バス・ピンと GND1 の間に 6kV HBM
- 安全および規制当局の承認
  - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した基本絶縁耐圧：4242V_{PK}
  - UL 1577 に準拠した絶縁耐圧：2500V_{RMS} (1 分間)
  - CSA Component Acceptance Notice 5A、IEC 60950-1 および IEC 61010-1 標準

2 アプリケーション

- 絶縁型 RS-485/RS-422 インターフェイス
- ファクトリ・オートメーション
- モータおよびモーション制御
- HVAC およびビルディング・オートメーション・ネットワーク
- ネットワーク接続セキュリティ・ステーション

3 概要

ISO3086T は、絶縁トランスに 1 次電圧を供給する発振器出力を内蔵した絶縁型差動ライン・トランシーバです。デバイスは、RS-485 および RS-422 アプリケーションの全二重差動ライン・トランシーバで、ピン 11 をピン 14 に、ピン 12 をピン 13 に接続することで、半二重動作用に簡単に構成できます。

これらのデバイスは、はるかに広い同相電圧範囲を許容するためにグランド・ループが切断されているため、長い伝送ラインに理想的です。各デバイスの対称型絶縁バリアは、バスライン・トランシーバとロジックレベル・インターフェイスとの間で、VDE に従い、4242 V_{PK} で 1 分間の絶縁を行うことがテスト済みです。

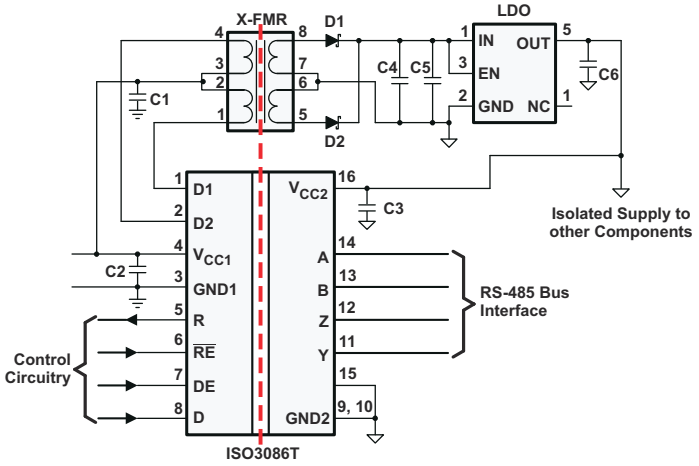
ケーブル接続されたすべての I/O は、各種ノイズ源からの電気的ノイズの過渡現象にさらされる可能性があります。このようなノイズ過渡は、十分な大きさと持続時間を持つ場合、トランシーバまたは隣接している高感度回路に損傷を与える可能性があります。これらの絶縁型デバイスは、保護機能を大幅に強化し、高価な制御回路の損傷リスクを低減できます。

ISO3086T は、–40℃～85℃で動作が規定されています。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
ISO3086T	SOIC (16)	10.30mm × 7.50mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (October 2015) to Revision E (August 2023) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations ... 6
- Updated electrical and switching characteristics to match device performance ... 8

Changes from Revision C (July 2011) to Revision D (October 2015) — **Page**

- 「特長」の項目「TIA/EIA-485 を満たすか上回る」を追加 ... 1
- VDE 規格を DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 に変更 ... 1
- 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1

Changes from Revision * (January 2011) to Revision A (March 2011) — **Page**

- 特長と概要を変更。 ... 1
- データシートを次のように変更:「プレビュー」から「量産」 ... 1
- Added 図 9-2 Typical Application Circuit ... 3

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5 Pin Configuration and Functions

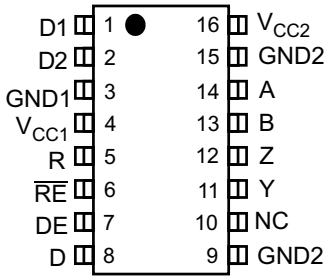

図 5-1. DW Package 16-Pin SOIC Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	14	I	Non-inverting Receiver Input
B	13	I	Inverting Receiver Input
D1	1	O	Transformer Driver Terminal 1, Open Drain Output
D2	2	O	Transformer Driver Terminal 2, Open Drain Output
D	8	I	Driver Input
DE	7	I	Driver Enable Input
GND1	3	—	Logic-side Ground
GND2	9, 15	—	Bus-side Ground. Both pins are internally connected.
NC	10	—	No Connect. This pin is not connected to any internal circuitry.
R	5	O	Receiver Output
$\overline{RE}$	6	I	Receiver Enable Input. This pin has complementary logic.
V_{CC1}	4	—	Logic-side Power Supply
V_{CC2}	16	—	Bus-side Power Supply
Y	11	O	Non-inverting Driver Output
Z	12	O	Inverting Driver Output

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC} (2)	Supply voltage, V_{CC1}, V_{CC2}	-0.3	6	V
V_A, V_B, V_Y, V_Z	Voltage at any bus I/O terminal (A,B,Y,Z)	-9	14	V
V_{D1}, V_{D2}	Voltage at D1, D2		14	V
$V_{(TRANS)}$	Voltage input, transient pulse, A, B, Y, and Z (through 100Ω, see Figure 27)	-50	50	V
V_I	Voltage input at any D, DE or $\overline{RE}$ terminal	-0.5	6	V
I_O	Receiver output current	-10	10	mA
I_{D1}, I_{D2}	Transformer Driver Output Current		450	mA
T_J	Junction temperature		150	℃
T_{STG}	Storage temperature	-65	150	℃

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Human body model (HBM), per ANSI/ ESDA/JEDEC JS-001(1)	Bus pins and GND1	±6000	V
$V_{(ESD)}$		Bus pins and GND2	±11000	V
$V_{(ESD)}$		All pins	±4000	V
$V_{(ESD)}$	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		±1500	V
$V_{(ESD)}$	Machine model (MM), ANSI/ ESDS5.2-1996		±200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{CC1}	Logic-side supply voltage - 3.3V operation	3	3.3	3.6	V
V_{CC1}	Logic-side supply voltage - 5 V operation	4.5	5	5.5	V
V_{CC2}	Bus-side supply voltage	4.5	5	5.5	V
V_{IC}	Voltage at any bus terminal (separately or common-mode)	-7		12	V
V_{IH}	High-level input voltage ($\overline{RE}$ inputs)	2		V_{CC1}	V
V_{IH}	High-level input voltage (D, DE inputs)	0.7*V_{CC}			V
V_{IL}	Low-level input voltage ($\overline{RE}$ inputs)	0		0.8	V
V_{IL}	Low-level input voltage (D, DE inputs)	0		0.3*V_{CC}	V
V_{ID}	Differential input voltage, A with respect to B	-12		12	V
V_{ID}	Differential input voltage, Dynamic	See Figure 16			V
R_L	Differential load resistance	54	60		Ω
I_O	Output current, Driver	-60		60	mA

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		MIN	TYP	MAX	UNIT
I_O	Output current, Receiver	-8		8	mA
T_A	Operating ambient temperature	-40		85	°C
$1/t_{UI}$	Signaling Rate			20	Mbps

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6.4 Thermal Information

THERMAL METRIC[1]		ISO308x DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2} = 5.5V$, $T_J = 150°C$, $R_L = 54\Omega$, $C_L = 50pF$ (Driver), $C_L = 15pF$ (Receiver),Input a 10 MHz 50% duty cycle square wave to Driver and Receiver			490	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE DW-16	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	8	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>400	V
	Material group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) [2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	4242	V_{PK}
q_{pd}	Apparent charge[3]	Method b; At routine test (100% production) $V_{ini} = 1.2 \times V_{IOTM}$, $t_{ini} = 1$ s; $V_{pd(m)} = 1.5 \times V_{IORM}$, $t_m = 1$ s	≤5	pC
C_{IO}	Barrier capacitance, input to output[4]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	2	pF
C_I	Input capacitance to ground	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, f = 1 MHz, V_{CC} = 5 V	2	pF
R_{IO}	Isolation resistance[4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, T_S = 150°C	$>10^{12}$	
	Pollution degree		2	
	Climatic category		40/085/21	
UL 1577				

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PARAMETER		TEST CONDITIONS	VALUE	UNIT
			DW-16	
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	2500	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *basic electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

VDE	CSA	UL
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 60950-1 and IEC 61010-1	Approved under UL 1577 Component Recognition Program
Basic insulation Maximum Transient Isolation Voltage, 4242 V_{PK} Maximum Surge Isolation Voltage, 4000 V_{PK} Maximum Repetitive Peak Isolation Voltage, 566 V_{PK}	3000 V_{RMS} Isolation Rating; Reinforced insulation per CSA 61010-1 and IEC 61010-1 150 V_{RMS} working voltage; Basic insulation per CSA 61010-1 and IEC 61010-1 600 V_{RMS} working voltage; Basic insulation per CSA 60950-1 and IEC 60950-1 760 V_{RMS} working voltage	Single protection, 2500 V_{RMS}
Certificate number: 40047657	Master contract number: 220991	File number: E181974

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 80.5°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			282	mA
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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6.9 Electrical Characteristics: Driver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential-output voltage magnitude	I_O = 0 mA, no load	3	4.3	V_{CC2}	V
		R_L = 54 Ω, See Figure 17	1.5	2.3		V
		R_L = 100 Ω (RS-422), See Figure 17	2	2.3		V
		V_{test} from –7 V to +12 V, See Figure 18	1.5			V
$\Delta\|V_{OD}\|$	Change in differential output voltage between two states	See Figure 17 and Figure 18	–200		200	mV
$V_{OC(SS)}$	Common-mode output voltage	See Figure 19	1	2.6	3	V
$\Delta V_{OC(SS)}$	change in steady-state common-mode output voltage between two states		–100		100	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			0.5		V
I_I	Input current	D, DE, VI at 0 V or V_{CC1}	–10		10	µA
I_{OZ}	High-impedance state output current	V_Y or V_Z = 12 V, V_{CC2} = 0 V or 5 V, DE = 0 V, Other input at 0 V			1	µA
I_{OZ}	High-impedance state output current	V_Y or V_Z = -7 V, V_{CC2} = 0 V or 5 V, DE = 0 V, Other input at 0 V	-1			µA
I_{OS}	Short-circuit output current	V_A or V_B at –7 V, Other input at 0 V	–200		200	mA
I_{OS}	Short-circuit output current	V_A or V_B at 12 V, Other input at 0 V	–200		200	mA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 14 and Figure 15	25	50		kV/µs

6.10 Electrical Characteristics: Receiver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA		-85	–10	mV
$V_{IT–}$	Negative-going input threshold voltage	I_O = 8 mA	–200	-115		mV
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)			30		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_O = -8 mA, 3.3 V V_{CC1}	V_{CC1} – 0.4	3.1		V
	High-level output voltage	V_{ID} = 200 mV, I_O = -8 mA, 5 V V_{CC1}	4	4.8		V
V_{OL}	Low-level output voltage	V_{ID} = -200 mV, I_O = 8 mA, 3.3 V V_{CC1}		0.15	0.4	V
	Low-level output voltage	V_{ID} = -200 mV, I_O = 8 mA, 5 V V_{CC1}		0.15	0.4	V
I_{OZ}	Output high-impedance current on the R pin	V_I = –7 to 12 V, Other input = 0 V	–1		1	µA
I_I	Bus input current	V_A or V_B = 12 V, Other input at 0 V		0.04	0.1	mA
		V_A or V_B = 12 V, VCC = 0, Other input at 0 V		0.06	0.13	mA
		V_A or V_B = –7 V, Other input at 0 V	-0.1	-0.04		mA
		V_A or V_B = –7 V, V_{CC} = 0, Other input at 0 V	-0.05	-0.03		mA
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2 V	-10		10	µA
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.8 V	-10		10	µA

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All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ID}	Differential input resistance	A, B	96			kohm
C_{ID}	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		7		pF

6.11 Transformer Driver Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency	V_{CC1} = 5 V ± 10%, D1 and D2 connected to transformer	350	450	610	kHz
f_{OSC}	Oscillator frequency	V_{CC1} = 3.3 V ± 10%, D1 and D2 connected to transformer	300	400	550	kHz
R_{ON}	Switch on resistance	D1 and D2 connected to 50Ω pullup resistors		1	2.5	ohm
t_{r_D}	D1, D2 output rise time	V_{CC1} = 5 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		80		ns
t_{r_D}	D1, D2 output rise time	V_{CC1} = 3.3 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		70		ns
t_{f_D}	D1, D2 output fall time	V_{CC1} = 5 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		55		ns
t_{f_D}	D1, D2 output fall time	V_{CC1} = 3.3 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		80		ns
f_{St}	Startup frequency	V_{CC1} = 2.4 V, D1 and D2 connected to transformer		350		kHz
t_{BBM}	Break before make time delay	V_{CC1} = 5 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		38		ns
t_{BBM}	Break before make time delay	V_{CC1} = 3.3 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		140		ns

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6.12 Supply Current

Bus loaded or unloaded (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER ENABLED, RECEIVER DISABLED					
I_{CC1} (1)	Logic-side supply current, $\overline{RE}$ at 0 V or V_{CC}, DE at 0 V or VC_{C1}, 3.3-V V_{CC1}		5	8	mA
I_{CC1} (1)	Logic-side supply current, $\overline{RE}$ at 0 V or V_{CC}, DE at 0 V or V_{CC1}, 5-V V_{CC1}		7	12	mA
I_{CC2} (1)	Bus-side supply current, $\overline{RE}$ at 0 V or V_{CC}, DE at 0 V, No load		10	15	mA
I_{CC2} (1)	Bus-side supply current, $\overline{RE}$ at 0 V or V_{CC}, DE at V_{CC1}, No load		10	15	mA
CMTI	Common-mode transient immunity, See Figure 28, V_I = V_{CC1} or 0 V	25	50		kV/µs

(1) I_{CC1} and I_{CC2} are measured when device is connected to external power supplies, V_{CC1} and V_{CC2}. In this case, D1 and D2 are open and disconnected from external transformer.

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6.13 Switching Characteristics: Driver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
20-Mbps						
t_{PHL}, t_{PLH}	Propagation delay	See Figure 20		25	45	ns
PWD	Pulse width distortion(1), $\|t_{PHL} - t_{PLH}\|$	See Figure 20		1	7.5	ns
t_R, t_F	Differential output signal rise time and fall time	See Figure 20		7	15	ns
t_{PZH}, t_{PZL}	Propagation delay, high-impedance-tohigh-level output and high-impedance-tolow-level output	See Figure 21, DE at 0 V		25	55	ns
t_{PHZ}, t_{PLZ}	Propagation delay, high-level-to-highimpedance output and low-level to highimpedance output	See Figure 22, DE at 0 V		25	55	ns

(1) Also known as pulse skew.

6.14 Switching Characteristics: Receiver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
20-Mbps						
t_r, t_f	Differential output rise time and fall time	See Figure 24		1		ns
t_{PHL}, t_{PLH}	Propagation delay	See Figure 24		103	125	ns
PWD	Pulse Skew, $\|t_{PHL} - t_{PLH}\|$	See Figure 24		3	15	ns
t_{PHZ}, t_{PZH}	Propagation delay, high-level-tohigh-impedance output and highimpedance-to-high-level output	See Figure 25, DE at 0 V		11	22	ns
t_{PZL}, t_{PLZ}	Propagation delay, highimpedance-to-low-level output and low-level-to-high-impedance output	See Figure 26, DE at 0 V		11	22	ns

6.15 Insulation Characteristics Curves

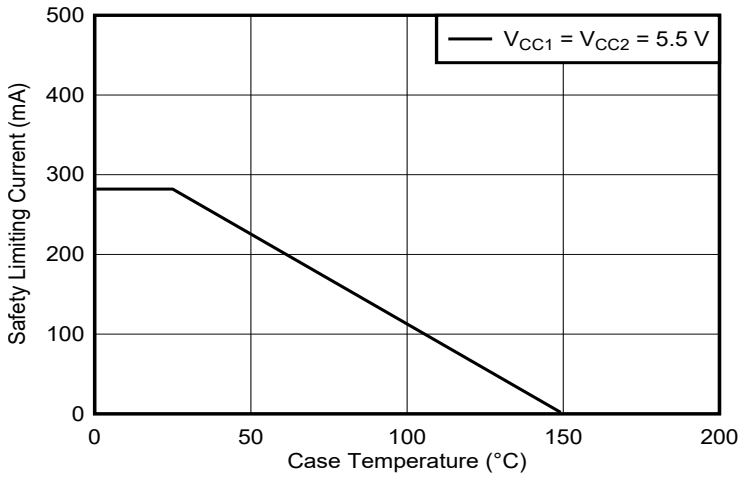
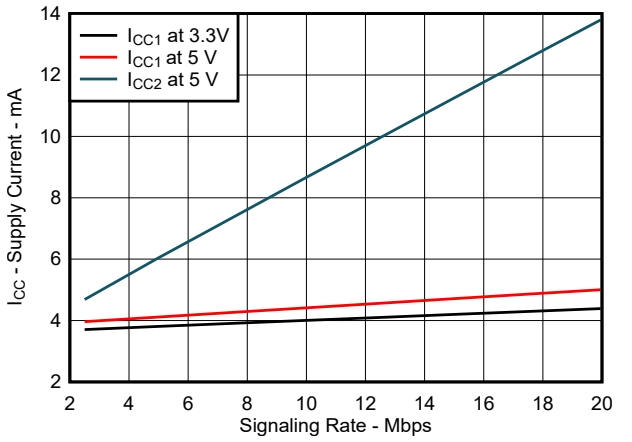


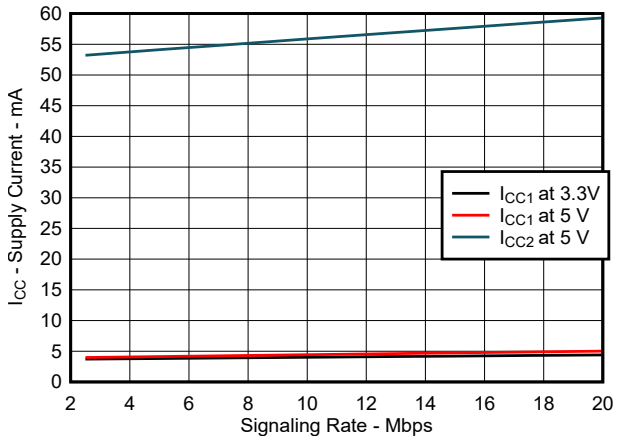
図 6-1. Thermal Derating Curve for Safety Limiting Power for DW-16 Package

6.16 Typical Characteristics



T_A = 25 °C PRBS Data 2^{16} - 1

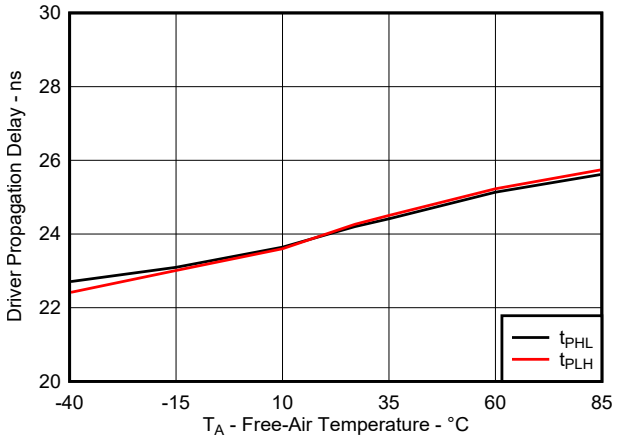
図 6-2. Supply Current vs Signaling Rate (No Load)



T_A = 25 °C Receiver C_L = 15 pF PRBS Data 2^{16} - 1

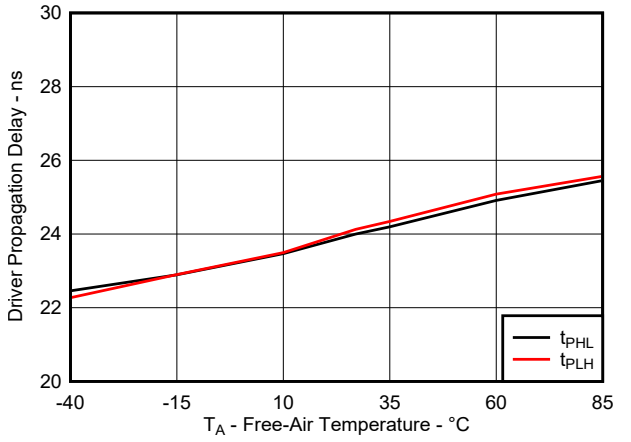
Driver C_L = 50 pF Driver R_L = 54 Ω

図 6-3. Supply Current vs Signaling Rate (With Load)



V_{CC1} = V_{CC2} = 5 V C_L = 50 pF R_L = 54 Ω

図 6-4. Driver Propagation Delay vs Free-Air Temperature



V_{CC1} = 3.3V, V_{CC2} = 5 V C_L = 50 pF R_L = 54 Ω

図 6-5. Driver Propagation Delay vs Free-Air Temperature

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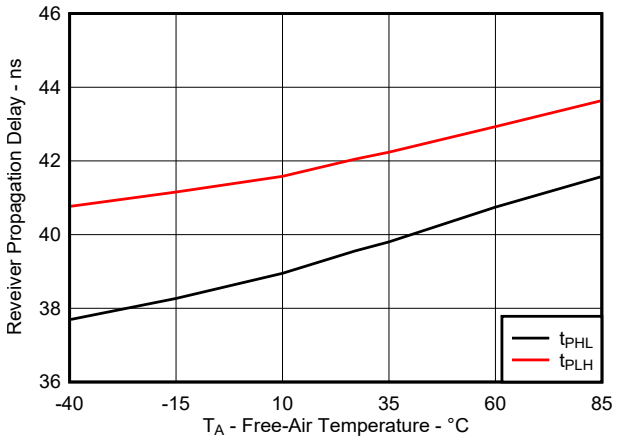
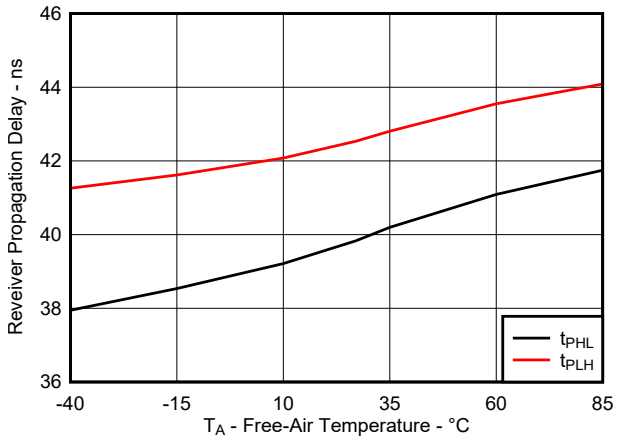
6.16 Typical Characteristics (continued)



V_{CC1} = V_{CC2} = 5 V C_L = 15 pF

図 6-6. Receiver Propagation Delay vs Free-Air Temperature



V_{CC1} = 3.3V, V_{CC2} = 5 V C_L = 15 pF R_L = 54 Ω

図 6-7. Receiver Propagation vs Free-Air Temperature

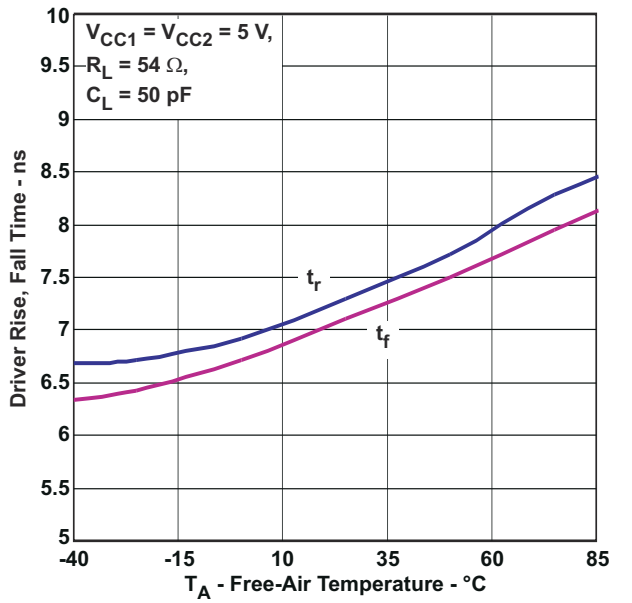


図 6-8. Driver Rise, Fall Time vs Free-Air Temperature

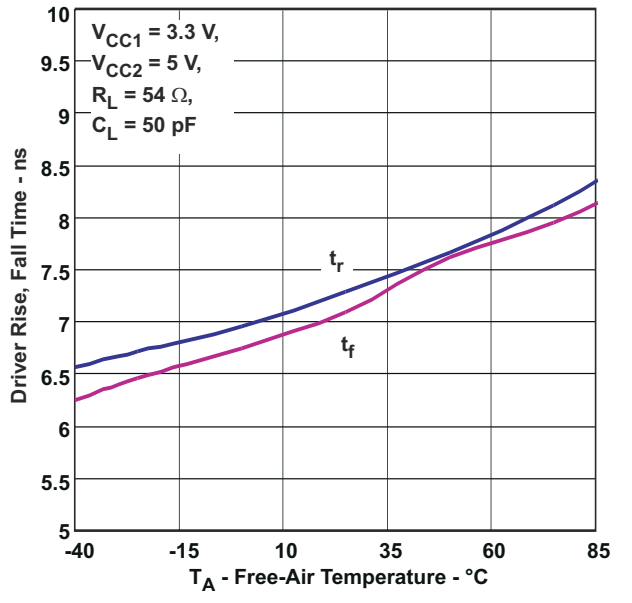


図 6-9. Driver Rise, Fall Time vs Free-Air Temperature

6.16 Typical Characteristics (continued)

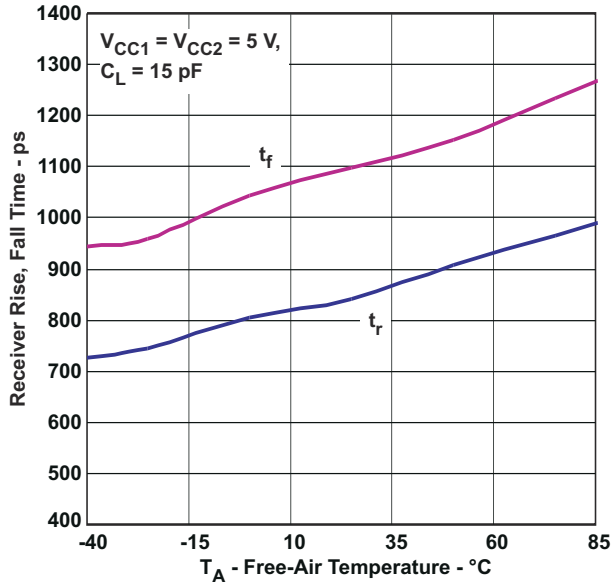


図 6-10. Receiver Rise, Fall Time vs Free-Air Temperature

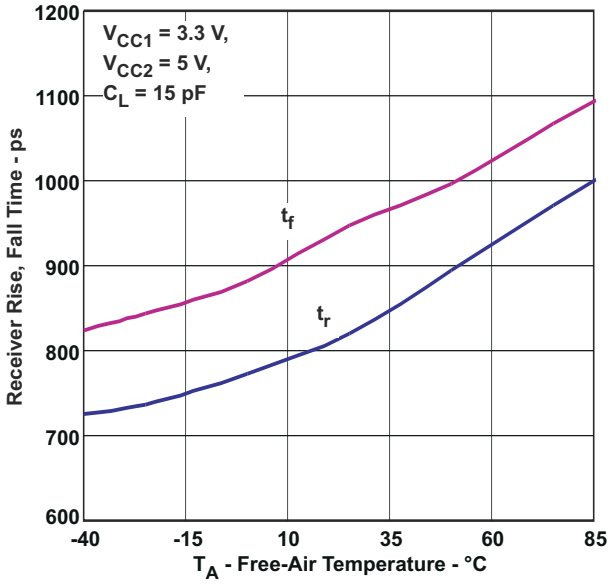


図 6-11. Receiver Rise, Fall Time vs Free-Air Temperature

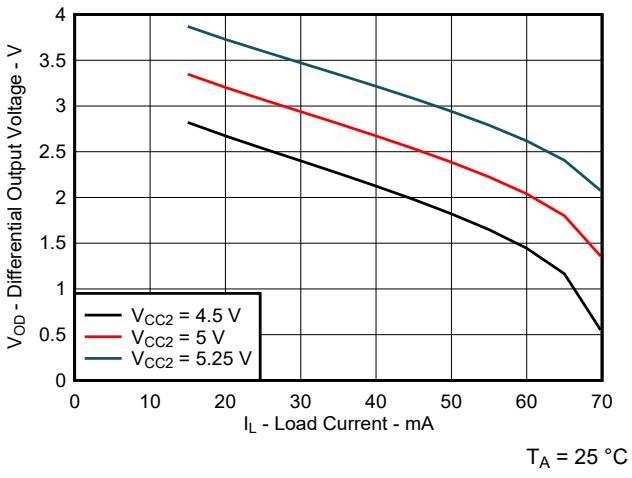


図 6-12. Driver Differential Output Voltage vs Load Current

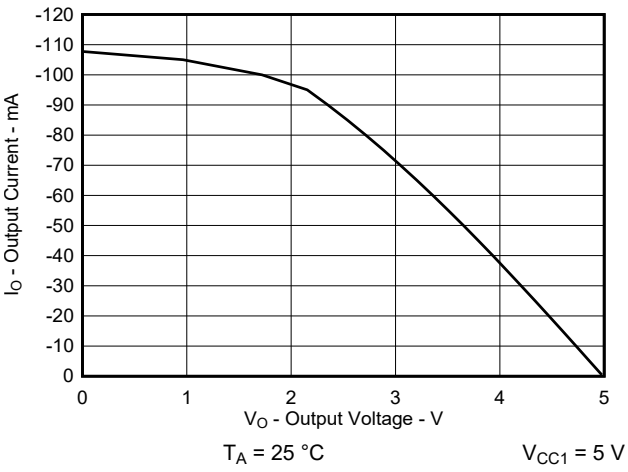


図 6-13. Receiver High-Level Output Current vs High-Level Output Voltage

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6.16 Typical Characteristics (continued)

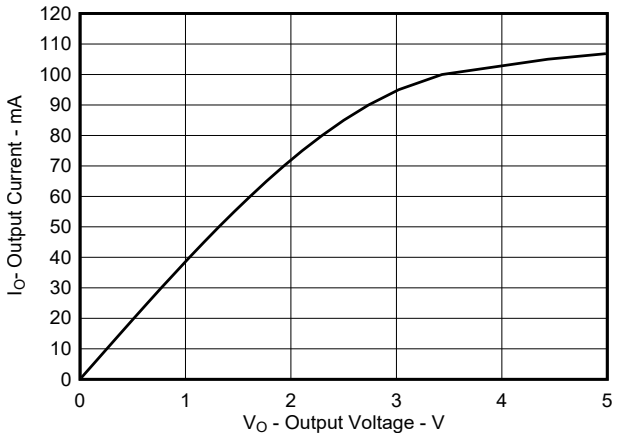


図 6-14. Receiver Low-Level Output Current vs Low-Level Output Voltage

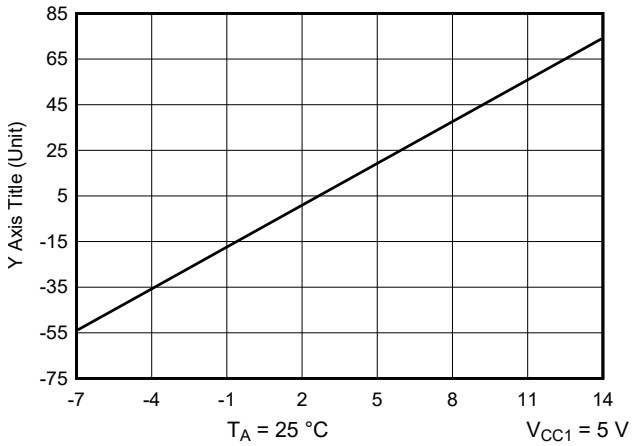


図 6-15. Input Bias Current vs Bus Input Voltage

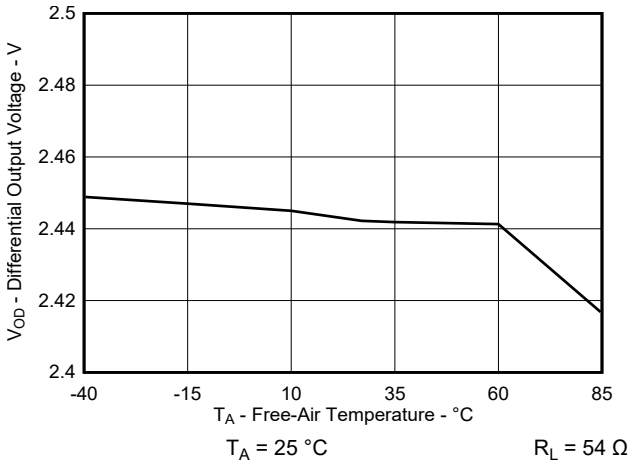


図 6-16. Differential Output Voltage vs Free-Air Temperature

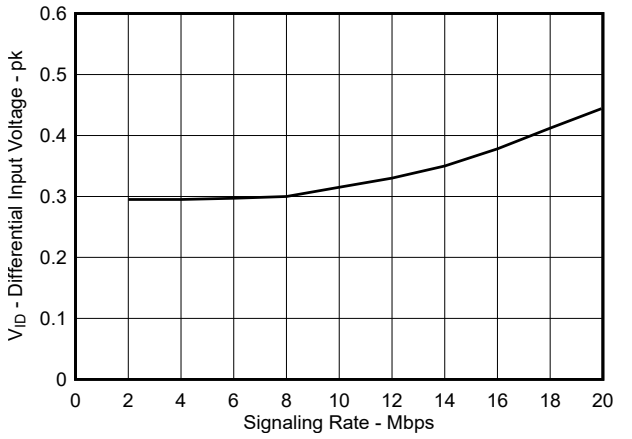


図 6-17. Recommended Minimum Differential Input Voltage vs Signaling Rate

7 Parameter Measurement Information

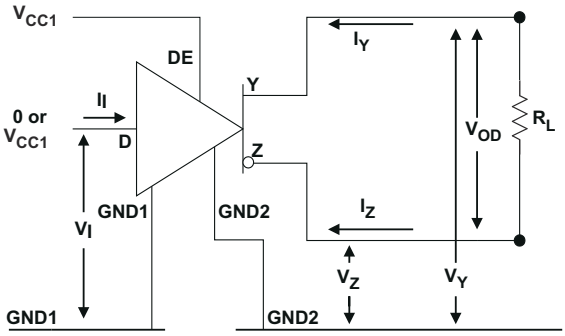


図 7-1. Driver V_{OD} Test and Current Definitions

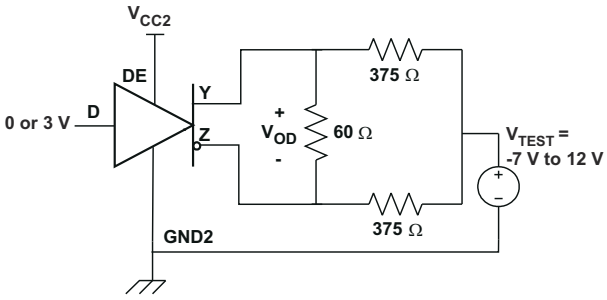
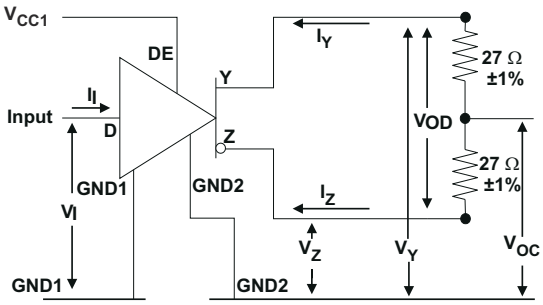


図 7-2. Driver V_{OD} With Common-Mode Loading Test Circuit



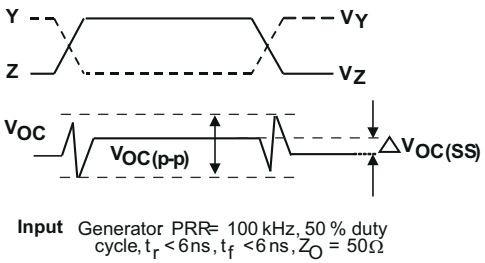
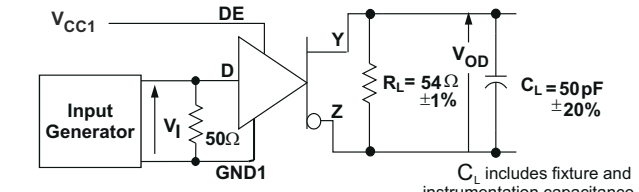


図 7-3. Test Circuit and Waveform Definitions For The Driver Common-Mode Output Voltage



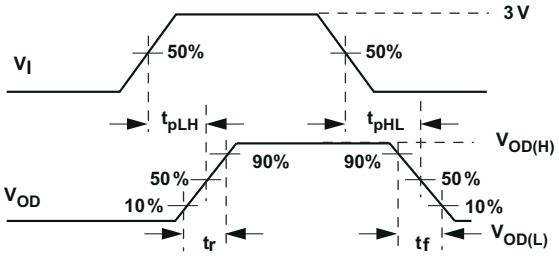
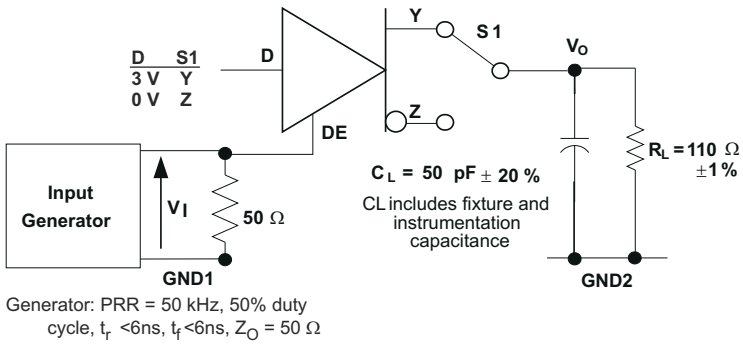


図 7-4. Driver Switching Test Circuit and Voltage Waveforms



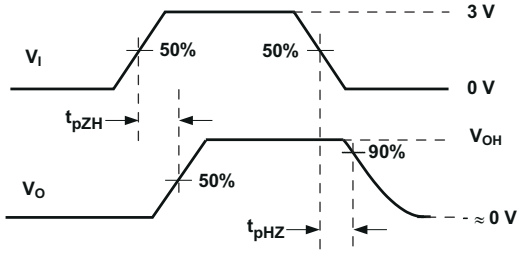


図 7-5. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

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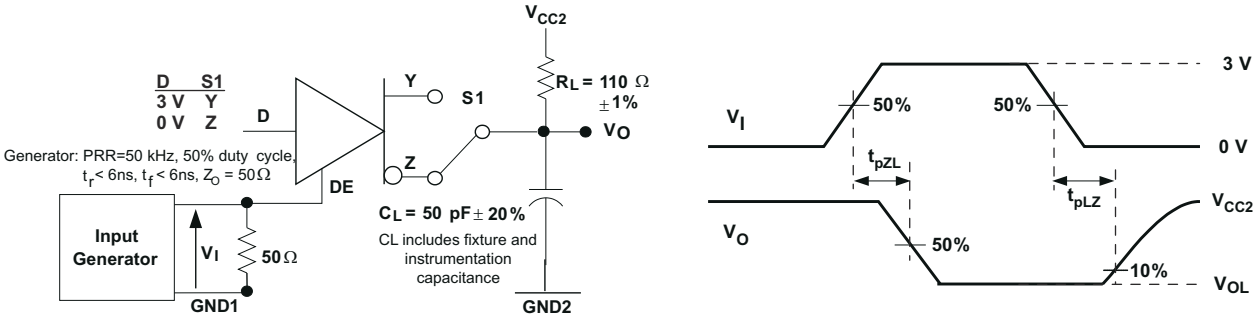

図 7-6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveform

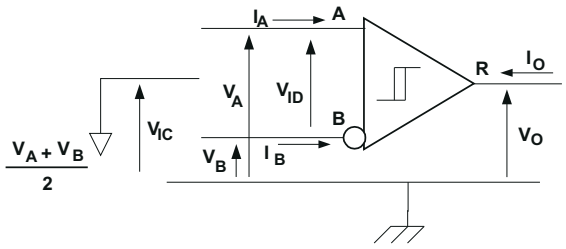

図 7-7. Receiver Voltage and Current Definitions

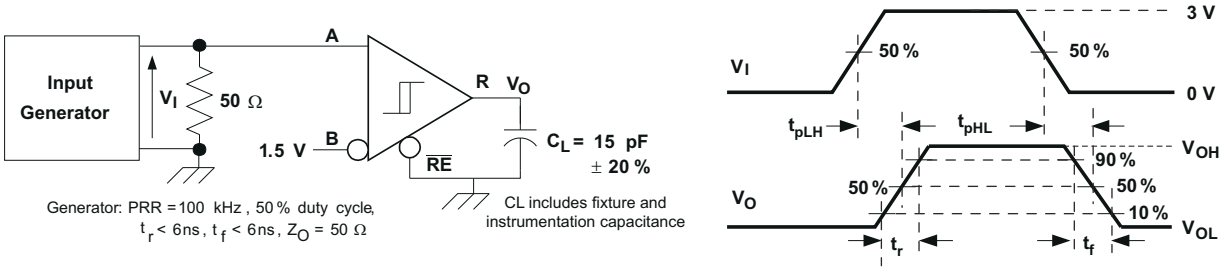

図 7-8. Receiver Switching Test Circuit and Waveforms

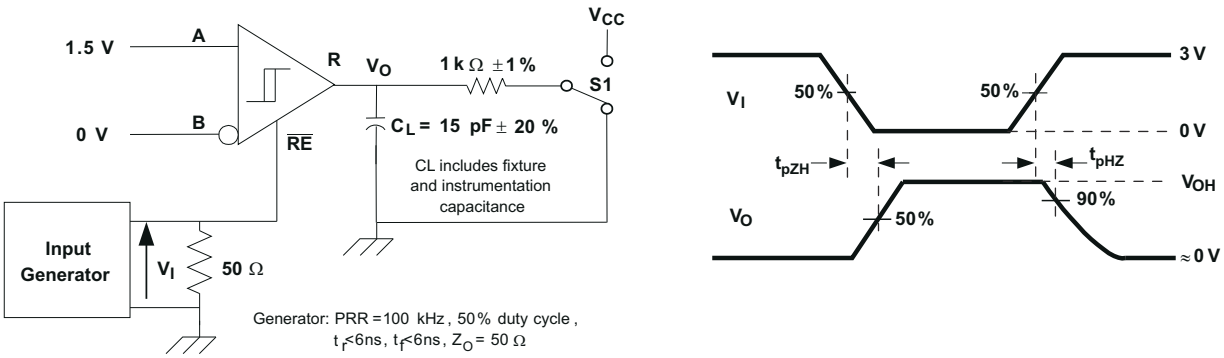

図 7-9. Receiver Enable Test Circuit and Waveforms, Data Output High

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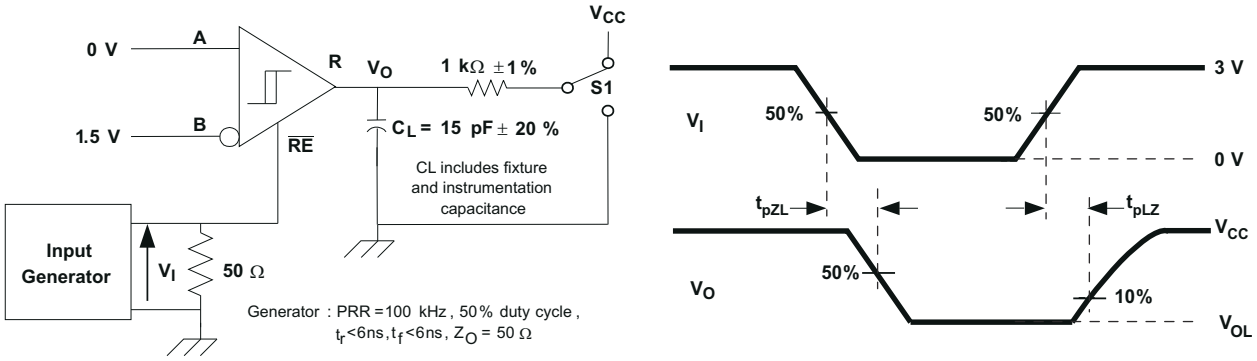

図 7-10. Receiver Enable Test Circuit and Waveforms, Data Output Low

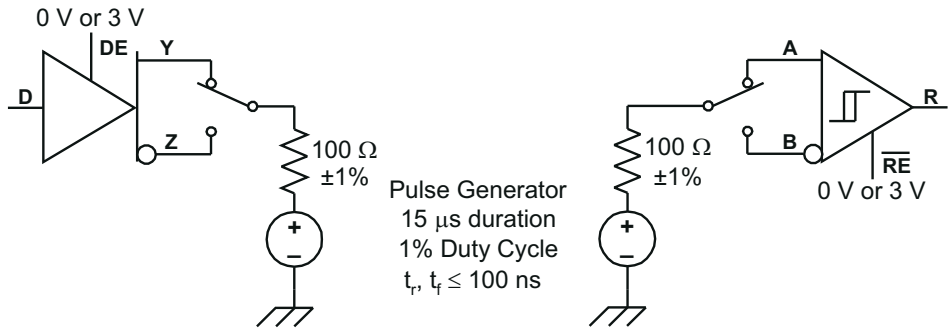

図 7-11. Transient Over-Voltage Test Circuit

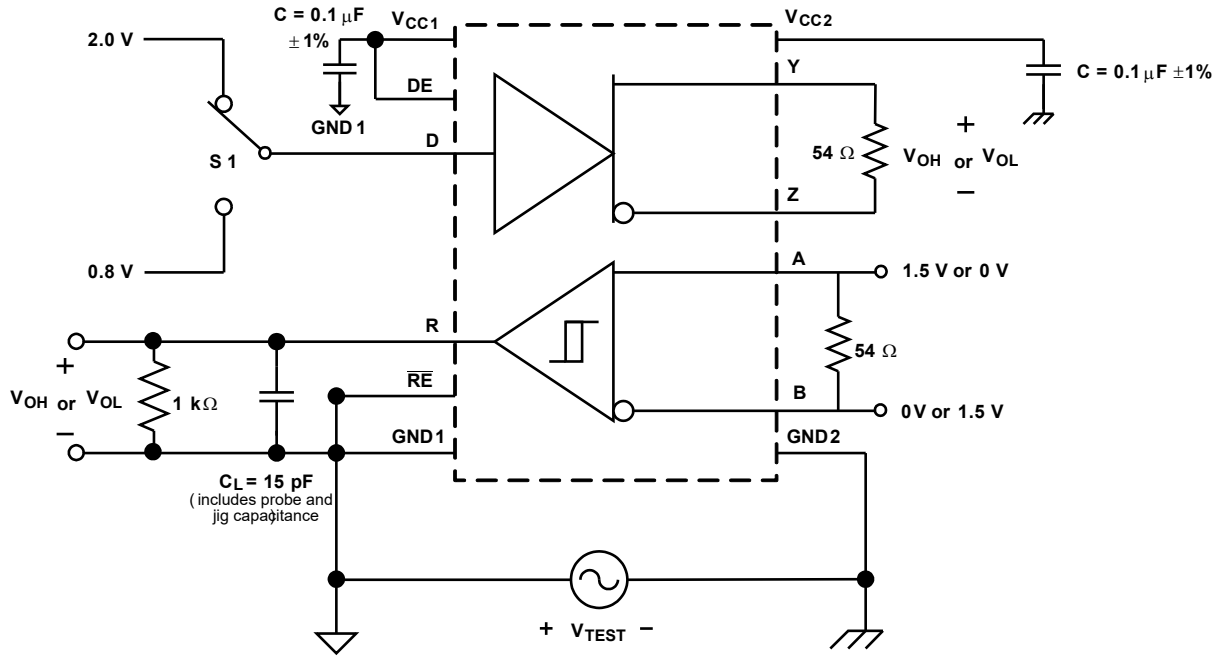

図 7-12. Common-Mode Transient Immunity Test Circuit

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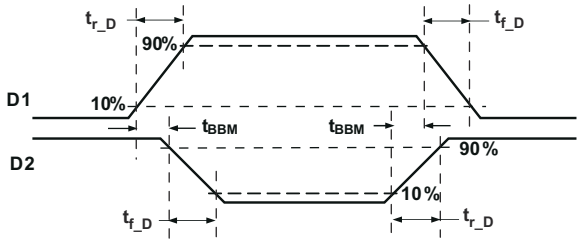

図 7-13. Transition Times and Break-Before-Make Time Delay for D1, D2 Outputs

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8 Detailed Description

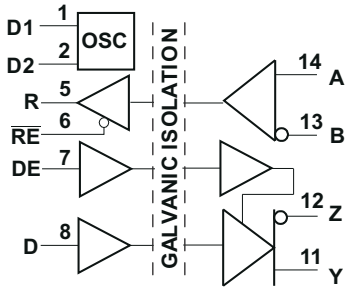
8.1 Overview

ISO3086T is an isolated full-duplex differential transceiver with integrated transformer driver. The integrated transformer driver supports elegant secondary power supply design. This device is rated to provide galvanic isolation up to 4242 V_{PK} per VDE and 2500 V_{RMS} per UL. It has active-high driver enable and active-low receiver enable to control the data flow. It is suitable for data transmission up to 20 Mbps.

When the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as $V_{OD} = V_{(Y)} – V_{(Z)}$ is positive. When D is low, the output states reverse, Z turns high, Y becomes low, and V_{OD} is negative. When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_{(A)} – V_{(B)}$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$ the output is indeterminate. When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

8.2 Functional Block Diagram



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8.3 Device Functional Modes

表 8-1 and 表 8-2 are the function tables for the ISO3086T driver and receiver.

表 8-1. Driver Function Table

INPUT	ENABLE	OUTPUTS	
(D)	(DE)	Y	Z
H	H	H	L
L	H	L	H
X	L	hi-Z	hi-Z
X	OPEN	hi-Z	hi-Z
OPEN	H	H	L

表 8-2. Receiver Function Table

DIFFERENTIAL INPUT $V_{ID} = (V_A – V_B)$	ENABLE ($\overline{RE}$)	OUTPUT (R)
–0.01 V ≤ V_{ID}	L	H
–0.2 V < V_{ID} –0.01 V	L	?
V_{ID} ≤ –0.2 V	L	L
X	H	hi-Z
X	OPEN	hi-Z
Open circuit	L	H
Short Circuit	L	H
Idle (terminated) bus	L	H

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8.3.1 Device I/O Schematics

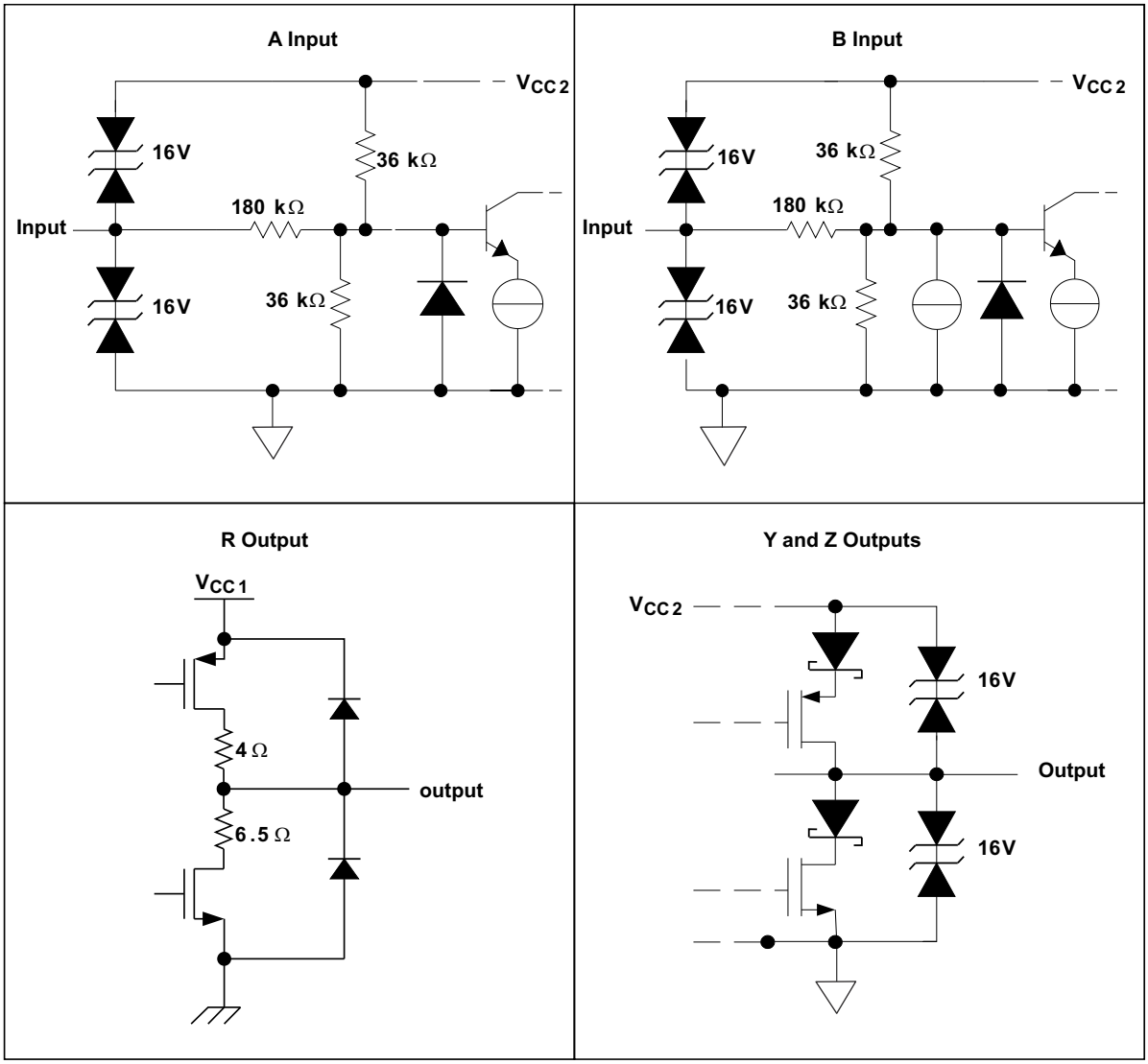

図 8-1. Equivalent Circuit Schematics

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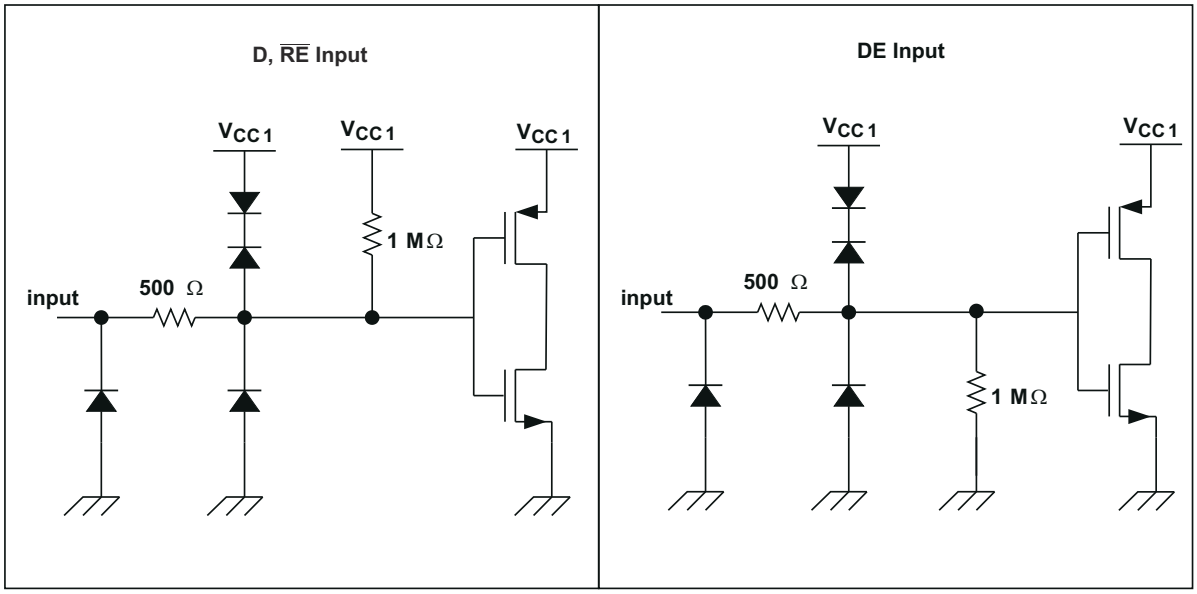

図 8-2. Equivalent Circuit Schematics

9 Application and Implementation

注

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9.1 Application Information

The ISO308T consists of an RS-485 transceiver commonly used for asynchronous data transmissions. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair. To eliminate line reflections, each cable end is terminated with a termination resistor, R(T), whose value matches the characteristic impedance, Z0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

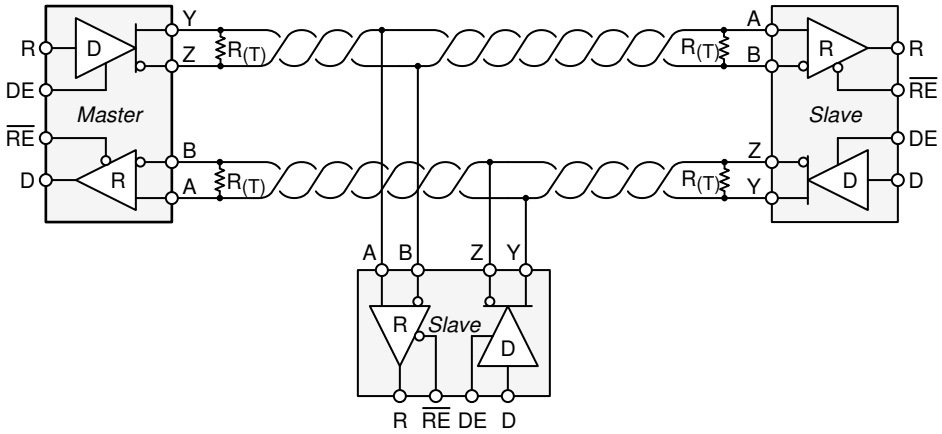

図 9-1. Half-Duplex Transceiver Configurations

9.2 Typical Application

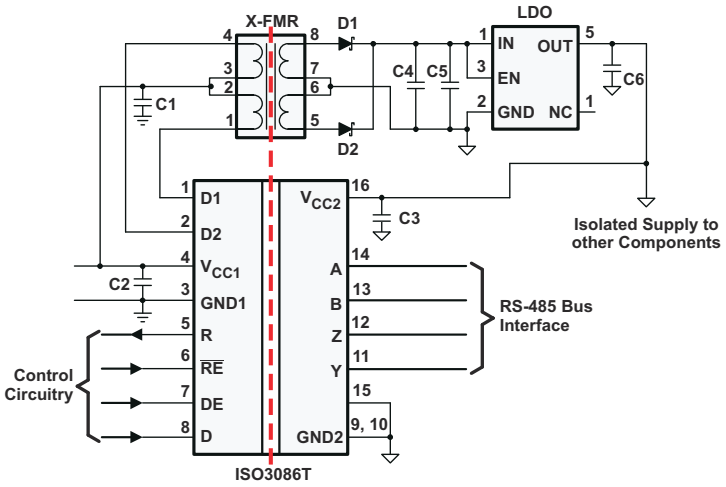

図 9-2. Typical Application Circuit

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9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

表 9-1. Design Parameters

PARAMETER	VALUE
Pullup and Pulldown Resistors	1 kΩ to 10 kΩ
Decoupling Capacitors	100 nF

9.2.2 Detailed Design Procedure

9.2.2.1 Transient Voltages

Isolation of a circuit insulates it from other circuits and earth so that noise develops across the insulation rather than circuit components. The most common noise threat to data-line circuits is voltage surges or electrical fast transients that occur after installation and the transient ratings of the ISO3086T are sufficient for all but the most severe installations. However, some equipment manufacturers use their ESD generators to test transient susceptibility of their equipment and can easily exceed insulation ratings. ESD generators simulate static discharges that may occur during device or equipment handling with low-energy but very high voltage transients.

図 9-3 models the ISO3086T bus IO connected to a noise generator. C_{IN} and R_{IN} is the device and any other stray or added capacitance or resistance across the A or B pin to GND2, C_{ISO} and R_{ISO} is the capacitance and resistance between GND1 and GND2 of the ISO3086T plus those of any other insulation (transformer, etc.), and we assume stray inductance negligible. From this model, the voltage at the isolated bus return is shown in 式 1 and will always be less than 16 V from V_N.

$$v_{GND2} = v_N \frac{Z_{ISO}}{Z_{ISO} + Z_{IN}} \tag{1}$$

If the ISO3086T are tested as a stand-alone device, R_{IN}= 6 × 10^4Ω, C_{IN}= 16 × 10^{-12} F, R_{ISO}= 10^9Ω and C_{ISO}= 10^{-12} F.

In 図 9-3 the resistor ratio determines the voltage ratio at low frequency and it is the inverse capacitance ratio at high frequency. In the stand-alone case and for low frequency, use 式 2, or essentially all of noise appears across the barrier.

$$\frac{v_{GND2}}{v_N} = \frac{R_{ISO}}{R_{ISO} + R_{IN}} = \frac{10^9}{10^9 + 6 \times 10^4} \tag{2}$$

At very high frequency, 式 3 is true, and 94% of V_N appears across the barrier.

$$\frac{v_{GND2}}{v_N} = \frac{\frac{1}{C_{ISO}}}{\frac{1}{C_{ISO}} + \frac{1}{C_{IN}}} = \frac{1}{1 + \frac{C_{ISO}}{C_{IN}}} = \frac{1}{1 + \frac{1}{16}} = 0.94 \tag{3}$$

As long as R_{ISO} is greater than R_{IN} and C_{ISO} is less than C_{IN}, most of transient noise appears across the isolation barrier, as it should.

TI recommends not testing equipment transient susceptibility with ESD generators or consider product claims of ESD ratings above the barrier transient ratings of an isolated interface. ESD is best managed through recessing or covering connector pins in a conductive connector shell and installer training.

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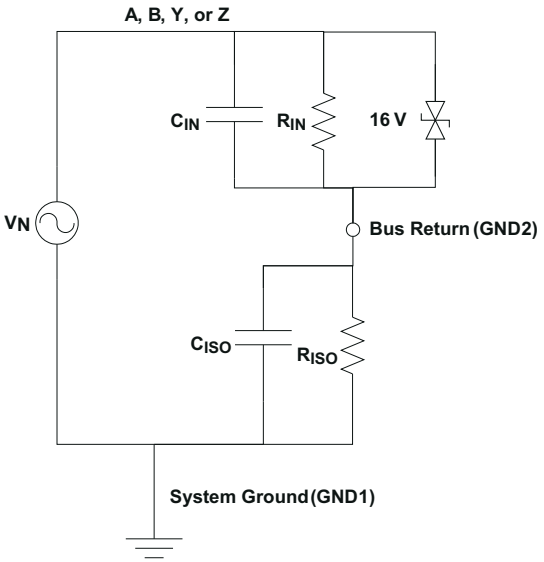

図 9-3. Noise Model

9.2.3 Application Curve

At maximum working voltage, ISO3086T isolation barrier has more than 28 years of life.

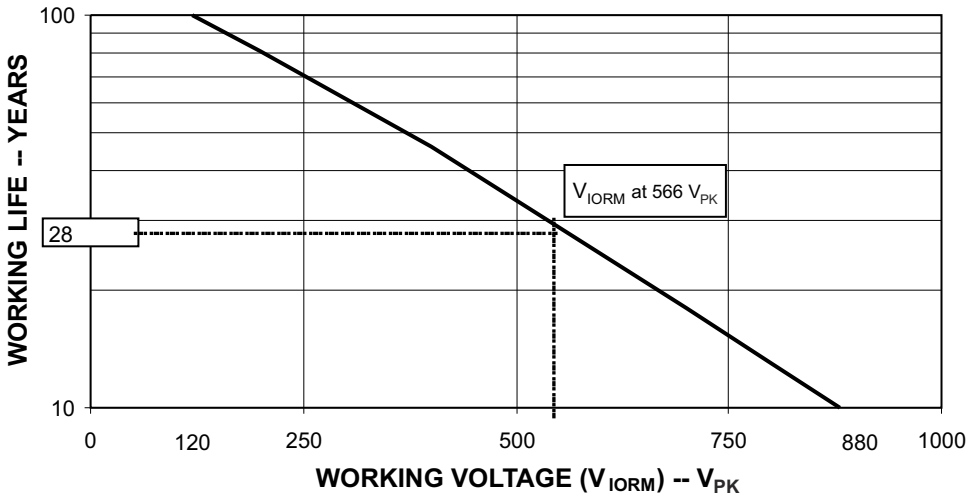

図 9-4. Time-Dependent Dielectric Breakdown Test Results

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10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, TI recommends a 0.1-µF bypass capacitor at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. This device is used in applications where only a single primary-side power supply is available. Isolated power can be generated for the secondary-side with the help of integrated transformer driver.

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11 Layout

11.1 Layout Guidelines

ON-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design. A minimum of four layers is required to accomplish a low EMI PCB design (see 図 11-1).

- Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
- Use V_{CC} and ground planes to provide low-inductance. High-frequency currents might follow the path of least inductance and not necessarily the path of least resistance.
- Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
- Apply 0.1-µF bypass capacitors as close as possible to the V_{CC}-pins of transceiver, UART, and controller ICs on the board.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
- Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.
- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.

If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

注

For detailed layout recommendations, see Application Note *Digital Isolator Design Guide*, SLLA284.

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11.2 Layout Example

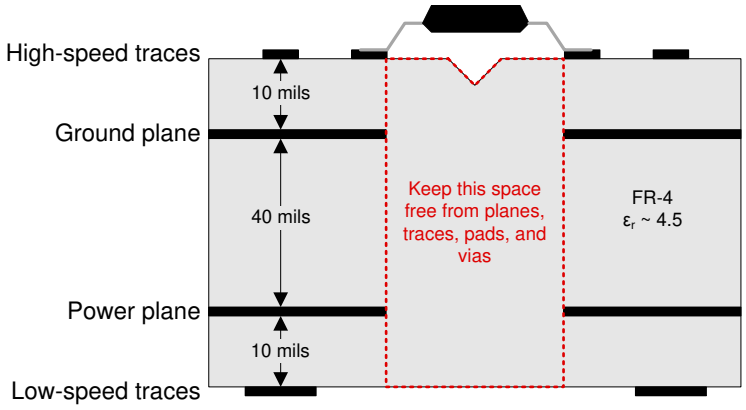

図 11-1. Recommended Layer Stack

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolated, Full-Duplex, 20-Mbps, 3.3-V to 5-V RS-485 Interface* reference guide
- Texas Instruments, *Digital Isolator Design Guide* application report
- Texas Instruments, *Isolation Glossary* application report

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12.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO3086TDW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-40 to 85	ISO3086T
ISO3086TDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3086T
ISO3086TDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3086T
ISO3086TDWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
ISO3086TDWRG4	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3086T
ISO3086TDWRG4.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3086T
ISO3086TDWRG4.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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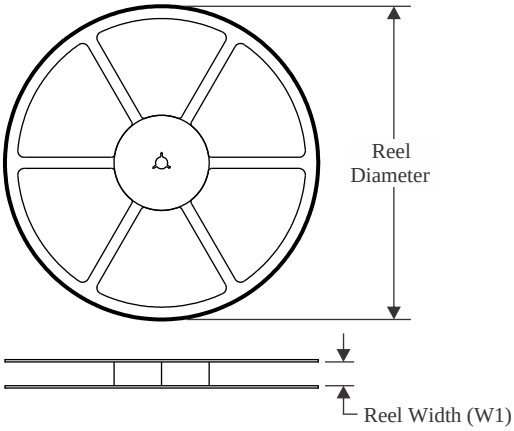
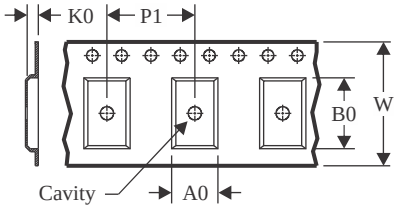
TAPE AND REEL INFORMATION

REEL DIMENSIONS

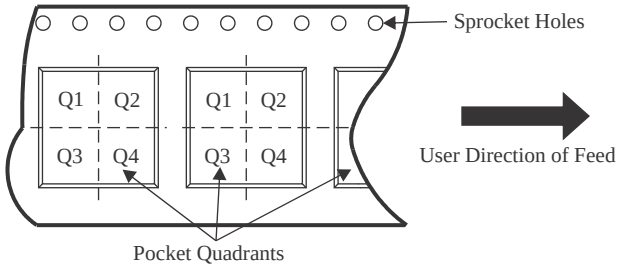


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

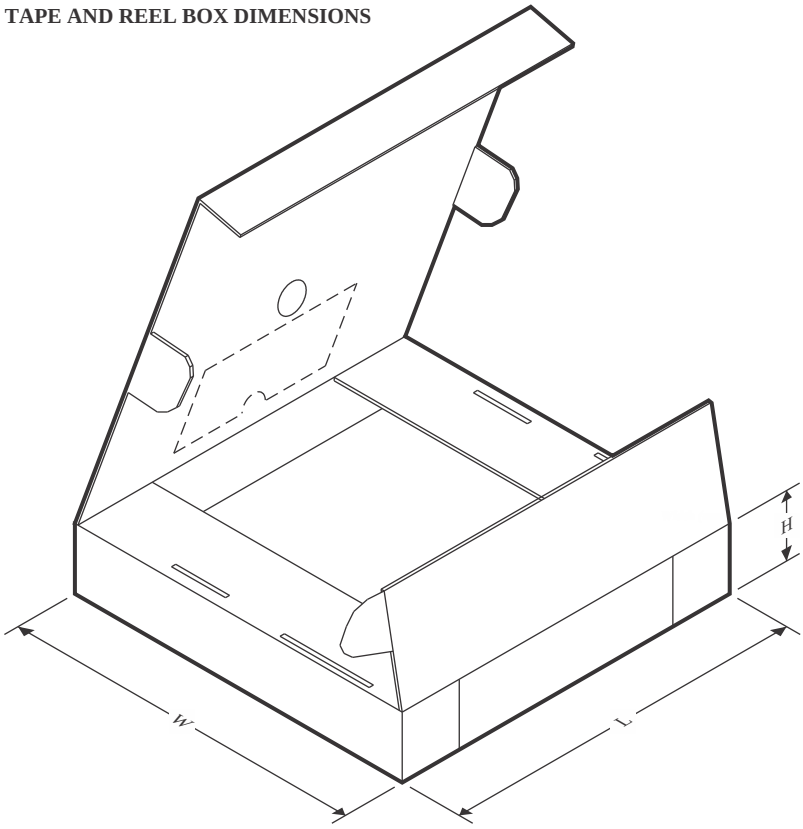
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO3086TDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO3086TDWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO3086TDWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO3086TDWRG4	SOIC	DW	16	2000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

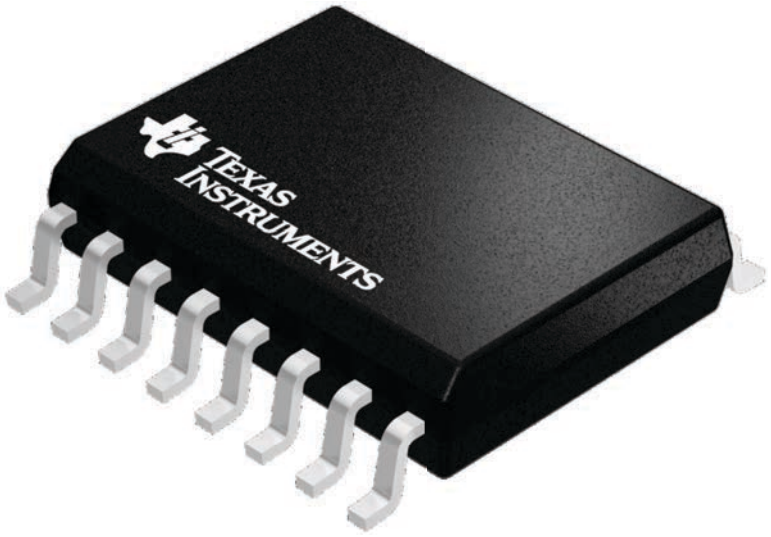
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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