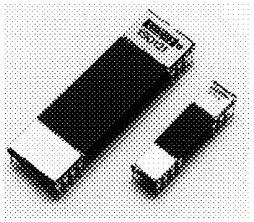
BURR-BROWN®



ISO120
ISO121

Precision Low Cost ISOLATION AMPLIFIER

FEATURES

- 100% TESTED FOR PARTIAL DISCHARGE
- ISO120: Rated 1500Vrms
- ISO121: Rated 3500Vrms
- HIGH IMR: 115dB at 60Hz
- USER CONTROL OF CARRIER FREQUENCY
- LOW NONLINEARITY: ±0.01% max
- BIPOLAR OPERATION: V_O = ±10V
- 0.3"-WIDE 24-PIN HERMETIC DIP, ISO120
- SYNCHRONIZATION CAPABILITY
- WIDE TEMP RANGE: –55°C to +125°C (ISO120)

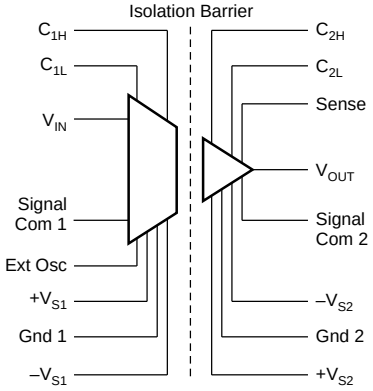
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: Transducer Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4mA to 20mA Loop Isolation
- GROUND LOOP ELIMINATION
- MOTOR AND SCR CONTROL
- POWER MONITORING
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT

DESCRIPTION

The ISO120 and ISO121 are precision isolation amplifiers incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2pF differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity, which results in excellent reliability and good high frequency transient immunity across the barrier. Both the amplifier and barrier capacitors are housed in a hermetic DIP. The ISO120 and ISO121 differ only in package size and isolation voltage rating.

These amplifiers are easy to use. No external components are required for 60kHz bandwidth. With the addition of two external capacitors, precision specifications of 0.01% max nonlinearity and 150µV/°C max V_{OS} drift are guaranteed with 6kHz bandwidth. A power supply range of ±4.5V to ±18V and low quiescent current make these amplifiers ideal for a wide range of applications.



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PDS-820D
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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C: V_{S1} = V_{S2} = ±15V: and R_L = 2kΩ, unless otherwise noted.

PARAMETER	CONDITIONS	ISO120BG, ISO121BG MIN	ISO120BG, ISO121BG TYP	ISO120BG, ISO121BG MAX	ISO120G, ISO120SG[4], ISO121G MIN	ISO120G, ISO120SG[4], ISO121G TYP	ISO120G, ISO120SG[4], ISO121G MAX	UNITS
ISOLATION								
Voltage Rated Continuous ISO120: AC 60Hz	T_{MIN} to T_{MAX}	1500			*			Vrms
DC	T_{MIN} to T_{MAX}	2121			*			VDC
ISO121: AC 60Hz	T_{MIN} to T_{MAX}	3500			*			Vrms
DC	T_{MIN} to T_{MAX}	4950			*			VDC
100% Test (AC 60Hz): ISO120	1s; Partial Discharge ≤ 5pC	2500			*			Vrms
ISO121	1s; Partial Discharge ≤ 5pC	5600			*			Vrms
Isolation Mode Rejection ISO 120: AC 60Hz	1500Vrms		115			*		dB
DC			160			*		dB
ISO121: AC60Hz	3500Vrms		115			*		dB
DC			160			*		dB
Barrier Impedance			10^{14} || 2			*		Ω || pF
Leakage Current	V_{ISO} = 240Vrms, 60Hz		0.18	0.5		*	*	µArms
GAIN[4]	V_O = ±10V							
Nominal Gain	C_1 = C_2 = 1000pF		1			1		V/V
Gain Error			±0.04	±0.1		±0.05	±0.25	%FSR
Gain vs Temperature			±5	±20		±10	±40	ppm/°C
Nonlinearity			±0.005	±0.01		±0.01	±0.05	%FSR
Nominal Gain	C_1 = C_2 = 0		1			1		V/V
Gain Error			±0.04	±0.25		±0.05	±0.25	%FSR
Gain vs Temperature			±40			±40		ppm/°C
Nonlinearity			±0.02	±0.1		±0.04	±0.1	%FSR
INPUT OFFSET VOLTAGE[4]								
Initial Offset	C_1 = C_2 = 1000pF		±5	±25		±10	±50	mV
vs Temperature			±100	±150		±150	±400	µV/°C
Initial Offset	C_1 = C_2 = 0		±25	±100		±40	±100	mV
vs Temperature			±250			±500		µV/°C
Initial Offset								
vs Supply	±V_{S1} or ±V_{S2} = ±4.5V to ±18V		±2			±2		mV/V
Noise			4			4		µV/√Hz
INPUT								
Voltage Range[1]		±10	±15		*	*		V
Resistance			200			*		kΩ
OUTPUT								
Voltage Range		±10	±12.5		*	*		V
Current Drive		±5	±15		*	*		mA
Capacitive Load Drive			0.1			*		µF
Ripple Voltage[2]			10			*		mVp-p
FREQUENCY RESPONSE								
Small Signal Bandwith	C_1 = C_2 = 0		60			*		kHz
	C_1 = C_2 = 1000pF		6			*		kHz
Slew Rate			2			*		V/µs
Settling Time	V_O = ±10V							
0.1%	C_2 = 100pF		50			*		µs
0.01%	C_1 = C_2 = 1000pF		350			*		µs
Overload Recovery Time[3]	50% Output Overload, C_1 = C_2 = 0		150			*		µs
POWER SUPPLIES								
Rated Voltage			15			*		V
Voltage Range		±4.5		±18	*		*	V
Quiescent Current: V_{S1}			±4.0	±5.5		*	*	mA
V_{S2}			±5.0	±6.5		*	*	mA
TEMPERATURE RANGE								
Specification: BG and G		–25		85	–25		85	°C
SG[4]		–25		85	–55		125	°C
Operating		–55		125	–55		125	°C
Storage		–65		150	–55		150	°C
θ_{JA}: ISO120			40			40		°C/W
ISO121			25			25		°C/W

*Specifications same as ISO120BG, ISO121BG.

NOTE: (1) Input voltage range = ±10V for V_{S1}, V_{S2} = ±4.5VDC to ±18VDC. (2) Ripple frequency is at carrier frequency. (3) Overload recovery is approximately three times the settling time for other values of C_2. (4) The SG-grade is specified –55°C to +125°C; performance of the SG in the –25°C to +85°C temperature range is the same as the BG-grade.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (any supply)	18V
V_{IN}, Sense Voltage	±100V
External Oscillator Input	±25V
Signal Common 1 to Ground 1	±1V
Signal Common 2 to Ground 2	±1V
Continuous Isolation Voltage: ISO120	1500Vrms
ISO121	3500Vrms
V_{ISO}, dv/dt	20kV/µs
Junction Temperature	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Duration	Continuous to Common

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ISO120G	24-Pin DIP	225
ISO120BG	24-Pin DIP	225
ISO120SG	24-Pin DIP	225
ISO121G	40-Pin DIP	206
ISO121BG	40-Pin DIP	206

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

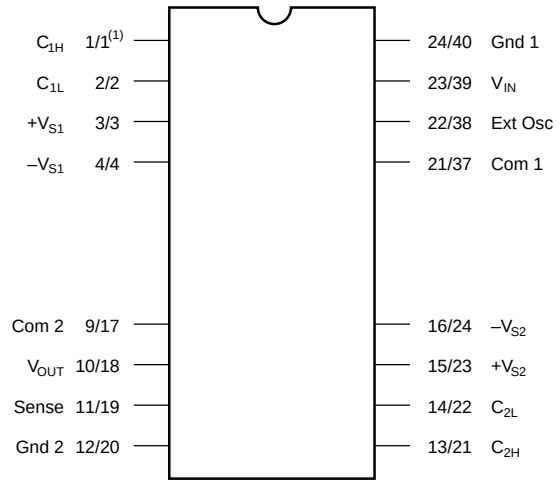
ORDERING INFORMATION

MODEL	TEMPERATURE RANGE
ISO120G	–25°C to 85°C
ISO120BG	–25°C to 85°C
ISO120SG	–55C to 125°C
ISO121G	–25°C to 85°C
ISO121BG	–25°C to 85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

CONNECTION DIAGRAM

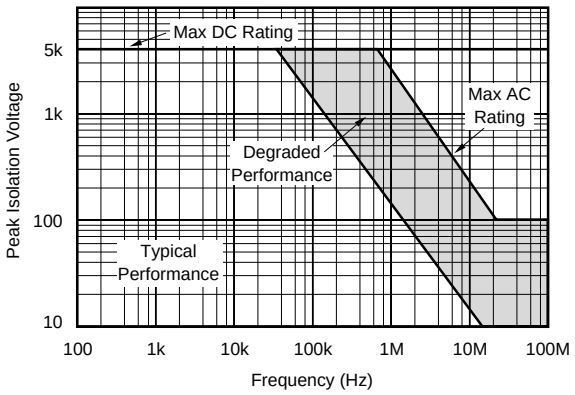


NOTE: (1) First pin number is for ISO120. Second pin number is for ISO121.

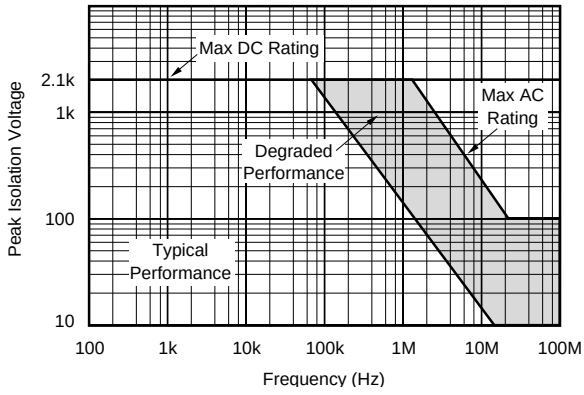
TYPICAL PERFORMANCE CURVES

T_A = +25°C; V_{S1} = V_{S2} = ±15V; and R_L = 2kΩ, unless otherwise noted.

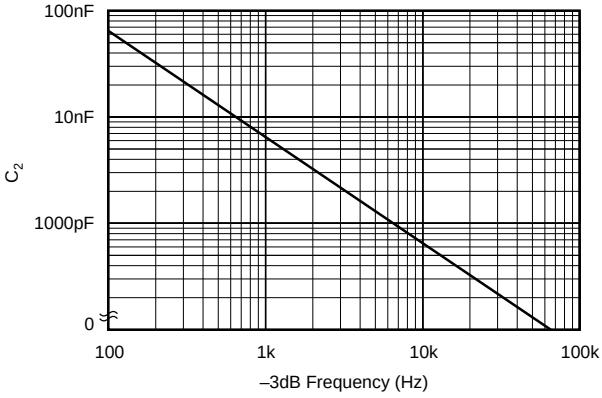
ISOLATION MODE VOLTAGE
vs FREQUENCY ISO121



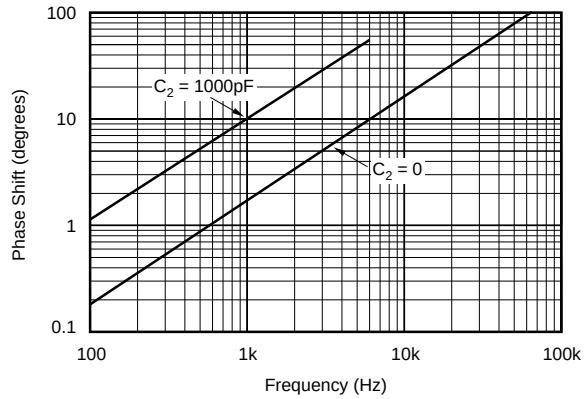
ISOLATION MODE VOLTAGE
vs FREQUENCY ISO120



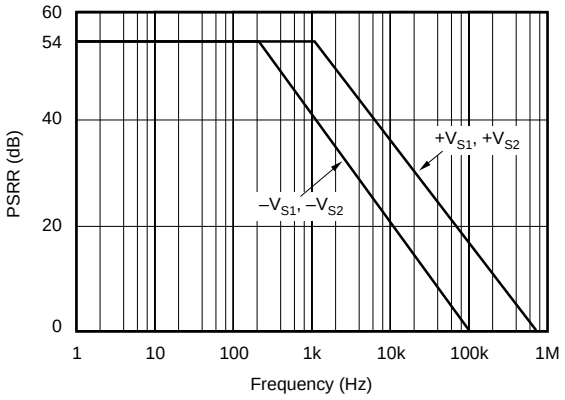
BANDWIDTH vs C_2



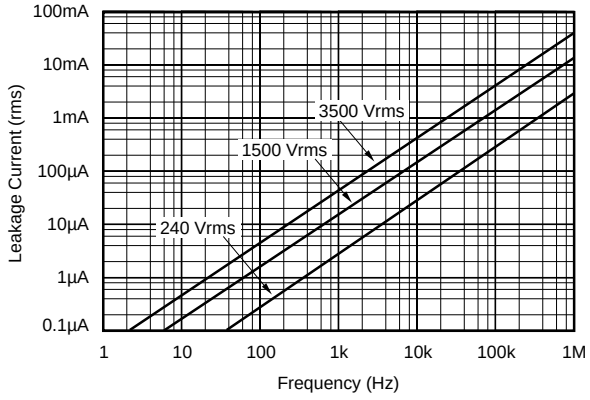
PHASE SHIFT vs C_2



PSRR vs FREQUENCY



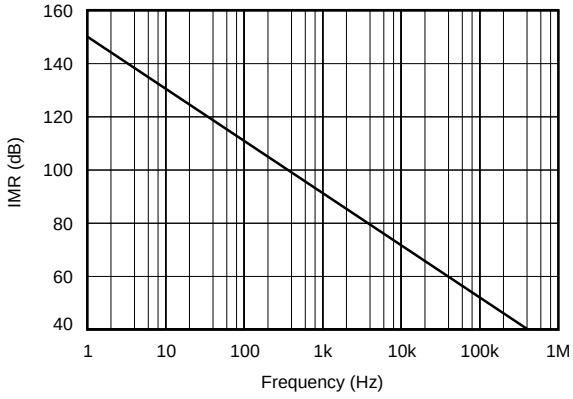
ISOLATION LEAKAGE CURRENT
vs FREQUENCY



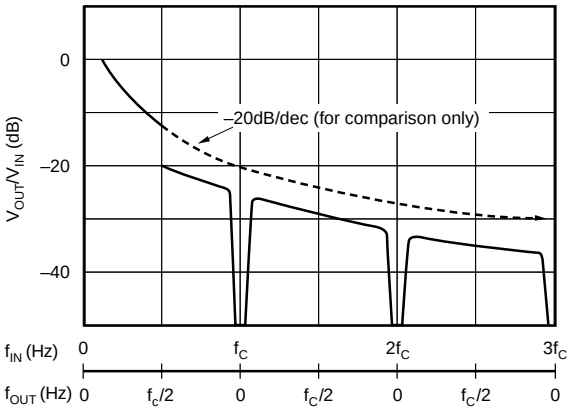
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C; V_{S1} = V_{S2} = ±15V; and R_L = 2kΩ, unless otherwise noted.

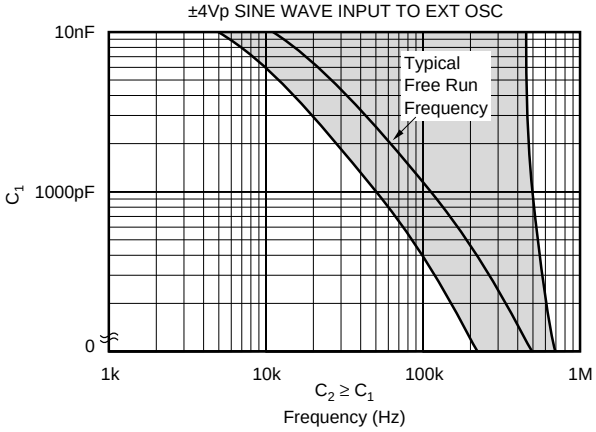
IMR vs FREQUENCY



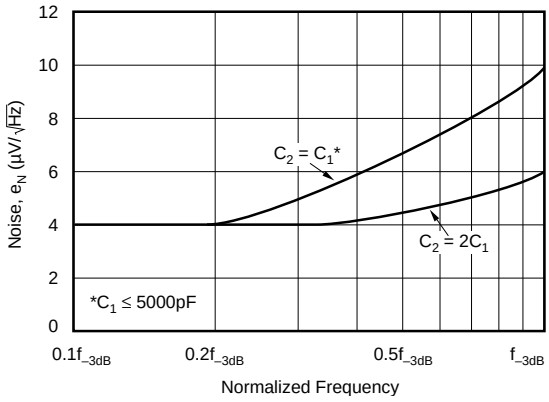
SIGNAL RESPONSE vs CARRIER FREQUENCY



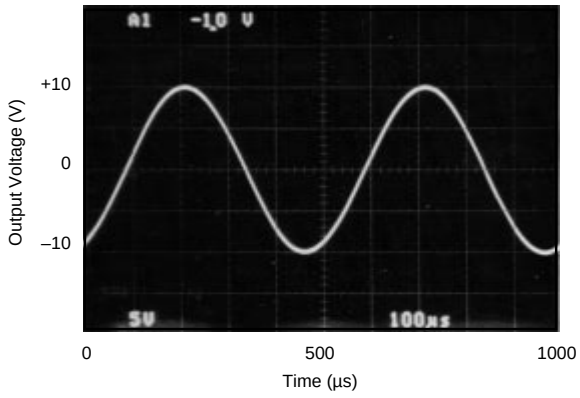
SYNCHRONIZATION RANGE at 25°C
±4Vp SINE WAVE INPUT TO EXT OSC



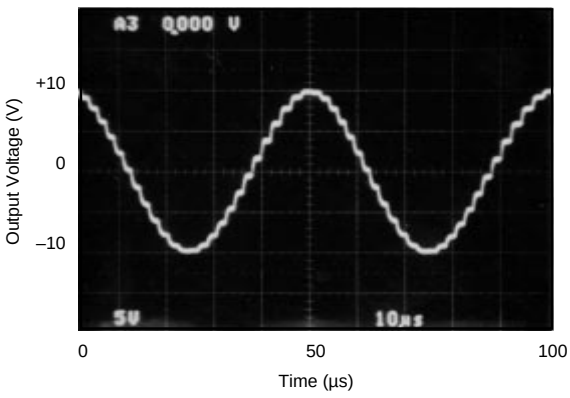
NOISE vs SMALL SIGNAL BANDWIDTH



SINE RESPONSE
(f = 2kHz, C_2 = 0)



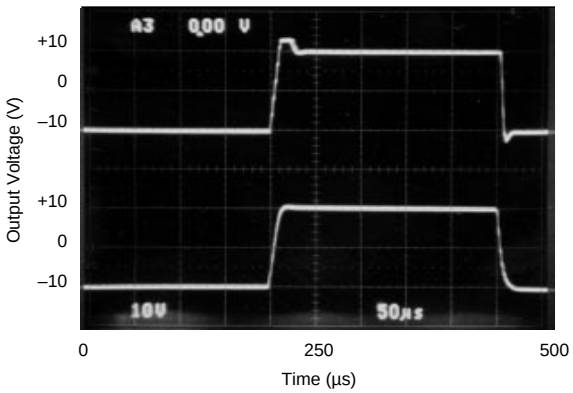
SINE RESPONSE
(f = 20kHz, C_2 = 0)



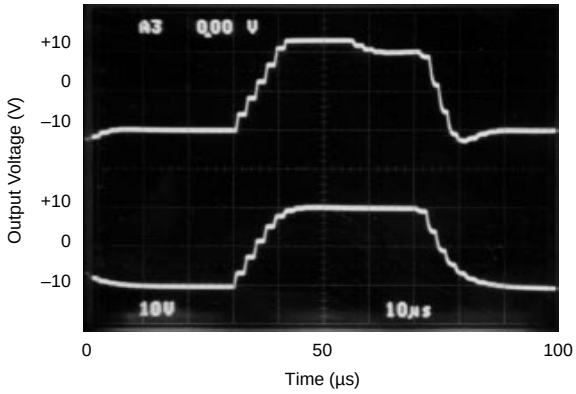
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C; V_{S1} = V_{S2} = ±15V; and R_L = 2kΩ, unless otherwise noted.

STEP RESPONSE



STEP RESPONSE



THEORY OF OPERATION

The ISO120 and ISO121 isolation amplifiers comprise input and output sections galvanically isolated by matched 1pF capacitors built into the ceramic barrier. The input is duty-cycle modulated and transmitted digitally across the barrier. The output section receives the modulated signal, converts it back to an analog voltage and removes the ripple component inherent in the demodulation. The input and output sections are laser-trimmed for exceptional matching of circuitry common to both input and output sections.

FREE-RUNNING MODE

An input amplifier (A1, Figure1) integrates the difference between the input current (V_{IN}/200kΩ) and a switched ±100µA current source. This current source is implemented by a switchable 200µA source and a fixed 100µA current sink. To understand the basic operation of the input section, assume that V_{IN} = 0. The integrator will ramp in one direction until the comparator threshold is exceeded. The comparator and sense amp will force the current source to switch; the resultant signal is a triangular waveform with a 50% duty cycle. If V_{IN} changes, the duty cycle of the integrator will change to keep the average DC value at the output of A1 near zero volts. This action converts the input voltage to a duty-cycle modulated triangular waveform at the output of A1 near zero volts. This action converts the input voltage to a duty-cycle modulated triangular waveform at the output of A1 with a frequency determined by the internal 150pF capacitor. The comparator generates a fast rise time square wave that is simultaneously fed back to keep A1 in charge balance and also across the barrier to a differential sense amplifier with high common-mode rejection characteristics. The sense amplifier drives a switched current source surrounding A2. The output stage balances the duty-cycle modulated current against the feedback current through the 200kΩ feedback resistor, resulting in an average value at the Sense pin equal to V_{IN}. The sample and hold amplifiers in the output feedback loop serve to remove undesired ripple voltages inherent in the demodulation process.

SYNCHRONIZED MODE

A unique feature of the ISO120 and ISO121 is the ability to synchronize the modulator to an external signal source. This capability is useful in eliminating trouble-some beat frequencies in multi-channel systems and in rejecting AC signals and their harmonics. To use this feature, external capacitors are connected at C_1 and C_2 (Figure 1) to change the free-running carrier frequency. An external signal is applied to the Ext Osc pin. This signal forces the current source to switch at the frequency of the external signal. If V_{IN} is zero, and the external source has a 50% duty cycle, operation proceeds as described above, except that the switching frequency is that of the external source. If the external signal has a duty cycle other than 50%, its average value is not zero. At start-up, the current source does not switch until the integrator establishes an output equal to the average DC value of the external signal. At this point, the external signal is able to trigger the current source, producing a triangular waveform, symmetrical about the new DC value, at the output of A1. For V_{IN} = 0, this waveform has a 50% duty cycle. As V_{IN} varies, the waveform retains its DC offset, but varies in duty cycle to maintain charge balance around A1. Operation of the demodulator is the same as outlined above.

Synchronizing to a Sine or Triangle Wave External Clock

The ideal external clock signal for the ISO120/121 is a ±4V sine wave or ±4V, 50% duty-cycle triangle wave. The *ext osc* pin of the ISO120/121 can be driven directly with a ±3V to ±5V sine or 25% to 75% duty-cycle triangle wave and the ISO amp's internal modulator/demodulator circuitry will synchronize to the signal.

Synchronizing to signals below 400kHz requires the addition of two external capacitors to the ISO120/121. Connect one capacitor in parallel with the internal modulator capacitor and connect the other capacitor in parallel with the internal demodulator capacitor as shown in Figure 1.

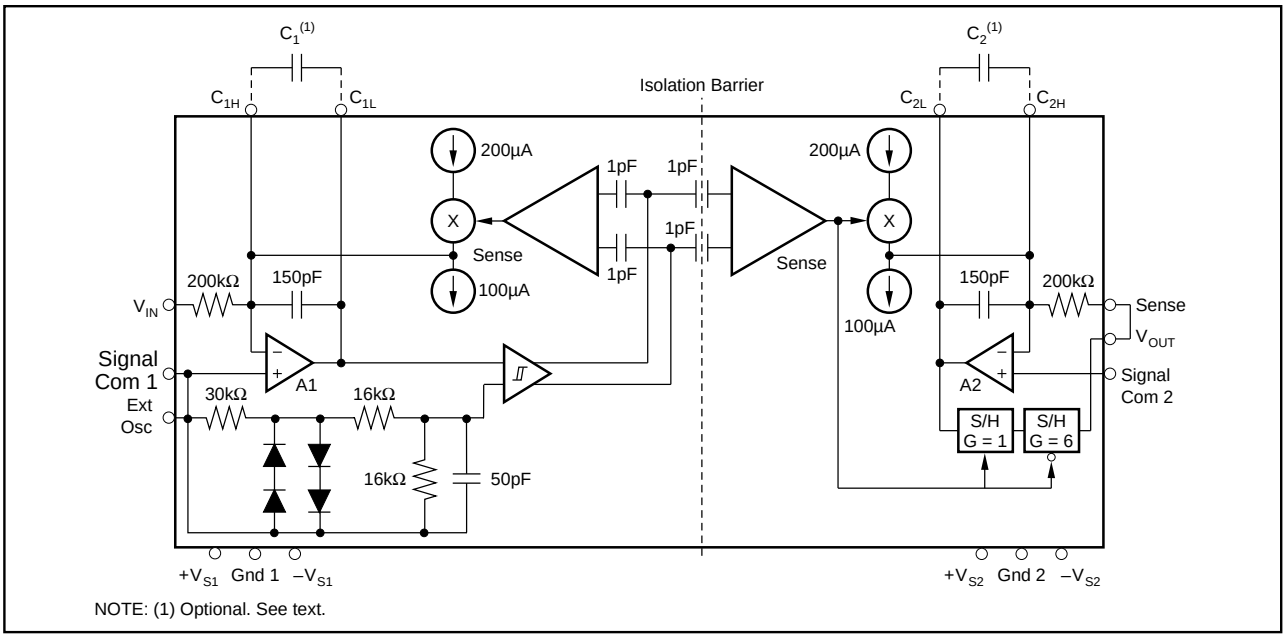


FIGURE 1. Block Diagram.

The value of the external modulator capacitor, C_1, depends on the frequency of the external clock signal. Table I lists recommended values.

EXTERNAL CLOCK FREQUENCY RANGE	C_1, C_2 ISO120/121 MODULATOR, DEMODULATOR EXTERNAL CAPACITOR
400kHz to 700kHz	none
200kHz to 400kHz	500pF
100kHz to 200kHz	1000pF
50kHz to 100kHz	2200pF
20kHz to 50kHz	4700pF
10kHz to 20kHz	0.01µF
5kHz to 10kHz	0.022µF

TABLE I. Recommended ISO120/121 External Modulator/ Demodulator Capacitor Values vs External Clock Frequency.

The value of the external demodulator capacitor, C_2, depends on the value of the external modulator capacitor. To assure stability, C_2 must be greater than $0.8 \cdot C_1$. A larger value for C_2 will decrease bandwidth and improve stability:

$$f_{-3\,dB} \approx \frac{1.2}{200\,k\Omega\,(150\,pF + C_2)}$$

Where:

$f_{-3dB} \approx$ –3dB bandwidth of ISO amp with external C_2 (Hz)
C_2 = External demodulator capacitor (f)

For example, with C_2 = 0.01µF, the f_{-3dB} bandwidth of the ISO120/121 is approximately 600Hz.

Synchronizing to a 400kHz to 700kHz Square-Wave External Clock

At frequencies above 400kHz, an internal clamp and filter provides signal conditioning so that a square-wave signal can be used to directly drive the ISO120/121. A square-wave external clock signal can be used to directly drive the ISO120/121 *ext osc* pin if: the signal is in the 400kHz to 700kHz frequency range with a 25% to 75% duty cycle, and ±3V to ±20V level. Details of the internal clamp and filter circuitry are shown in Figure 1.

Synchronizing to a 10% to 90% Duty-cycle External Clock

With the addition of the signal conditioning circuit shown in Figure 2, any 10% to 90% duty-cycle square-wave signal can be used to drive the ISO120/121 ext osc pin. With the values shown, the circuit can be driven by a 4Vp-p TTL signal. For a higher or lower voltage input, increase or decrease the 1kΩ resistor, R_X, proportionally. e.g. for a ±4V square wave (8Vp-p) R_X should be increased to 2kΩ.

The value of C_X used in the Figure 2 circuit depends on the frequency of the external clock signal. Table II shows recommended capacitor values.

Note: For external clock frequencies below 400kHz, external modulator/demodulator capacitors are required on the ISO120/121 as before.

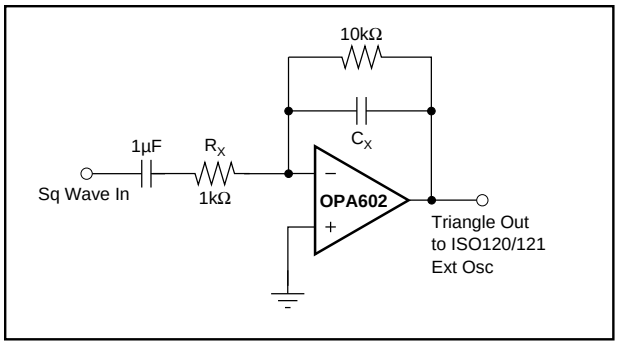


FIGURE 2. Square Wave to Triangle Wave Signal Conditioner for Driving ISO120/121 Ext Osc Pin.

EXTERNAL CLOCK FREQUENCY RANGE	C_x
400kHz to 700kHz	30pF
200kHz to 400kHz	180pF
100kHz to 200kHz	680pF
50kHz to 100kHz	1800pF
20kHz to 50kHz	3300pF
10kHz to 20kHz	0.01µF
5kHz to 10kHz	0.022µF

TABLE II. Recommended C_X Values vs Frequency for Figure 2 Circuit.

BASIC OPERATION

Signal and Power Connections

Figure 3 shows proper power and signal connections. Each power supply pin should be bypassed with 1µF tantalum capacitor located as close to the amplifier as possible. All ground connections should be run independently to a common point if possible. Signal Common on both input and output sections provide a high-impedance point for sensing signal ground in noisy applications. Signal Common must have a path to ground for bias current return and should be maintained within ±1V of Gnd. The output sense pin may be connected directly to V_{OUT} or may be connected to a remote load to eliminate errors due to IR drops. Pins are provided for use of external integrator capacitors. The C_{1H} and C_{2H} pins are connected to the integrator summing junctions and are therefore particularly sensitive to external pickup. This sensitivity will most often appear as degraded IMR or PSR performance. AC or DC currents coupled into these pins results in $V_{ERROR} = I_{ERROR}$ X 200kΩ at the output. Guarding of these pins to their respective Signal Common, or C_{1L} and C_{2L} is strongly recommended. For similar reasons, long traces or physically large capacitors are not desirable. If wound-foil capacitors are used, the outside foil should be connected to C_{1L} and C_{2L}, respectively.

Optional Gain and Offset Adjustments

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 4a may be used to provide a gain trim of ±0.5% for values shown; greater range may be provided by increasing the size of R_1 and R_2. Every 2kΩ increase in R_1 will give an additional 1% adjustment range, with $R_2 \geq 2R_1$. If safety or convenience dictates location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 4a, the positions of R_1 and R_2 may be reversed. Gains greater than one may be obtained by using the circuit of Figure 4b. Note that the effect of input offset errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in inverse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

Figure 5 shows a method for trimming V_{OS} of the ISO120 and ISO121. This circuit may be applied to either Signal Com (input or output) as desired for safety or convenience. With the values shown, ±15V supplies and unity gain, the circuit will provide ±150mV adjustment range and 0.25mV

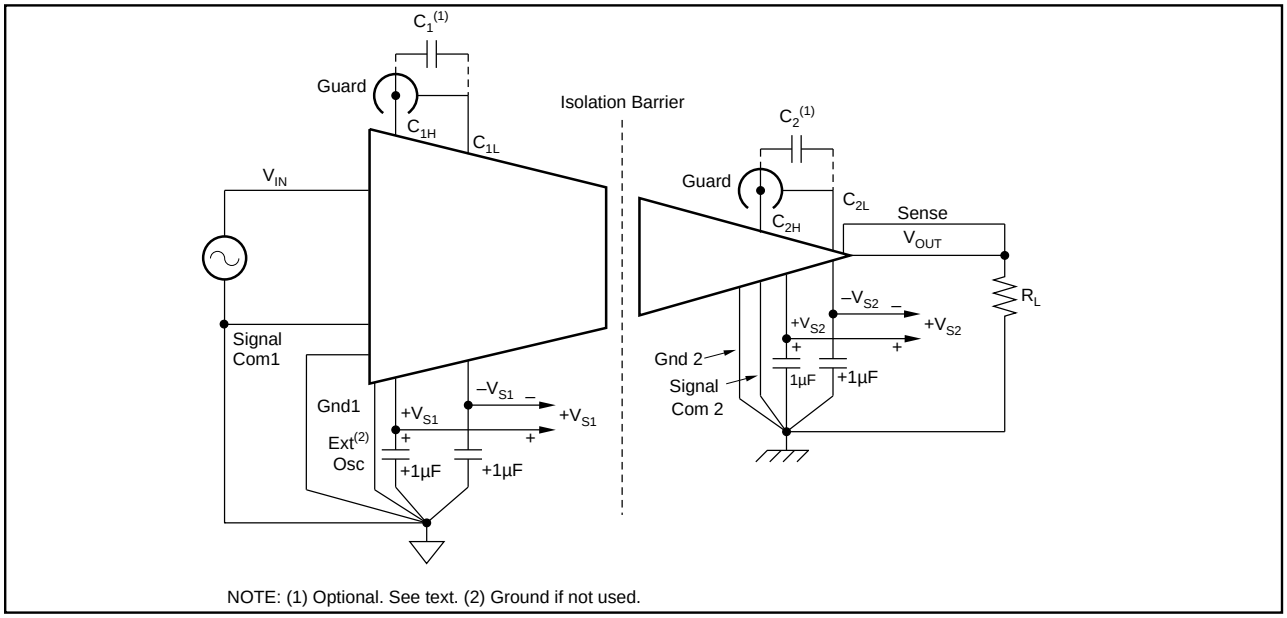


FIGURE 3. Power and Signal Connections.

resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a ±100mV trim, power supply sensitivity is 8mV/V at the output.

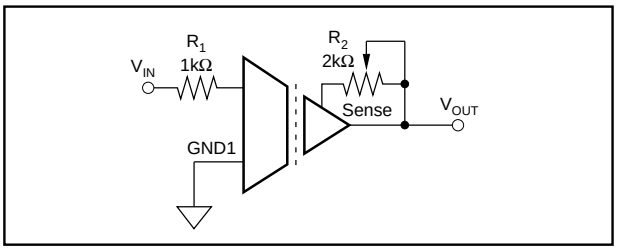


FIGURE 4a. Gain Adjust.

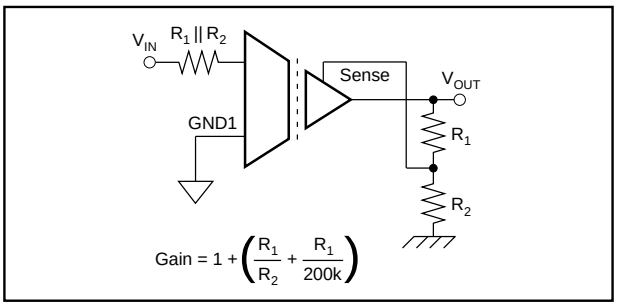


FIGURE 4b. Gain Setting.

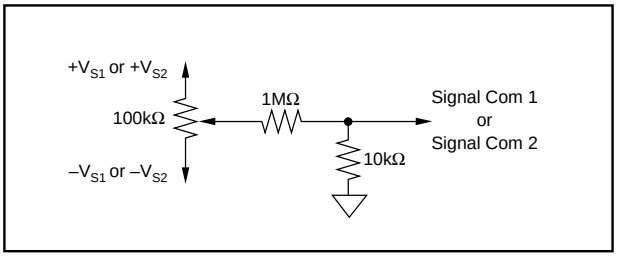


FIGURE 5. V_{OS} Adjust.

CARRIER FREQUENCY CONSIDERATIONS

As previously discussed, the ISO120 and ISO121 amplifiers transmit the signal across the iso-barrier by a duty-cycle modulation technique. This system works like any linear amplifier for input signals having frequencies below one half the carrier frequency, f_C. For signal frequencies above $f_C/2$, the behavior becomes more complex. The Signal Response vs Carrier Frequency performance curve describes this behavior graphically. The upper curve illustrates the response for input signals varying from DC to $f_C/2$. At input frequencies at or above $f_C/2$, the device generates an output signal component that varies in both amplitude and frequency, as shown by the lower curve. The lower horizontal scale shows the periodic variation in the frequency of the output component. Note that at the carrier frequency and its harmonics, both the frequency and amplitude of the response go the zero. These characteristics can be exploited in certain applications. It should be noted that when C_1 is zero, the carrier frequency is nominally 500kHz and the –3dB point of the amplifier is 60kHz. Spurious signals at the output are not significant under these circumstances unless the input signal contains significant components above 250kHz.

There are two ways to use these characteristics. One is to move the carrier frequency low enough that the troublesome signal components are attenuated to an acceptable level as shown in Signal Response vs Carrier Frequency. This in effect limits the bandwidth of the amplifier. The Synchronization Range performance curve shows the relationship between carrier frequency and the value of C_1. To maintain stability, C_2 must also be connected and must be equal to or larger in value than C_1. C_2 may be further increased in value for additional attenuation of the undesired signal components and provides the additional benefit of reducing the residual carrier ripple at the output. See the Bandwidth vs C_2 performance curve.

When periodic noise from external sources such as system clocks and DC/DC converters are a problem, ISO120 and ISO121 can be used to reject this noise. The amplifier can be synchronized to an external frequency source, f_{EXT}, placing the amplifier response curve at one of the frequency and amplitude nulls indicated in the Signal Response vs Carrier Frequency performance curve. For proper synchronization, choose C_1 as shown in the Synchronization Range performance curve. Remember that $C_2 \geq C_1$ is a necessary condition for stability of the isolation amplifier. This curve shows the range of lock at the fundamental frequency for a 4V sinusoidal signal source. The applications section shows the ISO120 and ISO121 synchronized to isolation power supplies, while Figure 6 shows circuitry with opto-isolation suitable for driving the Ext Osc input from TTL levels.

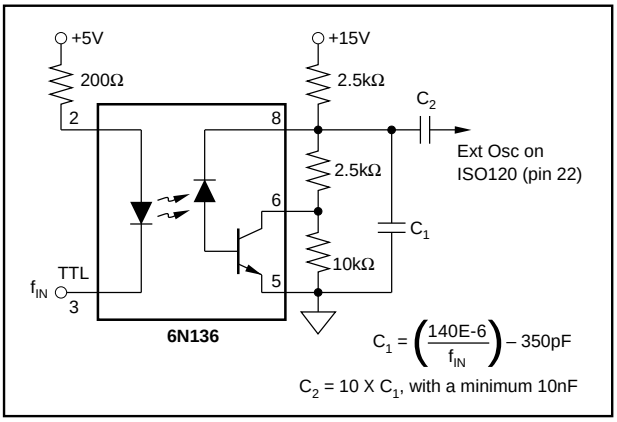


FIGURE 6. Synchronization with Isolated Drive Circuit for Ext Osc Pin.

ISOLATION MODE VOLTAGE

Isolation mode voltage (IMV) is the voltage appearing between isolated grounds Gnd 1 and Gnd 2. IMV can induce error at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds $f_C/2$, the output will display spurious outputs in a manner similar to that described above, and the amplifier response will be identical to that shown in the Signal Response vs Carrier Frequency performance curve. This occurs

because IMV-induced errors behave like input-referred error signals. To predict the total IMR, divide the isolation voltage by the IMR shown in IMR vs Frequency performance curve and compute the amplifier response to this input-referred error signal from the data given in the Signal Response vs Carrier Frequency performance curve. Due to effects of very high-frequency signals, typical IMV performance can be achieved only when dV/dT of the isolation mode voltage falls below 1000V/µs. For convenience, this is plotted in the typical performance curves for the ISO120 and ISO121 as a function of voltage and frequency for sinusoidal voltages. When dV/dT exceeds 1000V/µs but falls below 20kV/µs, performance may be degraded. At rates of change above 20kV/µs, the amplifier may be damaged, but the barrier retains its full integrity. Lowering the power supply voltages below ±15V may decrease the dV/dT to 500V/µs for typical performance, but the maximum dV/dT of 20kV/µs remains unchanged.

Leakage current is determined solely by the impedance of the 2pF barrier capacitance and is plotted in the Isolation Leakage Current vs Frequency curve.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one. Historically, Burr-Brown has chosen a deliberately conservative one: V_{TEST} = (2 X ACrms continuous rating) + 1000V for 10 seconds, followed by a test at rated ACrms voltage for one minute. This choice was appropriate for conditions where system transients are not well defined.

Recent improvements in high-voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology in the manufacture and testing of the ISO120 and ISO121.

Partial Discharge

When an insulation defect such as a void occurs within an insulation system, the defect will display localized corona or ionization during exposure to high-voltage stress. This ionization requires a higher applied voltage to start the discharge and lower voltage to maintain it or extinguish it once started. The higher start voltage is known as the inception voltage, while the extinction voltage is that level of voltage stress at which the discharge ceases. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached, at which point the void will ionize, effectively shorting itself out. This action redistributes electrical charge within the dielectric and is known as partial discharge. If, as is the case with AC, the applied voltage gradient across the device continues to rise, another partial discharge cycle begins. The importance of this phenomenon is that, if the discharge does not occur, the insulation system retains its integrity. If the discharge begins, and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is still useful in rating the devices and providing quality control of the manufacturing process. Since the ISO120 and ISO121 do not use organic insulation, partial discharge is non-destructive.

The inception voltage for these voids tends to be constant, so that the measurement of *total charge* being redistributed within the dielectric is a very good indicator of the size of the voids and *their likelihood of becoming an incipient failure*. The *bulk inception voltage*, on the other hand, varies with the insulation system, and the number of ionization defects and directly establishes the *absolute maximum voltage* (transient) that can be applied across the test device before destructive partial discharge can begin. Measuring the *bulk extinction voltage* provides a lower, more conservative voltage from which to derive a *safe continuous rating*. In production, measuring at a level somewhat below the expected inception voltage and then derating by a factor related to expectations about system transients is an accepted practice.

Partial Discharge Testing

Not only does this test method provide far more qualitative information about stress-withstand levels than did previous stress tests, but it provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers, such as those of high-voltage power distribution equipment, for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge, and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to quantify partial discharge. VDE, the national standards group in Germany and an acknowledged leader in high-voltage test standards, has developed a standard test method to apply this powerful technique. Use of partial discharge testing is an improved method for measuring the integrity of an isolation barrier.

To accommodate poorly-defined transients, the part under test is exposed to voltage that is 1.6 times the continuous-rated voltage and must display ≤5pC partial discharge level in a 100% production test.

APPLICATIONS

The ISO120 and ISO121 isolation amplifiers are used in three categories of applications:

1. Accurate isolation of signals from high voltage ground potentials,
2. Accurate isolation of signals from severe ground noise and,
3. Fault protection from high voltages in analog measurements.

Figures 7 through 12 show a variety of Application Circuits.

APPLICATION CIRCUITS

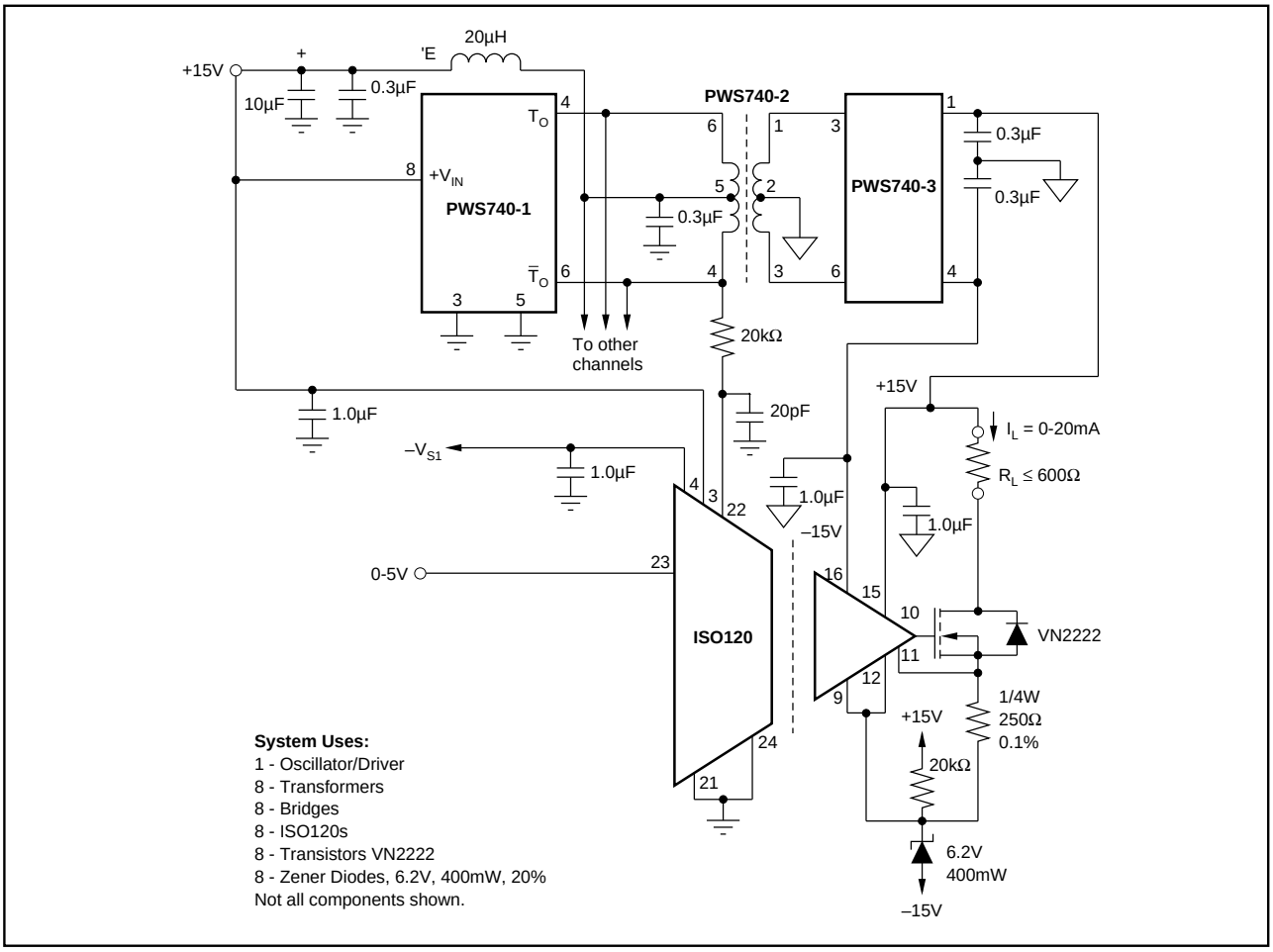


FIGURE 7. Eight-channel Isolated 0-20mA Loop Driver.

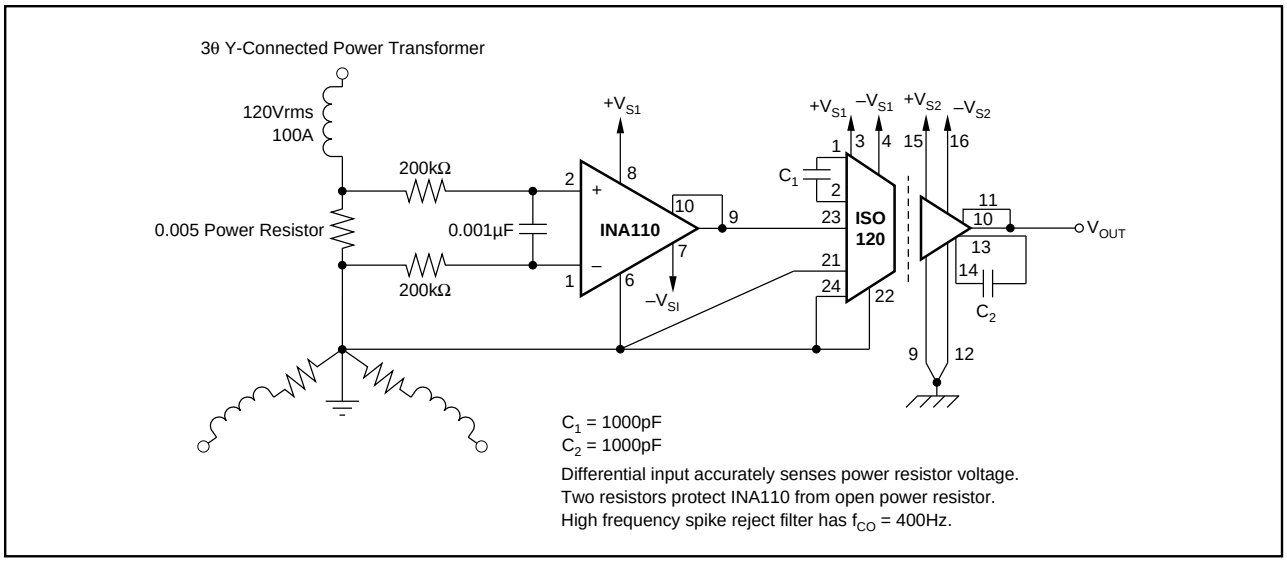


FIGURE 8. Isolated Powerline Monitor.

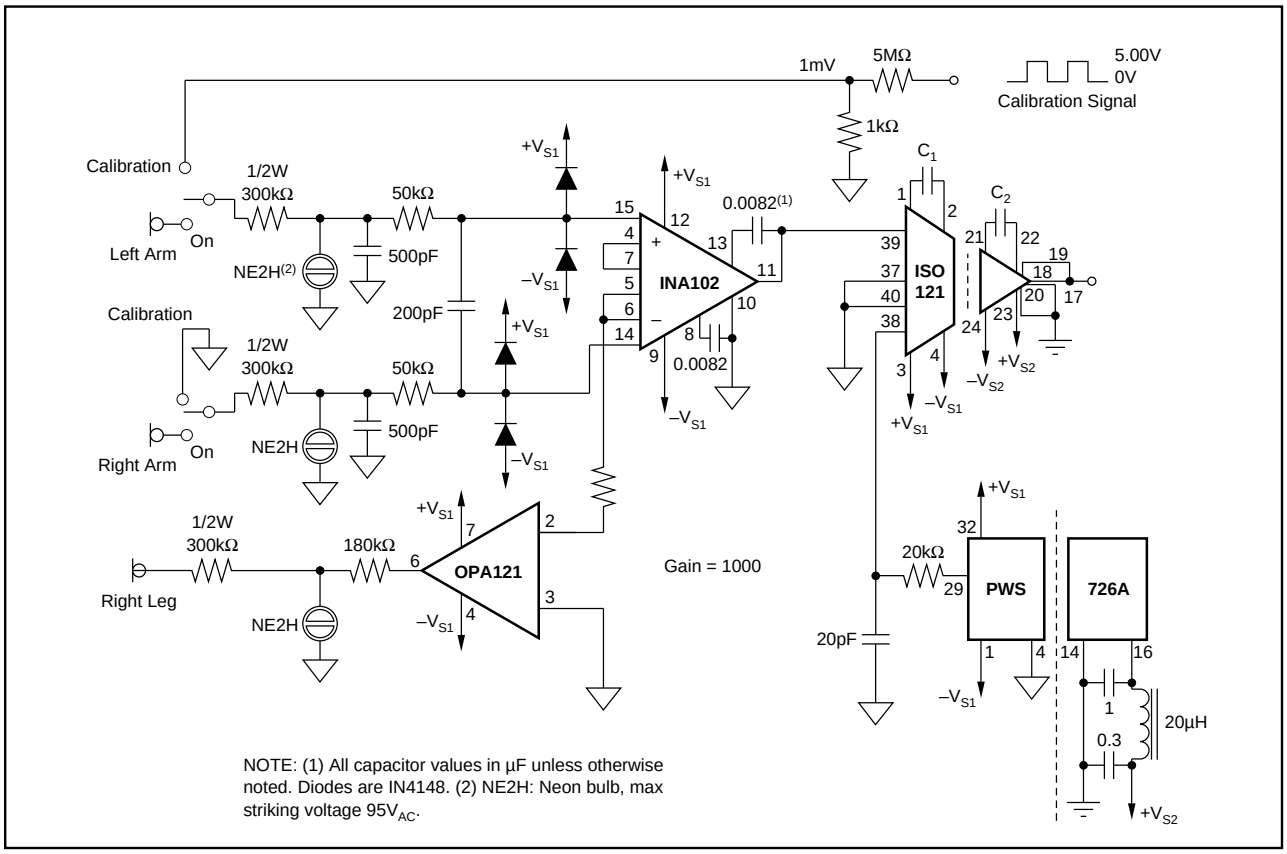


FIGURE 9. Right-Leg Driven ECG Amplifier (with defibrillator protection and calibration).

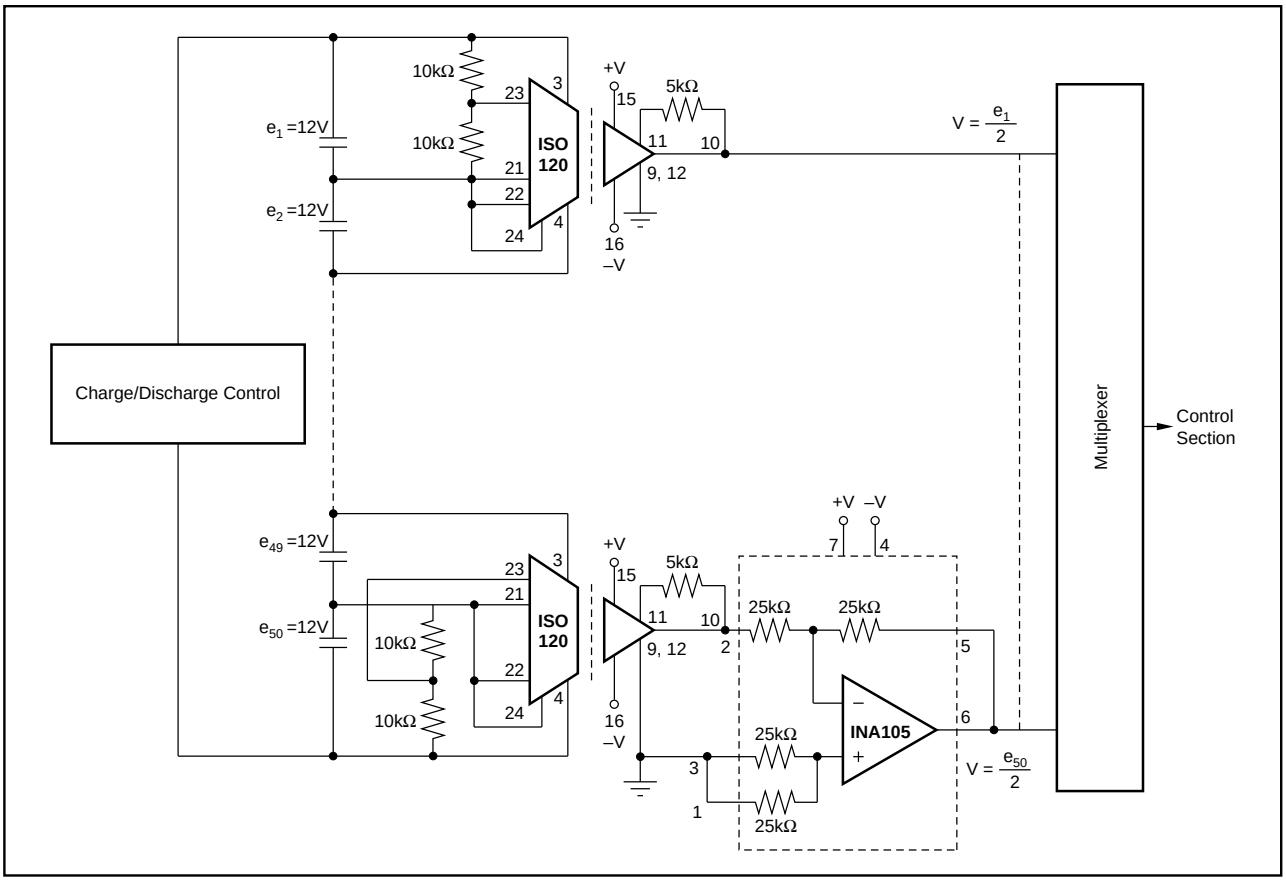


FIGURE 10. Battery Monitor for a 600V Battery Power System.

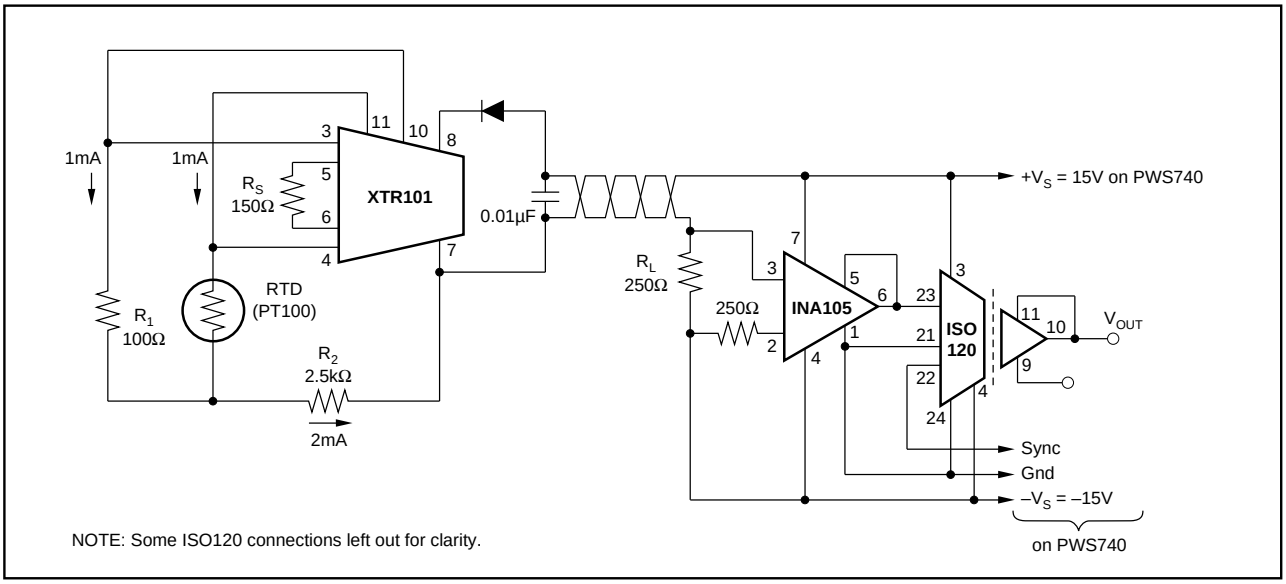


FIGURE 11. Isolated 4-20mA Instrument Loop. (RTD shown).

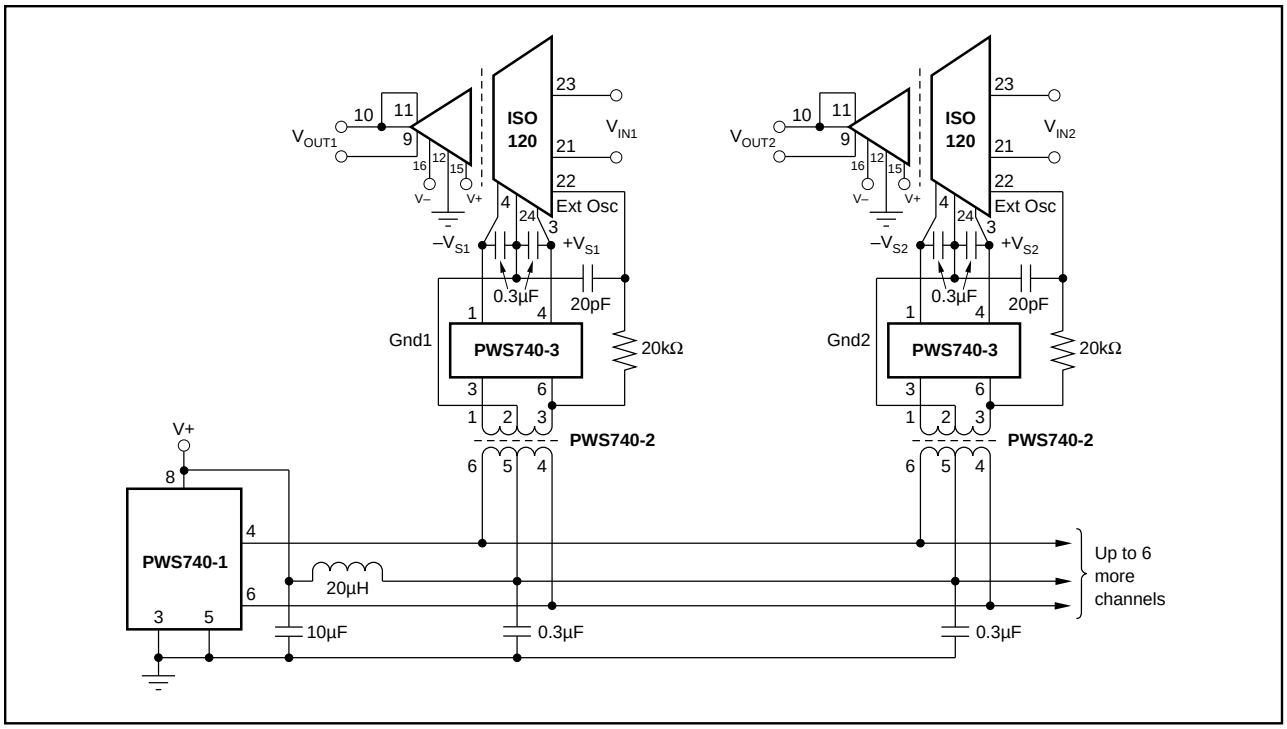


FIGURE 12. Synchronized-Multichannel Isolation System.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO120BG	NRND	Production	CDIP SB (JVA) | 16	9 | TUBE	Yes	Call TI	N/A for Pkg Type	-	ISO120BG
ISO120BG.A	NRND	Production	CDIP SB (JVA) | 16	9 | TUBE	Yes	Call TI	N/A for Pkg Type	See ISO120BG	ISO120BG
ISO120BG.B	NRND	Production	CDIP SB (JVA) | 16	9 | TUBE	Yes	Call TI	N/A for Pkg Type	See ISO120BG	ISO120BG
ISO120G	NRND	Production	CDIP SB (JVA) | 16	9 | TUBE	-	Call TI	N/A for Pkg Type	-	ISO120G
ISO120G.A	NRND	Production	CDIP SB (JVA) | 16	9 | TUBE	-	Call TI	N/A for Pkg Type	See ISO120G	ISO120G
ISO120G.B	NRND	Production	CDIP SB (JVA) | 16	9 | TUBE	-	Call TI	N/A for Pkg Type	See ISO120G	ISO120G
ISO120SG	NRND	Production	CDIP SB (JVA) | 16	9 | TUBE	Yes	AU	N/A for Pkg Type	-	ISO120SG
ISO120SG.A	NRND	Production	CDIP SB (JVA) | 16	9 | TUBE	Yes	AU	N/A for Pkg Type	See ISO120SG	ISO120SG
ISO120SG.B	NRND	Production	CDIP SB (JVA) | 16	9 | TUBE	Yes	AU	N/A for Pkg Type	See ISO120SG	ISO120SG
ISO121BG	Active	Production	CDIP SB (JVD) | 16	9 | TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 125	ISO121BG
ISO121BG.A	Active	Production	CDIP SB (JVD) | 16	9 | TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 125	ISO121BG
ISO121BG.B	Active	Production	CDIP SB (JVD) | 16	9 | TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 125	ISO121BG
ISO121G	Active	Production	CDIP SB (JVD) | 16	9 | TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 125	ISO121G
ISO121G.A	Active	Production	CDIP SB (JVD) | 16	9 | TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 125	ISO121G
ISO121G.B	Active	Production	CDIP SB (JVD) | 16	9 | TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 125	ISO121G

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

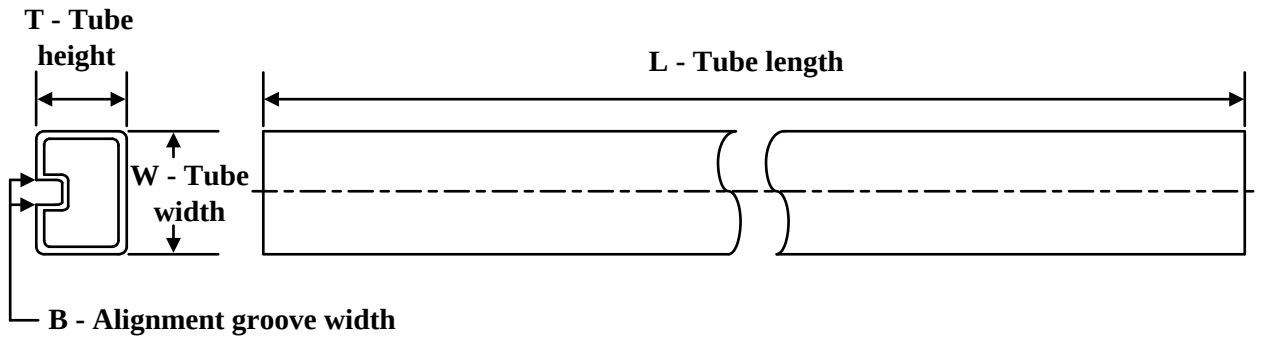
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO120BG	JVA	CDIP SB	16	9	506.98	15.24	12290	NA
ISO120BG.A	JVA	CDIP SB	16	9	506.98	15.24	12290	NA
ISO120BG.B	JVA	CDIP SB	16	9	506.98	15.24	12290	NA
ISO120G	JVA	CDIP SB	16	9	506.98	15.24	12290	NA
ISO120G.A	JVA	CDIP SB	16	9	506.98	15.24	12290	NA
ISO120G.B	JVA	CDIP SB	16	9	506.98	15.24	12290	NA
ISO120SG	JVA	CDIP SB	16	9	506.98	15.24	12290	NA
ISO120SG.A	JVA	CDIP SB	16	9	506.98	15.24	12290	NA
ISO120SG.B	JVA	CDIP SB	16	9	506.98	15.24	12290	NA
ISO121BG	JVD	CDIP SB	16	9	508	22.05	13080	NA
ISO121BG.A	JVD	CDIP SB	16	9	508	22.05	13080	NA
ISO121BG.B	JVD	CDIP SB	16	9	508	22.05	13080	NA
ISO121G	JVD	CDIP SB	16	9	508	22.05	13080	NA
ISO121G.A	JVD	CDIP SB	16	9	508	22.05	13080	NA
ISO121G.B	JVD	CDIP SB	16	9	508	22.05	13080	NA

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