

INA828 50 μ Vオフセット、7nV/ $\sqrt{\text{Hz}}$ ノイズ、低消費電力、高精度計測アンプ

1 特長

- 高精度計測アンプの発展
 - 第2世代: INA828
 - 第1世代: INA128
- 低いオフセット電圧: 最大50 μ V
- ゲイン・ドリフト係数: 5ppm/ $^{\circ}\text{C}$ ($G = 1$)、50ppm/ $^{\circ}\text{C}$ ($G > 1$)
- ノイズ: 7nV/ $\sqrt{\text{Hz}}$
- 帯域幅: 2MHz ($G = 1$)、260kHz ($G = 100$)
- 1nFの容量性負荷で安定
- $\pm 40\text{V}$ まで入力を保護
- 同相信号除去:
 - 110dB (最小値、 $G = 10$)
- 電源電圧除去: 100dB (最小値、 $G = 1$)
- 消費電流: 650 μA (最大値)
- 電源電圧範囲:
 - 単一電源: 4.5V $\sim$ 36V
 - デュアル電源: $\pm 2.25\text{V} \sim \pm 18\text{V}$
- 定格温度範囲:
 - $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$
- パッケージ: 8ピンSOIC

2 アプリケーション

- 産業用プロセス制御
- サーキット・ブレーカ
- バッテリー・テスタ
- ECGアンプ
- パワー・オートメーション
- 医療用計測機器
- ポータブル機器

3 概要

INA828は、単一電源またはデュアル電源の非常に幅広い電圧範囲で動作する、低消費電力の高精度計測アンプです。単一の外付け抵抗によって、1 $\sim$ 1000の範囲でゲインを設定できます。このデバイスは、入力オフセット電圧、オフセット電圧ドリフト、入力バイアス電流、入力電圧ノイズ、入力電流ノイズを極めて低く抑える新しいスーパー β 入力トランジスタを使用することで、卓越した精度を実現します。追加回路により、 $\pm 40\text{V}$ までの過電圧から入力を保護します。

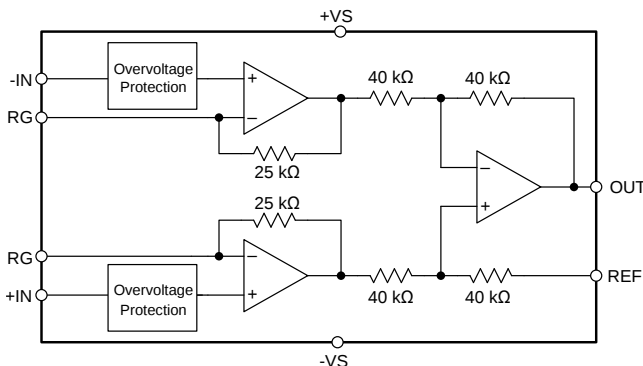
INA828は非常に高い同相除去比を提供するように最適化されています。 $G = 1$ での同相除去比は、全入力同相範囲を通じて90dBを上回ります。このデバイスは、5Vの単一電源から最大 $\pm 18\text{V}$ のデュアル電源までの低電圧動作に適しています。INA828は、8ピンSOICパッケージで供給され、 $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$ の温度範囲で動作が規定されています。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
INA828	SOIC (8)	4.90mm $\times$ 3.91mm

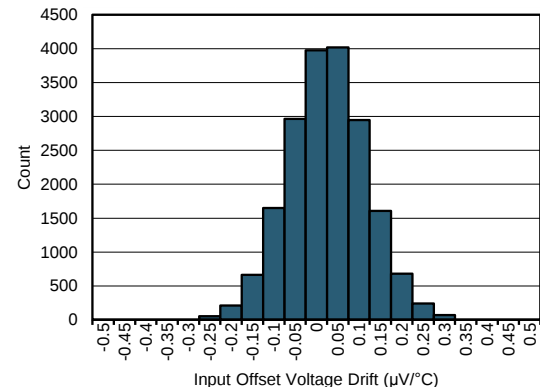
(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

INA828の簡略化された内部回路図



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入力オフセット電圧ドリフトの代表的な分布



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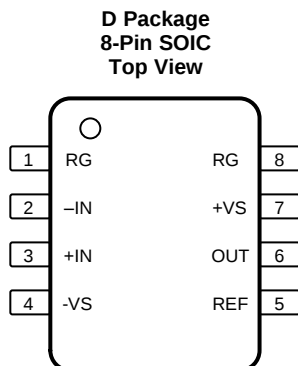
4 改訂履歴

2017年8月発行のものから更新

Page

•	Changed MAX value for G = 1 in "GE" row from "±0.020%" to "±0.025%"	5
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5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
RG	1	—	Gain setting pin. Place a gain resistor between pin 1 and pin 8.
	8		
-IN	2	I	Negative (inverting) input
+IN	3	I	Positive (noninverting) input
-VS	4	—	Negative supply
REF	5	I	Reference input. This pin must be driven by a low impedance source.
OUT	6	O	Output
+VS	7	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage		–18	18	V
Signal input pins	Voltage	–40	40	V
	REF pin	–18	18	
Output short-circuit ⁽²⁾		Continuous		
Temperature	Operating, T _A	–50	150	°C
	Junction, T _J		175	
	Storage, T _{stg}	–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to V_S / 2.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	Single supply	4.5	36	V
	Dual supply	±2.25	±18	
Specified temperature		–40	125	°C
Operating temperature		–50	150	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		INA828	UNIT
		D (SOIC)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	119.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	66.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	61.9	°C/W
ψ _{JT}	Junction-to-top characterization parameter	20.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	61.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 1$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V _{OSI}	Input stage offset voltage ⁽¹⁾⁽²⁾	G = 100, RTI		20	50	μV
		T _A = –40°C to +125°C ⁽³⁾			90	μV
		vs temperature, T _A = –40°C to +125°C			0.5	μV/°C
V _{OSO}	Output stage offset voltage ⁽¹⁾⁽²⁾	G = 1, RTI		50	250	μV
		T _A = –40°C to +125°C ⁽³⁾			500	μV
		vs temperature, T _A = –40°C to +125°C			5	μV/°C
PSRR	Power-supply rejection ratio	G = 1, RTI	110	120		dB
		G = 10, RTI	114	130		
		G = 100, RTI	130	135		
		G = 1000, RTI	136	140		
Z _{id}	Differential impedance			100 1		GΩ pF
Z _{ic}	Common-mode impedance			100 10		GΩ pF
	RFI filter, –3-dB frequency			53		MHz
V _{CM}	Operating input range ⁽⁴⁾		(V–) + 2	(V+) – 2		V
		V _S = ±2.25 V to ±18 V, T _A = –40°C to +125°C	See Figure 48 to Figure 51			
	Input overvoltage range	T _A = –40°C to +125°C			±40	V
CMRR	Common-mode rejection ratio	At dc to 60 Hz, RTI, V _{CM} = (V–) + 2 V to (V+) – 2 V, G = 1	90	100		dB
		At dc to 60 Hz, RTI, V _{CM} = (V–) + 2 V to (V+) – 2 V, G = 10	110	120		
		At dc to 60 Hz, RTI, V _{CM} = (V–) + 2 V to (V+) – 2 V, G = 100	130	140		
		At dc to 60 Hz, RTI, V _{CM} = (V–) + 2 V to (V+) – 2 V, G = 1000	140	145		
BIAS CURRENT						
I _B	Input bias current	V _{CM} = V _S / 2		0.15	0.6	nA
		T _A = –40°C to +125°C			2	
I _{OS}	Input offset current	V _{CM} = V _S / 2		0.15	0.6	nA
		T _A = –40°C to +125°C			2	
NOISE VOLTAGE						
e _{NI}	Input stage voltage noise ⁽⁵⁾	f = 1 kHz, G = 100, R _S = 0 Ω		7		nV/√Hz
		f _B = 0.1 Hz to 10 Hz, G = 100, R _S = 0 Ω		0.14		μV _{PP}
e _{NO}	Output stage voltage noise ⁽⁵⁾	f = 1 kHz, R _S = 0 Ω		90		nV/√Hz
		f _B = 0.1 Hz to 10 Hz, R _S = 0 Ω		7.7		μV _{PP}
I _n	Noise current	f = 1 kHz		170		fA/√Hz
		f _B = 0.1 Hz to 10 Hz, G = 100		4.7		pA _{PP}
GAIN						
G	Gain equation		1 + (50 kΩ / R _G)			V/V
	Range of gain		1		1000	V/V
GE	Gain error	G = 1, V _O = ±10 V		±0.005%	±0.025%	
		G = 10, V _O = ±10 V		±0.025%	±0.15%	
		G = 100, V _O = ±10 V		±0.025%	±0.15%	
		G = 1000, V _O = ±10 V		±0.05%		
	Gain vs temperature ⁽⁶⁾	G = 1, T _A = –40°C to +125°C			±5	ppm/°C
		G > 1, T _A = –40°C to +125°C			±50	

(1) Total offset, referred-to-input (RTI): $V_{\text{OS}} = (V_{\text{OSI}}) + (V_{\text{OSO}} / G)$.

(2) Offset drifts are uncorrelated. Input-referred offset drift is calculated using: $\Delta V_{\text{OS(RTI)}} = \sqrt{[\Delta V_{\text{OSI}}]^2 + (\Delta V_{\text{OSO}} / G)^2}$

(3) Specified by characterization.

(4) Input voltage range of the INA828 input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See *Typical Characteristic* curves [48](#) through [51](#) for more information.

(5) Total RTI voltage noise is equal to: $e_{\text{N(RTI)}} = \sqrt{[e_{\text{NI}}]^2 + (e_{\text{NO}} / G)^2}$

(6) The values specified for $G > 1$ do not include the effects of the external gain-setting resistor, R_G .

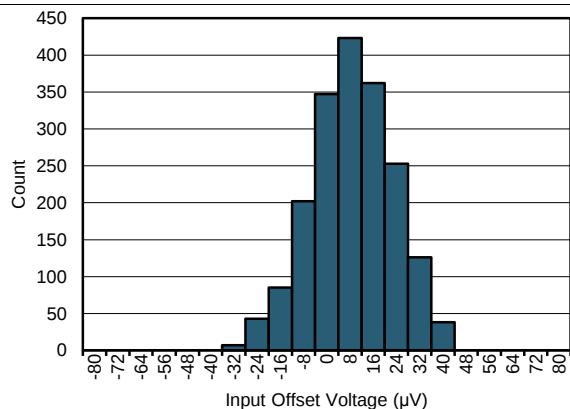
Electrical Characteristics (continued)

 at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 1$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain nonlinearity		G = 1 to 10, V _O = −10 V to +10 V, R _L = 10 kΩ		1	10	ppm
		G = 100, V _O = −10 V to +10 V, R _L = 10 kΩ			15	
		G = 1000, V _O = −10 V to +10 V, R _L = 10 kΩ			20	
		G = 1 to 100, V _O = −10 V to +10 V, R _L = 2 kΩ		30		
OUTPUT						
	Voltage swing		(V−) + 0.15		(V+) − 0.15	V
	Load capacitance stability			1000		pF
Z _O	Closed-loop output impedance	f = 10 kHz		1.3		Ω
I _{SC}	Short-circuit current	Continuous to V _S / 2		±18		mA
FREQUENCY RESPONSE						
BW	Bandwidth, −3 dB	G = 1		2.0		MHz
		G = 10		640		kHz
		G = 100		260		
		G = 1000		33		
SR	Slew rate	G = 1, V _O = ±10 V		1.2		V/μs
t _S	Settling time	0.01%, G = 1 to 100, V _{STEP} = 10 V		12		μs
		0.01%, G = 1000, V _{STEP} = 10 V		40		
		0.001%, G = 1 to 100, V _{STEP} = 10 V		16		
		0.001%, G = 1000, V _{STEP} = 10 V		50		
REFERENCE INPUT						
R _{IN}	Input impedance			40		kΩ
	Voltage range		(V−)		(V+)	V
	Gain to output			1		V/V
	Reference gain error			0.01%		
POWER SUPPLY						
V _S	Power-supply voltage	Single supply	4.5		36	V
		Dual supply	±2.25		±18	
I _Q	Quiescent current	V _{IN} = 0 V		600	650	μA
		vs temperature, T _A = −40°C to +125°C			850	

6.6 Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 1$ (unless otherwise noted)

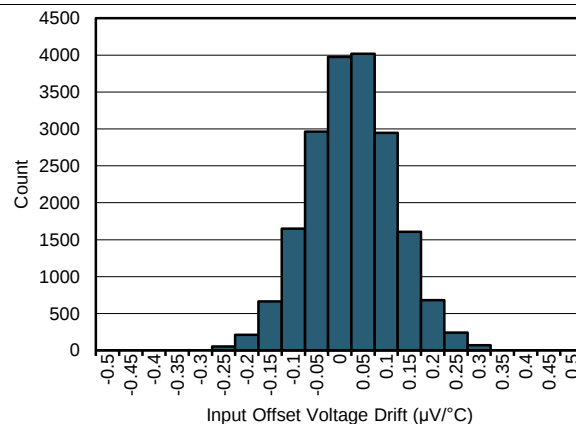


N = 1886

Std. Dev. = 13.98 µV

Mean = 4.73 µV

FIG 1. Typical Distribution of Input Offset Voltage

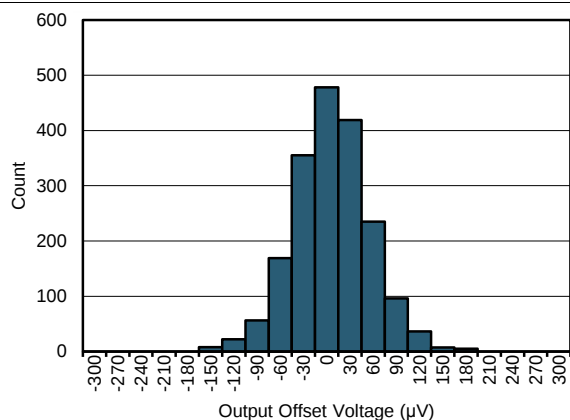


N = 19081

Std. Dev. = 0.09 µV/°C

Mean = 0.16 nV/°C

FIG 2. Typical Distribution of Input Offset Voltage Drift

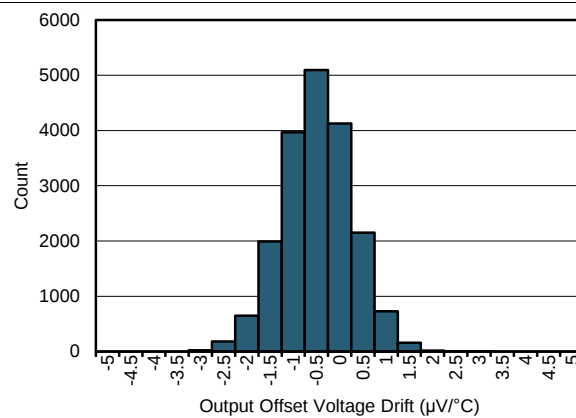


N = 1886

Std. Dev. = 48.57 µV

Mean = -8.71 µV

FIG 3. Typical Distribution of Output Offset Voltage

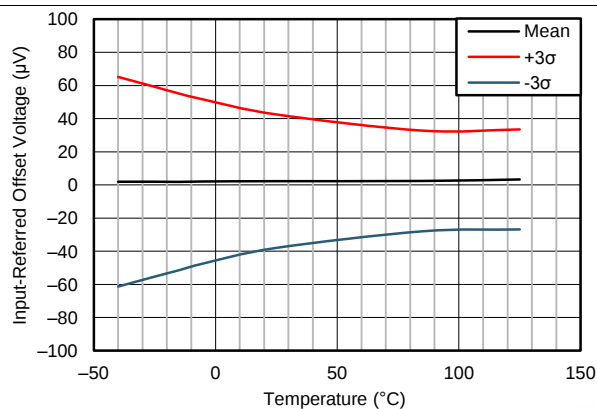


N = 19081

Std. Dev. = 0.74 µV/°C

Mean = -0.73 µV/°C

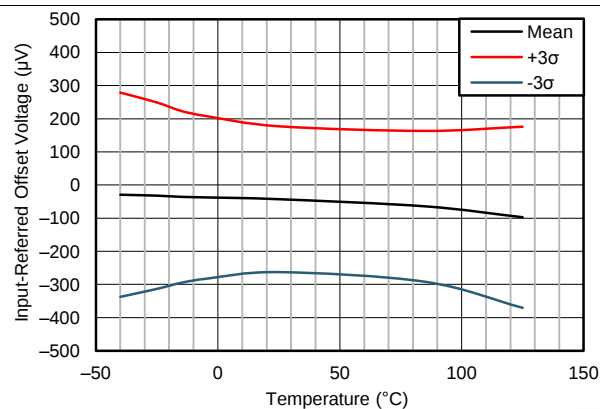
FIG 4. Typical Distribution of Output Offset Voltage Drift



G = 100

88 units, 3 wafer lots

FIG 5. Input-Referred Offset Voltage vs Temperature



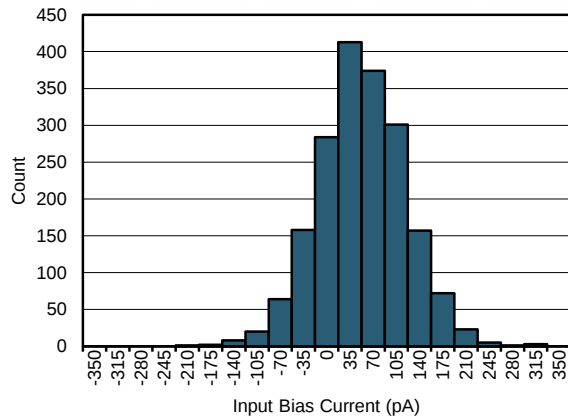
G = 1

88 units, 3 wafer lots

FIG 6. Input-Referred Offset Voltage vs Temperature

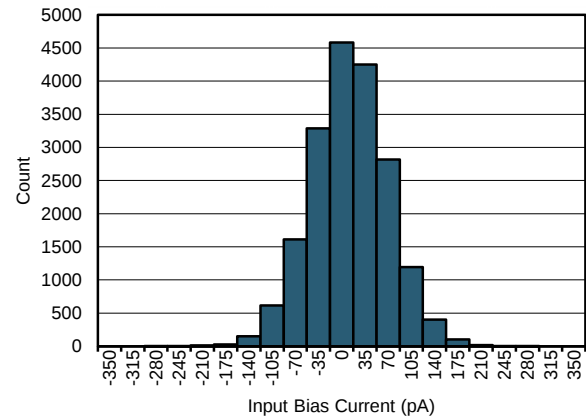
Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 1$ (unless otherwise noted)



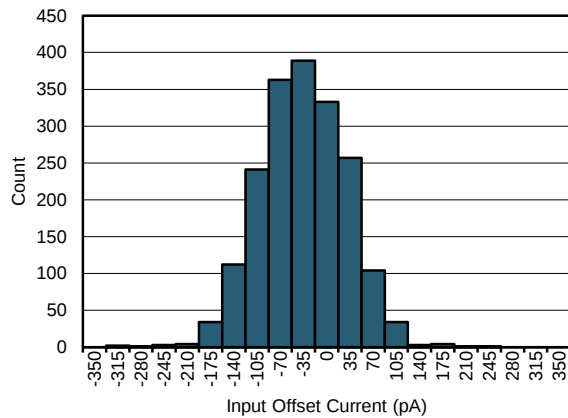
N = 1886
Std. Dev. = 65.31 pA
Mean = 36.25 pA

FIG 7. Typical Distribution of Input Bias Current (25°C)



N = 19081
Std. Dev. = 57.46 pA
Mean = -5.32 pA

FIG 8. Typical Distribution of Input Bias Current (90°C)



N = 1886
Std. Dev. = 63.86 pA
Mean = -52.64 pA

FIG 9. Typical Distribution of Input Offset Current

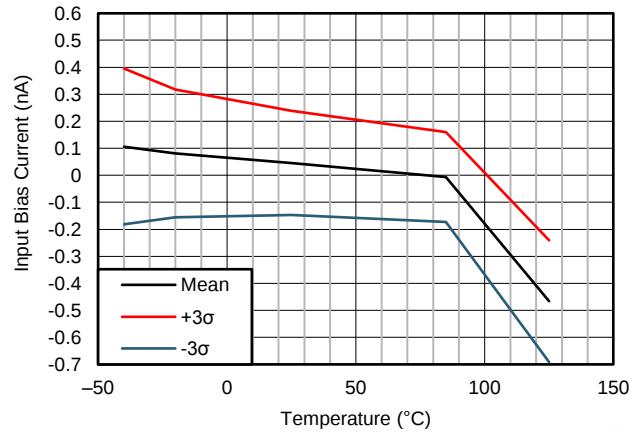


FIG 10. Input Bias Current vs Temperature

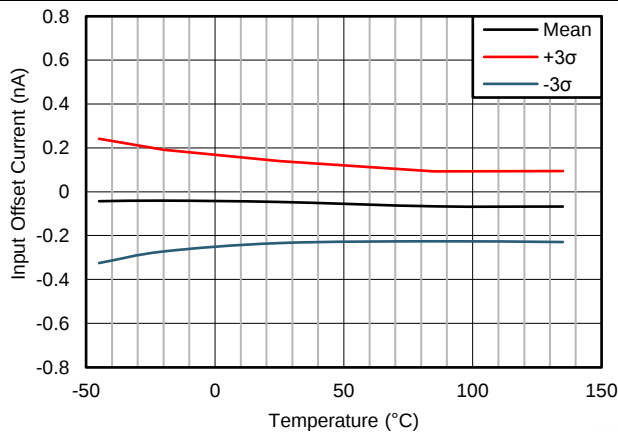
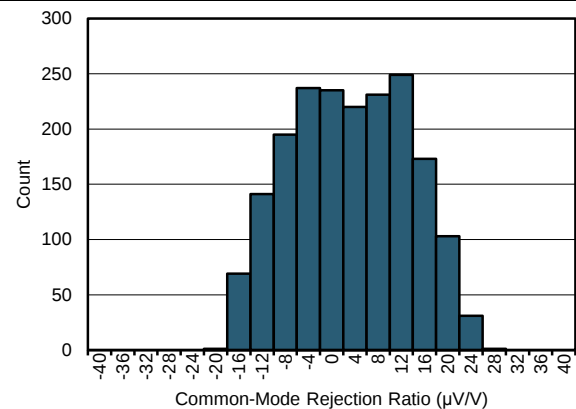


FIG 11. Input Offset Current vs Temperature

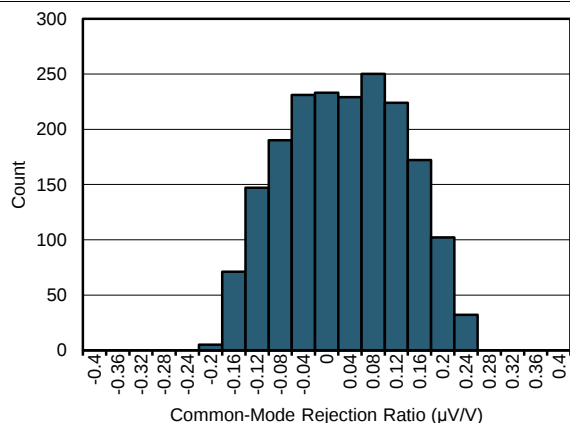


N = 1886
Std. Dev. = 10.04 $\mu\text{V/V}$
Mean = 1.18 $\mu\text{V/V}$

FIG 12. Typical CMRR Distribution (G = 1)

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 1$ (unless otherwise noted)



$N = 1886$

Mean = $0.01\text{ }\mu\text{V/V}$

Std. Dev. = $0.1\text{ }\mu\text{V/V}$

FIG 13. Typical CMRR Distribution ($G = 100$)

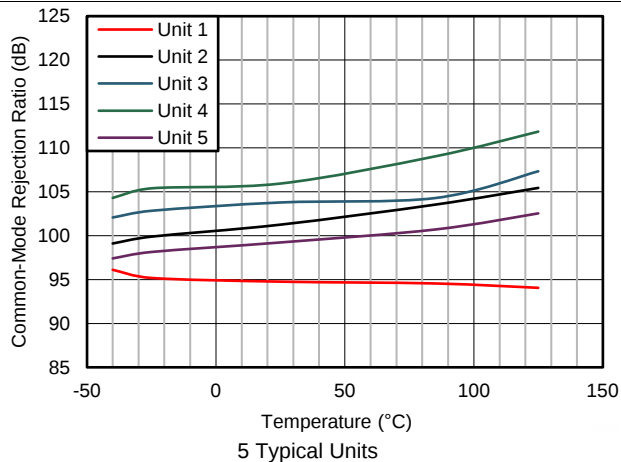


FIG 14. CMRR vs Temperature ($G = 1$)

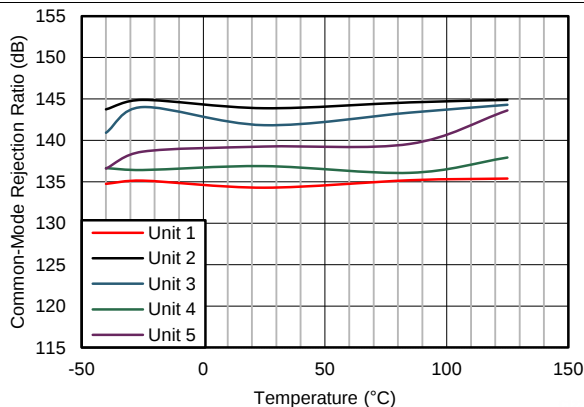


FIG 15. CMRR vs Temperature ($G = 100$)

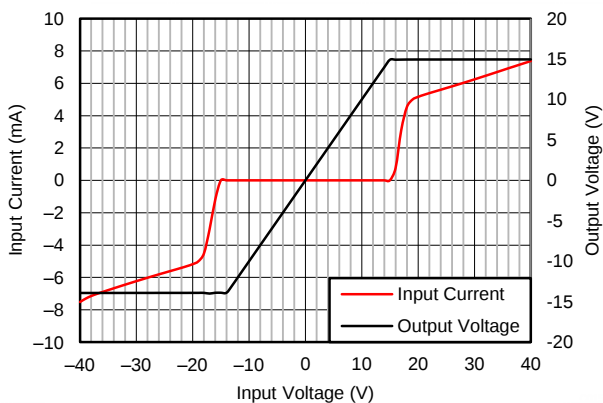


FIG 16. Input Current vs Input Overvoltage

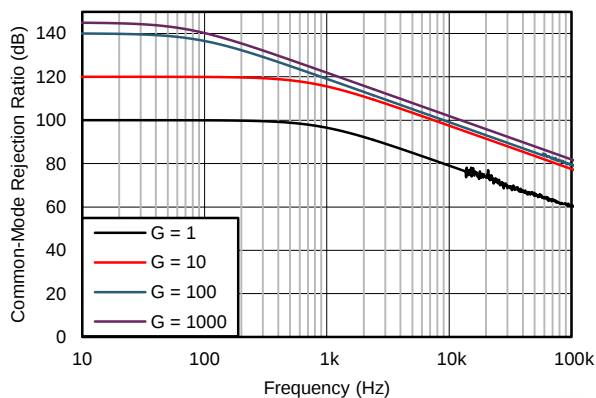


FIG 17. CMRR vs Frequency (RTI)

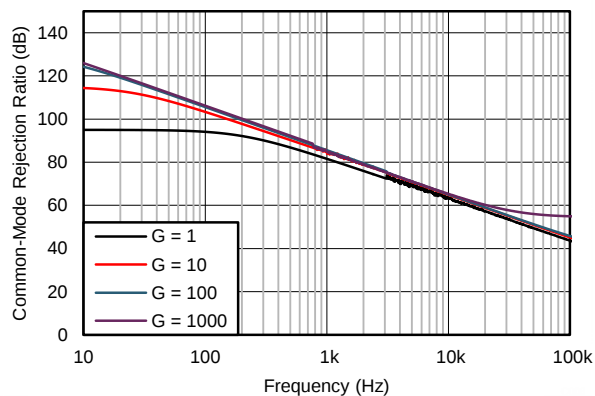


FIG 18. CMRR vs Frequency (RTI, 1-k Ω Source Imbalance)

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 1$ (unless otherwise noted)

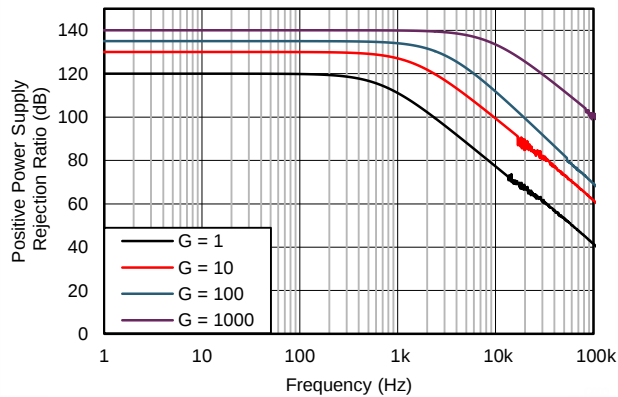


图 19. Positive PSRR vs Frequency (RTI)

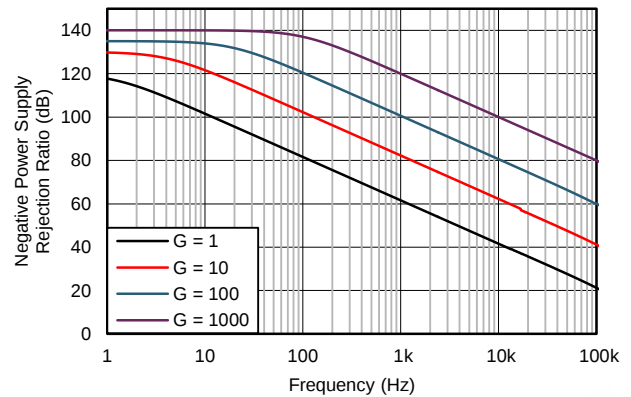


图 20. Negative PSRR vs Frequency (RTI)

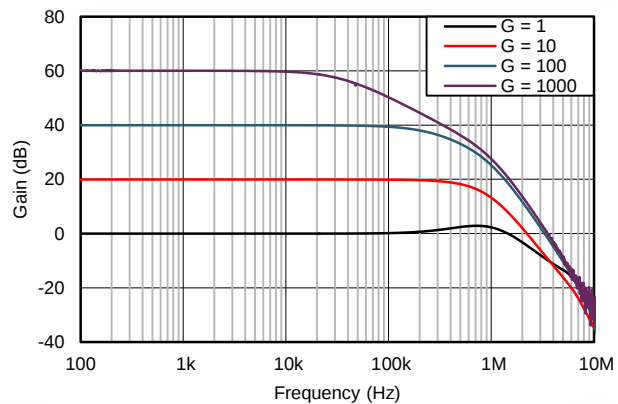


图 21. Gain vs Frequency

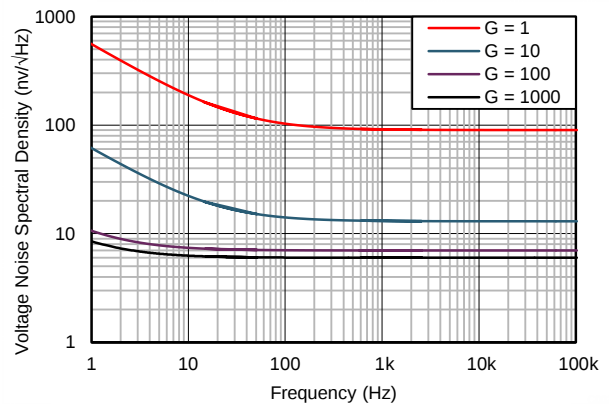


图 22. Voltage Noise Spectral Density vs Frequency (RTI)

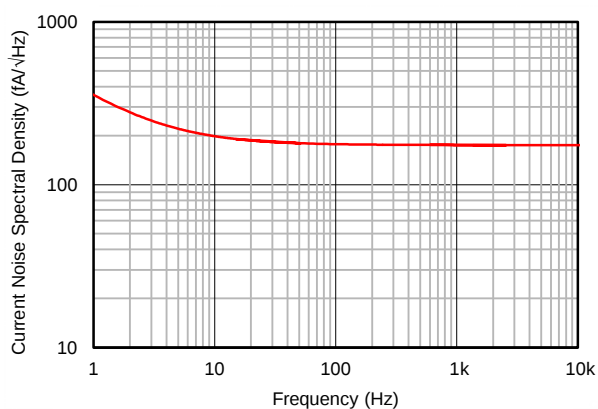


图 23. Current Noise Spectral Density vs Frequency (RTI)

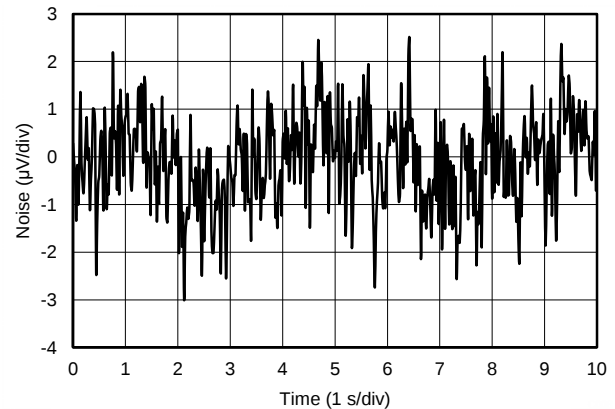


图 24. 0.1-Hz to 10-Hz RTI Voltage Noise ($G = 1$)

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 1$ (unless otherwise noted)

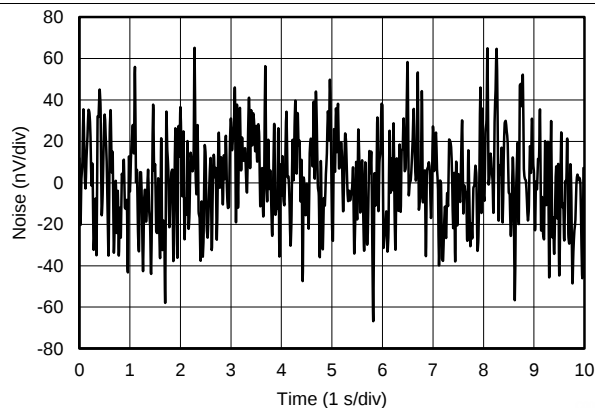


FIG 25. 0.1-Hz to 10-Hz RTI Voltage Noise ($G = 1000$)

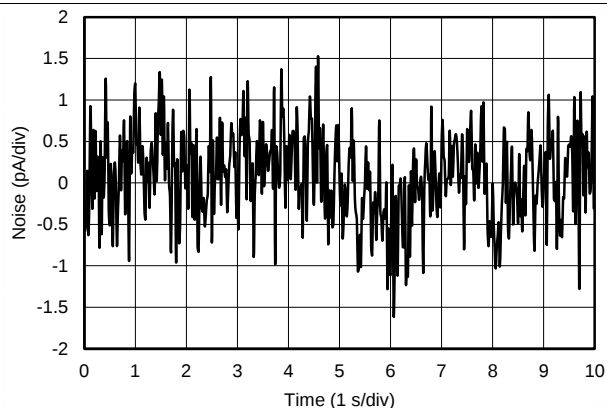


FIG 26. 0.1-Hz to 10-Hz RTI Current Noise

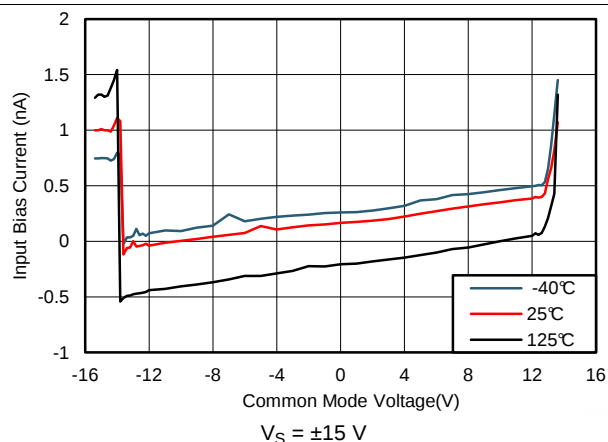


FIG 27. Input Bias Current vs Common-Mode Voltage

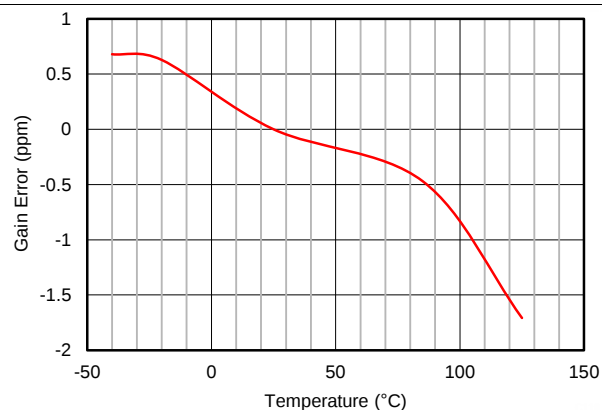


FIG 28. Gain Error vs Temperature ($G = 1$)

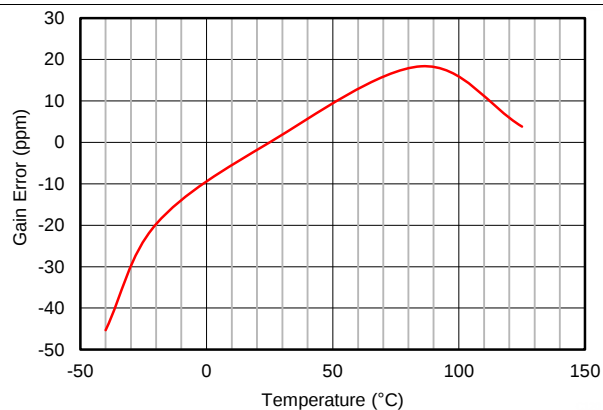


FIG 29. Gain Error vs Temperature ($G = 100$)

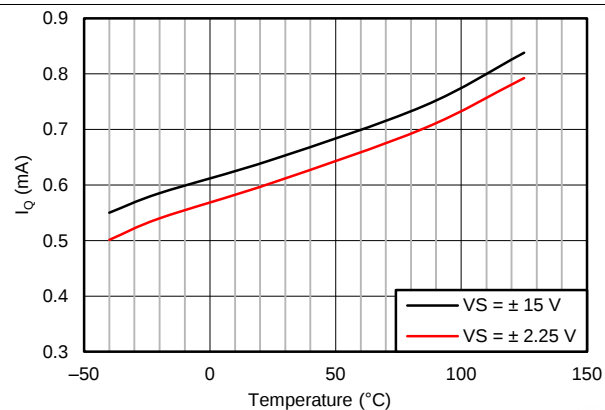


FIG 30. Supply Current vs Temperature

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 1$ (unless otherwise noted)

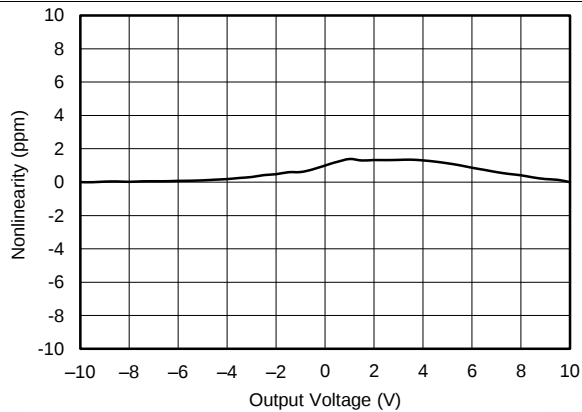


图 31. Gain Nonlinearity ($G = 1$)

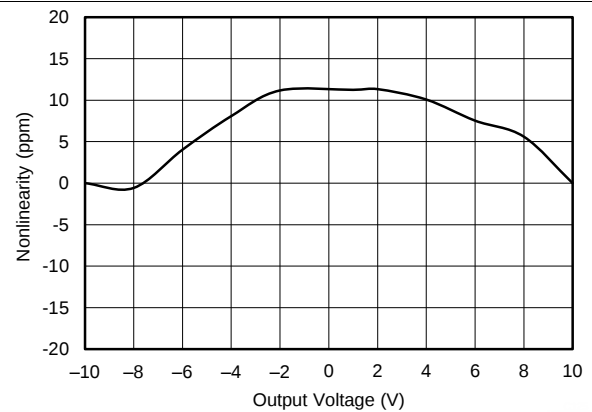


图 32. Gain Nonlinearity ($G = 100$)

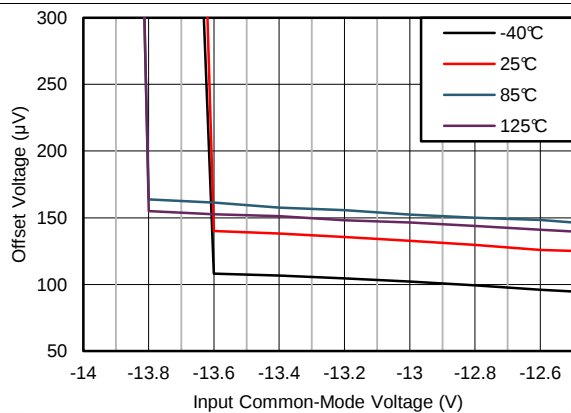


图 33. Offset Voltage vs Negative Common-Mode Voltage

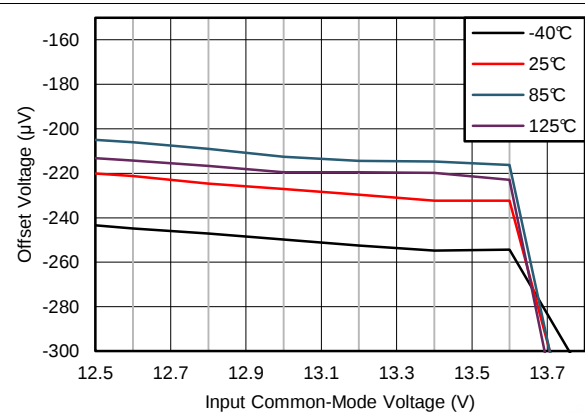


图 34. Offset Voltage vs Positive Common-Mode Voltage

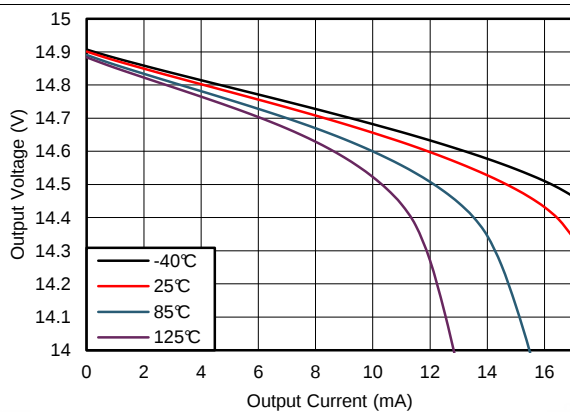


图 35. Positive Output Voltage Swing vs Output Current

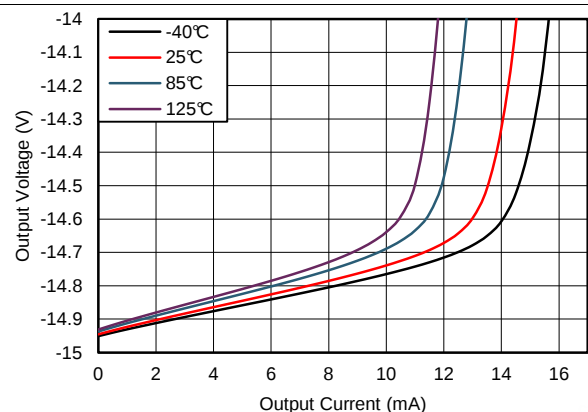


图 36. Negative Output Voltage Swing vs Output Current

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 1$ (unless otherwise noted)

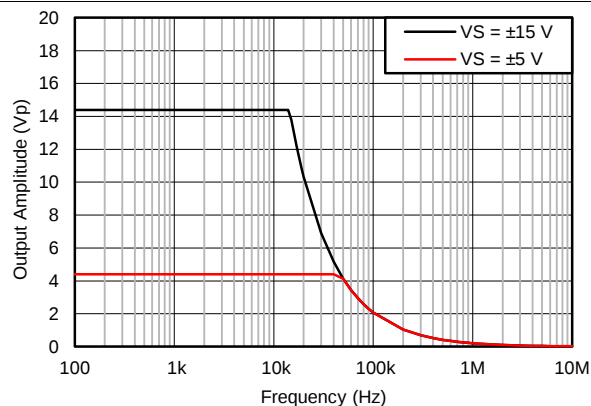
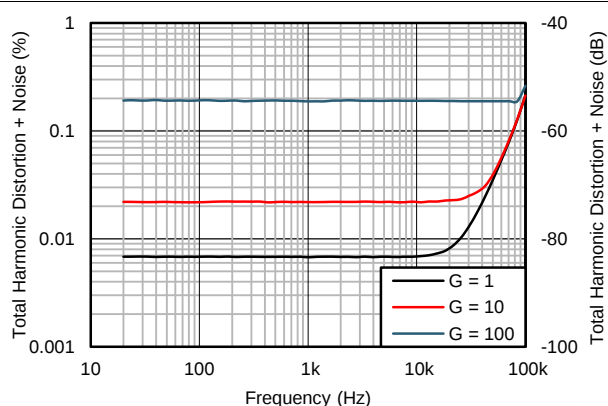


Figure 37. Large-Signal Frequency Response



500-kHz Measurement bandwidth
1- V_{RMS} Output voltage
100-k Ω Load

Figure 38. THD+N vs Frequency

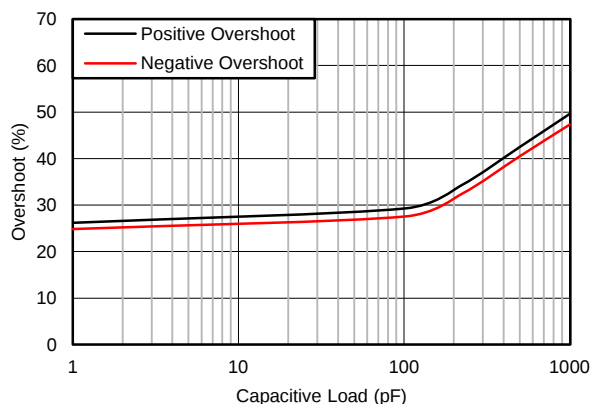
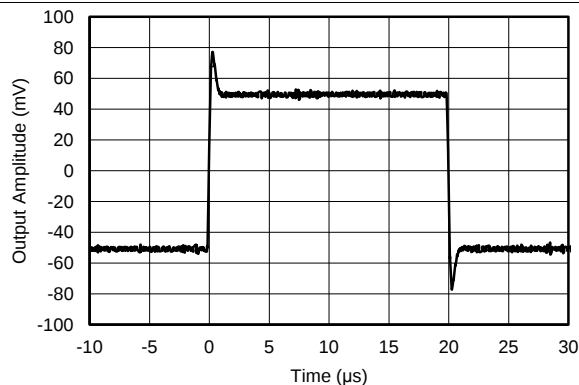
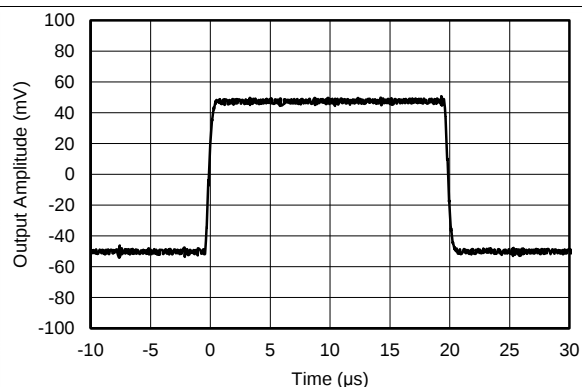


Figure 39. Overshoot vs Capacitive Loads



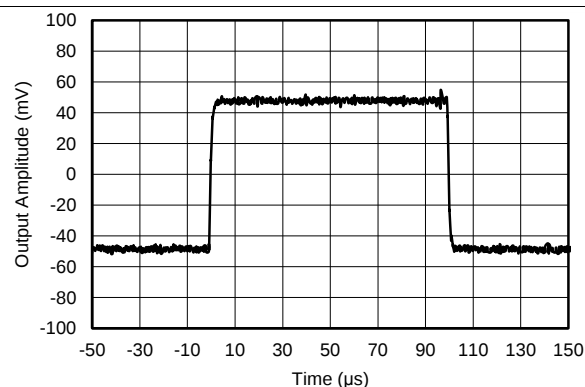
$G = 1$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$

Figure 40. Small-Signal Response



$G = 10$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$

Figure 41. Small-Signal Response

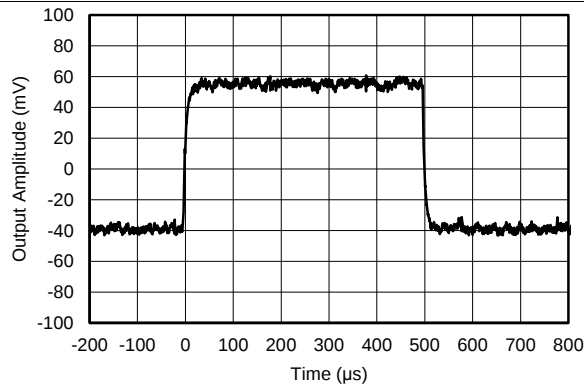


$G = 100$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$

Figure 42. Small-Signal Response

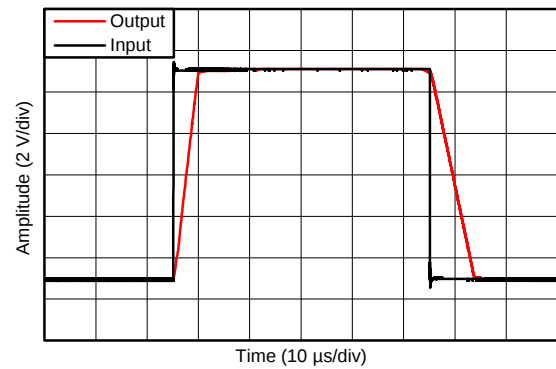
Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 1$ (unless otherwise noted)

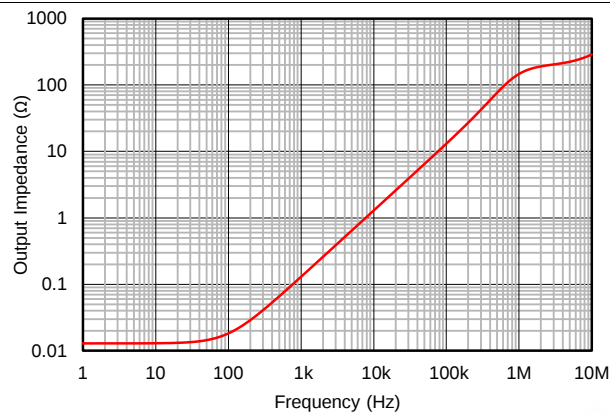


$G = 1000$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$

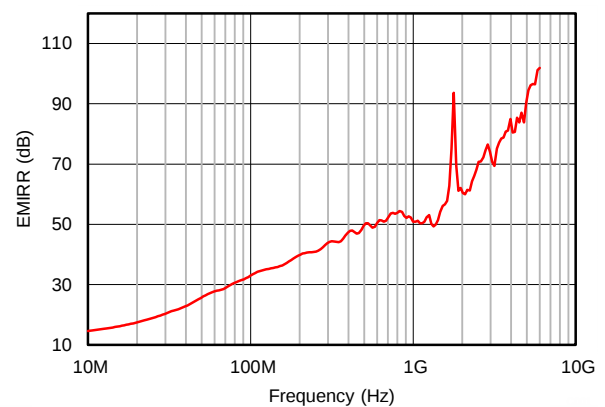
✎ 43. Small-Signal Response



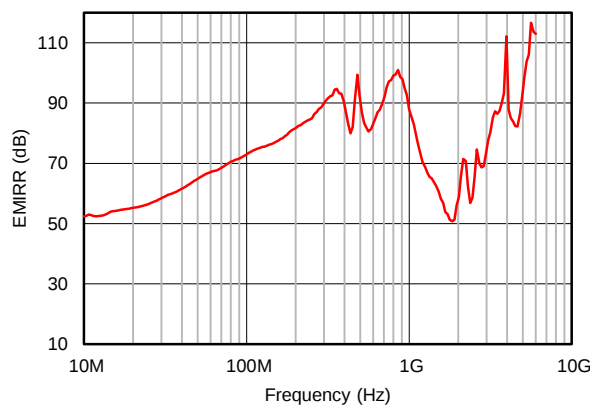
✎ 44. Large Signal Step Response



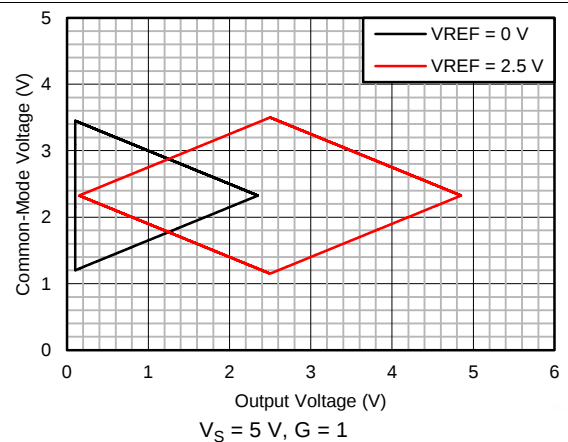
✎ 45. Closed-Loop Output Impedance



✎ 46. Differential-Mode EMI Rejection Ratio



✎ 47. Common-Mode EMI Rejection Ratio



✎ 48. Input Common-Mode Voltage vs Output Voltage
 $V_S = 5\text{ V}$, $G = 1$

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{REF} = 0\text{ V}$, and $G = 1$ (unless otherwise noted)

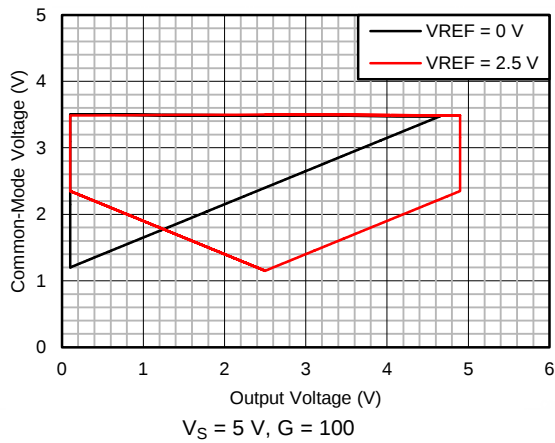


图 49. Input Common-Mode Voltage vs Output Voltage

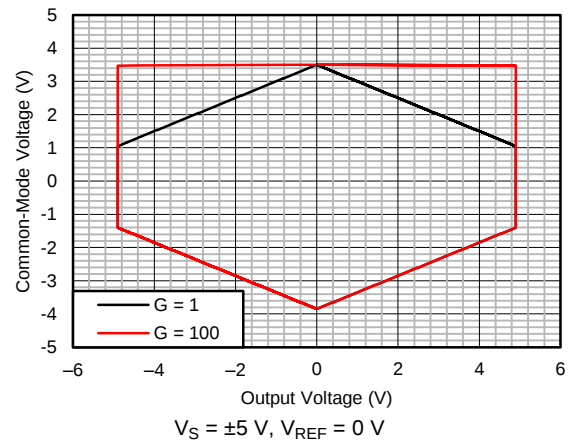


图 50. Input Common-Mode Voltage vs Output Voltage

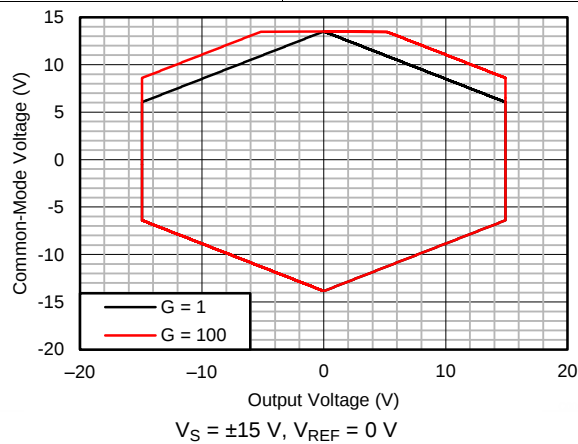


图 51. Input Common-Mode Voltage vs Output Voltage

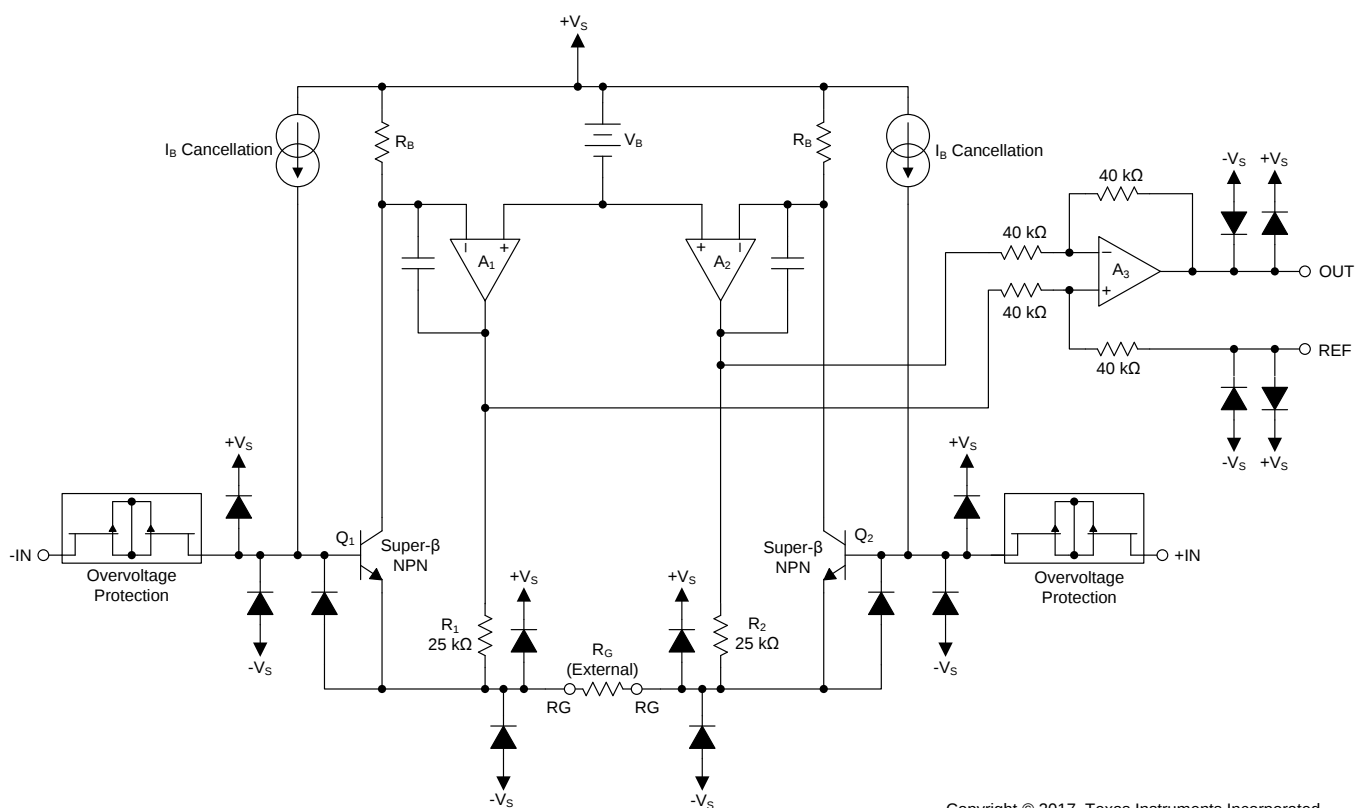
7 Detailed Description

7.1 Overview

The INA828 is a monolithic precision instrumentation amplifier incorporating a current-feedback input stage and a 4-resistor difference amplifier output stage. The differential input voltage is buffered by Q_1 and Q_2 and is forced across R_G , which causes a signal current to flow through R_G , R_1 , and R_2 . The output difference amplifier, A_3 , removes the common-mode component of the input signal and refers the output signal to the REF terminal. The V_{BE} and voltage drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 0.8 V lower than the input voltages.

Each input is protected by two field-effect transistors (FETs) that provide a low series resistance under normal signal conditions, and preserve excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 8 mA.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Setting the Gain

Figure 52 shows that the gain of the INA828 is set by a single external resistor, R_G , connected between the RG pins (pins 1 and 8).

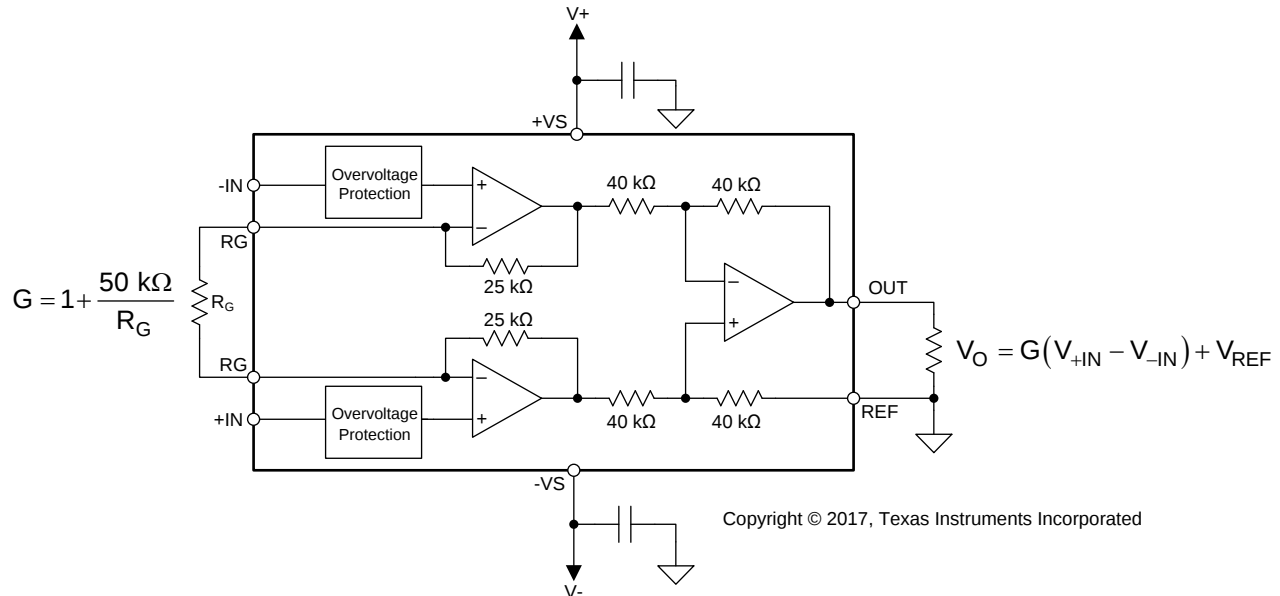


Figure 52. Simplified Diagram of the INA828 With Gain and Output Equations

The value of R_G is selected according to:

$$G = 1 + \frac{50 \text{ k}\Omega}{R_G} \quad (1)$$

Table 1 lists several commonly-used gains and resistor values. The 50-kΩ term in Equation 1 comes from the sum of the two internal 25-kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA828.

Table 1. Commonly-Used Gains and Resistor Values

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	50 k	49.9 k
5	12.5 k	12.4 k
10	5.556 k	5.49 k
20	2.632 k	2.61 k
50	1.02 k	1.02 k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9

7.3.1.1 Gain Drift

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. The contribution of R_G to gain accuracy and drift can be determined from 式 1.

The best gain drift of 5 ppm/°C (maximum) can be achieved when the INA828 uses $G = 1$ without R_G connected. In this case, gain drift is limited only by the slight mismatch of the temperature coefficient of the integrated 40-kΩ resistors in the differential amplifier (A_3). At gains greater than 1, gain drift increases as a result of the individual drift of the 25-kΩ resistors in the feedback of A_1 and A_2 , relative to the drift of the external gain resistor R_G . The low temperature coefficient of the internal feedback resistors significantly improves the overall temperature stability of applications using gains greater than 1 V/V over alternate solutions.

Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 100 or greater. To assure stability, avoid parasitic capacitance of more than a few picofarads at R_G connections. Careful matching of any parasitics on both R_G pins maintains optimal CMRR over frequency; see *Typical Characteristics*, 图 17.

7.3.2 EMI Rejection

Texas Instruments developed a method to accurately measure the immunity of an amplifier over a broad frequency spectrum, extending from 10 MHz to 6 GHz. This method uses an EMI rejection ratio (EMIRR) to quantify the ability of the INA828 to reject EMI. The offset resulting from an input EMI signal can be calculated using 式 2:

$$\Delta V_{OS} = \left(\frac{V_{RF_PEAK}^2}{100 \text{ mV}_P} \right) \cdot 10^{\left(\frac{EMIRR \text{ (dB)}}{20} \right)}$$

where

- V_{RF_PEAK} is the peak amplitude of the input EMI signal. (2)

图 53 and 图 54 show the INA828 EMIRR graph for both differential and common-mode EMI rejection across this frequency range. 表 2 shows the EMIRR values for the INA828 at frequencies commonly encountered in real-world applications. Applications listed in 表 2 can be centered on or operated near the particular frequency shown. Depending on the end-system requirements, additional EMI filters may be required near the signal inputs of the system, as well as incorporating known good practices such as using short traces, low-pass filters, and damping resistors combined with parallel and shielded signal routing.

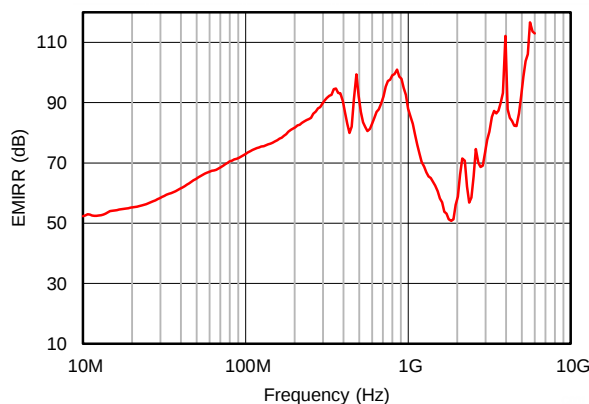


图 53. Common-Mode EMIRR Testing

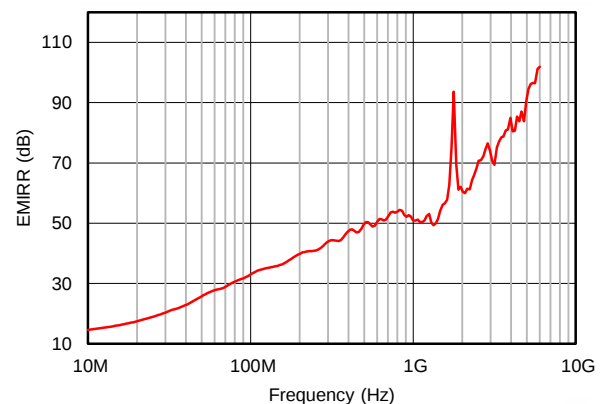


图 54. Differential Mode EMIRR Testing

表 2. INA828 EMIRR for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	DIFFERENTIAL EMIRR	COMMON-MODE EMIRR
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh-frequency (UHF) applications	48 dB	87 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (up to 1.6 GHz), GSM, aeronautical mobile, UHF applications	52 dB	98 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	94 dB	51 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	66 dB	57 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	79 dB	87 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	90 dB	92 dB

7.3.3 Input Common-Mode Range

The linear input voltage range of the INA828 input circuitry extends within 2 Volts of both power supplies and maintains excellent common-mode rejection throughout this range. The common-mode range for the most common operating conditions are shown in [Figure 55](#), [Figure 56](#), and [Figure 51](#). The common-mode range for other operating conditions is best calculated using the [INA common-mode range calculating tool](#). The INA828 device can operate over a wide range of power supplies and VREF configurations, thus providing a comprehensive guide to common-mode range limits for all possible conditions is impractical.

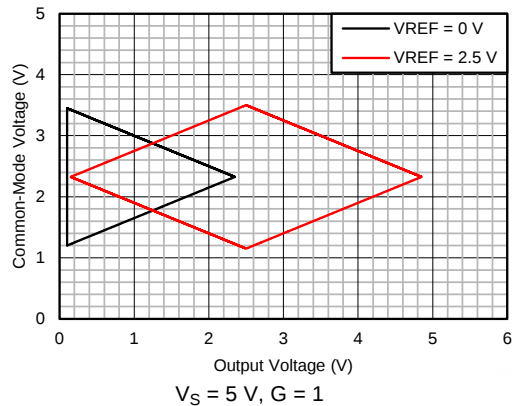


Figure 55. Input Common-Mode Voltage vs Output Voltage

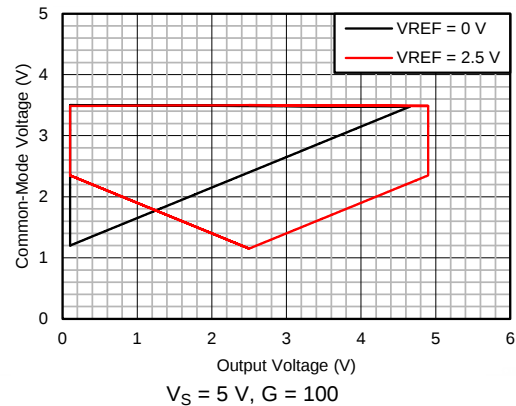


Figure 56. Input Common-Mode Voltage vs Output Voltage

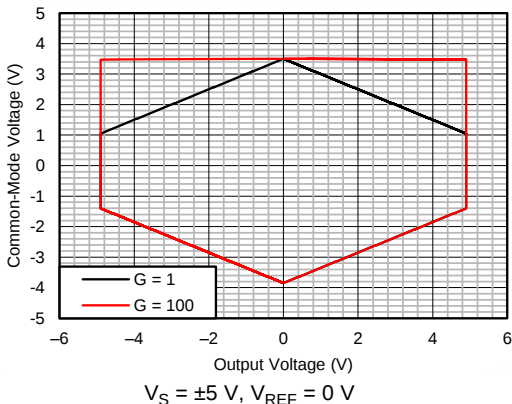


Figure 57. Input Common-Mode Voltage vs Output Voltage

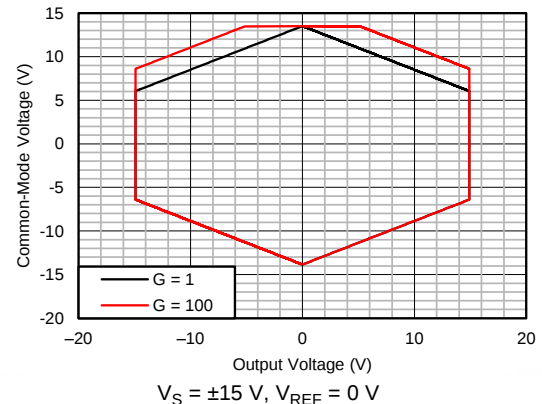


Figure 58. Input Common-Mode Voltage vs Output Voltage

7.3.4 Input Protection

The inputs of the INA828 device are individually protected for voltages up to ± 40 V. For example, a condition of -40 V on one input and 40 V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 8 mA.

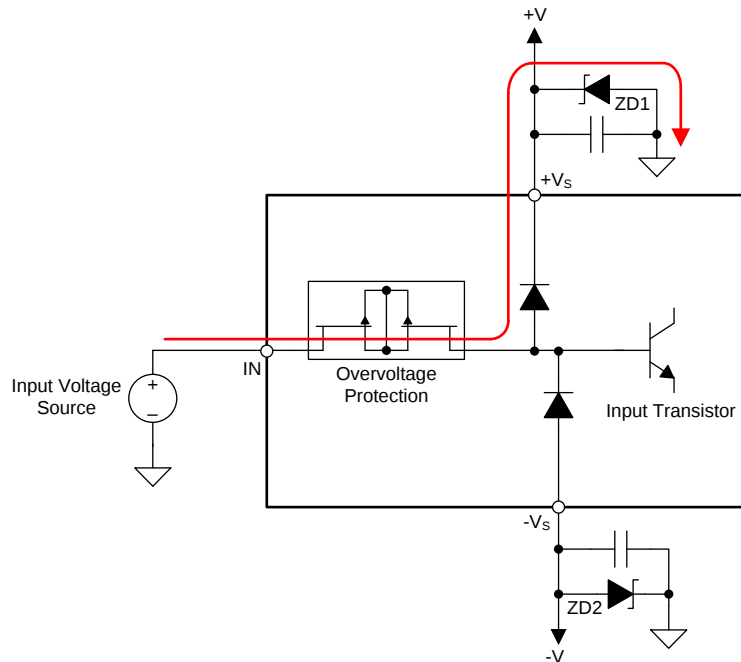


FIG 59. Input Current Path During an Overvoltage Condition

During an input overvoltage condition, current flows through the input protection diodes into the power supplies, see FIG 59. If the power supplies are unable to sink current, then Zener diode clamps (ZD1 and ZD2 in FIG 59) must be placed on the power supplies to provide a current pathway to ground. FIG 60 illustrates the input current for input voltages from -40 V to $+40$ V when the INA828 is powered by ± 15 -V supplies.

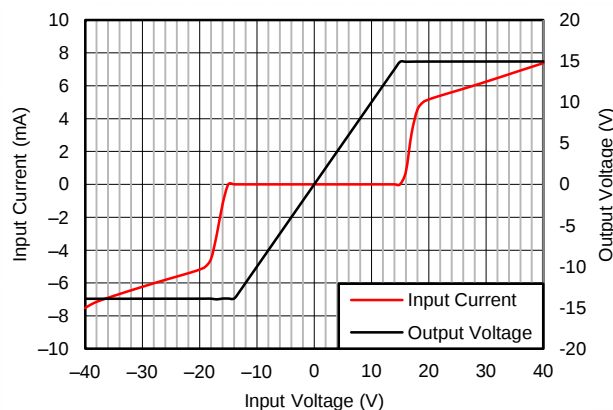


FIG 60. Input Current vs Input Overvoltage

7.3.5 Operating Voltage

The INA828 operates over a power-supply range of 4.5 V to 36 V (± 2.25 V to ± 18 V).

注意

Supply voltages higher than 40 V (± 20 V) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section of this data sheet.

7.4 Device Functional Modes

The INA828 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (± 2.25 V). The maximum power-supply voltage for the INA828 is 36 V (± 18 V).

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Reference Terminal

The output voltage of the INA828 is developed with respect to the voltage on the reference terminal, REF. Often, in dual-supply operation, the reference pin (pin 6) is connected to the low-impedance system ground. In single-supply operation, offsetting the output signal to a precise mid-supply level is useful (for example, 2.5 V in a 5-V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level-shift the output so that the INA828 can drive a single-supply ADC.

The voltage source applied to the reference terminal must have a low output impedance. As illustrated in [Figure 61](#), any resistance at the reference terminal (shown as R_{REF} in [Figure 61](#)) is in series with one of the internal 40-k Ω resistors.

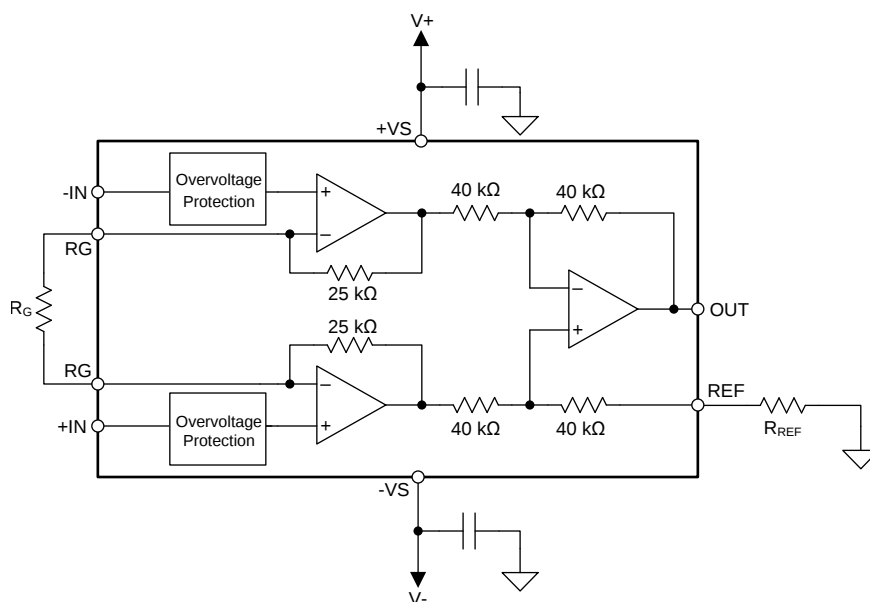


Figure 61. Parasitic Resistance Shown at the Reference Terminal

The parasitic resistance at the reference terminal, R_{REF} , creates an imbalance in the 4 resistors of the internal difference amplifier, resulting in degraded common-mode rejection ratio (CMRR). [Figure 62](#) shows the degradation in CMRR of the INA828 for increasing resistance at the reference terminal. For the best performance, keep the source impedance to the REF terminal, R_{REF} , below 5 Ω .

Reference Terminal (continued)

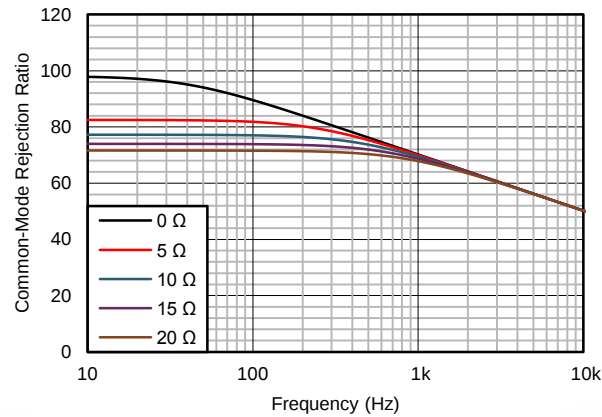
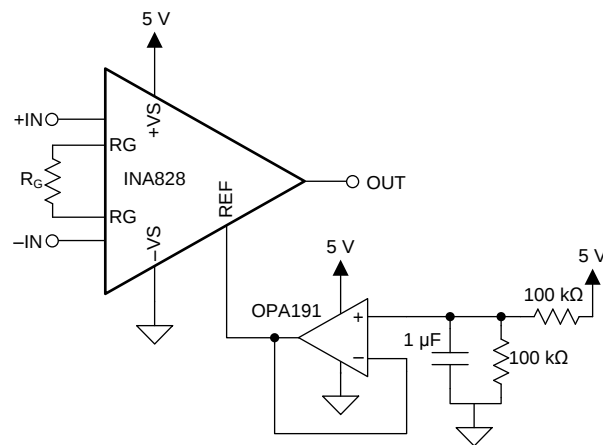


FIG 62. The Effect of Increasing Resistance at the Reference Terminal

Voltage reference ICs are an excellent option for providing a low-impedance voltage source for the reference terminal. However, if a resistor voltage divider is used to generate a reference voltage, it must be buffered by an op amp as shown in FIG 63 to avoid CMRR degradation.



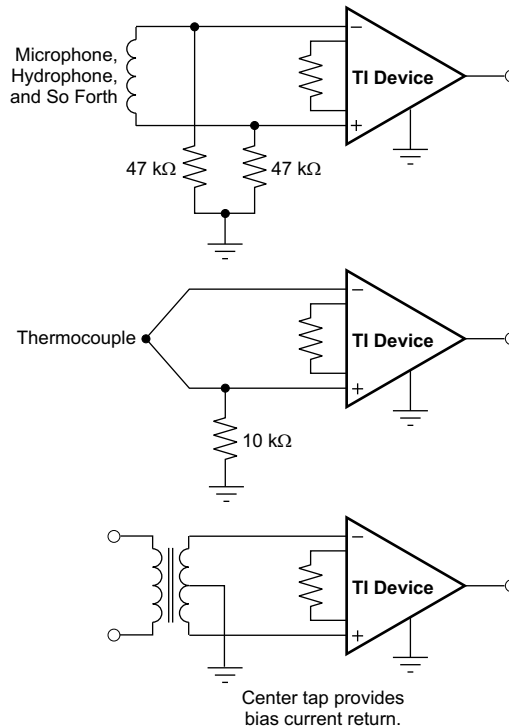
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FIG 63. Using an Op Amp to Buffer Reference Voltages

8.2 Input Bias Current Return Path

The input impedance of the INA828 is extremely high—approximately 100 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically 150 pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. [Figure 64](#) shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA828, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path can be connected to one input (as shown in the thermocouple example in [Figure 64](#)). With a higher source impedance, using two equal resistors provides a balanced input with possible advantages of a lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.



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Figure 64. Providing an Input Common-Mode Current Path

8.3 PCB Assembly Effects on Precision

The printed-circuit board (PCB) assembly process, including reflow soldering, imparts thermal stresses on the INA828 which can degrade the precision of the device and must be considered in the development of very-high-precision systems. Baking the PCBs after the assembly process can restore the precision of the device to pre-assembly values. Figure 65, Figure 66, and Figure 67 illustrate the effect of reflow soldering on the typical distribution of input offset voltage of the INA828. Figure 65 shows the distribution of input offset voltage for a set of INA828 devices prior to the PCB assembly process. Exposing the INA828 to a JEDEC-standard thermal profile for reflow soldering produces the histogram shown in Figure 66 on another set of INA828 devices. The standard deviation of input offset voltage has almost doubled due to the thermal stress imparted to the INA828 from the reflow process. However, baking INA828 units for 30 minutes at 125°C after the reflow soldering process produced the distribution given in Figure 67. The post-reflow bake restored the standard deviation of the input offset voltage to pre-assembly levels.

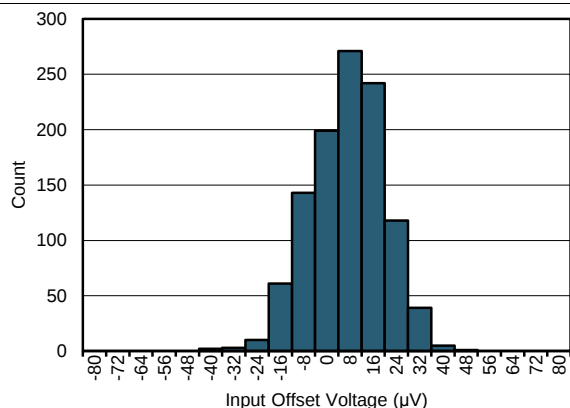


Figure 65. Typical Distribution of INA828 Input Offset Voltage Prior to Reflow Soldering

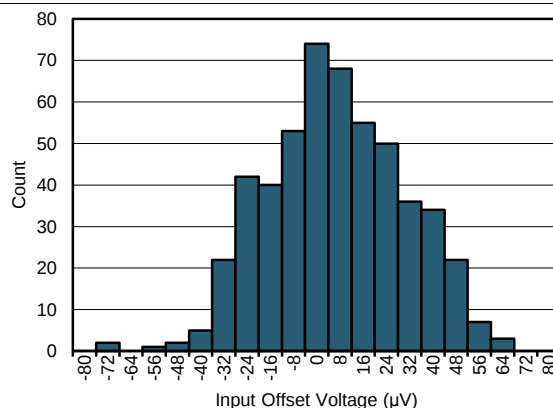


Figure 66. Typical Distribution of INA828 Input Offset Voltage After Reflow Soldering

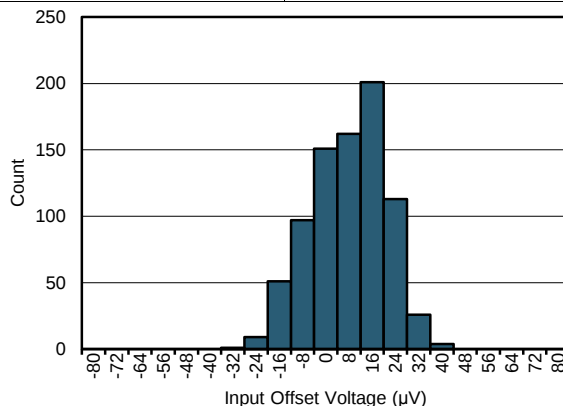
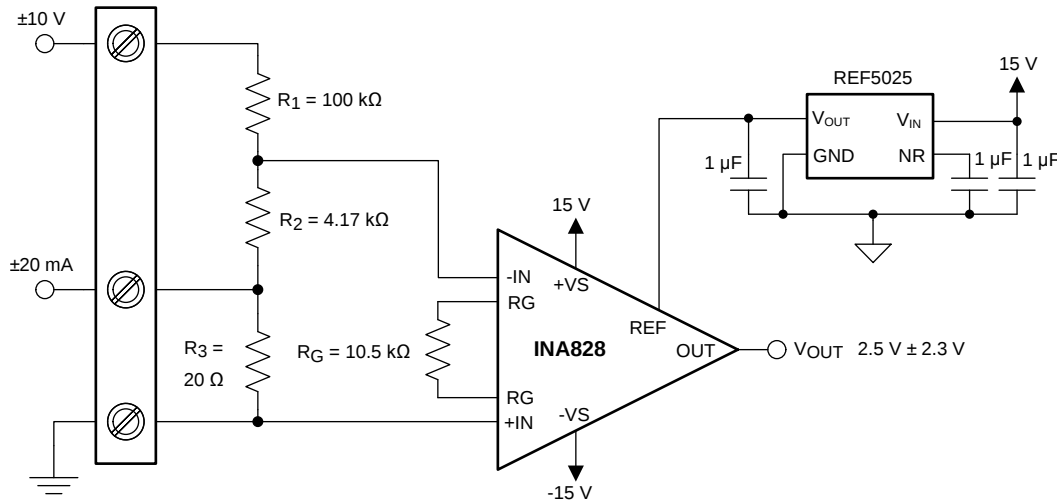


Figure 67. Typical Distribution of Post-Reflow INA828 Units Baked at 125°C for 30 Minutes

8.4 Typical Application

Figure 68 shows a three-terminal programmable-logic controller (PLC) design for the INA828. This PLC reference design accepts inputs of ± 10 V or ± 20 mA. The output is a single-ended voltage of $2.5 \text{ V} \pm 2.3 \text{ V}$ (or 200 mV to 4.8 V). Many PLCs typically have these input and output ranges.



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Figure 68. PLC Input (± 10 V, 4 mA to 20 mA)

8.4.1 Design Requirements

For this application, the design requirements are:

- 4-mA to 20-mA input with less than 20-Ω burden
- ± 20 -mA input with less than 20-Ω burden
- ± 10 -V input with impedance of approximately 100 kΩ
- Maximum 4-mA to 20-mA or ± 20 -mA burden voltage equal to $\pm 0.4 \text{ V}$
- Output range within 0 V to 5 V

8.4.2 Detailed Design Procedure

There are two modes of operation for the circuit shown in Figure 68: current input and voltage input. This design requires $R_1 \gg R_2 \gg R_3$. Given this relationship, Equation 3 calculates the current input mode transfer function.

$$V_{\text{OUT-I}} = V_D \times G + V_{\text{REF}} = -(I_{\text{IN}} \times R_3) \times G + V_{\text{REF}}$$

where

- G represents the gain of the instrumentation amplifier
- V_D represents the differential voltage at the INA828 inputs
- V_{REF} is the voltage at the INA828 REF pin
- I_{IN} is the input current

(3)

Equation 4 shows the transfer function for the voltage input mode.

$$V_{\text{OUT-V}} = V_D \times G + V_{\text{REF}} = -\left[V_{\text{IN}} \times \frac{R_2}{R_1 + R_2}\right] \times G + V_{\text{REF}}$$

where

- V_{IN} is the input voltage

(4)

R_1 sets the input impedance of the voltage input mode. The minimum typical input impedance is 100 kΩ. 100 kΩ is selected for R_1 because increasing the R_1 value also increases noise. The value of R_3 must be extremely small compared to R_1 and R_2 . 20 Ω for R_3 is selected because that resistance value is much smaller than R_1 and yields an input voltage of $\pm 400 \text{ mV}$ when operated in current mode ($\pm 20 \text{ mA}$).

Typical Application (continued)

Use 式 5 to calculate R_2 given $V_D = \pm 400$ mV, $V_{IN} = \pm 10$ V, and $R_1 = 100$ k Ω .

$$V_D = V_{IN} \times \frac{R_2}{R_1 + R_2} \rightarrow R_2 = \frac{R_1 \times V_D}{V_{IN} - V_D} = 4.167 \text{ k}\Omega \quad (5)$$

The value obtained from 式 5 is not a standard 0.1% value, so 4.17 k Ω is selected. R_1 and R_2 also use 0.1% tolerance resistors to minimize error.

Use 式 6 to calculate the ideal gain of the instrumentation amplifier.

$$G = \frac{V_{OUT} - V_{REF}}{V_D} = \frac{4.8 \text{ V} - 2.5 \text{ V}}{400 \text{ mV}} = 5.75 \frac{\text{V}}{\text{V}} \quad (6)$$

式 7 calculates the gain-setting resistor value using the INA828 gain equation, 式 1.

$$R_G = \frac{50 \text{ k}\Omega}{G - 1} = \frac{50 \text{ k}\Omega}{5.75 - 1} = 10.5 \text{ k}\Omega \quad (7)$$

10.5 k Ω is a standard 0.1% resistor value that can be used in this design.

8.4.3 Application Curves

図 69 and 図 70 show typical characteristic curves for the circuit in 図 68.

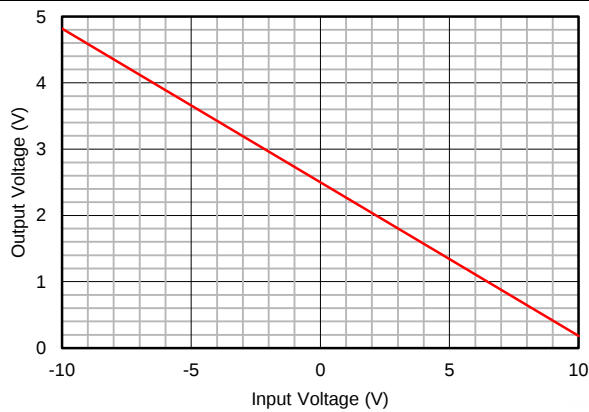


図 69. PLC Output Voltage vs Input Voltage

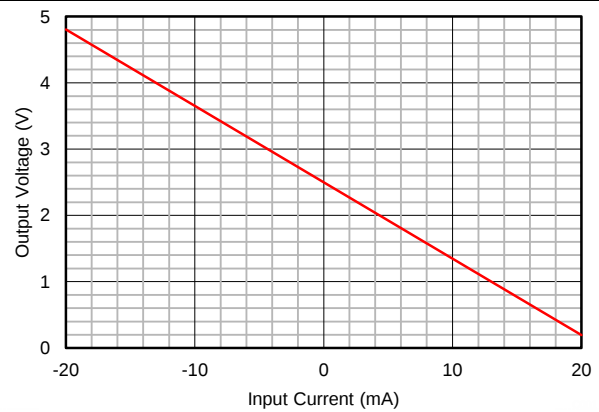


図 70. PLC Output Voltage vs Input Current

9 Power Supply Recommendations

The nominal performance of the INA828 is specified with a supply voltage of ± 15 V and mid-supply reference voltage. The device can also be operated using power supplies from ± 1.5 V (3 V) to ± 18 V (36 V) and non mid-supply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are illustrated in the [Typical Characteristics](#) section.

10 Layout

10.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

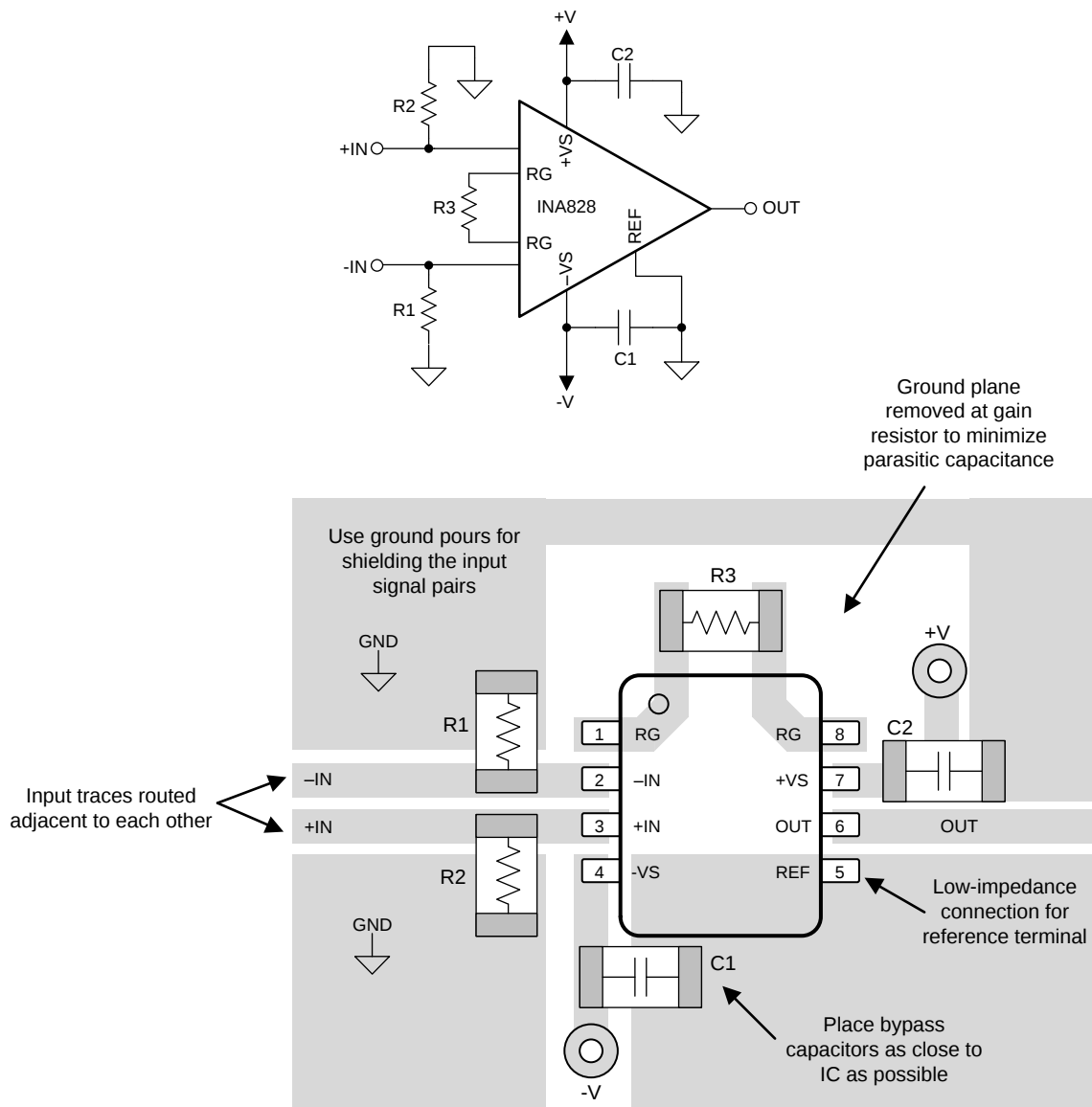
- Care must be taken to assure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. In addition, parasitic capacitance at the gain-setting pins can also affect CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS[®] relays to change the value of R_G , select the component so that the switch capacitance is as small as possible.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the device itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from $V+$ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [Figure 74](#), keeping R_G close to the pins minimizes parasitic capacitance.
- Keep the traces as short as possible.

INA828

JAJSR5A –AUGUST 2017 –REVISED JANUARY 2018

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10.2 Layout Example



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74. Example Schematic and Associated PCB Layout

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- 『REF50xx 低ノイズ、超低ドリフト係数、高精度基準電圧』
- 『OPA191 低消費電力、高精度、36V、e-trim CMOS アンプ』
- 『SPICE ベースのアナログ・シミュレーション・プログラム』
- 『計測アンプの入力同相範囲を計算』

11.2 ドキュメントの更新通知を受け取る方法

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11.3 コミュニティ・リソース

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11.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA828ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA828
INA828ID.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA828
INA828IDG4.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA828
INA828IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA828
INA828IDR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA828

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

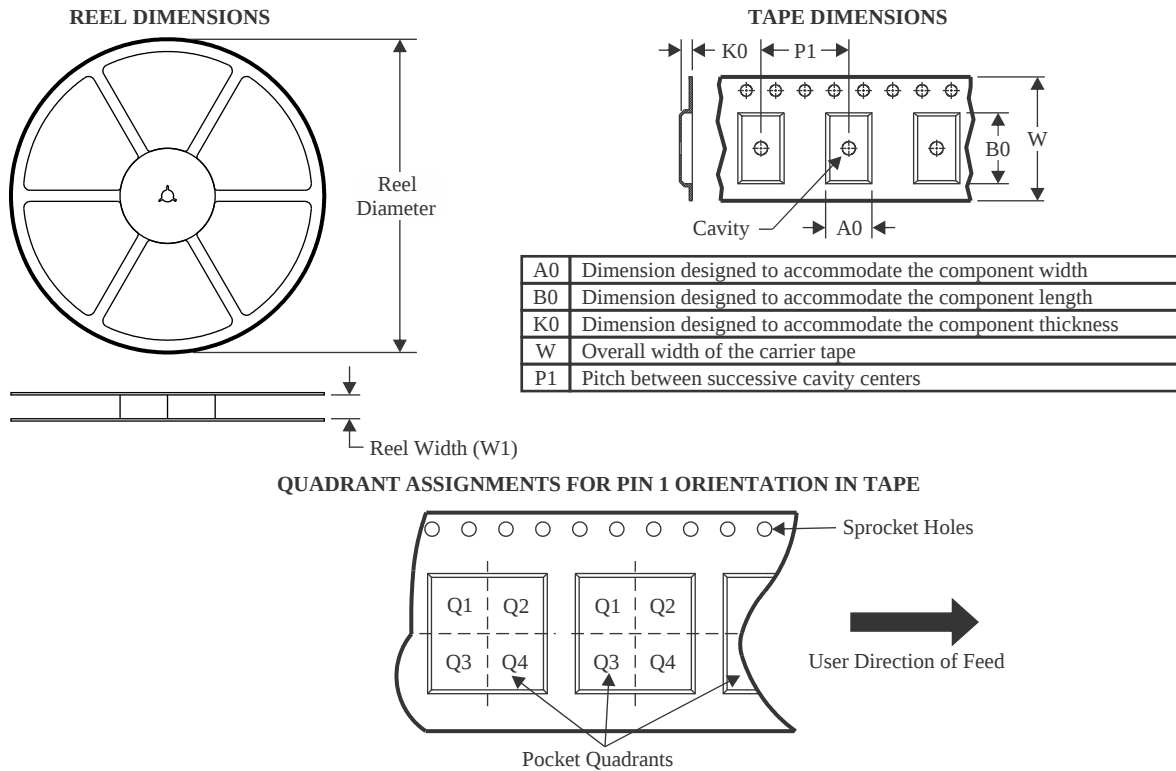
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "--" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA828IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

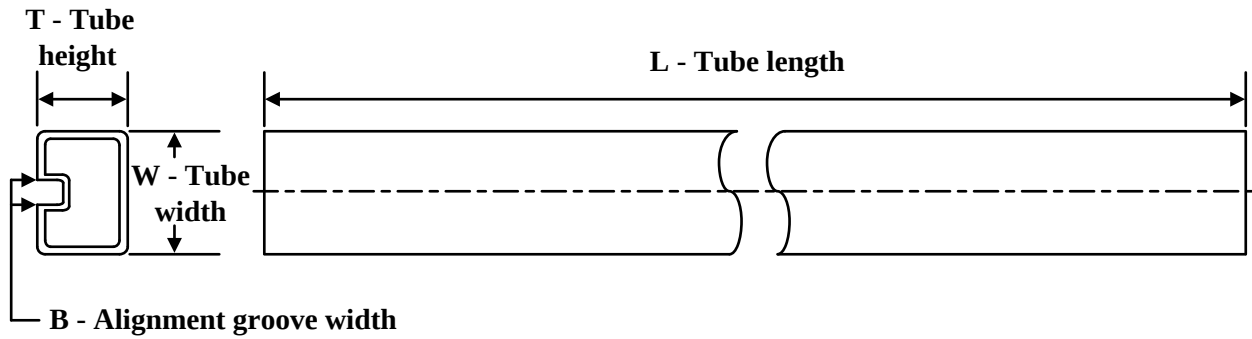
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

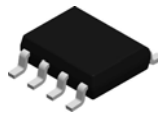
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA828IDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA828ID	D	SOIC	8	75	506.6	8	3940	4.32
INA828ID.B	D	SOIC	8	75	506.6	8	3940	4.32
INA828IDG4.B	D	SOIC	8	75	506.6	8	3940	4.32

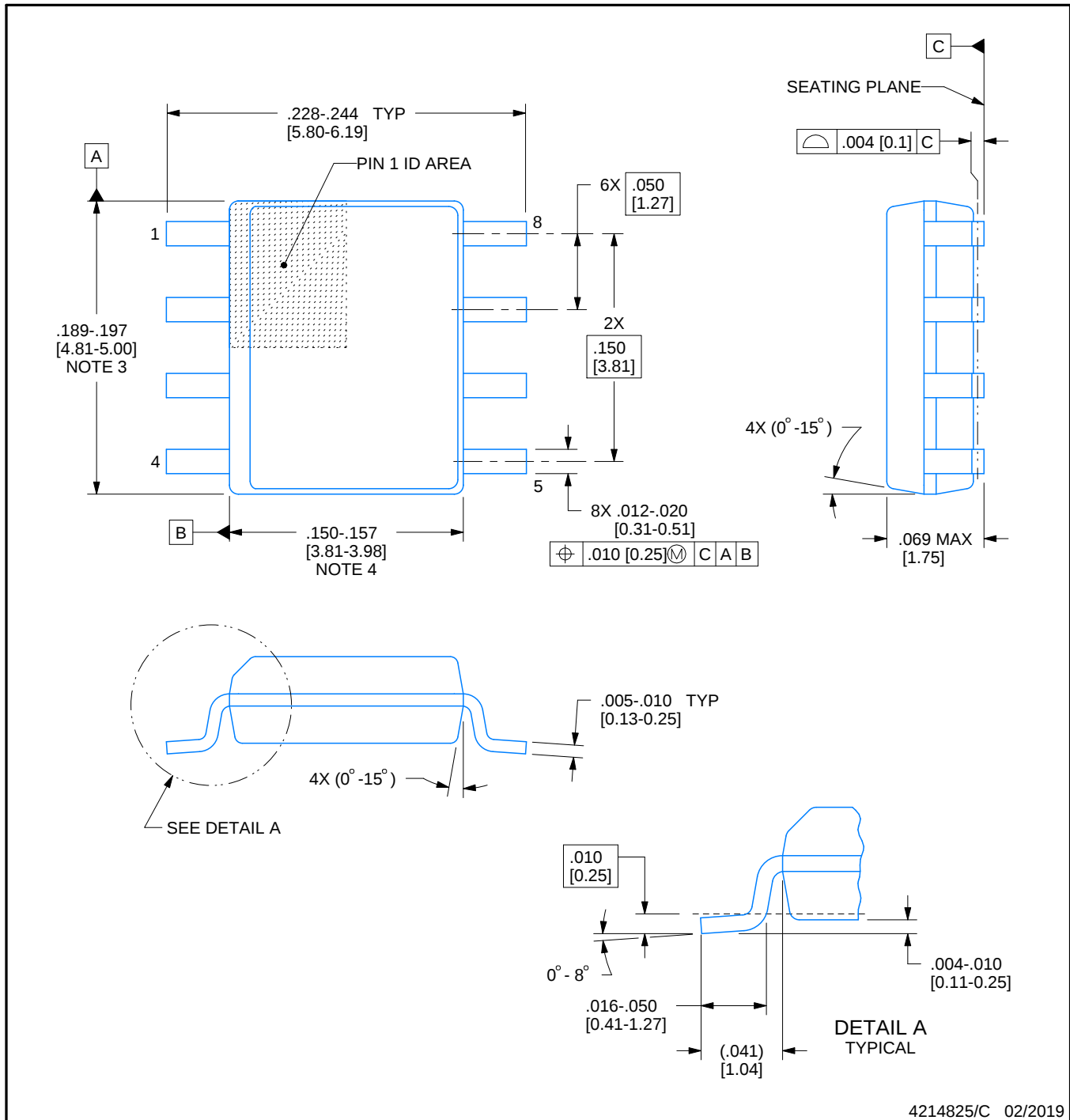


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

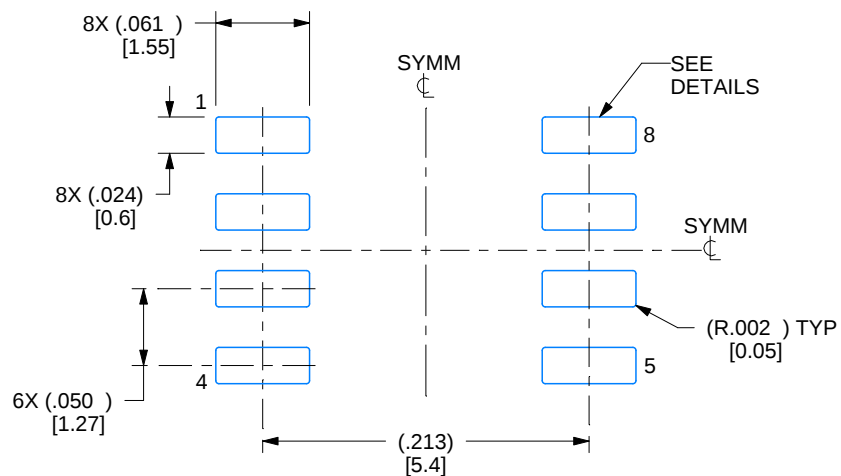
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

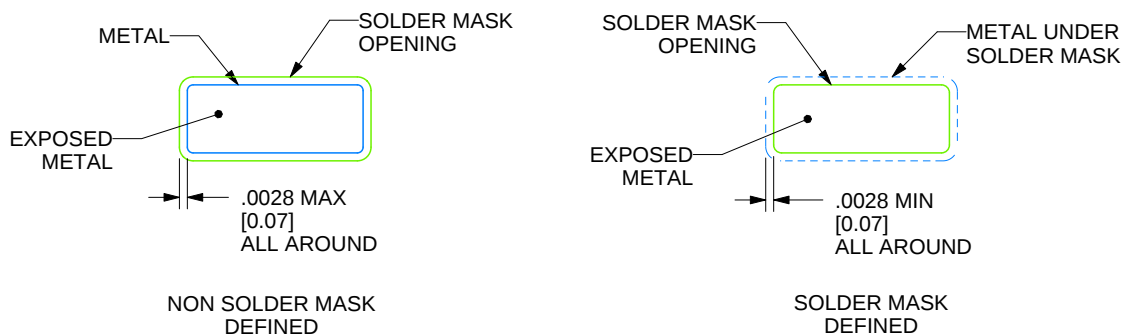
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

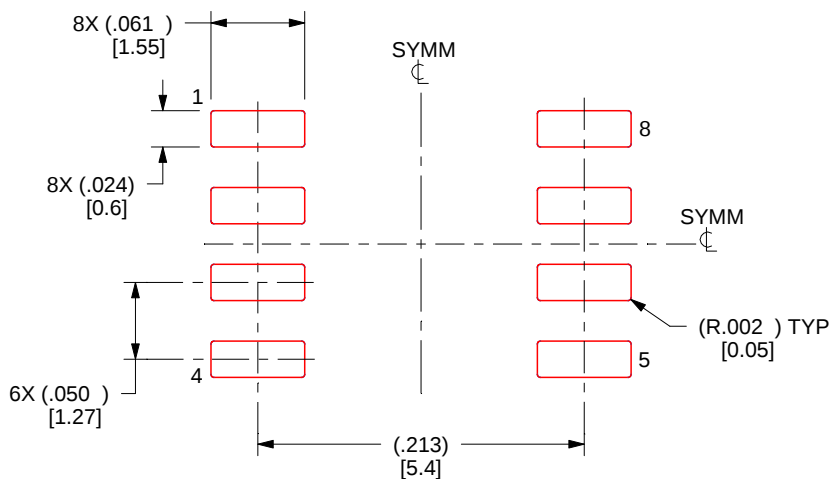
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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