INA821 35µVオフセット、7nV/√Hzノイズ、低消費電力、高精度計装アンプ

1 特長

- 低いオフセット電圧： 10µV (標準値)、35µV (最大値)
- ゲイン・ドリフト係数： 5ppm/°C (G = 1)、35ppm/°C (G > 1) (最大値)
- ノイズ: 7nV/√Hz
- 帯域幅: 4.7MHz (G = 1)、290kHz (G = 100)
- 1nF の容量性負荷で安定
- ±40V まで入力を保護
- 同相除去比： 112dB、G = 10 (最小値)
- 電源除去比：110dB、G = 1 (最小値)
- 消費電流： 650µA (最大値)
- 電源電圧範囲
  - 単一電源: 4.5V～36V
  - デュアル電源: ±2.25V～±18V
- 定格温度範囲： -40°C～+125°C
- パッケージ： 8 ピン SOIC および VSSOP

2 アプリケーション

- バッテリ・テスト機器
- 流量トランスミッタ
- ECG アンプ
- アナログ入力モジュール
- サーキット・ブレーカ
- 産業用プロセス制御
- ラボ計測機器

3 概要

INA821 は、広い電圧範囲の単一電源またはデュアル電源で動作する、低消費電力の高精度計装アンプです。単一の外付け抵抗によって、1～10,000 の範囲でゲインを設定できます。このデバイスは、入力オフセット電圧、オフセット電圧ドリフト、入力バイアス電流、入力電圧ノイズ、入力電流ノイズを極めて低く抑える新しいスーパーβ入力トランジスタを使用することで、卓越した精度を実現します。追加回路により、±40V までの過電圧から入力を保護します。

INA821 は、高い同相除去比を実現するよう最適化されています。G = 1 での同相除去比は、全入力同相範囲を通じて 92dB を上回ります。このデバイスは、4.5V 単一電源および最大 ±18V のデュアル電源による低電圧動作用に設計されています。

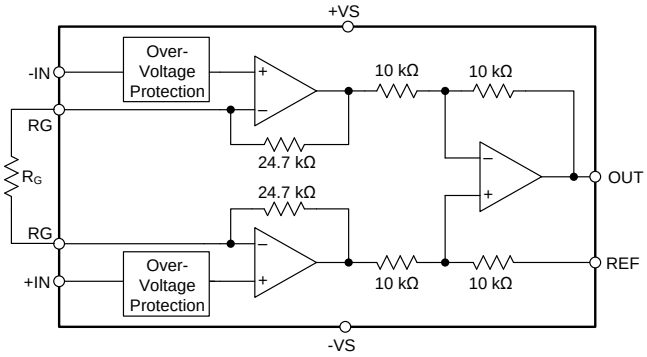
INA821 は 8 ピン SOIC および 8 ピン VSSOP パッケージで供給され、-40℃～+125℃の温度範囲で動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
INA821	SOIC (8)	4.90mm×3.91mm
	VSSOP (8)	3.00mm×3.00mm

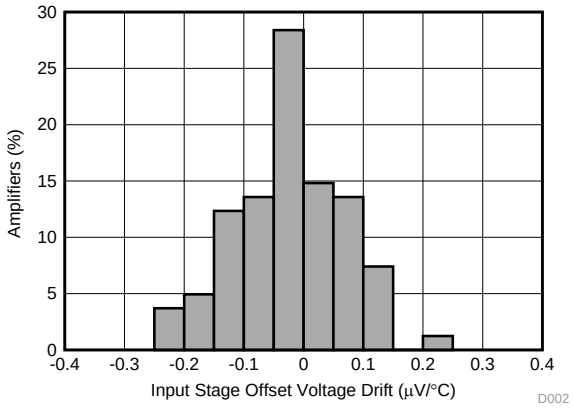
(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

INA821 の簡略化された内部回路図



$$G = 1 + \frac{49.4\ k\Omega}{R_G} \qquad V_O = G(V_{+IN} - V_{-IN}) + V_{REF}$$

入力段のオフセット電圧ドリフトの代表的な分布



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (May 2019) から Revision C に変更 — **Page**

- DGK (VSSOP) パッケージを事前情報 (プレビュー) から量産データ (アクティブ) に 変更 ... 1
- 変更 Figure 9, *Typical Distribution of Input Offset Current*, to show correct image ... 11
- 変更 Figure 27, *Typical Distribution of Gain Error, G = 1*, to show improved data ... 14

Revision A (December 2018) から Revision B に変更 — **Page**

- データシートに 8 ピン DGK (VSSOP) 事前情報パッケージと関連情報を 追加 ... 1
- 「アプリケーション」の項目 変更 ... 1

2018年8月発行のものから更新 — **Page**

- 量産データ・データシートの初回リリース ... 1

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5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION	RG PINS AT PIN
INA821	35-µV Offset, 0.4 µV/°C V_{OS} Drift, 7-nV/√Hz Noise, High-Bandwidth, Precision Instrumentation Amplifier	G = 1 + 49.4 kΩ / RG	2, 3
INA819	35-µV Offset, 0.4 µV/°C V_{OS} Drift, 8-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50 kΩ / RG	2, 3
INA818	35-µV Offset, 0.4 µV/°C V_{OS} Drift, 8-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50 kΩ / RG	1, 8
INA828	50-µV Offset, 0.5 µV/°C V_{OS} Drift, 7-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50 kΩ / RG	1, 8
INA333	25-µV V_{OS}, 0.1 µV/°C V_{OS} Drift, 1.8-V to 5-V, RRO, 50-µA I_Q, Chopper-Stabilized INA	G = 1 + 100 kΩ / RG	1, 8
PGA280	20-mV to ±10-V Programmable Gain IA With 3-V or 5-V Differential Output; Analog Supply up to ±18 V	Digital programmable	N/A
INA159	G = 0.2 V Differential Amplifier for ±10-V to 3-V and 5-V Conversion	G = 0.2 V/V	N/A
PGA112	Precision Programmable Gain Op Amp With SPI	Digital programmable	N/A

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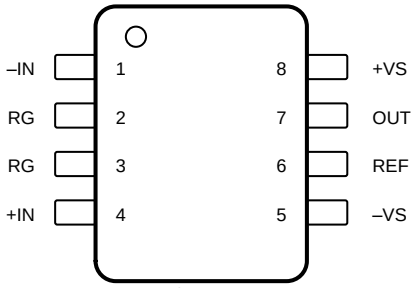
6 Pin Configuration and Functions

D and DGK Packages
8-Pin SOIC and 8-Pin VSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	1	I	Negative (inverting) input
+IN	4	O	Positive (noninverting) input
OUT	7	—	Output
RG	2, 3	I	Gain setting pin. Place a gain resistor between pin 2 and pin 3.
REF	6	—	Reference input. This pin must be driven by a low impedance source.
–VS	5	—	Negative supply
+VS	8		Positive supply

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage		–20	20	V
Signal input pins	Voltage	–40	40	V
	REF pin	–20	20	
Signal output pins		$(-V_S)$ - 0.5	$(+V_S)$ + 0.5	V
Output short-circuit[2]		Continuous		
Operating Temperature, T_A		–50	150	°C
Junction Temperature, T_J			175	
Storage Temperature, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage V_S	Single-supply	4.5	36	V
	Dual-supply	±2.25	±18	
Specified temperature	Specified temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		INA821		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.6	215.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.3	66.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.9	97.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.5	10.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.4	96.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OSI}	Input stage offset voltage(1)(2)	T_A = 25°C	INA821ID		10	35	µV
			INA821IDGK			40	µV
		T_A = –40°C to 125°C(3)	INA821ID			75	µV
			INA821IDGK			80	µV
		vs temperature, T_A = –40°C to 125°C				0.4	µV/°C
V_{OSO}	Output stage offset voltage(1)(2)	T_A = 25°C			50	350	µV
		T_A = –40°C to 125°C(3)				850	µV
		vs temperature, T_A = –40°C to 125°C				5	µV/°C
PSRR	Power-supply rejection ratio	G = 1, RTI		110	120		dB
		G = 10, RTI		114	130		
		G = 100, RTI		130	135		
		G = 1000, RTI		136	140		
z_{id}	Differential impedance				100 || 1		GΩ || pF
z_{ic}	Common-mode impedance				100 || 7		GΩ || pF
	RFI filter, –3-dB frequency				45		MHz
V_{CM}	Operating input range(4)			(V–) + 2		(V+) – 2	V
		V_S = ±2.25 V to ±18 V, T_A = –40°C to 125°C		See 図 51 to 図 54			
	Input overvoltage range	T_A = –40°C to 125°C(3)				±40	V
CMRR	Common-mode rejection ratio	At DC to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 1		92	105		dB
		At DC to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 10		112	125		
		At DC to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 100		132	145		
		At DC to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 1000		140	150		
BIAS CURRENT							
I_B	Input bias current	V_{CM} = V_S / 2			0.15	0.5	nA
		T_A = –40°C to 125°C				2	
I_{OS}	Input offset current	V_{CM} = V_S / 2			0.15	0.5	nA
		T_A = –40°C to 125°C				2	
NOISE VOLTAGE							
e_{NI}	Input stage voltage noise(5)	f = 1 kHz, G = 100, R_S = 0 Ω			7		nV/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 100, R_S = 0 Ω			0.14		$µV_{PP}$
e_{NO}	Output stage voltage noise(5)	f = 1 kHz, R_S = 0 Ω			65		nV/√Hz
		f_B = 0.1 Hz to 10 Hz, R_S = 0 Ω			2.5		$µV_{PP}$
I_n	Noise current	f = 1 kHz			130		fA/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 100			4.7		pA_{PP}
GAIN							
G	Gain equation				1 + (49.4 kΩ / R_G)		V/V
	Range of gain			1		10000	V/V

(1) Total offset, referred-to-input (RTI): V_{OS} = (V_{OSI}) + (V_{OSO} / G).
(2) Offset drifts are uncorrelated. Input-referred offset drift is calculated using: $\Delta V_{OS(RTI)} = \sqrt{[\Delta V_{OSI}^2 + (\Delta V_{OSO} / G)^2]}$
(3) Specified by characterization.
(4) Input voltage range of the INA821 input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See *Typical Characteristic* curves 図 51 through 図 54 for more information.
(5) Total RTI voltage noise is equal to: $e_{N(RTI)} = \sqrt{[e_{NI}^2 + (e_{NO} / G)^2]}$

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Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GE	Gain error	G = 1, V_O = ±10 V		±0.005%	±0.025%	
		G = 10, V_O = ±10 V		±0.025%	±0.15%	
		G = 100, V_O = ±10 V		±0.025%	±0.15%	
		G = 1000, V_O = ±10 V		±0.05%		
	Gain vs temperature (6)	G = 1, T_A = –40°C to 125°C			±5	ppm/°C
		G > 1, T_A = –40°C to 125°C			±35	
	Gain nonlinearity	G = 1 to 10, V_O = –10 V to 10 V, R_L = 10 kΩ		1	10	ppm
		G = 100, V_O = –10 V to 10 V, R_L = 10 kΩ			15	
		G = 1000, V_O = –10 V to 10 V, R_L = 10 kΩ		10		
		G = 1 to 100, V_O = –10 V to 10 V, R_L = 2 kΩ		30		
OUTPUT						
	Voltage swing		(V–) + 0.15		(V+) – 0.15	V
	Load capacitance stability			1000		pF
Z_O	Closed-loop output impedance	f = 10 kHz		1.3		Ω
I_{SC}	Short-circuit current	Continuous to V_S / 2		±20		mA
FREQUENCY RESPONSE						
BW	Bandwidth, –3 dB	G = 1		4.7		MHz
		G = 10		970		kHz
		G = 100		290		
		G = 1000		30		
SR	Slew rate	G = 1, V_O = ±10 V		2.0		V/µs
t_S	Settling time	0.01%, G = 1 to 100, V_{STEP} = 10 V		6		µs
		0.01%, G = 1000, V_{STEP} = 10 V		40		
		0.001%, G = 1 to 100, V_{STEP} = 10 V		10		
		0.001%, G = 1000, V_{STEP} = 10 V		50		
REFERENCE INPUT						
R_{IN}	Input impedance			10		kΩ
	Voltage range		(V–)		(V+)	V
	Gain to output			1		V/V
	Reference gain error			0.01%		
POWER SUPPLY						
V_S	Power-supply voltage	Single-supply	4.5		36	V
		Dual-supply	±2.25		±18	
I_Q	Quiescent current	V_{IN} = 0 V		600	650	µA
		vs temperature, T_A = –40°C to 125°C			870	

(6) The values specified for G > 1 do not include the effects of the external gain-setting resistor, "R_G".

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7.6 Typical Characteristics: Table of Graphs

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

表 1. Table of Graphs

DESCRIPTION	FIGURE
Typical Distribution of Input Stage Offset Voltage	図 1
Typical Distribution of Input Stage Offset Voltage Drift	図 2
Typical Distribution of Output Stage Offset Voltage	図 3
Typical Distribution of Output Stage Offset Voltage Drift	図 4
Input Stage Offset Voltage vs Temperature	図 5
Output Stage Offset Voltage vs Temperature	図 6
Typical Distribution of Input Bias Current, T_A = 25°C	図 7
Typical Distribution of Input Bias Current, T_A = 90°C	図 8
Typical Distribution of Input Offset Current	図 9
Input Bias Current vs Temperature	図 10
Input Offset Current vs Temperature	図 11
Typical CMRR Distribution, G = 1	図 12
Typical CMRR Distribution, G = 10	図 13
CMRR vs Temperature, G = 1	図 14
CMRR vs Temperature, G = 10	図 15
Input Current vs Input Overvoltage	図 16
CMRR vs Frequency (RTI)	図 17
CMRR vs Frequency (RTI, 1-kΩ source imbalance)	図 18
Positive PSRR vs Frequency (RTI)	図 19
Negative PSRR vs Frequency (RTI)	図 20
Gain vs Frequency	図 21
Voltage Noise Spectral Density vs Frequency (RTI)	図 22
Current Noise Spectral Density vs Frequency (RTI)	図 23
0.1-Hz to 10-Hz RTI Voltage Noise, G = 1	図 24
0.1-Hz to 10-Hz RTI Voltage Noise, G = 1000	図 25
0.1-Hz to 10-Hz RTI Current Noise	図 26
Typical Distribution of Gain Error, G = 1	図 27
Typical Distribution of Gain Error, G = 10	図 28
Input Bias Current vs Common-Mode Voltage	図 29
Gain Error vs Temperature, G = 1	図 30
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Small-Signal Response, G = 1	図 43
Small-Signal Response, G = 10	図 44
Small-Signal Response, G = 100	図 45

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Typical Characteristics: Table of Graphs (continued)

表 1. Table of Graphs (continued)

DESCRIPTION	FIGURE
Small-Signal Response, G = 1000	図 46
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Differential-Mode EMI Rejection Ratio	図 49
Common-Mode EMI Rejection Ratio	図 50
Input Common-Mode Voltage vs Output Voltage, G = 1, V_S = 5 V	図 51
Input Common-Mode Voltage vs Output Voltage, G = 100, V_S = 5 V	図 52
Input Common-Mode Voltage vs Output Voltage, V_S = ±5 V	図 53
Input Common-Mode Voltage vs Output Voltage, V_S = ±15 V	図 54

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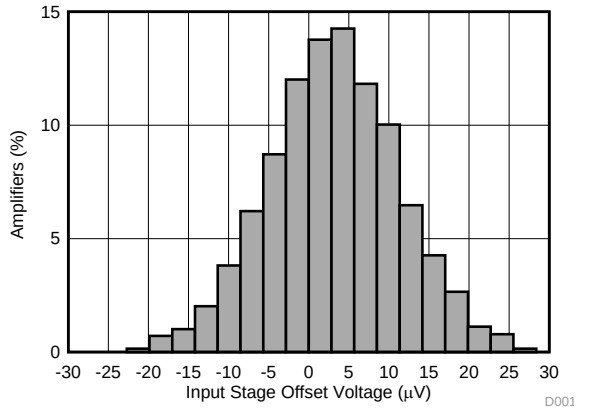
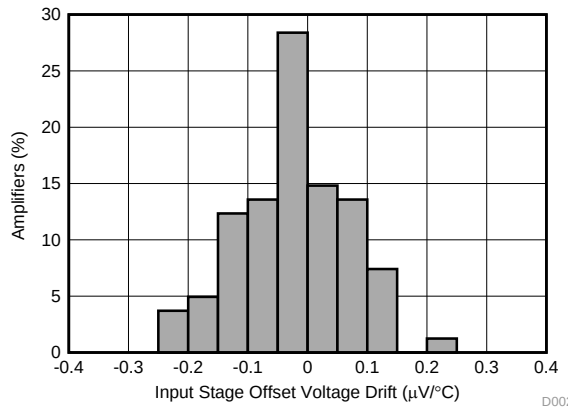
7.7 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



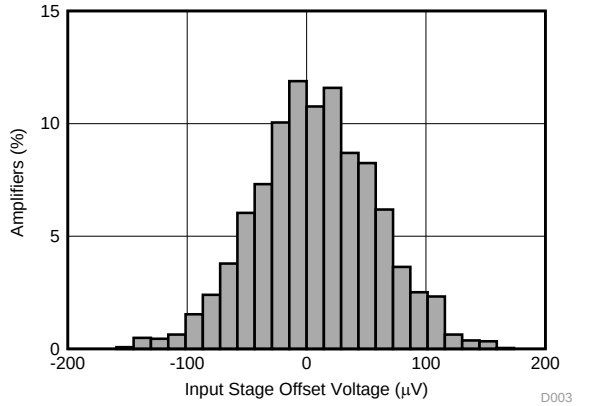
N = 2667 Mean = 3.1 µV Std. Dev. = 8.1 µV

図 1. Typical Distribution of Input Stage Offset Voltage



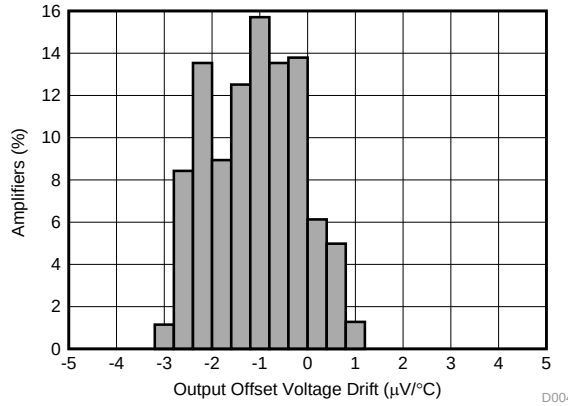
N = 81 Mean = -0.03 µV/°C Std. Dev. = 0.09 µV/°C

図 2. Typical Distribution of Input Stage Offset Voltage Drift



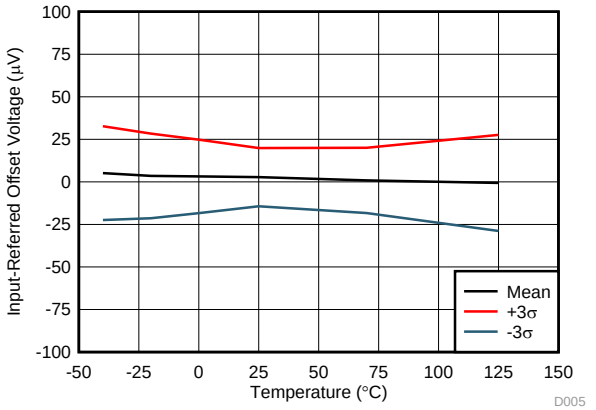
N = 2667 Mean = 7.7 µV Std. Dev. = 50.7 µV

図 3. Typical Distribution of Output Stage Offset Voltage



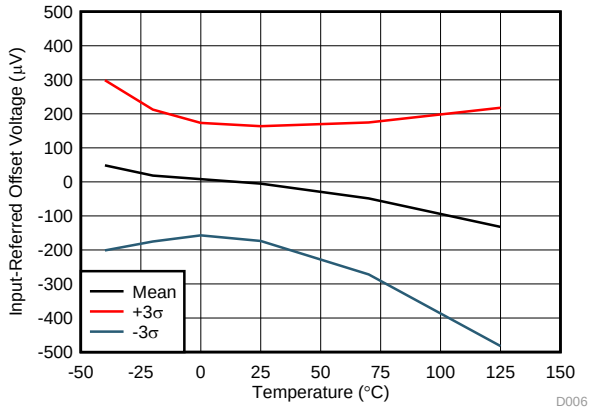
N = 81 Mean = –1.09 µV/°C Std. Dev. = 0.94 µV/°C

図 4. Typical Distribution of Output Stage Offset Voltage Drift



81 units

図 5. Input Stage Offset Voltage vs Temperature



81 units

図 6. Output Stage Offset Voltage vs Temperature

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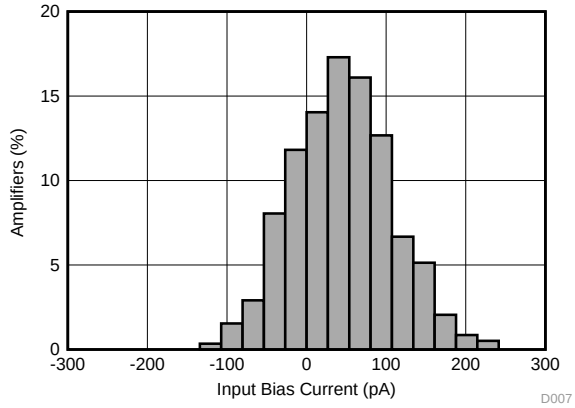
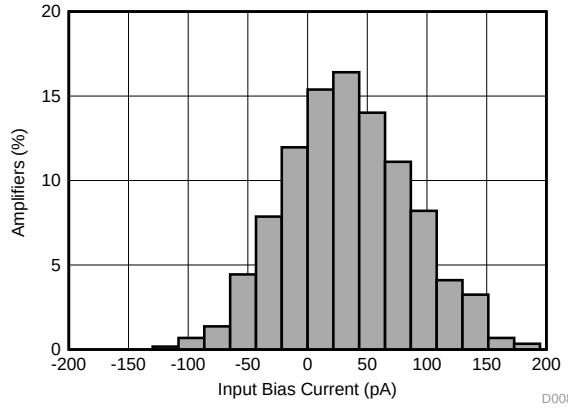
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



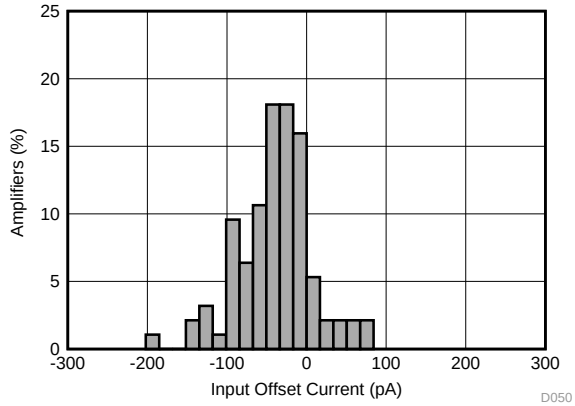
N = 292 Mean = 45 pA Std. Dev. = 62 pA
T_A = 25°C

図 7. Typical Distribution of Input Bias Current, T_A = 25°C



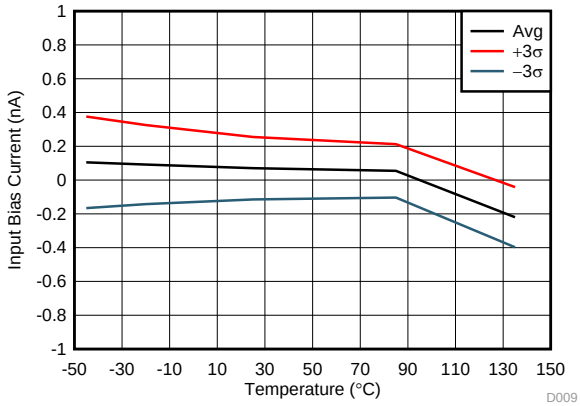
N = 292 Mean = 34 pA Std. Dev. = 52 pA
T_A = 90°C

図 8. Typical Distribution of Input Bias Current, T_A = 90°C



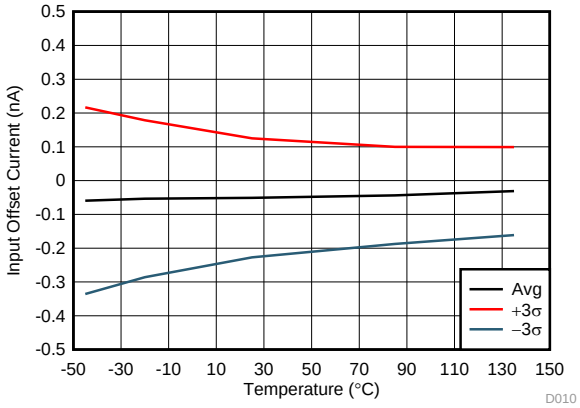
N = 94 Mean = –38.82 pA Std. Dev. = 47.24 pA

図 9. Typical Distribution of Input Offset Current



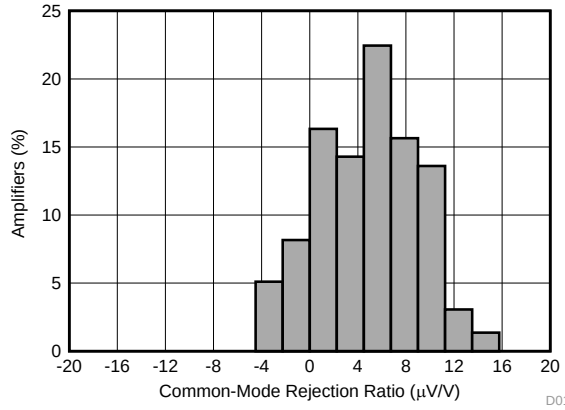
N = 294 G = 1

図 10. Input Bias Current vs Temperature



N = 294 G = 1

図 11. Input Offset Current vs Temperature

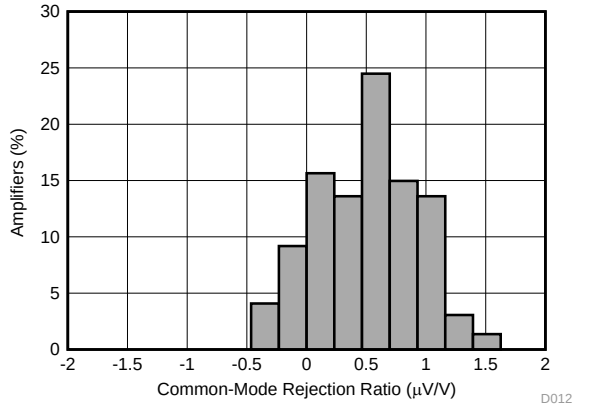


N = 294 Mean = 4.87 µV/V Std. Dev. = 4.14 µV/V
G = 1

図 12. Typical CMRR Distribution, G = 1

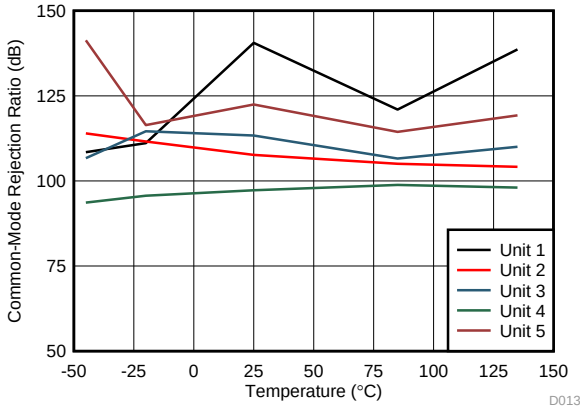
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



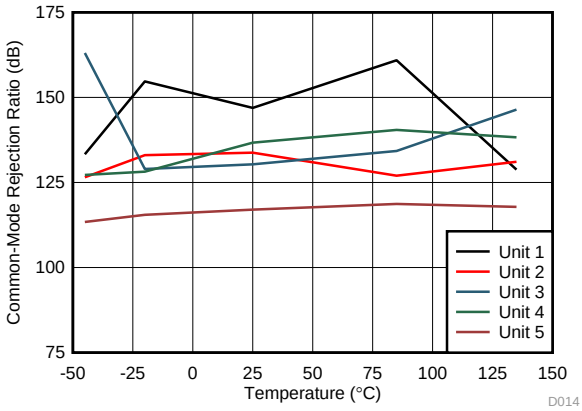
N = 294 Mean = 0.51 µV/V Std. Dev. = 0.42 µV/V
G = 10

図 13. Typical CMRR Distribution, G = 10



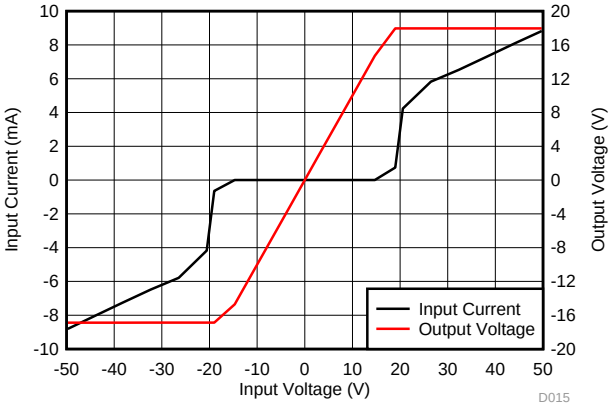
N = 5 G = 1

図 14. CMRR vs Temperature, G = 1



N = 5 G = 10

図 15. CMRR vs Temperature, G = 10



V_S = ±18 V

図 16. Input Current vs Input Overvoltage

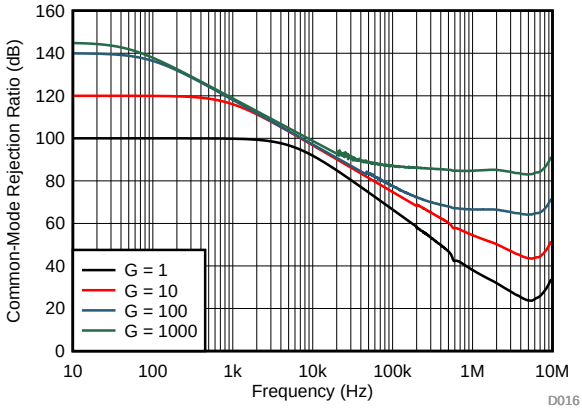


図 17. CMRR vs Frequency (RTI)

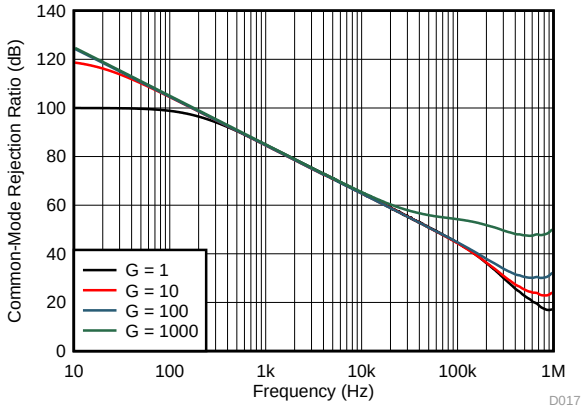


図 18. CMRR vs Frequency (RTI, 1-kΩ source imbalance)

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Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

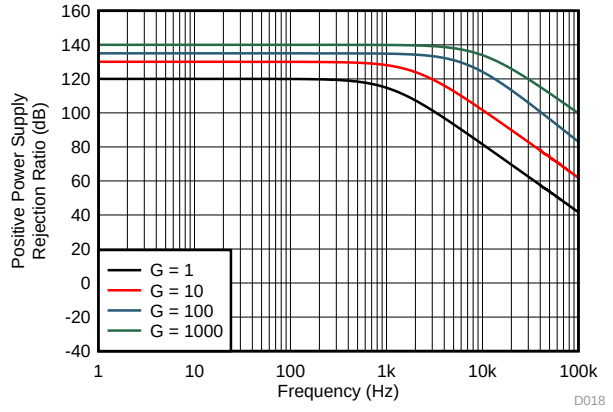


図 19. Positive PSRR vs Frequency (RTI)

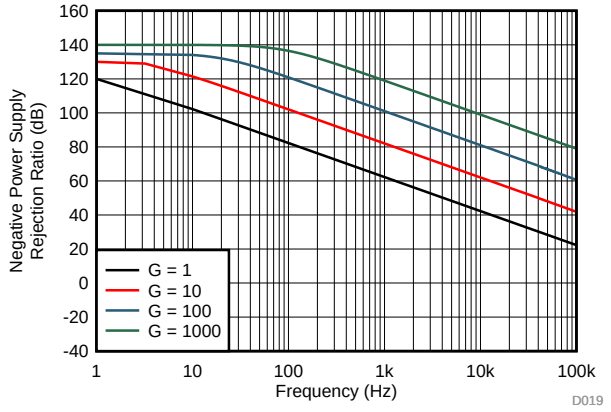


図 20. Negative PSRR vs Frequency (RTI)

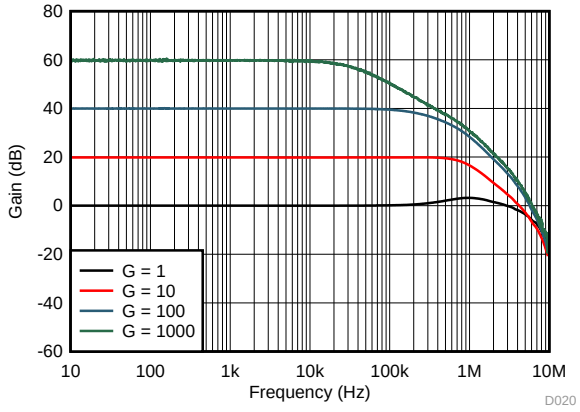


図 21. Gain vs Frequency

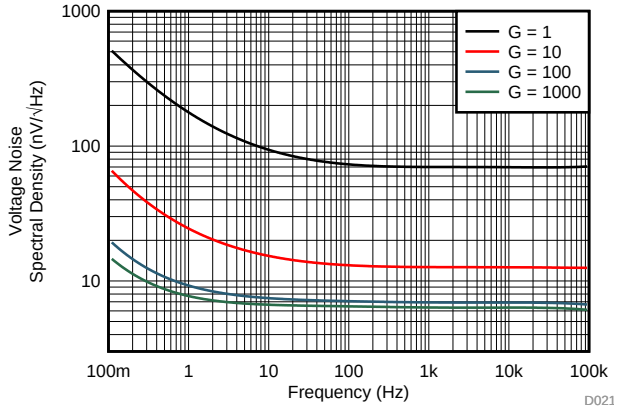


図 22. Voltage Noise Spectral Density vs Frequency (RTI)

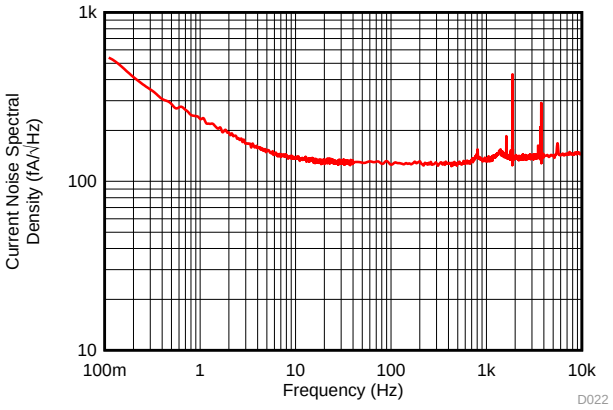
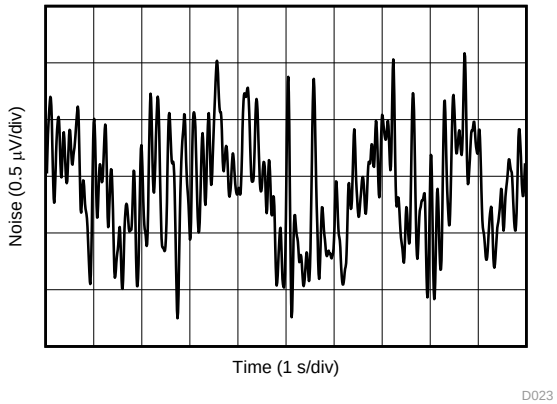


図 23. Current Noise Spectral Density vs Frequency (RTI)

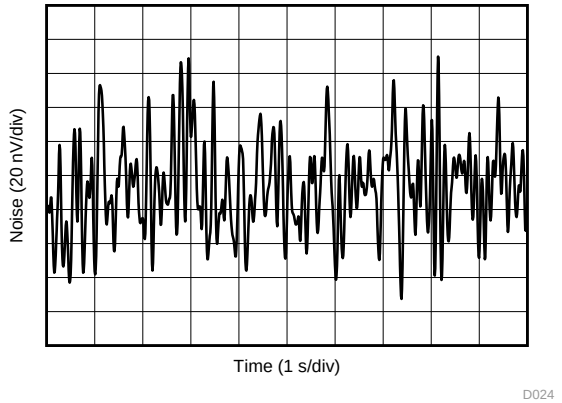


G = 1

図 24. 0.1-Hz to 10-Hz RTI Voltage Noise, G = 1

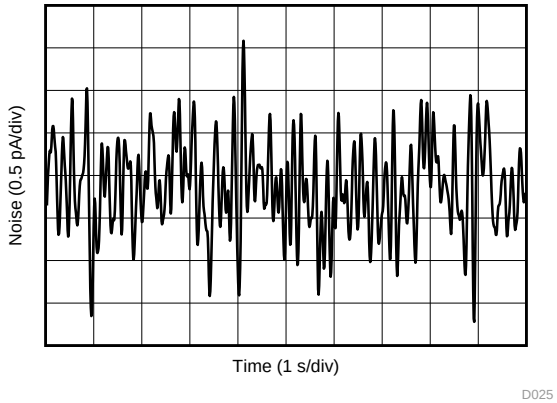
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



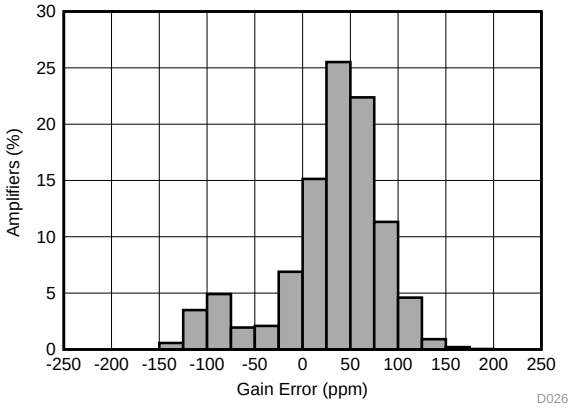
G = 1000

図 25. 0.1-Hz to 10-Hz RTI Voltage Noise, G = 1000



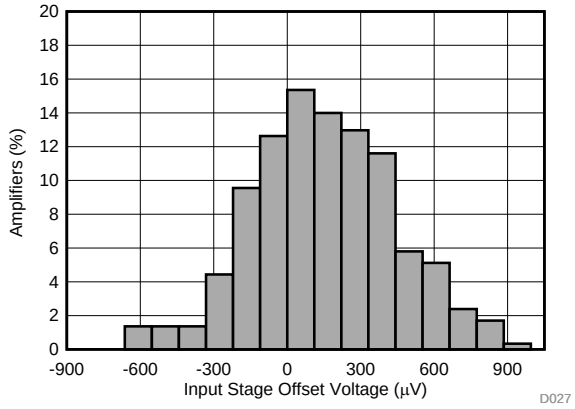
G = 1

図 26. 0.1-Hz to 10-Hz RTI Current Noise



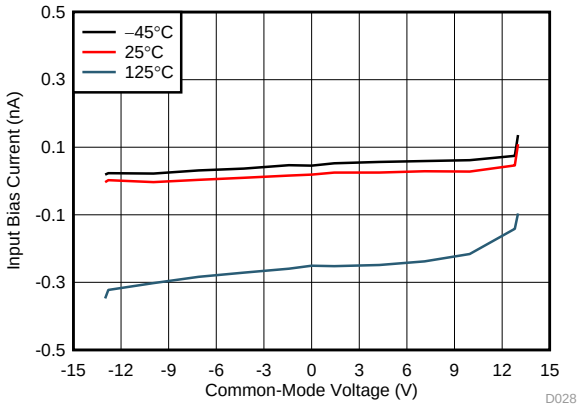
N = 5412 Mean = 30 ppm Std. Dev. = 55 ppm
G = 1

図 27. Typical Distribution of Gain Error, G = 1



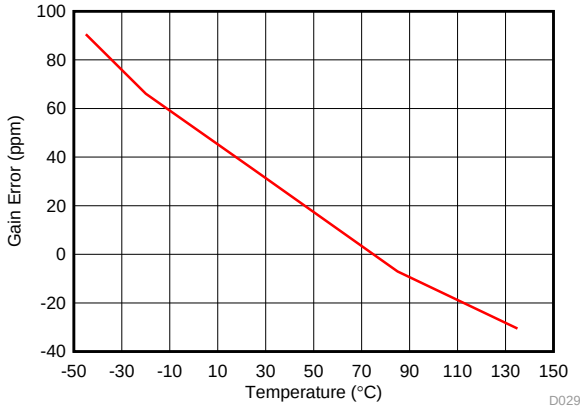
N = 293 Mean = 152 ppm Std. Dev. = 291 ppm
G = 10

図 28. Typical Distribution of Gain Error, G = 10



V_S = ±15 V

図 29. Input Bias Current vs Common-Mode Voltage



Average of 294 units G = 1

図 30. Gain Error vs Temperature, G = 1

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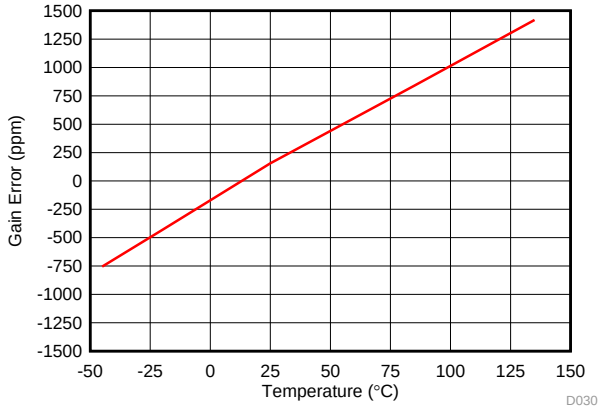
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



Average of 294 units G = 10

図 31. Gain Error vs Temperature, G = 10

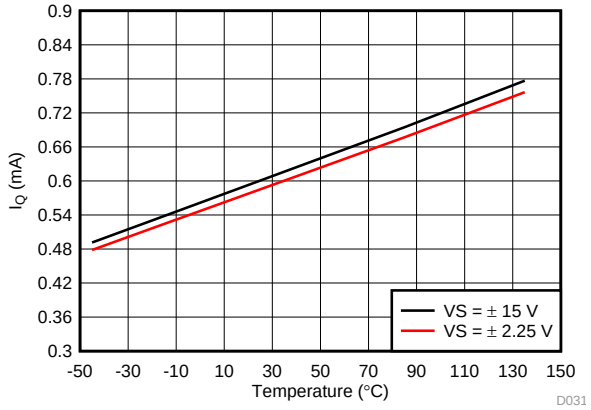
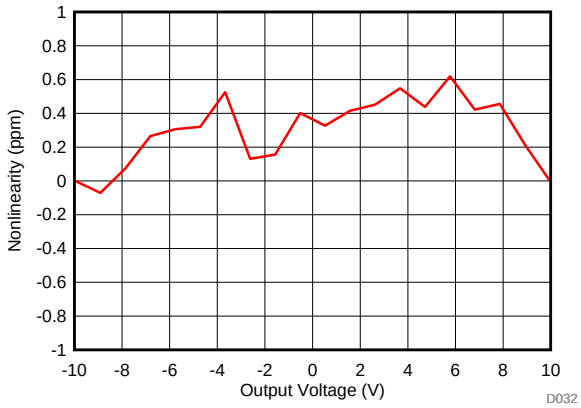
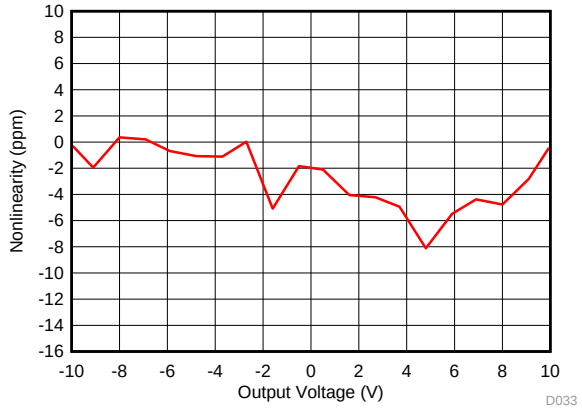


図 32. Supply Current vs Temperature



G = 1

図 33. Gain Nonlinearity, G = 1



G = 10

図 34. Gain Nonlinearity, G = 10

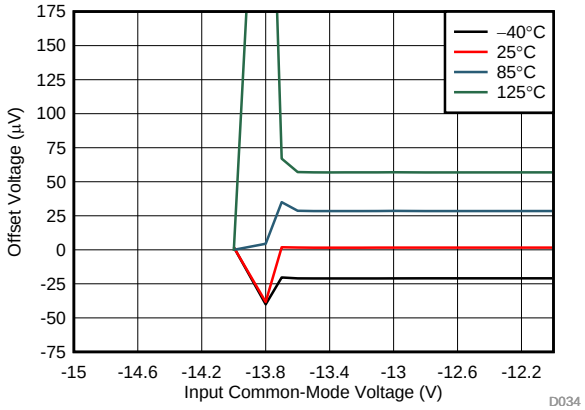


図 35. Offset Voltage vs Negative Common-Mode Voltage

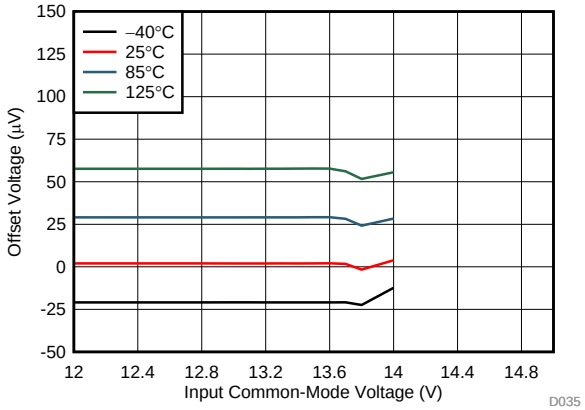


図 36. Offset Voltage vs Positive Common-Mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

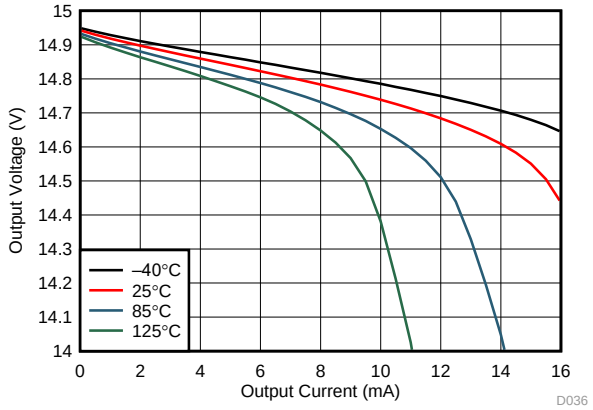


図 37. Positive Output Voltage Swing vs Output Current

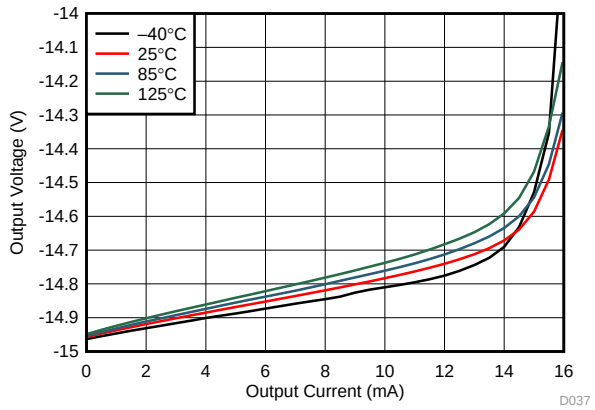


図 38. Negative Output Voltage Swing vs Output Current

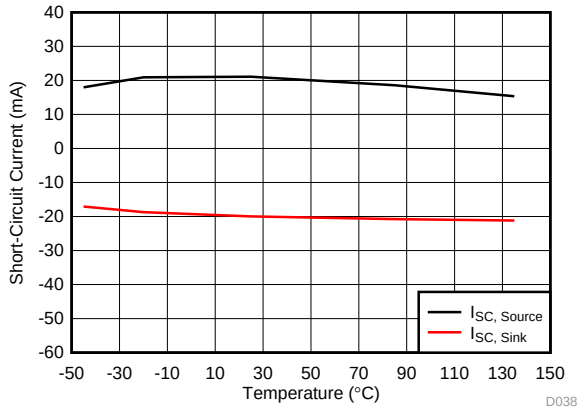


図 39. Short-Circuit Current vs Temperature

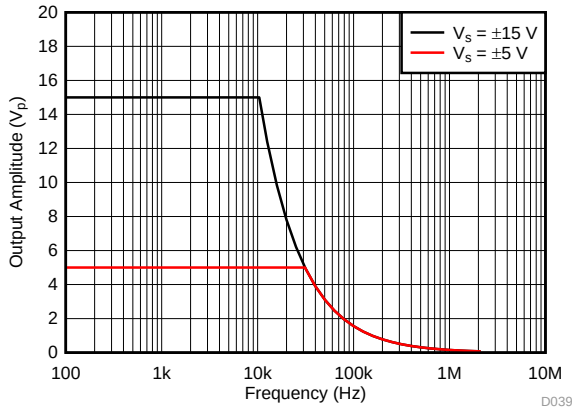
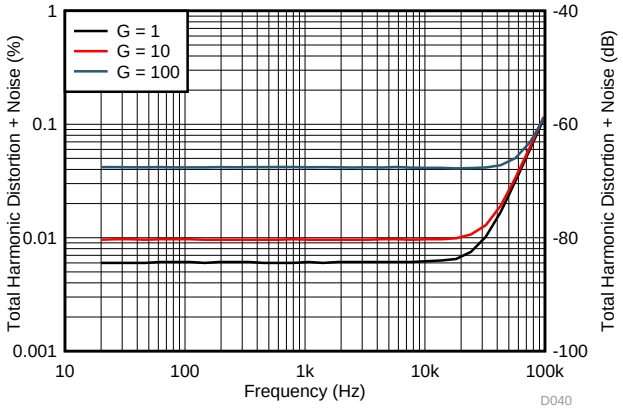


図 40. Large-Signal Frequency Response



500-kHz measurement bandwidth

1-V_{RMS} output voltage 100-kΩ load

図 41. THD+N vs Frequency

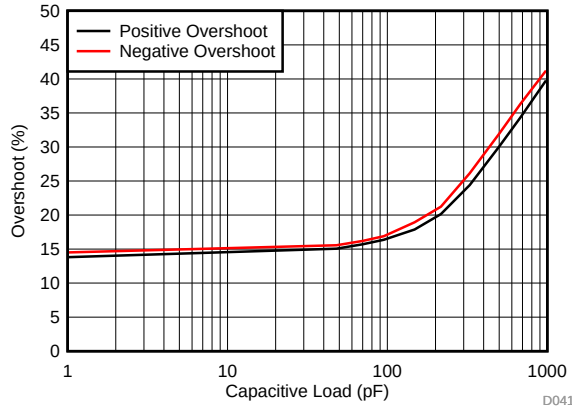


図 42. Overshoot vs Capacitive Loads

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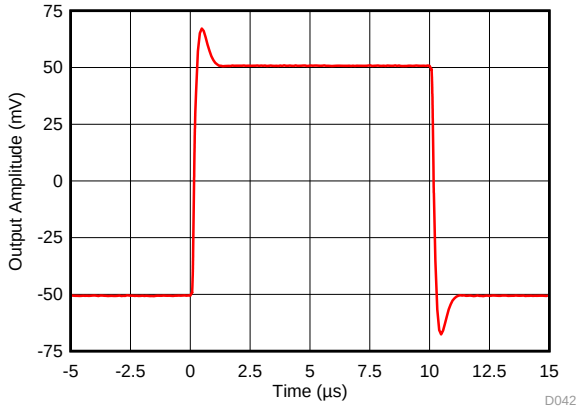
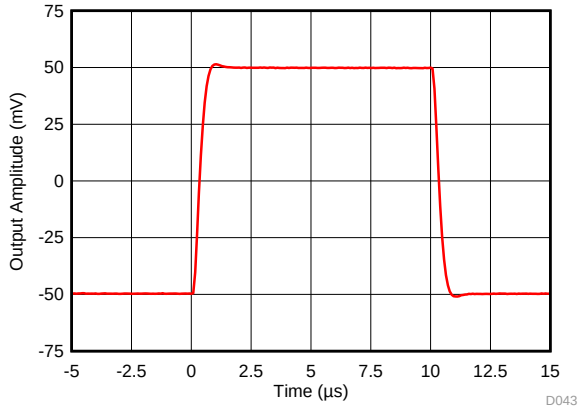
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



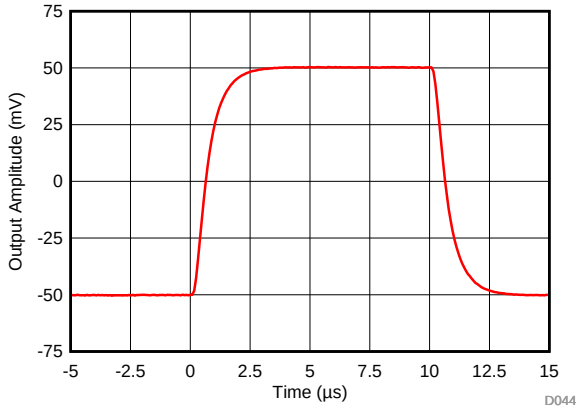
G = 1 R_L = 10 kΩ C_L = 100 pF

図 43. Small-Signal Response



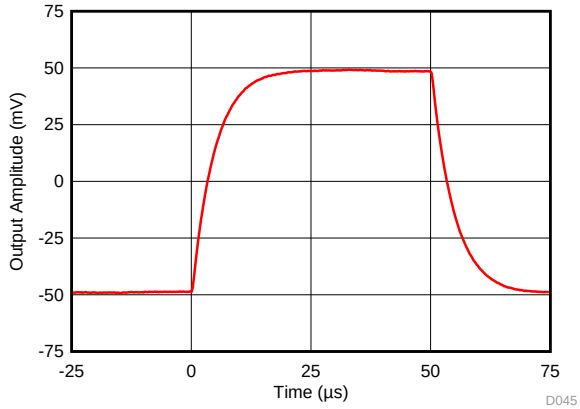
G = 10 R_L = 10 kΩ C_L = 100 pF

図 44. Small-Signal Response



G = 100 R_L = 10 kΩ C_L = 100 pF

図 45. Small-Signal Response



G = 1000 R_L = 10 kΩ C_L = 100 pF

図 46. Small-Signal Response

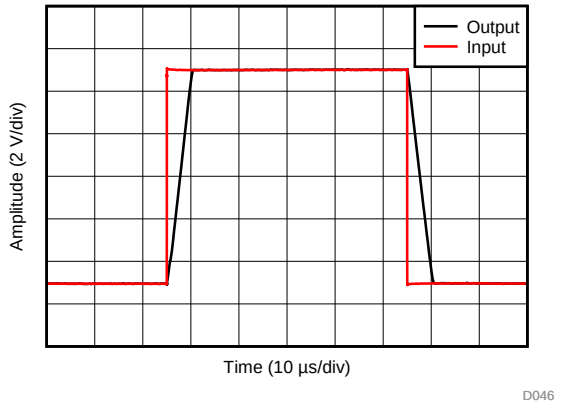


図 47. Large-Signal Step Response

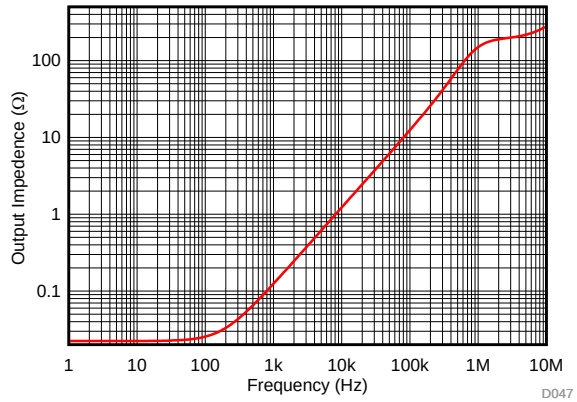


図 48. Closed-Loop Output Impedance

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

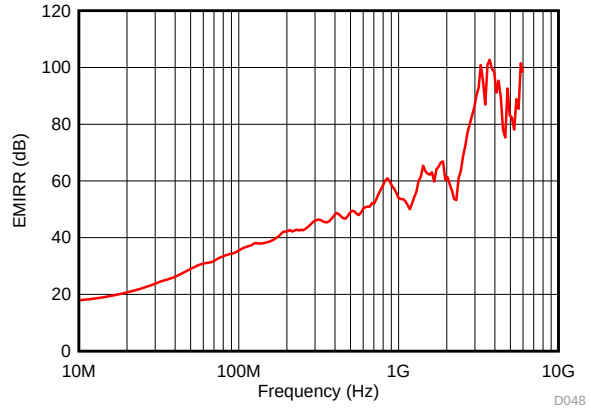


図 49. Differential-Mode EMI Rejection Ratio

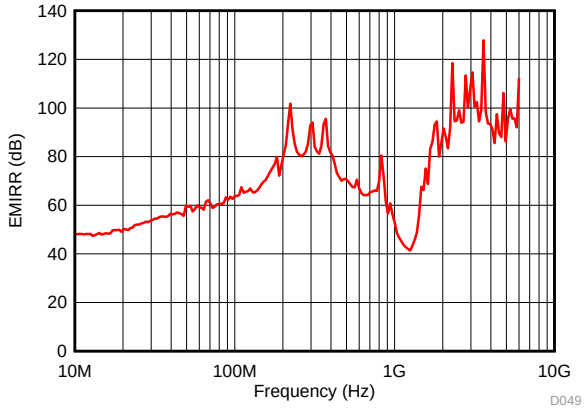
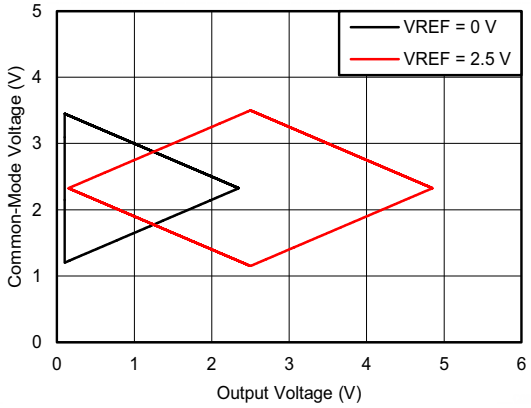
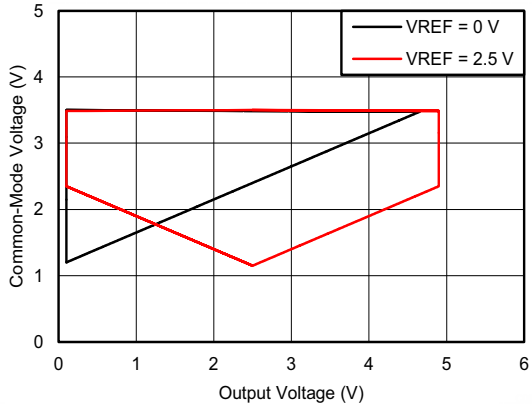


図 50. Common-Mode EMI Rejection Ratio



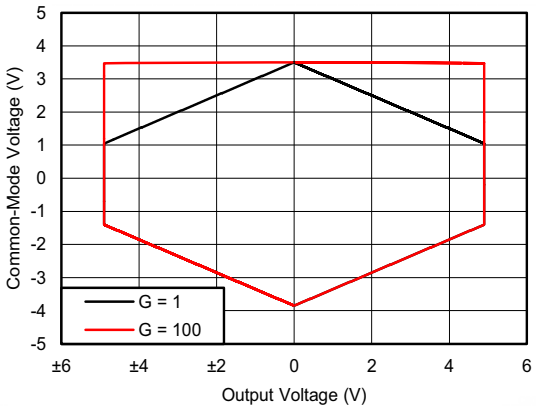
V_S = 5 V G = 1

図 51. Input Common-Mode Voltage vs Output Voltage



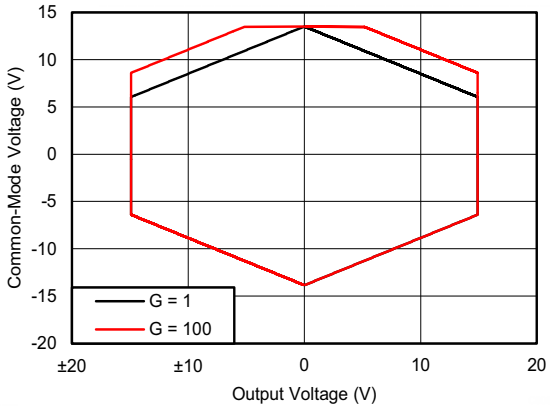
V_S = 5 V G = 100

図 52. Input Common-Mode Voltage vs Output Voltage



V_S = ±5 V V_{REF} = 0 V

図 53. Input Common-Mode Voltage vs Output Voltage



V_S = ±15 V V_{REF} = 0 V

図 54. Input Common-Mode Voltage vs Output Voltage

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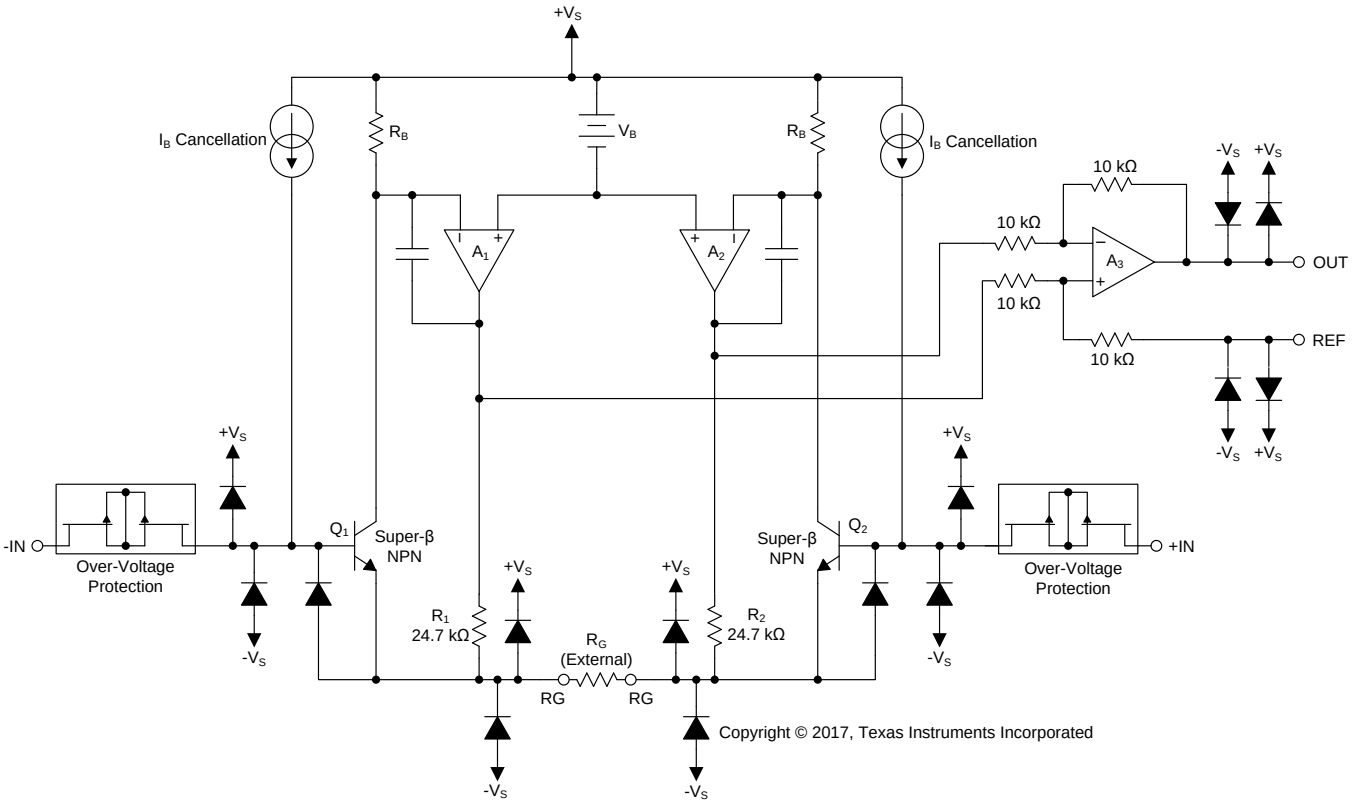
8 Detailed Description

8.1 Overview

The INA821 is a monolithic precision instrumentation amplifier that incorporates a current-feedback input stage and a four-resistor difference amplifier output stage. The functional block diagram in the next section shows how the differential input voltage is buffered by Q_1 and Q_2 and is forced across R_G, which causes a signal current to flow through R_G, R_1, and R_2. The output difference amplifier, A_3, removes the common-mode component of the input signal and refers the output signal to the REF pin. The V_{BE} and voltage drop across R_1 and R_2 produces output voltages on A_1 and A_2 that are approximately 0.8 V lower than the input voltages.

Each input is protected by two field-effect transistors (FETs) that provide a low series resistance under normal signal conditions, and preserve excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 8 mA.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Setting the Gain

図 55 shows that the gain of the INA821 is set by a single external resistor (R_G) connected between the RG pins (pins 1 and 8).

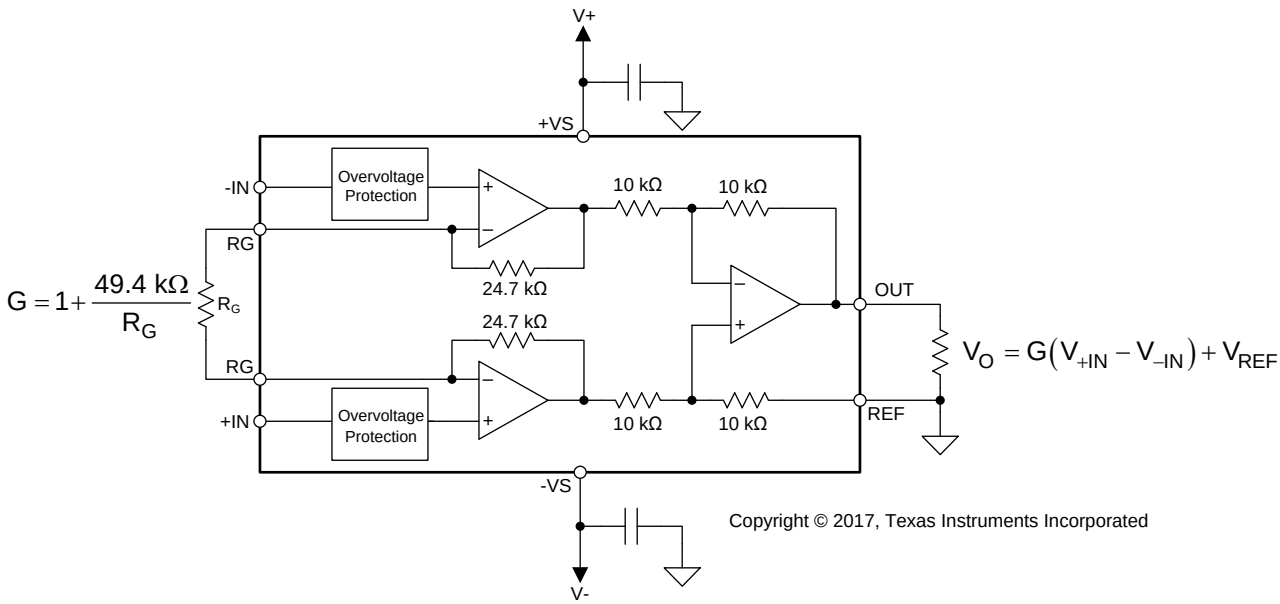


図 55. Simplified Diagram of the INA821 With Gain and Output Equations

The value of R_G is selected according to:

$$G = 1 + \frac{49.4\ k\Omega}{R_G} \tag{1}$$

表 2 lists several commonly used gains and resistor values. The 49.4-kΩ term in 式 1 is a result of the sum of the two internal 24.7-kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA821. As shown in 図 55 and explained in more details in the *Layout* section, make sure to connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, that are placed as close to the device as possible.

表 2. Commonly-Used Gains and Resistor Values

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	49.4 k	49.9 k
5	12.35 k	12.4 k
10	5.489 k	5.49 k
20	2.600 k	2.61 k
50	1.008 k	1 k
100	499	499
200	248	249
500	99	100
1000	49.4	49.9

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8.3.1.1 Gain Drift

The stability and temperature drift of the external gain setting resistor (R_G) also affects gain. The contribution of R_G to gain accuracy and drift is determined from 式 1.

The best gain drift of 5 ppm/℃ (maximum) is achieved when the INA821 uses G = 1 without R_G connected. In this case, gain drift is limited by the slight mismatch of the temperature coefficient of the integrated 10-kΩ resistors in the differential amplifier (A_3). At gains greater than 1, gain drift increases as a result of the individual drift of the 24.7-kΩ resistors in the feedback of A_1 and A_2 relative to the drift of the external gain resistor (R_G.) The low temperature coefficient of the internal feedback resistors significantly improves the overall temperature stability of applications using gains greater than 1 V/V over alternate options.

Low resistor values required for high gain make wiring resistance an important consideration. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 100 or greater. To maintain stability, avoid parasitic capacitance of more than a few picofarads at R_G connections. Careful matching of any parasitics on the R_G pins maintains optimal CMRR over frequency; see 図 17.

8.3.2 EMI Rejection

Texas Instruments developed a method to accurately measure the immunity of an amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. This method uses an EMI rejection ratio (EMIRR) to quantify the ability of the INA821 to reject EMI. The offset resulting from an input EMI signal is calculated using 式 2:

$$\Delta V_{OS} = \left(\frac{V_{RF_PEAK}^{2}}{100\ mV_P}\right) \cdot 10^{-\left(\frac{EMIRR\ (dB)}{20}\right)}$$

where

- V_{RF_PEAK} is the peak amplitude of the input EMI signal. (2)

図 56 and 図 57 show the INA821 EMIRR graph for differential and common-mode EMI rejection across this frequency range. 表 3 lists the EMIRR values for the INA821 at frequencies commonly encountered in real-world applications. Applications listed in 表 3 are centered on or operated near the particular frequency shown. Depending on the end-system requirements, additional EMI filters may be required near the signal inputs of the system. Incorporating known good practices such as using short traces, low-pass filters, and damping resistors combined with parallel and shielded signal routing may be required.

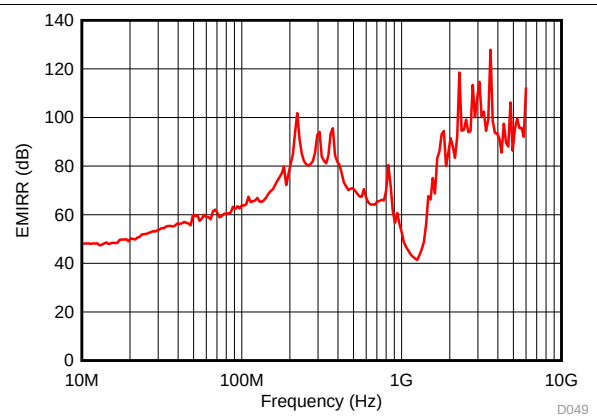


図 56. Common-Mode EMIRR Testing

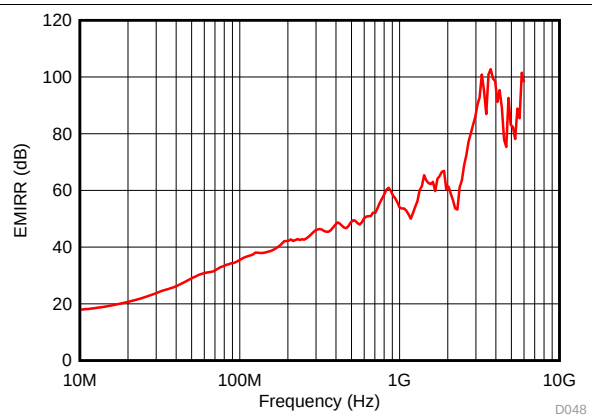


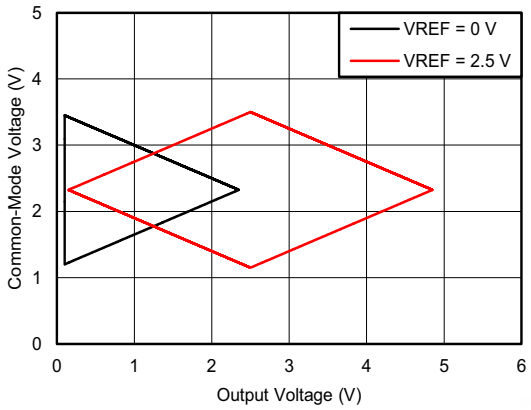
図 57. Differential Mode EMIRR Testing

表 3. INA821 EMIRR for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	DIFFERENTIAL EMIRR	COMMON-MODE EM is a result of the sum of the two IRR
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh-frequency (UHF) applications	60 dB	88 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (up to 1.6 GHz), GSM, aeronautical mobile, UHF applications	58 dB	60 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	66 dB	89 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	73 dB	98 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	99 dB	111 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	83 dB	91 dB

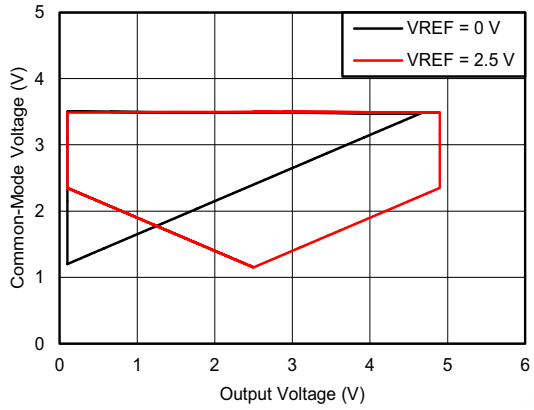
8.3.3 Input Common-Mode Range

The linear input voltage range of the INA821 input circuitry extends within 2 V of power supplies and maintains excellent common-mode rejection throughout this range. The common-mode range for the most common operating conditions are shown in 図 58 to図 61. The common-mode range for other operating conditions is best calculated using the *Common-Mode Input Range Calculator for Instrumentation Amplifiers*.



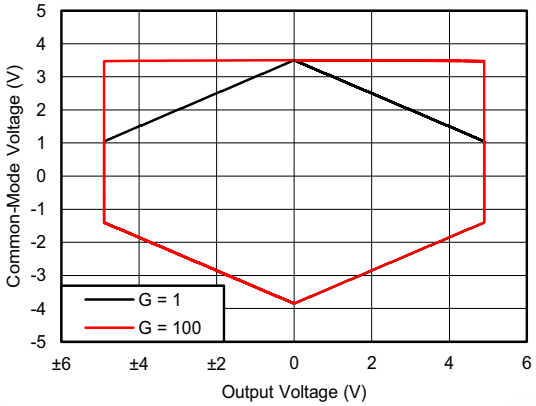
V_S = 5 V G = 1

図 58. Input Common-Mode Voltage vs Output Voltage



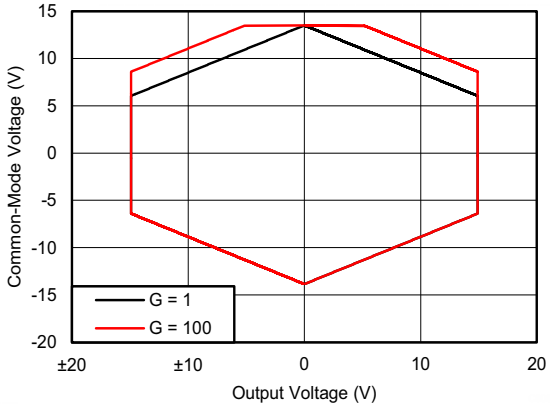
V_S = 5 V G = 100

図 59. Input Common-Mode Voltage vs Output Voltage



V_S = ±5 V V_{REF} = 0 V

図 60. Input Common-Mode Voltage vs Output Voltage



V_S = ±15 V V_{REF} = 0 V

図 61. Input Common-Mode Voltage vs Output Voltage

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8.3.4 Input Protection

The inputs of the INA821 device are individually protected for voltages up to ±40 V. For example, a condition of –40 V on one input and +40 V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 8 mA.

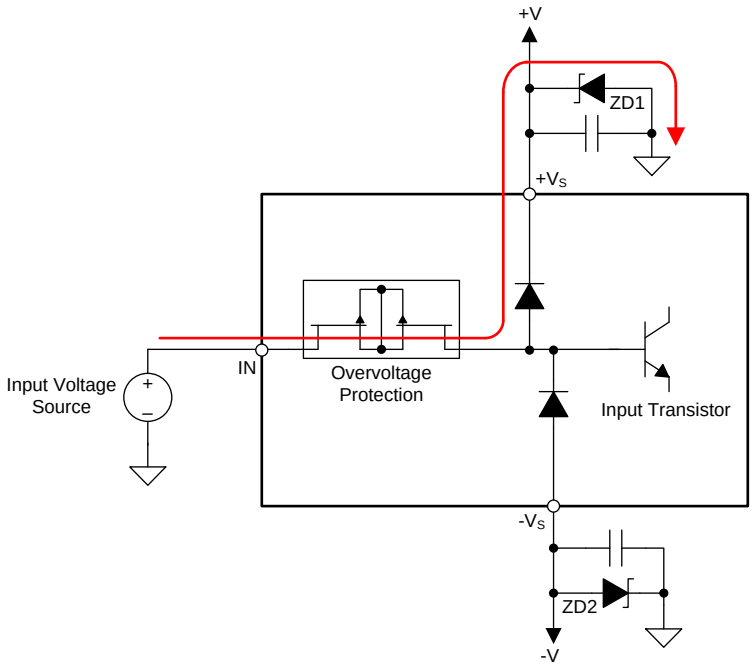

図 62. Input Current Path During an Overvoltage Condition

During an input overvoltage condition, current flows through the input protection diodes into the power supplies; see 図 62. If the power supplies are unable to sink current, then Zener diode clamps (ZD1 and ZD2 in 図 62) must be placed on the power supplies to provide a current pathway to ground. 図 63 shows the input current for input voltages from –40 V to 40 V when the INA821 is powered by ±15-V supplies.

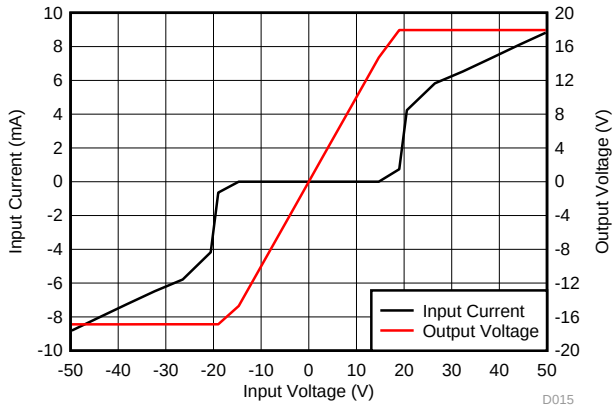

図 63. Input Current vs Input Overvoltage

8.3.5 Operating Voltage

The INA821 operates over a power-supply range of 4.5 V to 36 V (±2.25 V to ±18 V).

> **注意**
>
> Supply voltages higher than 40 V (±20 V) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section of this data sheet.

8.3.6 Error Sources

Most modern signal-conditioning systems calibrate errors at room temperature. However, calibration of errors that result from a change in temperature is normally difficult and costly. Therefore, minimize these errors by choosing high-precision components, such as the INA821, that have improved specifications in critical areas that impact the precision of the overall system. 図 64 shows an example application.

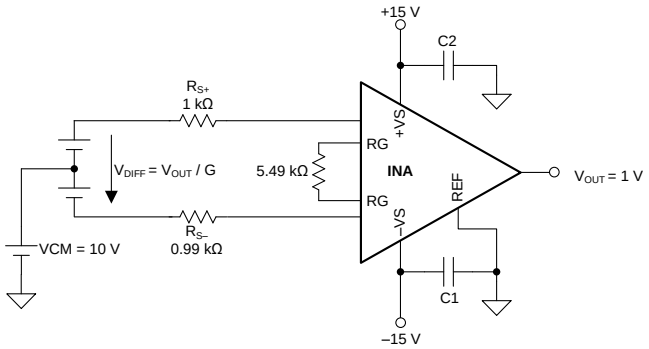

図 64. Example Application with G = 10 V/V and 1 V Output Voltage

Resistor-adjustable devices (such as the INA821) show the lowest gain error in G = 1 because of the inherently well-matched drift of the internal resistors of the differential amplifier. At gains greater than 1 (for instance, G = 10 V/V or G = 100 V/V), the gain error becomes a significant error source because of the contribution of the resistor drift of the 24.7-kΩ feedback resistors in conjunction with the external gain resistor. Except for very high gain applications, the gain drift is by far the largest error contributor compared to other drift errors, such as offset drift.

The INA821 offers excellent gain error over temperature for both G > 1 and G = 1 (no external gain resistor). 表 5 summarizes the major error sources in common INA applications and compares the three cases of G = 1 (no external resistor) and G = 10 (5.49-kΩ external resistor) and G = 100 (499-Ω external resistor). All calculations are assuming an output voltage of V_{OUT} = 1 V. Thus, the input signal V_{DIFF} (given by V_{DIFF}= V_{OUT}/G) exhibits smaller and smaller amplitudes with increasing gain G. In this example, V_{DIFF} = 1 mV at G = 1000. All calculations refer the error to the input for easy comparison and system evaluation. As 表 5 shows, errors generated by the input stage (such as input offset voltage) are more dominant at higher gain, while the effects of output stage are suppressed because they are divided by the gain when referring them back to the input. the gain error and gain drift error are much more significant for gains greater than 1 because of the contribution of the resistor drift of the 24.7-kΩ feedback resistors in conjunction with the external gain resistor. In most applications, static errors (absolute accuracy errors) can readily be removed during calibration in production, while the drift errors are the key factors limiting overall system performance.

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表 4. System Specifications for Error Calculation

QUANTITY	VALUE	UNIT
V_{OUT}	1	V
VCM	10	V
VS	1	V
R_{S+}	1000	Ω
$R_{S–}$	999	Ω
RG tolerance	0.01	%
RG drift	10	ppm/°C
Temperature range upper limit	105	°C

表 5. Error Calculation

ERROR SOURCE	ERROR CALCULATION	INA821 VALUES				
		SPECIFICATION	UNIT	G = 1 ERROR (ppm)	G = 100 ERROR (ppm)	G = 1000 ERROR (ppm)
ABSOLUTE ACCURACY AT 25°C						
Input offset voltage	V_{OSI} / V_{DIFF}	35	µV	35	350	3500
Output offset voltage	V_{OSO} / (G × V_{DIFF})	300	µV	350	350	350
Input offset current	I_{OS} × maximum (R_{S+}, $R_{S–}$) / V_{DIFF}	0.5	nA	1	5	50
CMRR (min)	V_{CM} / ($10^{CMRR/20}$ × V_{DIFF})	92 (G = 1), 112 (G = 10), 132 (G = 100)	dB	251	251	251
PSRR (min)	(V_{CC} – V_S)/ ($10^{PSRR/20}$ × V_{DIFF})	110 (G = 1), 114 (G = 10), 130 (G = 100)	dB	3	20	32
Gain error from INA (max)	GE(%) × 10^4	0.02 (G = 1), 0.15 (G = 10, 100)	%	200	1500	1500
Gain error from external resistor RG (max)	GE(%) × 10^4	0.01	%	100	100	100
Total absolute accuracy error (ppm) at 25°C, worst case	sum of all errors	—	—	940	2576	5738
Total absolute accuracy error (ppm) at 25°C, average	rms sum of all errors	—	—	487	1603	3834
DRIFT TO 105°C						
Gain drift from INA (max)	GTC × (T_A – 25)	5 (G = 1), 35 (G = 10, 100)	ppm/°C	400	2800	2800
Gain drift from external resistor RG (max)	GTC × (T_A – 25)	10	ppm/°C	800	800	800
Input offset voltage drift (max)	(V_{OSI_TC} / V_{DIFF}) × (T_A – 25)	0.4	µV/°C	32	320	3200
Output offset voltage drift	[V_{OSO_TC} / (G × V_{DIFF})] × (T_A – 25)	5	µV/°C	400	400	400
Offset current drift	I_{OS_TC} × maximum (R_{S+}, $R_{S–}$) × (T_A – 25) / V_{DIFF}	20	pA/°C	2	16	160
Total drift error to 105°C (ppm), worst case	sum of all errors	—	—	1634	4336	7360
Total drift error to 105°C (ppm), typical	rms sum of all errors	—	—	980	2957	4348
RESOLUTION						
Gain nonlinearity		10 (G = 1, 10), 15 (G = 100)	ppm of FS	10	10	15
Voltage noise (at 1 kHz)	$\sqrt{BW} \times \sqrt{\left(e_{NI}^2 + \left[\frac{e_{NO}}{G}\right]^2\right)} \times \frac{6}{V_{DIFF}}$	e_{NI} = 7, e_{NO} = 65	μV_{PP}	1335	886	3566
Current noise (at 1kHz)	I_N × maximum (R_{S+}, $R_{S–}$) × $\sqrt{BW}$ / V_{DIFF}	0.13	pA/$\sqrt{Hz}$	0.4	2	11
Total resolution error (ppm), worst case	sum of all errors	—	—	1345	896	3581
Total resolution error (ppm), typical	rms sum of all errors	—	—	1335	886	3566
TOTAL ERROR						
Total error (ppm), worst case	sum of all errors	—	—	3919	7808	16724
Total error (ppm), typical	rms sum of all errors	—	—	1726	3478	6806

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8.4 Device Functional Modes

The INA821 has a single functional mode and is operational when the power supply voltage is greater than 4.5 V (±2.25 V). The maximum power-supply voltage for the INA821 is 36 V (±18 V).

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Reference Pin

The output voltage of the INA821 is developed with respect to the voltage on the reference pin (REF.) Often, in dual-supply operation, REF (pin 6) connects to the low-impedance system ground. In single-supply operation, offsetting the output signal to a precise midsupply level is useful (for example, 2.5 V in a 5-V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level-shift the output so that the INA821 drives a single-supply analog-to-digital converter (ADC).

The voltage source applied to the reference pin must have a low output impedance. As shown in 図 65, any resistance at the reference pin (R_{REF} in 図 65) is in series with one of the internal 10-kΩ resistors.

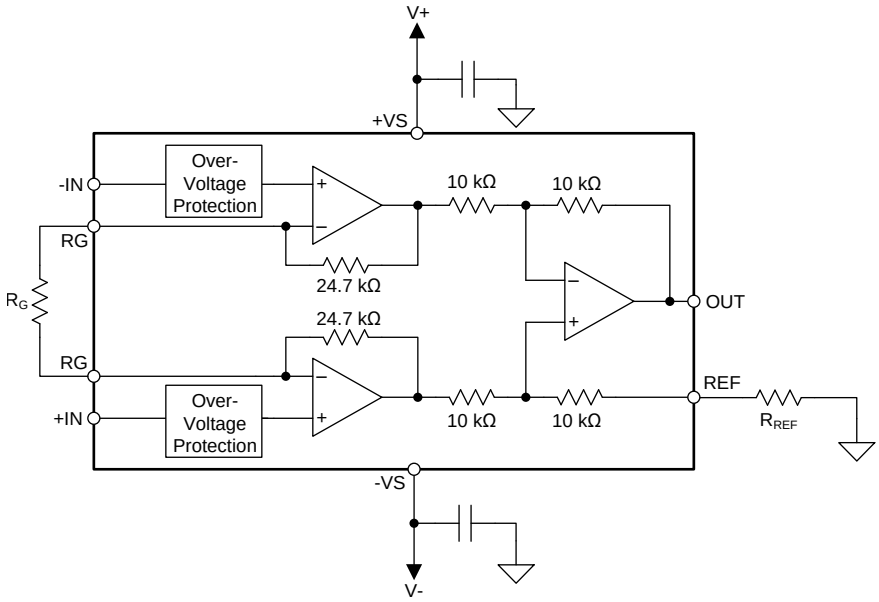

図 65. Parasitic Resistance Shown at the Reference Pin

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Application Information (continued)

The parasitic resistance at the reference pin (R_{REF}) creates an imbalance in the four resistors of the internal difference amplifier that results in a degraded common-mode rejection ratio (CMRR). 図 66 shows the degradation in CMRR of the INA821 as a result of the increased resistance at the reference pin. For the best performance, keep the source impedance to the REF pin (R_{REF}) less than 5 Ω.

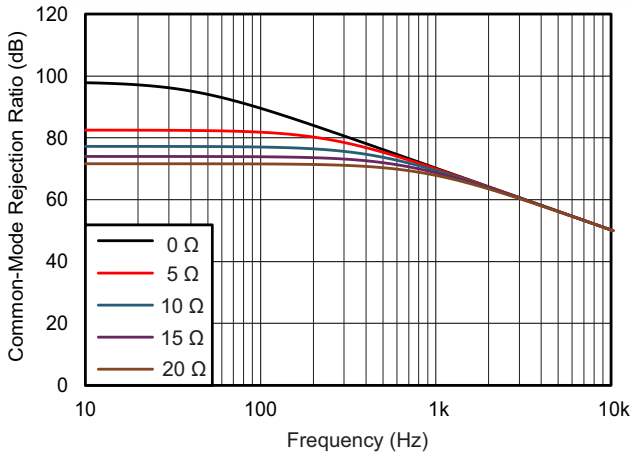

図 66. The Effect of Increasing Resistance at the Reference Pin

Voltage reference devices are an excellent option for providing a low-impedance voltage source for the reference pin. However, if a resistor voltage divider generates a reference voltage, the divider must be buffered by an op amp, as 図 67 shows, to avoid CMRR degradation.

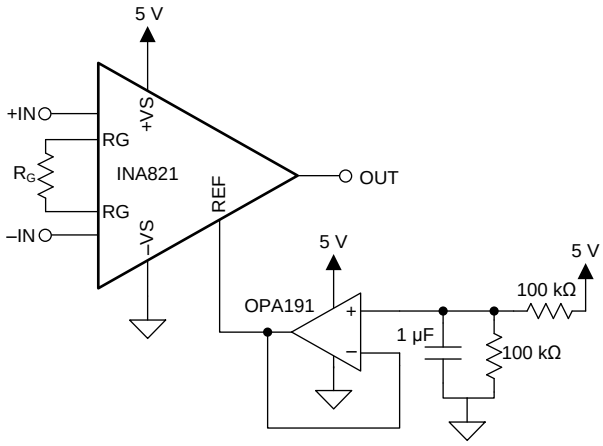

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図 67. Using an Op Amp to Buffer Reference Voltages

Application Information (continued)

9.1.2 Input Bias Current Return Path

The input impedance of the INA821 is extremely high (approximately 100 GΩ.) However, a path must be provided for the input bias current of both inputs. This input bias current is typically 150 pA. High input impedance means that this input bias current changes little with varying input voltage.

For proper operation, Input circuitry must provide a path for this input bias current. 図 68 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA821 and the input amplifiers saturate. If the differential source resistance is low, the bias current return path connects to one input (as shown in the thermocouple example in 図 68). With a higher source impedance, using two equal resistors provides a balanced input with possible advantages of a lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

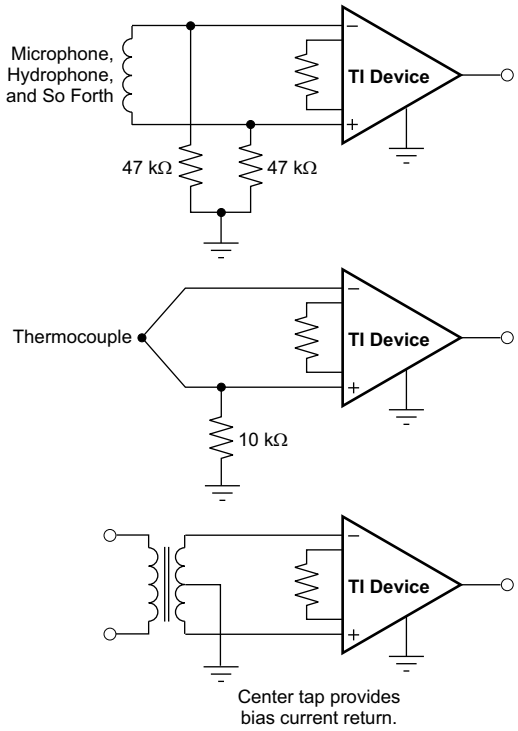

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図 68. Providing an Input Common-Mode Current Path

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9.2 Typical Application

図 69 shows a three-pin programmable-logic controller (PLC) design for the INA821. This PLC reference design accepts inputs of ±10 V or ±20 mA. The output is a single-ended voltage of 2.5 V ±2.3 V (or 200 mV to 4.8 V). Typically, PLCs have these input and output ranges.

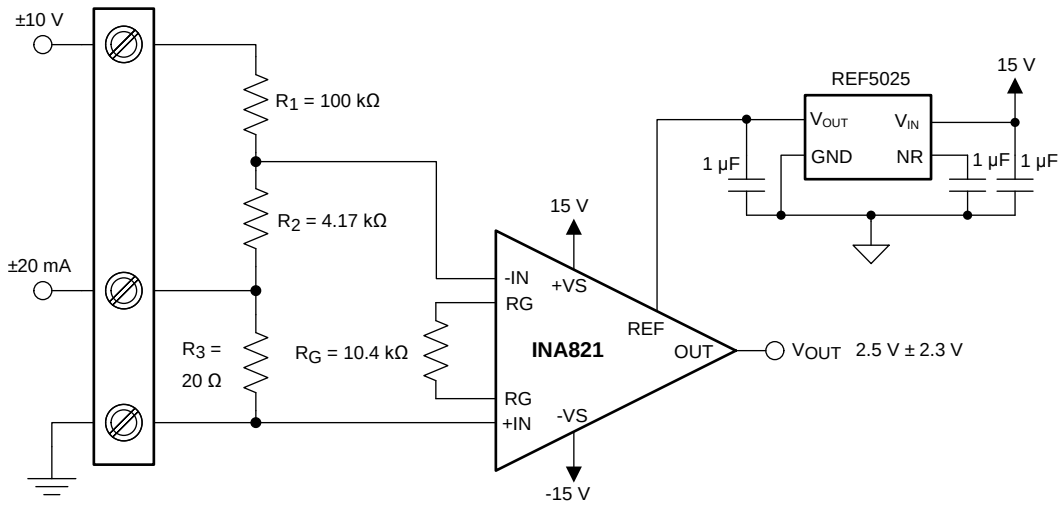

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図 69. PLC Input (±10 V, 4 mA to 20 mA)

9.2.1 Design Requirements

For this application, the design requirements are as follows:

- 4-mA to 20-mA input with less than 20-Ω burden
- ±20-mA input with less than 20-Ω burden
- ±10-V input with impedance of approximately 100 kΩ
- Maximum 4-mA to 20-mA or ±20 mA burden voltage equal to ±0.4 V
- Output range within 0 V to 5 V

9.2.2 Detailed Design Procedure

There are two modes of operation for the circuit shown in 図 69: current input and voltage input. This design requires $R_1 >> R_2 >> R_3$. Given this relationship, 式 3 calculates the current input mode transfer function.

$$V_{OUT-I} = V_D \times G + V_{REF} = -(I_{IN} \times R_3) \times G + V_{REF}$$

where

- G represents the gain of the instrumentation amplifier.
- V_D represents the differential voltage at the INA821 inputs.
- V_{REF} is the voltage at the INA821 REF pin.
- I_{IN} is the input current. (3)

式 4 shows the transfer function for the voltage input mode.

$$V_{OUT-V} = V_D \times G + V_{REF} = -\left(V_{IN} \times \frac{R_2}{R_1 + R_2}\right) \times G + V_{REF}$$

where

- V_{IN} is the input voltage (4)

Typical Application (continued)

R_1 sets the input impedance of the voltage input mode. The minimum typical input impedance is 100 kΩ. The R_1 value is 100 kΩ because increasing the R_1 value also increases noise. The value of R_3 must be extremely small compared to R_1 and R_2. The value of R_3 is 20 Ω because that resistance value is smaller than R_1 and yields an input voltage of ±400 mV when operating in current mode (±20 mA).

Use 式 5 to calculate R_2 if V_D = ±400 mV, V_{IN} = ±10 V, and R_1 = 100 kΩ.

$$V_D = V_{IN} \times \frac{R_2}{R_1 + R_2} \rightarrow R_2 = \frac{R_1 \times V_D}{V_{IN} - V_D} = 4.167\ k\Omega \tag{5}$$

The value obtained from 式 5 is not a standard 0.1% value, so 4.17 kΩ is selected. R_1 and R_2 use 0.1% tolerance resistors to minimize error.

Use 式 6 to calculate the gain of the instrumentation amplifier.

$$G = \frac{V_{OUT} - V_{REF}}{V_D} = \frac{4.8\ V - 2.5\ V}{400\ mV} = 5.75\ \frac{V}{V} \tag{6}$$

式 7 calculates the gain-setting resistor value using the INA821 gain equation (式 1).

$$R_G = \frac{49.4\ k\Omega}{G - 1} = \frac{49.4\ k\Omega}{5.75 - 1} = 10.4\ k\Omega \tag{7}$$

Use a standard 0.1% resistor value of 10.5 kΩ for this design.

9.2.3 Application Curves

図 70 and 図 71 show typical characteristic curves for the circuit in 図 69.

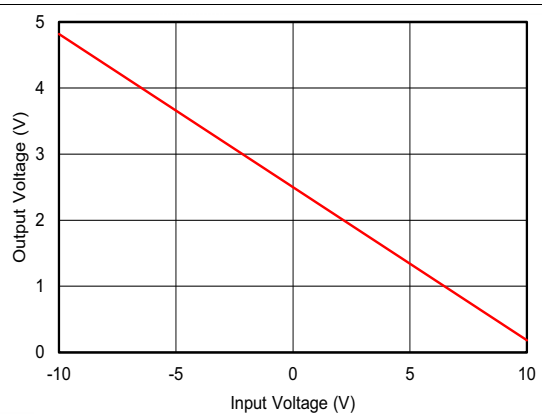

図 70. PLC Output Voltage vs Input Voltage

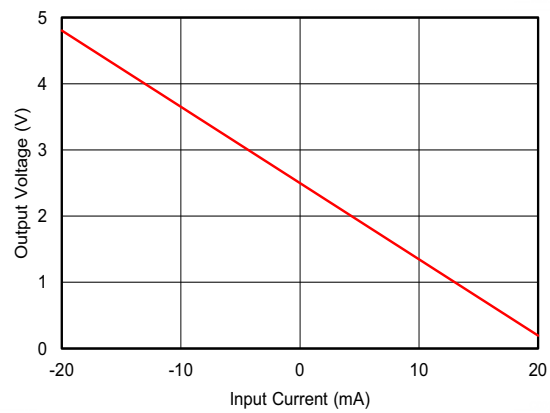

図 71. PLC Output Voltage vs Input Current

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9.3 Other Application Examples

9.3.1 Resistance Temperature Detector Interface

図 72 illustrates a 3-wire interface circuit for resistance temperature detectors (RTDs). The circuit incorporates analog linearization and has an output voltage range from 0 V to 5 V. The linearization technique employed is described in *Analog linearization of resistance temperature detectors* analog application journal. Series and parallel combinations of standard 1% resistor values are used to achieve less than 0.02°C of error over a 200°C temperature span.

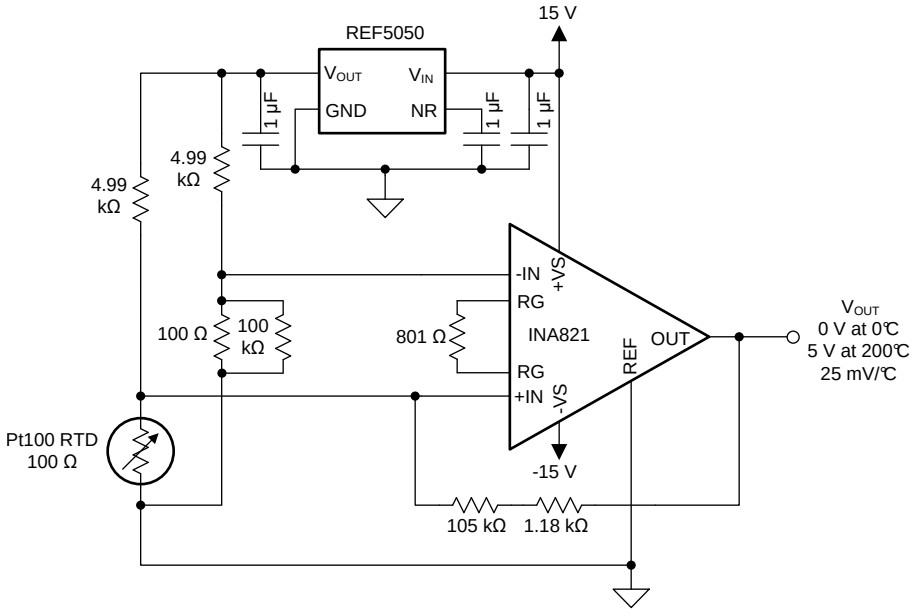

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図 72. A 3-Wire Interface for RTDs With Analog Linearization

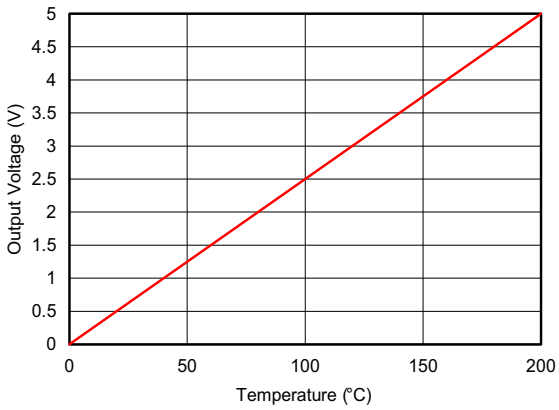

図 73. Transfer Function of 3-Wire RTD Interface

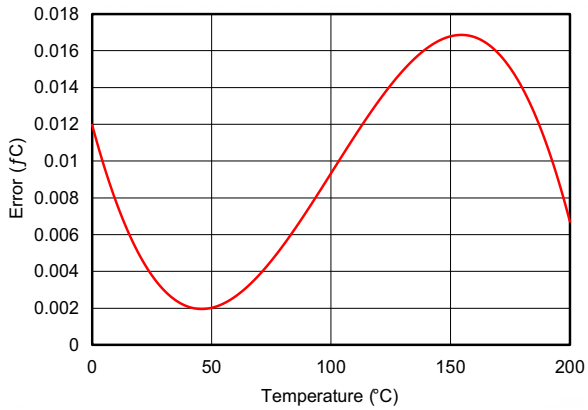

図 74. Temperature Error Over Full Temperature Range

10 Power Supply Recommendations

The nominal performance of the INA821 is specified with a supply voltage of ±15 V and midsupply reference voltage. The device also operates using power supplies from ±2.25 V (4.5 V) to ±18 V (36 V) and non-midsupply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are shown in the *Typical Characteristics* section.

11 Layout

11.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- Take care to make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. Even slight mismatch in parasitic capacitance at the gain setting pins can degrade CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of R_G, select the component so that the switch capacitance is as small as possible and most importantly so that capacitance mismatch between the RG pins is minimized.
- Noise propagates into analog circuitry through the power pins of the circuit as a whole and of the device. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 図 75, keep R_G close to the pins to minimize parasitic capacitance.
- Keep the traces as short as possible.

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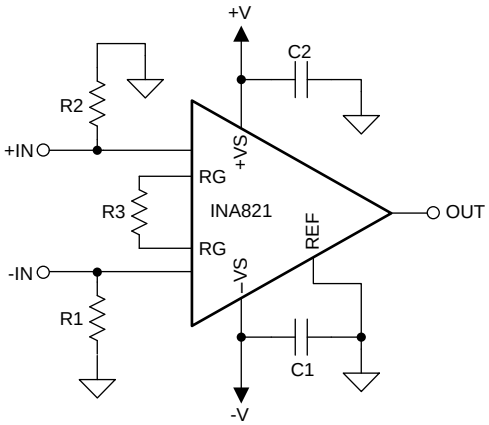
11.2 Layout Example



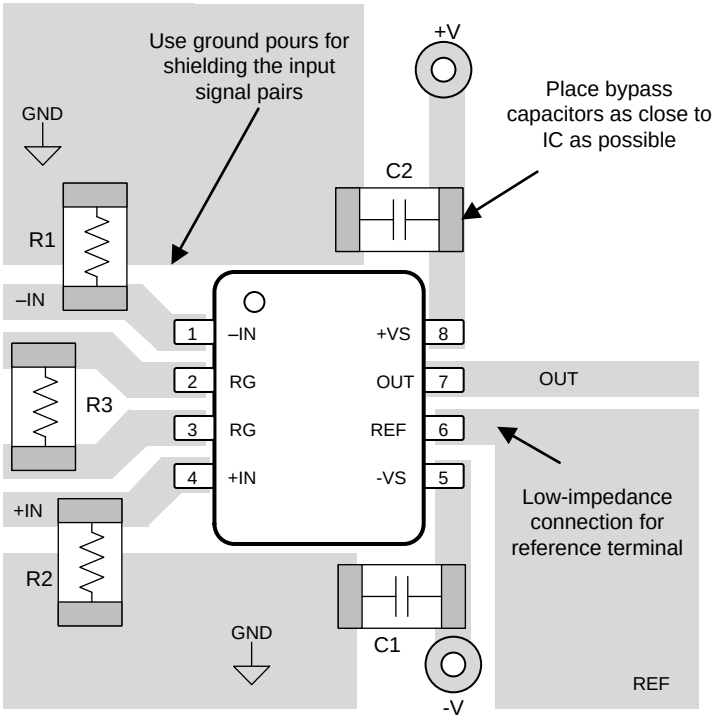


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図 75. Example Schematic and Associated PCB Layout

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

- *SPICE ベースのアナログ・シミュレーション・プログラム - TINA-TI ソフトウェア・フォルダ*
- *計装アンプの入力同相範囲を計算*

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『Comprehensive Error Calculation for Instrumentation Amplifiers』アプリケーション・ノート* (英語)
- テキサス・インスツルメンツ、*『REF50xx 低ノイズ、超低ドリフト、高精度基準電圧』データシート*
- テキサス・インスツルメンツ、*『OPAx191　36V、低消費電力、高精度、CMOS、レール・ツー・レール入力/出力、低オフセット電圧、低入力バイアス電流オペアンプ』データシート*

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA821ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA821
INA821ID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA821
INA821IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1X4Q
INA821IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1X4Q
INA821IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1X4Q
INA821IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1X4Q
INA821IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA821
INA821IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA821
INA821IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA821
INA821IDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA821
INA821IDRGR	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	INA821
INA821IDRGR.B	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	INA821
INA821IDRGT	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	INA821
INA821IDRGT.B	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	INA821

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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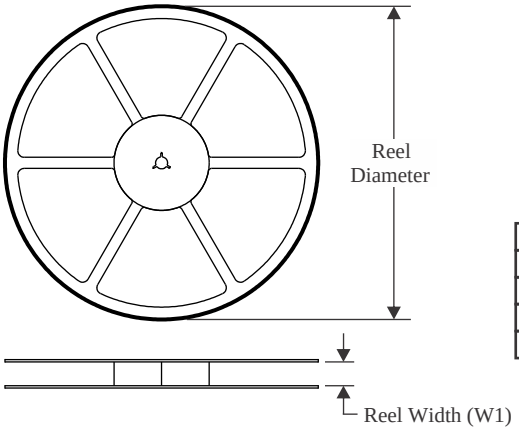
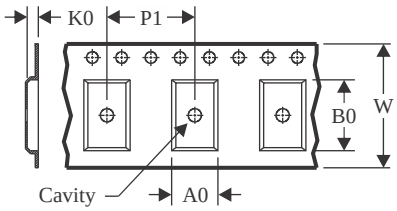
TAPE AND REEL INFORMATION

REEL DIMENSIONS

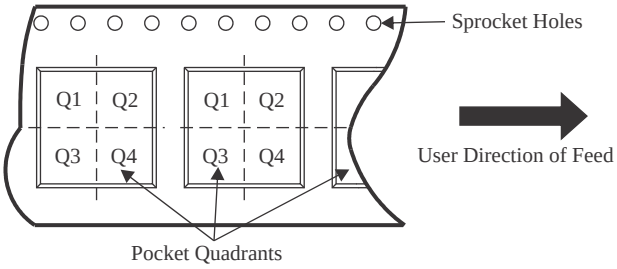


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

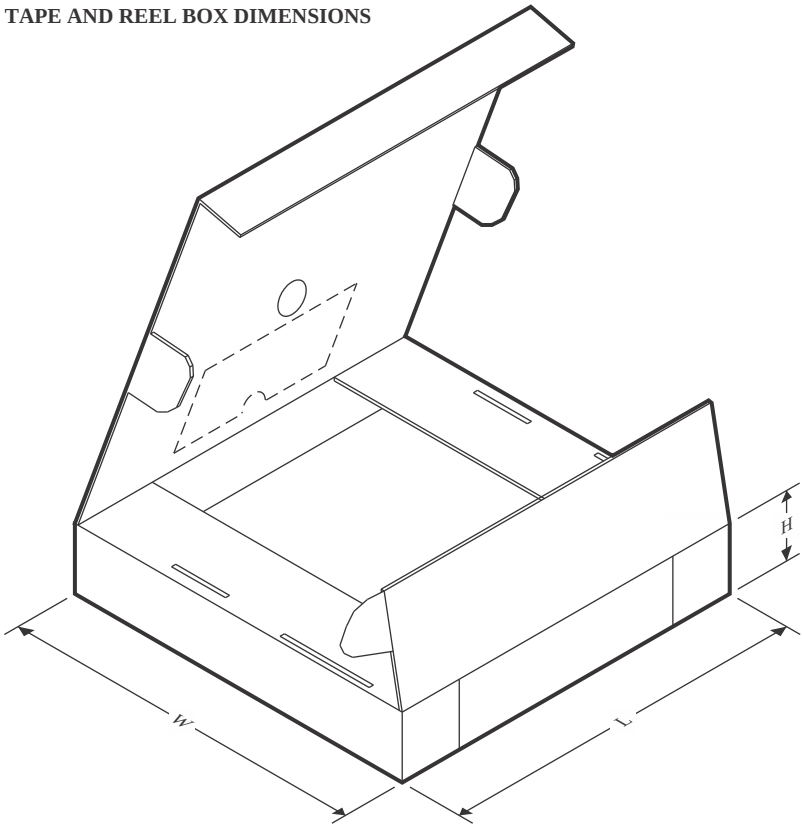
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA821IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
INA821IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
INA821IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA821IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA821IDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
INA821IDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

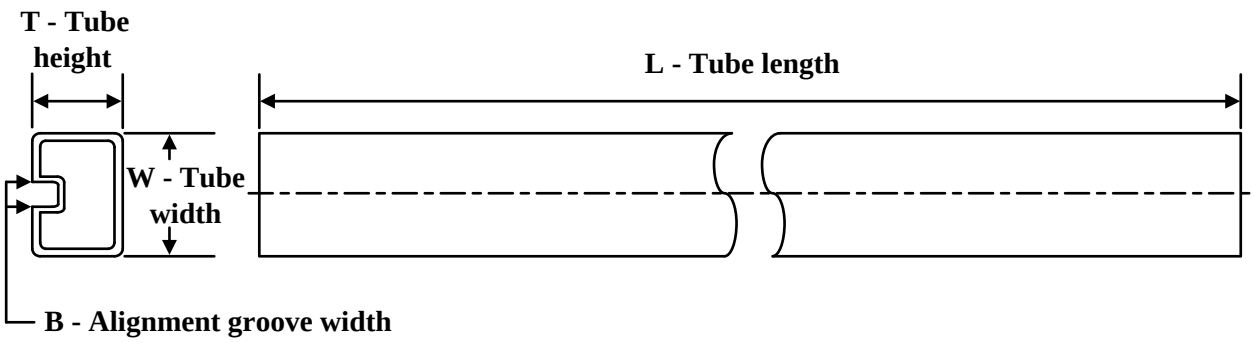
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA821IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA821IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
INA821IDR	SOIC	D	8	2500	353.0	353.0	32.0
INA821IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
INA821IDRGR	SON	DRG	8	3000	367.0	367.0	35.0
INA821IDRGT	SON	DRG	8	250	210.0	185.0	35.0

TUBE

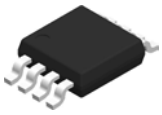


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA821ID	D	SOIC	8	75	506.6	8	3940	4.32
INA821ID.B	D	SOIC	8	75	506.6	8	3940	4.32

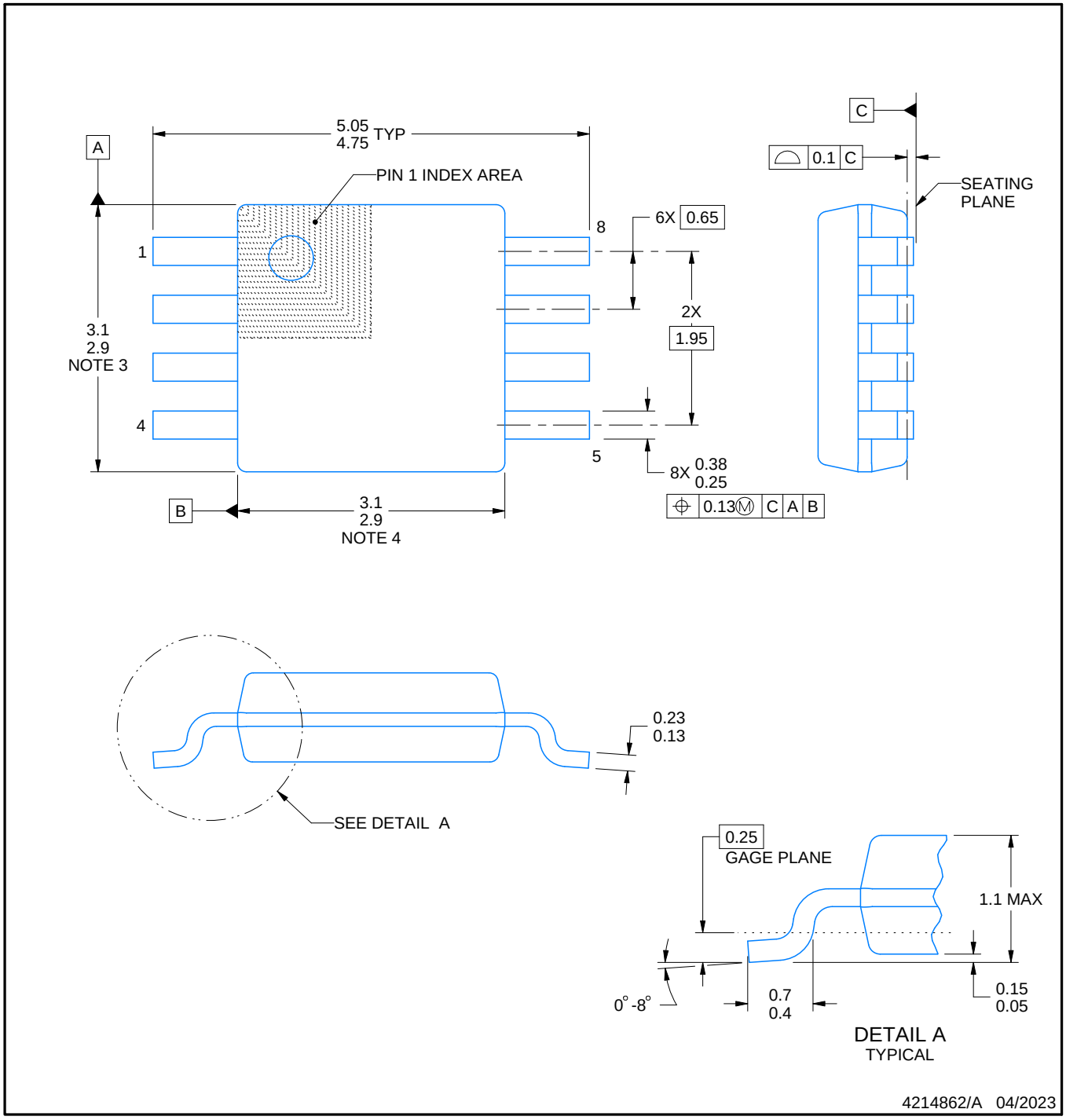
PACKAGE OUTLINE

DGK0008A



VSSOP - 1.1 mm max height

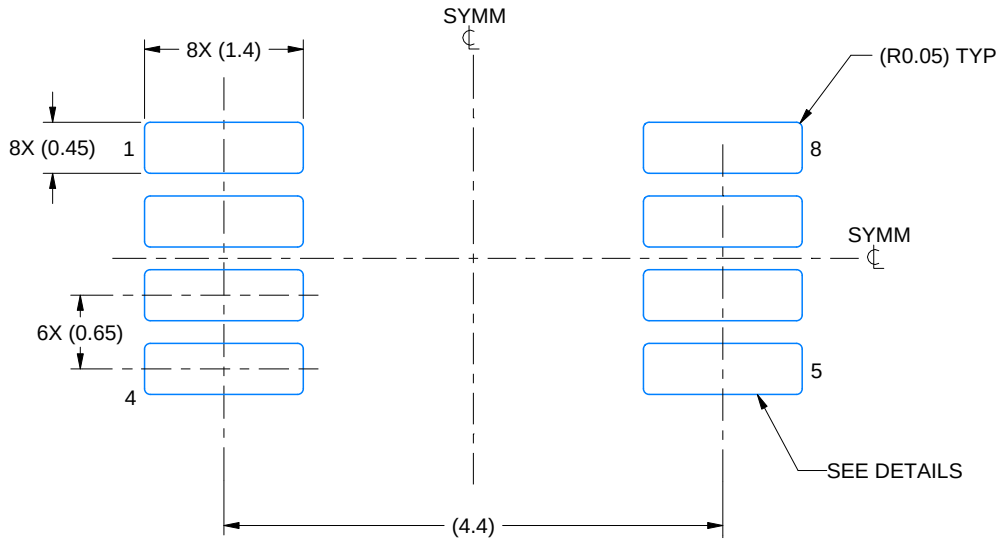
SMALL OUTLINE PACKAGE



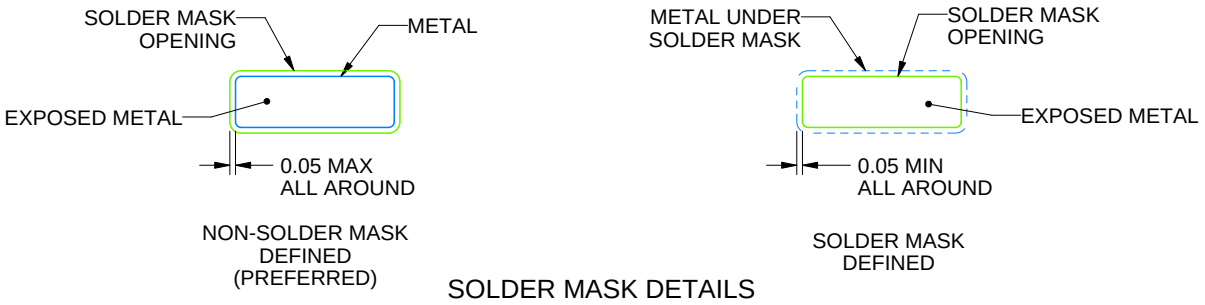
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

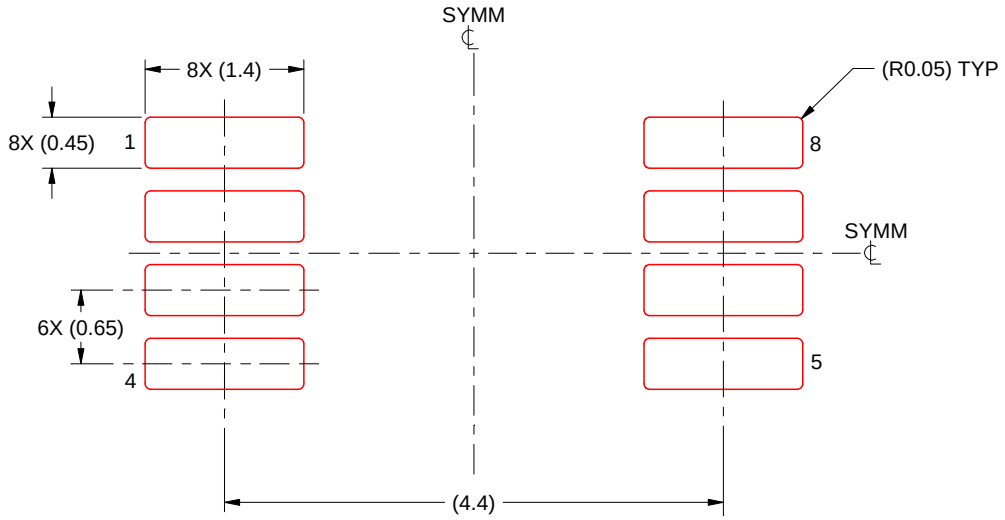


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

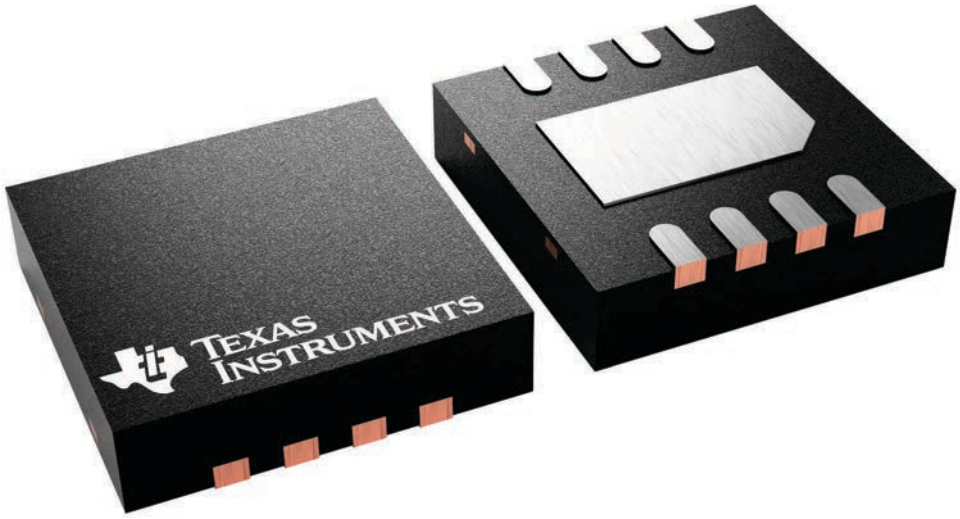
DRG 8

WSON - 0.8 mm max height

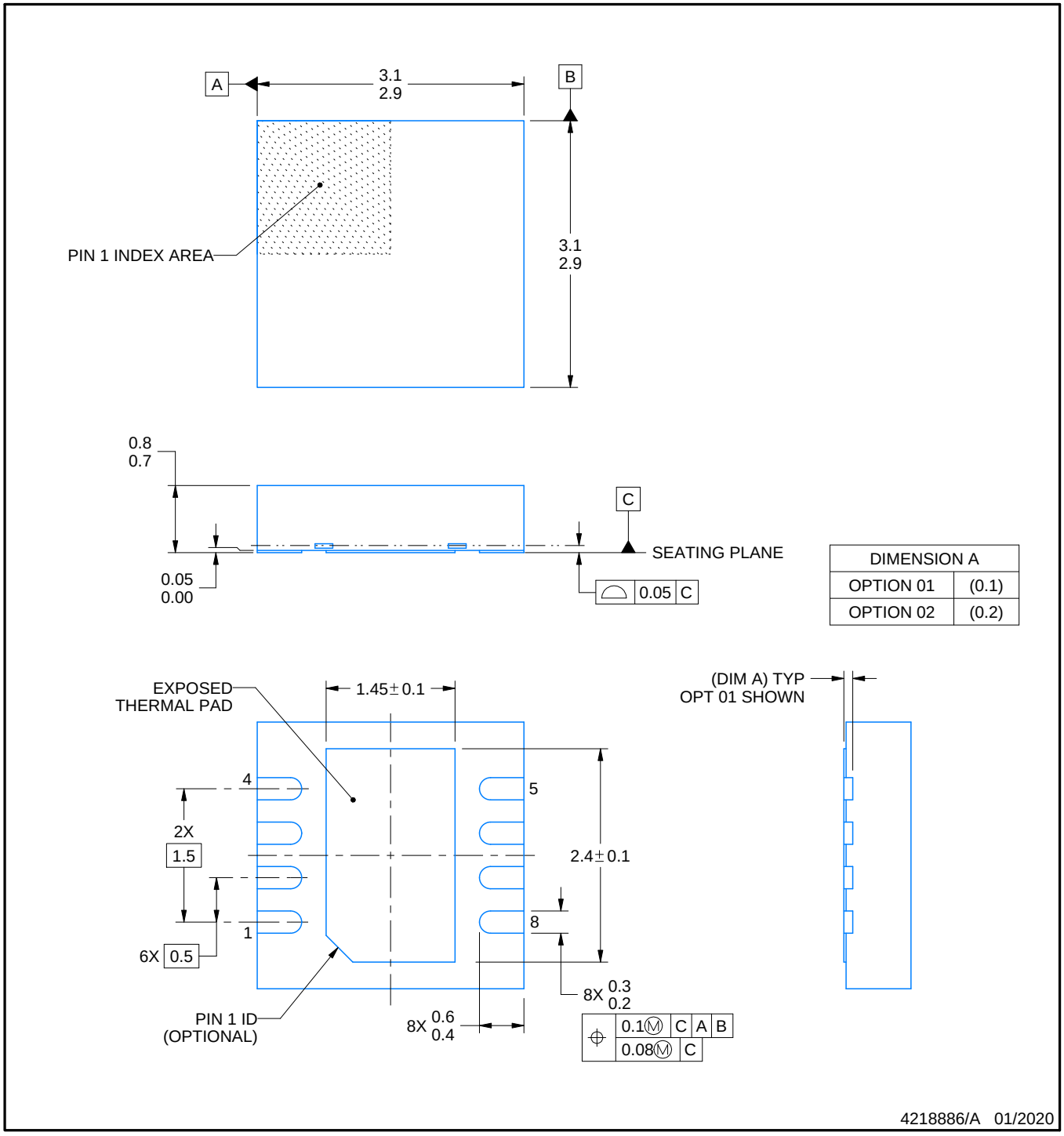
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



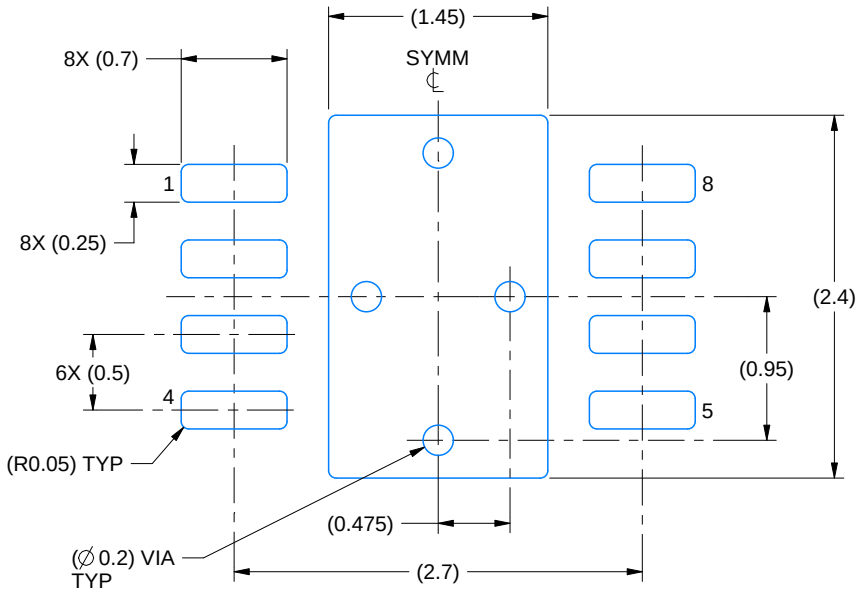
4225794/A



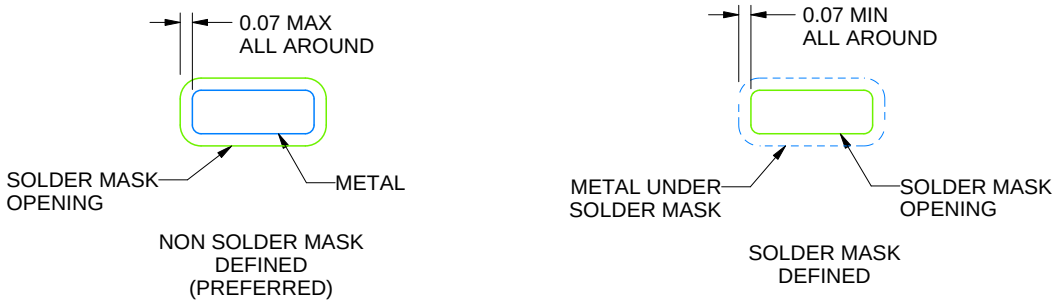
DIMENSION A	
OPTION 01	(0.1)
OPTION 02	(0.2)

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

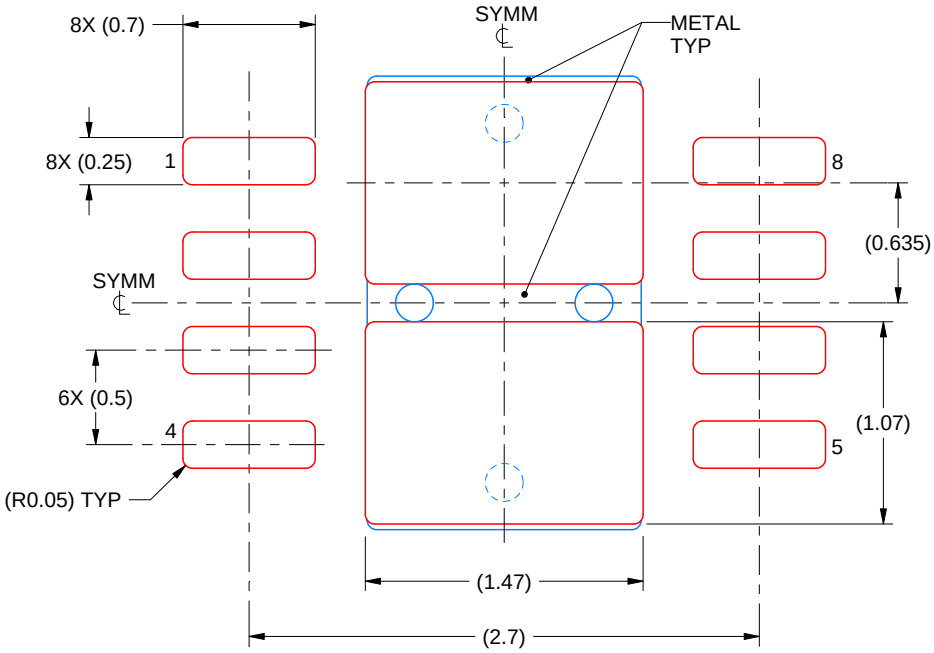


SOLDER MASK DETAILS

4218886/A 01/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



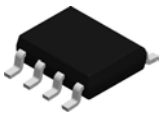
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218886/A 01/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

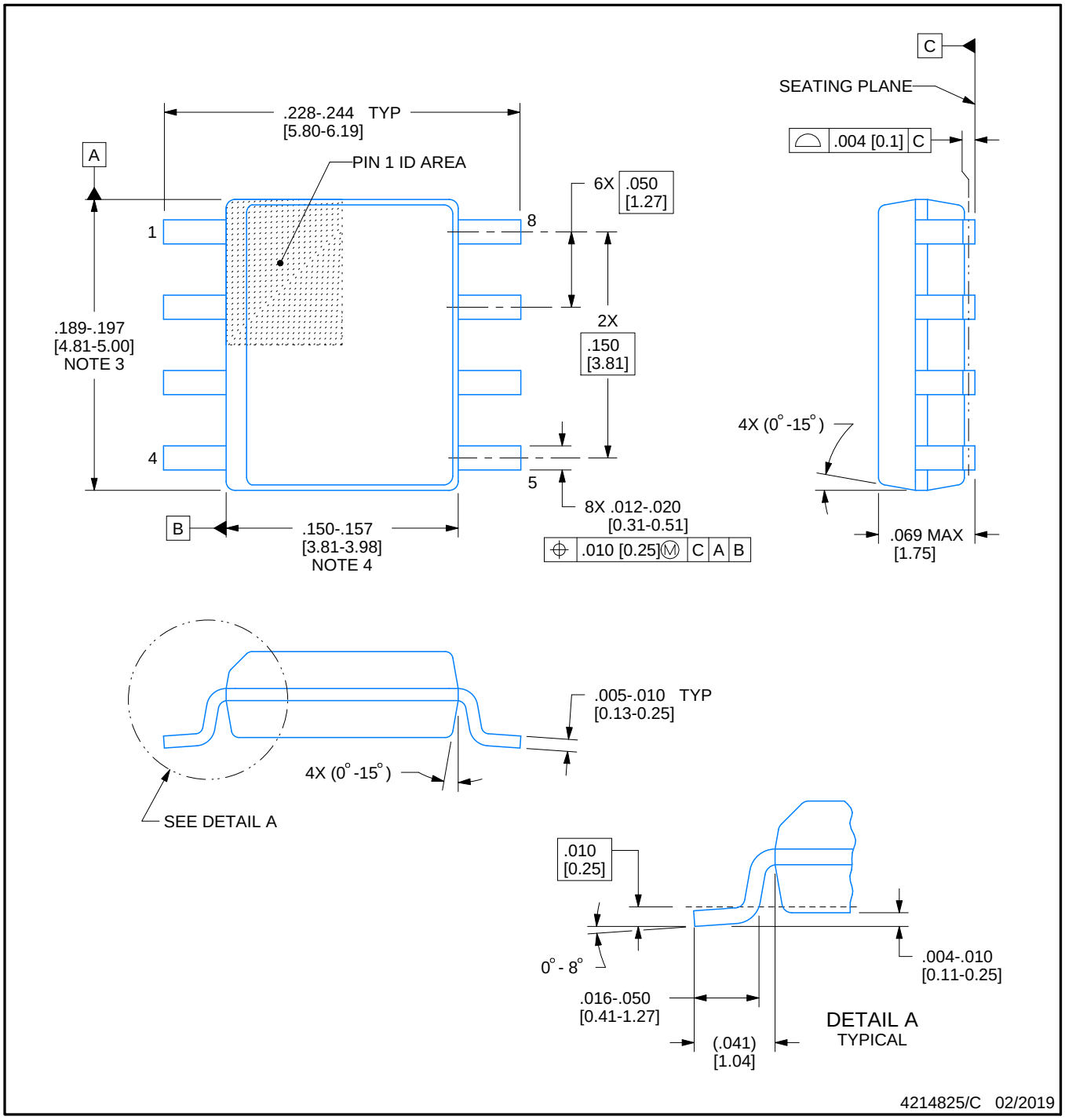


PACKAGE OUTLINE

D0008A

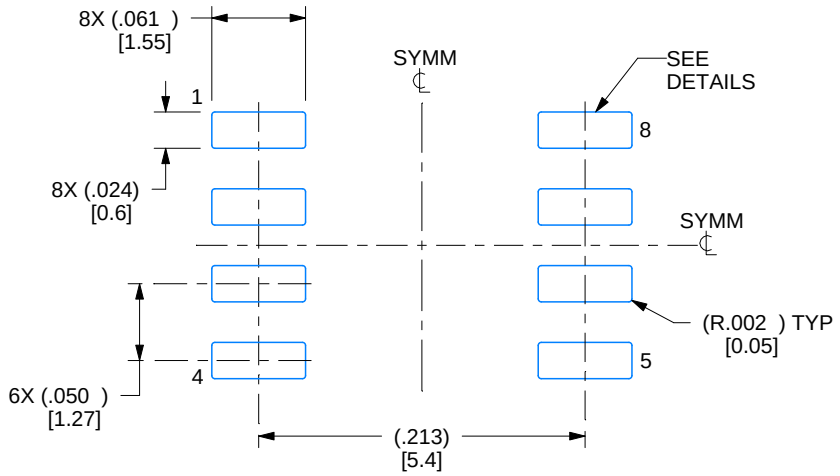
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

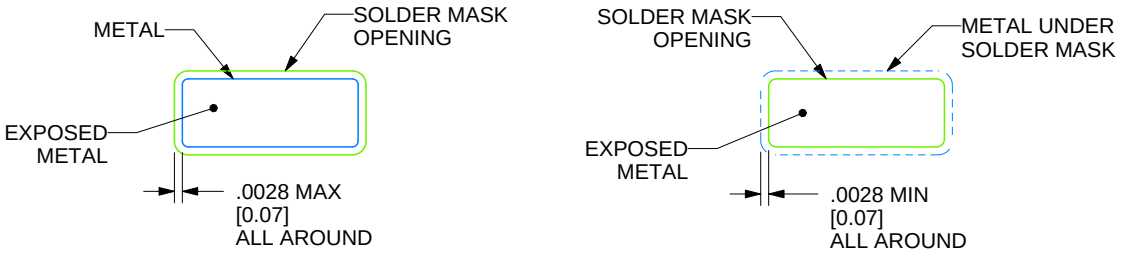


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

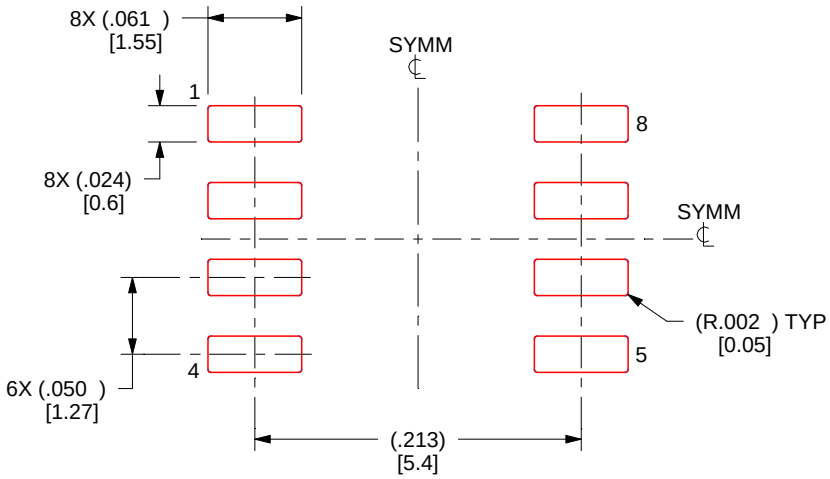


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月