

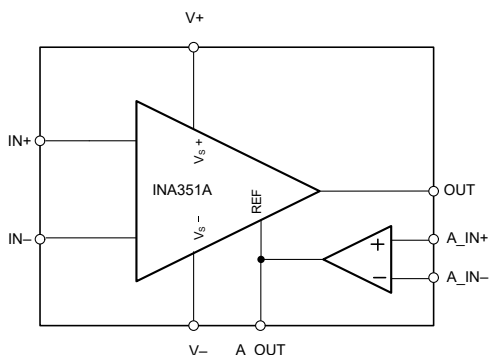
# INA351A - 低消費電力、1.8V~5.5V 小型サイズ計測アンプ、構成可能なリファレンス・アンプ付き

## 1 特長

- 10V/V の固定ゲインの計測アンプで、構成可能なリファレンス・アンプを搭載
- 10 ビット~14 ビットのシステムに対応する INA の性能
  - CMRR: 95dB (標準値)
  - ゲイン誤差: 0.015% (標準値)
  - 帯域幅: 100kHz (標準値)
- リファレンス・アンプは以下の用途に使用できます。
  - サーボ・ループによる外部 DC 誤差のキャリブレーション
  - 外部回路のバッファ電圧を提供
  - リファレンス電圧のフィルタリングまたは調整
- 超小型パッケージのオプション (2mm × 2mm)
- 10% 未満のオーバーシュートで 1nF を駆動 (標準値)
- 最適化された静止電流: 110μA (標準値)
- 電源電圧範囲: 1.8V (±0.9V)~5.5V (±2.75V)
- 仕様温度範囲: -40°C~125°C

## 2 アプリケーション

- 心電計 (ECG)
- 圧力トランスミッタ
- 重量計
- 流量トランスミッタ
- ウェアラブル・フィットネスおよびアクティビティ・モニタ
- 血糖値測定器
- RTD による温度センサ



概略内部回路図

## 3 概要

INA351A は、小型パッケージに構成可能なリファレンス・アンプを備えた 10 の固定ゲインの計測アンプです。この計測アンプ (INA) は、高精度に整合された抵抗を使用し、構築されており、小型で低コストのフォーム・ファクタで、優れた CMRR とゲイン誤差性能を実現しています。このため、INA351A はディスクリート INA 実装に代わる優れたソリューションとなり、部品表 (BOM) コストへの影響を最小限に抑えながら、より高性能でよりコンパクトな設計を実現します。

内蔵された構成可能なリファレンス・アンプは、外部使用のバッファとして、または閉ループ校正回路の一部として使用して、より優れた DC 精度を実現できます。閉ループ校正は、アプリケーションに応じて、INA 入力信号が DC よりもわずかに高い周波数にある場合、INA 出力でセンサからの DC 誤差 (オフセット、オフセット・ドリフトなど) を校正するサーボ・ループ・アンプを実装することで実現できます。

INA351A は、最小 CMRR 86dB、最大ゲイン誤差 0.1% の正確さを達成し、室温で最大 135μA の静止電流しか消費しません。INA は、サブ 1kHz、10 ビット~14 ビットのデルタ・シグマ A/D コンバータ (ADC) を、ADC ドライバなしで直接駆動できるため、心電図やウェアラブル・ヘルス・モニタなどのポータブルなバッテリー駆動の医療アプリケーションに最適です。

### パッケージ情報

部品番号 (3)	パッケージ (1)	パッケージ・サイズ (2)
INA351A	DSG (WSON, 8)	2mm × 2mm

- 利用可能なパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。
- パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- デバイス比較表を参照してください。



## Table of Contents

<b>1 特長</b> .....	<b>1</b>	8.4 Device Functional Modes.....	<b>20</b>
<b>2 アプリケーション</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>21</b>
<b>3 概要</b> .....	<b>1</b>	9.1 Application Information.....	21
<b>4 Revision History</b> .....	<b>2</b>	9.2 Typical Applications.....	24
<b>5 Device Comparison Table</b> .....	<b>3</b>	9.3 Power Supply Recommendations.....	26
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	9.4 Layout.....	27
<b>7 Specifications</b> .....	<b>4</b>	<b>10 Device and Documentation Support</b> .....	<b>29</b>
7.1 Absolute Maximum Ratings.....	4	10.1 Device Support.....	29
7.2 ESD Ratings .....	4	10.2 Documentation Support.....	29
7.3 Recommended Operating Conditions.....	4	10.3 ドキュメントの更新通知を受け取る方法.....	29
7.4 Thermal Information.....	4	10.4 サポート・リソース.....	29
7.5 Electrical Characteristics.....	5	10.5 Trademarks.....	29
7.6 Typical Characteristics.....	7	10.6 静電気放電に関する注意事項.....	29
<b>8 Detailed Description</b> .....	<b>16</b>	10.7 用語集.....	29
8.1 Overview.....	16	<b>11 Mechanical, Packaging, and Orderable</b>	
8.2 Functional Block Diagram.....	16	<b>Information</b> .....	<b>29</b>
8.3 Feature Description.....	17		

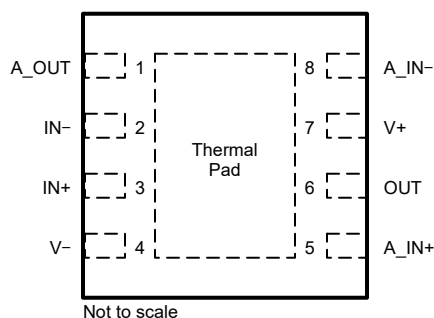
## 4 Revision History

DATE	REVISION	NOTES
June 2023	*	Initial Release

## 5 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS
		WSN DSG
INA351A	1	8

## 6 Pin Configuration and Functions



Note: Connect Thermal Pad to (V-)

**图 6-1. DSG Package,  
8-Pin WSON With Exposed Thermal Pad  
(Top View)**

**表 6-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
IN-	2	I	Instrumentation amplifier negative (inverting) input
IN+	3	I	Instrumentation amplifier positive (non-inverting) input
OUT	6	O	Instrumentation amplifier output
A_IN+	5	I	Reference amplifier positive (non-inverting) input. This pin usually connects to a reference voltage externally.
A_OUT	1	O	Reference amplifier output. This is connected internally to the 60 kΩ resistor of the INA which is also called as REF node.
A_IN-	8	I	Reference amplifier negative (inverting) input.
V-	4	—	Negative supply
V+	7	—	Positive supply

(1) I = input, O = output

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$		0	6	V
Signal input pins	Common mode voltage <sup>(2)</sup>	$(V-) - 0.5$	$(V+) + 0.5$	V
	Differential voltage <sup>(3)</sup>		$V_S + 0.2$	V
	Current <sup>(2)</sup>	-10	10	mA
Output short-circuit <sup>(4)</sup>		Continuous		
Operating Temperature, $T_A$		-55	150	°C
Junction Temperature, $T_J$			150	
Storage Temperature, $T_{stg}$		-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less
- (3) Differential input voltages greater than 0.5 V applied continuously can result in a shift to the input offset voltage above the maximum specification of this parameter. The magnitude of this effect increases as the ambient operating temperature rises.
- (4) Short-circuit to  $V_S / 2$ .

### 7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage $V_S = (V+) - (V-)$	Single-supply	1.8	5.5	V
	Dual-supply	±0.9	±2.75	
Input Voltage Range		$(V-)$	$(V+)$	V
Specified temperature		-40	125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		INA351A	UNIT
		DSG (WSON)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	100.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.4	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	5.3	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	46.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	21.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

For  $V_S = (V_+) - (V_-) = 1.8\text{ V to }5.5\text{ V}$  ( $\pm 0.9\text{ V to } \pm 2.75\text{ V}$ ) at  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = [(V_{IN+}) + (V_{IN-})] / 2 = V_S / 2$ ,  $V_{IN} = (V_{IN+}) - (V_{IN-}) = 0\text{ V}$ ,  $V_{A\_IN+} = V_S / 2$ ,  $V_{A\_IN-} = V_{A\_OUT}$ ,  $G = 10$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V <sub>OSI</sub>	Offset Voltage, RTI <sup>(1)</sup>	V <sub>S</sub> = 5.5 V	T <sub>A</sub> = 25°C		±0.2	±1.3	mV
	Offset Voltage over T, RTI <sup>(1)</sup>	V <sub>S</sub> = 5.5 V	T <sub>A</sub> = −40°C to 125°C			±1.4	mV
	Offset temp drift, RTI <sup>(2)</sup>	V <sub>S</sub> = 5.5 V	T <sub>A</sub> = −40°C to 125°C		±0.60		μV/°C
PSRR	Power-supply rejection ratio		T <sub>A</sub> = 25°C		20	75	μV/V
Z <sub>IN-DM</sub>	Differential Impedance				100    5		GΩ    pF
Z <sub>IN-CM</sub>	Common Mode Impedance				100    9		GΩ    pF
V <sub>CM</sub>	Input Stage Common Mode Range <sup>(3)</sup>			(V−)		(V+)	V
CMRR DC	Common-mode rejection ratio, RTI	V <sub>CM</sub> = (V−) + 0.1 V to (V+) − 1 V, High CMRR Region	V <sub>S</sub> = 5.5 V	86	103		dB
		V <sub>CM</sub> = (V−) + 0.1 V to (V+) − 1 V, High CMRR Region	V <sub>S</sub> = 3.3 V		94		
		V <sub>CM</sub> = (V−) + 0.1 V to (V+) − 0.1 V	V <sub>S</sub> = 5.5 V	62	75		
BIAS CURRENT							
I <sub>B</sub>	Input bias current	V <sub>CM</sub> = V <sub>S</sub> / 2			±0.75		pA
I <sub>OS</sub>	Input offset current	V <sub>CM</sub> = V <sub>S</sub> / 2			±0.40		pA
NOISE VOLTAGE							
e <sub>NI</sub>	Input referred voltage noise density <sup>(5)</sup>	f = 1 kHz			36		nV/√Hz
		f = 10 kHz			35		
E <sub>NI</sub>	Input referred voltage noise <sup>(5)</sup>	f <sub>B</sub> = 0.1 Hz to 10 Hz			3.0		μV <sub>PP</sub>
i <sub>n</sub>	Input current noise	f = 1 kHz			22		fA/√Hz
GAIN							
GE	Gain error <sup>(4)</sup>	V <sub>REF</sub> = V <sub>S</sub> /2	V <sub>O</sub> = (V−) + 0.1 V to (V+) − 0.1V		±0.02	±0.10	%
OUTPUT							
V <sub>OH</sub>	Positive rail headroom	R <sub>L</sub> = 10 kΩ to V <sub>S</sub> /2			15	30	mV
V <sub>OL</sub>	Negative rail headroom	R <sub>L</sub> = 10 kΩ to V <sub>S</sub> /2			15	30	mV
C <sub>L</sub> Drive	Load capacitance drive	V <sub>O</sub> = 100 mV step, Overshoot < 20%			500		pF
Z <sub>O</sub>	Closed-loop output impedance	f = 10 kHz			51		Ω
I <sub>SC</sub>	Short-circuit current	V <sub>S</sub> = 5.5 V			±20		mA
FREQUENCY RESPONSE							
BW	Bandwidth, −3 dB	V <sub>IN</sub> = 10 mV <sub>pk-pk</sub>			100		kHz
THD + N	Total harmonic distortion + noise	V <sub>S</sub> = 5.5 V, V <sub>CM</sub> = 2.75 V, V <sub>O</sub> = 1 V <sub>RMS</sub> , R <sub>L</sub> = 100 kΩ f = 1 kHz, 80-kHz measurement BW			0.035		%
EMIRR	Electro-magnetic interference rejection ratio	f = 1 GHz, V <sub>IN-EMIRR</sub> = 100 mV			96		dB
SR	Slew rate	V <sub>S</sub> = 5 V, V <sub>O</sub> = 2 V step			0.20		V/μs
t <sub>S</sub>	Settling time	To 0.1%, V <sub>S</sub> = 5.5 V, V <sub>STEP</sub> = 2 V, C <sub>L</sub> = 10 pF			14		μs
		To 0.01%, V <sub>S</sub> = 5.5 V, V <sub>STEP</sub> = 2 V, C <sub>L</sub> = 10 pF			24		
	Overload recovery	V <sub>IN</sub> = 1 V			8		μs
REFERENCE AMPLIFIER							
REF - V <sub>OS</sub>	Ref. input offset voltage	V <sub>S</sub> = 5.5 V <sup>(4)</sup>			±0.6	±2.25	mV
REF - V <sub>OS</sub>	Ref. input offset voltage drift	V <sub>S</sub> = 5.5 V			±0.8		μV/°C

## 7.5 Electrical Characteristics (continued)

For  $V_S = (V_+) - (V_-) = 1.8\text{ V to } 5.5\text{ V}$  ( $\pm 0.9\text{ V to } \pm 2.75\text{ V}$ ) at  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = [(V_{IN+}) + (V_{IN-})] / 2 = V_S / 2$ ,  $V_{IN} = (V_{IN+}) - (V_{IN-}) = 0\text{ V}$ ,  $V_{A\_IN+} = V_S / 2$ ,  $V_{A\_IN-} = V_{A\_OUT}$ ,  $G = 10$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
REF - I <sub>B</sub>	Ref. input bias current	V <sub>S</sub> = 5.5 V		±1			pA
REF - Z <sub>INCM</sub>	Ref. common mode input impedance			100    0.5			GΩ    pF
REF - E <sub>N</sub>	Ref. input voltage noise	f = 0.1 to 10 Hz		8.7			μV <sub>PP</sub>
REF - e <sub>N</sub>	Ref. input voltage noise density	f = 10 kHz		64			nV/√Hz
REF - V <sub>IN</sub>	Ref. input voltage range	V <sub>S</sub> = 5.5 V		(V−)		(V+)	V
REF - A <sub>OL</sub>	Ref. open loop voltage gain	(V−) + 0.1 V < V <sub>O</sub> < (V+) − 0.1 V	V <sub>S</sub> = 5.5 V	120			dB
REF - GBW	Ref. gain-bandwidth product	V <sub>S</sub> = 5.5 V		360			kHz
REF - t <sub>S</sub>	Ref. settling time	To 0.1%, V <sub>S</sub> = 5.5 V, V <sub>STEP</sub> = 2 V, G = 1, C <sub>L</sub> = 10 pF		25			μs
REF - PM	Ref. phase margin	V <sub>S</sub> = 5.5 V, G = 1, C <sub>L</sub> = 10 pF		65			°
REF - V <sub>O</sub>	Ref. voltage output swing from rail	V <sub>S</sub> = 5.5 V, G = 1				175	mV
REF - I <sub>SC</sub>	Ref. short circuit current	V <sub>S</sub> = 5.5 V, G = 1		±3			mA
POWER SUPPLY							
V <sub>S</sub>	Power-supply voltage	Single-supply		1.8		5.5	V
		Dual-supply		±0.85		±2.75	
I <sub>Q</sub>	Quiescent current	V <sub>IN</sub> = 0 V		110		135	μA
		T <sub>A</sub> = −40°C to 125°C				147	

- (1) Total offset, referred-to-input (RTI):  $V_{OS} = (V_{OSI}) + (V_{OSO} / G)$ .
- (2) Offset drifts are uncorrelated. Input-referred offset drift is calculated using:  $\Delta V_{OS(RTI)} = \sqrt{[\Delta V_{OSI}]^2 + (\Delta V_{OSO} / G)^2}$
- (3) Input common mode voltage range of the just the input stage of the instrumentation amplifier. The entire INA351 input range depends on the combination input common-mode voltage, differential voltage, gain,  $A\_OUT$  voltage and power supply voltage. *Typical Characteristic* curves will be added with more information.
- (4) Min and Max values are specified by characterization.
- (5) Total RTI voltage noise is equal to:  $e_{N(RTI)} = \sqrt{[e_{NI}]^2 + (e_{NO} / G)^2}$

## 7.6 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = (V_+) - (V_-) = 5.5\text{ V}$ ,  $V_{IN} = (V_{IN+}) - (V_{IN-}) = 0\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$ ,  $V_{REF} = V_S / 2$ ,  $V_{CM} = [(V_{IN+}) + (V_{IN-})] / 2 = V_S / 2$ ,  $V_{OUT} = V_S / 2$ ,  $V_{A\_IN+} = V_S / 2$ ,  $V_{A\_OUT} = V_{A\_IN-}$  and  $G = 10$  (unless otherwise noted)

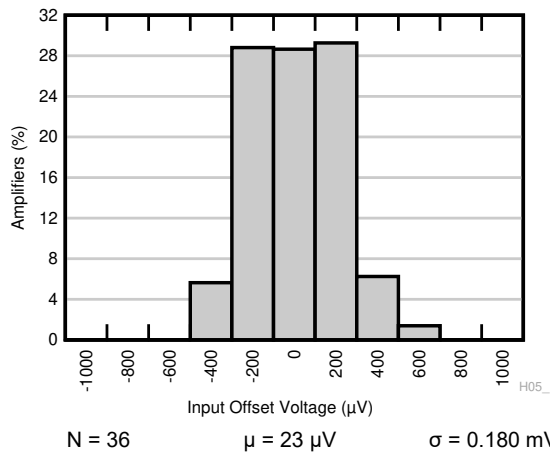


FIG 7-1. Typical Distribution of Input Referred Offset Voltage

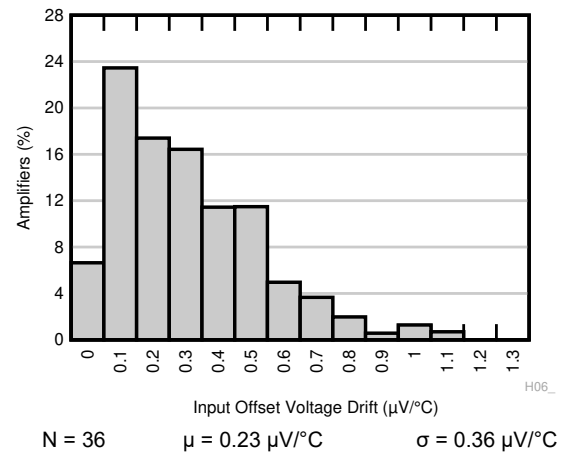


FIG 7-2. Typical Distribution of Input Referred Offset Drift

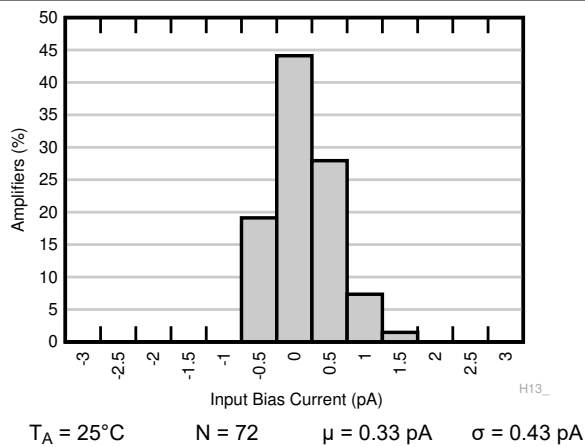


FIG 7-3. Typical Distribution of Input Bias Current

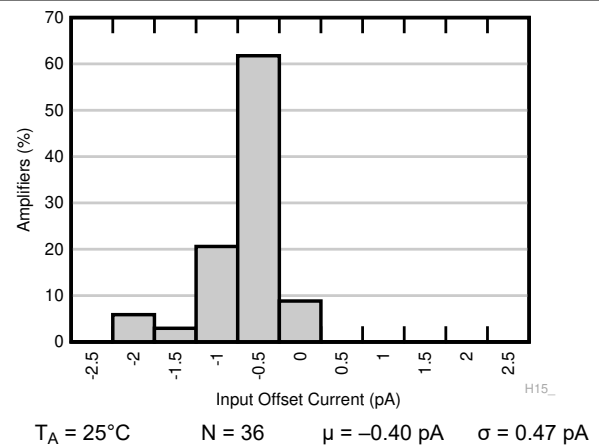


FIG 7-4. Typical Distribution of Input Offset Current

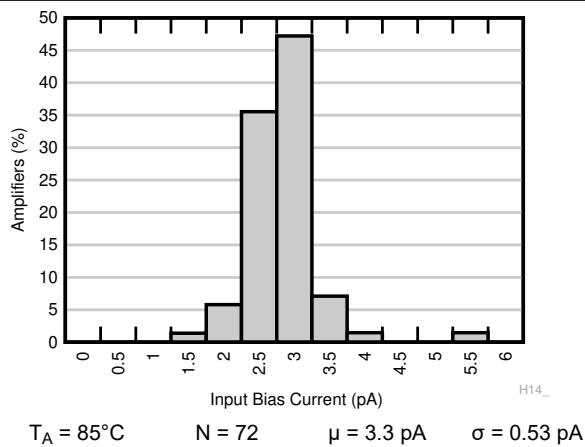


FIG 7-5. Typical Distribution of Input Bias Current

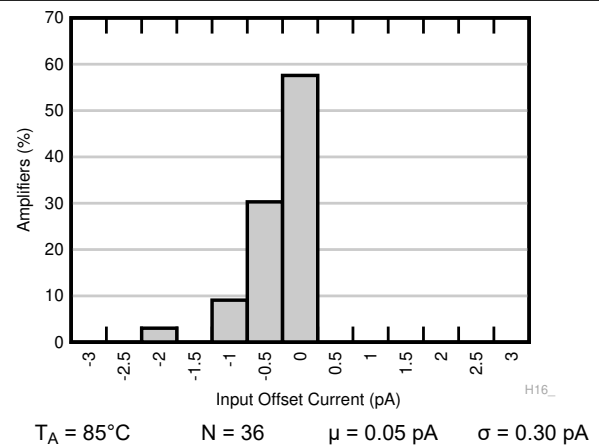


FIG 7-6. Typical Distribution of Input Offset Current

## 7.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = (V_+) - (V_-) = 5.5\text{ V}$ ,  $V_{IN} = (V_{IN+}) - (V_{IN-}) = 0\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$ ,  $V_{REF} = V_S / 2$ ,  $V_{CM} = [(V_{IN+}) + (V_{IN-})] / 2 = V_S / 2$ ,  $V_{OUT} = V_S / 2$ ,  $V_{A\_IN+} = V_S / 2$ ,  $V_{A\_OUT} = V_{A\_IN-}$  and  $G = 10$  (unless otherwise noted)

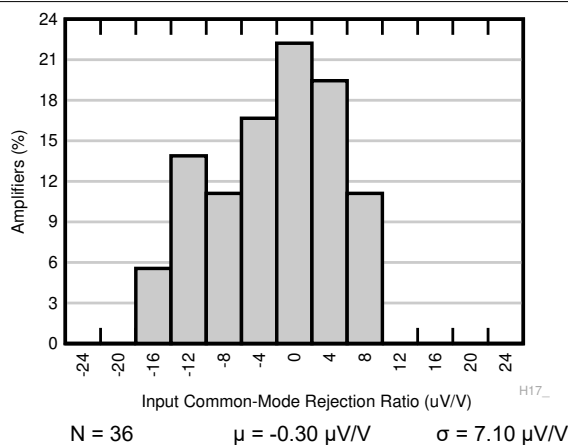


FIG 7-7. Typical Distribution of CMRR

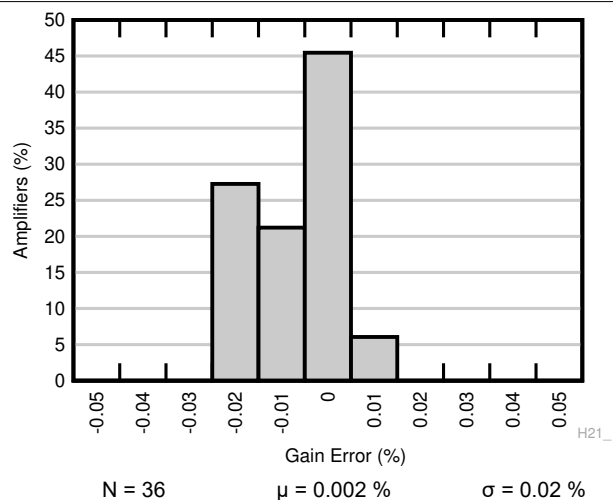


FIG 7-8. Typical Distribution of Gain Error

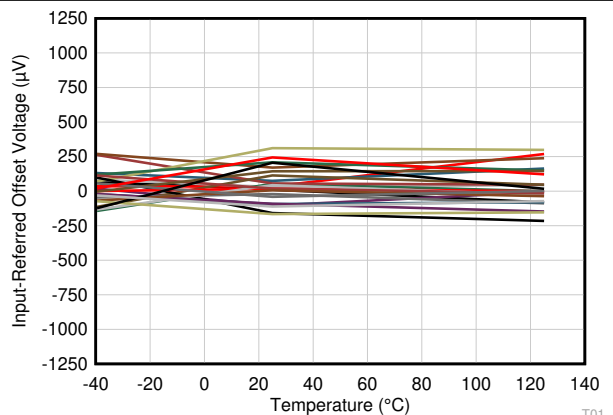


FIG 7-9. Input Referred Offset Voltage vs Temperature

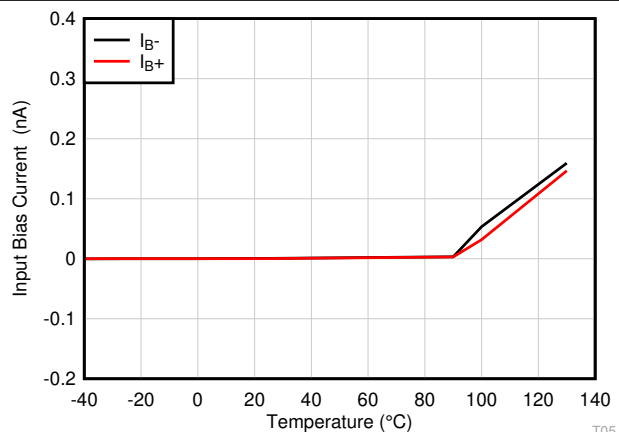


FIG 7-10. Input Bias Current vs Temperature

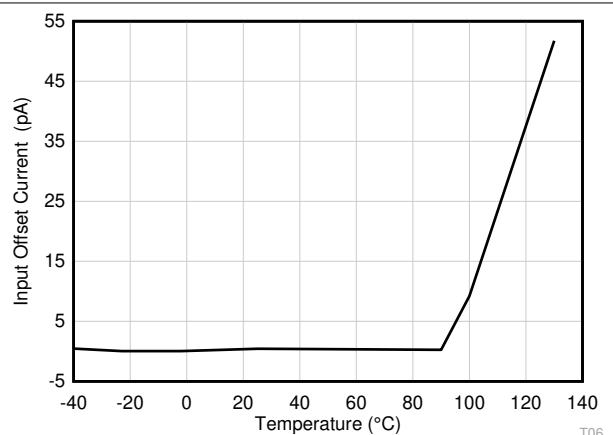


FIG 7-11. Input Offset Current vs Temperature

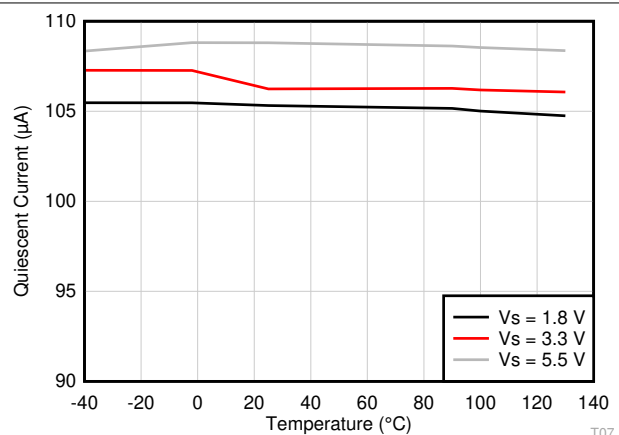


FIG 7-12. Quiescent Current vs Temperature

## 7.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = (V_+) - (V_-) = 5.5\text{ V}$ ,  $V_{IN} = (V_{IN+}) - (V_{IN-}) = 0\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$ ,  $V_{REF} = V_S / 2$ ,  $V_{CM} = [(V_{IN+}) + (V_{IN-})] / 2 = V_S / 2$ ,  $V_{OUT} = V_S / 2$ ,  $V_{A\_IN+} = V_S / 2$ ,  $V_{A\_OUT} = V_{A\_IN-}$  and  $G = 10$  (unless otherwise noted)

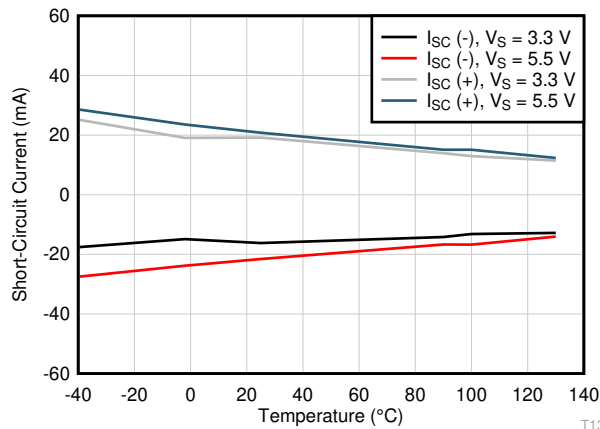


FIG 7-13. Short Circuit Current vs Temperature

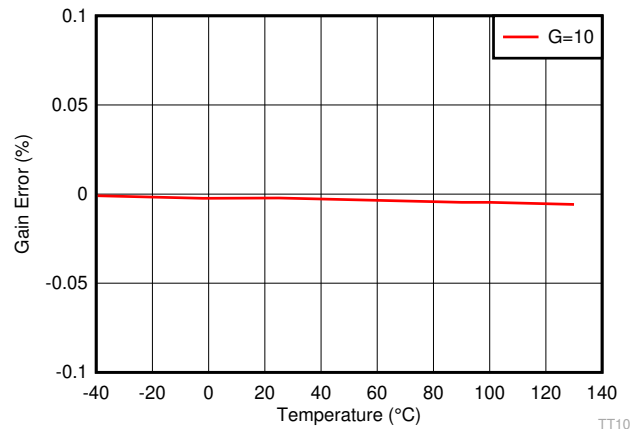


FIG 7-14. Gain Error vs Temperature

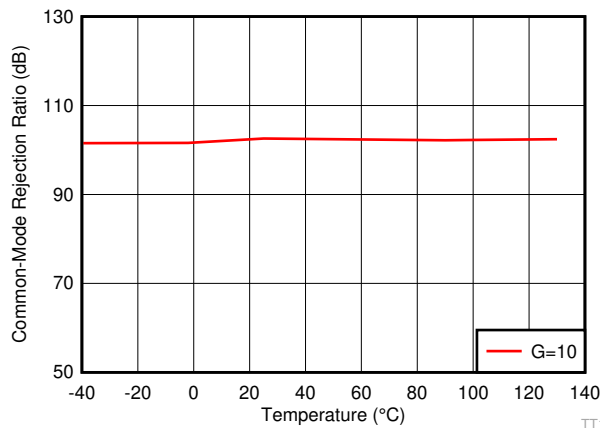
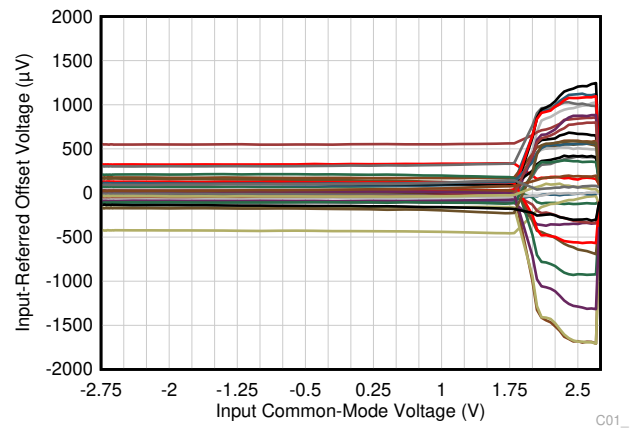
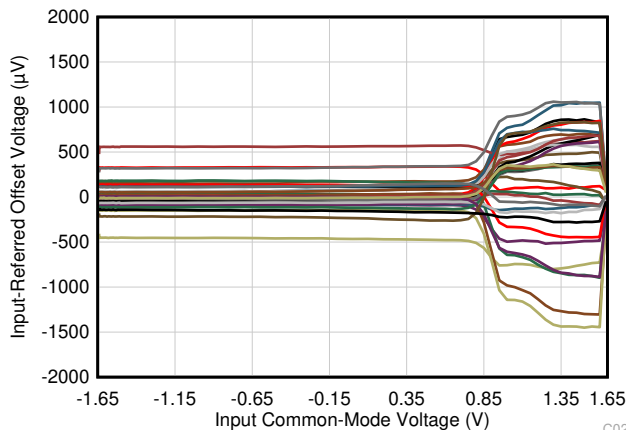


FIG 7-15. CMRR vs Temperature



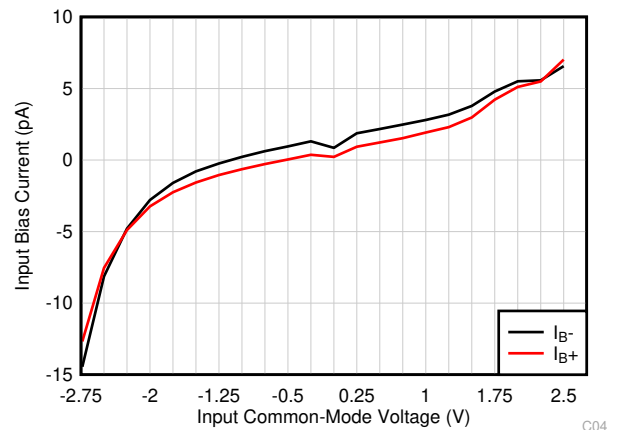
$V_+ = 2.75\text{ V}$  and  $V_- = -2.75\text{ V}$

FIG 7-16. Input Referred Offset Voltage vs Input Common-Mode Voltage



$V_+ = 1.65\text{ V}$  and  $V_- = -1.65\text{ V}$

FIG 7-17. Input Referred Offset Voltage vs Input Common-Mode Voltage

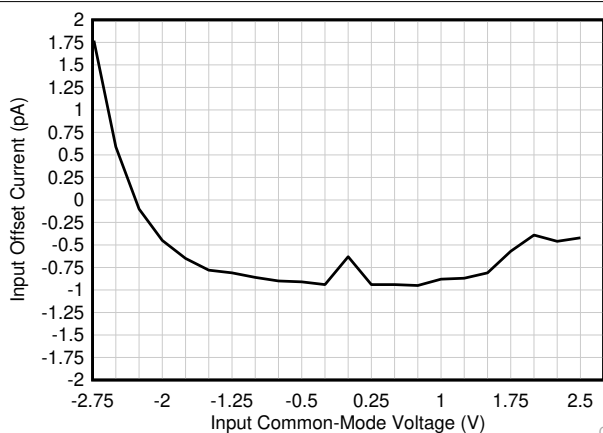


$V_+ = 2.75\text{ V}$  and  $V_- = -2.75\text{ V}$

FIG 7-18. Input Bias Current vs Input Common-Mode Voltage

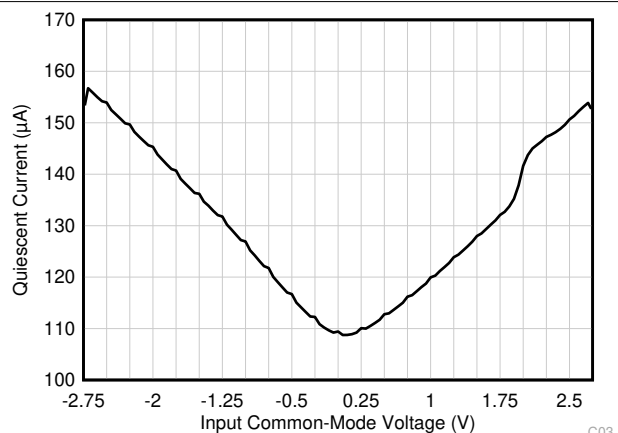
## 7.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = (V_+) - (V_-) = 5.5\text{ V}$ ,  $V_{IN} = (V_{IN+}) - (V_{IN-}) = 0\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$ ,  $V_{REF} = V_S / 2$ ,  $V_{CM} = [(V_{IN+}) + (V_{IN-})] / 2 = V_S / 2$ ,  $V_{OUT} = V_S / 2$ ,  $V_{A\_IN+} = V_S / 2$ ,  $V_{A\_OUT} = V_{A\_IN-}$  and  $G = 10$  (unless otherwise noted)



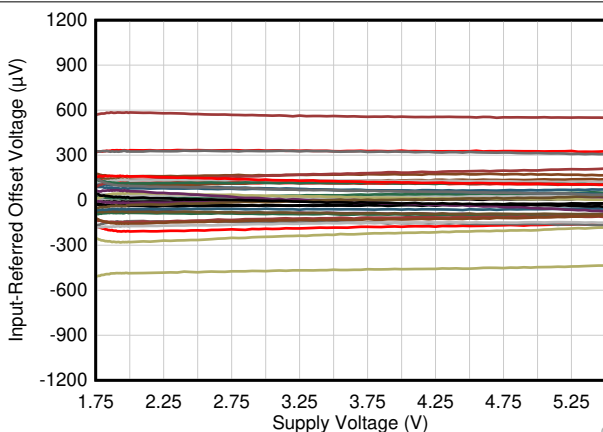
$V_+ = 2.75\text{ V}$  and  $V_- = -2.75\text{ V}$

7-19. Input Offset Current vs Input Common-Mode Voltage

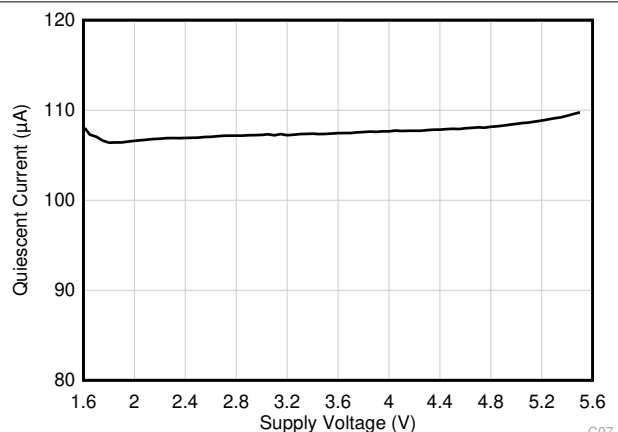


$V_+ = 2.75\text{ V}$  and  $V_- = -2.75\text{ V}$

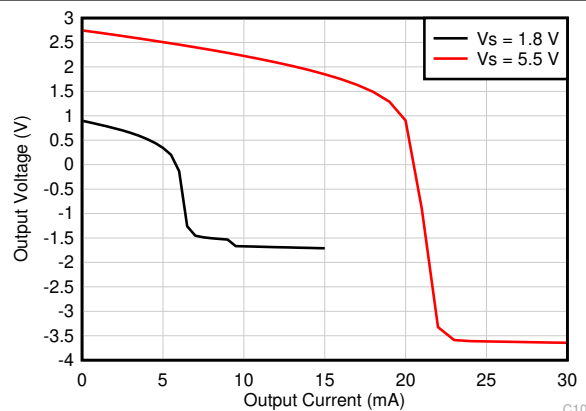
7-20. Quiescent Current vs Input Common-Mode Voltage



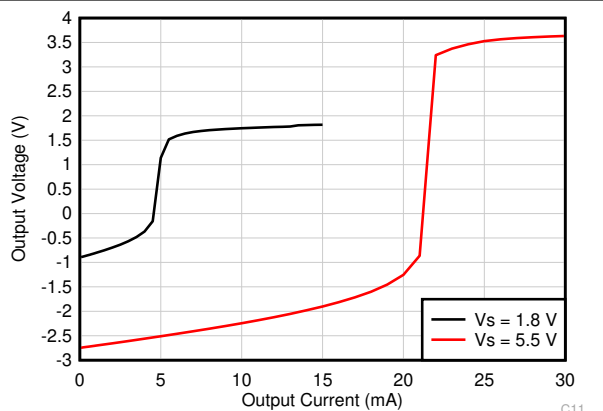
7-21. Input Referred Offset Voltage vs Supply Voltage



7-22. Quiescent Current vs Supply Voltage



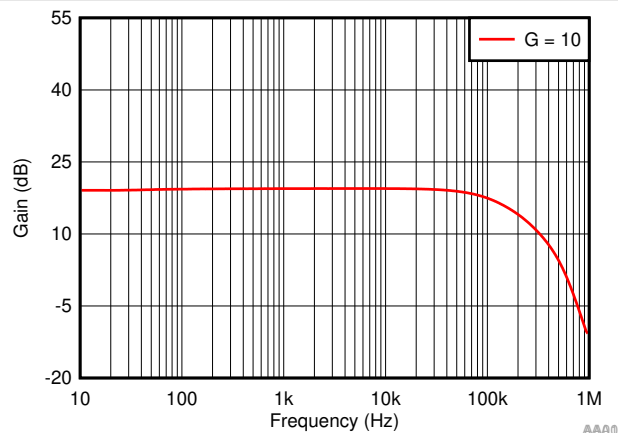
7-23. Output Voltage vs Output Current (Sourcing)



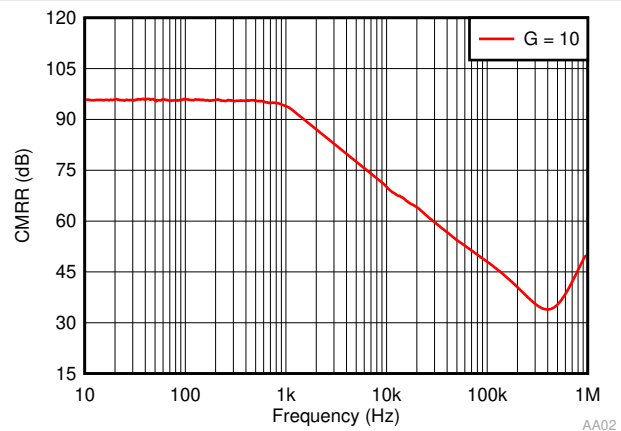
7-24. Output Voltage vs Output Current (Sinking)

## 7.6 Typical Characteristics (continued)

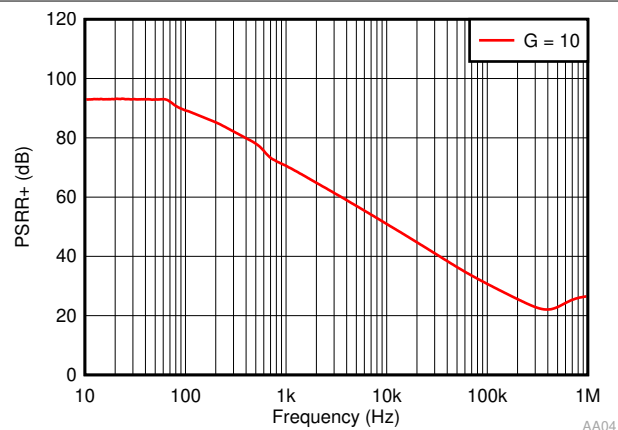
at  $T_A = 25^\circ\text{C}$ ,  $V_S = (V_+) - (V_-) = 5.5\text{ V}$ ,  $V_{IN} = (V_{IN+}) - (V_{IN-}) = 0\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$ ,  $V_{REF} = V_S / 2$ ,  $V_{CM} = [(V_{IN+}) + (V_{IN-})] / 2 = V_S / 2$ ,  $V_{OUT} = V_S / 2$ ,  $V_{A\_IN+} = V_S / 2$ ,  $V_{A\_OUT} = V_{A\_IN-}$  and  $G = 10$  (unless otherwise noted)



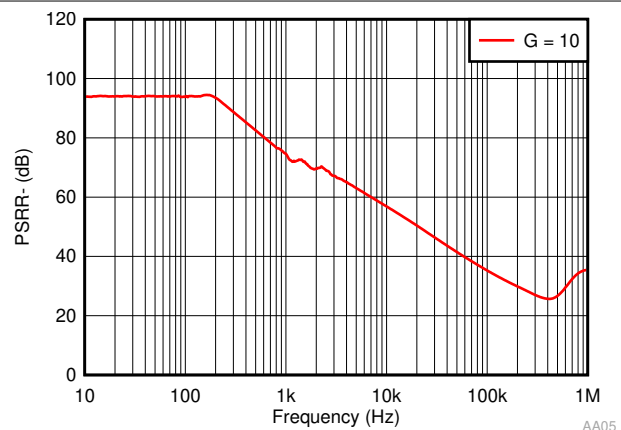
7-25. Closed-Loop Gain vs Frequency



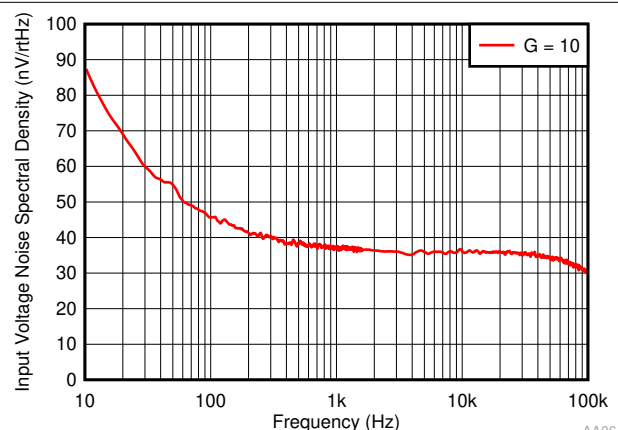
7-26. CMRR (Referred to Input) vs Frequency



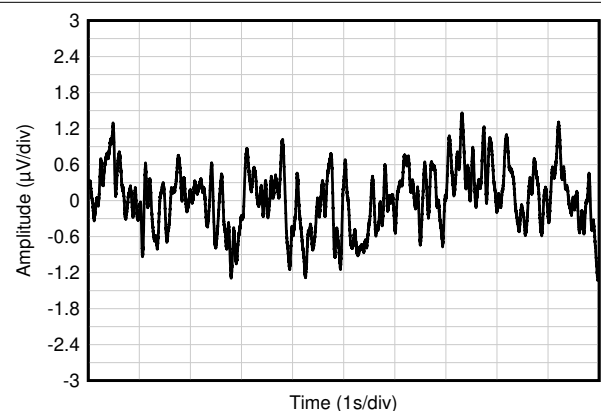
7-27. PSRR+ (Referred to Input) vs Frequency



7-28. PSRR- (Referred to Input) vs Frequency



7-29. Input Referred Voltage Noise Spectral Density



7-30. 0.1 Hz to 10 Hz Voltage Noise in Time Domain

## 7.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = (V_+) - (V_-) = 5.5\text{ V}$ ,  $V_{IN} = (V_{IN+}) - (V_{IN-}) = 0\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$ ,  $V_{REF} = V_S / 2$ ,  $V_{CM} = [(V_{IN+}) + (V_{IN-})] / 2 = V_S / 2$ ,  $V_{OUT} = V_S / 2$ ,  $V_{A\_IN+} = V_S / 2$ ,  $V_{A\_OUT} = V_{A\_IN-}$  and  $G = 10$  (unless otherwise noted)

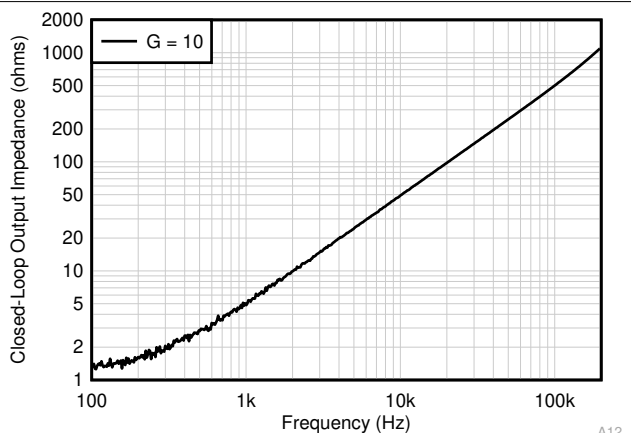


FIG 7-31. Closed-Loop Output Impedance vs Frequency

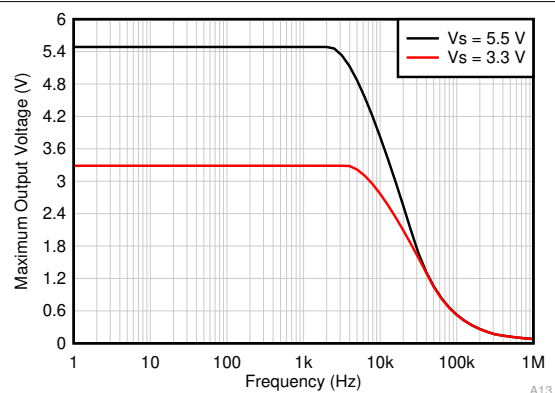


FIG 7-32. Maximum Output Voltage vs Frequency

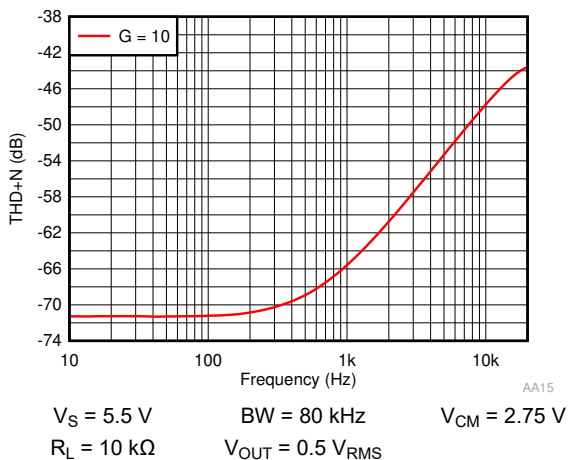


FIG 7-33. THD + N Frequency

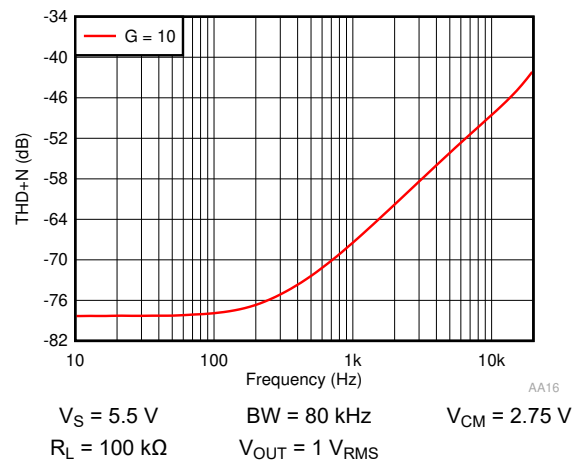


FIG 7-34. THD + N Frequency

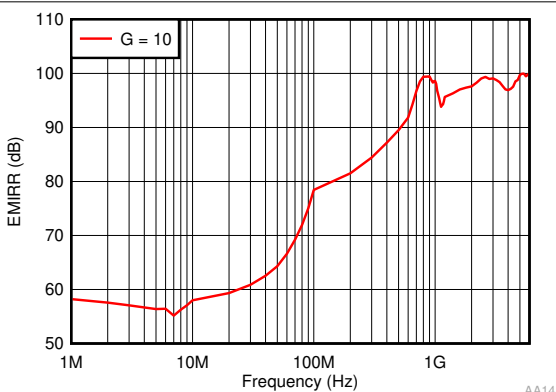


FIG 7-35. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

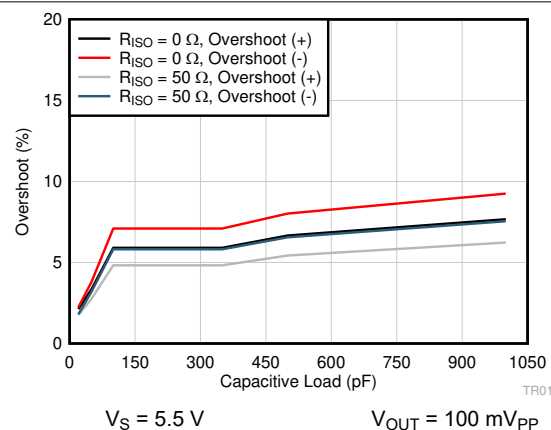
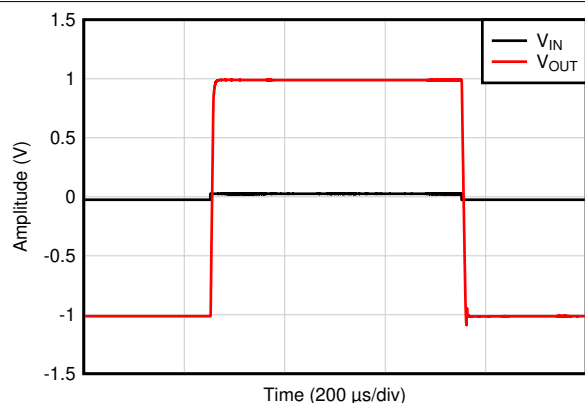


FIG 7-36. Small-Signal Overshoot vs Capacitive Load

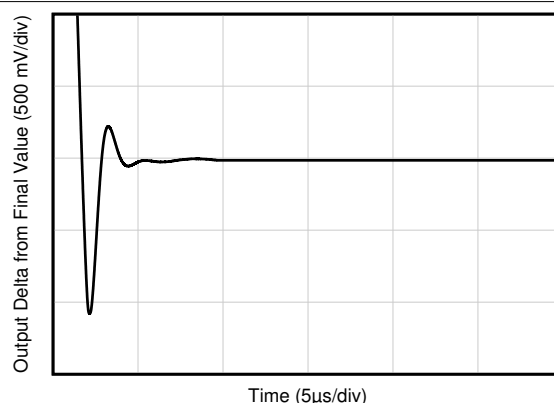
## 7.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = (V_+) - (V_-) = 5.5\text{ V}$ ,  $V_{IN} = (V_{IN+}) - (V_{IN-}) = 0\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$ ,  $V_{REF} = V_S / 2$ ,  $V_{CM} = [(V_{IN+}) + (V_{IN-})] / 2 = V_S / 2$ ,  $V_{OUT} = V_S / 2$ ,  $V_{A\_IN+} = V_S / 2$ ,  $V_{A\_OUT} = V_{A\_IN-}$  and  $G = 10$  (unless otherwise noted)



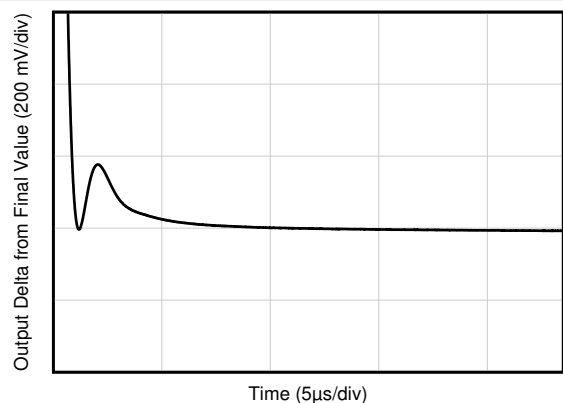
$V_+ = 2.75\text{ V}$        $V_- = -2.75\text{ V}$        $V_{OUT} = 2\text{ V}_{PP}$

7-37. Large Signal Step Response



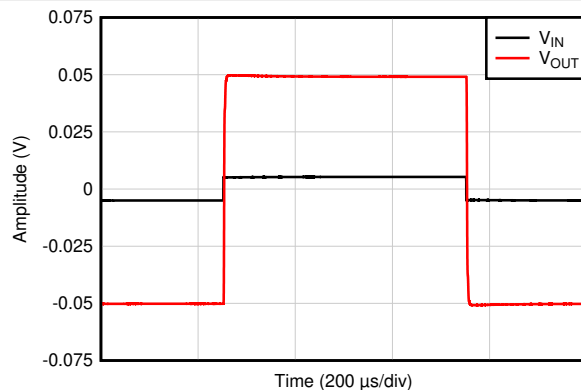
$V_+ = 2.75\text{ V}$        $V_- = -2.75\text{ V}$        $V_{OUT} = 2\text{ V}_{PP}$

7-38. Large Signal Settling Time (Falling Edge)



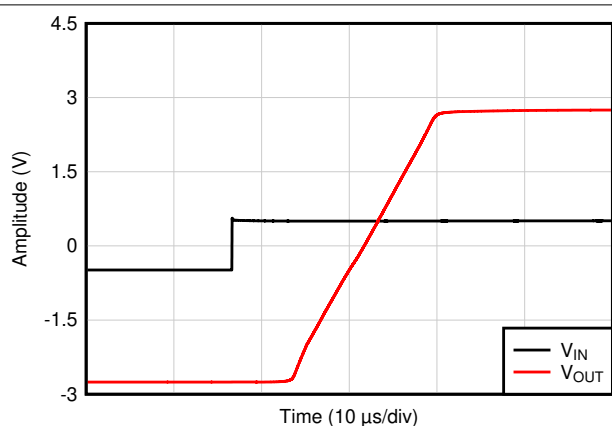
$V_+ = 2.75\text{ V}$        $V_- = -2.75\text{ V}$        $V_{OUT} = 2\text{ V}_{PP}$

7-39. Large Signal Settling Time (Rising Edge)



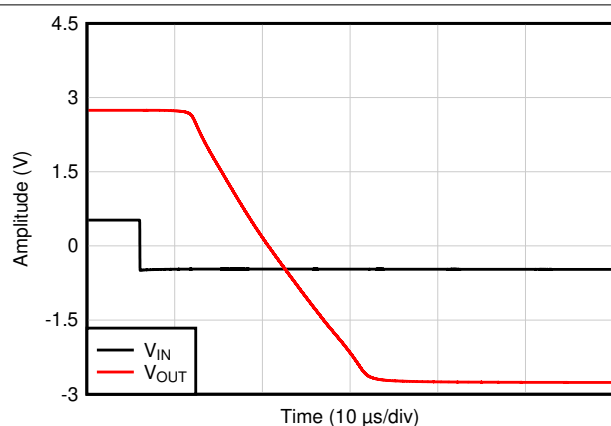
$V_+ = 2.75\text{ V}$        $V_- = -2.75\text{ V}$        $V_{OUT} = 0.1\text{ V}_{PP}$

7-40. Small-Signal Step Response



$V_+ = 2.75\text{ V}$        $V_- = -2.75\text{ V}$        $V_{IN} = 1\text{ V}_{PP}$

7-41. Over-Load Recovery (Rising Edge)

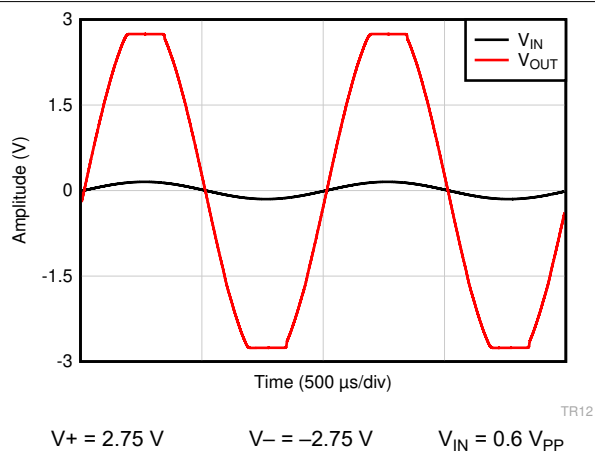


$V_+ = 2.75\text{ V}$        $V_- = -2.75\text{ V}$        $V_{IN} = 1\text{ V}_{PP}$

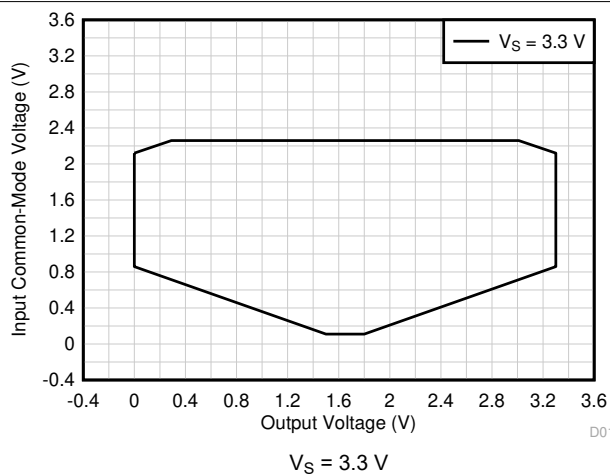
7-42. Over-Load Recovery (Falling Edge)

## 7.6 Typical Characteristics (continued)

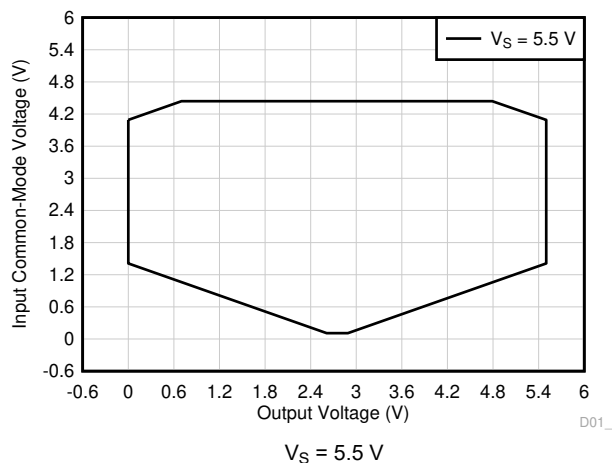
at  $T_A = 25^\circ\text{C}$ ,  $V_S = (V_+) - (V_-) = 5.5\text{ V}$ ,  $V_{IN} = (V_{IN+}) - (V_{IN-}) = 0\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$ ,  $V_{REF} = V_S / 2$ ,  $V_{CM} = [(V_{IN+}) + (V_{IN-})] / 2 = V_S / 2$ ,  $V_{OUT} = V_S / 2$ ,  $V_{A\_IN+} = V_S / 2$ ,  $V_{A\_OUT} = V_{A\_IN-}$  and  $G = 10$  (unless otherwise noted)



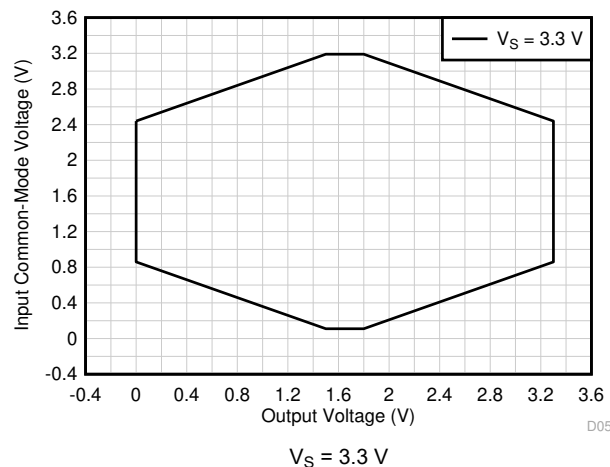
7-43. No Phase Reversal



7-44. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)



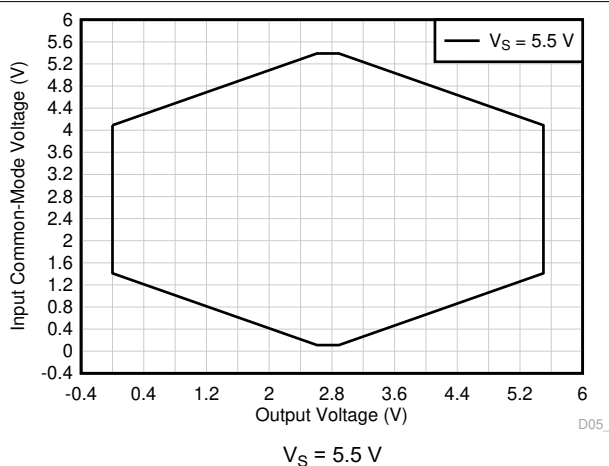
7-45. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)



7-46. Input Common-Mode Voltage vs Output Voltage

## 7.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = (V_+) - (V_-) = 5.5\text{ V}$ ,  $V_{IN} = (V_{IN+}) - (V_{IN-}) = 0\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$ ,  $V_{REF} = V_S / 2$ ,  $V_{CM} = [(V_{IN+}) + (V_{IN-})] / 2 = V_S / 2$ ,  $V_{OUT} = V_S / 2$ ,  $V_{A\_IN+} = V_S / 2$ ,  $V_{A\_OUT} = V_{A\_IN-}$  and  $G = 10$  (unless otherwise noted)



**7-47. Input Common-Mode Voltage vs Output Voltage**

## 8 Detailed Description

### 8.1 Overview

INA351A is a  $G = 10$  instrumentation amplifier with configurable reference amplifier designed to provide an integrated, small size, cost-effective solution for applications employing discrete implementation of INA using commodity amplifiers and resistors. This integrated instrumentation amplifier is built using four operational amplifiers and seven precision matched integrated resistors. With 86dB minimum CMRR and 0.1% maximum gain error, INA351A is suitable to be used directly in sub 10-bit systems without any external calibration. Additional calibration of offset and gain error at a system level can further improve system resolution and accuracy, enabling use in 12-bit to 14-bit precision applications.

INA351A has a configurable reference amplifier with external input and output pins. This reference amplifier's output is connected to the 60-k $\Omega$  internal resistor so that any reference voltage on the amplifier input that sets the output common mode of the INA could be buffered. This buffered output voltage is available externally and could be used to bias subsequent amplifier stages.

More importantly, the reference amplifier enables DC error calibration when configured in a servo loop. When the INA input signal is at a slightly higher frequency than DC, the servo amplifier can enable external calibration of total DC errors (offset, drift etc.) at the INA output leading to a overall better DC precision. The INA351A in calibration loop is well suited for medical applications where the low-frequency signals like ECG, EEG, EMG are to be amplified with relatively lower noise and lesser DC errors. It is also suitable for use in industrial applications in higher frequency pressure transducers and lock in amplifier designs.

One of the key features of INA351A is that the device does not need any external resistors to set the gain. Often these external resistors require tighter tolerance and careful routing, which adds to system complexity and cost. The device is highly suitable for voltage sensing in space-constrained applications such as patient monitoring, sleep diagnostics, electronic hospital beds, and blood glucose monitoring. INA351A can enable these systems to reduce their overall size and cost while providing optimal performance.

### 8.2 Functional Block Diagram

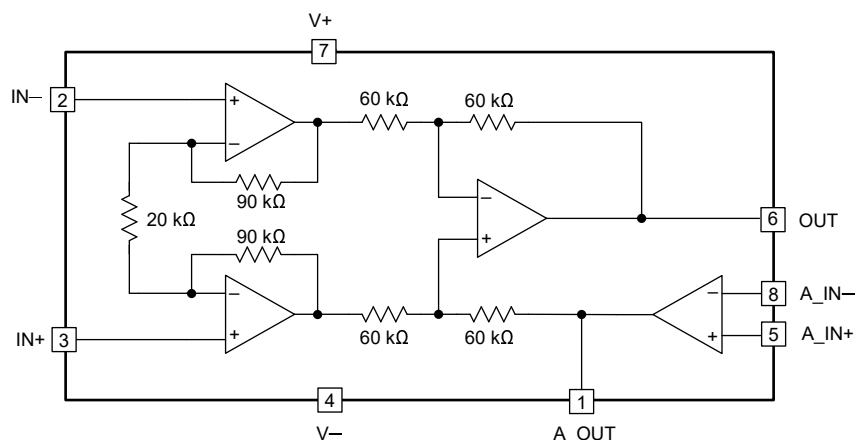


图 8-1. Simplified Internal Schematic

## 8.3 Feature Description

### 8.3.1 Gain-Setting

#### 8.3.1.1 Gain Error and Drift

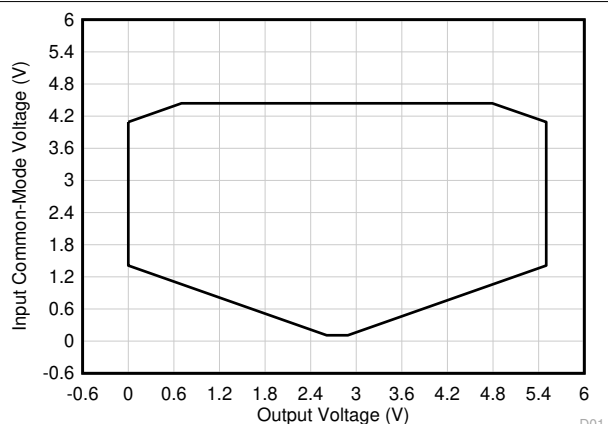
Gain error in INA351A is limited by the mismatch of the integrated precision resistors and is specified based on characterization results. Gain error of maximum 0.1% can be expected for this INA. Gain drift in INA351A is limited by the slight mismatch of the temperature coefficient of the integrated resistors. Since these integrated resistors are precision matched with low temperature coefficient resistors to begin with, the overall gain drift is much better in comparison to discrete implementation of the instrumentation amplifiers built using external resistors.

### 8.3.2 Input Common-Mode Voltage Range

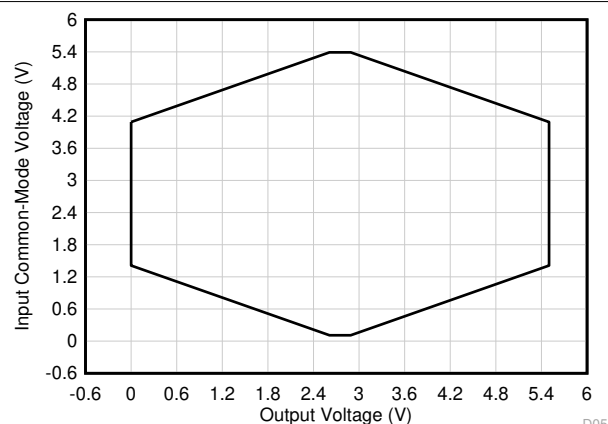
INA351A has two gain stages, the first stage has a common-mode gain of 1 and a differential gain of 10. The second stage is configured in a difference-amplifier configuration with differential gain of 1 and ideally rejects all of the input common mode completely. The second stage also provides a gain of 1 from voltage at A\_OUT to set the output common-mode voltage.

The linear input voltage range of the INA351A, even for a rail-to-rail first stage, is dictated by both the signal swing at output of the first stage as well as the input common-mode voltage range output swing of the second stage. In order to maximize performance, it is critical to keep the INA351A within its linear range for a given combination of reference amp's output voltage (A\_OUT connects to REF), and input common-mode voltage for a particular input differential. Input common-mode voltage ( $V_{CM}$ ) vs output voltage graphs ( $V_{OUT}$ ) in this section show a particular A\_OUT voltage and gain configuration to outline the linear performance region of INA351A. A good common-mode rejection can be expected when operating within the limits of the  $V_{CM}$  vs  $V_{OUT}$  graph. Note that the INA351A linear input voltage cannot be close to or extend beyond the supply rails, as the output of the first stage will be driven into saturation.

The common-mode range for the most common operating conditions is outlined in the following figures. [Figure 8-2](#) shows the region of operation where a minimum of 86 dB can be achieved. [Figure 8-3](#) has much wider region of operation with a lower minimum CMRR of 62 dB, because the input signal crosses over the transition region of the input pairs to achieve rail-to-rail operation. The common-mode range for other operating conditions is best calculated with the INA  $V_{CM}$  vs  $V_{OUT}$  tool located under the *Amplifiers and Comparators* section of the [Analog Engineer's Calculator](#) on ti.com. INA351-HCM model can be specifically used for applications requiring high CMRR and corresponds to performance shown in [Figure 8-2](#). INA351xxS model can be used for applications where the input common mode can be expected to vary rail-to-rail and the model corresponds to performance shown in [Figure 8-3](#), where CMRR drops to 62-dB minimum.



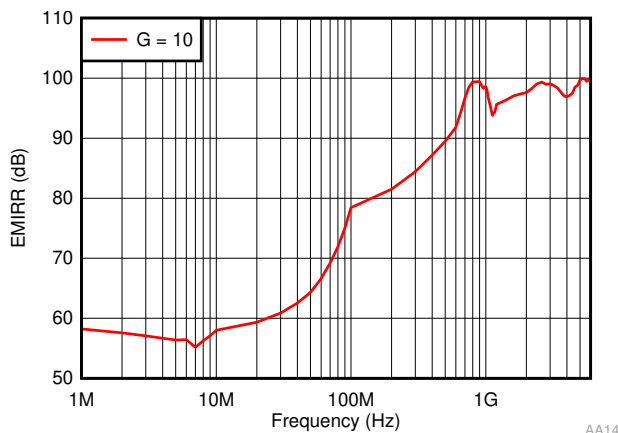
**Figure 8-2. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)**



**Figure 8-3. Input Common-Mode Voltage vs Output Voltage**

### 8.3.3 EMI Rejection

The INA351A uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the INA351A benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. [图 8-4](#) shows the results of this testing on the INA351A. [表 8-1](#) provides the EMIRR IN+ values for the INA351A at particular frequencies commonly encountered in real-world applications. The [EMI Rejection Ratio of Operational Amplifiers](#) application report contains detailed information on the topic of EMIRR performance relating to op amps and is available for download from [www.ti.com](http://www.ti.com).



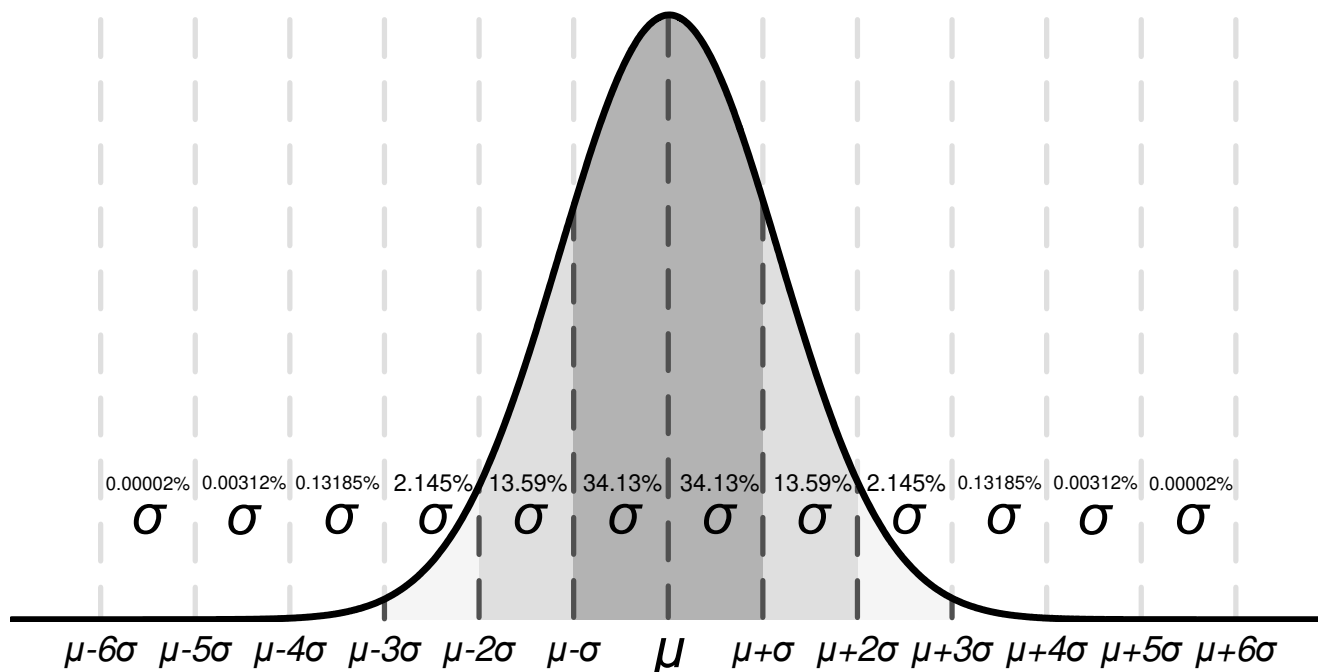
**图 8-4. EMIRR Testing**

**表 8-1. INA351A EMIRR IN+ for Frequencies of Interest**

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	88 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	99 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	97 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	98 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	97 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	99 dB

### 8.3.4 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier exhibits some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian (bell curve)*, or *normal* distributions, and circuit designers can leverage this information to guard band their system, even when there is not a minimum or maximum specification in the [Electrical Characteristics](#) table.



8-5. Ideal Gaussian Distribution

8-5 shows an example distribution, where  $\mu$ , or *mu*, is the mean of the distribution, and where  $\sigma$ , or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from  $\mu - \sigma$  to  $\mu + \sigma$ ).

Depending on the specification, values listed in the *typical* column of the [Electrical Characteristics](#) table are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean ( $\mu$ ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation ( $\mu + \sigma$ ) to most accurately represent the typical value.

Designers can use this chart to calculate approximate probability of a specification in a unit; for example, the INA351A typical input referred voltage offset is 200  $\mu$ V, so 68.2% of all INA351A devices are expected to have an offset from  $-200 \mu$ V to  $+200 \mu$ V. At  $4 \sigma$  ( $\pm 800 \mu$ V), 99.9937% of the distribution has an offset voltage less than  $\pm 800 \mu$ V, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are verified by TI, and units outside these limits are removed from production material. For example, the INA351A family has a maximum offset voltage of 1.3 mV at 25°C, and even though this corresponds to  $6 \sigma$  ( $\approx 1$  in 500 million units), which is extremely unlikely, TI verifies that any unit with larger offset than 1.3 mV are removed from production material.

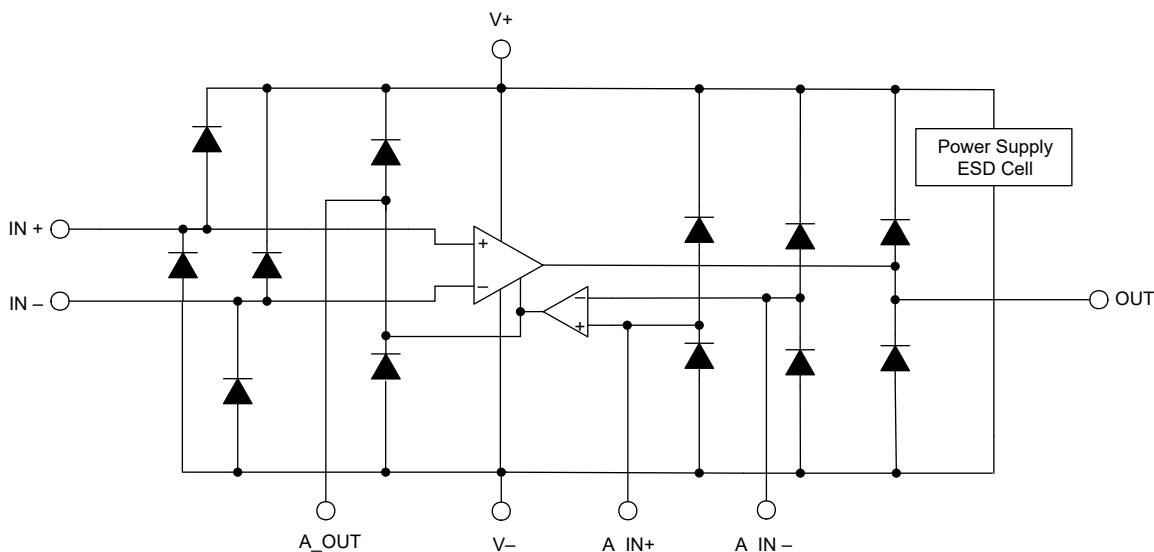
For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guard band for the designers application, and design worst-case conditions using this value. As stated earlier, the  $6\text{-}\sigma$  value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and can be an option as a wide guard band to design a system around. In this case, the INA351A family does not have a maximum or minimum for offset voltage drift, but based on 7-2 and the typical value of 0.65  $\mu$ V/°C in the [Electrical Characteristics](#) table, the  $6\text{-}\sigma$  value for offset voltage drift can be calculated to 3.9  $\mu$ V/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset drift without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot verify the performance of a device. This information must be used only to estimate the performance of a device.

### 8.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. [Figure 8-6](#) shows the ESD circuits contained in the INA351A devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where these diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.



**Figure 8-6. Equivalent Internal ESD Circuitry**

## 8.4 Device Functional Modes

INA351A has only one functional mode. The device can be powered in single supply or dual supply configurations as long as the device is supplied with  $V_S = (V+) - (V-) = 1.8\text{ V to }5.5\text{ V}$  as specified in the recommended operating conditions.

## 9 Application and Implementation

注


Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

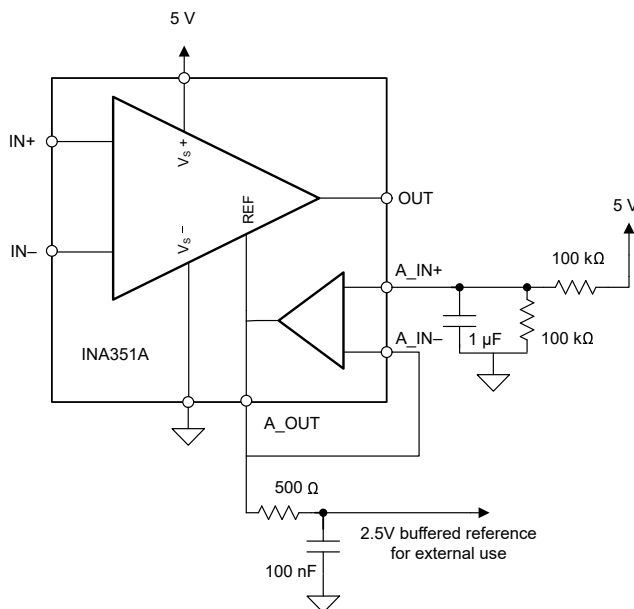
## 9.1 Application Information

### 9.1.1 Reference Amplifier

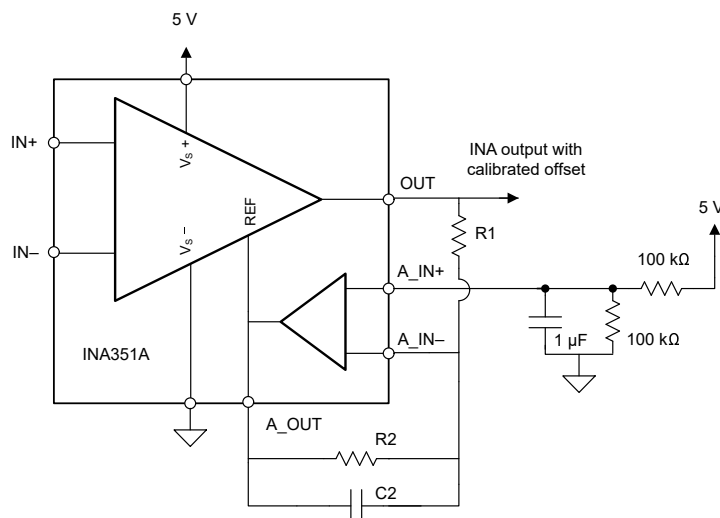
The output voltage of the INA351A is developed with respect to the voltage on the pin A\_OUT. The voltage on the A\_OUT pin sets the common-mode voltage of the instrumentation amplifier OUT pin. In single-supply operation with a bipolar input, setting the output common-mode to a precise mid-supply level is useful and required (for example, 2.75-V in a 5.5-V supply environment) to allow the output signal to swing negative and positive in equal proportions. Traditionally, this is accomplished using a resistive divider from supply and an external reference buffer.

In INA351A, the reference amplifier is integrated on-chip and it is sufficient to only have the resistive divider from supply. With that, the reference amplifier can be connected in  $G = 1$  as shown in [Figure 9-1](#) to provide buffered reference voltage internally to the INA as well as to additional circuits for external use.

Moreover, INA351A has a provision to include servo loop based calibration for external DC offset, drift from the sensor as well as the internal INA offset, drift. This is accomplished using the internal reference amplifier and the three external passive components ( $R_1$ ,  $R_2$ , and  $C_2$ ) as shown in  9-2. The ratio of resistors  $R_2$  with respect to  $R_1$  sets the gain in the calibration loop to attenuate the DC errors at lower frequencies around DC. At higher frequencies, the capacitor,  $C_2$  shorts  $R_2$  to put the reference buffer in  $G = 1$ . This enables the instrumentation amplifier's input differential voltage to influence the INA output at higher frequencies while the reference amplifier in servo loop influences the INA output at lower frequencies around DC. Care should be taken to limit the gain in servo loop so as to maintain sufficient stability. Also, the value of  $C_2$ ,  $R_2$  should be chosen based on the frequency of input signal at the INA input. Now, the resulting residual DC error after calibration would be that of the reference amplifier itself which is minor in comparison to higher DC offset from the instrumentation amplifier, sensor.



### 9-1. INA351A in Reference Buffer Configuration

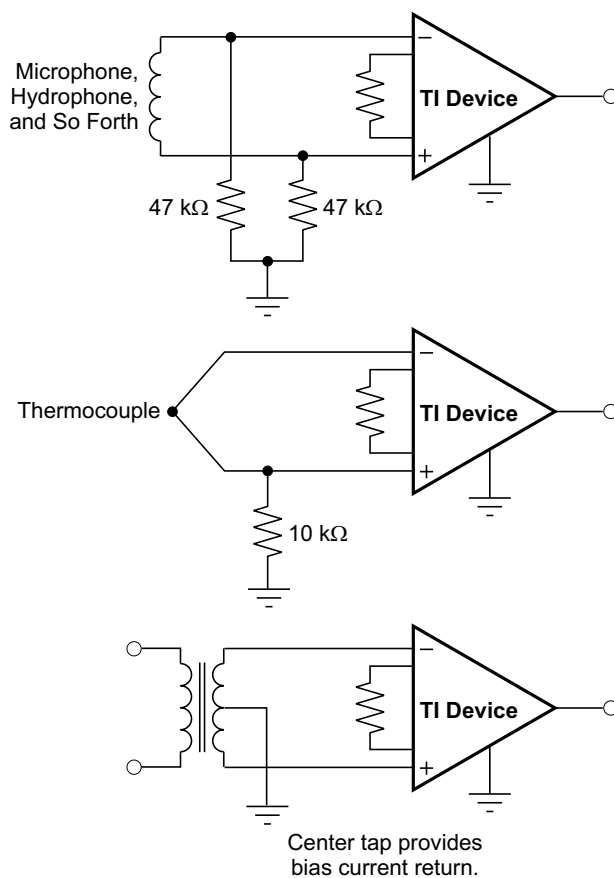


**图 9-2. INA351A in Servo-Loop Calibration Configuration**

### 9.1.2 Input Bias Current Return Path

The input impedance of the INA351A is extremely high, but a path must be provided for the input bias current of both inputs. This input bias current is typically a few pico amps but at high temperature this can be a few nano amps. High input impedance means that the input bias current changes little with varying input voltage.

For proper operation, input circuitry must provide a path for this input bias current. 图 9-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA351A, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path connects to one input (as shown in the thermocouple example in 图 9-3). With a higher source impedance, use two equal resistors to provide a balanced input, with the possible advantages of a lower input offset voltage as a result of bias current, and better high-frequency common-mode rejection.



Copyright © 2017, Texas Instruments Incorporated

### 9-3. Providing an Input Common-Mode Current Path



### 9.2.1.1 Design Requirements

For this application, the design requirements are provided in 表 9-1.

**表 9-1. Design Requirements**

DESCRIPTION	VALUE
Single supply voltage	$V_S = 5.0\text{ V}$
Excitation voltage	$V_{EXT} = 5.0\text{ V}$
Occlusion pressure range	$P = 1\text{ psi to }12\text{ psi, increments of }P = 0.5\text{ psi}$
Occlusion pressure sensitivity	$S = 2 \pm 0.5\text{ (25\%)}\text{ mV/V/psi}$
Occlusion pressure impedance (R)	$R = 4.99\text{ k}\Omega \pm 50\text{ }\Omega\text{ (0.1\%)}$
Total pressure sampling rate	$S_r = 20\text{ Hz}$
ADC supply voltage	$V_{ADC(PS)} = 5.0\text{ V}$
Full-scale range of ADC	$V_{OUT} = 0.25\text{ V to }4.75\text{ V to avoid saturation}$

### 9.2.1.2 Detailed Design Procedure

This section provides basic calculations to lay out the instrumentation amplifier with respect to the given design requirements.

One of the key considerations in resistive-bridge sensors is the common-mode voltage,  $V_{CM}$ . If the bridge is balanced (no pressure, thus no voltage change),  $V_{CM(zero)}$  is half of the bridge excitation ( $V_{EXT}$ ). In this example  $V_{CM(zero)}$  is 2.5 V. For the maximum pressure of 12 psi, the bridge common-mode voltage,  $V_{CM(MAX)}$ , is calculated by:

$$V_{CM(MAX)} = \frac{V_{DIFF}}{2} + V_{CM(zero)} \quad (1)$$

where

$$V_{DIFF} = S_{MAX} \times V_{EXT} \times P_{MAX} = 2.5 \frac{\text{mV}}{\text{V} \times \text{psi}} \times 5\text{ V} \times 12\text{ psi} = 150\text{ mV} \quad (2)$$

Thus, the maximum common-mode voltage applied results in:

$$V_{CM(MAX)} = \frac{150\text{ mV}}{2} + 2.5\text{ V} = 2.575\text{ V} \quad (3)$$

Similarly, the minimum common-mode voltage can be calculated as,

$$V_{CM(MIN)} = \frac{-150\text{ mV}}{2} + 2.5\text{ V} = 2.425\text{ V} \quad (4)$$

The next step is to calculate the gain required for the given maximum sensor output voltage span,  $V_{DIFF}$ , in respect to the required  $V_{OUT}$  swing of maximum 4.75V to avoid saturating the amplifier and the ADC running at 5V supply.

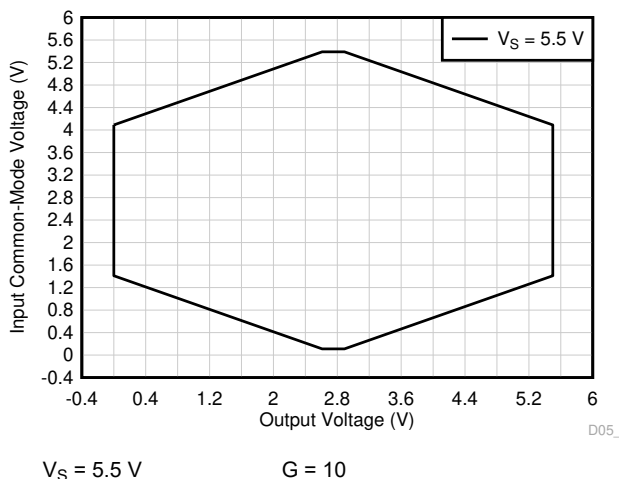
The following equation calculates the gain value using the maximum input voltage and the required output voltage:

$$G = \frac{V_{OUT}}{V_{DIFF(MAX)}} = \frac{2.25\text{ V}}{150\text{ mV}} = 15\text{ V/V} \quad (5)$$

Considering, INA351A is an INA in  $G = 10$ , an additional gain stage in  $G = 1.5$  is added.

Next, let us make sure that the INA351A can operate within this range checking the *Input Common-Mode Voltage vs Output Voltage* curves in the [Typical Characteristics](#) section. The relevant figure is also in this section

for convenience. Looking at [Figure 9-5](#), we can confirm that a output signal swing of 3 V is supported for the input signal swing between 2.425 V and 2.575 V, thus making sure of the linear operation.

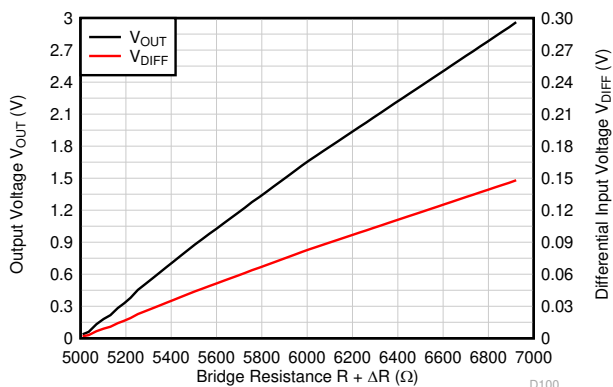


**Figure 9-5. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)**

An additional series resistor in the Wheatstone bridge string ( $R_1$ ) may or may not be required, and can be decided based on the intended output voltage swing for a particular combination of supply voltage, reference voltage and the selected gain for an input common mode voltage range.  $R_1$  helps adjust the input common-mode voltage range, and thus can help accommodate the intended output voltage swing. In this particular example, it is not required and can be shorted out.

### 9.2.1.3 Application Curves

The following typical characteristic curve is for the circuit in [Figure 9-4](#).



**Figure 9-6. Input Differential Voltage, Output Voltage vs Bridge Resistance**

## 9.3 Power Supply Recommendations

The nominal performance of the INA351A is specified with a supply voltage of  $\pm 2.75 \text{ V}$ . The device also operates using power supplies from  $\pm 0.9 \text{ V}$  (1.8 V) to  $\pm 2.75 \text{ V}$  (5.5 V) with excellent performance. Parameters can vary significantly with operating voltage.

## 9.4 Layout

### 9.4.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use the following PCB layout practices:

- Make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals.
- Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Route the input traces as far away from the supply and output traces as possible to reduce parasitic coupling. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the traces as short as possible.

## 9.4.2 Layout Example

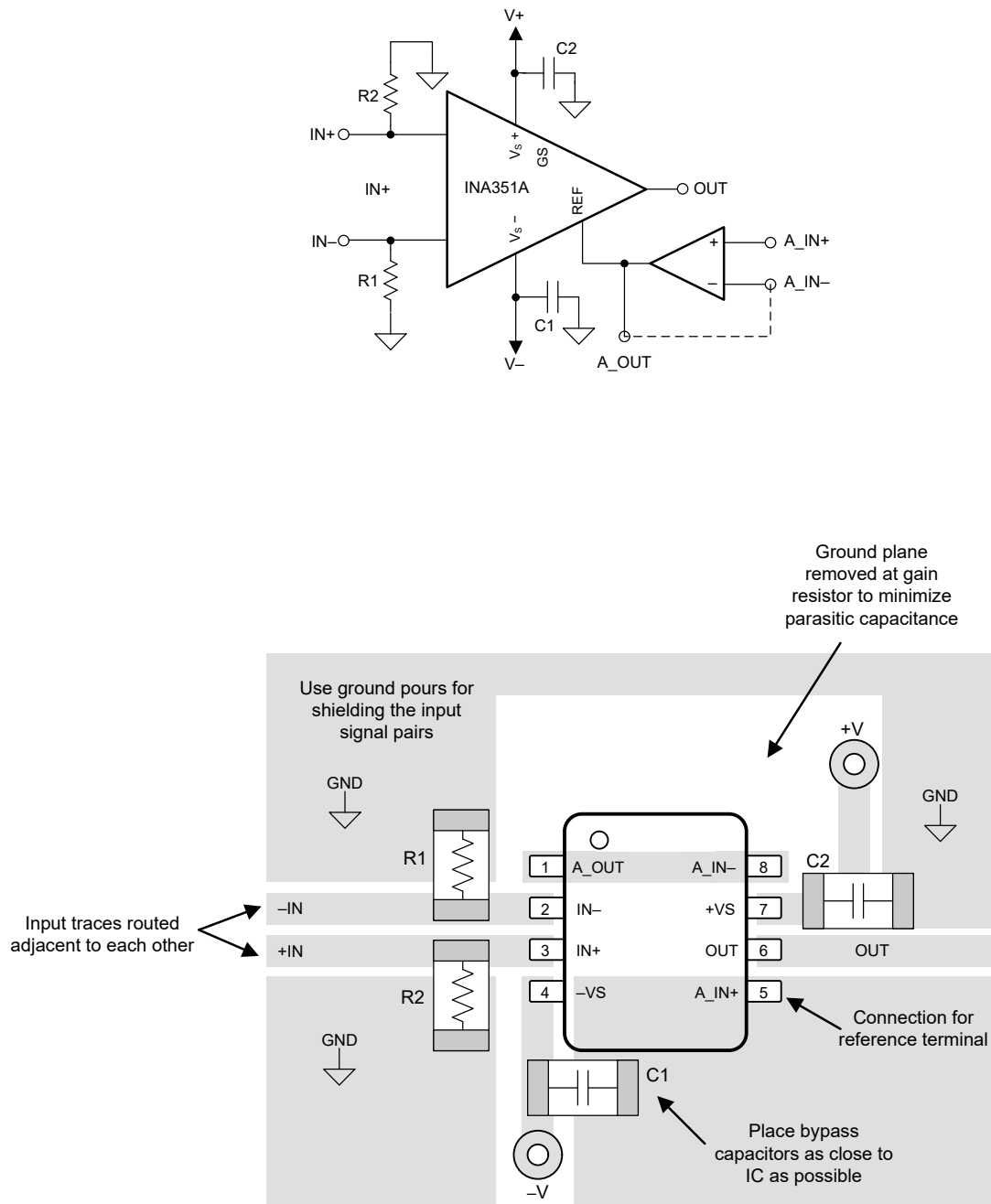


图 9-7. Example Schematic and Associated PCB Layout

## 10 Device and Documentation Support

### 10.1 Device Support

#### 10.1.1 Development Support

- [SPICE-based analog simulation program — TINA-TI software folder](#)
- [Analog Engineers Calculator](#)

##### 10.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

### 10.2 Documentation Support

#### 10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [EMI Rejection Ratio of Operational Amplifiers application report](#)

### 10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 10.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

### 10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

Bluetooth® is a registered trademark of Bluetooth SIG, Inc.

PSpice® is a registered trademark of Cadence Design Systems, Inc.

すべての商標は、それぞれの所有者に帰属します。

### 10.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 10.7 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">INA351AIDSGR</a>	Active	Production	WSO (DSG)   8	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2TSH
INA351AIDSGR.A	Active	Production	WSO (DSG)   8	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2TSH

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## GENERIC PACKAGE VIEW

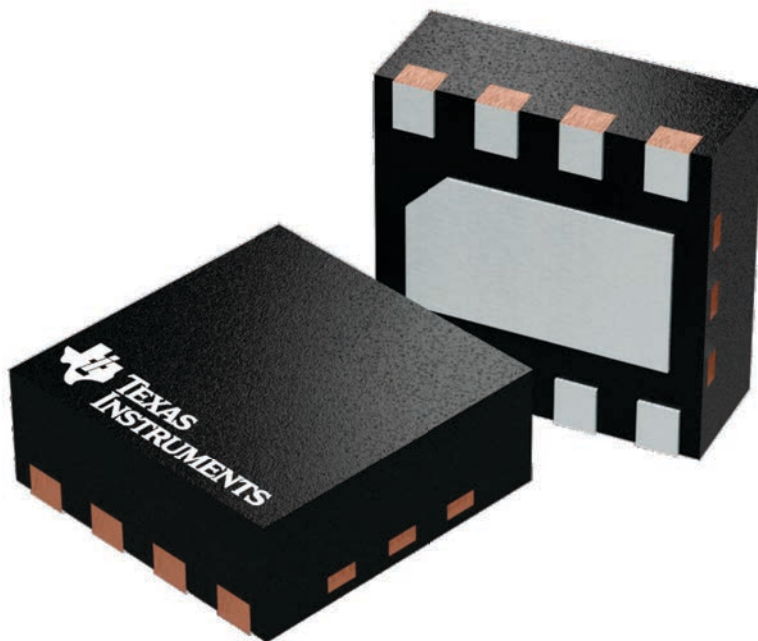
**DSG 8**

**WSON - 0.8 mm max height**

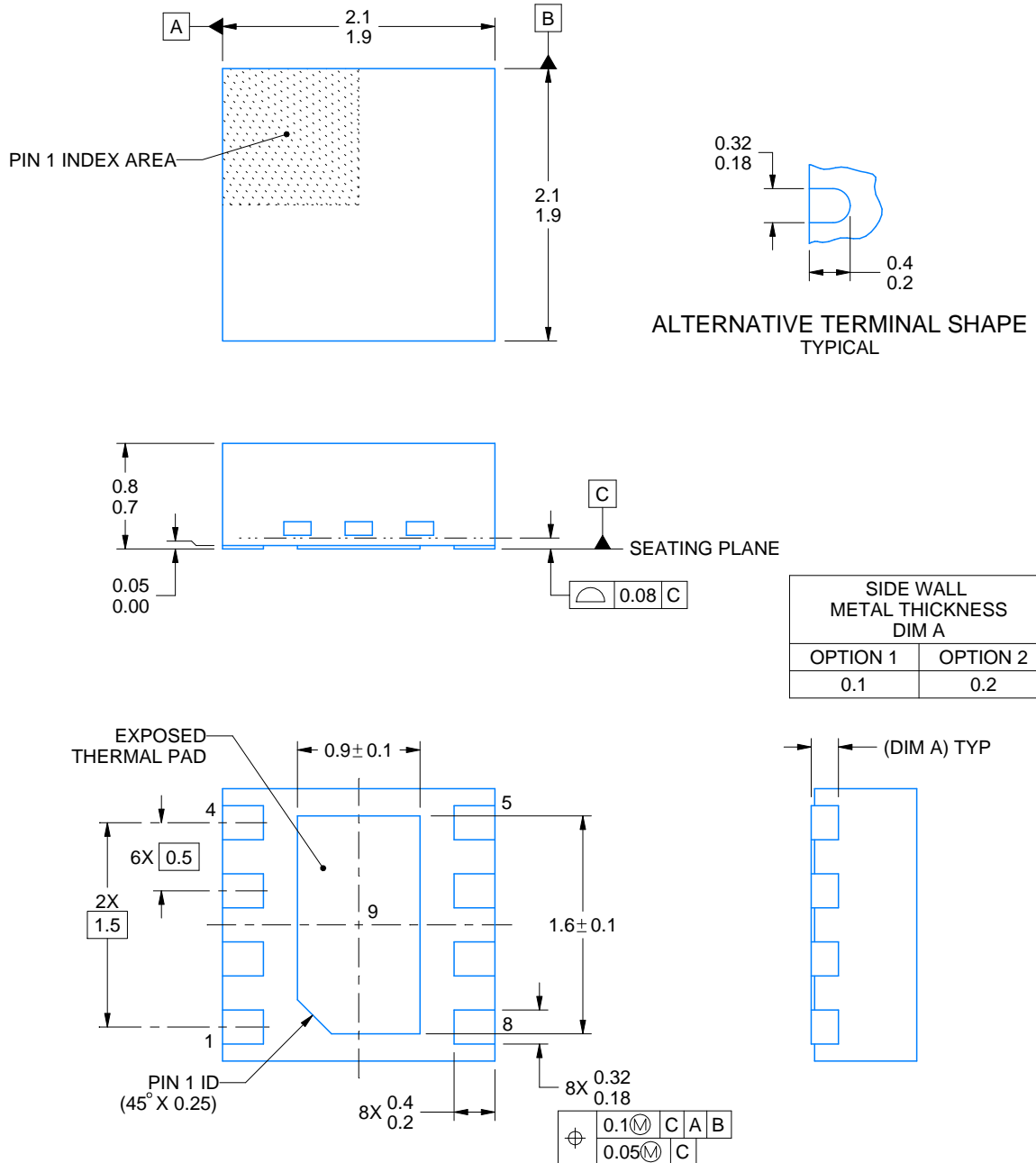
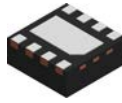
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224783/A



4218900/E 08/2022

## NOTES:

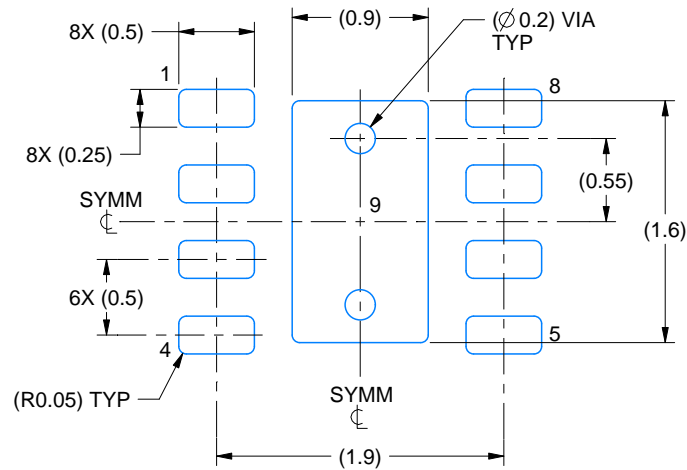
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

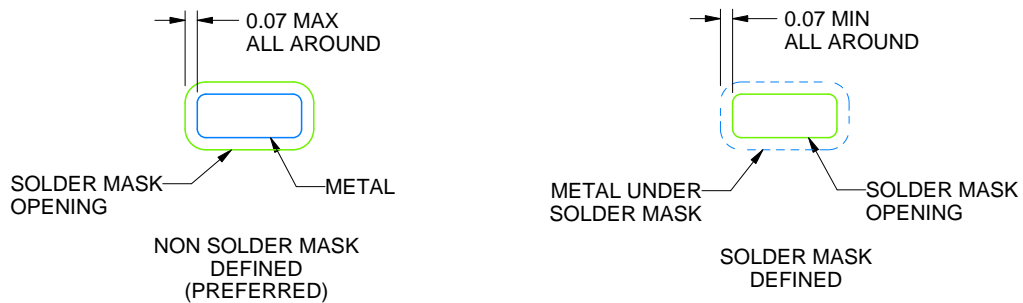
DSG0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

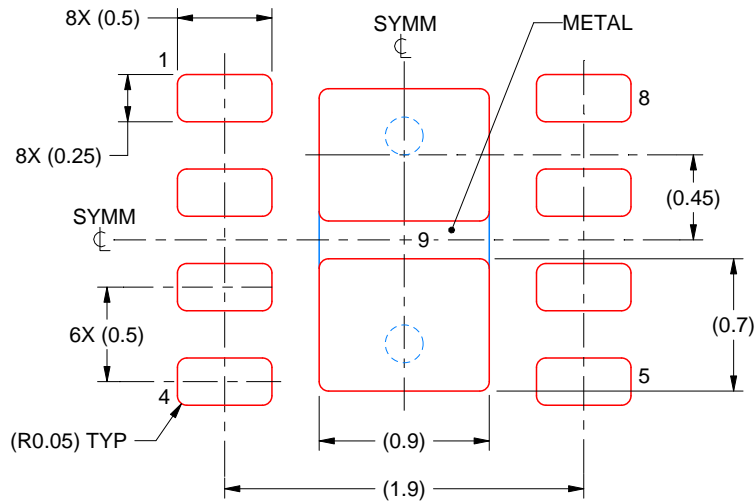
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

DSG0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](https://www.ti.com) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日：2025 年 10 月