

# INA30x-Q1 AEC-Q100、36V、双方向、550kHz、4V/μs、高精度電流センス・アンプ、デュアル・ウィンドウ・コンパレータ内蔵

## 1 特長

- 車載アプリケーション向けに AEC-Q100 認証済み
  - 温度グレード 1:  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$
  - HBM ESD 分類レベル 2
  - CDM ESD 分類レベル C6
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 広い同相入力範囲:  $-0.1\text{V} \sim +36\text{V}$
- デュアル・コンパレータ出力
  - INA302-Q1: 2 つの独立した制限超過アラート
  - INA303-Q1: ウィンドウ・コンパレータ
  - スレッショルド・レベルは個別に設定
  - コンパレータ 1 アラート応答:  $1\mu\text{s}$
  - コンパレータ 2 の調整可能な遅延:  $2\mu\text{s} \sim 10\text{s}$
  - 独立したラッチ制御モードによるオープン・ドレイン出力
- 高精度アンプ
  - オフセット電圧:  $30\mu\text{V}$  (最大値、A3 バージョン)
  - オフセット電圧ドリフト:  $0.5\mu\text{V}/^{\circ}\text{C}$  (最大値)
  - ゲイン誤差:  $0.15\%$  (最大値、A3 バージョン)
  - ゲインの温度特性:  $10\text{ppm}/^{\circ}\text{C}$
- アンプ・ゲインを選択可能
  - INA302A1-Q1, INA303A1-Q1:  $20\text{V}/\text{V}$
  - INA302A2-Q1, INA303A2-Q1:  $50\text{V}/\text{V}$
  - INA302A3-Q1, INA303A3-Q1:  $100\text{V}/\text{V}$

## 2 アプリケーション

- システムのフォルト検出
- モータ制御および保護
- ポンプ制御および保護
- DC/DC コンバータ
- 車体制御モジュール

## 3 概要

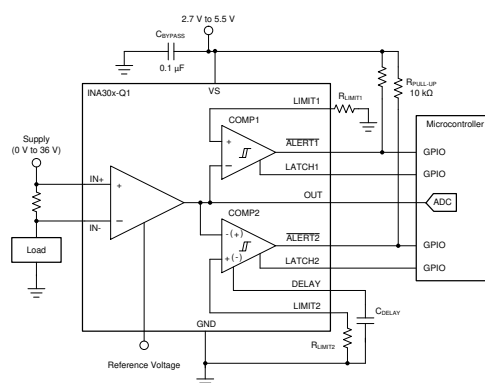
INA302-Q1 および INA303-Q1 (INA30x-Q1) デバイスは、範囲外電流条件を検出するために高コモンモード双方向電流センス・アンプと 2 つの高速コンパレータを備えています。INA302-Q1 コンパレータは、過電流条件を検出し応答するように構成されています。INA303-Q1 コンパレータは、ウィンドウ構成で過電流と低電流の両方の条件に応答するように構成されています。これらのデバイスは、外付けの抵抗を使用して、各コンパレータ・セットについてスレッショルド範囲を設定可能です。これらの電流シャント・モニタは、電源電圧にかかわらず、 $-0.1\text{V} \sim +36\text{V}$  の同相電圧上の差動電圧信号を測定できます。さらに、これらのデバイスは最高  $40\text{V}$  の同相電圧に耐えられます。

オープン・ドレインのアラート出力は、透過モード (出カステータスが入力状態に従う) またはラッチ・モード (ラッチがリセットされるとアラート出力がクリアされる) で動作するように構成できます。コンパレータ 1 のアラート応答時間は  $1\mu\text{s}$  未満であり、コンパレータ 2 のアラート応答は外付けコンデンサにより  $2\mu\text{s} \sim 10\text{s}$  の範囲に設定できます。

これらのデバイスは  $2.7\text{V} \sim 5.5\text{V}$  の単一電源で動作し、最大消費電流は  $950\mu\text{A}$  です。これらのデバイスは、拡張温度範囲の  $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$  で動作が規定されており、14 ピンの TSSOP パッケージで供給されます。

### 製品情報

部品番号	パッケージ	本体サイズ (公称)
INA302-Q1	TSSOP (14)	4.40mm × 5.00mm
INA303-Q1		



代表的なアプリケーション



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## 4 Revision History

Changes from Revision * (March 2019) to Revision A (May 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• 機能安全の箇条書き項目を追加.....	1

## 5 Pin Configuration and Functions

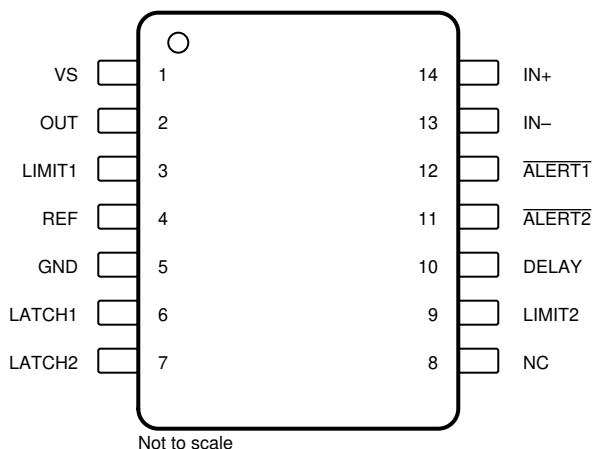


图 5-1. PW Package 14-Pin TSSOP Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VS	Analog	Power supply, 2.7 V to 5.5 V
2	OUT	Analog output	Output voltage
3	LIMIT1	Analog input	ALERT1 threshold limit input; see the <a href="#">Setting Alert Thresholds</a> section for details on setting the limit threshold
4	REF	Analog input	Reference voltage, 0 V to VS
5	GND	Analog	Ground
6	LATCH1	Digital input	Transparent or latch mode selection input
7	LATCH2	Digital input	Transparent or latch mode selection input
8	NC	—	No internal connection
9	LIMIT2	Analog input	ALERT2 threshold limit input; see the <a href="#">Setting Alert Thresholds</a> section for details on setting the limit threshold
10	DELAY	Analog input	Delay timing input; see the <a href="#">Alert Outputs</a> section for details on setting the delayed alert response for comparator 2
11	ALERT2	Analog output	Open-drain output; active-low. This pin is an overlimit alert for the INA302-Q1 and an underlimit alert for the INA303-Q1.
12	ALERT1	Analog output	Open-drain output, active-low overlimit alert
13	IN-	Analog input	Connect to load side of the current-sensing resistor
14	IN+	Analog input	Connect to supply side of the current-sensing resistor

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>S</sub>	Supply voltage			6	V
	Analog inputs (IN+, IN–)	Differential (V <sub>IN+</sub> ) – (V <sub>IN–</sub> ) <sup>(2)</sup>	–40	40	V
		Common-mode <sup>(3)</sup>	GND – 0.3	40	
	Analog input	LIMIT1, LIMIT2, DELAY, REF	GND – 0.3	(V <sub>S</sub> ) + 0.3	V
	Analog output	OUT	GND – 0.3	(V <sub>S</sub> ) + 0.3	V
	Digital input	LATCH1, LATCH2	GND – 0.3	(V <sub>S</sub> ) + 0.3	V
	Digital output	ALERT1, ALERT2	GND – 0.3	6	V
T <sub>J</sub>	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) V<sub>IN+</sub> and V<sub>IN–</sub> are the voltages at the IN+ and IN– pins, respectively.
- (3) Input voltage can exceed the voltage shown without causing damage to the device if the current at that pin is limited to 5 mA.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CM</sub>	Common-mode input voltage	–0.1	12	36	V
V <sub>S</sub>	Operating supply voltage	2.7	5	5.5	V
T <sub>A</sub>	Operating free-air temperature	–40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		INA30x-Q1	UNIT
		PW (TSSOP)	
		14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	110.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	35.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	53.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	52.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 6.5 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_{\text{SENSE}} = 0\text{ V}$ ,  $V_{\text{REF}} = V_S / 2$ ,  $V_S = 5\text{ V}$ ,  $V_{\text{IN}+} = 12\text{ V}$ ,  $V_{\text{LIMIT}1} = 3\text{ V}$ , and  $V_{\text{LIMIT}2} = 3\text{ V}$  (INA302-Q1) or  $2\text{ V}$  (INA303-Q1) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT</b>						
$V_{\text{IN}}$	Differential input voltage range	$V_{\text{IN}} = V_{\text{IN}+} - V_{\text{IN}-}$ , $V_{\text{REF}} = V_S / 2$ , A1 versions	0		$\pm 125$	mV
		$V_{\text{IN}} = V_{\text{IN}+} - V_{\text{IN}-}$ , $V_{\text{REF}} = V_S / 2$ , A2 versions	0		$\pm 50$	
		$V_{\text{IN}} = V_{\text{IN}+} - V_{\text{IN}-}$ , $V_{\text{REF}} = V_S / 2$ , A3 versions	0		$\pm 25$	
CMRR	Common-mode rejection ratio	$V_{\text{IN}+} = 0\text{ V}$ to $36\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , A1 versions	100	114		dB
		$V_{\text{IN}+} = 0\text{ V}$ to $36\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , A2 versions	106	118		
		$V_{\text{IN}+} = 0\text{ V}$ to $36\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , A3 versions	110	120		
$V_{\text{OS}}$	Offset voltage, RTI <sup>(1)</sup>	A1 versions		$\pm 15$	$\pm 80$	$\mu\text{V}$
		A2 versions		$\pm 10$	$\pm 50$	
		A3 versions		$\pm 5$	$\pm 30$	
$dV_{\text{OS}}/dT$	Offset voltage drift, RTI <sup>(1)</sup>	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.02	0.25	$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 2.7\text{ V}$ to $5.5\text{ V}$ , $V_{\text{IN}+} = 12\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		$\pm 0.3$	$\pm 5$	$\mu\text{V}/\text{V}$
$I_B$	Input bias current	$I_{B+}$ , $I_{B-}$		115		$\mu\text{A}$
$I_{\text{OS}}$	Input offset current	$V_{\text{SENSE}} = 0\text{ mV}$		$\pm 0.01$		$\mu\text{A}$
<b>OUTPUT</b>						
G	Gain	A1 versions		20		V/V
		A2 versions		50		
		A3 versions		100		
	Gain error	$V_{\text{OUT}} = 0.5\text{ V}$ to $V_S - 0.5\text{ V}$ , A1 versions		$\pm 0.02\%$	$\pm 0.075\%$	ppm/ $^\circ\text{C}$
		$V_{\text{OUT}} = 0.5\text{ V}$ to $V_S - 0.5\text{ V}$ , A2 versions		$\pm 0.05\%$	$\pm 0.1\%$	
		$V_{\text{OUT}} = 0.5\text{ V}$ to $V_S - 0.5\text{ V}$ , A3 versions		$\pm 0.1\%$	$\pm 0.15\%$	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		3	10	
	Nonlinearity error	$V_{\text{OUT}} = 0.5\text{ V}$ to $V_S - 0.5\text{ V}$		$\pm 0.01\%$		
	Maximum capacitive load	No sustained oscillation		500		pF
<b>VOLTAGE OUTPUT</b>						
	Swing to $V_S$ power-supply rail	$R_L = 10\text{ k}\Omega$ to GND, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		$V_S - 0.05$	$V_S - 0.1$	V
	Swing to GND	$R_L = 10\text{ k}\Omega$ to GND, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		$V_{\text{GND}} + 15$	$V_{\text{GND}} + 30$	mV
<b>FREQUENCY RESPONSE</b>						
BW	Bandwidth	A1 versions, $C_{\text{OUT}} = 500\text{ pF}$		550		kHz
		A2 versions, $C_{\text{OUT}} = 500\text{ pF}$		440		
		A3 versions, $C_{\text{OUT}} = 500\text{ pF}$		400		
SR	Slew rate			4		V/ $\mu\text{s}$
<b>NOISE, RTI<sup>(1)</sup></b>						
	Voltage noise density			30		nV/ $\sqrt{\text{Hz}}$

**INA302-Q1, INA303-Q1**

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at  $T_A = 25^\circ\text{C}$ ,  $V_{\text{SENSE}} = 0\text{ V}$ ,  $V_{\text{REF}} = V_S / 2$ ,  $V_S = 5\text{ V}$ ,  $V_{\text{IN}+} = 12\text{ V}$ ,  $V_{\text{LIMIT}1} = 3\text{ V}$ , and  $V_{\text{LIMIT}2} = 3\text{ V}$  (INA302-Q1) or  $2\text{ V}$  (INA303-Q1) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>COMPARATOR</b>						
$t_p$	Total alert propagation delay	Comparator 1, input overdrive = $1\text{ mV}$		0.6	1	$\mu\text{s}$
		Comparator 2, input overdrive = $1\text{ mV}$ , delay = $100\text{ k}\Omega$ to $V_S$		1.25	2	
	Slew-rate-limited $t_p$	Comparator 1, $V_{\text{OUT}}$ step = $0.5\text{ V}$ to $4.5\text{ V}$ , $V_{\text{LIMIT}} = 4\text{ V}$		1	1.5	$\mu\text{s}$
		Comparator 2 (INA302-Q1), $V_{\text{OUT}}$ step = $0.5\text{ V}$ to $4.5\text{ V}$ , $V_{\text{LIMIT}} = 4\text{ V}$ , delay = $100\text{ k}\Omega$ to $V_S$		1.5	2.5	
		Comparator 2 (INA303-Q1), $V_{\text{OUT}}$ step = $4.5\text{ V}$ to $0.5\text{ V}$ , $V_{\text{LIMIT}} = 1\text{ V}$ , delay = $100\text{ k}\Omega$ to $V_S$		1.5	2.5	
$I_{\text{LIMIT}1}$	Limit threshold output current, comparator 1	$T_A = 25^\circ\text{C}$ , $V_{\text{LIMIT}1} < V_S - 0.6\text{ V}$	79.2	80	80.8	$\mu\text{A}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{\text{LIMIT}1} < V_S - 0.6\text{ V}$	78.4		81.6	
$I_{\text{LIMIT}2}$	Limit threshold output current, comparator 2	$T_A = 25^\circ\text{C}$ , $V_{\text{LIMIT}2} < V_S - 0.6\text{ V}$	79.7	80	80.4	$\mu\text{A}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{\text{LIMIT}2} < V_S - 0.6\text{ V}$	79.2		80.8	
$V_{\text{OS}}$	Offset voltage, both comparators	A1 versions		0.5	3.5	$\text{mV}$
		A2 versions		0.5	3.5	
		A3 versions		0.5	4.0	
HYS	Hysteresis	comparator 1, comparator 2		100		$\text{mV}$
	Internal programmable delay error	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			4%	
$V_{\text{TH}}$	Delay threshold voltage	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	1.21	1.22	1.23	$\text{V}$
$I_D$	Delay charging current	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{\text{DELAY}} = 0.6\text{ V}$	4.85	5	5.15	$\mu\text{A}$
$R_D$	Delay discharge resistance			70		$\Omega$
$V_{\text{IH}}$	LATCH1, LATCH2 high-level input voltage	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	1.4		6	$\text{V}$
$V_{\text{IL}}$	LATCH1, LATCH2 low-level input voltage	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	0		0.4	$\text{V}$
$V_{\text{OL}}$	Alert low-level output voltage	$I_{\text{OL}} = 3\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		70	400	$\text{mV}$
	ALERT1, ALERT2 pin leakage input current	$V_{\text{OH}} = 3.3\text{ V}$		0.1	1	$\mu\text{A}$
	LATCH1, LATCH2 digital leakage input current	$0\text{ V} \leq V_{\text{LATCH}1}, V_{\text{LATCH}2} \leq V_S$		1		$\mu\text{A}$
<b>POWER SUPPLY</b>						
$I_Q$	Quiescent current	$T_A = 25^\circ\text{C}$		850	950	$\mu\text{A}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			1150	

(1) RTI = referred-to-input.

## 6.6 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_{\text{REF}} = V_S / 2$ ,  $V_{\text{SENSE}} = 0\text{ V}$ ,  $V_S = 5\text{ V}$ ,  $V_{\text{IN}+} = 12\text{ V}$ , and  $\overline{\text{ALERT1}}$ ,  $\overline{\text{ALERT2}}$  pullup resistors =  $10\text{ k}\Omega$  (unless otherwise noted)

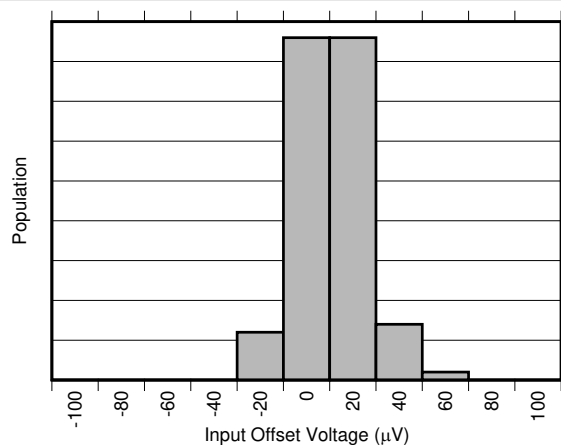


FIG 6-1. Input Offset Voltage Distribution (INA30xA1-Q1)

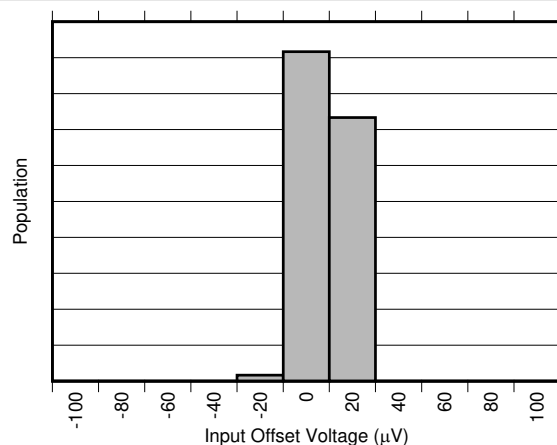


FIG 6-2. Input Offset Voltage Distribution (INA30xA2-Q1)

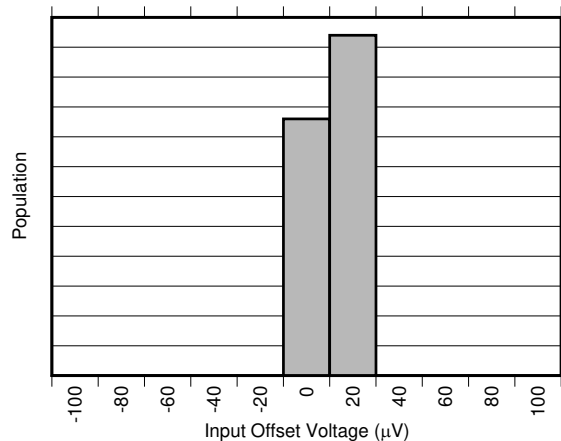


FIG 6-3. Input Offset Voltage Distribution (INA30xA3-Q1)

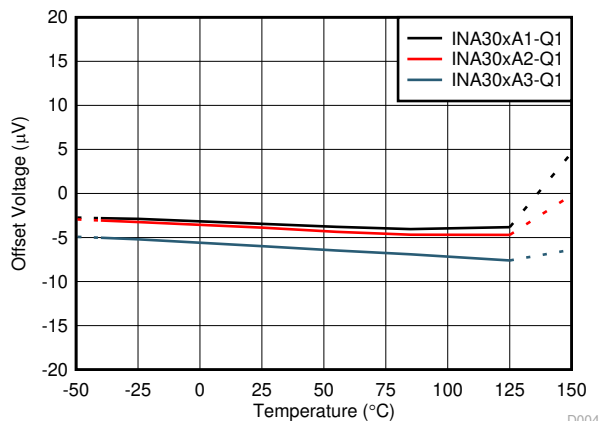


FIG 6-4. Input Offset Voltage vs. Temperature

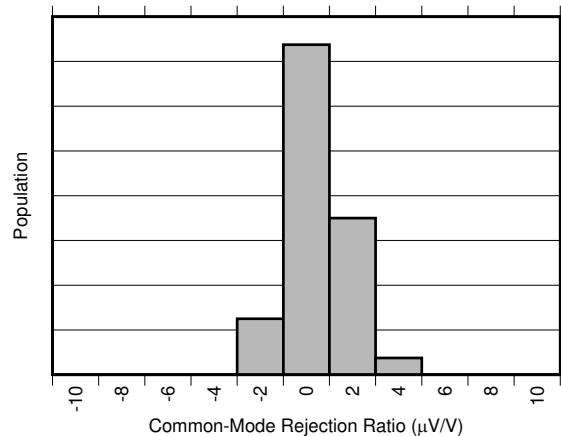


FIG 6-5. CMRR Distribution (INA30xA1-Q1)

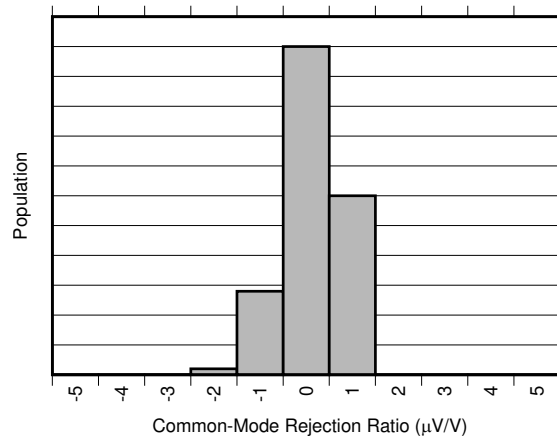


FIG 6-6. CMRR Distribution (INA30xA2-Q1)

## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{\text{REF}} = V_S / 2$ ,  $V_{\text{SENSE}} = 0\text{ V}$ ,  $V_S = 5\text{ V}$ ,  $V_{\text{IN}+} = 12\text{ V}$ , and  $\overline{\text{ALERT1}}$ ,  $\overline{\text{ALERT2}}$  pullup resistors = 10 k $\Omega$  (unless otherwise noted)

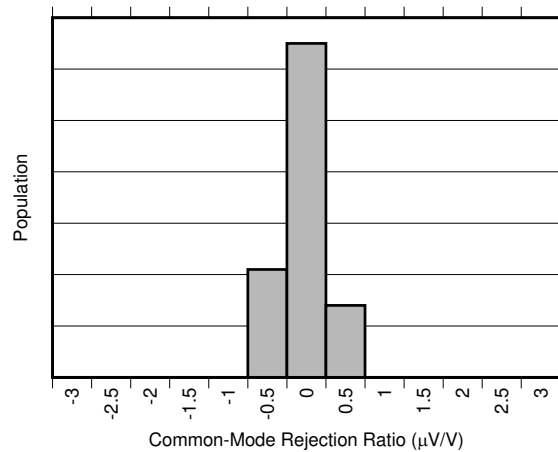


FIG 6-7. CMRR Distribution (INA30xA3-Q1)

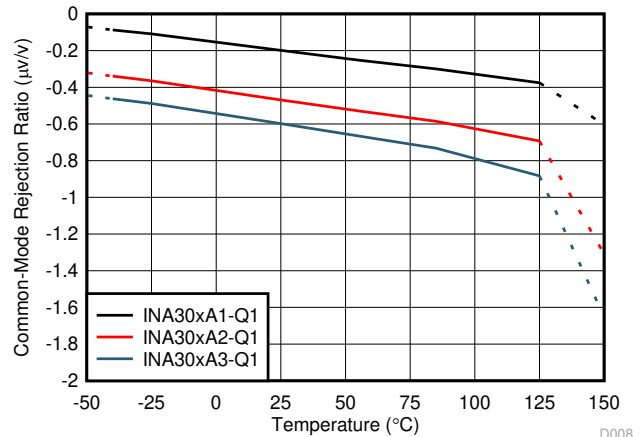


FIG 6-8. CMRR vs. Temperature

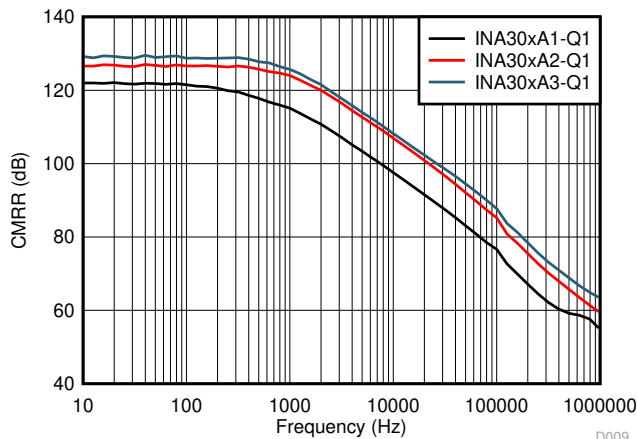


FIG 6-9. CMRR vs. Frequency

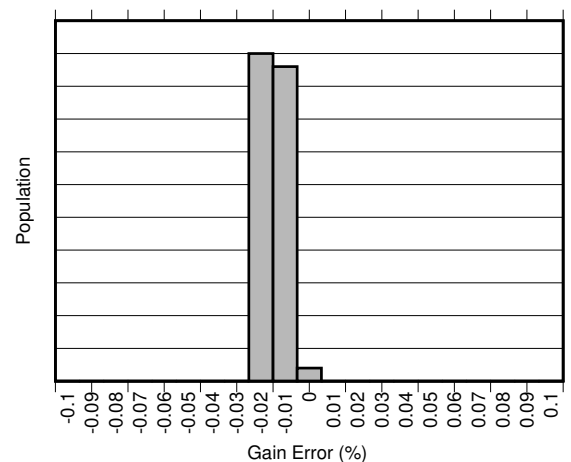


FIG 6-10. Gain Error Distribution (INA30xA1-Q1)

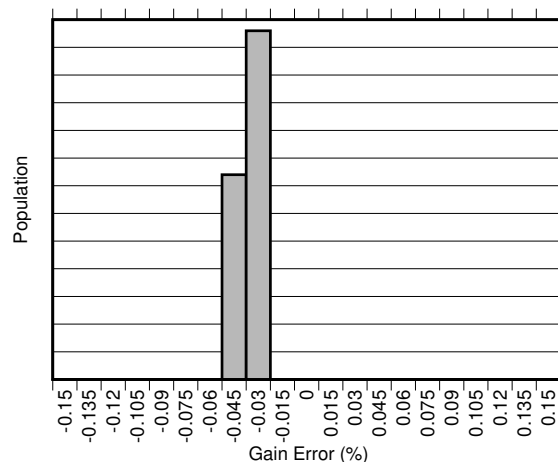


FIG 6-11. Gain Error Distribution (INA30xA2-Q1)

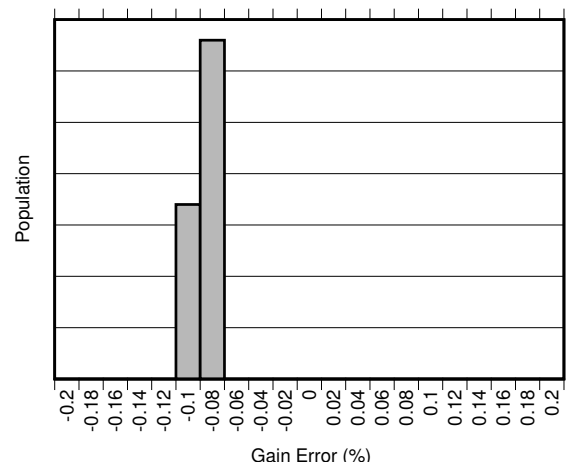


FIG 6-12. Gain Error Distribution (INA30xA3-Q1)



## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{\text{REF}} = V_S / 2$ ,  $V_{\text{SENSE}} = 0\text{ V}$ ,  $V_S = 5\text{ V}$ ,  $V_{\text{IN}+} = 12\text{ V}$ , and  $\overline{\text{ALERT1}}$ ,  $\overline{\text{ALERT2}}$  pullup resistors =  $10\text{ k}\Omega$  (unless otherwise noted)

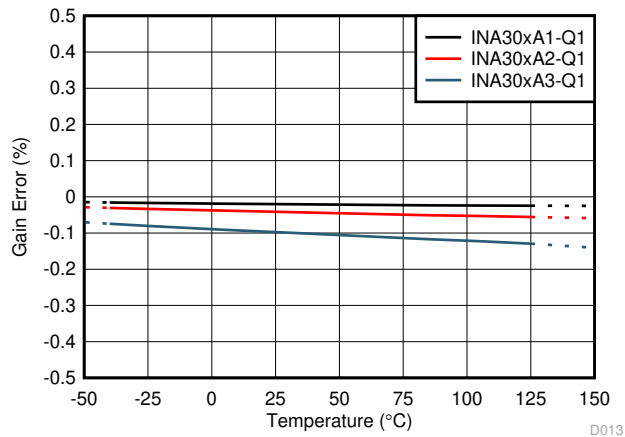


FIG 6-13. Gain Error vs. Temperature

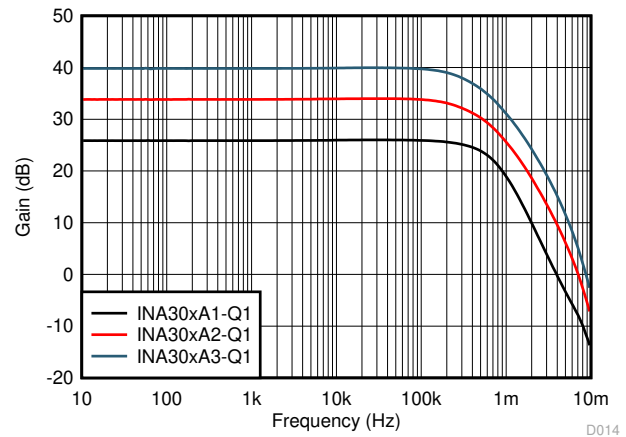


FIG 6-14. Gain vs. Frequency

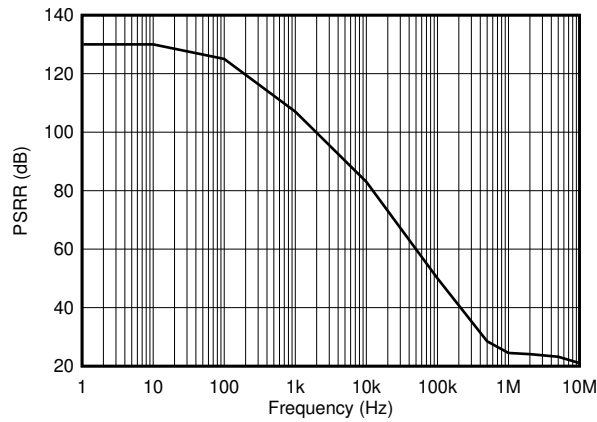


FIG 6-15. PSRR vs. Frequency

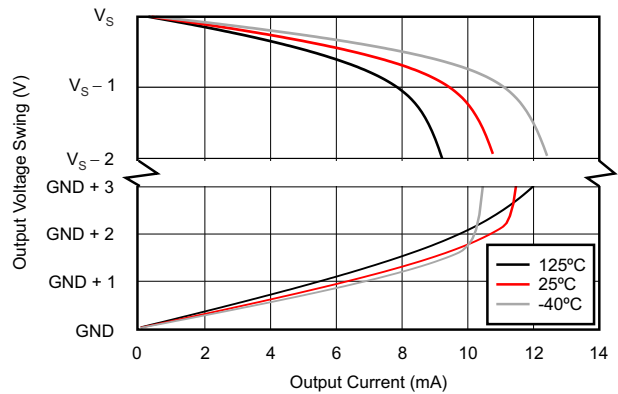


FIG 6-16. Output Voltage Swing vs. Output Current

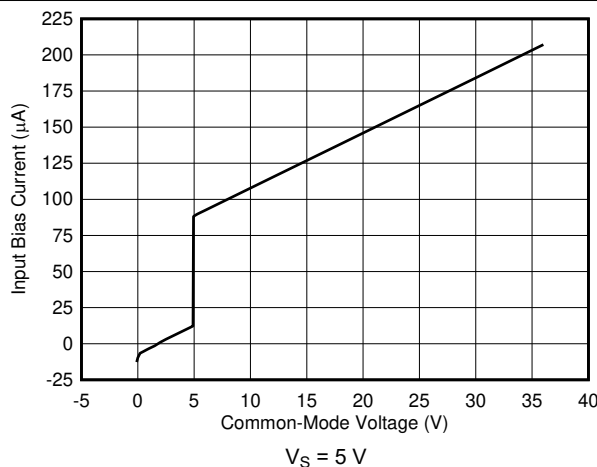


FIG 6-17. Input Bias Current vs. Common-Mode Voltage

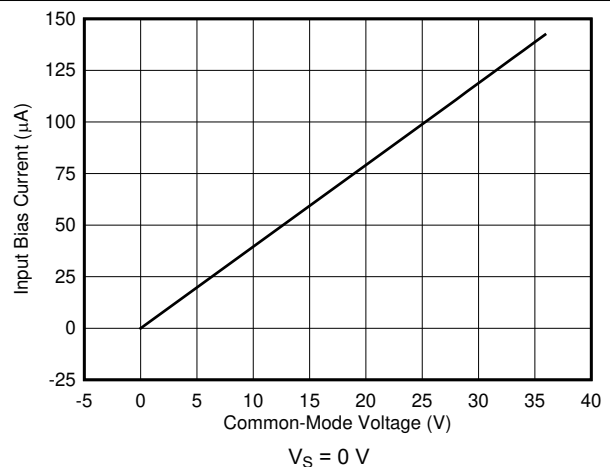


FIG 6-18. Input Bias Current vs. Common-Mode Voltage

## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{\text{REF}} = V_S / 2$ ,  $V_{\text{SENSE}} = 0\text{ V}$ ,  $V_S = 5\text{ V}$ ,  $V_{\text{IN}+} = 12\text{ V}$ , and  $\overline{\text{ALERT1}}$ ,  $\overline{\text{ALERT2}}$  pullup resistors = 10 k $\Omega$  (unless otherwise noted)

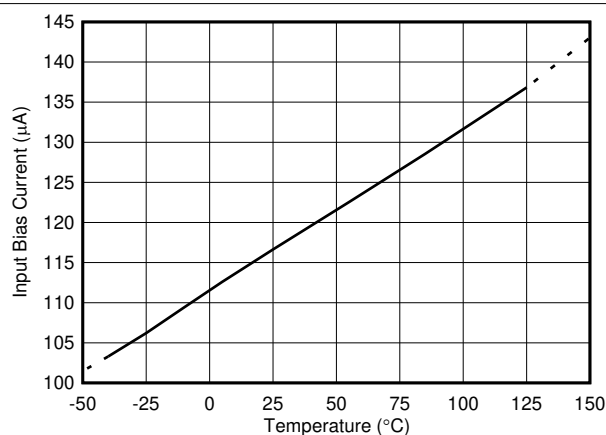


FIG 6-19. Input Bias Current vs. Temperature

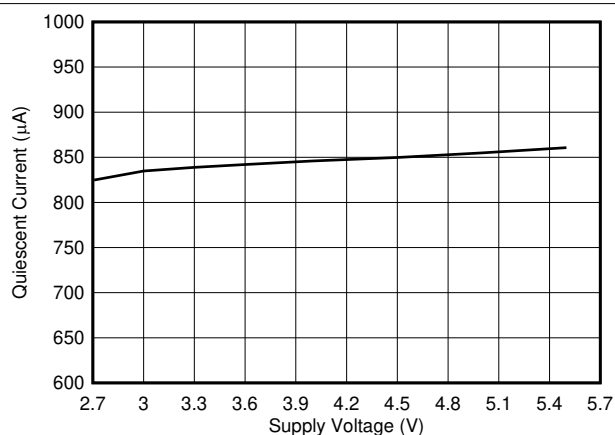


FIG 6-20. Quiescent Current vs. Supply Voltage

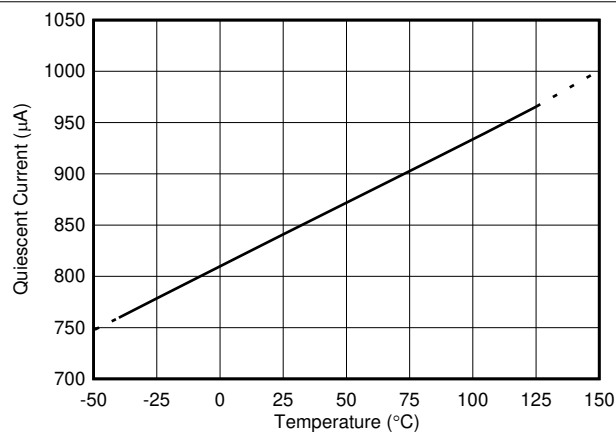


FIG 6-21. Quiescent Current vs. Temperature

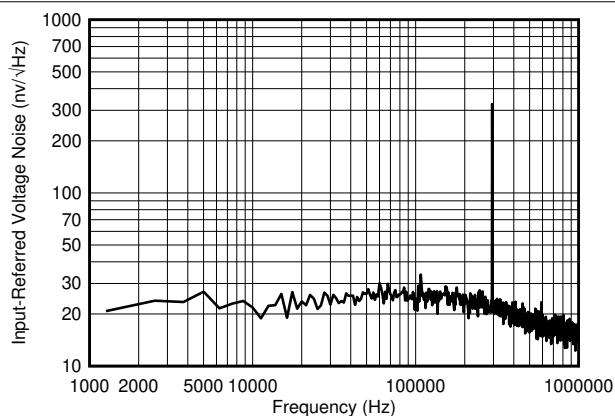


FIG 6-22. Input-Referred Voltage Noise vs. Frequency

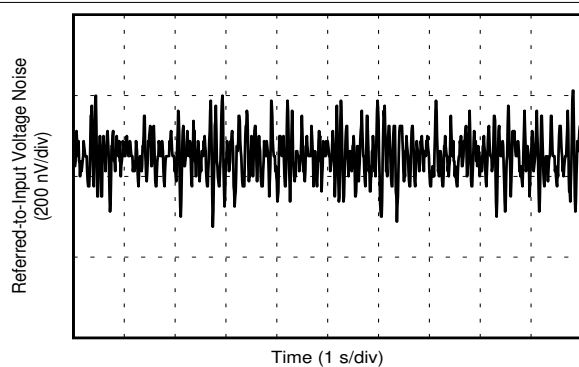


FIG 6-23. 0.1-Hz to 10-Hz Voltage Noise (Referred to Input)

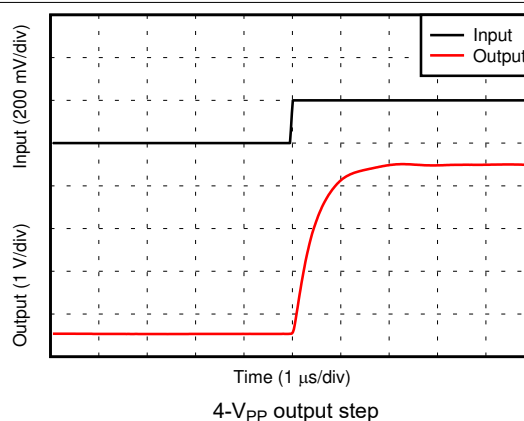


FIG 6-24. Voltage Output Rising Step Response

## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{\text{REF}} = V_S / 2$ ,  $V_{\text{SENSE}} = 0\text{ V}$ ,  $V_S = 5\text{ V}$ ,  $V_{\text{IN}+} = 12\text{ V}$ , and  $\overline{\text{ALERT1}}$ ,  $\overline{\text{ALERT2}}$  pullup resistors =  $10\text{ k}\Omega$  (unless otherwise noted)

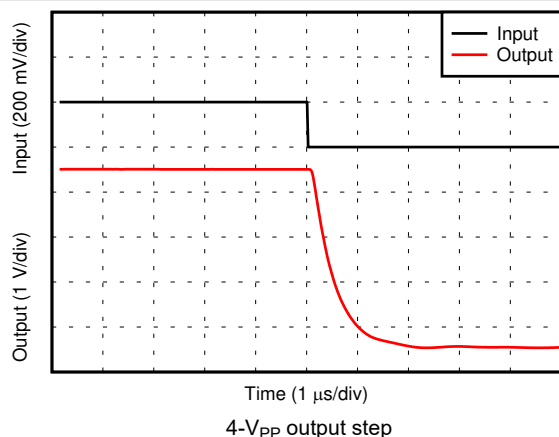


FIG 6-25. Voltage Output Falling Step Response

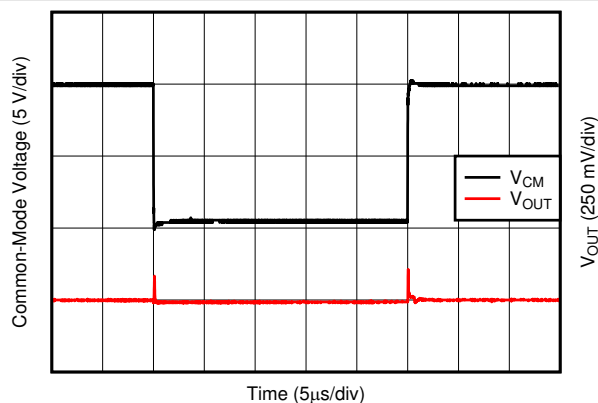


FIG 6-26. Common-Mode Voltage Transient Response

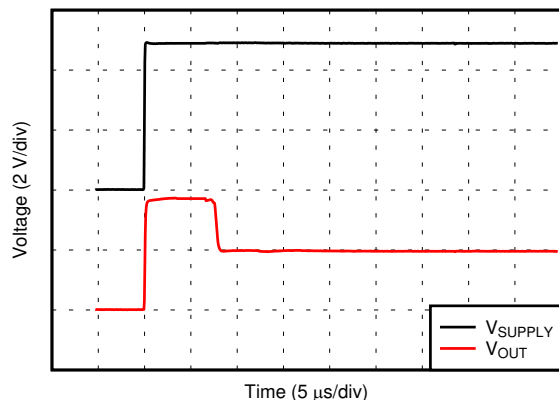


FIG 6-27. Start-Up Response

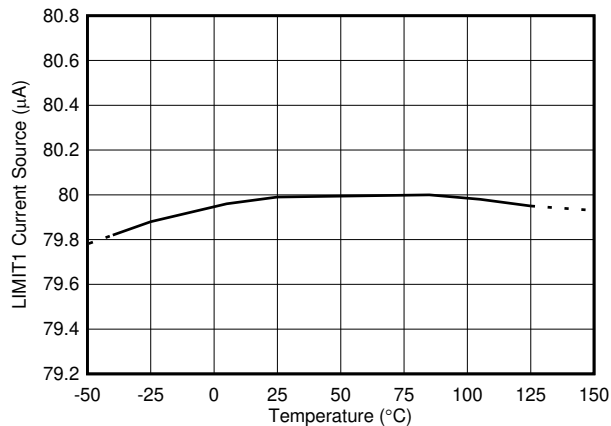


FIG 6-28. LIMIT1 Current Source vs. Temperature

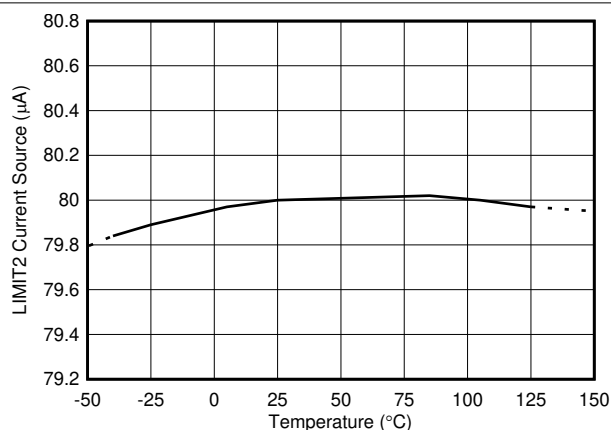


FIG 6-29. LIMIT2 Current Source vs. Temperature

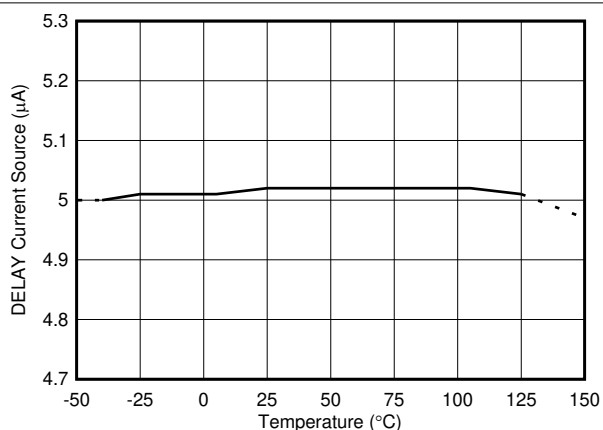
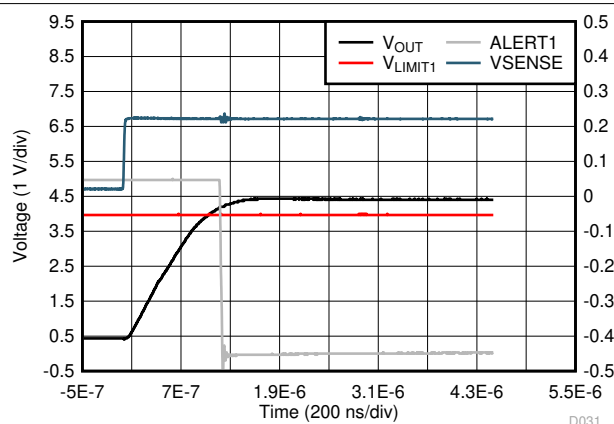


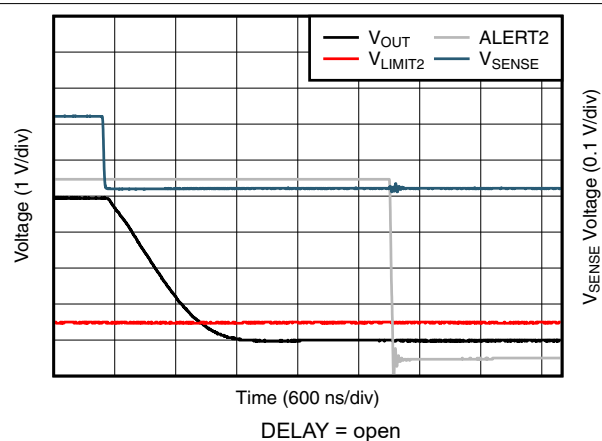
FIG 6-30. DELAY Current vs. Temperature

## 6.6 Typical Characteristics (continued)

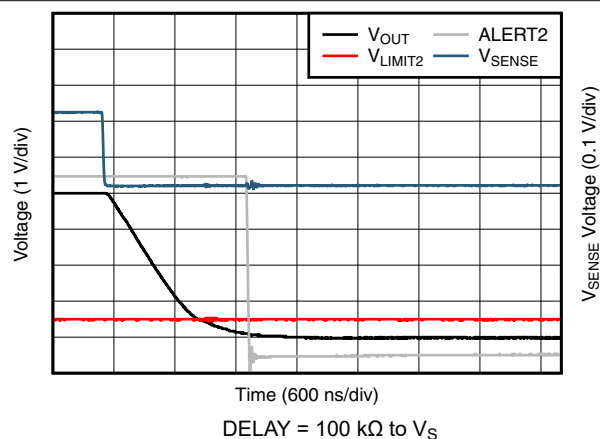
at  $T_A = 25^\circ\text{C}$ ,  $V_{\text{REF}} = V_S / 2$ ,  $V_{\text{SENSE}} = 0\text{ V}$ ,  $V_S = 5\text{ V}$ ,  $V_{\text{IN}+} = 12\text{ V}$ , and  $\overline{\text{ALERT1}}$ ,  $\overline{\text{ALERT2}}$  pullup resistors =  $10\text{ k}\Omega$  (unless otherwise noted)



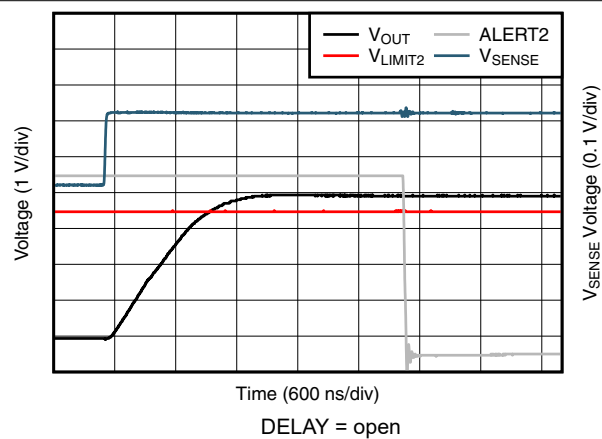
6-31. Comparator 1 Total Propagation Delay (INA30x-Q1)



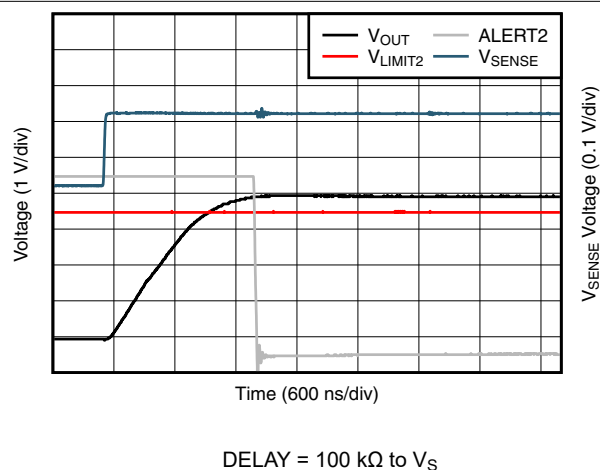
6-32. Comparator 2 Total Propagation Delay (INA303-Q1)



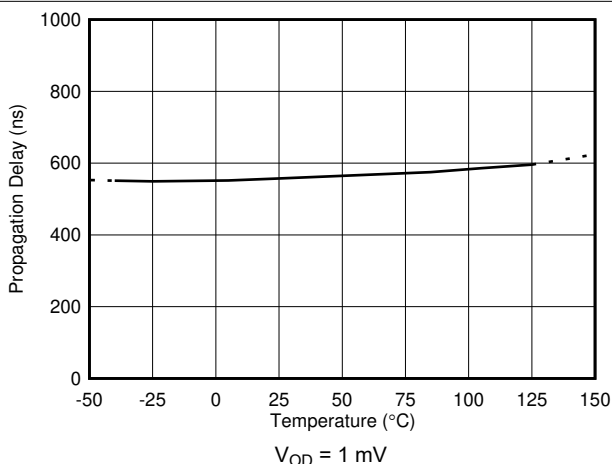
6-33. Comparator 2 Total Propagation Delay (INA303-Q1)



6-34. Comparator 2 Total Propagation Delay (INA302-Q1)



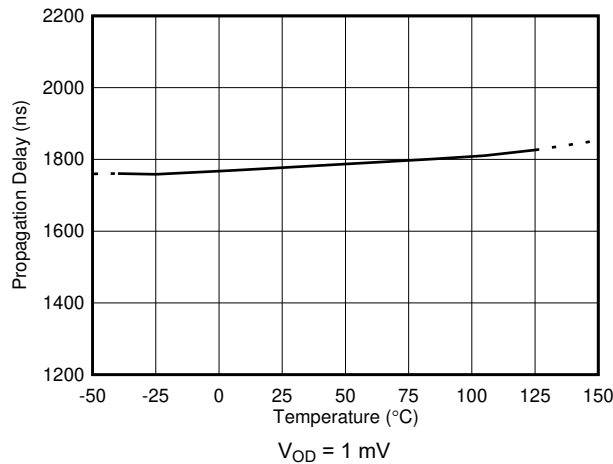
6-35. Comparator 2 Total Propagation Delay (INA302-Q1)



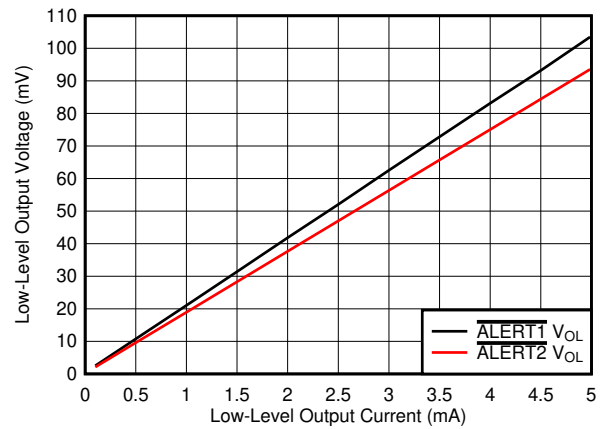
6-36. Comparator 1 Propagation Delay vs. Temperature

## 6.6 Typical Characteristics (continued)

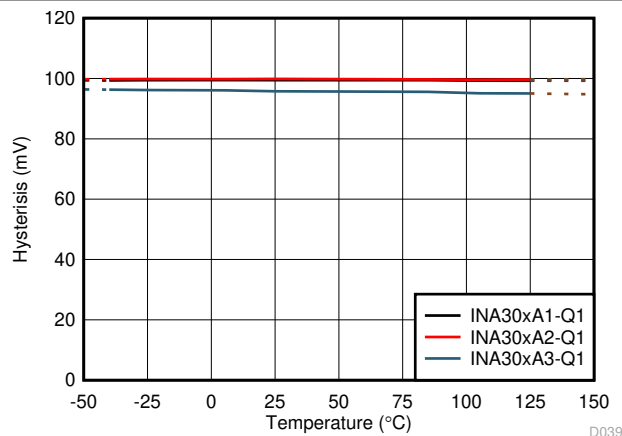
at  $T_A = 25^\circ\text{C}$ ,  $V_{\text{REF}} = V_S / 2$ ,  $V_{\text{SENSE}} = 0\text{ V}$ ,  $V_S = 5\text{ V}$ ,  $V_{\text{IN}+} = 12\text{ V}$ , and  $\overline{\text{ALERT1}}$ ,  $\overline{\text{ALERT2}}$  pullup resistors =  $10\text{ k}\Omega$  (unless otherwise noted)



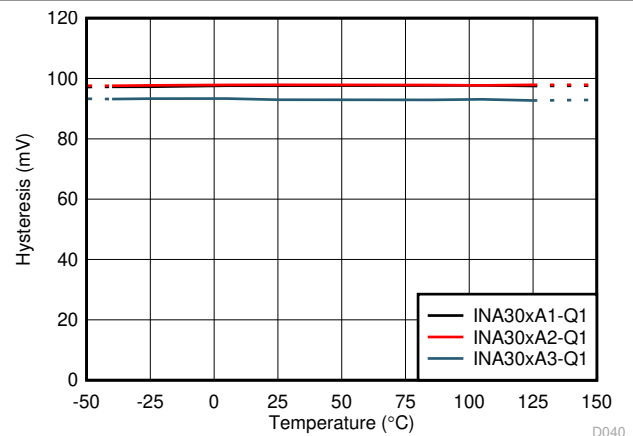
6-37. Comparator 2 Propagation Delay vs. Temperature



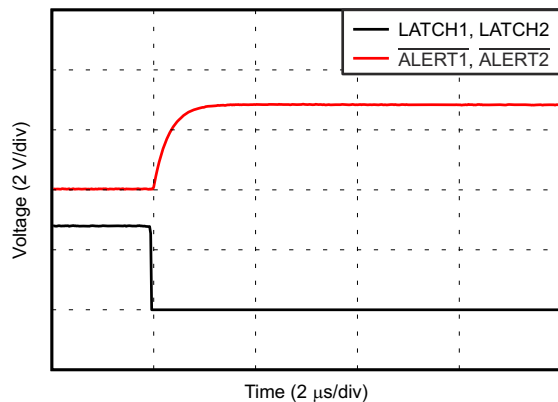
6-38. Comparator Alert  $V_{\text{OL}}$  vs.  $I_{\text{OL}}$



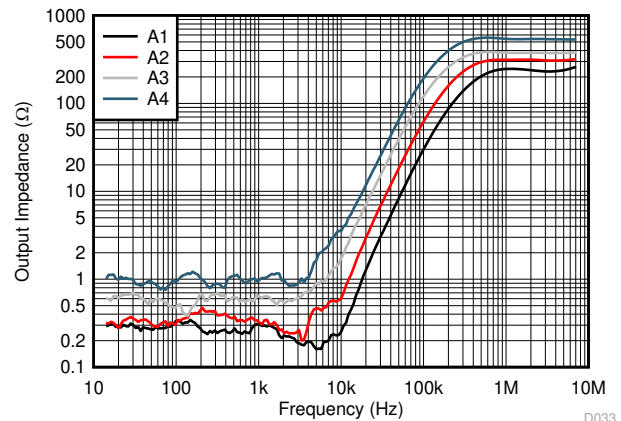
6-39. Comparator 1 Hysteresis vs. Temperature



6-40. Comparator 2 Hysteresis vs. Temperature



6-41. Comparator Latch Response



6-42. Output Impedance vs. Frequency

## 7 Detailed Description

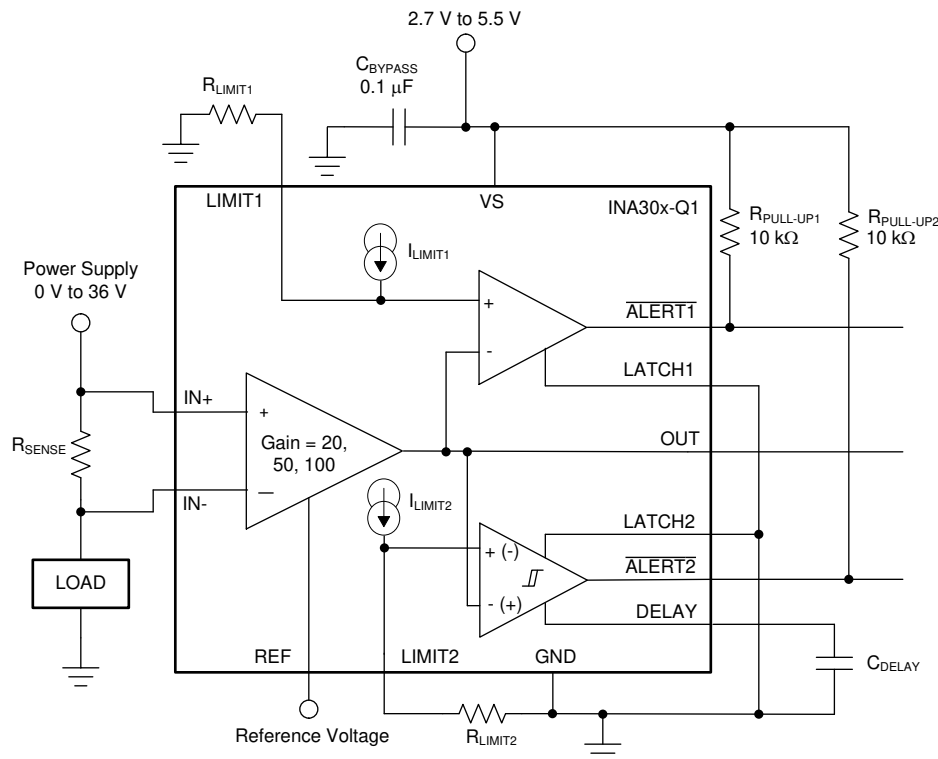
### 7.1 Overview

The INA30x-Q1 feature a zero-drift, 36-V, common-mode, bidirectional, current-sensing amplifier, and two high-speed comparators that can detect multiple out-of-range current conditions. These specially designed, current-sensing amplifiers can be used in both low-side or high-side applications where common-mode voltages far exceed the supply voltage of the device. Currents are measured by accurately sensing voltages developed across current-sensing resistors (also known as *current-shunt resistors*). Current can be measured on input voltage rails as high as 36 V, and the device can be powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 30  $\mu\text{V}$  (max) with a temperature contribution of only 0.25  $\mu\text{V}/^\circ\text{C}$  (max) over the full temperature range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . The low total offset voltage of the INA302-Q1 enables smaller current-sense resistor values to be used, improving power-efficiency without sacrificing measurement accuracy resulting from the smaller input signal.

Both devices use a single external resistor to set each out-of-range threshold. The INA302-Q1 allows for two overcurrent thresholds, and the INA303-Q1 allows for both an undercurrent and overcurrent threshold. The response time of the  $\overline{\text{ALERT1}}$  threshold is fixed and is less than 1  $\mu\text{s}$ . The response time of the  $\overline{\text{ALERT2}}$  threshold can be set with an external capacitor. The combination of a precision current-sense amplifier with onboard comparators creates a highly-accurate solution that is capable of fast detection of multiple out-of-range conditions. The ability to detect when currents are out-of-range allows the system to take corrective actions to prevent potential component or system-wide damage.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Bidirectional Current Sensing

The INA30x-Q1 sense current flow through a sense resistor in both directions. The bidirectional current-sensing capability is achieved by applying a voltage at the REF pin to offset the output voltage. A positive differential voltage sensed at the inputs results in an output voltage that is greater than the applied reference voltage. Likewise, a negative differential voltage at the inputs results in output voltage that is less than the applied reference voltage. The equation for the output voltage of the current-sense amplifier is shown in 式 1.

$$V_{OUT} = (I_{LOAD} \times R_{SENSE} \times GAIN) + V_{REF} \quad (1)$$

where

- $I_{LOAD}$  is the load current to be monitored.
- $R_{SENSE}$  is the current-sense resistor.
- $GAIN$  is the gain option of the device selected.
- $V_{REF}$  is the voltage applied to the REF pin.

### 7.3.2 Out-of-Range Detection

The INA303-Q1 detects when negative currents are out-of-range by setting a voltage at the LIMIT2 pin that is less than the applied reference voltage. The limit voltage is set with an external resistor or externally driven by a voltage source or digital-to-analog converter (DAC); see the [Setting Alert Thresholds](#) section for additional information. A typical application using the INA303-Q1 to detect negative overcurrent conditions is illustrated in the [Typical Application](#) section.

### 7.3.3 Alert Outputs

Both  $\overline{ALERTx}$  pins are active-low, open-drain outputs that pull low when the sensed current is detected to be out of range. Both open-drain  $\overline{ALERTx}$  pins require an external pullup resistor to an external supply. The external supply for the pullup voltage can exceed the supply voltage,  $V_S$ , but is restricted from operating at greater than 5.5 V. The pullup resistance is selected based on the capacitive load and required rise time; however, a 10-k $\Omega$  resistor value is typically sufficient for most applications. The response time of the  $\overline{ALERT1}$  output to an out-of-range event is less than 1  $\mu$ s, and the response time of the  $\overline{ALERT2}$  output is proportional to the value of the external  $C_{DELAY}$  capacitor. The equation to calculate the delay time for the  $\overline{ALERT2}$  output is given in 式 2:

$$t_{DELAY} = \begin{cases} 1.5 \mu s & \text{If DELAY is connected to VS with 100 k}\Omega \\ \frac{C_{DELAY} \times V_{TH}}{I_D} + 2.5 \mu s & \text{If } C_{DELAY} \geq 47 \text{ pF} \end{cases} \quad (2)$$

where

- $C_{DELAY}$  is the external delay capacitor.
- $V_{TH}$  is the delay threshold voltage.
- $I_D$  is the DELAY pin current for comparator 2.

For example, if a delay time of 10  $\mu$ s is desired, the calculated value for  $C_{DELAY}$  is 30.7 pF. The closest standard capacitor value to the calculated value is 30 pF. If a delay time greater than 2.5  $\mu$ s on the  $\overline{ALERT2}$  output is not needed, the  $C_{DELAY}$  capacitor can be omitted. To achieve minimum delay on the  $\overline{ALERT2}$  output, connect a 100-k $\Omega$  resistor from the DELAY pin to the VS pin. Both comparators in the INA30x-Q1 have hysteresis to avoid oscillations in the  $\overline{ALERTx}$  outputs. The effect hysteresis has on the comparator behavior is described in the [Hysteresis](#) section.

Figure 7-1 shows the alert output response of the internal comparators for the INA302-Q1. When the output voltage of the current-sense amplifier is less than the voltage developed on either limit pin, both  $\overline{\text{ALERTx}}$  outputs are in the default high state. When the current sense amplifier output is greater than the threshold voltage set by the LIMIT2 pin, the  $\overline{\text{ALERT2}}$  output pulls low after a delay time set by the external delay capacitor. The lower overcurrent threshold is commonly referred to as the *overcurrent warning threshold*. If the current continues to rise until the current-sense amplifier output voltage exceeds the threshold voltage set at the LIMIT1 pin, then the  $\overline{\text{ALERT1}}$  output becomes active and immediately pulls low. The low voltage on  $\overline{\text{ALERT1}}$  indicates that the measured signal at the amplifier input has exceeded the programmed threshold level, indicating an overcurrent condition has occurred. The upper threshold is commonly referred to as the *fault or system critical threshold*. Systems often initiate protection procedures (such as a system shutdown) when the current exceeds this threshold.

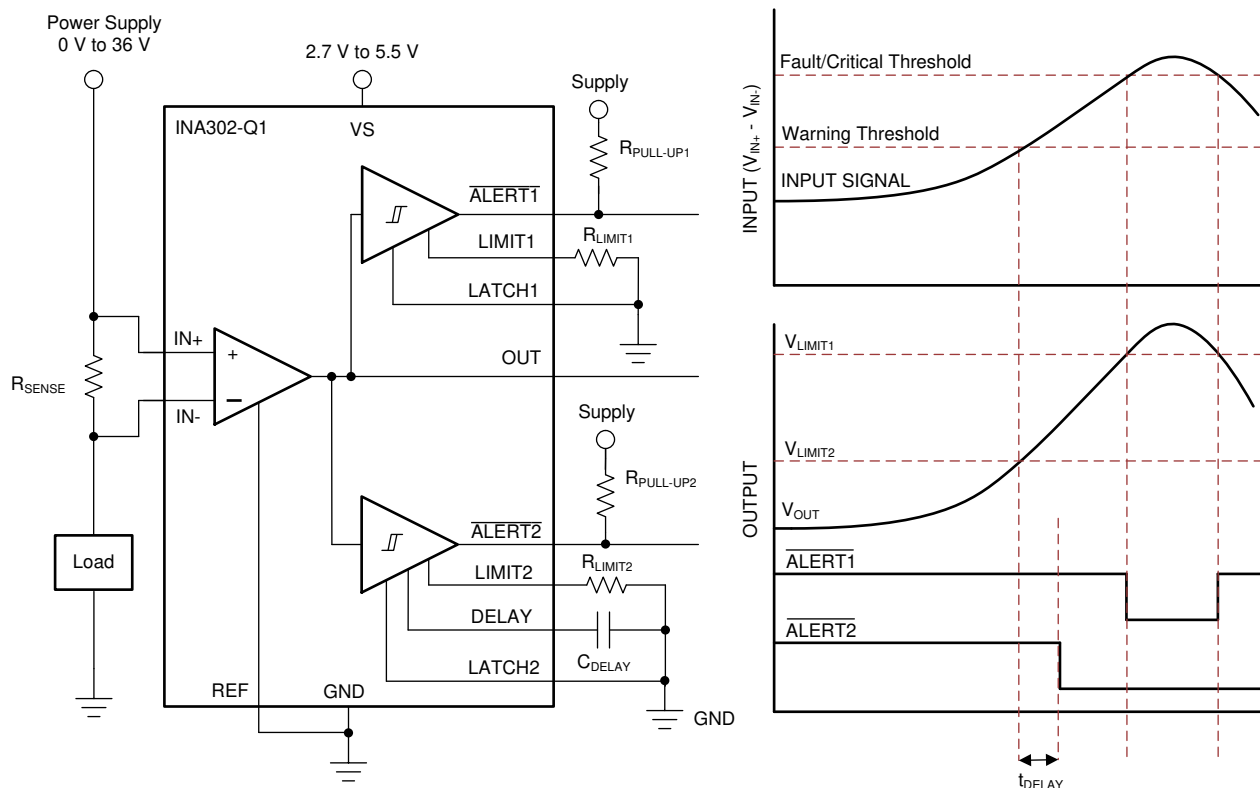
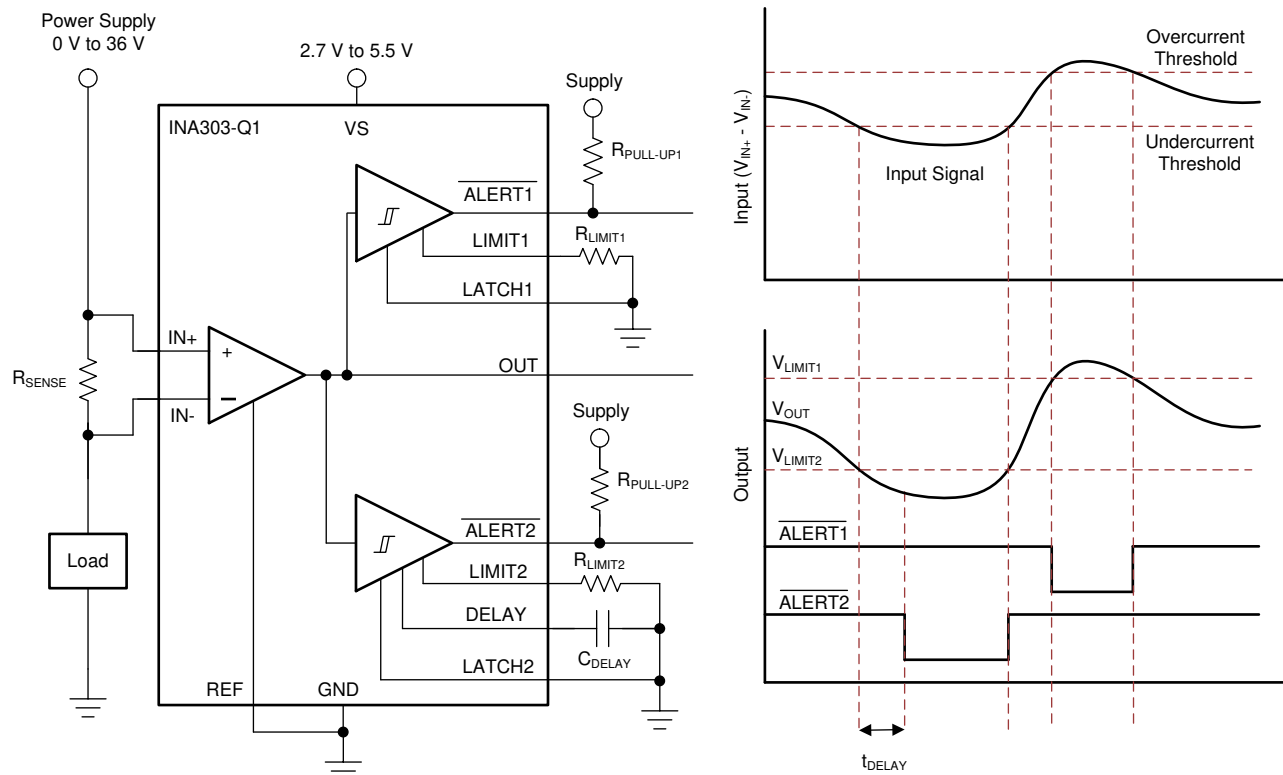


Figure 7-1. Out-of-Range Alert Responses for the INA302-Q1

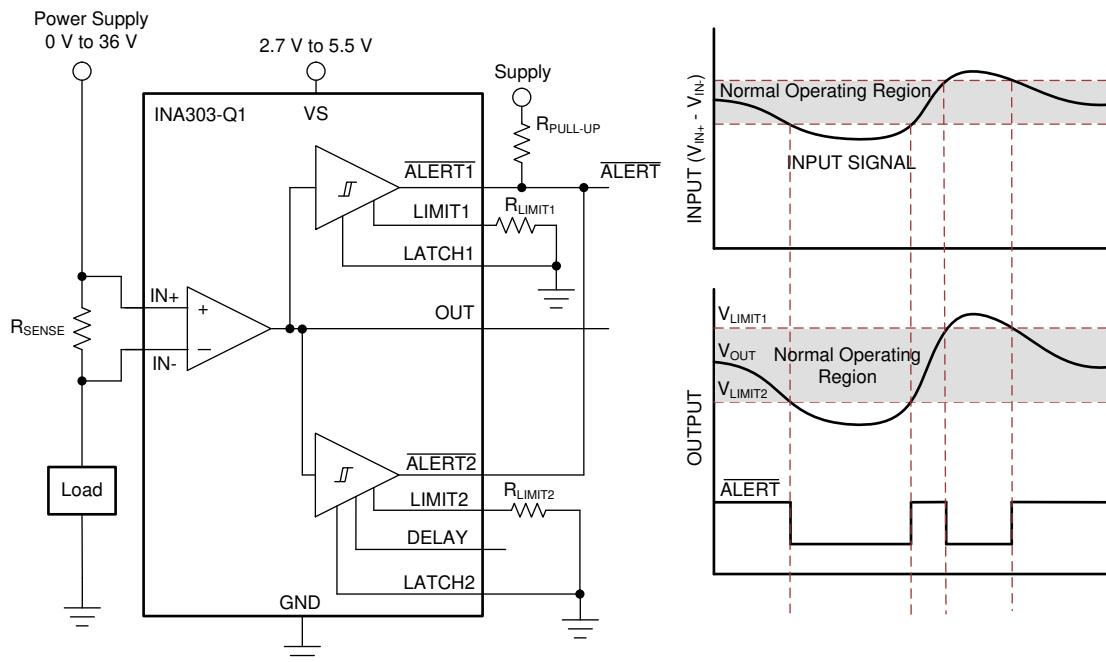


Figure 7-2 shows the alert output response of the internal comparators for the INA303-Q1. Both  $\overline{\text{ALERTx}}$  outputs are in the default high state when the output voltage of the current-sense amplifier is less than the voltage developed at the LIMIT1 pin and is greater than the voltage developed at the LIMIT2 pin. The  $\overline{\text{ALERT1}}$  output becomes active and pulls low when the current-sense amplifier output voltage exceeds the threshold voltage set at the LIMIT1 pin. The low voltage on  $\overline{\text{ALERT1}}$  indicates that the measured signal at the amplifier input has exceeded the programmed threshold level, indicating an overcurrent or out-of-range condition has occurred. When the current-sense amplifier output is less than the threshold voltage set by the LIMIT2 pin, the  $\overline{\text{ALERT2}}$  output pulls low after the delay time set by the external delay capacitor expires. The delay time for the  $\overline{\text{ALERT2}}$  output is proportional to the value of the external  $C_{\text{DELAY}}$  capacitor, and is calculated by Equation 2.



**Figure 7-2. Out-of-Range Alert Responses for the INA303-Q1**

Figure 7-3 shows the alert output response of the INA303-Q1 when the two  $\overline{\text{ALERTx}}$  pins are connected together. When configured in this manner, the INA303-Q1 can provide a single signal to indicate when the sensed current is operating either outside the normal operating bands or within a normal operational window. Both  $\overline{\text{ALERT1}}$  and  $\overline{\text{ALERT2}}$  outputs behave the same in regard to the alert mode. The difference with  $\overline{\text{ALERT2}}$  is that the transition of the output state is delayed by the time set by the external delay capacitor. If the overcurrent or undercurrent event is not present when the delay time expires,  $\overline{\text{ALERT2}}$  does not respond.



### 7-3. Current Window Comparator Implementation With the INA303-Q1

### 7.3.3.1 Setting Alert Thresholds

The INA30x-Q1 family of devices determines if an out-of-range event is present by comparing the amplifier output voltage to the voltage at the corresponding LIMITx pin. The threshold voltage for the LIMITx pins can be set using a single external resistor or by connecting an external voltage source to each pin. The INA302-Q1 allows setting limits for two overcurrent conditions. Generally, the lower overcurrent threshold is referred to as a *warning limit* and the higher overcurrent threshold is referred to as the *critical* or *fault limit*. The INA303-Q1 allows setting thresholds to detect both undercurrent and overcurrent limit conditions.

#### 7.3.3.1.1 Resistor-Controlled Current Limit

The typical approach to set the limit threshold voltage is to connect resistors from the two LIMITx pins to ground. The voltage developed across the  $R_{LIMIT1}$ ,  $R_{LIMIT2}$  resistors represents the desired fault current value at which the corresponding ALERTx pin becomes active. The values for the  $R_{LIMIT1}$ ,  $R_{LIMIT2}$  resistors are calculated using 式 3:

$$R_{LIMIT} = \frac{(I_{TRIP} \times R_{SENSE} \times GAIN) + V_{REF}}{I_{LIMIT}} \quad (3)$$

where

- $I_{TRIP}$  is the desired out-of-range current threshold.
- $R_{SENSE}$  is the current-sensing resistor.
- $GAIN$  is the gain option of the device selected.
- $V_{REF}$  is the voltage applied to the REF pin.
- $I_{LIMIT}$  is the limit threshold output current for the selected comparator, typically 80  $\mu$ A.

#### Note

When solving for the value of  $R_{LIMIT}$ , the voltage at the corresponding LIMITx pin as determined by the product of  $R_{LIMIT}$  and  $I_{LIMIT}$  must not exceed the compliance voltage of  $V_S - 0.6$  V.

#### 7.3.3.1.1.1 Resistor-Controlled Current Limit: Example

For example, if the current level indicating an out-of-range condition ( $I_{TRIP}$ ) is 20 A and the current-sense resistor value ( $R_{SENSE}$ ) is 10 m $\Omega$ , then the input threshold signal is 200 mV. The INA302A1-Q1 has a gain of 20, so the resulting output voltage at the 20-A input condition is 4 V at the output of the current-sense amplifier when the REF pin is grounded. The value for  $R_{LIMIT}$  is selected to allow the device to detect this 20-A threshold, indicating that an overcurrent event has occurred. When the INA302-Q1 detects this out-of-range condition, the ALERTx pin asserts and pulls low. For this example, the value of  $R_{LIMIT}$  to detect a 4-V level is calculated to be 50 k $\Omega$ .

### 7.3.3.1.2 Voltage-Source-Controlled Current Limit

The second method for setting the out-of-range threshold is to directly drive the LIMITx pins with a programmable DAC or other external voltage source. The benefit of this method is the ability to adjust the current-limit threshold to account for different threshold voltages used for different system operating conditions. For example, this method can be used in a system with one current-limit threshold level that must be monitored during a power-up sequence, but different threshold levels must be monitored during other system operating modes.

The voltage applied at the LIMITx pins sets the threshold voltage for out-of-range detection. The value of the voltage for a given desired current trip point is calculated using 式 4:

$$V_{\text{SOURCE}} = (I_{\text{TRIP}} \times R_{\text{SENSE}} \times \text{GAIN}) + V_{\text{REF}} \quad (4)$$

where

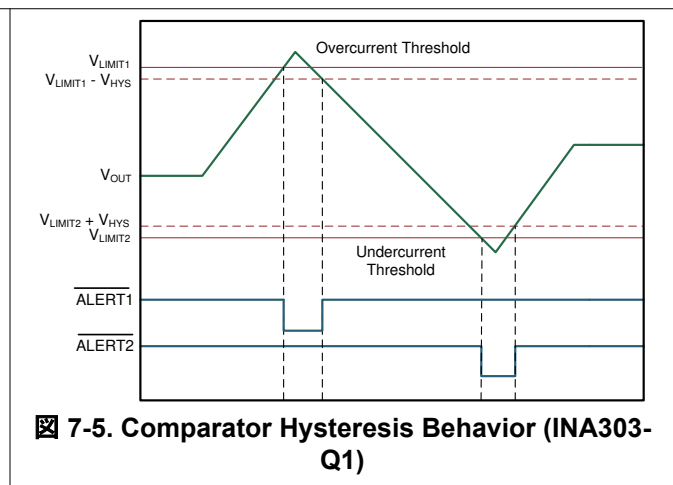
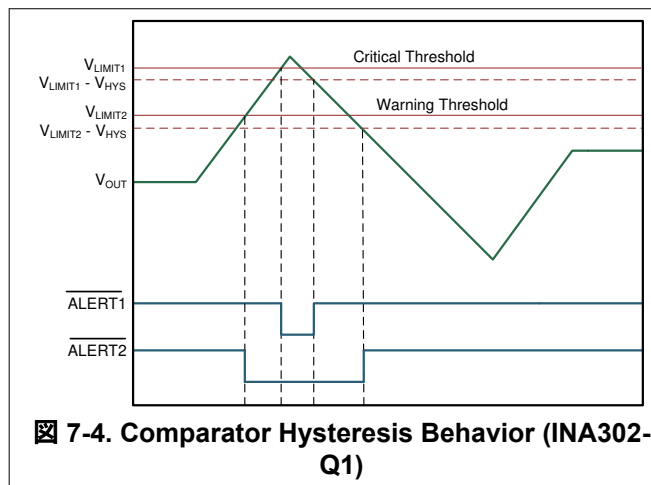
- $I_{\text{TRIP}}$  is the desired out-of-range current threshold.
- $R_{\text{SENSE}}$  is the current-sensing resistor.
- GAIN is the gain option of the device selected.
- $V_{\text{REF}}$  is the voltage applied to the REF pin.

#### Note

The maximum voltage that can be applied to the LIMIT2 pin is  $V_S - 0.6 \text{ V}$  and the maximum voltage that can be applied to the LIMIT1 pin must not exceed  $V_S$ .

### 7.3.3.2 Hysteresis

The hysteresis included in the comparators of the INA30x-Q1 reduces the possibility of oscillations in the alert outputs when the measured signal level is near the overlimit threshold level. For overrange events, the corresponding ALERTx pin is asserted when the output voltage ( $V_{\text{OUT}}$ ) exceeds the threshold set at either LIMITx pin. The output voltage must drop to less than the LIMITx pin threshold voltage by the hysteresis value in order for the ALERTx pin to deassert and return to the nominal high state. Likewise for underrange events, the corresponding ALERTx pin is also pulled low when the output voltage drops to less than the threshold set by either LIMITx pin. The ALERTx pin is released when the output voltage of the current-sense amplifier rises to greater than the set threshold plus hysteresis. Hysteresis functionality for both overrange and underrange events is shown in 图 7-4 and 图 7-5 for the INA302-Q1 and INA303-Q1, respectively.



## 7.4 Device Functional Modes

### 7.4.1 Alert Operating Modes

Each comparator has two output operating modes: transparent and latched. These modes determine how the  $\overline{\text{ALERTx}}$  pins respond when an out-of-range condition is removed. The device is placed into either transparent or latched state based on the voltage applied to the corresponding LATCHx pin, as shown in 表 7-1.

**表 7-1. Output Mode Settings**

OUTPUT MODE	LATCHx PINS SETTINGS
$\overline{\text{ALERTx}}$ transparent mode	LATCHx = low
$\overline{\text{ALERTx}}$ latch mode	LATCHx = high

#### 7.4.1.1 Transparent Output Mode

The comparators are set to transparent output mode when the corresponding LATCHx pin is pulled low. When set to transparent mode, the output of the comparators changes and follows the input signal with respect to the programmed alert threshold. For example, when the amplifier output violates the set limit value, the  $\overline{\text{ALERTx}}$  output pin is pulled low. As soon as the differential input signal drops to less than the alert threshold, the output returns to the default high output state. A common implementation using the device in transparent mode is to connect the  $\overline{\text{ALERTx}}$  pins to a hardware interrupt input on a microcontroller. The  $\overline{\text{ALERTx}}$  pin is pulled low as soon as an out-of-range condition is detected, thus notifying the microcontroller. The microcontroller immediately reacts to the alert and takes action to address the overcurrent condition. In transparent output mode, there is no need to latch the state of the alert output because the microcontroller responds as soon as the out-of-range condition occurs.

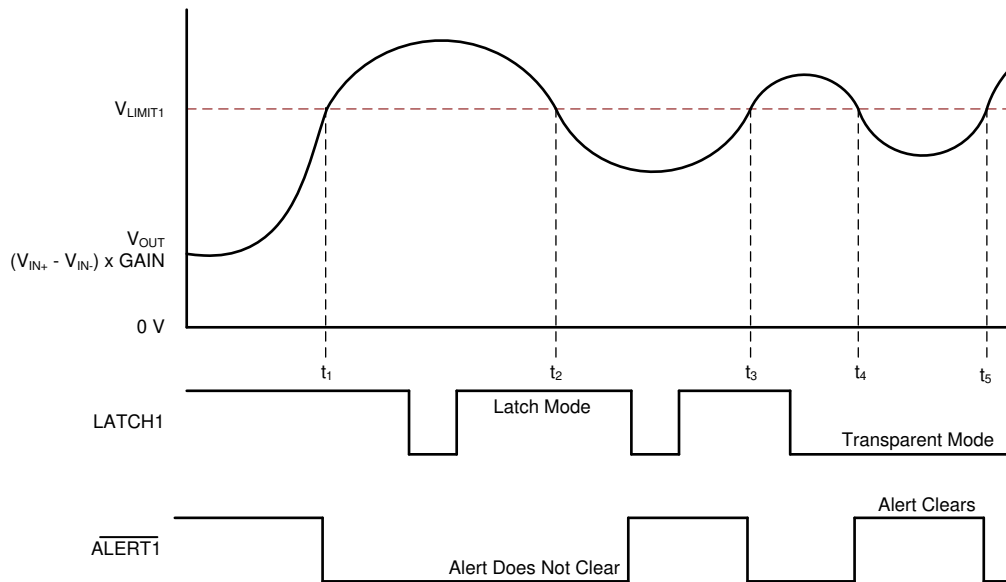
#### 7.4.1.2 Latch Output Mode

The comparators are set to latch output mode when the corresponding LATCHx pin is pulled high. Some applications do not continuously monitor the state of the  $\overline{\text{ALERTx}}$  pins as described in the [Transparent Output Mode](#) section. For example, if the device is set to transparent output mode in an application that only polls the state of the  $\overline{\text{ALERTx}}$  pins periodically, then the transition of the  $\overline{\text{ALERTx}}$  pins can be missed when the out-of-range condition is not present during one of these periodic polling events. Latch output mode allows the output of the comparators to latch the output of the range condition so that the transition of the  $\overline{\text{ALERTx}}$  pins is not missed when the status of the comparator  $\overline{\text{ALERTx}}$  pins is polled.

The difference between latch mode and transparent mode is how the alert output responds when an overcurrent condition is removed. In transparent mode (LATCH1, LATCH2 = low), when the differential input signal drops to within normal operating range, the  $\overline{\text{ALERTx}}$  pin returns to the default high setting to indicate that the overcurrent event has ended.

In latch mode (LATCHx = high), when an out-of-range condition is detected and the corresponding  $\overline{\text{ALERTx}}$  pin is pulled low; the  $\overline{\text{ALERTx}}$  pin does not return to the default high state when the out-of-range condition is removed. In order to clear the alert, the corresponding LATCHx pin must be pulled low for at least 100 ns. Pulling the LATCHx pins low allows the corresponding  $\overline{\text{ALERTx}}$  pin to return to the default high level, provided the out-of-range condition is no longer present. If the out-of-range condition is still present when the LATCHx pins are pulled low, then the corresponding  $\overline{\text{ALERTx}}$  pin remains low. The  $\overline{\text{ALERTx}}$  pins can be cleared (reset to high) by toggling the corresponding LATCHx pin when the alert condition is detected by the system controller.

The latch and transparent modes are illustrated in [Figure 7-6](#). As illustrated in this figure, at time  $t_1$ , the current-sense amplifier exceeds the limit threshold. During this time the LATCH1 pin is toggled with no affect to the  $\overline{\text{ALERT1}}$  output. The state of the LATCH1 pin only matters when the output of the current-sense amplifier returns to the normal operating region, as shown at  $t_2$ . At this time the LATCH1 pin is high and the overcurrent condition is latched on the  $\overline{\text{ALERT1}}$  output. As shown in the time interval between  $t_2$  and  $t_3$ , the latch condition is cleared when the LATCHx pin is pulled low. At time  $t_4$ , the LATCH1 pin is already pulled low when the amplifier output drops below the limit threshold for the second time. The device is set to transparent mode at this point and the  $\overline{\text{ALERT1}}$  pin is pulled back high as soon as the output of the current-sense amplifier drops below the alert threshold.



**Figure 7-6. Transparent vs. Latch Mode**

## 8 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 8.1 Application Information

#### 8.1.1 Selecting a Current-Sensing Resistor ( $R_{\text{SENSE}}$ )

Selecting the value of this current-sensing resistor is based primarily on two factors: the required accuracy of the current measurement and the allowable power dissipation across the current-sensing resistor. Larger voltages developed across this resistor allow for more accurate measurements to be made. Amplifiers have fixed internal errors that are largely dominated by the inherent input offset voltage. When the input signal decreases, these fixed internal amplifier errors become a larger portion of the measurement and increase the uncertainty in the measurement accuracy. When the input signal increases, the measurement uncertainty is reduced because the fixed errors are a smaller percentage of the signal being measured. Therefore, the use of larger-value, current-sensing resistors inherently improves measurement accuracy.

However, a system design trade-off must be evaluated through the use of larger input signals for improving measurement accuracy. Increasing the current-sense resistor value results in an increase in power dissipation across the current-sensing resistor. Increasing the value of the current-shunt resistor increases the differential voltage developed across the resistor when current passes through the component. This increase in voltage across the resistor increases the power that the resistor must be able to dissipate. Decreasing the value of the current-shunt resistor value reduces the power dissipation requirements of the resistor, but increases the measurement errors resulting from the decreased input signal. Selecting the optimal value for the shunt resistor requires factoring both the accuracy requirement for the specific application and the allowable power dissipation of this component.

An increasing number of very low ohmic-value resistors are becoming more widely available with values reaching down to 200  $\mu\Omega$  or lower, with power dissipations of up to 5 W that enable large currents to be accurately monitored with sensing resistors.

##### 8.1.1.1 Selecting a Current-Sensing Resistor: Example

In this example, the trade-offs involved in selecting a current-sensing resistor are discussed. This example requires 2.5% accuracy for detecting a 10-A overcurrent event where only 250 mW is allowed for the dissipation across the current-sensing resistor at the full-scale current level. Although the maximum power dissipation is defined as 250 mW, a lower dissipation is preferred to improve system efficiency. Some initial assumptions are made that are used in this example: the limit-setting resistor ( $R_{\text{LIMIT}}$ ) is a 1% component, and the maximum tolerance specification for the internal threshold setting current source (1%) is used. Given the total error budget of 2.5%, up to 0.5% of error can be attributed to the measurement error of the device under these conditions.

As shown in 表 8-1, the maximum value calculated for the current-sensing resistor with these requirements is 2.5 mΩ. Although this value satisfies the maximum power dissipation requirement of 250 mW, headroom is available from the 2.5% maximum total overcurrent detection error to reduce the value of the current-sensing resistor and to further reduce power dissipation. Selecting a 1.5-mΩ, current-sensing resistor value offers a good tradeoff for reducing the power dissipation in this scenario by approximately 40% and stays within the accuracy region.

**表 8-1. Calculating the Current-Sensing Resistor, R<sub>SENSE</sub>**

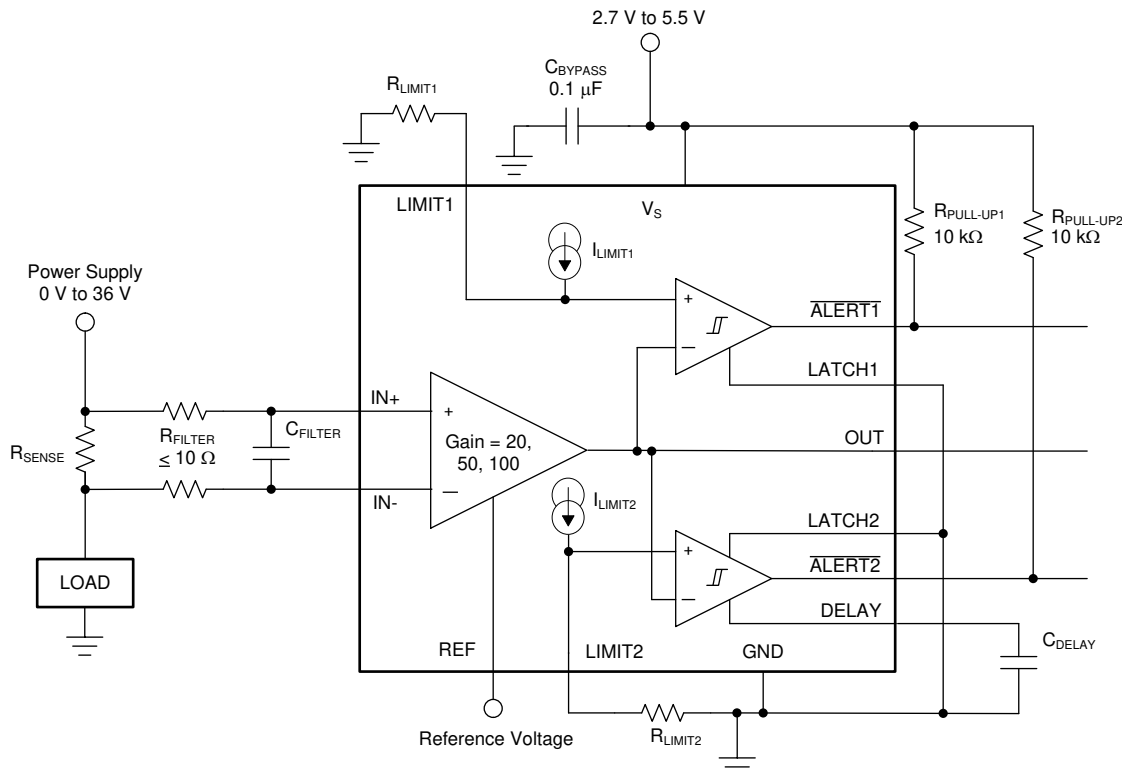
PARAMETER		EQUATION	VALUE	UNIT
<b>DESIGN TARGETS</b>				
I <sub>MAX</sub>	Maximum current		10	A
P <sub>D_MAX</sub>	Maximum allowable power dissipation		250	mW
	Allowable current threshold accuracy		2.5%	
<b>DEVICE PARAMETERS</b>				
V <sub>OS</sub>	Offset voltage		30	μV
E <sub>G</sub>	Gain error		0.15%	
<b>CALCULATIONS</b>				
R <sub>SENSE_MAX</sub>	Maximum allowable R <sub>SENSE</sub>	$P_{D\_MAX} / I_{MAX}^2$	2.5	mΩ
V <sub>OS_ERROR</sub>	Initial offset voltage error	$(V_{OS} / (R_{SENSE\_MAX} \times I_{MAX})) \times 100$	0.12%	
ERROR <sub>TOTAL</sub>	Total measurement error	$\sqrt{(V_{OS\_ERROR}^2 + E_G^2)}$	0.19%	
ERROR <sub>INITIAL</sub>	Initial threshold error	I <sub>LIMIT</sub> tolerance + R <sub>LIMIT</sub> tolerance	2%	
ERROR <sub>AVAILABLE</sub>	Maximum allowable measurement error	Maximum error – ERROR <sub>INITIAL</sub>	1%	
V <sub>OS_ERROR_MAX</sub>	Maximum allowable offset error	$\sqrt{(ERROR_{AVAILABLE}^2 - E_G^2)}$	0.48%	
V <sub>DIFF_MIN</sub>	Minimum differential voltage	$V_{OS} / V_{OS\_ERROR\_MAX} (1\%)$	6.3	mV
R <sub>SENSE_MIN</sub>	Minimum sense resistor value	$V_{DIFF\_MIN} / I_{MAX}$	0.63	mΩ
P <sub>D_MIN</sub>	Lowest-possible power dissipation	$R_{SENSE\_MIN} \times I_{MAX}^2$	63	mW



## 8.1.2 Input Filtering

The integrated comparators in the INA30x-Q1 are very accurate at detecting out-of-range events because of the low offset voltage; however, noise present at the input of the current-sense amplifier and noise internal to the device can make the offset appear larger than specified. The most obvious effect that external noise can have on the operation of a comparator is to cause a false alert condition. If a comparator detects a large noise transient coupled into the signal, the device can easily falsely interpret this transient as an overrange condition.

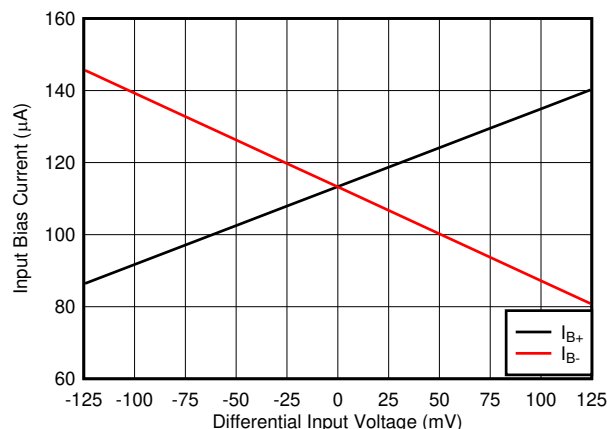
External filtering helps reduce the amount of noise that reaches the comparator and reduce the likelihood of a false alert from occurring because of external noise. The trade-off to adding this noise filter is that the alert response time is increased because the input signal and the noise are filtered. [Figure 8-1](#) shows the implementation of an input filter for the device.



**Figure 8-1. Input Filter Implementation**

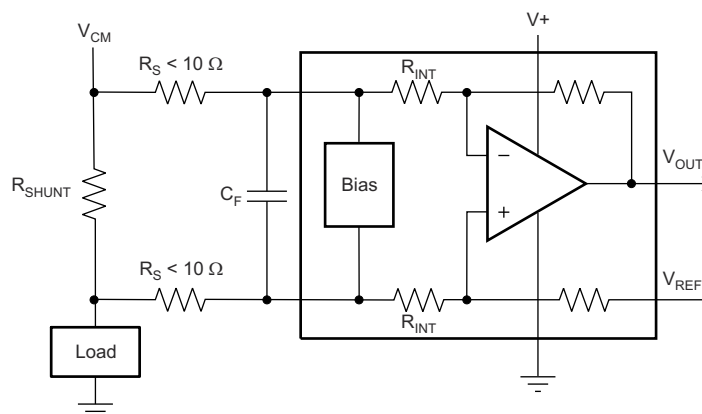
Limiting the amount of input resistance used in this filter is important because this resistance can have a significant effect on the input signal that reaches the device input pins by adversely affecting the gain error of the device. A typical system implementation involves placing the current-sensing resistor very near the device so the traces are very short and the trace impedance is very small. This layout helps reduce coupling of additional noise into the measurement. Under these conditions, the characteristics of the input bias currents have minimal effect on device performance.

As shown in [Figure 8-2](#), the input bias currents increase in opposite directions when the differential input voltage increases. This increase results from the design of the device that allows common-mode input voltages to far exceed the device supply voltage range. When input filter resistors are placed in series with the unequal input bias currents, unequal voltage drops are developed across the input resistors. The difference between these two drops appears as an added signal that (in this case) subtracts from the voltage developed across the current-sensing resistor, thus reducing the signal that reaches the device input pins. Smaller-value input resistors reduce this effect of signal attenuation to allow for a more accurate measurement.



**Figure 8-2. Input Bias Current vs Differential Input Voltage**

The internal bias network present at the input pins shown in [Figure 8-3](#) is responsible for the mismatch in input bias currents that is shown in [Figure 8-2](#). If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed at the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistors add to the measurement is calculated using [Equation 6](#), where the gain error factor is calculated using [Equation 5](#).



Comparators omitted for simplicity.

**Figure 8-3. Filter at Input Pins**

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance value as well as the internal input resistors,  $R_3$  and  $R_4$  (or  $R_{INT}$  as illustrated in [Figure 8-3](#)). The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external

series resistance. The equation used to calculate the expected deviation from the shunt voltage to what is measured at the device input pins is given in 式 5:

$$\text{Gain Error Factor} = \frac{(1250 \times R_{\text{INT}})}{(1250 \times R_S) + (1250 \times R_{\text{INT}}) + (R_S \times R_{\text{INT}})} \quad (5)$$

where

- $R_{\text{INT}}$  is the internal input resistor (R3 and R4).
- $R_S$  is the external series resistance.

With the adjustment factor from 式 5, including the device internal input resistance, this factor varies with each gain version, as shown in 表 8-2. Each individual device gain error factor is shown in 表 8-3.

**表 8-2. Input Resistance**

PRODUCT	GAIN	$R_{\text{INT}}$ (kΩ)
INA30xA1-Q1	20	12.5
INA30xA2-Q1	50	5
INA30xA3-Q1	100	2.5

**表 8-3. Device Gain Error Factor**

PRODUCT	SIMPLIFIED GAIN ERROR FACTOR
INA30xA1-Q1	$\frac{12,500}{(11 \times R_S) + 12,500}$
INA30xA2-Q1	$\frac{1000}{R_S + 1000}$
INA30xA3-Q1	$\frac{2500}{(3 \times R_S) + 2500}$

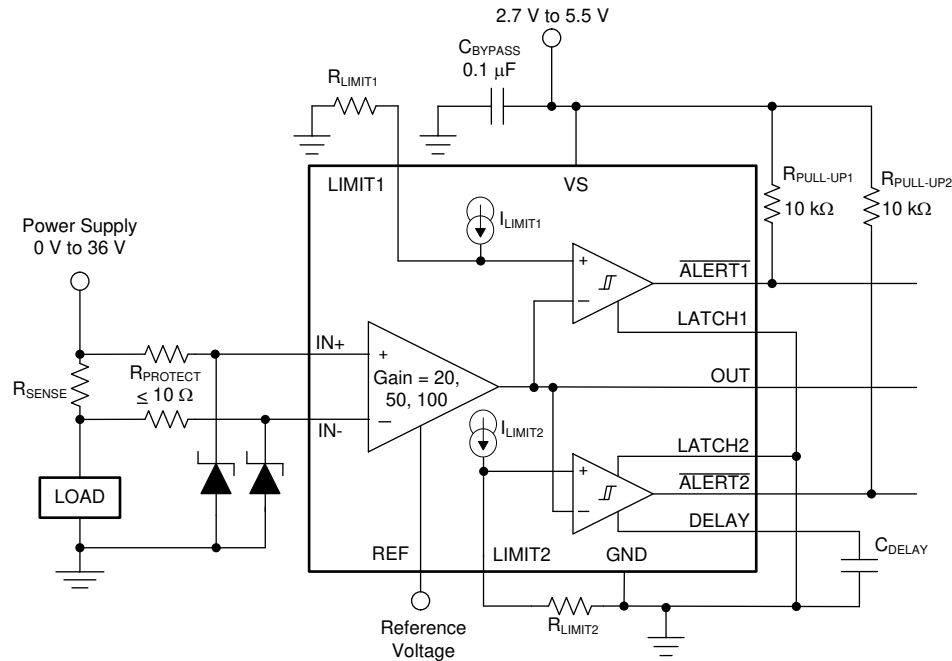
The gain error that is expected from the addition of the external series resistors is then calculated based on 式 6:

$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (6)$$

For example, using an INA302A2-Q1 and the corresponding gain error equation from 表 8-3, a series resistance of 10 Ω results in a gain error factor of 0.99. The corresponding gain error is then calculated using 式 6, resulting in a gain error of approximately 1% solely because of the external 10-Ω series resistors.

### 8.1.3 Using the INA30x-Q1 With Common-Mode Transients Greater Than 36 V

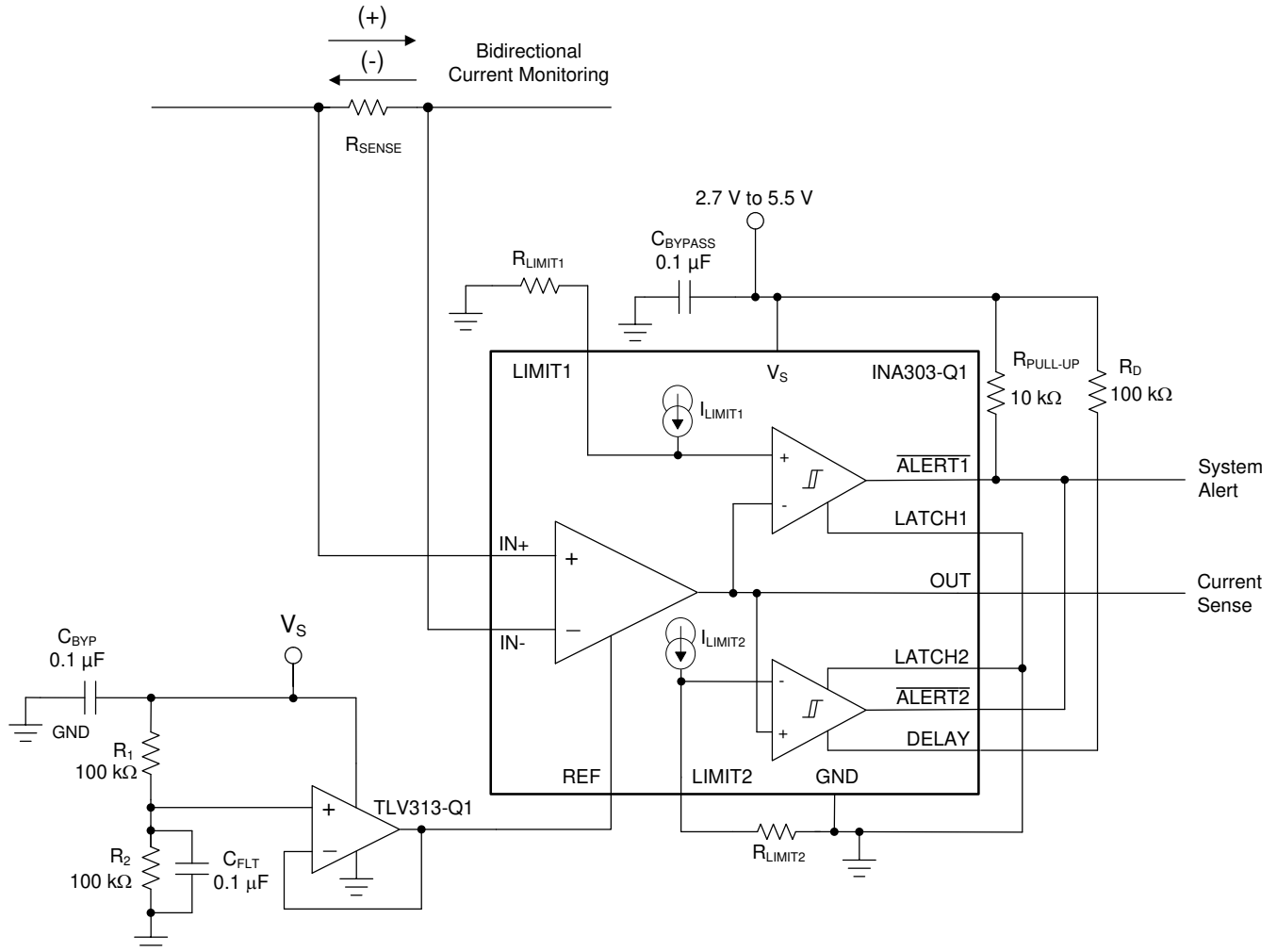
With a small amount of additional circuitry, these devices can be used in circuits subject to transients higher than 36 V. Use only zener diodes or zener-type transient absorbers (sometimes referred to as *transzorb*s). Any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as a working impedance for the zener diode, as shown in [Figure 8-4](#). Keep these resistors as small as possible, preferably 10  $\Omega$  or less. Larger values can be used with an additional induced error resulting from a reduced signal that actually reaches the device input pins. Many applications are satisfied with a 10- $\Omega$  resistor along with conventional zener diodes of the lowest power rating available because this circuit limits only short-term transients. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.



**Figure 8-4. Transient Protection**

## 8.2 Typical Application

The INA30x-Q1 are designed to be easily configured for detecting multiple out-of-range current conditions in an application. These devices are capable of monitoring and providing overcurrent detection of bidirectional currents. By using the REF pin of the INA303-Q1, both positive and negative overcurrent events can be detected.



**8-5. Bidirectional Application**

## 8.2.1 Design Requirements

To allow for bidirectional monitoring, the INA303-Q1 requires a voltage applied to the REF pin. A voltage that is half of the supply voltage is usually preferred to allow for maximum output swing in both the positive and negative current direction. To reduce the errors in the reference voltage, drive the REF pin with a low-impedance source (such as an op amp or external reference). A low-value resistor divider can be used at the expense of quiescent current and accuracy. For this design, a single alert output is preferred, so both  $\overline{\text{ALERT1}}$  and  $\overline{\text{ALERT2}}$  are connected together and use a single pullup resistor.

## 8.2.2 Detailed Design Procedure

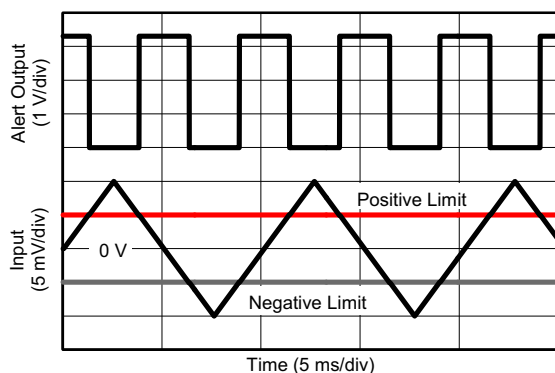
To achieve bidirectional monitoring, drive the reference pin halfway between the supply with a resistor divider buffered by an op amp, as shown in 表 8-4. To reduce the current draw from the supply, use 100-k $\Omega$  resistors to create the divide-by-two voltage divider. The TLV313-Q1 is selected to buffer the voltage divider because this device can operate from a single-supply rail with low  $I_Q$  and offset voltage. To minimize the response time of the  $\overline{\text{ALERT2}}$  output, a 100-k $\Omega$  pullup resistor was added from the DELAY pin to the VS pin. Select values for  $R_{\text{SENSE}}$ ,  $R_{\text{LIMIT2}}$ , and  $R_{\text{LIMIT1}}$  based on the desired current-sense levels and trip thresholds using the information in the [Resistor-Controlled Current Limit](#) and [Selecting a Current-Sensing Resistor \( \$R\_{\text{SENSE}}\$ \)](#) sections. For this example, the values of  $R_{\text{LIMIT1}}$  and  $R_{\text{LIMIT2}}$  were selected so that the positive and negative overcurrent thresholds are the same. 表 8-4 shows the alert output of the INA303-Q1 application circuit with the capability to detect both positive and negative overcurrent conditions.

**表 8-4. Bidirectional Overcurrent Output Status**

OVERCURRENT PROTECTION (OCP) STATUS	OUTPUT
Positive overcurrent detection (OCP+)	0
Negative overcurrent detection (OCP-)	0
Normal operation (no OCP)	1

## 8.2.3 Application Curve

图 8-6 shows the INA303-Q1 device being used in a bidirectional configuration to detect both negative and positive overcurrent events.



**图 8-6. Bidirectional Application Curve**

## 9 Power Supply Recommendations

The device input circuitry accurately measures signals on common-mode voltages beyond the power-supply voltage,  $V_S$ . For example, the voltage applied to the  $V_S$  power-supply pin can be 5 V, whereas the load power-supply voltage being monitored ( $V_{CM}$ ) can be as high as 36 V. At power-up, for applications where the common-mode voltage ( $V_{CM}$ ) slew rate is greater than 6 V/ $\mu$ s with a final common-mode voltage greater than 20 V, the  $V_S$  supply is recommended to be present before  $V_{CM}$ . If the use case requires  $V_{CM}$  to be present before  $V_S$  with  $V_{CM}$  under these same slewing conditions, then a 331- $\Omega$  resistor must be added between the  $V_S$  supply and the VS pin bypass capacitor.

Power-supply bypass capacitors are required for stability, and must be placed as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.1  $\mu$ F. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

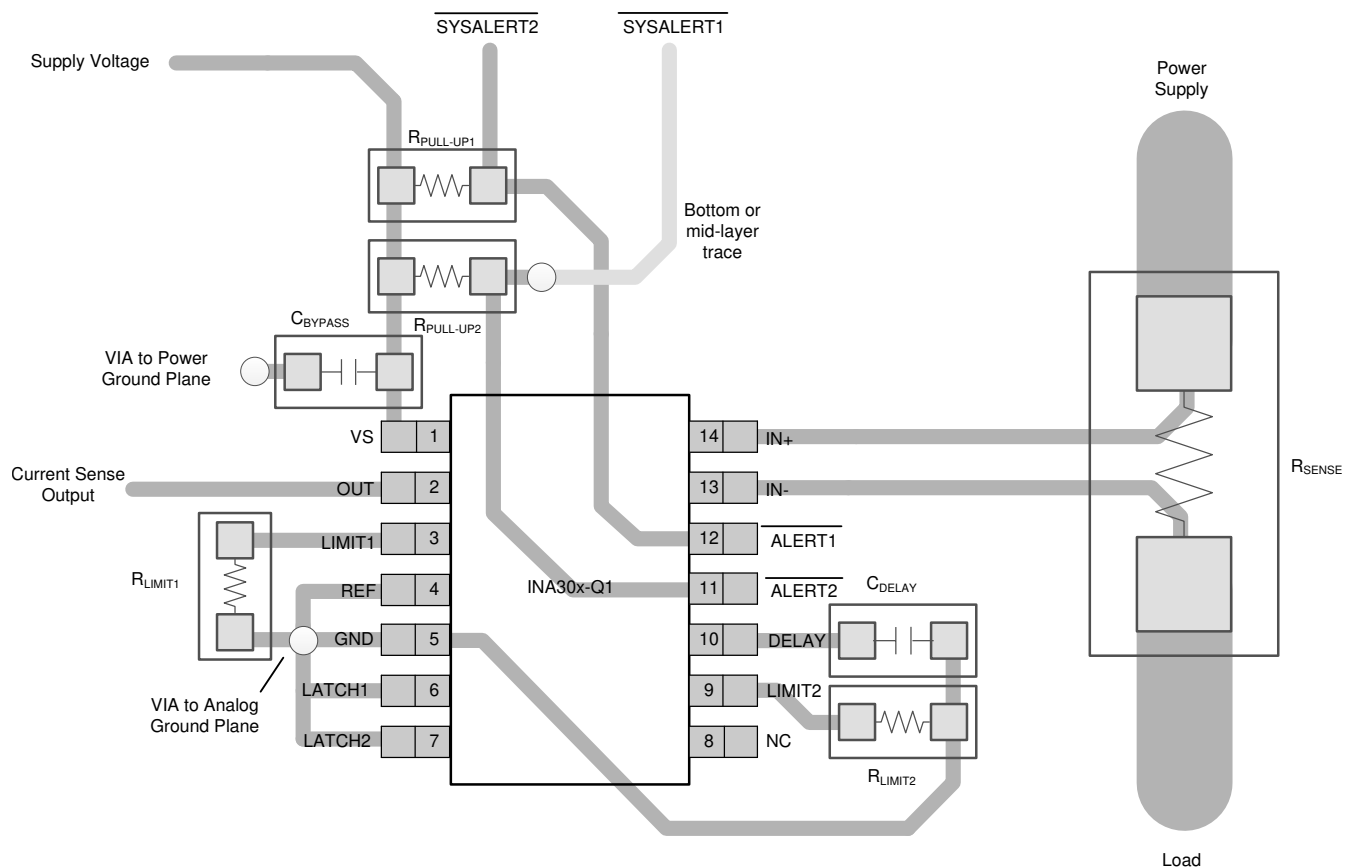
During slow power-up events, current flow through the sense resistor or voltage applied to the REF pin can result in the output voltage momentarily exceeding the voltage at the LIMITx pins, resulting in an erroneous indication of an out-of-range event on the  $\overline{\text{ALERTx}}$  output. When powering the device with a slow ramping power rail where an input signal is already present, all alert indications should be disregarded until the supply voltage has reached the final value.

## 10 Layout

### 10.1 Layout Guidelines

- Apply connections to the current-sense resistor,  $R_{SENSE}$ , on the inside of the resistor pads to avoid additional voltage losses incurred by the high current traces to the resistor. Route the traces from the current-sense resistor symmetrically and side-by-side back to the input of the INA to minimize common-mode errors and noise pickup.
- Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1  $\mu\text{F}$ . Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- Make the connection of  $R_{LIMIT}$  to the ground pin as direct as possible to limit additional capacitance on this node. Routing this connection must be limited to the same plane if possible to avoid vias to internal planes. If the routing can not be made on the same plane and must pass through vias, make sure that a path is routed from  $R_{LIMIT}$  back to the ground pin, and that  $R_{LIMIT}$  is not simply connected directly to a ground plane.
- Routing to the delay capacitor must be short and direct. Keep the routing trace from the DELAY pin to the delay capacitor away from the  $\overline{\text{ALERT2}}$  trace (or any other noisy signals) to minimize any coupling effects. If no delay capacitor is used do not have any connection to the DELAY pin. Long trace lengths on the DELAY pin can cause noise to couple to the device, resulting in false trips.
- Pull up the open-drain output pins to the supply voltage rail; a 10-k $\Omega$  pullup resistor is recommended.

### 10.2 Layout Example



Connect the limit resistors and delay capacitors directly to the GND pin; leave the DELAY pin unconnected or connected to VS through a pullup resistor if no delay is needed.

**10-1. Recommended Layout**



## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [TLVx313-Q1 Low Power Rail-to-Rail In/Out 750- \$\mu\$ V Typical Offset Op Amps data sheet](#)
- Texas Instruments, [Monitoring Current for Multiple Out-of-Range Conditions application report](#)

#### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.3 サポート・リソース

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#### 11.4 Related Links

表 11-1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 11-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
INA302-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
INA303-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

#### 11.5 Trademarks

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#### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 11.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">INA302A1QPWRQ1</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A1Q
INA302A1QPWRQ1.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A1Q
<a href="#">INA302A2QPWRQ1</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A2Q
INA302A2QPWRQ1.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A2Q
<a href="#">INA302A3QPWRQ1</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A3Q
INA302A3QPWRQ1.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A3Q
<a href="#">INA303A1QPWRQ1</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A1Q
INA303A1QPWRQ1.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A1Q
<a href="#">INA303A2QPWRQ1</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A2Q
INA303A2QPWRQ1.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A2Q
<a href="#">INA303A3QPWRQ1</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A3Q
INA303A3QPWRQ1.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A3Q

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

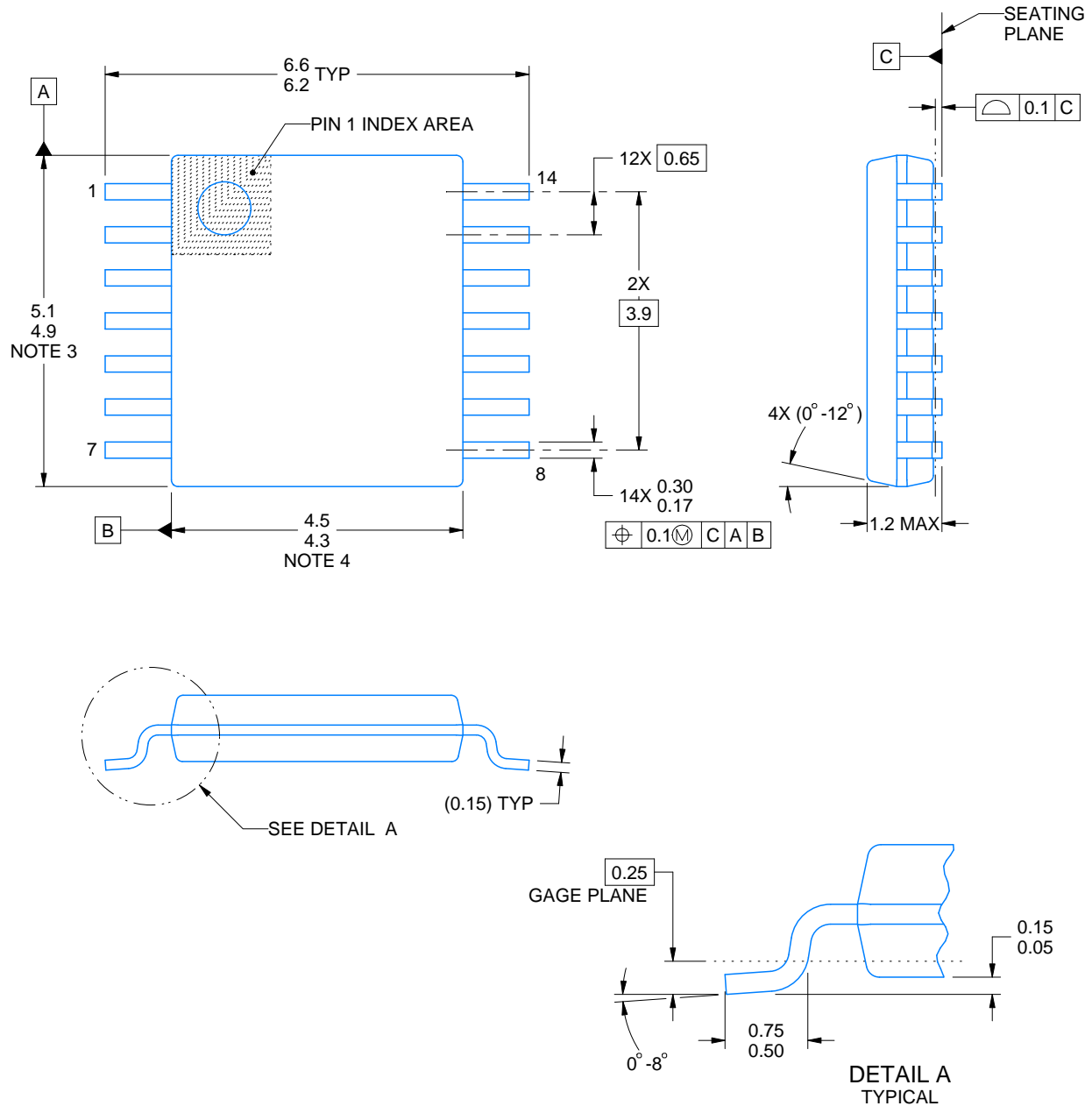
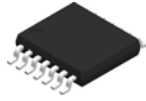
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF INA302-Q1, INA303-Q1 :**

- Catalog : [INA302](#), [INA303](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



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## NOTES:

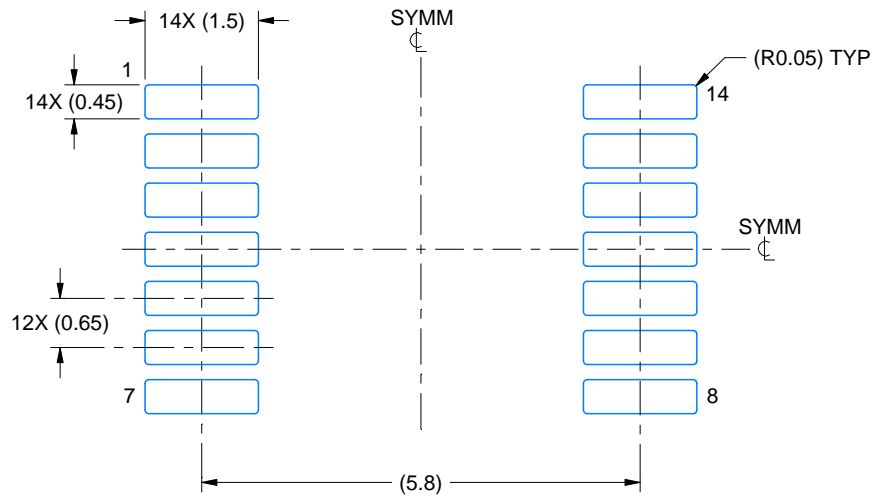
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

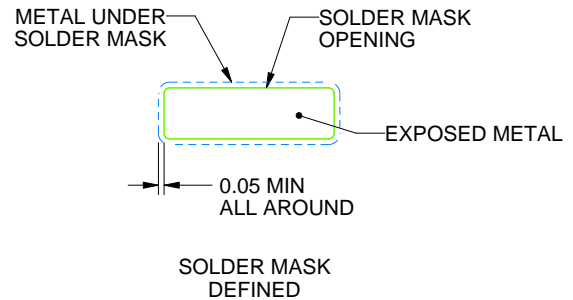
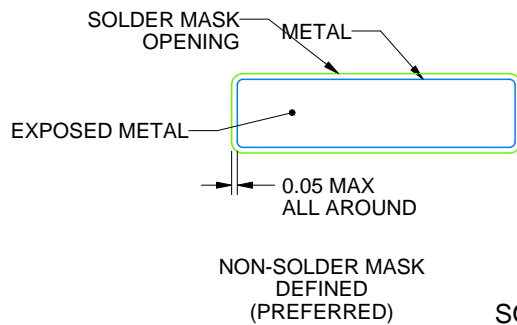
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

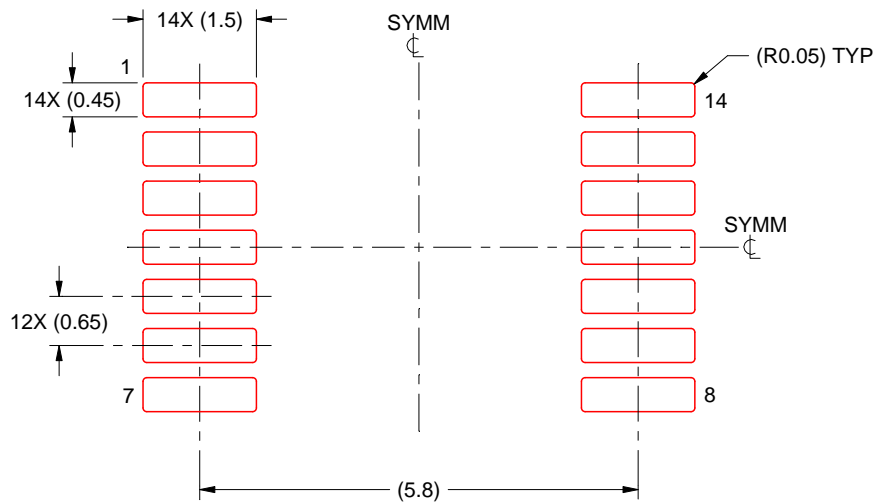
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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