TEXAS INSTRUMENTS
INA250-Q1
JAJSIY5C – JULY 2016 – REVISED SEPTEMBER 2023

INA250-Q1 シャント抵抗内蔵、AEC-Q100 認定済みの 36V、双方向、高精度電流センス・アンプ

1 特長

- 車載アプリケーション用に認定済み
- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40℃～+125℃の周囲動作温度範囲
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C5
- 機能安全対応
  - 機能安全システム設計に役立つ資料を利用可能
- 高精度のシャント抵抗を内蔵:
  - シャント抵抗:2mΩ
  - シャント抵抗の許容誤差:0.1% (最大値)
  - -40℃～+85℃で 15A の連続電流
  - 0℃～+125℃の温度係数:10ppm/℃
- 高精度:
  - ゲイン誤差 (シャントとアンプ):0.3% (最大値)
  - オフセット電流:50mA (最大値、INA250A2-Q1)
- 4 種類のゲインを利用可能
  - INA250A1-Q1:200mV/A
  - INA250A2-Q1:500 mV/A
  - INA250A3-Q1:800 mV/A
  - INA250A4-Q1:2V/A
- 広い同相モード範囲:-0.1V～36V
- 規定動作温度:-40℃～+125℃

2 アプリケーション

- 車体制御モジュール
- DC/DC コンバータ
- バッテリ管理システム
- エンジン制御システム
- サスペンション・システム

3 概要

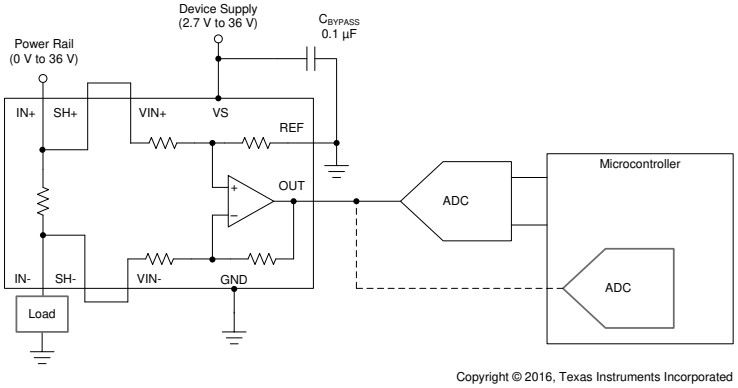
車載用認定済みの INA250-Q1 は、電源電圧にかかわらず 0V～36V の同相電圧で高精度電流測定を可能にするための高精度シャント抵抗を内蔵した電圧出力、電流センシング・アンプのファミリです。

INA250-Q1 ファミリは、4 種類の出力電圧スケールで供給されます。200mV/A、500mV/A、800mV/A、および 2V/A です。このデバイスは、最大温度 +125℃で最大 10A の連続電流について完全にテストして規定されています。INA250-Q1 デバイスは単一の 2.7V～36V の電源で動作し、消費電流は最大 300µA です。INA250-Q1 のすべてのゲイン・バージョンは、拡張動作温度範囲 (-40℃～+125℃) で動作が規定され、TSSOP-16 パッケージで供給されます。

製品情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
INA250-Q1	PW (TSSOP、16)	5.00mm × 6.40mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (April 2020) to Revision C (September 2023) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を変更.....1
- 「製品情報」表を「パッケージ情報」に変更.....1
- Changed the *Shunt resistance (SH+ to SH–)* minimum value for use as stand-alone resistor from: 1.9 mΩ to 1.8 mΩ in the *Electrical Characteristics* table.....6
- Changed the *Shunt resistance (SH+ to SH–)* minimum value for use as stand-alone resistor from: 2.1 mΩ to 2.2 mΩ in the *Electrical Characteristics* table.....6

Changes from Revision A (November 2016) to Revision B (April 2020) — **Page**

- 機能安全対応の情報を追加.....1

Changes from Revision * (July 2016) to Revision A (November 2016) — **Page**

- ドキュメントのステータスを「製品プレビュー」から「量産データ」に変更.....1
- Changed maximum charged-device model ESD value from ±750 to ±1000.....4
- Changed maximum I_B values in the *Electrical Characteristics* table from ±35 to ±40.....6

5 Pin Configuration and Functions

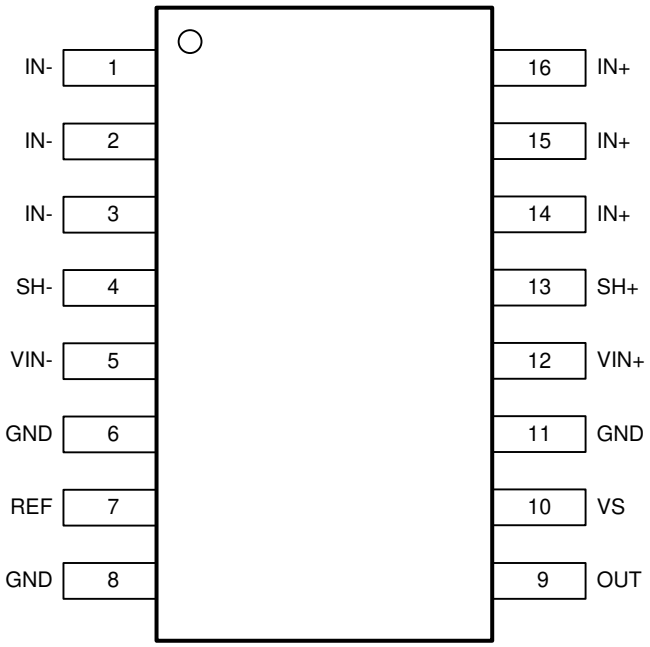


図 5-1. PW Package 16-Pin TSSOP Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	6, 8, 11	Analog	Ground
IN–	1, 2, 3	Analog input	Connect to load
IN+	14, 15, 16	Analog input	Connect to supply
OUT	9	Analog output	Output voltage
REF	7	Analog input	Reference voltage, 0 V to VS (up to 18 V)
SH–	4	Analog output	Kelvin connection to internal shunt. Connect to VIN– if no filtering is needed. See 図 7-4 for filter recommendations.
SH+	13	Analog output	Kelvin connection to internal shunt. Connect to VIN+ if no filtering is needed. See 図 7-4 for filter recommendations.
VIN–	5	Analog input	Voltage input from load side of shunt resistor.
VIN+	12	Analog input	Voltage input from supply side of shunt resistor.
VS	10	Analog	Device power supply, 2.7 V to 36 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage (VS)			40	V
Analog input current	Continuous current		±15	A
Analog inputs (IN+, IN–)	Common-mode	GND – 0.3	40	V
Analog inputs (VIN+, VIN–)	Common-mode	GND – 0.3	40	V
	Differential (V_{IN+}) – ($V_{IN–}$)	–40	40	
Analog inputs (REF)		GND – 0.3	VS + 0.3	V
Analog outputs (SH+, SH–)	Common-mode	GND – 0.3	40	V
Analog outputs (OUT)		GND – 0.3	(VS + 0.3) up to 18	V
Temperature	Operating, T_A	–55	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage	0		36	V
VS	Operating supply voltage	2.7		36	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		INA250-Q1 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	104.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

6.5 Electrical Characteristics

at T_A = 25°C, VS = 5 V, V_{IN+} = 12 V, V_{REF} = 2.5 V, I_{SENSE} = IN+ = 0 A, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{CM}	Common-mode input range		–0.1		36	V
CMR	Common-mode rejection	INA250A1-Q1, V_{IN+} = 0 V to 36 V, T_A = –40°C to 125°C	94	102		dB
		INA250A2-Q1, V_{IN+} = 0 V to 36 V, T_A = –40°C to 125°C	97	110		
		INA250A3-Q1, V_{IN+} = 0 V to 36 V, T_A = –40°C to 125°C	106	114		
		INA250A4-Q1, V_{IN+} = 0 V to 36 V, T_A = –40°C to 125°C	108	118		
I_{OS}	Offset current, RTI(1)	INA250A1-Q1, I_{SENSE} = 0 A		±15	±100	mA
		INA250A2-Q1, I_{SENSE} = 0 A		±12.5	±50	
		INA250A3-Q1, I_{SENSE} = 0 A		±5	±30	
		INA250A4-Q1, I_{SENSE} = 0 A		±5	±20	
dI_{OS}/dT	RTI versus temperature	T_A = –40°C to 125°C		25	250	µA/°C
PSR		VS = 2.7 V to 36 V, T_A = –40°C to 125°C		±0.03	±1	mA/V
I_B	Input bias current	I_{B+}, I_{B-}, I_{SENSE} = 0 A		±28	±40	µA
V_{REF}	Reference input range(3)		0		(VS) up to 18	V
SHUNT RESISTOR(5)						
R_{SHUNT}	Shunt resistance (SH+ to SH–)	Equivalent resistance when used with onboard amplifier	1.998	2	2.002	mΩ
		Used as stand-alone resistor(7)	1.8	2	2.2	
	Package resistance	IN+ to IN–		4.5		mΩ
	Resistor temperature coefficient	T_A = –40°C to 125°C		15		ppm/°C
		T_A = –40°C to 0°C		50		
		T_A = 0°C to 125°C		10		
I_{SENSE}	Maximum continuous current(4)	T_A = –40°C to 85°C			±15	A
	Shunt short time overload	I_{SENSE} = 30 A for 5 seconds		±0.05%		
	Shunt thermal shock	–65°C to 150°C, 500 cycles		±0.1%		
	Shunt resistance to solder heat	260°C solder, 10 s		±0.1%		
	Shunt high temperature exposure	1000 hours, T_A = 150°C		±0.15%		
	Shunt cold temperature storage	24 hours, T_A = –65°C		±0.025%		

at T_A = 25°C, VS = 5 V, V_{IN+} = 12 V, V_{REF} = 2.5 V, I_{SENSE} = IN+ = 0 A, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
G	Gain	INA250A1-Q1		200		mV/A
		INA250A2-Q1		500		
		INA250A3-Q1		800		
		INA250A4-Q1		2		V/A
	System gain error(6)	I_{SENSE} = –10 A to 10 A, T_A = 25°C		±0.05%	±0.3%	
		I_{SENSE} = –10 A to 10 A, T_A = –40°C to 125°C			±0.75%	
		T_A = –40°C to 125°C			45	ppm/°C
	Nonlinearity error	I_{SENSE} = 0.5 A to 10 A		±0.03%		
R_O	Output impedance			1.5		Ω
	Maximum capacitive load	No sustained oscillation		1		nF
VOLTAGE OUTPUT(2)						
	Swing to VS power-supply rail	R_L = 10 kΩ to GND		(VS) – 0.1	(VS) – 0.2	V
	Swing to GND	R_L = 10 kΩ to GND		(V_{GND}) + 25	(V_{GND}) + 50	mV
FREQUENCY RESPONSE						
BW	Bandwidth	INA250A1-Q1, C_L = 10 pF		50		kHz
		INA250A2-Q1, C_L = 10 pF		50		
		INA250A3-Q1, C_L = 10 pF		35		
		INA250A4-Q1, C_L = 10 pF		11		
SR	Slew rate	C_L = 10 pF		0.2		V/µs
NOISE, RTI(1)						
	Voltage noise density	INA250A1-Q1		51		nV/√Hz
		INA250A2-Q1		35		
		INA250A3-Q1		37		
		INA250A4-Q1		27		
POWER SUPPLY						
VS	Operating voltage range		2.7		36	V
I_Q	Quiescent current	T_A = –40°C to 125°C		200	300	µA
TEMPERATURE RANGE						
	Specified range		–40		125	°C

(1) RTI = referred-to-input.
(2) See *Output Voltage Swing vs Output Current* (図 6-19).
(3) The supply voltage range maximum is 36 V, but the reference voltage cannot be higher than 18 V.
(4) See 図 7-1 and the *Layout* section for additional information on the current derating and layout recommendations to improve the current handling capability of the device at higher temperatures.
(5) See the *Integrated Shunt Resistor* section for additional information regarding the integrated current-sensing resistor.
(6) System gain error includes amplifier gain error and the integrated sense resistor tolerance. System gain error does not include the stress related characteristics of the integrated sense resistor. These characteristics are described in the *Shunt Resistor* section of the *Electrical Characteristics* table.
(7) The internal shunt resistor is intended to be used with the internal amplifier and is not intended to be used as a stand-alone resistor. See the *Integrated Shunt Resistor* section for more information.

6.6 Typical Characteristics

at T_A = 25°C, VS = 5 V, V_{IN+} = 12 V, V_{REF} = 2.5 V, I_{SENSE} = IN+ = 0 A, unless otherwise noted.

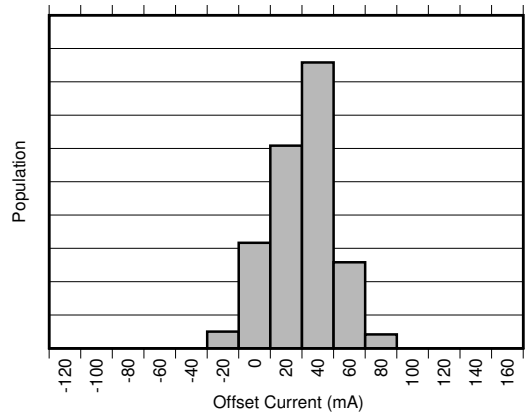


図 6-1. INA250A1-Q1 Input Offset Distribution

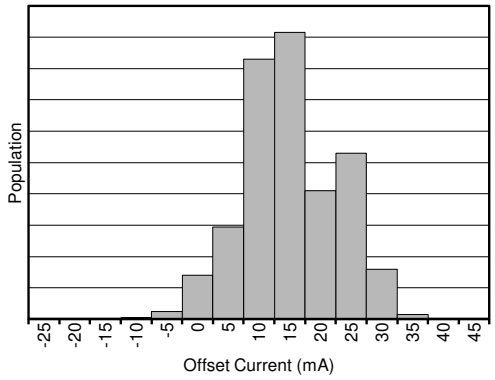


図 6-2. INA250A2-Q1 Input Offset Distribution

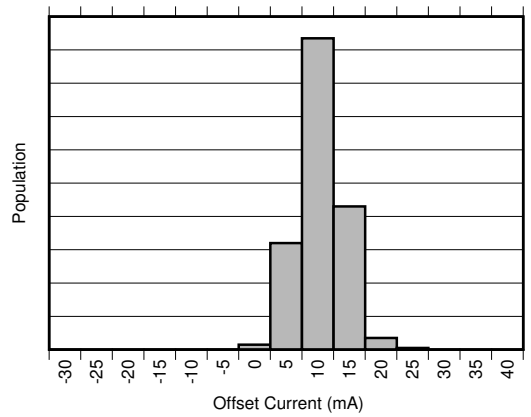


図 6-3. INA250A3-Q1 Input Offset Distribution

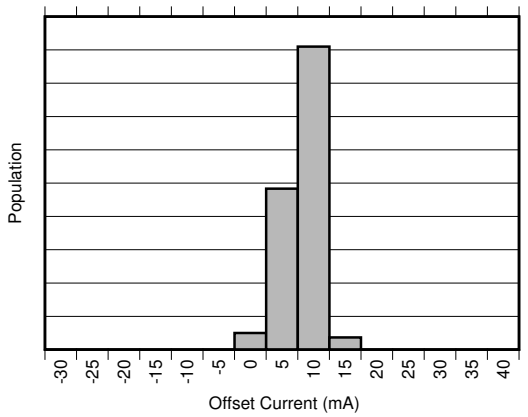


図 6-4. INA250A4-Q1 Input Offset Distribution

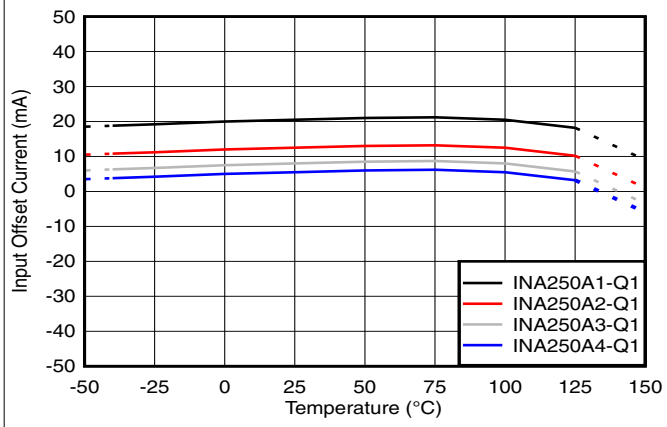


図 6-5. Input Offset vs Temperature

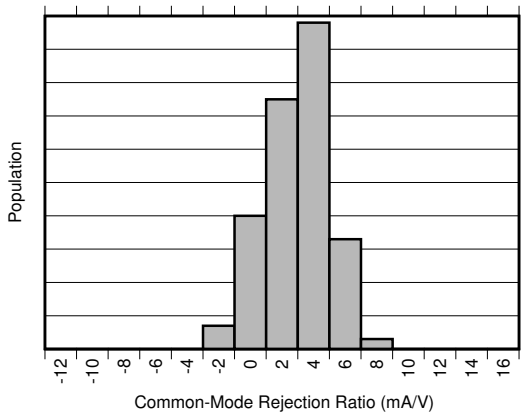


図 6-6. INA250A1-Q1 Common-Mode Rejection Ratio Distribution

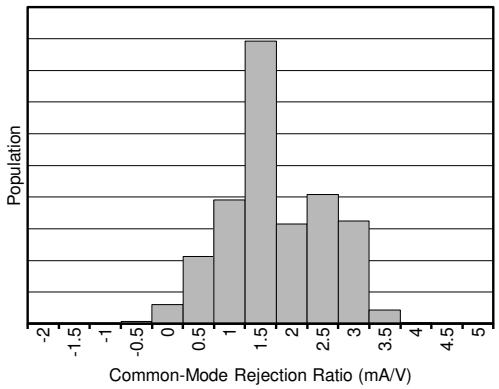


図 6-7. INA250A2-Q1 Common-Mode Rejection Ratio Distribution

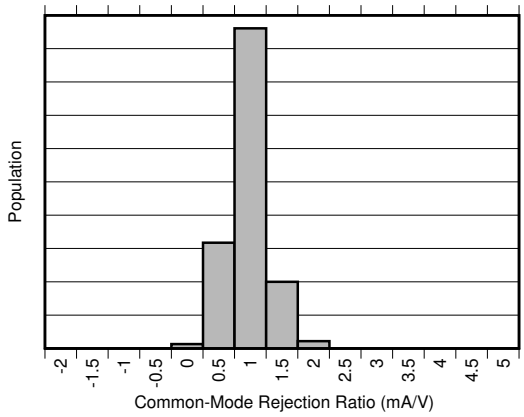


図 6-8. INA250A3-Q1 Common-Mode Rejection Ratio Distribution

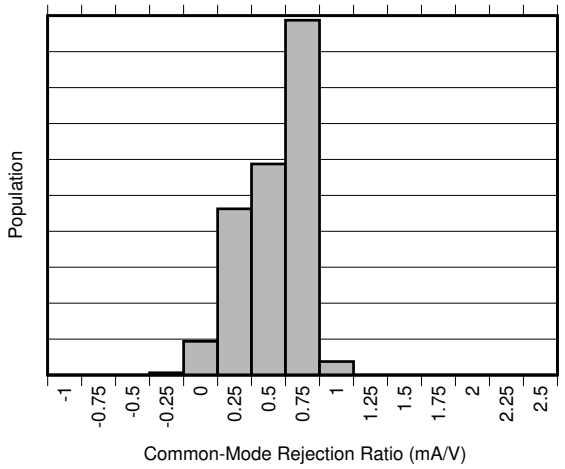


図 6-9. INA250A4-Q1 Common-Mode Rejection Ratio Distribution

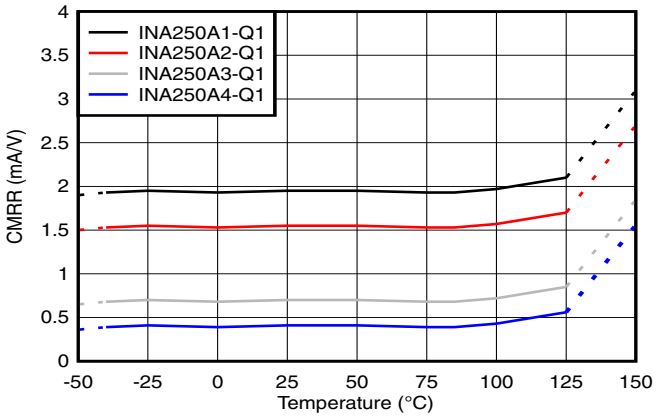


図 6-10. Common-Mode Rejection Ratio vs Temperature

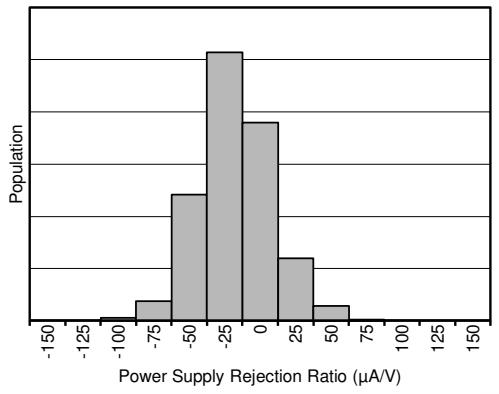


図 6-11. Power-Supply Rejection Ratio Distribution

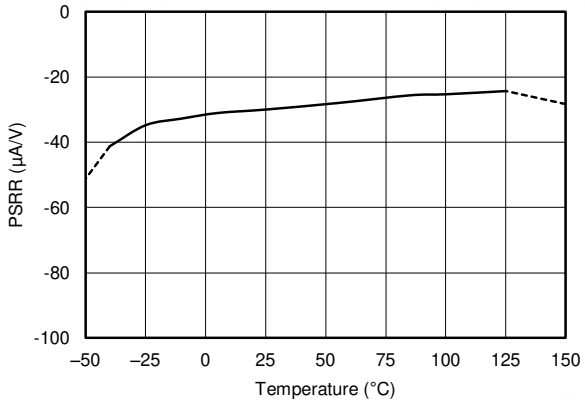


図 6-12. Power-Supply Rejection Ratio vs Temperature

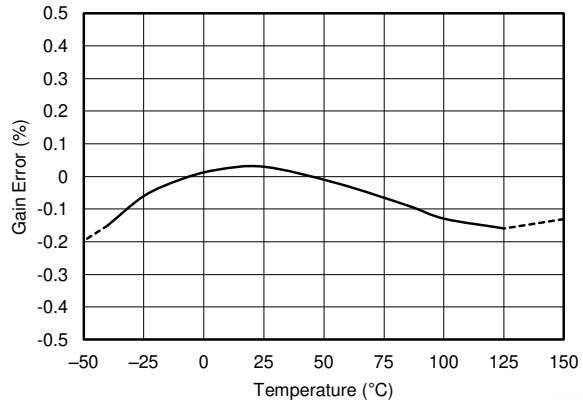
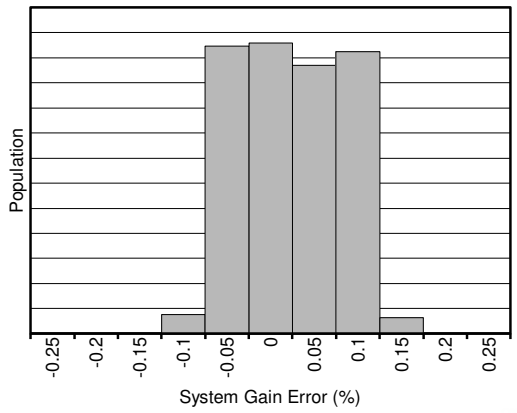


図 6-13. System Gain Error vs Temperature



System gain error = R_{SHUNT} error + amplifier gain error, load current = 10 A

図 6-14. System Gain Error Distribution

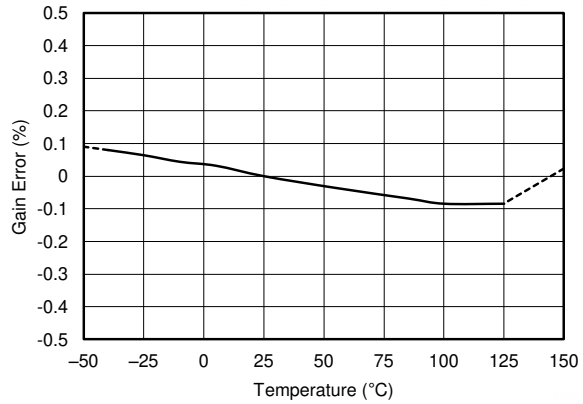
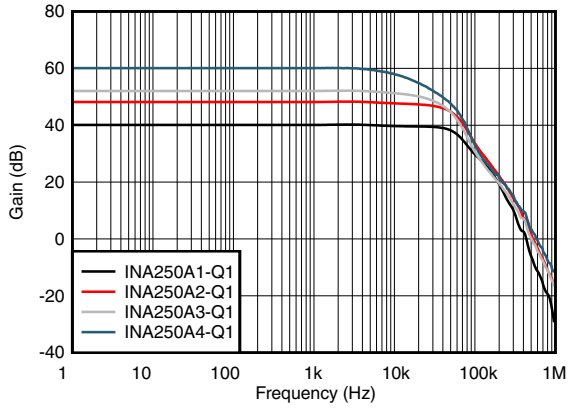
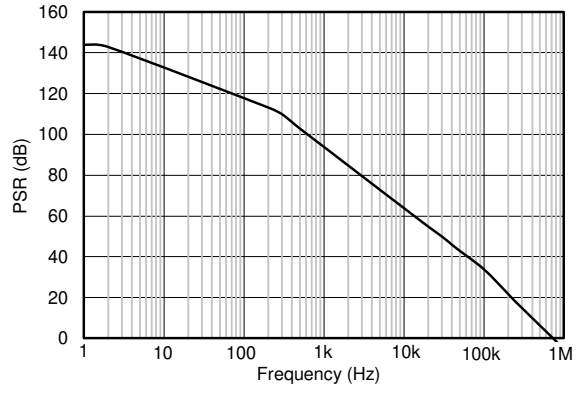


図 6-15. Amplifier Gain Error vs Temperature



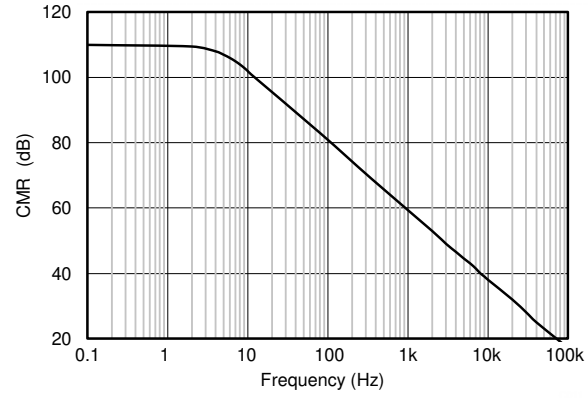
V_{CM} = 12 V, I_{SENSE} = 500 mA_{PP}

図 6-16. Amplifier Gain vs Frequency



V_{CM} = 12 V, V_{REF} = 2.5 V, I_{SENSE} = 0 A, VS = 5 V + 250-mV sine disturbance

図 6-17. Power-Supply Rejection vs Frequency



VS = 5 V, V_{REF} = 2.5 V, I_{SENSE} = 0 A, V_{CM} = 1-V sine wave

図 6-18. Common-Mode Rejection vs Frequency

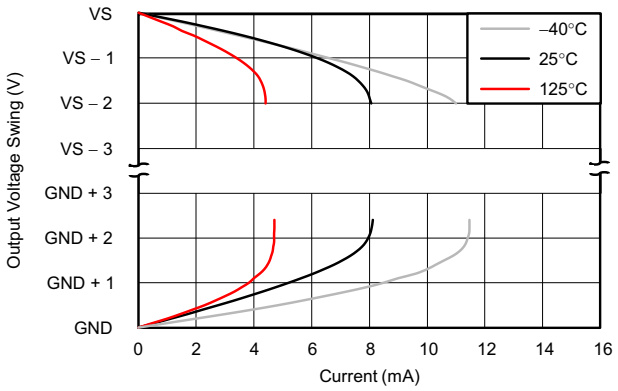
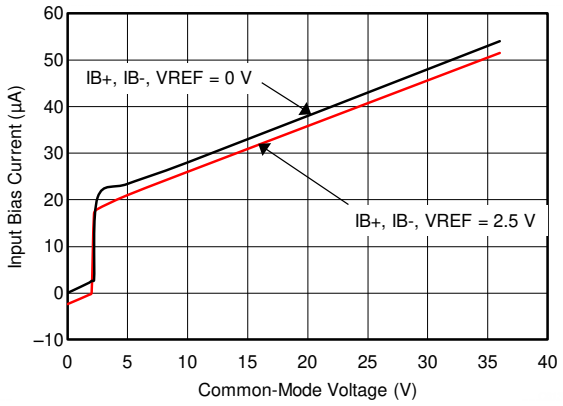
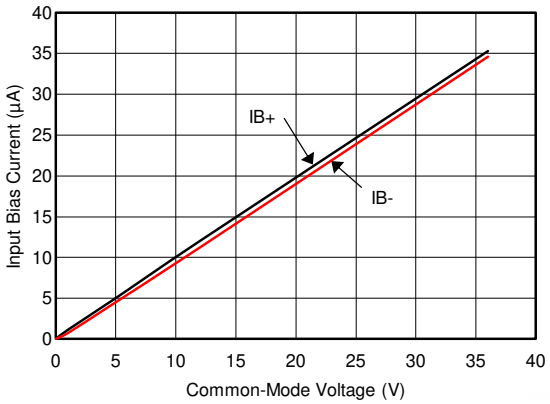


図 6-19. Output Voltage Swing vs Output Current



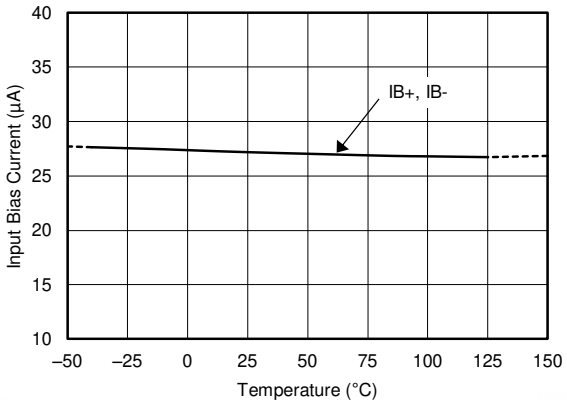
I_{SENSE} = 0 A, VS = 5 V

図 6-20. Input Bias Current vs Common-Mode Voltage (VS = 5 V)



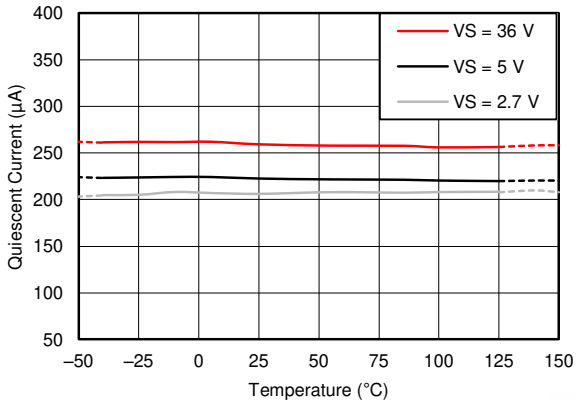
I_{SENSE} = 0 A, VS = 0 V, VREF = 0 V

図 6-21. Input Bias Current vs Common-Mode Voltage (VS = 0 V)



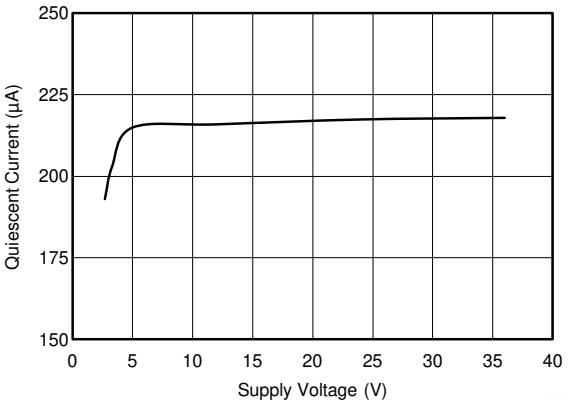
I_{SENSE} = 0 A, VS = 5 V

図 6-22. Input Bias Current vs Temperature



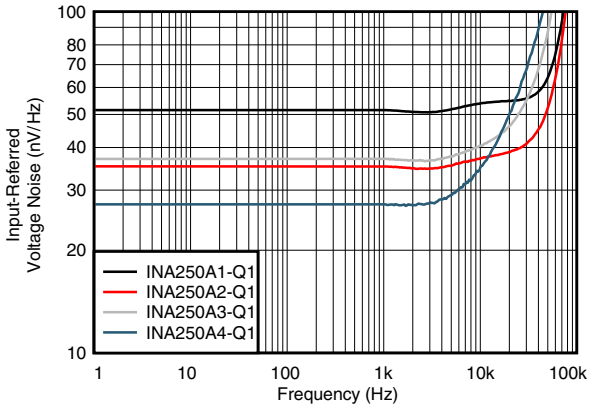
VREF = VS / 2

図 6-23. Quiescent Current vs Temperature



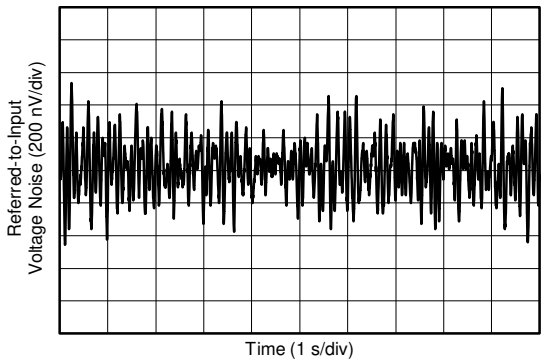
VREF = 2.5 V

図 6-24. Quiescent Current vs Supply Voltage



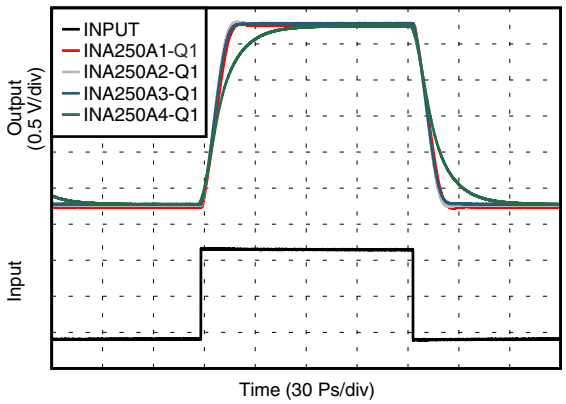
VS = 5 V, V_{REF} = 2.5 V, I_{SENSE} = 0 A

図 6-25. Input-Referred Voltage Noise vs Frequency



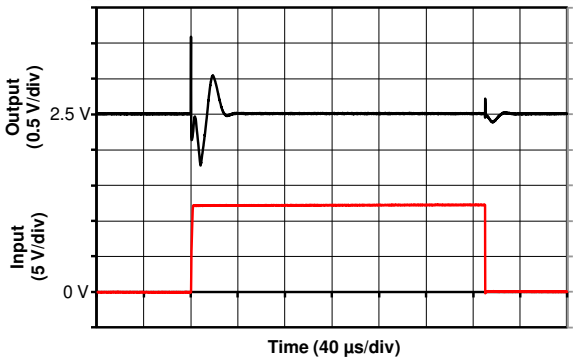
VS = 5 V, V_{CM} = 0 V, I_{SENSE} = 0 A

図 6-26. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)



Input = (VIN+) - (VIN-)

図 6-27. Step Response



Input = VIN+, V_{REF} = 2.5 V

図 6-28. Common-Mode Transient Response

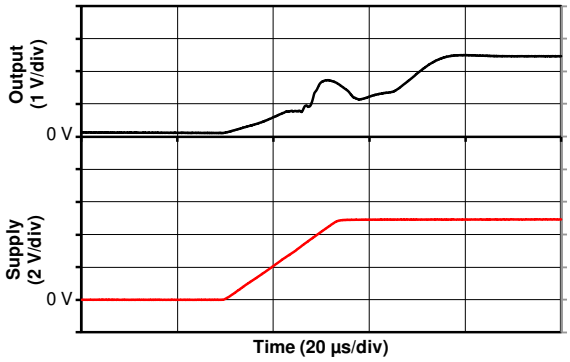


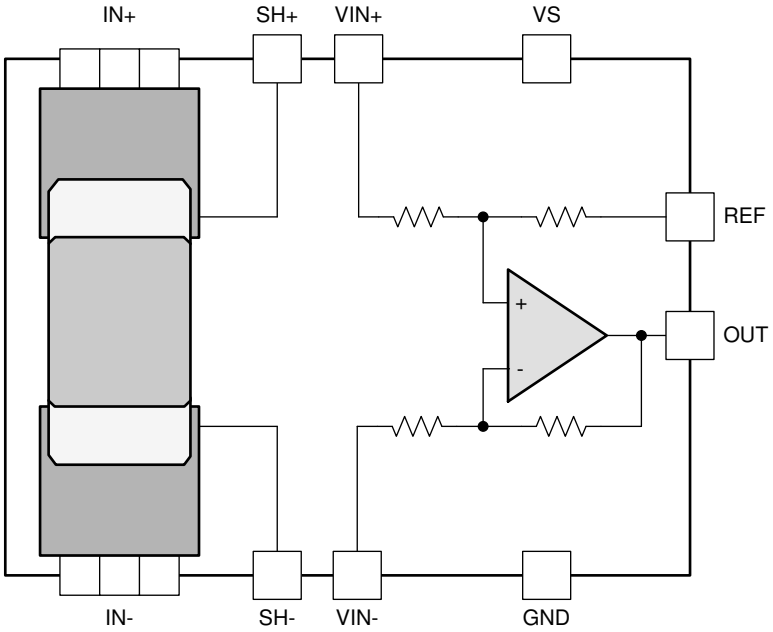
図 6-29. Start-Up Response

7 Detailed Description

7.1 Overview

The INA250-Q1 features a 2-mΩ, precision, current-sensing resistor and a 36-V common-mode, zero-drift topology, precision, current-sensing amplifier integrated into a single package. High precision measurements are enabled through the matching of the shunt resistor value and the current-sensing amplifier gain providing a highly-accurate, system-calibrated solution. Multiple gain versions are available to allow for the optimization of the desired full-scale output voltage based on the target current range expected in the application.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Integrated Shunt Resistor

The INA250-Q1 features a precise, low-drift, current-sensing resistor to allow for precision measurements over the entire specified temperature range of –40°C to +125°C. The integrated current-sensing resistor ensures measurement stability overtemperature and improves layout and board constraint difficulties common in high precision measurements.

The onboard current-sensing resistor is designed as a 4-wire (or Kelvin) connected resistor that enables accurate measurements through a force-sense connection. Connecting the amplifier inputs pins (VIN– and VIN+) to the sense pins of the shunt resistor (SH– and SH+) eliminates many of the parasitic impedances commonly found in typical very-low sensing-resistor level measurements. Although the sense connection of the current-sensing resistor may be accessed through the SH+ and SH– pins, this resistor is not intended to be used as a stand-alone component. The INA250-Q1 device is system-calibrated to ensure that the current-sensing resistor and current-sensing amplifier are both precisely matched to one another. Using the shunt resistor without the onboard amplifier results in a current-sensing resistor tolerance of approximately 5%. To achieve the optimized system gain specification, the onboard sensing resistor must be used with the internal current-sensing amplifier.

The INA250-Q1 has approximately 4.5-mΩ of package resistance. 2 mΩ of this total package resistance is a precisely-controlled resistance from the Kelvin-connected current-sensing resistor used by the amplifier. The power dissipation requirements of the system and package are based on the total 4.5-mΩ package resistance between the IN+ and IN– pins. The heat dissipated across the package when current flows through the device ultimately determines the maximum current that may be safely handled by the package. The current consumption of the silicon is relatively low, leaving the total package resistance carrying the high load current as

the primary contributor to the total power dissipation of the package. The maximum safe-operating current level ensures that the heat dissipated across the package is limited so that the resistor and the package are not damaged, and the internal junction temperature of the silicon does not exceed a +150°C limit.

External factors (such as ambient temperature, external air flow, and PCB layout) may contribute to how effectively the heat developed from the current flowing through the total package resistance may be removed from the device. Under the conditions of no air flow, a maximum ambient temperature of +85°C, and 1-oz. copper input power planes, the INA250-Q1 device can accommodate continuous current levels up to 15 A. As shown in 図 7-1, the current handling capability is derated at temperatures above the +85°C level with safe operation up to 10 A at a +125°C ambient temperature. With air flow and larger 2-oz. copper input power planes, the INA250-Q1 may safely accommodate continuous current levels up to 15 A over the entire –40°C to +125°C temperature range.

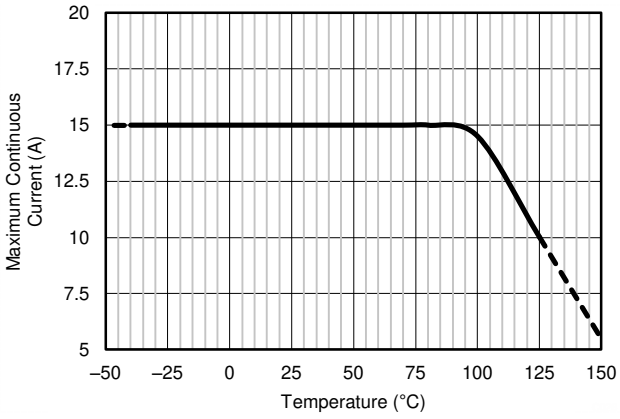


図 7-1. Maximum Current vs Temperature

7.3.2 Short-Circuit Duration

The INA250-Q1 features a physical shunt resistance that can withstand current levels higher than the continuous handling limit of 15 A without sustaining damage to the current-sensing resistor or the current-sensing amplifier if the excursions are brief. 図 7-2 shows the short-circuit duration curve for the INA250-Q1.

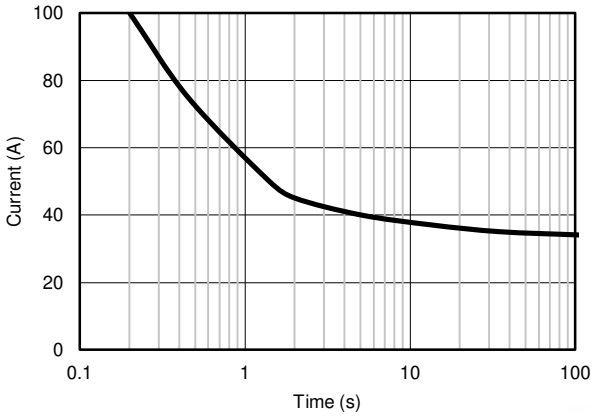


図 7-2. Short-Circuit Duration

7.3.3 Temperature Stability

System calibration is common for many industrial applications to eliminate initial component and system-level errors that may be present. A system-level calibration may reduce the initial accuracy requirement for many of the individual components because the calibration procedure eliminates these errors associated with the components Performing this calibration may enable precision measurements at the system calibration

temperature, but as the system temperature changes as a result of external ambient changes or self heating, measurement errors are reintroduced. Without using accurate temperature compensation in addition to the initial adjustment, the calibration procedure is ineffective in accounting for these temperature-induced changes. One of the primary benefits of the very-low-temperature coefficient of the INA250-Q1(including the integrated current-sensing resistor and current-sensing amplifier) is that the device measurement remains highly accurate, even when the temperature changes throughout the specified temperature range.

The drift performance of the integrated current-sensing resistor is shown in 図 7-3. Although several temperature ranges are specified in the *Electrical Characteristics* table, applications operating in ranges other than those described may use 図 7-3 to determine how much variance in the shunt resistor value may be expected. As with any resistive element, the tolerance of the component varies when exposed to different temperature conditions. For the current-sensing resistor integrated in the INA250-Q1, the resistor varies more when operating in temperatures ranging from –40°C to 0°C than when operating in ranges from 0°C to +125°C. However, even in the –40°C to 0°C temperature range, the drift is still low at 25 ppm/°C.

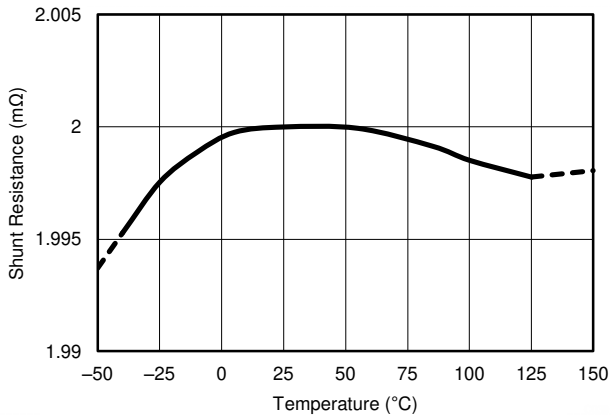


図 7-3. Sensing Resistor vs Temperature

An additional aspect to consider is that when current flows through the current-sensing resistor, power dissipates across this component. This dissipated power results in an increase in the internal temperature of the package, including the integrated sensing resistor. This resistor self-heating effect results in an increase of the resistor temperature helping to move the component out of the colder, wider drift temperature region.

7.4 Device Functional Modes

7.4.1 Amplifier Operation

The INA250-Q1 current-sense amplifier may be configured to measure both unidirectional and bidirectional currents through the reference voltage level applied to the reference pin (REF). The reference voltage connected to REF sets the output level that corresponds with a zero input current condition. For unidirectional operation, tie the REF pin to ground so that when the current increases, the output signal also increases upwards from this reference voltage (or ground in this case). For bidirectional currents, an external voltage source may be used as the reference voltage connected to the REF pin to bias up the output. Set the reference voltage to enable sufficient range above and below this level based on the expected current range to be measured. Positive currents result in an output signal that increases from the zero-current output level set by the reference voltage, whereas negative currents result in an output signal that decreases.

Equation 1 shows the amplifier transfer function for both unidirectional and bidirectional amplifiers:

$$V_{OUT} = (I_{LOAD} \times GAIN) + V_{REF} \quad (1)$$

where:

- I_{LOAD} is the current being measured passing through the internal shunt resistor,
- GAIN is the corresponding gain (mA/V) of the selected device, and
- V_{REF} is the voltage applied to the REF pin

As with any difference amplifier, the INA250-Q1 common-mode rejection ratio is affected by any impedance present at the REF input. This concern is not a problem when the REF pin is connected directly to a reference or power supply. When using resistive dividers from a power supply or a reference voltage, buffer the REF pin with an op amp.

7.4.2 Input Filtering

An obvious and straightforward location for filtering is at the device output; however, this location negates the advantage of the low output impedance of the output stage buffer. The input then represents the best location for implementing external filtering. 図 7-4 shows the typical implementation of the input filter for the device.

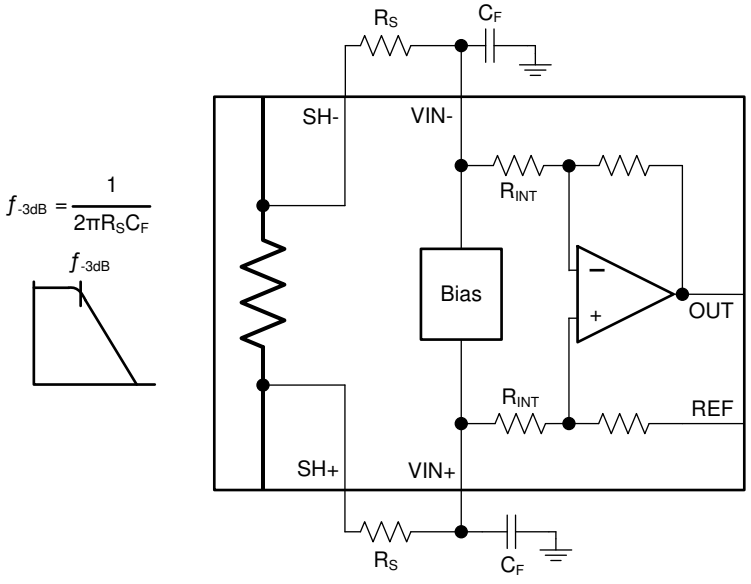


図 7-4. Input Filter

However, the addition of external series resistance at the input pins to the amplifier creates an additional error in the measurement. If possible, keep the value of these series resistors to 10 Ω or less to reduce the affect to accuracy. The internal bias network illustrated in 図 7-4 at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins, as shown in 図 7-5.

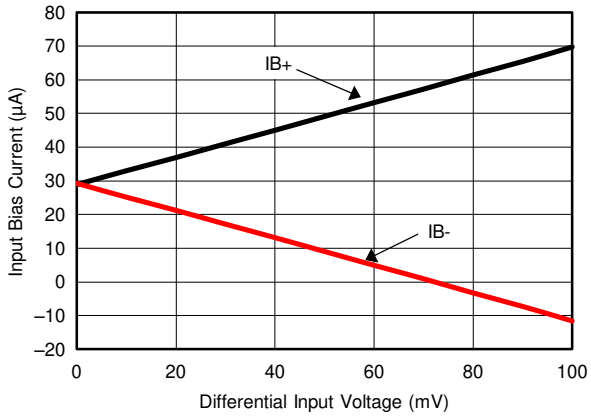


図 7-5. Input Bias Current vs Differential Input Voltage

7.4.2.1 Calculating Gain Error Resulting from External Filter Resistance

If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed across the Kelvin connection of the shunt resistor, thus reducing the voltage that reaches the amplifier input terminals. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation as a result of the low input bias current of the amplifier and the typically low impedance of the traces between the shunt and amplifier input pins. The amount of error these external filter resistors add to the measurement may be calculated using 式 3, where the gain error factor is calculated using 式 2.

The amount of variance between the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance value as well as the internal input resistors, R_{INT}, as shown in 図 7-4. The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor may be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. 式 2 calculates the expected deviation from the shunt voltage compared to the expected voltage at the device input pins.

$$\text{Gain Error Factor} = \frac{(1250 \times R_{INT})}{(1250 \times R_S) + (1250 \times R_{INT}) + (R_S \times R_{INT})} \quad (2)$$

where:

- R_{INT} is the internal input resistor and
- R_S is the external series resistance

$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (3)$$

With the adjustment factor equation including the device internal input resistance, this factor varies with each gain version, as shown in 表 7-1. 表 7-2 lists the gain error factor for each individual device.

式 3 calculates the expected gain error from the addition of the external series resistors.

表 7-1. Input Resistance

DEVICE	GAIN	R_{INT}
INA250A1-Q1	200 mV/A	50 kΩ
INA250A2-Q1	500 mV/A	20 kΩ
INA250A3-Q1	800 mV/A	12.5 kΩ
INA250A4-Q1	2 V/A	5 kΩ

表 7-2. Device Gain Error Factor

DEVICE	SIMPLIFIED GAIN ERROR FACTOR
INA250A1-Q1	$\frac{50{,}000}{(41 \bullet R_S) + 50{,}000}$
INA250A2-Q1	$\frac{20{,}000}{(17 \bullet R_S) + 20{,}000}$
INA250A3-Q1	$\frac{12{,}500}{(11 \bullet R_S) + 12{,}500}$
INA250A4-Q1	$\frac{1{,}000}{R_S + 1{,}000}$

For example, using an INA250A2-Q1 device and the corresponding gain error equation from 表 7-2, a series resistance of 10-Ω results in a gain error factor of 0.991. The corresponding gain error is then calculated using 式 3, resulting in a gain error of approximately 0.84% because of the external 10-Ω series resistors.

7.4.3 Shutting Down the Device

Although the device does not have a shutdown pin, the low power consumption allows for the device to be powered from the output of a logic gate or transistor switch that may turn on and turn off the voltage connected to the device power-supply pin. However, in current-shunt monitoring applications, there is also a concern for how much current is drained from the shunt circuit in shutdown conditions. Evaluating this current drain involves considering the simplified schematic in shutdown mode, as shown in 図 7-6.

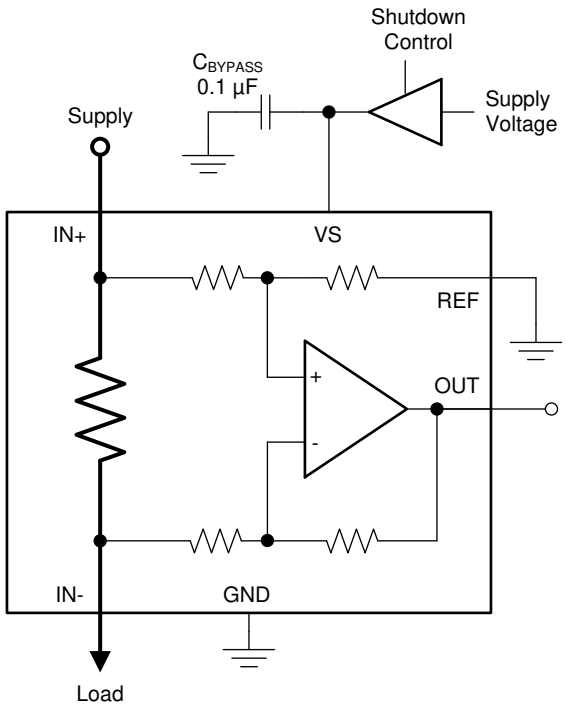


図 7-6. Shutting Down the Device

Note that there is typically an approximate 1-MΩ impedance (from the combination of the feedback and input resistors) from each device input to the REF pin. The amount of current flowing through these pins depends on the respective configuration. For example, if the REF pin is grounded, calculating the effect of the 1-MΩ impedance from the shunt to ground is straightforward. However, if the reference or op amp is powered when the device is shut down, the calculation is direct. Instead of assuming 1 MΩ to ground, assume 1 MΩ to the reference voltage. If the reference or op amp is also shut down, some knowledge of the reference or op amp output impedance under shutdown conditions is required. For instance, if the reference source functions similar to an open circuit when un-powered, little or no current flows through the 1-MΩ path.

7.4.4 Using the Device with Common-Mode Transients Above 36 V

With a small amount of additional circuitry, the device may be used in circuits subject to transients higher than 36 V (such as in automotive applications). Use only zener diodes or zener-type transient absorbers (sometimes referred to as *transzorbs*); any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors, as shown in 図 7-7, as a working impedance for the zener. Keeping these resistors as small as possible is preferable; a resistor value of 10-Ω is the most common. This value limits the effect on accuracy with the addition of these external components, as described in the *Input Filtering* section. Device interconnections between the shunt resistor and amplifier have a current handling limit of 1 A. Using a 10-Ω resistor limits the allowable transient range to 10 V above the zener clamp so the device is not damaged. Larger resistor values may be used in this protection circuit to accommodate a larger transient voltage range, which results in a larger effect on gain error. Because this circuit limits only short-term transients, many applications are satisfied with a 10-Ω resistor, along with conventional zener diodes of the lowest power rating available.

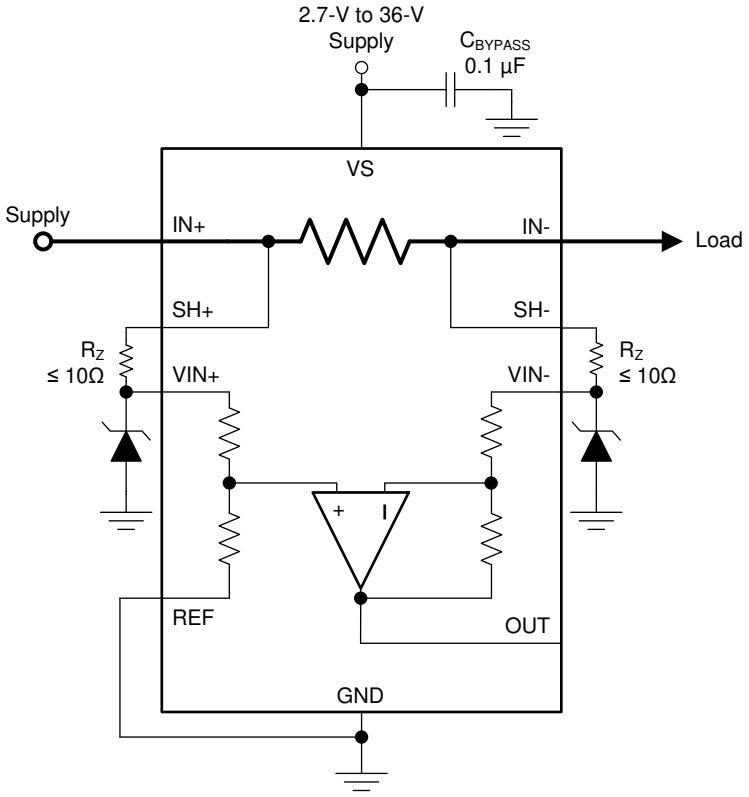


図 7-7. Device Transient Protection

8 Applications and Implementation

注

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8.1 Application Information

The INA250-Q1 measures the voltage developed across the internal current-sensing resistor when current passes through the device. The ability to drive the reference pin to adjust the functionality of the output signal offers multiple configurations, as discussed in this section.

8.2 Typical Applications

8.2.1 Current Summing

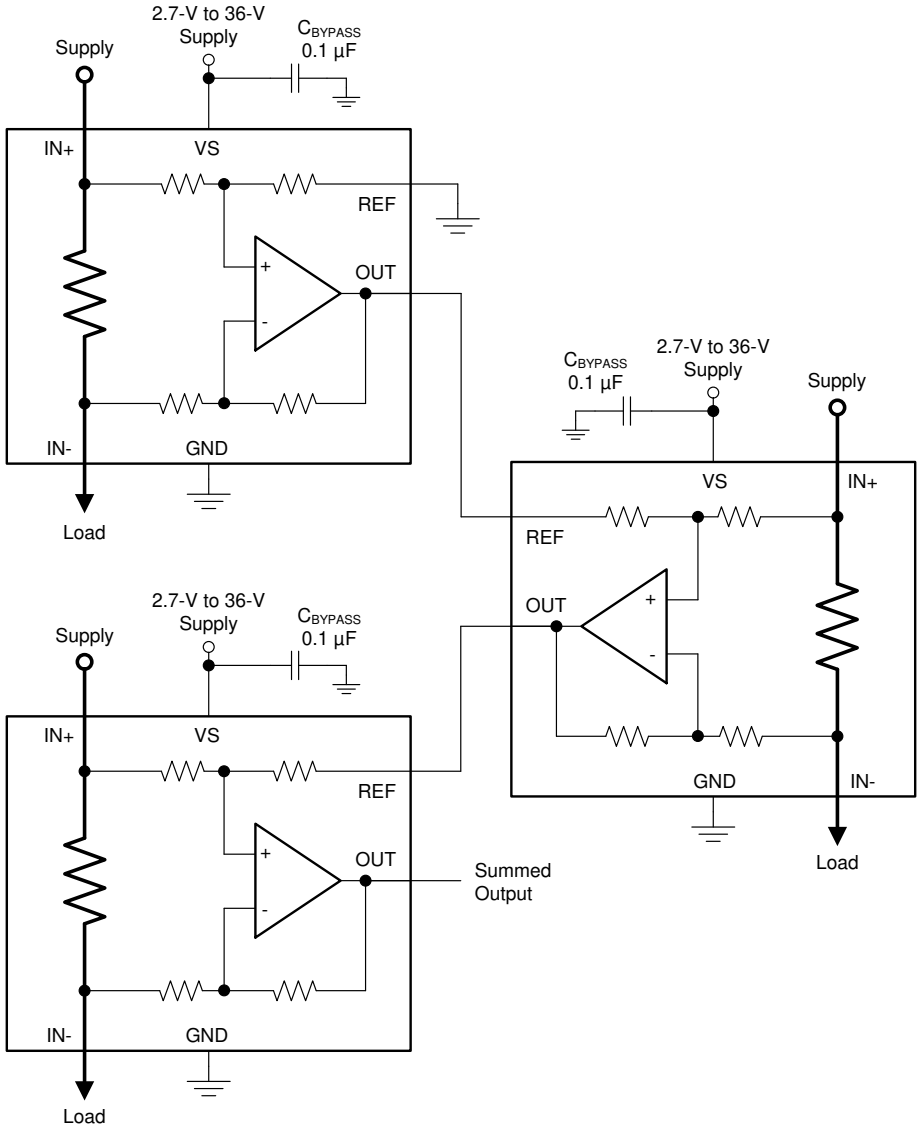


図 8-1. Daisy-Chain Configuration

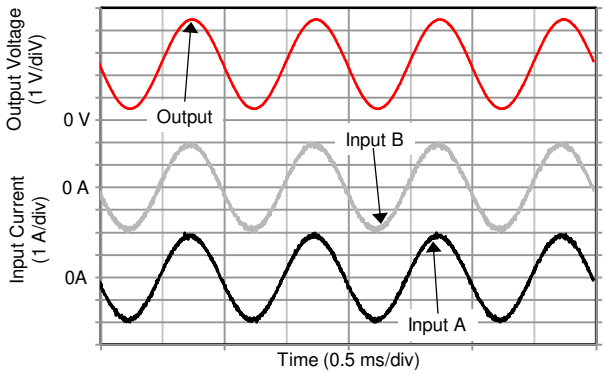
8.2.1.1 Design Requirements

Three daisy-chained devices are illustrated in 図 8-1. The reference input of the first INA250-Q1 device sets the quiescent level on the output of all the INA250-Q1 devices in the string.

8.2.1.2 Detailed Design Procedure

The outputs of multiple INA250-Q1 devices are easily summed by connecting the output signal of one INA250-Q1 device to the reference input of a second INA250-Q1 device. Summing beyond two devices is possible by repeating this configuration, connecting the output signal of the next INA250-Q1 device to the reference pin of a subsequent INA250-Q1 in the chain. The output signal of the final INA250-Q1 device in this chain includes the current level information for all channels in the chain.

8.2.1.3 Application Curve



VS = 5 V, V_{REF} = 2.5 V

図 8-2. Daisy-Chain Configuration Output Response

8.2.2 Parallel Multiple INA250-Q1 Devices for Higher Current

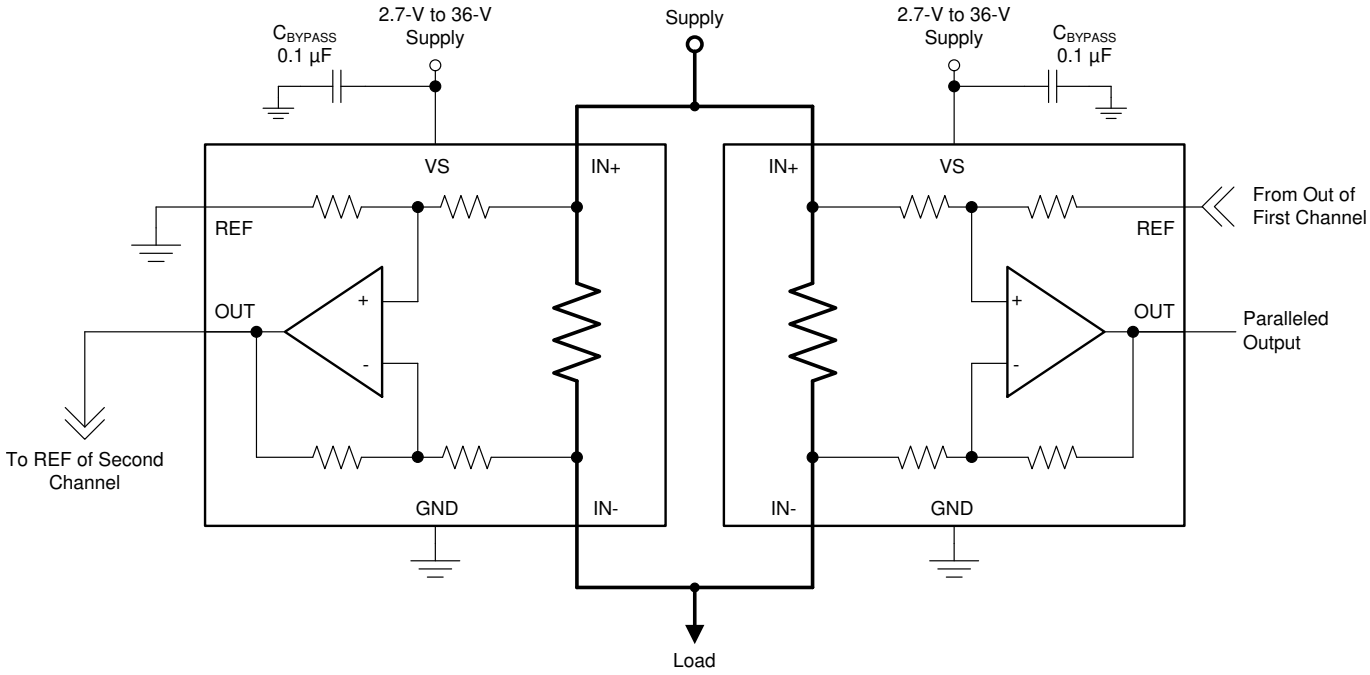


図 8-3. Parallel Summing Configuration

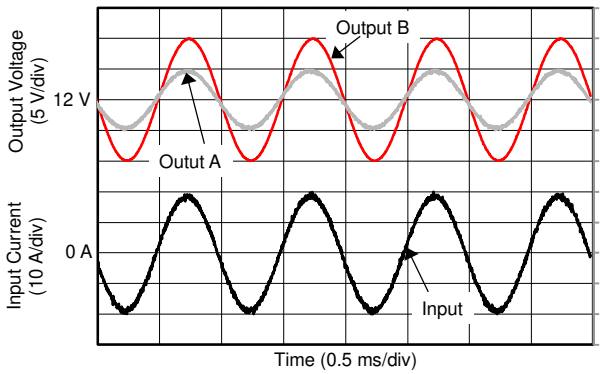
8.2.2.1 Design Requirements

The parallel connection for multiple INA250-Q1 devices may reduce the equivalent overall sense resistance, enabling monitoring of higher current levels than a single device is able to accommodate alone. This configuration also uses a summing arrangement, as described in the *Current Summing* section. A parallel summing configuration is shown in 図 8-3.

8.2.2.2 Detailed Design Procedure

With a summing configuration, the output of the first channel is fed into the reference input of the second, adding the distributed measurements back together into a single measured value.

8.2.2.3 Application Curve



VS = 24 V, V_{REF} = 12 V

図 8-4. Parallel Configuration Output Response

8.2.3 Current Differencing

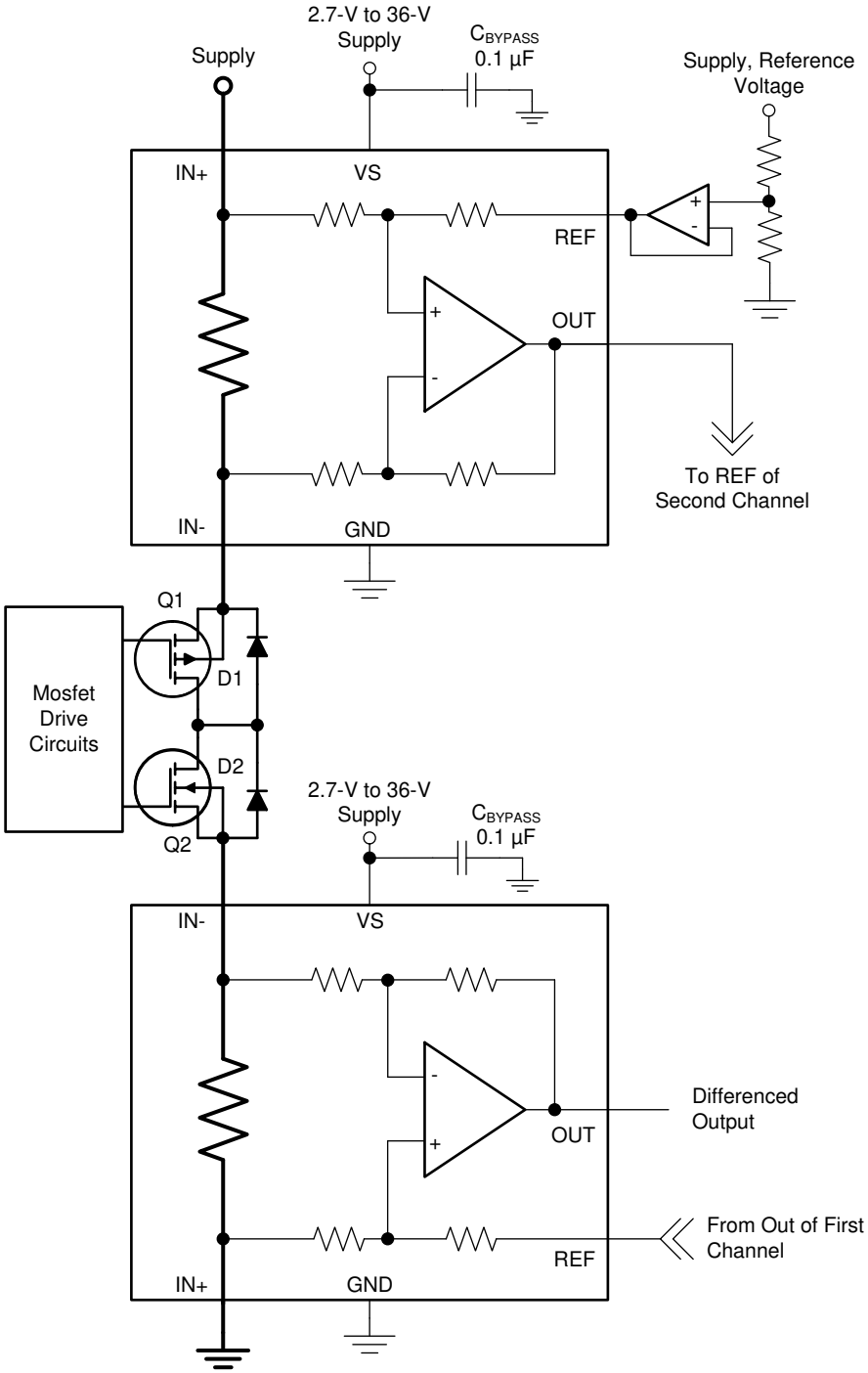


図 8-5. Current Differencing Configuration

8.2.3.1 Design Requirements

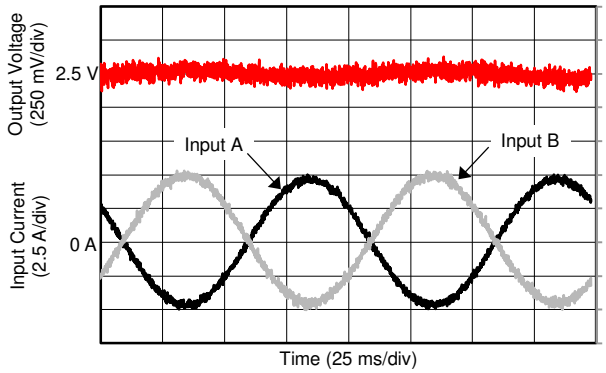
Occasionally, the need may arise to confirm that the current into a load is identical to the current coming out of a load, such as when performing diagnostic testing or fault detection. This procedure requires precision current differencing. This method is the same as current summing, except that the two amplifiers have the respective inputs connected opposite of each other. Under normal operating conditions, the final output is close to the

reference value and proportional to any current difference. 図 8-5 is an example of two INA250-Q1 devices connected for current differencing.

8.2.3.2 Detailed Design Procedure

The load current may also be measured directly at the output of the first channel. Although technically this configuration is current differencing, this connection (see 図 8-5) is intended to allow the upper (positive) sense channel to report any positive-going excursions in the overall output, and the lower (negative) sense channel to report any negative-going excursions.

8.2.3.3 Application Curve



VS = 5 V, V_{REF} = 2.5 V

図 8-6. Current Differencing Configuration Output Response

8.3 Power Supply Recommendations

The input circuitry of the device may accurately measure signals on common-mode voltages beyond the power-supply voltage, VS. For example, the voltage applied to the VS power-supply pin may be 5 V, whereas the load power-supply voltage being monitored (the common-mode voltage) may be as high as 36 V. Note that the device may withstand the full 0-V to 36-V range at the input pins, regardless of whether the device has power applied or not. Power-supply bypass capacitors are required for stability, and must be placed as closely as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

8.4 Layout

8.4.1 Layout Guidelines

- The INA250-Q1 is specified for current handling of up to 10 A over the entire –40°C to +125°C temperature range using a 1-oz. copper pour for the input power plane as well as no external airflow passing over the device.
- The primary current-handling limitation for the INA250-Q1 is how much heat is dissipated inside the package. Efforts to improve heat transfer out of the package and into the surrounding environment improve the ability of the device to handle currents of up to 15 A over the entire –40°C to +125°C temperature range.
- Heat transfer improvements primarily involve larger copper power traces and planes with increased copper thickness (2 oz.) as well as providing airflow to pass over the device. The *INA250EVM* (SBOU153) is capable of supporting 15 A at temperatures up to +125°C.
- Place the power-supply bypass capacitor as close as possible to the supply and ground pins. TI recommends a bypass capacitor value of 0.1 µF. Additional decoupling capacitance may be added to compensate for noisy or high-impedance power supplies.

8.4.2 Layout Examples

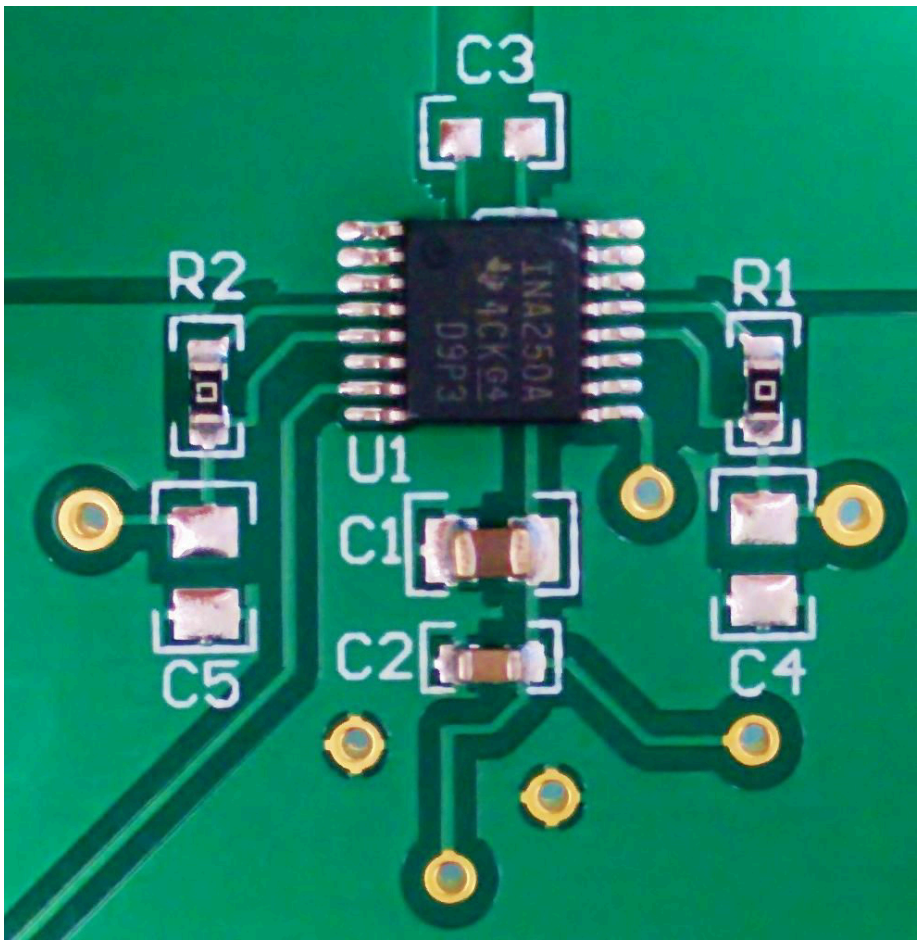


図 8-7. Recommended Layout

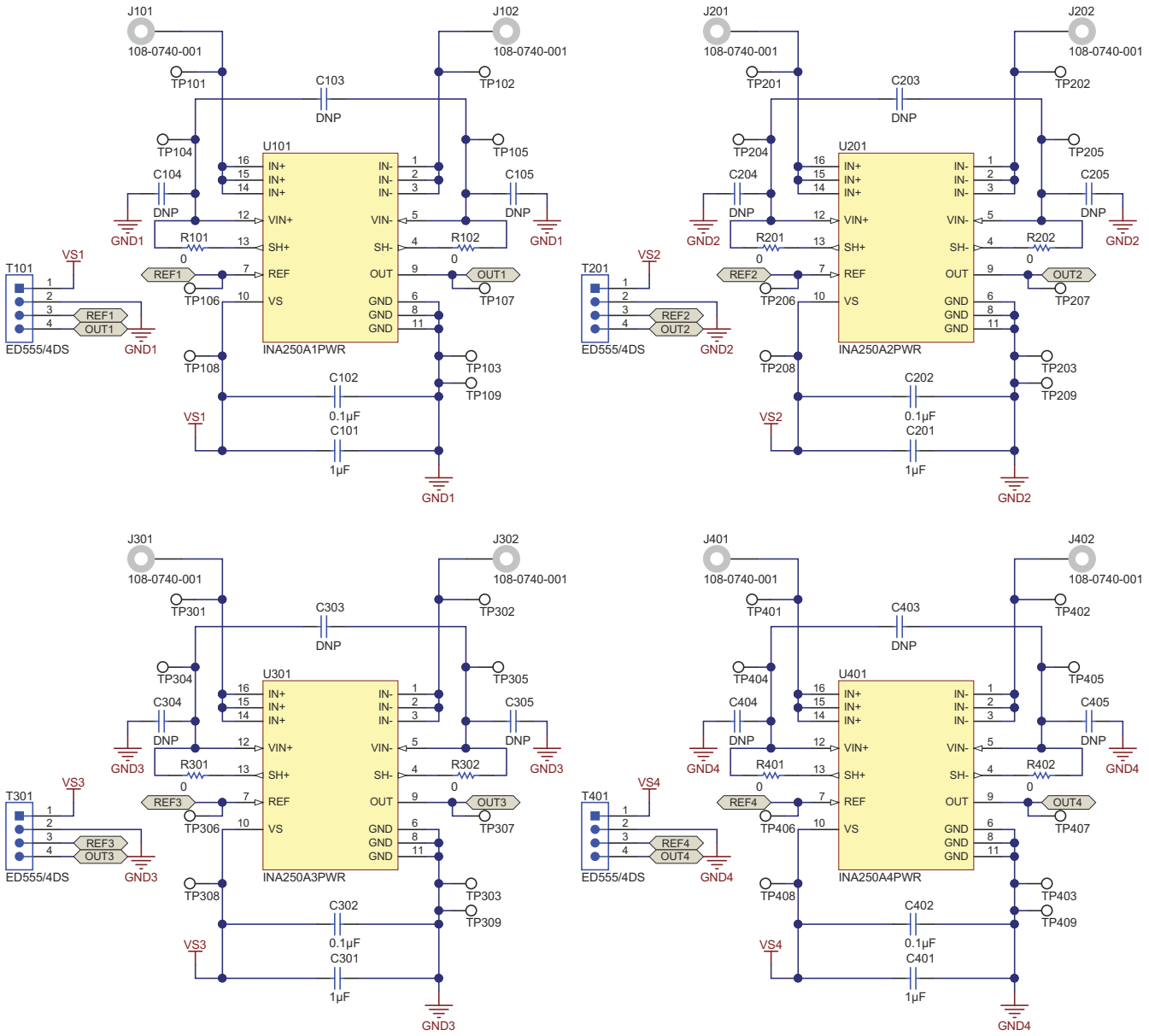


図 8-8. Recommended Layout Schematic

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

- *INA250EVM User Guide* (SBOU153).

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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9.4 Trademarks

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9.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA250A1QPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Q250A1
INA250A1QPWRQ1.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Q250A1
INA250A2QPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Q250A2
INA250A2QPWRQ1.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Q250A2
INA250A3QPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Q250A3
INA250A3QPWRQ1.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Q250A3
INA250A4QPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Q250A4
INA250A4QPWRQ1.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Q250A4

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA250-Q1 :

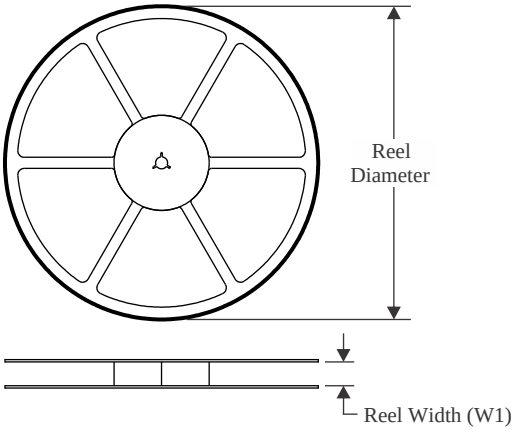
- Catalog : INA250

NOTE: Qualified Version Definitions:

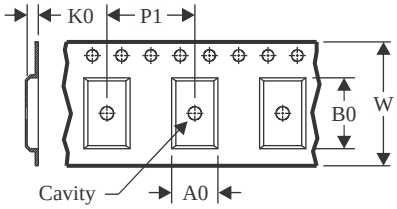
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

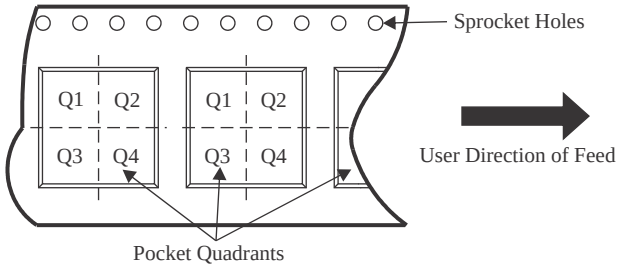


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

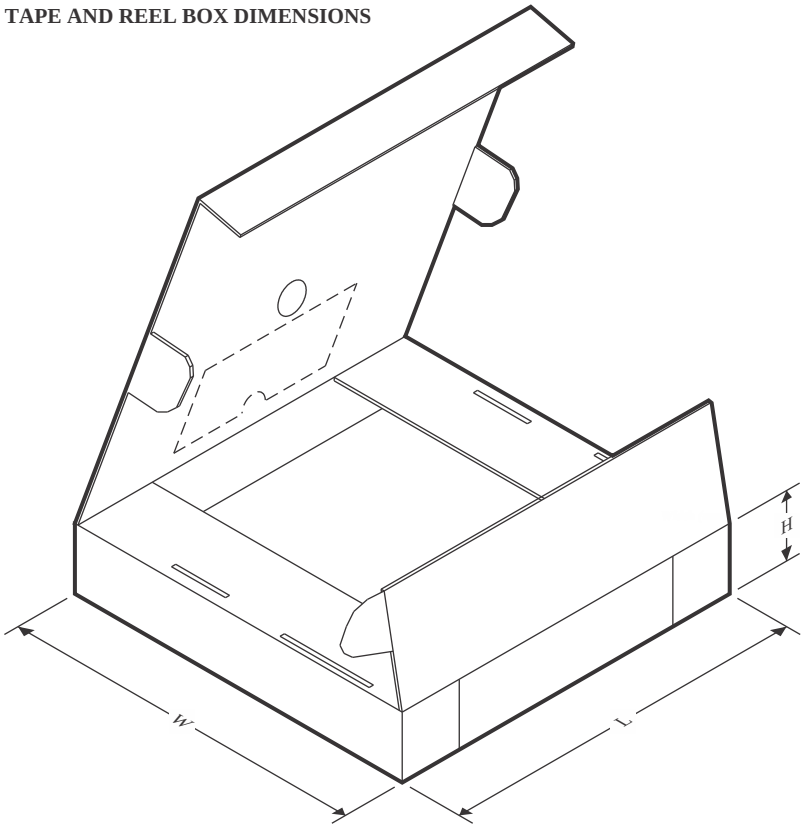
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA250A1QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA250A2QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA250A3QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA250A4QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

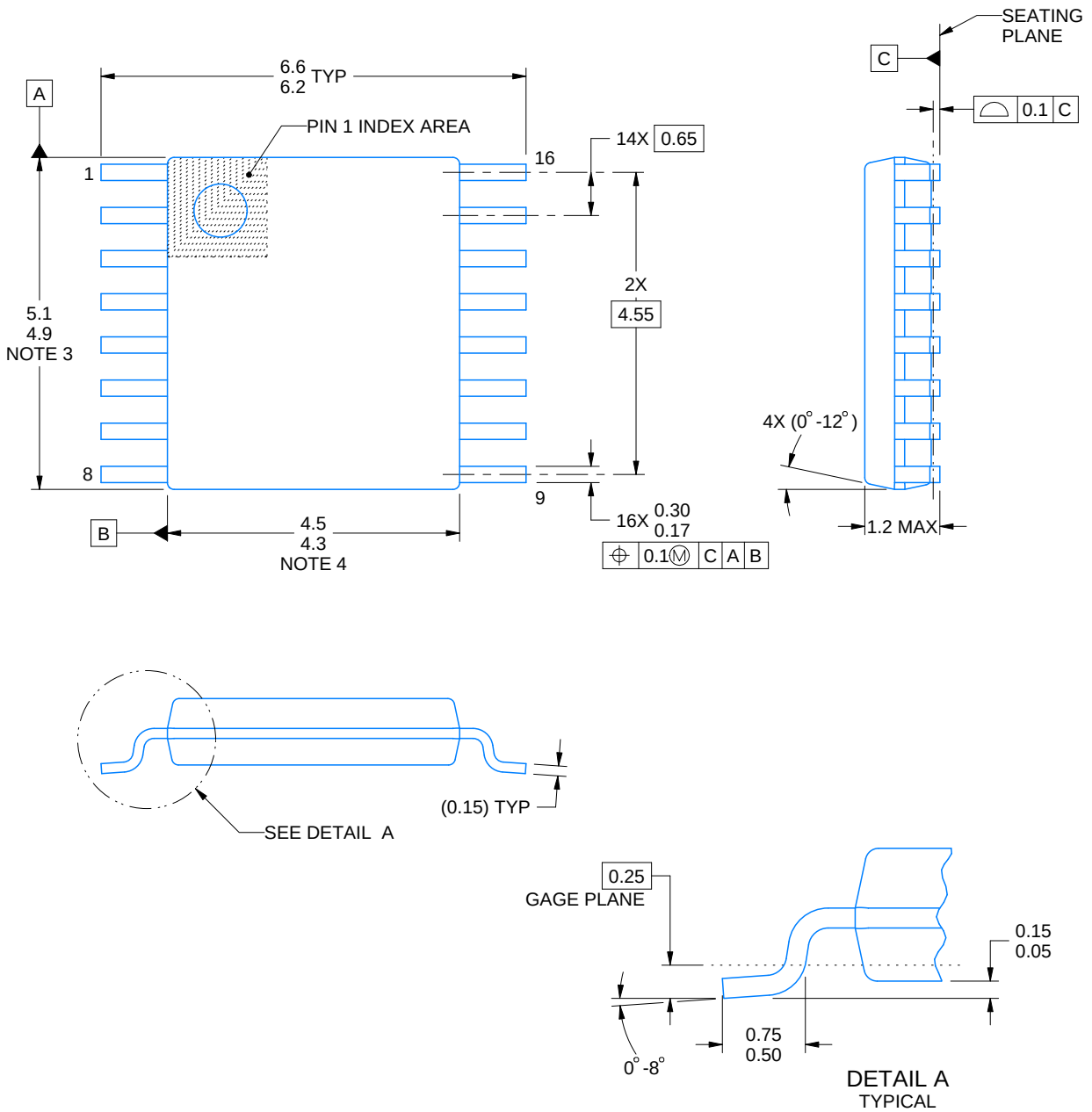
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA250A1QPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0
INA250A2QPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0
INA250A3QPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0
INA250A4QPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0016A

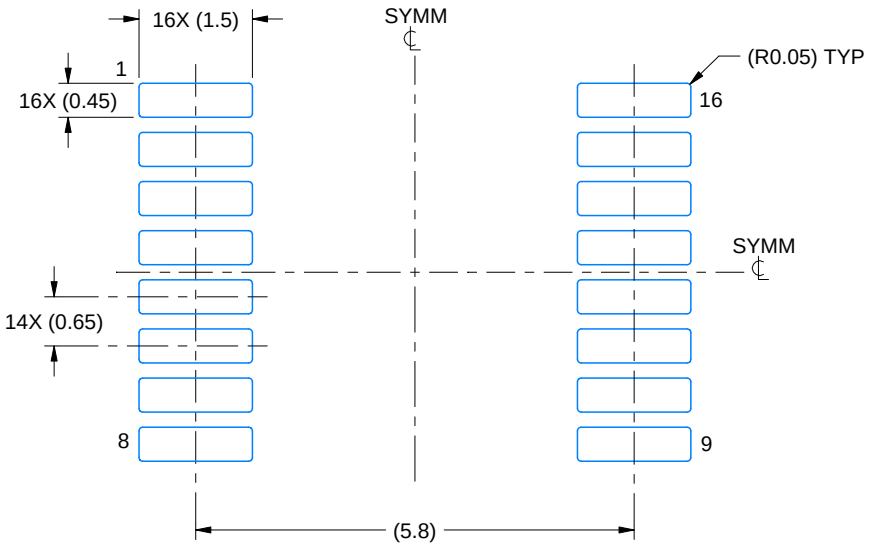
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



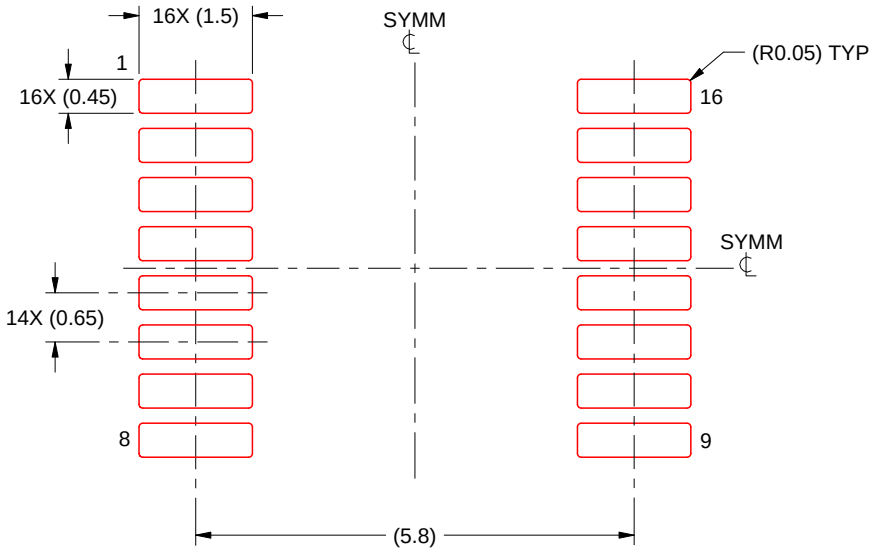
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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