INA219 ゼロドリフト、双方向電流/電力モニタ、I²Cインターフェイス搭載

1 特長

- 0～26Vのバス電圧を検出
- 電流、電圧、電力を報告
- 16のアドレスをプログラム可能
- 高精度: 全温度範囲にわたって0.5% (最大値、INA219B)
- フィルタ処理オプション
- 較正レジスタ
- SOT23-8およびSOIC-8パッケージ

2 アプリケーション

- サーバー
- 通信機器
- ノートブック・コンピュータ
- パワー・マネージメント
- バッテリ充電器
- 溶接機器
- 電源
- 試験用機器

3 概要

INA219は、I²CまたはSMBUS互換インターフェイスを搭載した電流シャントおよび電力モニタです。このデバイスはシャント電圧降下とバス電源電圧の両方を監視し、変換時間とフィルタ処理をプログラム可能です。プログラム可能な較正値と、内部的なマルチプライヤとの組み合わせにより、電流の値をアンペア単位で直接読み出すことが可能です。追加の乗算レジスタにより、電力がワット単位で計算されます。I²CまたはSMBUS互換のインターフェイスにより、16のアドレスをプログラム可能です。

INA219にはAとBの2つのグレードが存在し、Bグレードのほうが高い正確度と精度の仕様を満たしています。

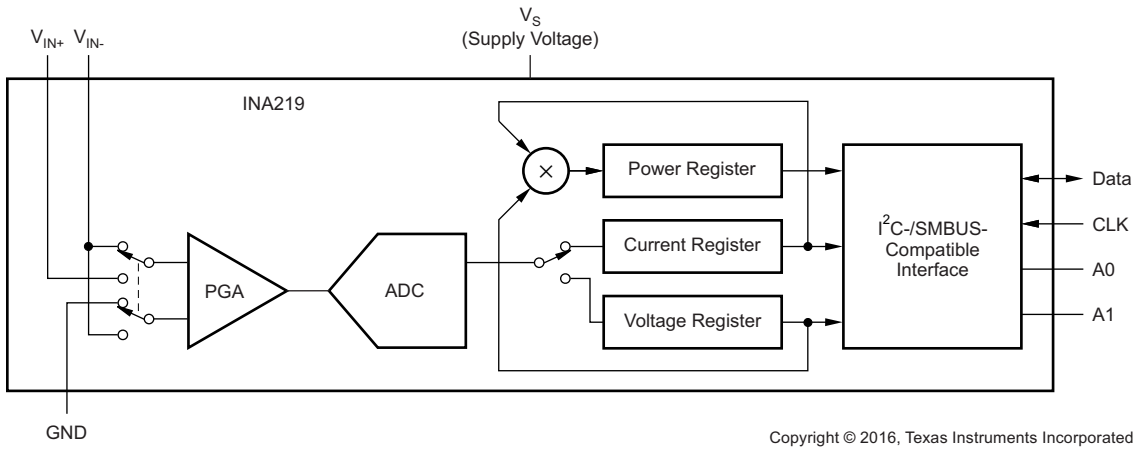
INA219は0～26Vの範囲のバス上でシャント両端の電圧を検出できます。このデバイスは3～5.5Vの単一電源で動作し、消費電流は最大1mAです。INA219は-40℃～125℃で動作します。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
INA219	SOIC (8)	3.91mm×4.90mm
	SOT-23 (8)	1.63mm×2.90mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision F (September 2011) から **Revision G** に変更 **Page**

- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- Updated *Bus Timing Diagram Definitions* table. I^2C timing table values were previously based on simulation and not characterized ... 6

Revision E (September 2010) から **Revision F** に変更 **Page**

- Changed step 5 and step 6 values in Table 8 ... 26

Revision D (September 2010) から **Revision E** に変更 **Page**

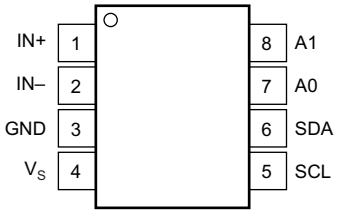
- Updated *Packaging Information* table ... 3

5 Related Products

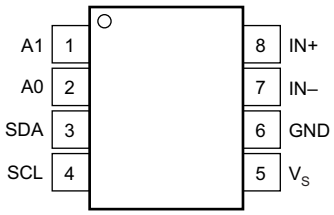
DEVICE	DESCRIPTION
INA209	Current/power monitor with watchdog, peak-hold, and fast comparator functions
INA210, INA211, INA212, INA213, INA214	Zerø-drift, low-cost, analog current shunt monitor series in small package

6 Pin Configuration and Functions

DCN Package
8-Pin SOT-23
Top View



D Package
8-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23	SOIC		
IN+	1	8	Analog Input	Positive differential shunt voltage. Connect to positive side of shunt resistor.
IN–	2	7	Analog Input	Negative differential shunt voltage. Connect to negative side of shunt resistor. Bus voltage is measured from this pin to ground.
GND	3	6	Analog	Ground
V_S	4	5	Analog	Power supply, 3 to 5.5 V
SCL	5	4	Digital Input	Serial bus clock line
SDA	6	3	Digital I/O	Serial bus data line
A0	7	2	Digital Input	Address pin. Table 1 shows pin settings and corresponding addresses.
A1	8	1	Digital Input	Address pin. Table 1 shows pin settings and corresponding addresses.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage		6	V
Analog Inputs IN+, IN–	Differential (V_{IN+} – $V_{IN–}$)(2)	–26	26	V
	Common-mode(V_{IN+} + $V_{IN–}$) / 2	-0.3	26	V
SDA		GND – 0.3	6	V
SCL		GND – 0.3	V_S + 0.3	V
Input current into any pin			5	mA
Open-drain digital output current			10	mA
Operating temperature		–40	125	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ may have a differential voltage of –26 to 26 V; however, the voltage at these pins must not exceed the range –0.3 to 26 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±750	
		Machine Model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{CM}		12		V
V_S		3.3		V
T_A	–25		85	ºC

7.4 Thermal Information

THERMAL METRIC(1)		INA219		UNIT
		D (SOIC)	DCN (SOT)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.3	135.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.9	68.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52	48.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.7	9.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.5	48.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics:

At T_A = 25°C, V_S = 3.3 V, V_{IN+} = 12V, V_{SHUNT} = (V_{IN+} – $V_{IN–}$) = 32 mV, PGA = /1, and BRNG(1) = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	INA219A			INA219B			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT									
V_{SHUNT}	Full-scale current sense (input) voltage range	PGA = /1	0		±40	0		±40	mV
		PGA = /2	0		±80	0		±80	mV
		PGA = /4	0		±160	0		±160	mV
		PGA = /8	0		±320	0		±320	mV
	Bus voltage (input voltage) range(2)	BRNG = 1	0		32	0		32	V
		BRNG = 0	0		16	0		16	V
CMRR	Common-mode rejection	V_{IN+} = 0 to 26 V	100	120		100	120		dB
V_{OS}	Offset voltage, RTI(3)	PGA = /1		±10	±100		±10	±50(4)	µV
		PGA = /2		±20	±125		±20	±75(4)	µV
		PGA = /4		±30	±150		±30	±75(4)	µV
		PGA = /8		±40	±200		±40	±100(4)	µV
	vs Temperature	T_A = –25°C to 85°C		0.1			0.1		µV/°C
PSRR	vs Power Supply	V_S = 3 to 5.5 V		10			10		µV/V
	Current sense gain error			±40			±40		m%
	vs Temperature	T_A = –25°C to 85°C		1			1		m%/°C
	IN+ pin input bias current	Active mode		20			20		µA
	IN– pin input bias current || $V_{IN–}$ pin input impedance	Active mode		20 || 320			20 || 320		µA || kΩ
	IN+ pin input leakage(5)	Power-down mode		0.1	±0.5		0.1	±0.5	µA
	IN– pin input leakage(5)	Power-down mode		0.1	±0.5		0.1	±0.5	µA
DC ACCURACY									
	ADC basic resolution			12			12		bits
	Shunt voltage, 1 LSB step size			10			10		µV
	Bus voltage, 1 LSB step size			4			4		mV
	Current measurement error			±0.2%	±0.5%		±0.2%	±0.3%(4)	
	over Temperature	T_A = –25°C to 85°C			±1%			±0.5%(4)	
	Bus voltage measurement error			±0.2%	±0.5%		±0.2%	±0.5%	
	over Temperature	T_A = –25°C to 85°C			±1%			±1%	
	Differential nonlinearity			±0.1			±0.1		LSB
ADC TIMING									
	ADC conversion time	12 bit		532	586		532	586	µs
		11 bit		276	304		276	304	µs
		10 bit		148	163		148	163	µs
		9 bit		84	93		84	93	µs
	Minimum convert input low time		4			4			µs
SMBus									
SMBus timeout(6)				28	35		28	35	ms
DIGITAL INPUTS (SDA as Input, SCL, A0, A1)									
	Input capacitance			3			3		pF
	Leakage input current	0 ≤ V_{IN} ≤ V_S		0.1	1		0.1	1	µA
	V_{IH} input logic level		0.7 (V_S)		6	0.7 (V_S)		6	V
	V_{IL} input logic level		–0.3		0.3 (V_S)	–0.3		0.3 (V_S)	V

(1) BRNG is bit 13 of the Configuration register 00h in Figure 19.
(2) This parameter only expresses the full-scale range of the ADC scaling. In no event should more than 26 V be applied to this device.
(3) Referred-to-input (RTI)
(4) Indicates improved specifications of the INA219B.
(5) Input leakage is positive (current flowing into the pin) for the conditions shown at the top of the table. Negative leakage currents can occur under different input conditions.
(6) SMBus timeout in the INA219 resets the interface any time SCL or SDA is low for over 28 ms.

Electrical Characteristics: (continued)

At T_A = 25°C, V_S = 3.3 V, V_{IN+} = 12V, V_{SHUNT} = (V_{IN+} – $V_{IN–}$) = 32 mV, PGA = /1, and BRNG(1) = 1, unless otherwise noted.

PARAMETER	TEST CONDITIONS	INA219A			INA219B			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Hysteresis			500			500		mV
OPEN-DRAIN DIGITAL OUTPUTS (SDA)								
Logic 0 output level	I_{SINK} = 3 mA		0.15	0.4		0.15	0.4	V
High-level output leakage current	V_{OUT} = V_S		0.1	1		0.1	1	µA
POWER SUPPLY								
Operating supply range		3		5.5	3		5.5	V
Quiescent current			0.7	1		0.7	1	mA
Quiescent current, power-down mode			6	15		6	15	µA
Power-on reset threshold			2			2		V

7.6 Bus Timing Diagram Definitions(1)

		FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	0.001	0.4	0.001	2.56	MHz
$t_{(BUF)}$	Bus free time between STOP and START condition	1300		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	600		160		ns
$t_{(SUSTA)}$	Repeated START condition setup time	600		160		ns
$t_{(SUSTO)}$	STOP condition setup time	600		160		ns
$t_{(HDDAT)}$	Data hold time	0	900	0	90	ns
$t_{(SUDAT)}$	Data setup time	100		10		ns
$t_{(LOW)}$	SCL clock LOW period	1300		250		ns
$t_{(HIGH)}$	SCL clock HIGH period	600		60		ns
t_F DA	Data fall time		300		150	ns
t_FCL	Clock fall time		300		40	ns
t_RCL	Clock rise time		300		40	ns
t_RCL	Clock rise time for SCLK ≤ 100kHz		1000			ns

(1) Values based on a statistical analysis of a one-time sample of devices. Minimum and maximum values are not ensured and not production tested.

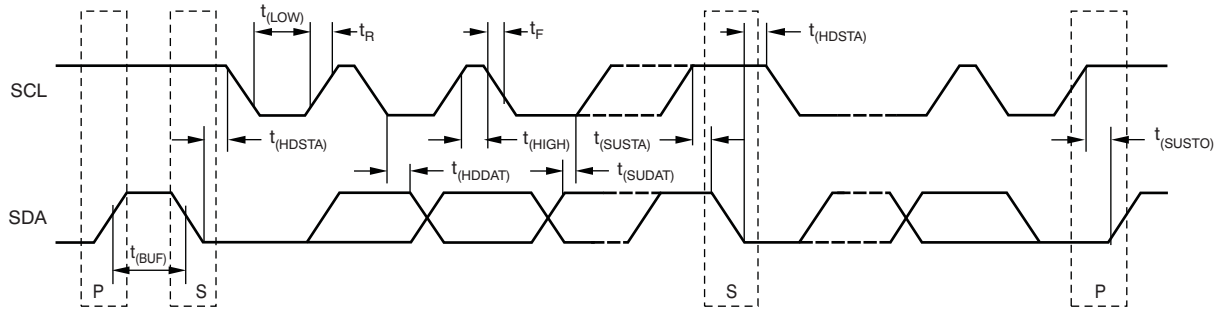


Figure 1. Bus Timing Diagram

7.7 Typical Characteristics

At T_A = 25°C, V_S = 3.3 V, V_{IN+} = 12 V, V_{SHUNT} = (V_{IN+} – $V_{IN–}$) = 32 mV, PGA = /1, and BRNG = 1, unless otherwise noted.

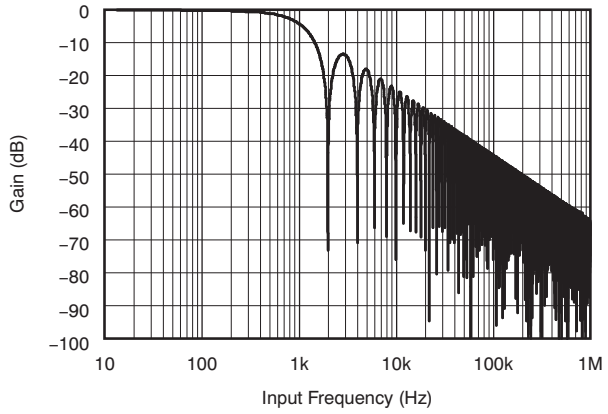


Figure 2. Frequency Response

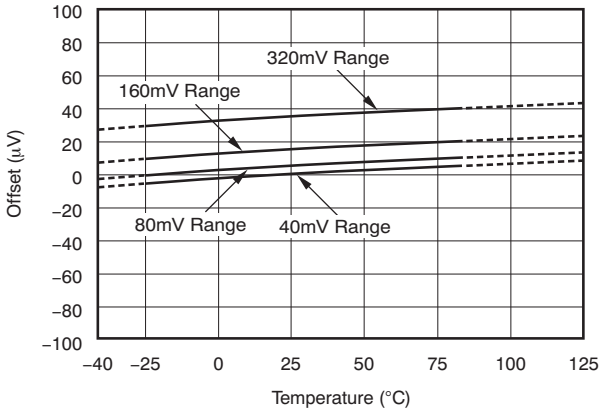


Figure 3. ADC Shunt Offset vs Temperature

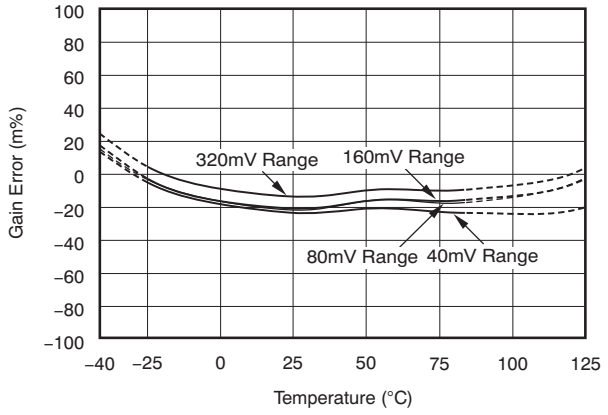


Figure 4. ADC Shunt Gain Error vs Temperature

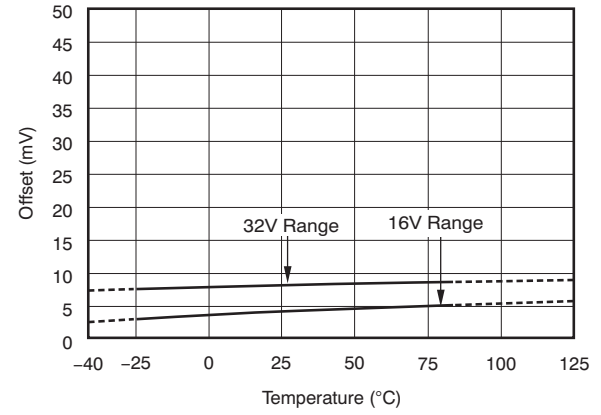


Figure 5. ADC Bus Voltage Offset vs Temperature

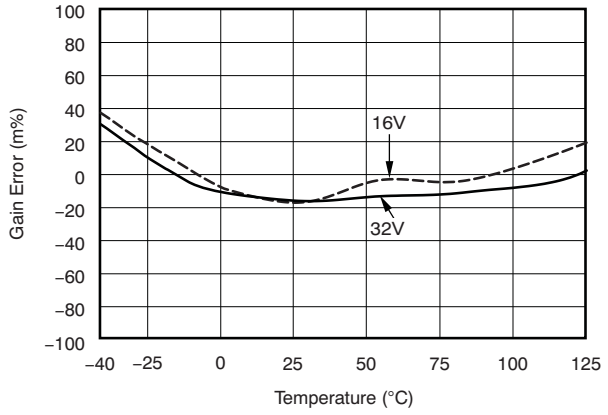


Figure 6. ADC Bus Gain Error vs Temperature

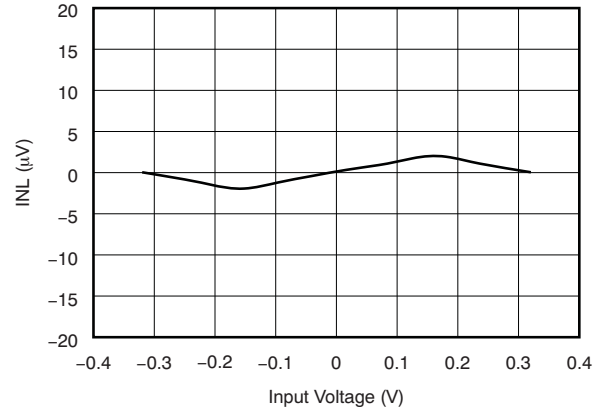


Figure 7. Integral Nonlinearity vs Input Voltage

Typical Characteristics (continued)

At T_A = 25°C, V_S = 3.3 V, V_{IN+} = 12 V, V_{SHUNT} = (V_{IN+} – $V_{IN–}$) = 32 mV, PGA = /1, and BRNG = 1, unless otherwise noted.

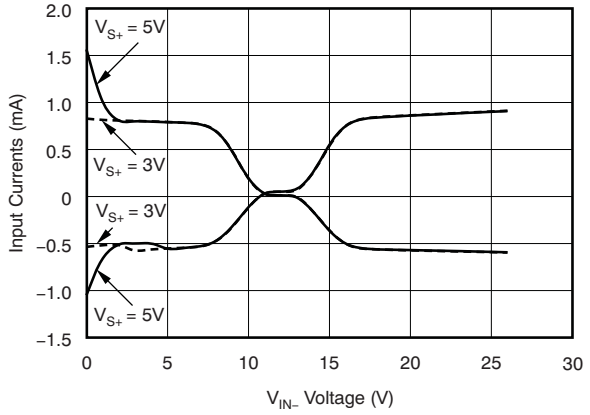


Figure 8. Input Currents With Large Differential Voltages(V_{IN+} at 12 V, Sweep Of $V_{IN–}$)

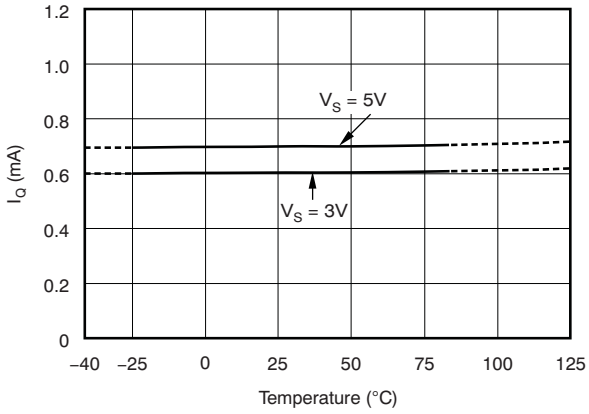


Figure 9. Active I_Q vs Temperature

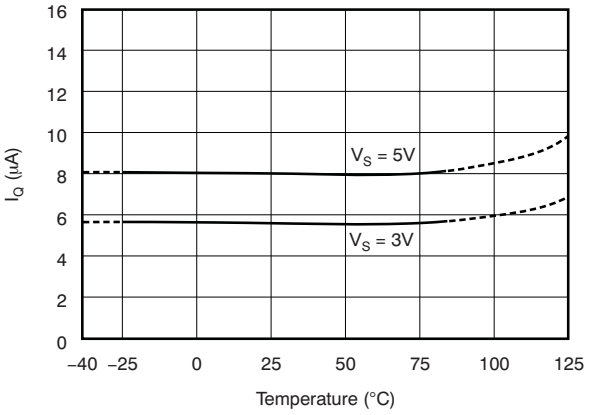


Figure 10. Shutdown I_Q vs Temperature

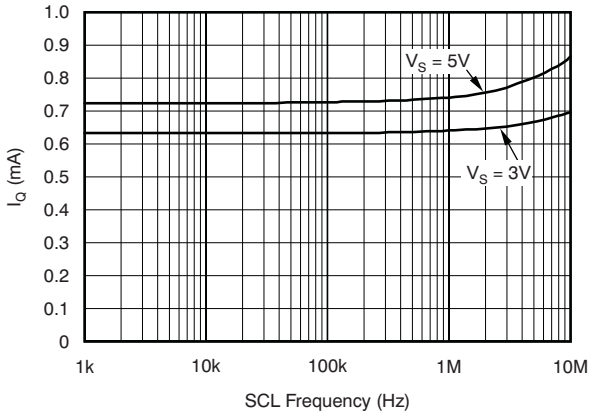


Figure 11. Active I_Q vs I^2C Clock Frequency

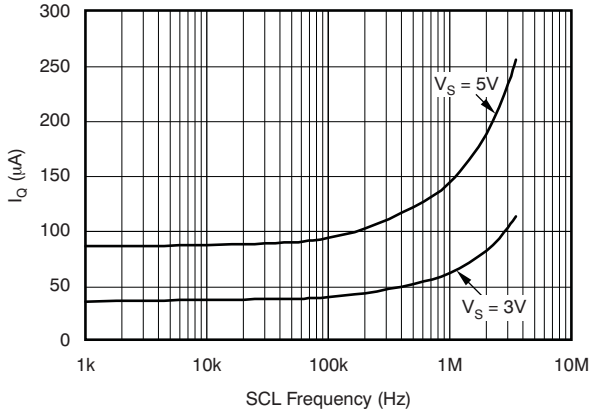


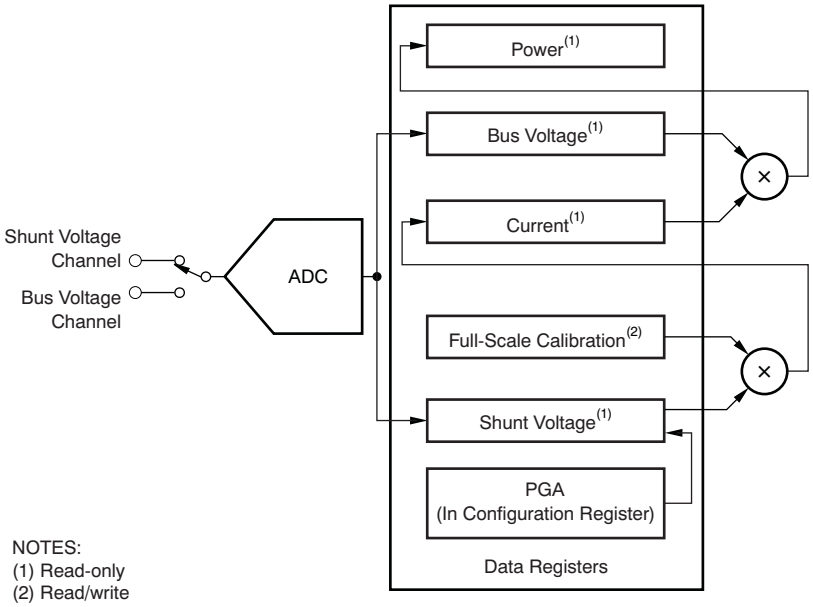
Figure 12. Shutdown I_Q vs I^2C Clock Frequency

8 Detailed Description

8.1 Overview

The INA219 is a digital current sense amplifier with an I^{2}C- and SMBus-compatible interface. It provides digital current, voltage, and power readings necessary for accurate decision-making in precisely-controlled systems. Programmable registers allow flexible configuration for measurement resolution as well as continuous-versus-triggered operation. Detailed register information appears at the end of this data sheet, beginning with Table 2. See the *Functional Block Diagram* section for a block diagram of the INA219 device.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Basic ADC Functions

The two analog inputs to the INA219, IN+ and IN–, connect to a shunt resistor in the bus of interest. The INA219 is typically powered by a separate supply from 3 to 5.5 V. The bus being sensed can vary from 0 to 26 V. There are no special considerations for power-supply sequencing (for example, a bus voltage can be present with the supply voltage off, and vice-versa). The INA219 senses the small drop across the shunt for shunt voltage, and senses the voltage with respect to ground from IN– for the bus voltage. Figure 13 shows this operation.

When the INA219 is in the normal operating mode (that is, MODE bits of the Configuration register are set to 111), it continuously converts the shunt voltage up to the number set in the shunt voltage averaging function (Configuration register, SADC bits). The device then converts the bus voltage up to the number set in the bus voltage averaging (Configuration register, BADC bits). The Mode control in the Configuration register also permits selecting modes to convert only voltage or current, either continuously or in response to an event (triggered).

All current and power calculations are performed in the background and do not contribute to conversion time; conversion times shown in the *Electrical Characteristics:* can be used to determine the actual conversion time.

Power-Down mode reduces the quiescent current and turns off current into the INA219 inputs, avoiding any supply drain. Full recovery from Power-Down requires 40 μs. ADC Off mode (set by the Configuration register, MODE bits) stops all conversions.

Writing any of the triggered convert modes into the Configuration register (even if the desired mode is already programmed into the register) triggers a single-shot conversion. Table 6 lists the triggered convert mode settings.

Feature Description (continued)

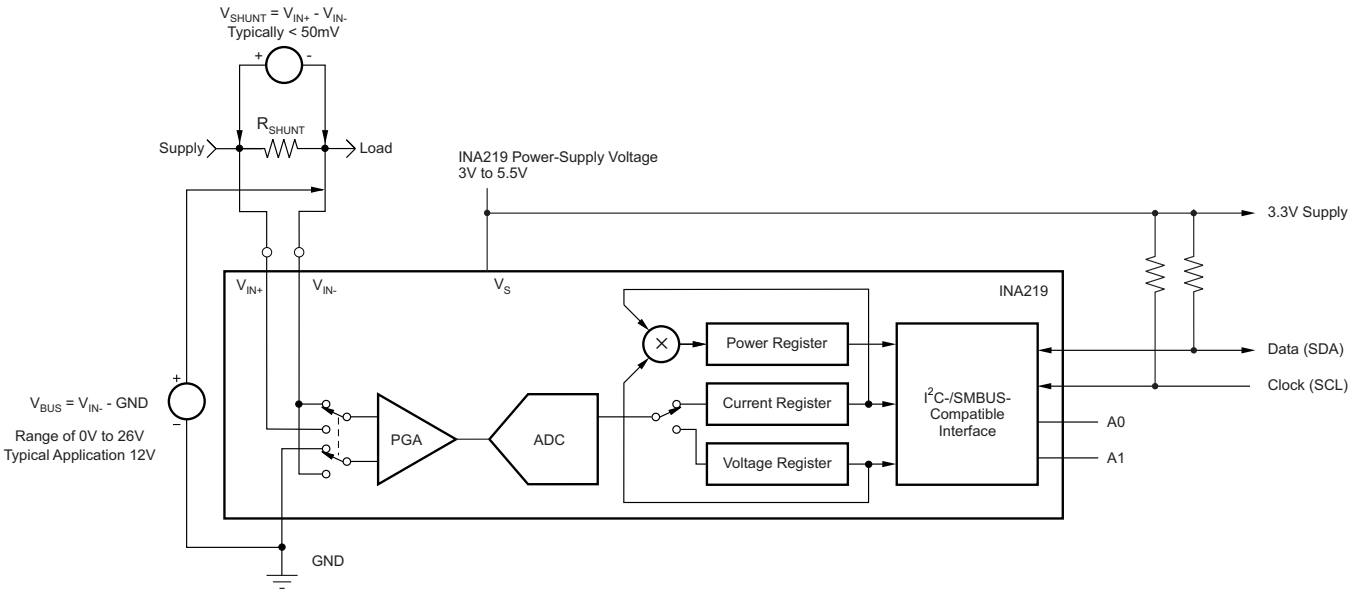


Figure 13. INA219 Configured for Shunt and Bus Voltage Measurement

Although the INA219 can be read at any time, and the data from the last conversion remain available, the conversion ready bit (Status register, CNVR bit) is provided to help coordinate one-shot or triggered conversions. The conversion ready bit is set after all conversions, averaging, and multiplication operations are complete.

The conversion ready bit clears under any of these conditions:

- Writing to the Configuration register, except when configuring the MODE bits for power down or ADC off (disable) modes
- Reading the Status register
- Triggering a single-shot conversion with the convert pin

8.3.1.1 Power Measurement

Current and bus voltage are converted at different points in time, depending on the resolution and averaging mode settings. For instance, when configured for 12-bit and 128 sample averaging, up to 68 ms in time between sampling these two values is possible. Again, these calculations are performed in the background and do not add to the overall conversion time.

8.3.1.2 PGA Function

If larger full-scale shunt voltages are desired, the INA219 provides a PGA function that increases the full-scale range up to 2, 4, or 8 times (320 mV). Additionally, the bus voltage measurement has two full-scale ranges: 16 or 32 V.

8.3.1.3 Compatibility With TI Hot Swap Controllers

The INA219 is designed for compatibility with hot swap controllers such the TI TPS2490. The TPS2490 uses a high-side shunt with a limit at 50 mV; the INA219 full-scale range of 40 mV enables the use of the same shunt for current sensing below this limit. When sensing is required at (or through) the 50-mV sense point of the TPS2490, the PGA of the INA219 can be set to /2 to provide an 80-mV full-scale range.

8.4 Device Functional Modes

8.4.1 Filtering and Input Considerations

Measuring current is often noisy, and such noise can be difficult to define. The INA219 offers several options for filtering by choosing resolution and averaging in the Configuration register. These filtering options can be set independently for either voltage or current measurement.

The internal ADC is based on a delta-sigma (ΔΣ) front-end with a 500-kHz (±30%) typical sampling rate. This architecture has good inherent noise rejection; however, transients that occur at or very close to the sampling rate harmonics can cause problems. Because these signals are at 1 MHz and higher, they can be dealt with by incorporating filtering at the input of the INA219. The high frequency enables the use of low-value series resistors on the filter for negligible effects on measurement accuracy. In general, filtering the INA219 input is only necessary if there are transients at exact harmonics of the 500-kHz (±30%) sampling rate (>1 MHz). Filter using the lowest possible series resistance and ceramic capacitor. Recommended values are 0.1 to 1 μF. Figure 14 shows the INA219 with an additional filter added at the input.

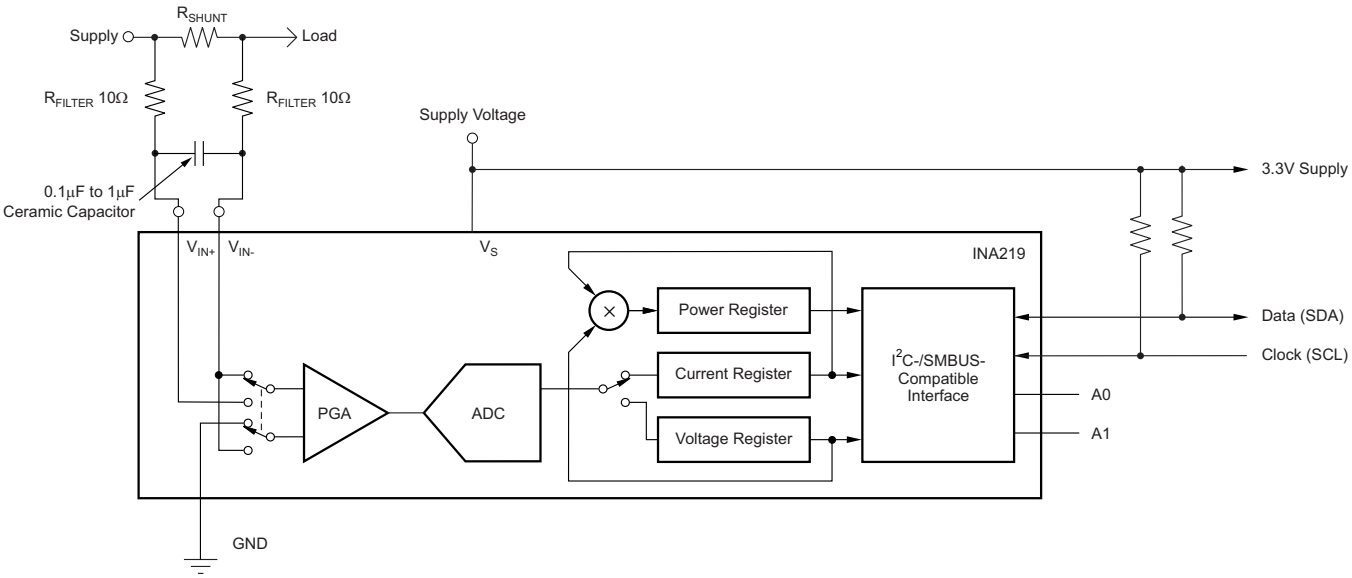


Figure 14. INA219 With Input Filtering

Overload conditions are another consideration for the INA219 inputs. The INA219 inputs are specified to tolerate 26 V across the inputs. A large differential scenario might be a short to ground on the load side of the shunt. This type of event can result in full power-supply voltage across the shunt (as long the power supply or energy storage capacitors support it). It must be remembered that removing a short to ground can result in inductive kickbacks that could exceed the 26-V differential and common-mode rating of the INA219. Inductive kickback voltages are best dealt with by zener-type transient-absorbing devices combined with sufficient energy storage capacitance.

In applications that do not have large energy storage electrolytics on one or both sides of the shunt, an input overstress condition may result from an excessive dV/dt of the voltage applied to the input. A hard physical short is the most likely cause of this event, particularly in applications with no large electrolytics present. This problem occurs because an excessive dV/dt can activate the ESD protection in the INA219 in systems where large currents are available. Testing has demonstrated that the addition of 10-Ω resistors in series with each input of the INA219 sufficiently protects the inputs against dV/dt failure up to the 26-V rating of the INA219. These resistors have no significant effect on accuracy.

8.5 Programming

An important aspect of the INA219 device is that it measure current or power if it is programmed based on the system. The device measures both the differential voltage applied between the IN+ and IN- input pins and the voltage at IN- pin. In order for the device to report both current and power values, the user must program the resolution of the Current Register (04h) and the value of the shunt resistor (R_{SHUNT}) present in the application to develop the differential voltage applied between the input pins. Both the Current_LSB and shunt resistor value are used in the calculation of the Calibration Register value that the device uses to calculate the corresponding current and power values based on the measured shunt and bus voltages.

After programming the Calibration Register, the Current Register (04h) and Power Register (03h) update accordingly based on the corresponding shunt voltage and bus voltage measurements. Until the Calibration Register is programmed, the Current Register (04h) and Power Register (03h) remain at zero.

8.5.1 Programming the Calibration Register

The Calibration Register is calculated based on Equation 1. This equation includes the term Current_LSB, which is the programmed value for the LSB for the Current Register (04h). The user uses this value to convert the value in the Current Register (04h) to the actual current in amperes. The highest resolution for the Current Register (04h) can be obtained by using the smallest allowable Current_LSB based on the maximum expected current as shown in Equation 2. While this value yields the highest resolution, it is common to select a value for the Current_LSB to the nearest round number above this value to simplify the conversion of the Current Register (04h) and Power Register (03h) to amperes and watts respectively. The R_{SHUNT} term is the value of the external shunt used to develop the differential voltage across the input pins. The Power Register (03h) is internally set to be 20 times the programmed Current_LSB see Equation 3.

$$Cal = \text{trunc}\left(\frac{0.04096}{\text{Current\_LSB} \times R_{SHUNT}}\right) \quad (1)$$

where

- 0.04096 is an internal fixed value used to ensure scaling is maintained properly

$$\text{Current\_LSB} = \frac{\text{Maximum Expected Current}}{2^{15}} \quad (2)$$

$$\text{Power\_LSB} = 20\ \text{Current\_LSB} \quad (3)$$

Shunt voltage is calculated by multiplying the Shunt Voltage Register contents with the Shunt Voltage LSB of 10 µV.

The Bus Voltage register bits are not right-aligned. In order to compute the value of the Bus Voltage, Bus Voltage Register contents must be shifted right by three bits. This shift puts the BD0 bit in the LSB position so that the contents can be multiplied by the Bus Voltage LSB of 4-mV to compute the bus voltage measured by the device.

After programming the Calibration Register, the value expected in the Current Register (04h) can be calculated by multiplying the Shunt Voltage register contents by the Calibration Register and then dividing by 4096 as shown in Equation 4. To obtain a value in amperes the Current register value is multiplied by the programmed Current_LSB.

$$\text{Current Register} = \frac{\text{Shunt Voltage Register} \times \text{Calibration Register}}{4096} \quad (4)$$

The value expected in the Power register (03h) can be calculated by multiplying the Current register value by the Bus Voltage register value and then dividing by 5000 as shown in Equation 5. Power Register content is multiplied by Power LSB which is 20 times the Current_LSB for a power value in watts.

$$\text{Power Register} = \frac{\text{Current Register} \times \text{Bus Voltage Register}}{5000} \quad (5)$$

Programming (continued)

8.5.2 Programming the Power Measurement Engine

8.5.2.1 Calibration Register and Scaling

The Calibration Register enables the user to scale the Current Register (04h) and Power Register (03h) to the most useful value for a given application. For example, set the Calibration Register such that the largest possible number is generated in the Current Register (04h) or Power Register (03h) at the expected full-scale point. This approach yields the highest resolution using the previously calculated minimum Current_LSB in the equation for the Calibration Register. The Calibration Register can also be selected to provide values in the Current Register (04h) and Power Register (03h) that either provide direct decimal equivalents of the values being measured, or yield a round LSB value for each corresponding register. After these choices have been made, the Calibration Register also offers possibilities for end user system-level calibration. After determining the exact current by using an external ammeter, the value of the Calibration Register can then be adjusted based on the measured current result of the INA219 to cancel the total system error as shown in Equation 6.

$$\text{Corrected\_Full\_Scale\_Cal} = \text{trunc}\left(\frac{\text{Cal} \times \text{MeasShuntCurrent}}{\text{INA219\_Current}}\right) \quad (6)$$

8.5.3 Simple Current Shunt Monitor Usage (No Programming Necessary)

The INA219 can be used without any programming if it is only necessary to read a shunt voltage drop and bus voltage with the default 12-bit resolution, 320-mV shunt full-scale range (PGA = /8), 32-V bus full-scale range, and continuous conversion of shunt and bus voltage.

Without programming, current is measured by reading the shunt voltage. The Current register and Power register are only available if the Calibration register contains a programmed value.

8.5.4 Default Settings

The default power-up states of the registers are shown in the *Register Details* section of this data sheet. These registers are volatile, and if programmed to other than default values, must be re-programmed at every device power-up. Detailed information on programming the Calibration register specifically is given in the section, *Programming the Calibration Register*.

8.5.5 Bus Overview

The INA219 offers compatibility with both I^2C and SMBus interfaces. The I^2C and SMBus protocols are essentially compatible with one another.

The I^2C interface is used throughout this data sheet as the primary example, with SMBus protocol specified only when a difference between the two systems is being addressed. Two bidirectional lines, SCL and SDA, connect the INA219 to the bus. Both SCL and SDA are open-drain connections.

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a HIGH to a LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and eight bits of data are sent, followed by an *Acknowledge* bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH is interpreted as a START or STOP condition.

Once all data have been transferred, the master generates a STOP condition, indicated by pulling SDA from LOW to HIGH while SCL is HIGH. The INA219 includes a 28-ms timeout on its interface to prevent locking up an SMBus.

Programming (continued)

8.5.5.1 Serial Bus Address

To communicate with the INA219, the master must first address slave devices through a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

The INA219 has two address pins, A0 and A1. Table 1 describes the pin logic levels for each of the 16 possible addresses. The state of pins A0 and A1 is sampled on every bus communication and should be set before any activity on the interface occurs. The address pins are read at the start of each communication event.

Table 1. INA219 Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V_{S+}	1000001
GND	SDA	1000010
GND	SCL	1000011
V_{S+}	GND	1000100
V_{S+}	V_{S+}	1000101
V_{S+}	SDA	1000110
V_{S+}	SCL	1000111
SDA	GND	1001000
SDA	V_{S+}	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V_{S+}	1001101
SCL	SDA	1001110
SCL	SCL	1001111

8.5.5.2 Serial Interface

The INA219 operates only as a slave device on the I^2C bus and SMBus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The INA219 supports the transmission protocol for fast (1- to 400-kHz) and high-speed (1-kHz to 2.56-MHz) modes. All data bytes are transmitted most significant byte first.

8.5.6 Writing to and Reading from the INA219

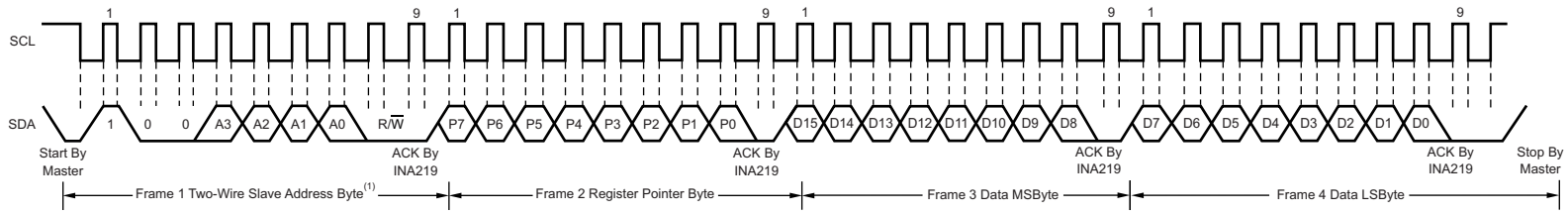
Accessing a particular register on the INA219 is accomplished by writing the appropriate value to the register pointer. Refer to Table 2 for a complete list of registers and corresponding addresses. The value for the register pointer as shown in Figure 18 is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit LOW. Every write operation to the INA219 requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the master. This byte is the slave address, with the R/$\overline{W}$ bit LOW. The INA219 then acknowledges receipt of a valid address. The next byte transmitted by the master is the address of the register to which data will be written. This register address value updates the register pointer to the desired register. The next two bytes are written to the register addressed by the register pointer. The INA219 acknowledges receipt of each data byte. The master may terminate data transfer by generating a START or STOP condition.

When reading from the INA219, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit LOW, followed by the register pointer byte. No additional data are required. The master then generates a START condition and sends the slave address byte with the R/$\overline{W}$ bit HIGH to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register

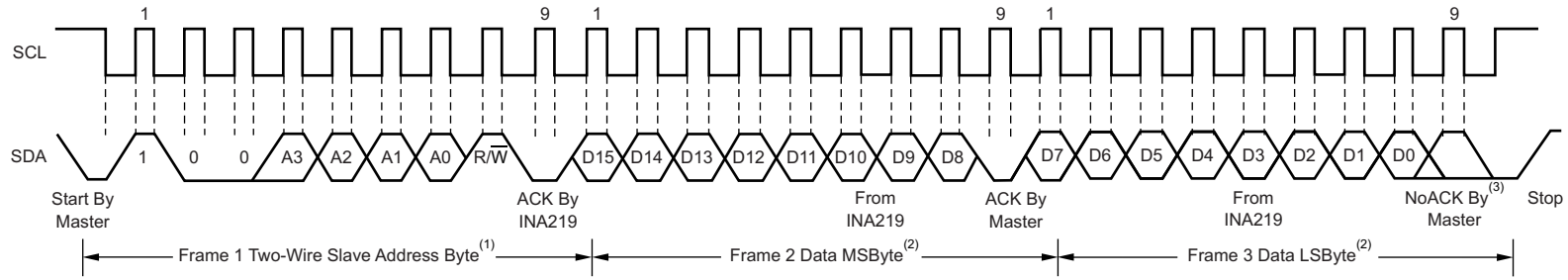
pointer. This byte is followed by an *Acknowledge* from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a *Not-Acknowledge* after receiving any data byte, or generating a START or STOP condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the INA219 retains the register pointer value until it is changed by the next write operation.

Figure 15 and Figure 16 show write and read operation timing diagrams, respectively. Note that register bytes are sent most-significant byte first, followed by the least significant byte. Figure 17 shows the timing diagram for the SMBus Alert response operation. Figure 18 shows a typical register pointer configuration.



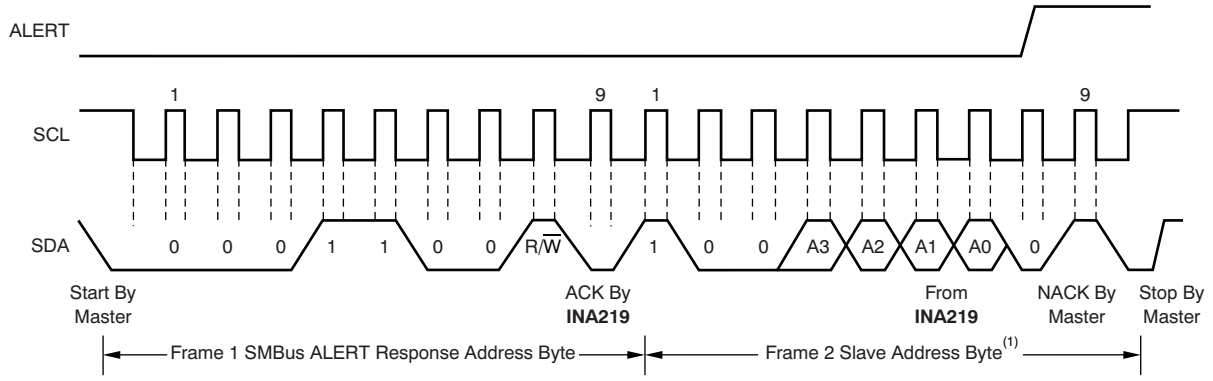
NOTE (1): The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

Figure 15. Timing Diagram for Write Word Format



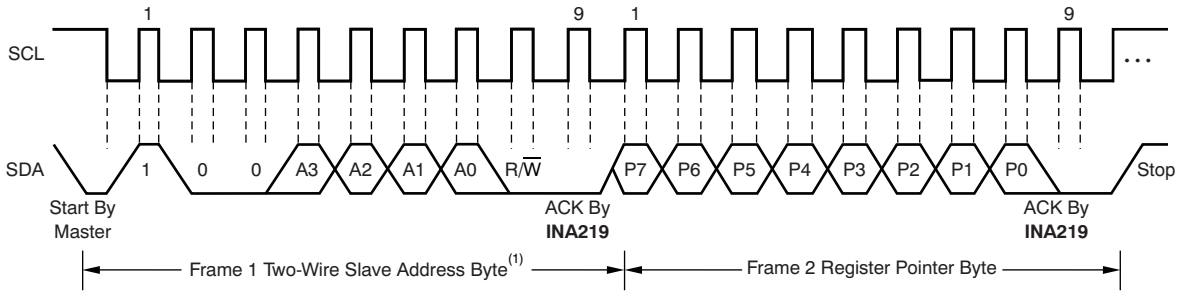
NOTES: (1) The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.
(2) Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated. See Figure 19.
(3) ACK by Master can also be sent.

Figure 16. Timing Diagram for Read Word Format



NOTE (1): The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

Figure 17. Timing Diagram for SMBus Alert



NOTE (1): The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

Figure 18. Typical Register Pointer Set

8.5.6.1 High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pull-up devices. The master generates a start condition followed by a valid serial byte containing high-speed (HS) master code *00001XXX*. This transmission is made in fast (400 kbps) or standard (100 kbps) (F/S) mode at no more than 400 kbps. The INA219 does not acknowledge the HS master code, but does recognize it and switches its internal filters to support 2.56 Mbps operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.56 Mbps are allowed. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the INA219 to support the F/S mode. For bus timing, see *Bus Timing Diagram Definitions*(1) and Figure 1.

8.5.6.2 Power-Up Conditions

Power-up conditions apply to a software reset through the RST bit (bit 15) in the Configuration register, or the I²C bus General Call Reset.

(1) Values based on a statistical analysis of a one-time sample of devices. Minimum and maximum values are not ensured and not production tested.

8.6 Register Maps

8.6.1 Register Information

The INA219 uses a bank of registers for holding configuration settings, measurement results, maximum/minimum limits, and status information. Table 2 summarizes the INA219 registers; *Functional Block Diagram* shows registers.

Register contents are updated 4 μs after completion of the write command. Therefore, a 4-μs delay is required between completion of a write to a given register and a subsequent read of that register (without changing the pointer) when using SCL frequencies in excess of 1 MHz.

Table 2. Summary of Register Set

POINTER ADDRESS	REGISTER NAME	FUNCTION	POWER-ON RESET		TYPE(1)
HEX			BINARY	HEX	
00	Configuration	All-register reset, settings for bus voltage range, PGA Gain, ADC resolution/averaging.	00111001 10011111	399F	R/$\overline{W}$
01	Shunt voltage	Shunt voltage measurement data.	Shunt voltage	—	R
02	Bus voltage	Bus voltage measurement data.	Bus voltage	—	R
03	Power(2)	Power measurement data.	00000000 00000000	0000	R
04	Current(2)	Contains the value of the current flowing through the shunt resistor.	00000000 00000000	0000	R
05	Calibration	Sets full-scale range and LSB of current and power measurements. Overall system calibration.	00000000 00000000	0000	R/$\overline{W}$

(1) Type: **R** = Read only, **R/$\overline{W}$** = Read/Write.
(2) The Power register and Current register default to 0 because the Calibration register defaults to 0, yielding a zero current value until the Calibration register is programmed.

8.6.2 Register Details

All INA219 16-bit registers are actually two 8-bit bytes through the I^2C interface.

8.6.2.1 Configuration Register (address = 00h) [reset = 399Fh]

Figure 19. Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	—	BRNG	PG1	PG0	BADC 4	BADC 3	BADC 2	BADC 1	SADC 4	SADC 3	SADC 2	SADC 1	MODE 3	MODE 2	MODE 1
R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3. Bit Descriptions

RST:	**Reset Bit**
Bit 15	Setting this bit to '1' generates a system reset that is the same as power-on reset. Resets all registers to default values; this bit self-clears.
BRNG:	**Bus Voltage Range**
Bit 13	0 = 16V FSR 1 = 32V FSR (default value)
PG:	**PGA (Shunt Voltage Only)**
Bits 11, 12	Sets PGA gain and range. Note that the PGA defaults to ÷8 (320mV range). Table 4 shows the gain and range for the various product gain settings.

Table 4. PG Bit Settings(1)

PG1	PG0	GAIN	Range
0	0	1	±40 mV
0	1	/2	±80 mV
1	0	/4	±160 mV
1	1	/8	±320 mV

(1) Shaded values are default.

BADC:	**BADC Bus ADC Resolution/Averaging**
Bits 7–10	These bits adjust the Bus ADC resolution (9-, 10-, 11-, or 12-bit) or set the number of samples used when averaging results for the Bus Voltage Register (02h).

SADC:	SADC Shunt ADC Resolution/Averaging
Bits 3–6	These bits adjust the Shunt ADC resolution (9-, 10-, 11-, or 12-bit) or set the number of samples used when averaging results for the Shunt Voltage Register (01h). BADC (Bus) and SADC (Shunt) ADC resolution/averaging and conversion time settings are shown in Table 5.

Table 5. ADC Settings(1)

ADC4	ADC3	ADC2	ADC1	Mode/Samples	Conversion Time
0	X(2)	0	0	9 bit	84 μs
0	X(2)	0	1	10 bit	148 μs
0	X(2)	1	0	11 bit	276 μs
0	X(2)	1	1	12 bit	532 μs
1	0	0	0	12 bit	532 μs
1	0	0	1	2	1.06 ms
1	0	1	0	4	2.13 ms
1	0	1	1	8	4.26 ms
1	1	0	0	16	8.51 ms
1	1	0	1	32	17.02 ms
1	1	1	0	64	34.05 ms
1	1	1	1	128	68.10 ms

(1) Shaded values are default.
(2) X = Don't care

MODE:	Operating Mode
Bits 0–2	Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The mode settings are shown in Table 6.

Table 6. Mode Settings(1)

MODE3	MODE2	MODE1	MODE
0	0	0	Power-down
0	0	1	Shunt voltage, triggered
0	1	0	Bus voltage, triggered
0	1	1	Shunt and bus, triggered
1	0	0	ADC off (disabled)
1	0	1	Shunt voltage, continuous
1	1	0	Bus voltage, continuous
1	1	1	Shunt and bus, continuous

(1) Shaded values are default.

8.6.3 Data Output Registers

8.6.3.1 Shunt Voltage Register (address = 01h)

The Shunt Voltage register stores the current shunt voltage reading, V_{SHUNT}. Shunt Voltage register bits are shifted according to the PGA setting selected in the Configuration register (00h). When multiple sign bits are present, they will all be the same value. Negative numbers are represented in 2's complement format. Generate the 2's complement of a negative number by complementing the absolute value binary number and adding 1. Extend the sign, denoting a negative number by setting the MSB = 1. Extend the sign to any additional sign bits to form the 16-bit word.

Example: For a value of V_{SHUNT} = –320 mV:

1. Take the absolute value (include accuracy to 0.01 mV) → 320.00
2. Translate this number to a whole decimal number → 32000
3. Convert it to binary → 111 1101 0000 0000

4. Complement the binary result : 000 0010 1111 1111
5. Add 1 to the Complement to create the Two's Complement formatted result → 000 0011 0000 0000
6. Extend the sign and create the 16-bit word: 1000 0011 0000 0000 = 8300h (Remember to extend the sign to all sign-bits, as necessary based on the PGA setting.)

At PGA = /8, full-scale range = ±320 mV (decimal = 32000). For V_{SHUNT} = +320 mV, Value = 7D00h; For V_{SHUNT} = –320 mV, Value = 8300h; and LSB = 10µV.

Figure 20. Shunt Voltage Register at PGA = /8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SD14_8	SD13_8	SD12_8	SD11_8	SD10_8	SD9_8	SD8_8	SD7_8	SD6_8	SD5_8	SD4_8	SD3_8	SD2_8	SD1_8	SD0_8

At PGA = /4, full-scale range = ±160 mV (decimal = 16000). For V_{SHUNT} = +160 mV, Value = 3E80h; For V_{SHUNT} = –160 mV, Value = C180h; and LSB = 10µV.

Figure 21. Shunt Voltage Register at PGA = /4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SIGN	SD13_4	SD12_4	SD11_4	SD10_4	SD9_4	SD8_4	SD7_4	SD6_4	SD5_4	SD4_4	SD3_4	SD2_4	SD1_4	SD0_4

At PGA = /2, full-scale range = ±80 mV (decimal = 8000). For V_{SHUNT} = +80 mV, Value = 1F40h; For V_{SHUNT} = –80 mV; Value = E0C0h; and LSB = 10µV.

Figure 22. Shunt Voltage Register at PGA = /2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SIGN	SIGN	SD12_2	SD11_2	SD10_2	SD9_2	SD8_2	SD7_2	SD6_2	SD5_2	SD4_2	SD3_2	SD2_2	SD1_2	SD0_2

At PGA = /1, full-scale range = ±40 mV (decimal = 4000). For V_{SHUNT} = +40 mV, Value = 0FA0h; For V_{SHUNT} = –40 mV, Value = F060h; and LSB = 10µV.

Figure 23. Shunt Voltage Register at PGA = /1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SIGN	SIGN	SIGN	SD11_1	SD10_1	SD9_1	SD8_1	SD7_1	SD6_1	SD5_1	SD4_1	SD3_1	SD2_1	SD1_1	SD0_1

Table 7. Shunt Voltage Register Format(1)

V_{SHUNT} Reading (mV)	Decimal Value	PGA = /8 (D15:D0)	PGA = /4 (D15:D0)	PGA = /2 (D15:D0)	PGA = /1 (D15:D0)
320.02	32002	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
320.01	32001	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
320.00	32000	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
319.99	31999	0111 1100 1111 1111	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
319.98	31998	0111 1100 1111 1110	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
⋮	⋮	⋮	⋮	⋮	⋮
160.02	16002	0011 1110 1000 0010	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
160.01	16001	0011 1110 1000 0001	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
160.00	16000	0011 1110 1000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
159.99	15999	0011 1110 0111 1111	0011 1110 0111 1111	0001 1111 0100 0000	0000 1111 1010 0000
159.98	15998	0011 1110 0111 1110	0011 1110 0111 1110	0001 1111 0100 0000	0000 1111 1010 0000
⋮	⋮	⋮	⋮	⋮	⋮
80.02	8002	0001 1111 0100 0010	0001 1111 0100 0010	0001 1111 0100 0000	0000 1111 1010 0000
80.01	8001	0001 1111 0100 0001	0001 1111 0100 0001	0001 1111 0100 0000	0000 1111 1010 0000
80.00	8000	0001 1111 0100 0000	0001 1111 0100 0000	0001 1111 0100 0000	0000 1111 1010 0000
79.99	7999	0001 1111 0011 1111	0001 1111 0011 1111	0001 1111 0011 1111	0000 1111 1010 0000
79.98	7998	0001 1111 0011 1110	0001 1111 0011 1110	0001 1111 0011 1110	0000 1111 1010 0000
⋮	⋮	⋮	⋮	⋮	⋮
40.02	4002	0000 1111 1010 0010	0000 1111 1010 0010	0000 1111 1010 0010	0000 1111 1010 0000
40.01	4001	0000 1111 1010 0001	0000 1111 1010 0001	0000 1111 1010 0001	0000 1111 1010 0000
40.00	4000	0000 1111 1010 0000	0000 1111 1010 0000	0000 1111 1010 0000	0000 1111 1010 0000
39.99	3999	0000 1111 1001 1111	0000 1111 1001 1111	0000 1111 1001 1111	0000 1111 1001 1111
39.98	3998	0000 1111 1001 1110	0000 1111 1001 1110	0000 1111 1001 1110	0000 1111 1001 1110
⋮	⋮	⋮	⋮	⋮	⋮
0.02	2	0000 0000 0000 0010	0000 0000 0000 0010	0000 0000 0000 0010	0000 0000 0000 0010
0.01	1	0000 0000 0000 0001	0000 0000 0000 0001	0000 0000 0000 0001	0000 0000 0000 0001
0	0	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000
–0.01	–1	1111 1111 1111 1111	1111 1111 1111 1111	1111 1111 1111 1111	1111 1111 1111 1111
–0.02	–2	1111 1111 1111 1110	1111 1111 1111 1110	1111 1111 1111 1110	1111 1111 1111 1110
⋮	⋮	⋮	⋮	⋮	⋮
–39.98	–3998	1111 0000 0110 0010	1111 0000 0110 0010	1111 0000 0110 0010	1111 0000 0110 0010
–39.99	–3999	1111 0000 0110 0001	1111 0000 0110 0001	1111 0000 0110 0001	1111 0000 0110 0001
–40.00	–4000	1111 0000 0110 0000	1111 0000 0110 0000	1111 0000 0110 0000	1111 0000 0110 0000
–40.01	–4001	1111 0000 0101 1111	1111 0000 0101 1111	1111 0000 0101 1111	1111 0000 0110 0000
–40.02	–4002	1111 0000 0101 1110	1111 0000 0101 1110	1111 0000 0101 1110	1111 0000 0110 0000
⋮	⋮	⋮	⋮	⋮	⋮
–79.98	–7998	1110 0000 1100 0010	1110 0000 1100 0010	1110 0000 1100 0010	1111 0000 0110 0000
–79.99	–7999	1110 0000 1100 0001	1110 0000 1100 0001	1110 0000 1100 0001	1111 0000 0110 0000
–80.00	–8000	1110 0000 1100 0000	1110 0000 1100 0000	1110 0000 1100 0000	1111 0000 0110 0000
–80.01	–8001	1110 0000 1011 1111	1110 0000 1011 1111	1110 0000 1100 0000	1111 0000 0110 0000
–80.02	–8002	1110 0000 1011 1110	1110 0000 1011 1110	1110 0000 1100 0000	1111 0000 0110 0000
⋮	⋮	⋮	⋮	⋮	⋮
–159.98	–15998	1100 0001 1000 0010	1100 0001 1000 0010	1110 0000 1100 0000	1111 0000 0110 0000
–159.99	–15999	1100 0001 1000 0001	1100 0001 1000 0001	1110 0000 1100 0000	1111 0000 0110 0000
–160.00	–16000	1100 0001 1000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–160.01	–16001	1100 0001 0111 1111	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–160.02	–16002	1100 0001 0111 1110	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
⋮	⋮	⋮	⋮	⋮	⋮
–319.98	–31998	1000 0011 0000 0010	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–319.99	–31999	1000 0011 0000 0001	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–320.00	–32000	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–320.01	–32001	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–320.02	–32002	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000

(1) Out-of-range values are shown in gray shading.

8.6.3.2 Bus Voltage Register (address = 02h)

The Bus Voltage register stores the most recent bus voltage reading, V_{BUS}.

At full-scale range = 32 V (decimal = 8000, hex = 1F40), and LSB = 4 mV.

Figure 24. Bus Voltage Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	CNVR	OVF

At full-scale range = 16 V (decimal = 4000, hex = 0FA0), and LSB = 4 mV.

CNVR: **Conversion Ready**

Bit 1

Although the data from the last conversion can be read at any time, the INA219 Conversion Ready bit (CNVR) indicates when data from a conversion is available in the data output registers. The CNVR bit is set after all conversions, averaging, and multiplications are complete. CNVR will clear under the following conditions:

1.) Writing a new mode into the Operating Mode bits in the Configuration Register (except for Power-Down or Disable)

2.) Reading the Power Register

OVF: **Math Overflow Flag**

Bit 0

The Math Overflow Flag (OVF) is set when the Power or Current calculations are out of range. It indicates that current and power data may be meaningless.

8.6.3.3 Power Register (address = 03h) [reset = 00h]

Full-scale range and LSB are set by the Calibration register. See the *Programming the Calibration Register*.

Figure 25. Power Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The Power register records power in watts by multiplying the values of the current with the value of the bus voltage according to the equation Equation 5:

8.6.3.4 Current Register (address = 04h) [reset = 00h]

Full-scale range and LSB depend on the value entered in the Calibration register. See *Programming the Calibration Register* for more information. Negative values are stored in 2's complement format.

Figure 26. Current Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSIGN	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The value of the Current register is calculated by multiplying the value in the Shunt Voltage register with the value in the Calibration register according to the Equation 4:

8.6.4 Calibration Register

8.6.4.1 Calibration Register (address = 05h) [reset = 00h]

Current and power calibration are set by bits FS15 to FS1 of the Calibration register. Note that bit FS0 is not used in the calculation. This register sets the current that corresponds to a full-scale drop across the shunt. Full-scale range and the LSB of the current and power measurement depend on the value entered in this register. See the *Programming the Calibration Register*. This register is suitable for use in overall system calibration. Note that the 0 POR values are all default.

Figure 27. Calibration Register(1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FS15	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) FS0 is a *void* bit and will always be 0. It is not possible to write a 1 to FS0. CALIBRATION is the value stored in FS15:FS1.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The INA219 is a current shunt and power monitor with an I²C- and SMBus-compatible interface. The device monitors both a shunt voltage drop and bus supply voltage. Programmable calibration value, combined with an internal multiplier, enable readouts of current and power.

9.2 Typical Application

Figure 28 shows a typical application circuit for the INA219. Use a 0.1-µF ceramic capacitor for power-supply bypassing, placed as closely as possible to the supply and ground pins.

The input filter circuit consisting of R_{F1}, R_{F2}, and C_F is not necessary in most applications. If the need for filtering is unknown, reserve board space for the components and install 0-Ω resistors for R_{F1} and R_{F2} and leave C_F unpopulated, unless a filter is needed (see *Filtering and Input Considerations*).

The pull-up resistors shown on the SDA and SCL lines are not needed if there are pullup resistors on these same lines elsewhere in the system. Resistor values shown are typical: consult either the I²C or SMBus specification to determine the acceptable minimum or maximum values and also refer to the *Specifications* for Output Current Limitations.

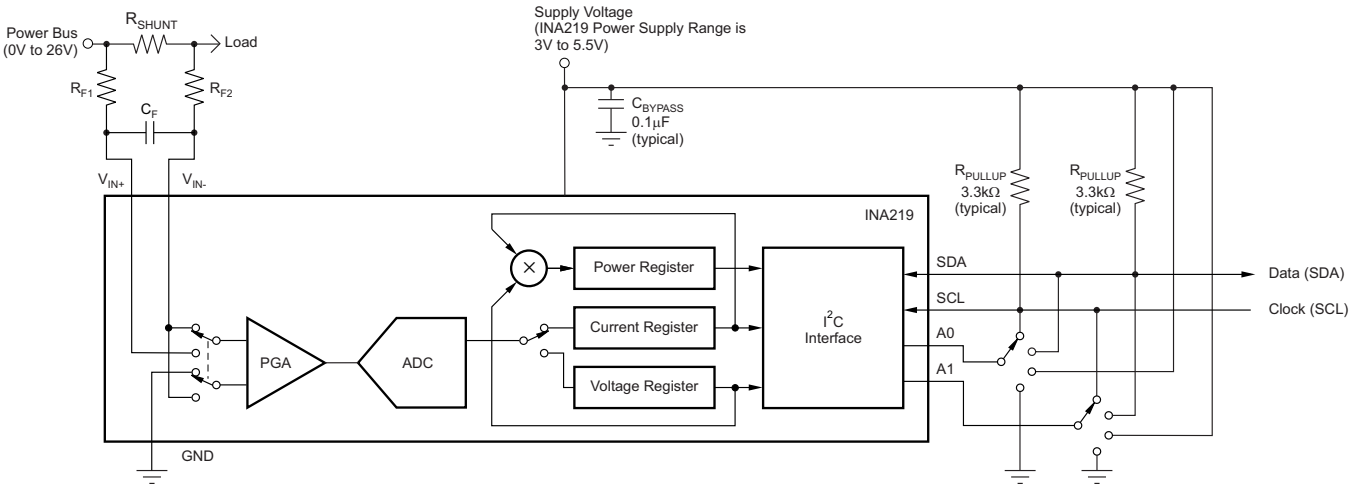


Figure 28. Typical Application Circuit

9.2.1 Design Requirements

The INA219 measures the voltage across a current-sensing resistor (R_{SHUNT}) when current passes through the resistor. The device also measures the bus supply voltage, and calculates power when calibrated. This section goes through the steps to program the device for power measurements, and shows the register results Table 8.

The Conditions for the example circuit is: Maximum expected load current = 15 A, Nominal load current = 10 A, V_{CM} = 12 V, R_{SHUNT} = 2 mΩ, V_{SHUNT} FSR = 40 mV (PGA = /1), and BRNG = 0 (VBUS range = 16 V).

9.2.2 Detailed Design Procedure

Figure 29 shows a nominal 10-A load that creates a differential voltage of 20 mV across a 2-mΩ shunt resistor. The common mode is at 12 volts and the voltage present at the IN– pin is equal to the common-mode voltage minus the differential drop across the resistor.

Typical Application (continued)

For this example, the minimum-current LSB is calculated to be 457.78 µA/bit, assuming a maximum expected current of 15 A using Equation 2. This value is rounded up to 1 mA/bit and is chosen for the current LSB. Setting the current LSB to this value allows for sufficient precision while serving to simplify the math as well. Using Equation 1 results in a calibration value of 20480 (5000h). This value is then programmed into the Calibration register.

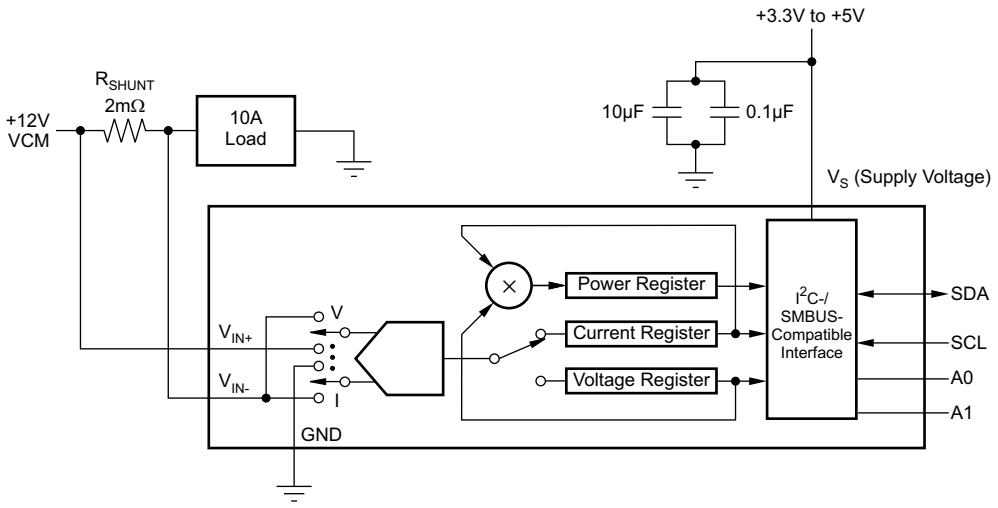


Figure 29. Example Circuit Configuration

The bus voltage is internally measured at the IN– pin to calculate the voltage level delivered to the load. The Bus Voltage register bits are not right-aligned; therefore, they must be shifted right by three bits. Multiply the shifted contents by the 4-mV LSB to compute the bus voltage measured by the device in volts. The shifted value of the Bus Voltage register contents is equal to BB3h, the decimal equivalent of 2995. This value of 2995 is multiplied by the 4-mV LSB, and results in a value of 11.98 V. As shown, the voltage at the IN– pin is 11.98 V. For a 40-mV, full-scale range, this small difference is not a significant deviation from the 12-V common-mode voltage. However, at larger full-scale ranges, this deviation can be much larger.

The Current register content is internally calculated using Equation 4, and the result of 10000 (2710h) is automatically loaded into the register. Current in amperes is equal to 1 mA/bit times 10000, and results in a 10-A load current.

The Power register content is internally calculated using Equation 5 and the result of 5990 (1766h) is automatically loaded into the register. Multiplying this result by the Power register LSB 20 × 10^{-3}(20 times 1 × 10^{-3} current LSB using Equation 3), results in a power calculation of 5990 × 20 mW/bit, and equals 119.8 W. This result matches what is expected for this register. A calculation for the power delivered to the load uses 11.98 V (12 VCM – 20-mV shunt drop) multiplied by the load current of 10 A to give a 119.8-W result.

9.2.2.1 Register Results for the Example Circuit

Table 8 shows the register readings for the Calibration example.

Table 8. Register Results (1)

REGISTER NAME	ADDRESS	CONTENTS	ADJ	DEC	LSB	VALUE
Configuration	00h	019Fh				
Shunt	01h	07D0h		2000	10 µV	20 mV
Bus	02h	5D98h	0BB3	2995	4 mV	11.98 V
Calibration	05h	5000h		20480		
Current	04h	2710h		10000	1 mA	10.0 A
Power	03h	1766h		5990	20 mW	119.8 W

(1) Conditions: load = 10 A, V_{CM} = 12 V, R_{SHUNT} = 2 mΩ, V_{SHUNT} FSR = 40 mV, and V_{BUS} = V_{IN-}, BRNG = 0 (VBUS range = 16 V).

10 Power Supply Recommendations

The input circuitry of the device can accurately measure signals on common-mode voltages beyond its power supply voltage, V_S. For example, the voltage applied to the V_S power supply terminal can be 5 V, whereas the load power-supply voltage being monitored (the common-mode voltage) can be as high as 26 V. Note also that the device can withstand the full 0-V to 26-V range at the input terminals, regardless of whether the device has power applied or not.

Place the required power-supply bypass capacitors as close as possible to the supply and ground terminals of the device to ensure stability. A typical value for this supply bypass capacitor is 0.1 μF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

11 Layout

11.1 Layout Guidelines

Connect the input pins (IN+ and IN–) to the sensing resistor using a Kelvin connection or a 4-wire connection. These connection techniques ensure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current-sensing resistor, any additional high-current carrying impedance causes significant measurement errors. Place the power-supply bypass capacitor as close as possible to the supply and ground pins.

11.2 Layout Example

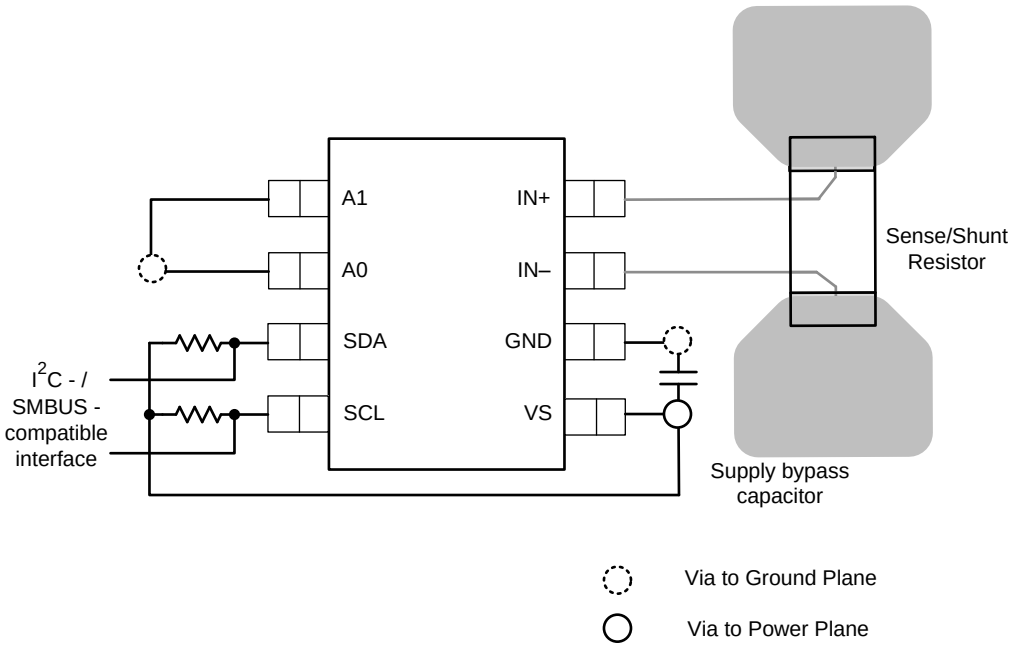


Figure 30. Recommended Layout

12 デバイスおよびドキュメントのサポート

12.1 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.2 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.4 用語集

SLYZ022 — *TI用語集*.

この用語集には、用語や略語の一覧および定義が記載されています。

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA219AID	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I219A
INA219AIDCNR	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A219
INA219AIDCNR.A	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A219
INA219AIDCNR.B	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A219
INA219AIDCNR1G4	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A219
INA219AIDCNR1G4.A	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A219
INA219AIDCNR1G4.B	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A219
INA219AIDCNT	Active	Production	SOT-23 (DCN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A219
INA219AIDCNT.A	Active	Production	SOT-23 (DCN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A219
INA219AIDCNT.B	Active	Production	SOT-23 (DCN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A219
INA219AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I219A
INA219AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I219A
INA219AIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I219A
INA219AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I219A
INA219AIDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I219A
INA219AIDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I219A
INA219BID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	I219B
INA219BIDCNR	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B219
INA219BIDCNR.A	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B219
INA219BIDCNR.B	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B219
INA219BIDCNRG4	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B219
INA219BIDCNRG4.A	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B219
INA219BIDCNRG4.B	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B219
INA219BIDCNT	Active	Production	SOT-23 (DCN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B219
INA219BIDCNT.A	Active	Production	SOT-23 (DCN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B219
INA219BIDCNT.B	Active	Production	SOT-23 (DCN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B219
INA219BIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I219B
INA219BIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I219B

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA219BIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I219B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

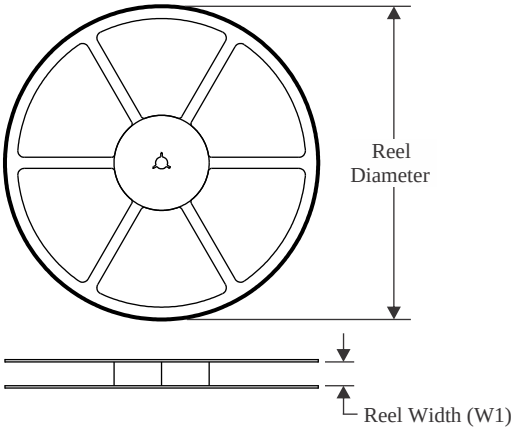
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

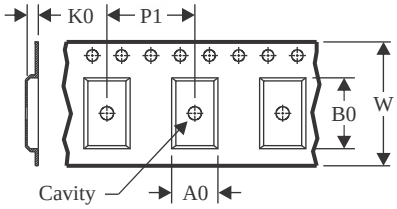
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

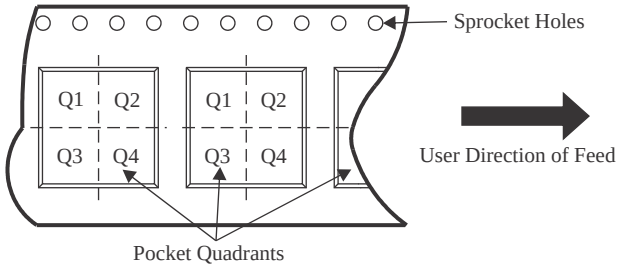


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

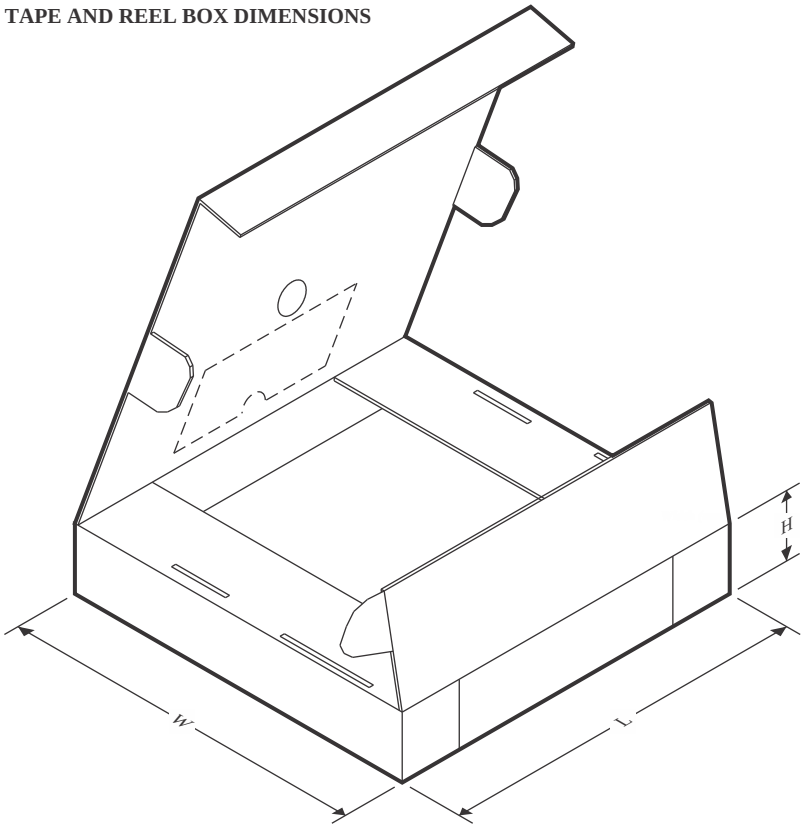
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA219AIDCNR	SOT-23	DCN	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA219AIDCNR	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA219AIDCNR1G4	SOT-23	DCN	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA219AIDCNT	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA219AIDCNT	SOT-23	DCN	8	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA219AIDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
INA219AIDRG4	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
INA219BIDCNR	SOT-23	DCN	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA219BIDCNR	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA219BIDCNRG4	SOT-23	DCN	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA219BIDCNT	SOT-23	DCN	8	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA219BIDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

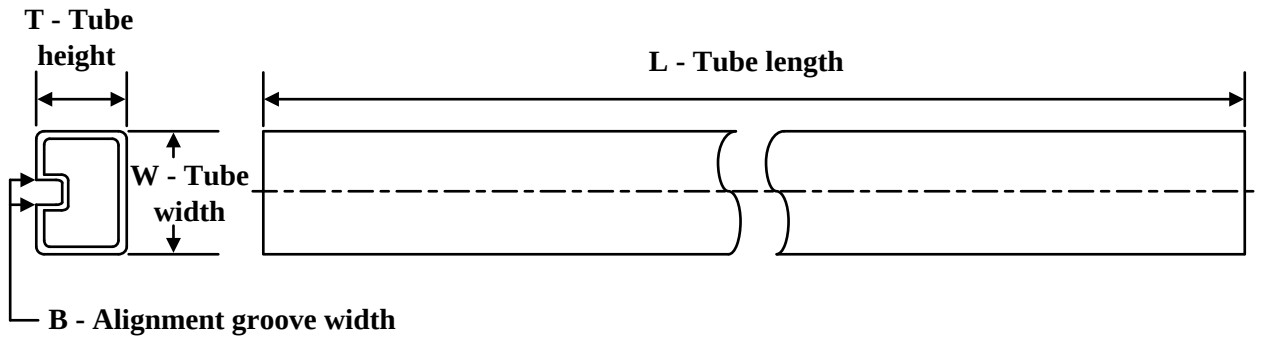
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

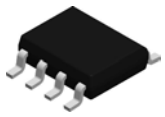
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA219AIDCNR	SOT-23	DCN	8	3000	210.0	185.0	35.0
INA219AIDCNR	SOT-23	DCN	8	3000	213.0	191.0	35.0
INA219AIDCNR1G4	SOT-23	DCN	8	3000	210.0	185.0	35.0
INA219AIDCNT	SOT-23	DCN	8	250	213.0	191.0	35.0
INA219AIDCNT	SOT-23	DCN	8	250	210.0	185.0	35.0
INA219AIDR	SOIC	D	8	2500	353.0	353.0	32.0
INA219AIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
INA219BIDCNR	SOT-23	DCN	8	3000	210.0	185.0	35.0
INA219BIDCNR	SOT-23	DCN	8	3000	213.0	191.0	35.0
INA219BIDCNRG4	SOT-23	DCN	8	3000	210.0	185.0	35.0
INA219BIDCNT	SOT-23	DCN	8	250	210.0	185.0	35.0
INA219BIDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA219AID	D	SOIC	8	75	507	8	3940	4.32

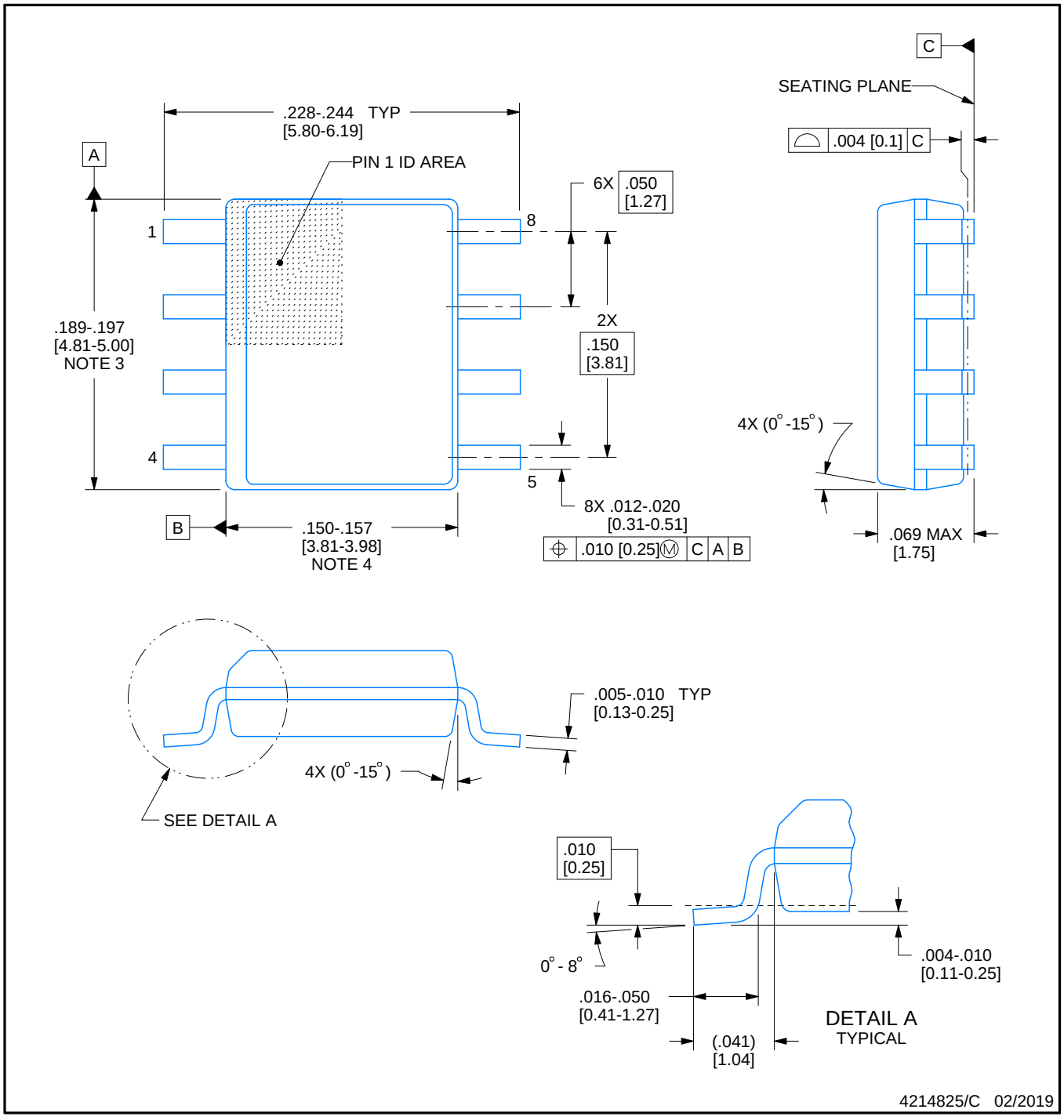


PACKAGE OUTLINE

D0008A

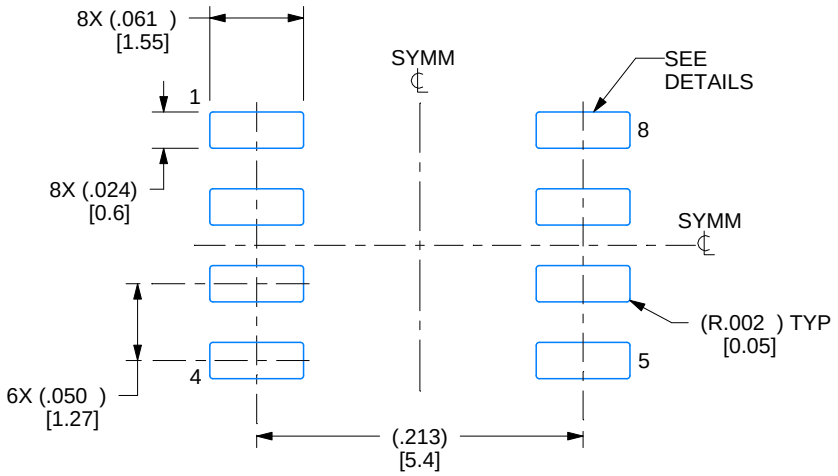
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

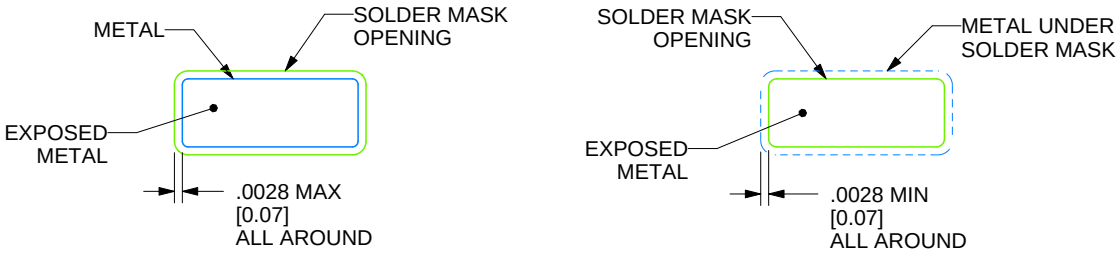


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

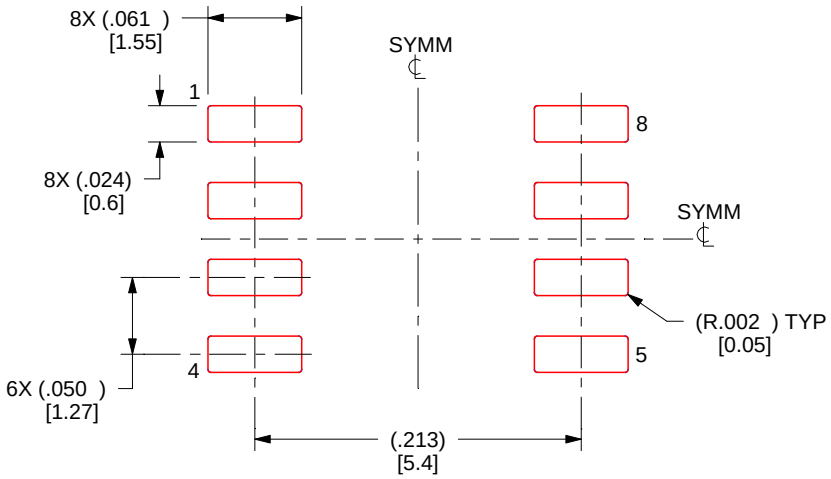
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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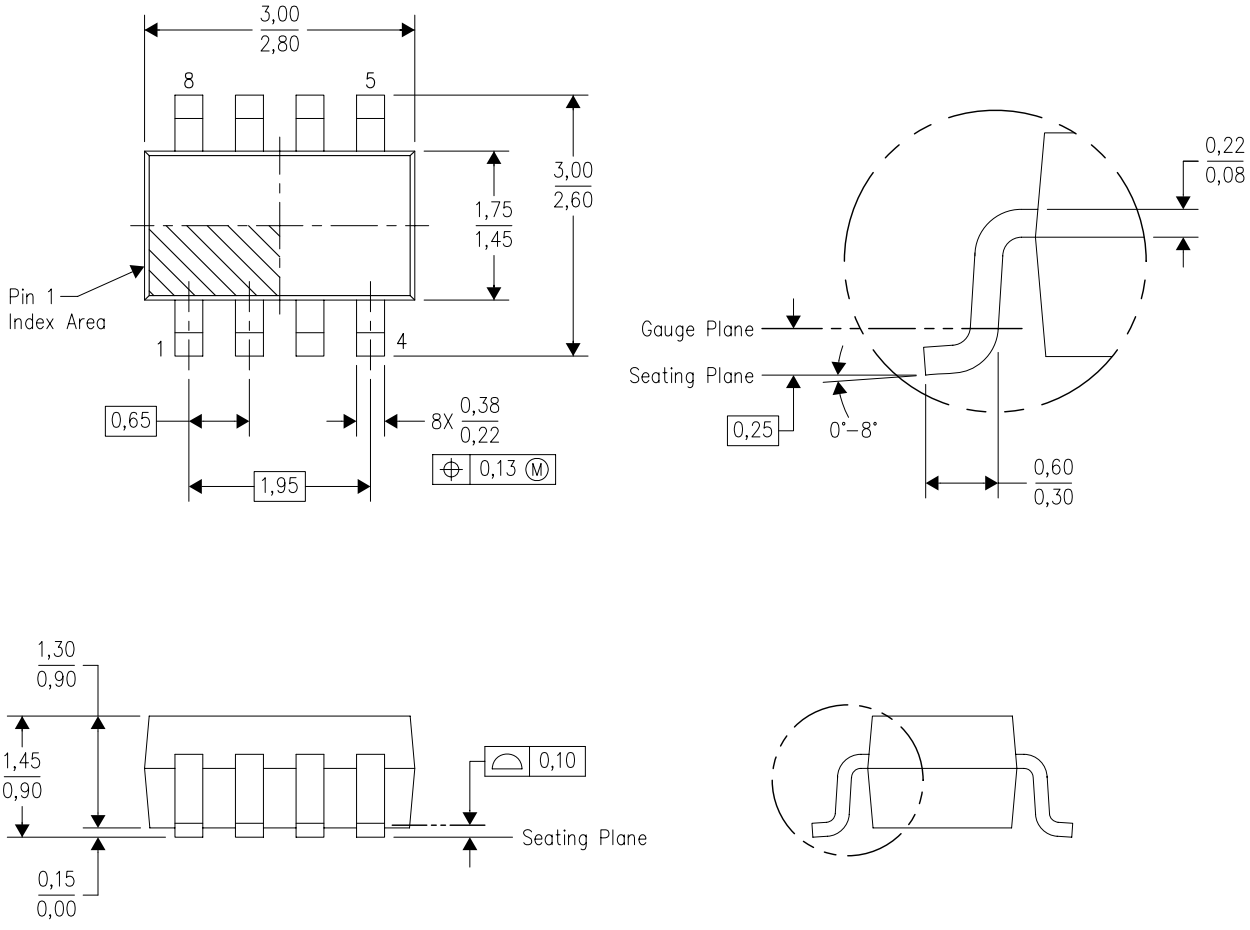
NOTES: (continued)

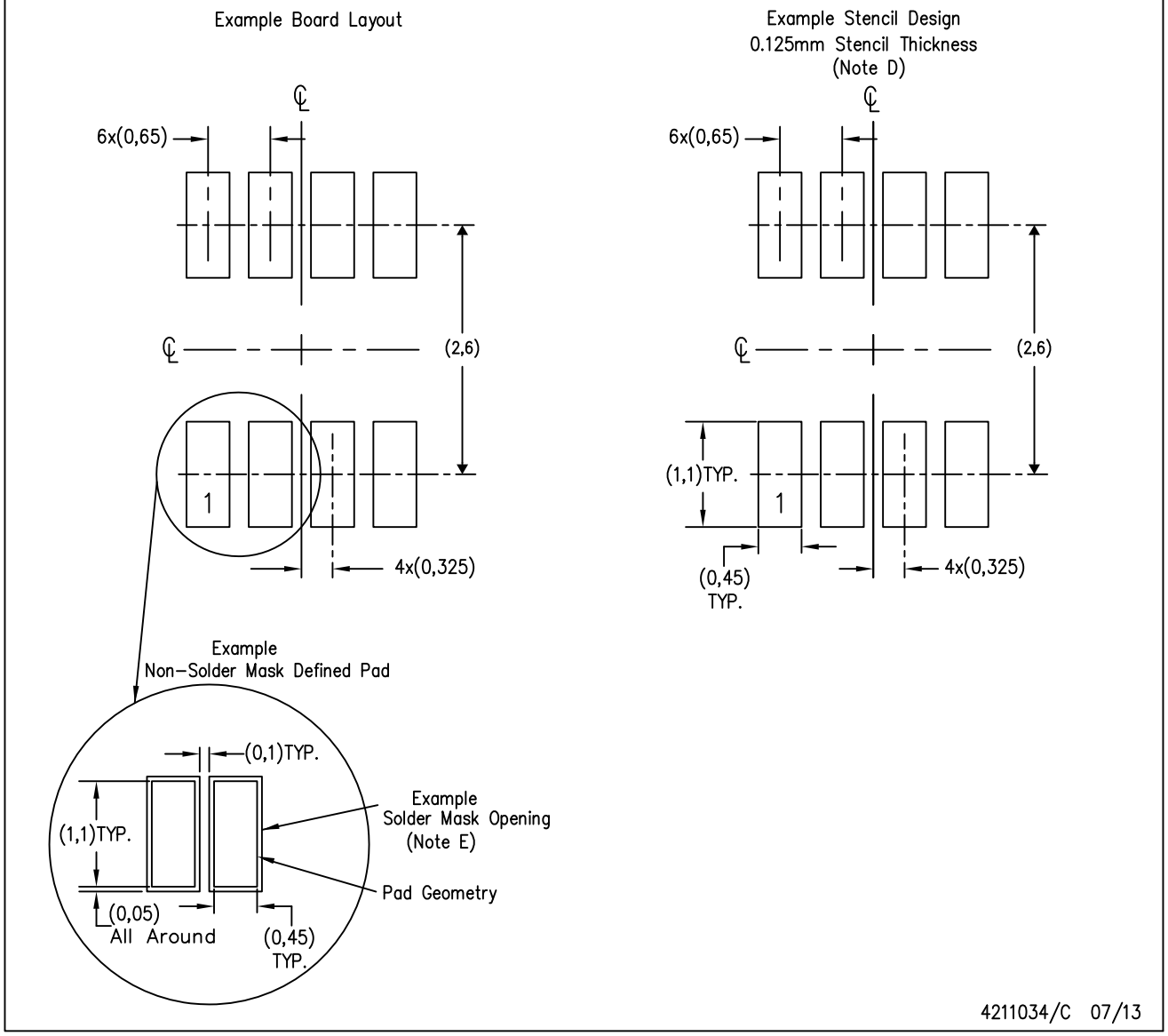
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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最終更新日：2025 年 10 月