



INA165x-Q1 SoundPlus™ 高同相除去比ライン・レシーバ

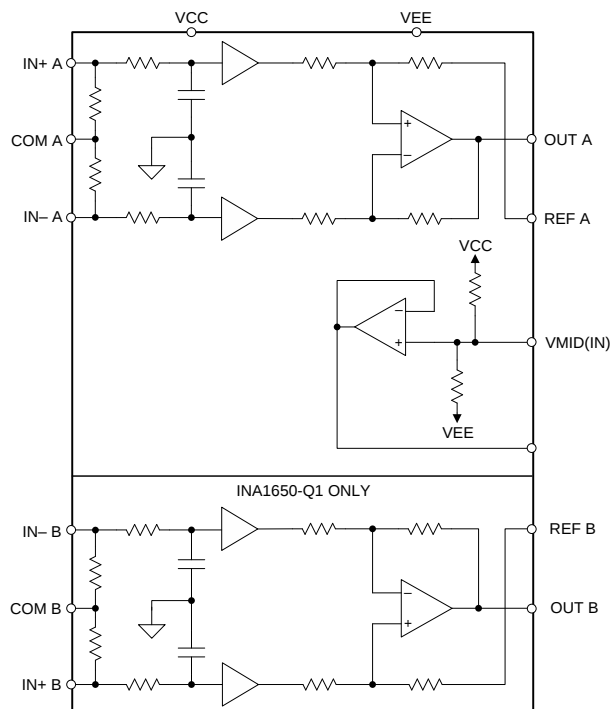
1 特長

- 車載アプリケーション用に AEC-Q100 認定済み
 - 温度グレード 1: $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$, T_A
- 高い同相除去: 91dB (標準値)
- 高い入力インピーダンス: $1\text{M}\Omega$ 差動
- 非常に低いノイズ: -104.7dBu 、重み付けなし
- 非常に低い全高調波歪 + ノイズ:
 - -119dB THD+N (20dBu , 22kHz 帯域幅)
- 短絡保護
- EMI フィルタを内蔵
- 広い電源電圧範囲: $\pm 2.25\text{V} \sim \pm 12\text{V}$
- 小型の 14 ピン TSSOP パッケージで供給

2 アプリケーション

- 車内用マイクロフォンのプリアンプ
- インフォテインメント・システム
- オーディオ入力回路
- ライン・ドライバ
- 外部オーディオ・パワー・アンプ

簡略化された内部回路図



3 概要

INA1650-Q1 デュアル・チャンネルおよび INA1651-Q1 シングル・チャンネル (INA165x-Q1) SoundPlus™ オーディオ・ライン・レシーバは、 20dBu の信号レベルにおいて 1kHz で -119dB という非常に低い THD+N を維持しながら、 91dB という非常に高い同相除去比 (CMRR) を実現します。他のライン・レシーバ製品とは異なり、INA165x-Q1 の CMRR は温度範囲全体にわたって特性が規定され、生産環境でテストされているため、広範なアプリケーションにおいて一貫した性能を発揮します。

INA165x-Q1 デバイスは、 $\pm 2.25\text{V} \sim \pm 12\text{V}$ の非常に広い電源電圧範囲で動作します。ライン・レシーバ・チャンネルに加えて、バッファ付きの中間電源基準出力を内蔵しているため、INA165x-Q1 をデュアル電源とシングル電源のどちらのアプリケーション用にも構成できます。中間電源出力は、信号チェーン内のその他のアナログ回路のバイアス電圧として使用できます。

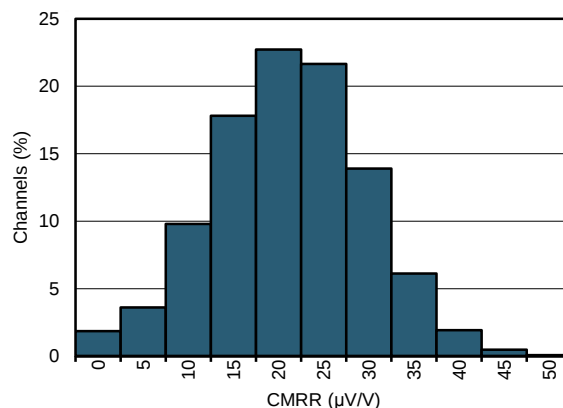
INA1650-Q1 は独自の内部レイアウトにより、最小のクロストークを実現しており、オーバードライブや過負荷時にもチャンネル間の相互干渉がありません。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ (公称)
INA1650-Q1	TSSOP (14)	5.00mm×4.40mm
INA1651-Q1		

(1) 提供されているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。

CMRR ヒストグラム (5746 チャンネル)



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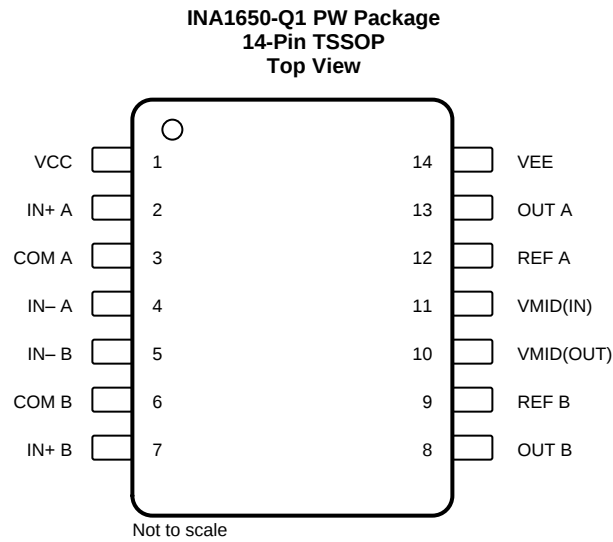
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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

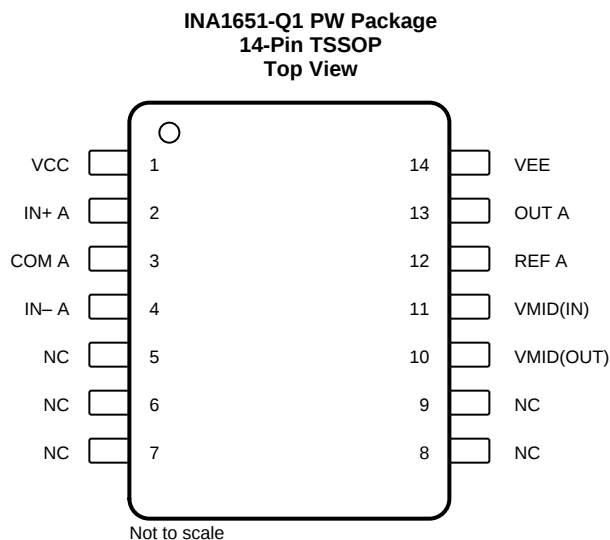
Revision B (April 2019) から Revision C に変更	Page
• Changed <i>ESD Ratings</i> table to show individual device ratings	5
Revision A (October 2017) から Revision B に変更	Page
• INA1651-Q1 デバイスと関連コンテンツをデータシートに 追加	1
2017年8月発行のものから更新	Page
• INA1650-Q1 の推奨電源電圧範囲を 36V から 24V に引き下げ。テキスト、グラフ、回路図で 36V 動作に言及している部分をすべて削除、または最大 24V 電源を反映するように変更	1

5 Pin Configuration and Functions



Pin Functions: INA1650-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
COM A	3	I	Input common, channel A
COM B	6	I	Input common, channel B
IN+ A	2	I	Noninverting input, channel A
IN- A	4	I	Inverting input, channel A
IN+ B	7	I	Noninverting input, channel B
IN- B	5	I	Inverting input, channel B
OUT A	13	O	Output, channel A
OUT B	8	O	Output, channel B
REF A	12	I	Reference input, channel A. This pin must be driven from a low impedance.
REF B	9	I	Reference input, channel B. This pin must be driven from a low impedance.
VCC	1	—	Positive (highest) power supply
VEE	14	—	Negative (lowest) power supply
VMID(IN)	11	I	Input node of internal supply divider. Connect a capacitor to this pin to reduce noise from the supply divider circuit.
VMID(OUT)	10	O	Buffered output of internal supply divider.


Pin Functions: INA1651-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
COM A	3	I	Input common, channel A
IN+ A	2	I	Noninverting input, channel A
IN- A	4	I	Inverting input, channel A
NC	5	—	No internal connection
NC	6	—	No internal connection
NC	7	—	No internal connection
NC	8	—	No internal connection
NC	9	—	No internal connection
OUT A	13	O	Output, channel A
REF A	12	I	Reference input, channel A. This pin must be driven from a low impedance.
VCC	1	—	Positive (highest) power supply
VEE	14	—	Negative (lowest) power supply
VMID(IN)	11	I	Input node of internal supply divider. Connect a capacitor to this pin to reduce noise from the supply divider circuit.
VMID(OUT)	10	O	Buffered output of internal supply divider.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply voltage, $V_S = (V+) - (V-)$		40	V
	Input voltage (signal inputs, enable, ground)	$(V-) - 0.5$	$(V+) + 0.5$	
	Input differential voltage		$(V+) - (V-)$	
Current	Input current (all pins except power-supply pins)		±10	mA
	Output short-circuit ⁽²⁾	Continuous		
Temperature	Operating, T_A	–55	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to $V_S / 2$ (ground in symmetrical dual supply setups), one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
INA1650-Q1				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 3A	±4000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1000	
INA1651-Q1				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 2	±2500	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4A	±500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage ($V+ - V-$)	4.5 (±2.25)		24 (±12)	V
Specified temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		INA1650-Q1	INA1651-Q1	UNIT
		PW (TSSOP)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.0	99.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.6	29.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.4	42.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.9	1.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.6	42.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Electrical Characteristics:

at $T_A = 25^\circ\text{C}$, $V_S = \pm 2.25\text{ V}$ to $\pm 12\text{ V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE						
THD+N	Total harmonic distortion + noise	$V_O = 3\text{ V}_{\text{RMS}}$, $f = 1\text{ kHz}$, 90-kHz measurement bandwidth, $V_S = \pm 12\text{ V}$	0.00039%			
			−108.1		dB	
		$V_{\text{IN}} = 20\text{ dBu}$ (7.746 V_{RMS}) , $F_{\text{IN}} = 1\text{ kHz}$, $V_S = \pm 12\text{ V}$, 90-kHz measurement bandwidth	0.000224%			
			−113.0		dB	
IMD	Intermodulation distortion	SMPTE and DIN two-tone, 4:1 (60 Hz and 7 kHz) $V_O = 3\text{ V}_{\text{RMS}}$, 90-kHz measurement bandwidth	0.0005%			
			−106.1		dB	
		CCIF twin-tone (19 kHz and 20 kHz), $V_O = 3\text{ V}_{\text{RMS}}$, 90-kHz measurement bandwidth	0.00066%			
			−103.6		dB	
AC PERFORMANCE						
BW	Small-signal bandwidth		2.7			MHz
SR	Slew rate		10			V/μs
	Full-power bandwidth ⁽¹⁾	$V_O = 1\text{ V}_P$	1.59			MHz
PM	Phase margin	$C_L = 20\text{ pF}$	71			degrees
		$C_L = 200\text{ pF}$	54			degrees
t _s	Settling time	To 0.01%, $V_S = \pm 12\text{ V}$, 10-V step	2.2			μs
	Overload recovery time		330			ns
	Channel separation	$f = 1\text{ kHz}$, REF and COM pins connected to ground	140			dB
		$f = 1\text{ kHz}$, REF and COM pins connected to VMID(OUT)	130			dB
	EMI/RFI filter corner frequency		80			MHz
NOISE						
e _n	Output voltage noise	$f = 20\text{ Hz}$ to 20 kHz, no weighting	4.5			μV _{RMS}
			−104.7			dBu
	Output voltage noise density ⁽²⁾	$f = 100\text{ Hz}$	47			$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$	31			
OFFSET VOLTAGE						
V _{OS}	Output offset voltage		±1	±3		mV
		T _A = −40°C to 125°C ⁽²⁾		±4		
dV _{OS} /dT	Output offset voltage drift ⁽²⁾	T _A = −40°C to 125°C	2	7		μV/°C
PSRR	Power-supply rejection ratio		2			μV/V
GAIN						
	Gain		1			V/V
	Gain error		0.04%	0.05%		
		T _A = −40°C to 125°C ⁽²⁾	0.05%	0.06%		
	Gain nonlinearity	$V_S = \pm 12\text{ V}$, −10 V < V _O < 10 V ⁽²⁾	1	5		ppm
INPUT VOLTAGE						
V _{CM}	Common-mode voltage		(V−) + 0.25	(V+) − 2		V
CMRR	Common-mode rejection ratio	(V−) + 0.25 V ≤ V _{CM} ≤ (V+) − 2 V, REF and COM pins connected to ground, V _S = ±12 V	85	91		dB
		T _A = −40°C to 125°C ⁽²⁾	82	89		
		(V−) + 0.25 V ≤ V _{CM} ≤ (V+) − 2 V, REF and COM pins connected to VMID(OUT), V _S = ±12 V	82	86		
		T _A = −40°C to 125°C ⁽²⁾	76	84		
CMRR	Common-mode rejection ratio	(V−) + 0.25 V ≤ V _{CM} ≤ (V+) − 2 V, REF and COM pins connected to ground, V _S = ±12 V, R _s mismatch = 20 Ω	84			dB

(1) Full-power bandwidth = $SR / (2\pi \times V_P)$, where SR = slew rate.

(2) Specified by design and characterization.

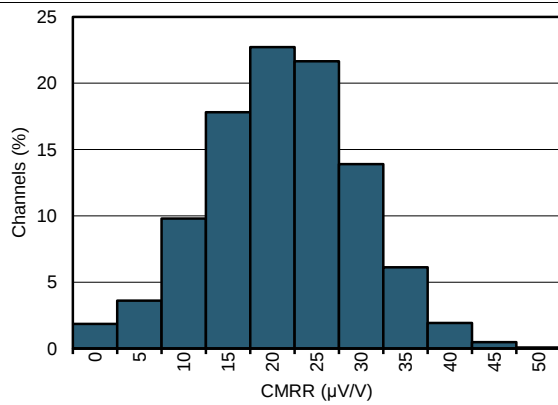
Electrical Characteristics: (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 2.25\text{ V}$ to $\pm 12\text{ V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT IMPEDANCE							
	Differential			850	1000	1150	kΩ
	Common-mode			212.5	250	287.5	kΩ
	Input resistance mismatch				0.01%	0.25%	
SUPPLY DIVIDER CIRCUIT							
	Nominal output voltage			[(V+) + (V–)] / 2			V
	Output voltage offset	VMID(IN) = ((V+) + (V–) / 2			2	4	mV
	Input impedance	VMID(IN) pin, f = 1 kHz			250		kΩ
	Output resistance	VMID(OUT) pin			0.35		Ω
	Output voltage noise	20 Hz to 20 kHz, C _{MID} = 1 μF			1.56		μV _{RMS}
	Output capacitive load limit	Phase Margin > 45°, R _{ISO} = 0 Ω			150		pF
OUTPUT							
V _O	Voltage output swing from rail	Positive rail	R _L = 2 kΩ		350		mV
			R _L = 600 Ω		1100		
		Negative rail	R _L = 2 kΩ		430		
			R _L = 600 Ω		1300		
Z _{OUT}	Output impedance	f ≤ 100 kHz, I _{OUT} = 0 A			< 1		Ω
I _{SC}	Short-circuit current	V _S = ±12 V			±75		mA
C _{LOAD}	Capacitive load drive				See Figure 19		pF
POWER SUPPLY							
I _Q	Quiescent current	I _{OUT} = 0 A, INA1651-Q1		4.6	6	6.9	mA
			T _A = –40°C to 125°C ⁽²⁾			8	
		I _{OUT} = 0 A, INA1650-Q1		8	10.5	12	
			T _A = –40°C to 125°C ⁽²⁾			14	

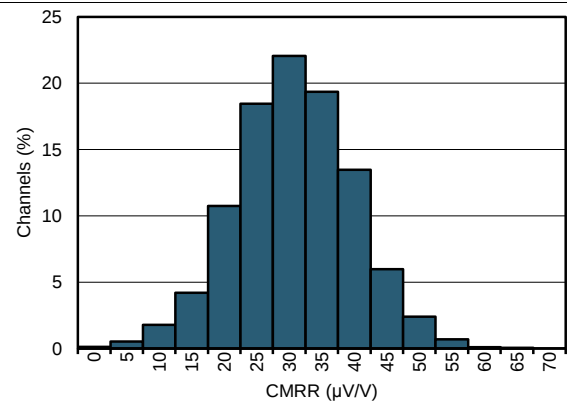
6.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 12\text{ V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)



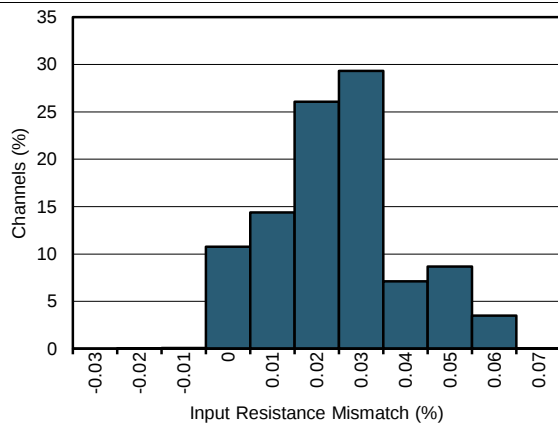
5746 channels
 V_{REF} pins connected to ground

FIG 1. Common-Mode Rejection Ratio Distribution



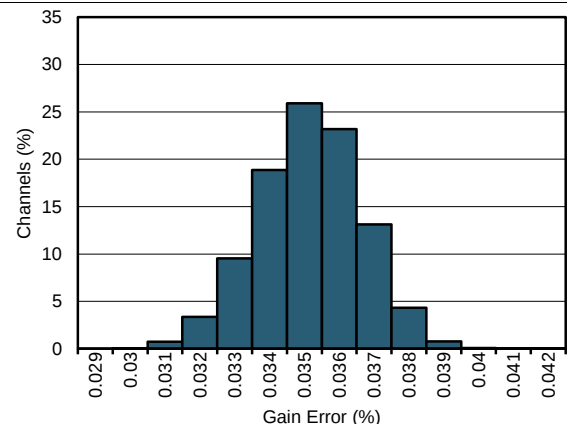
5746 channels
 V_{REF} pins connected to $V_{MID(OUT)}$

FIG 2. Common-Mode Rejection Ratio Distribution



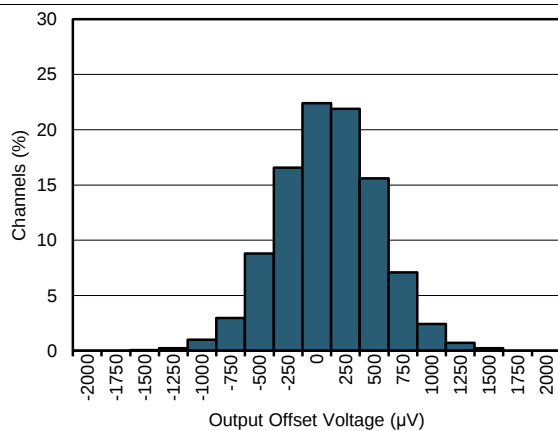
5746 channels

FIG 3. Distribution of Mismatch in 500-k Ω Input Resistors



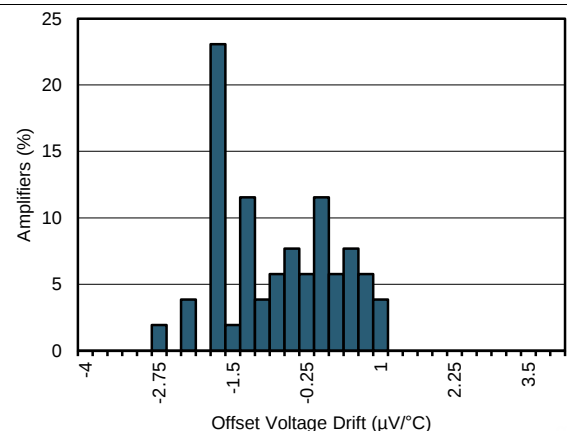
5746 channels

FIG 4. Gain Error Distribution



5746 channels

FIG 5. Offset Voltage Distribution



52 channels

FIG 6. Offset Voltage Drift Distribution

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 12\text{ V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

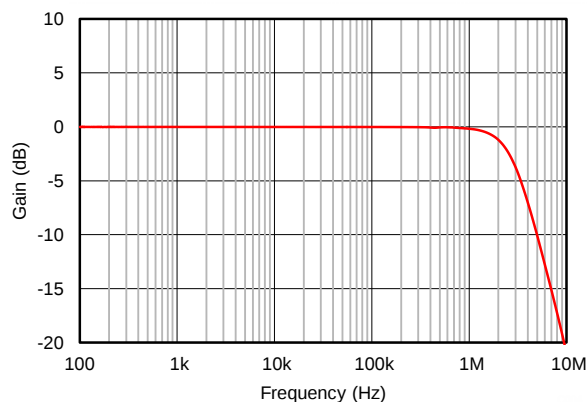


Figure 7. Frequency Response

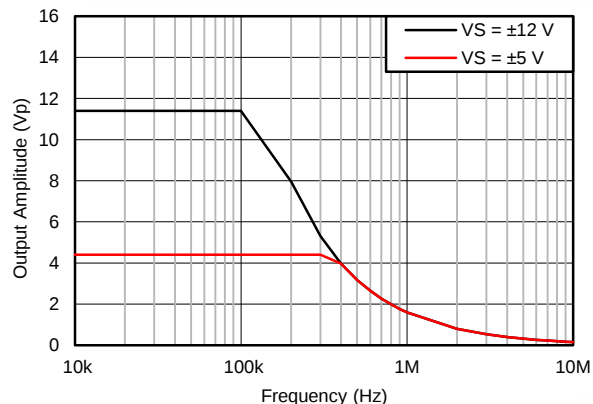


Figure 8. Maximum Output Voltage vs Frequency

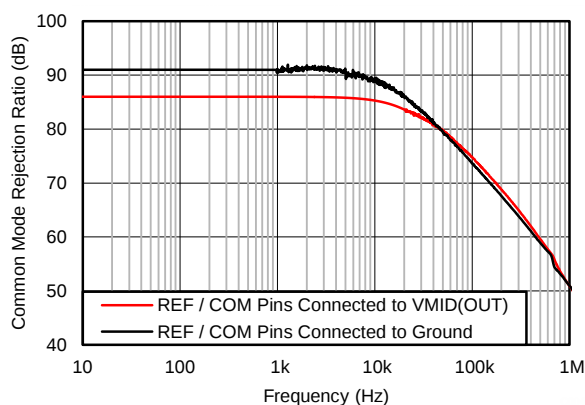


Figure 9. Common-Mode Rejection Ratio vs Frequency

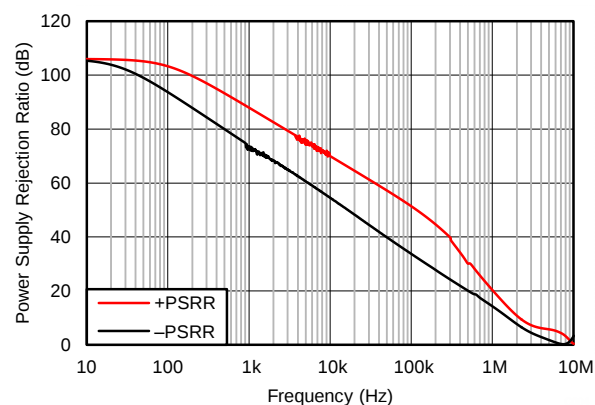


Figure 10. Power Supply Rejection Ratio vs Frequency

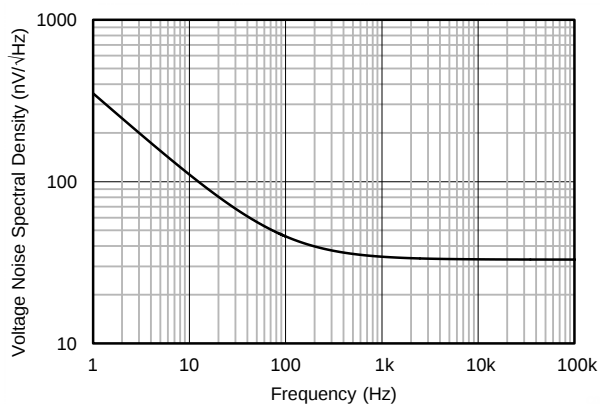


Figure 11. Voltage Noise Spectral Density

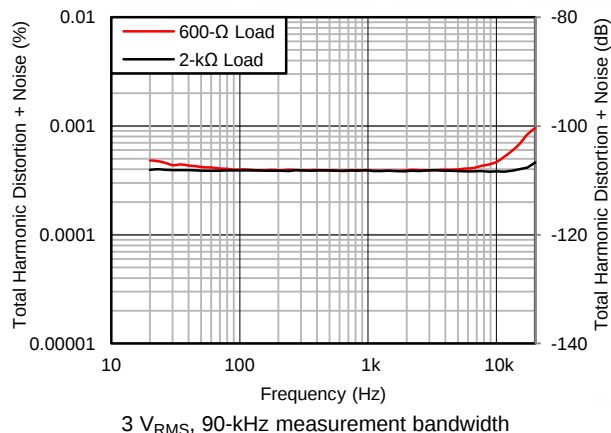


Figure 12. THD+N vs Frequency

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 12\text{ V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

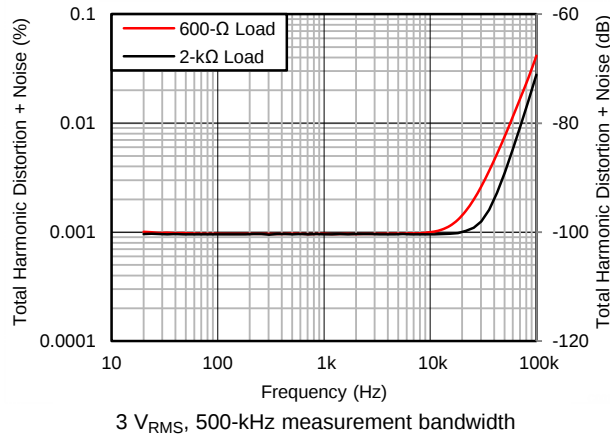


图 13. THD+N vs Frequency

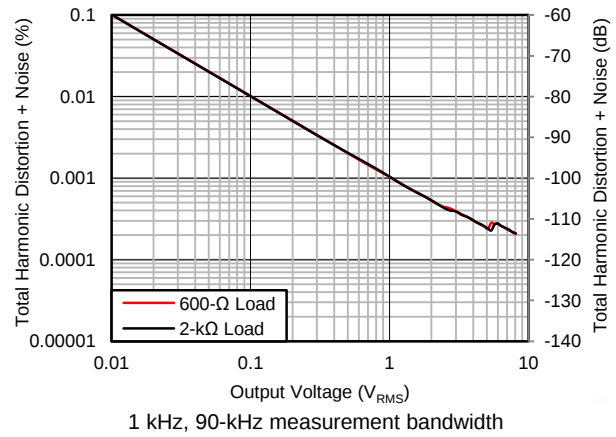


图 14. THD+N vs Output Amplitude

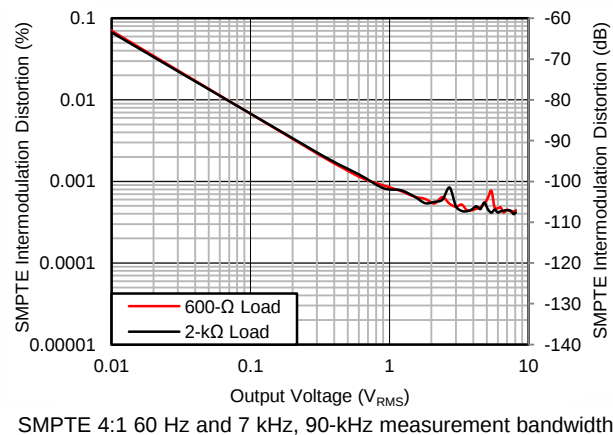


图 15. SMPTE Intermodulation Distortion vs Output Amplitude

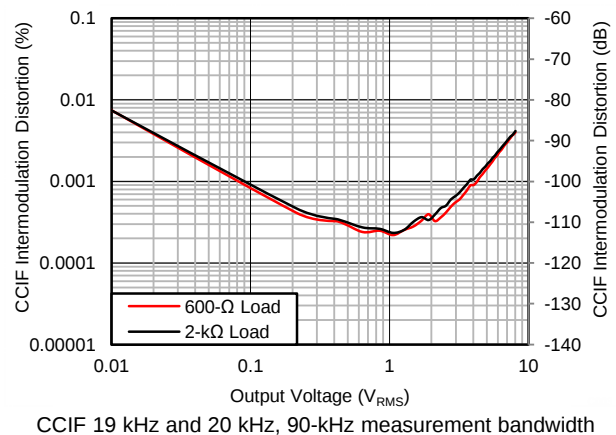


图 16. CCIF Intermodulation Distortion vs Output Amplitude

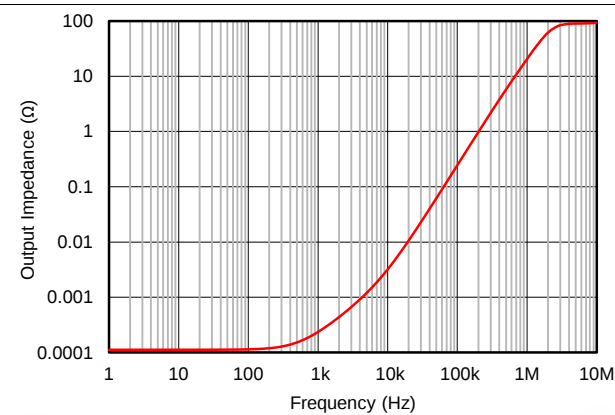


图 17. Signal Path Output Impedance vs Frequency

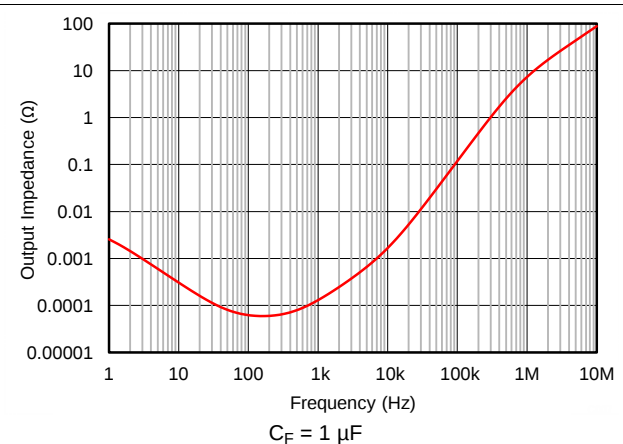


图 18. Supply Divider Output Impedance vs Frequency

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 12\text{ V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

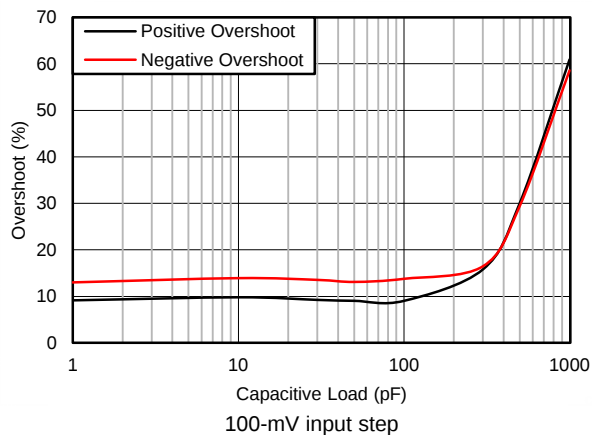


FIG 19. Overshoot vs Capacitive Load

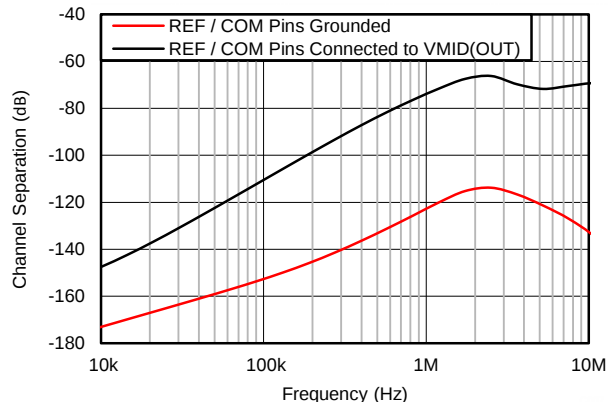
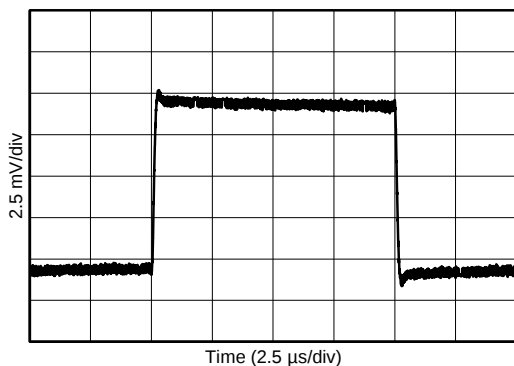
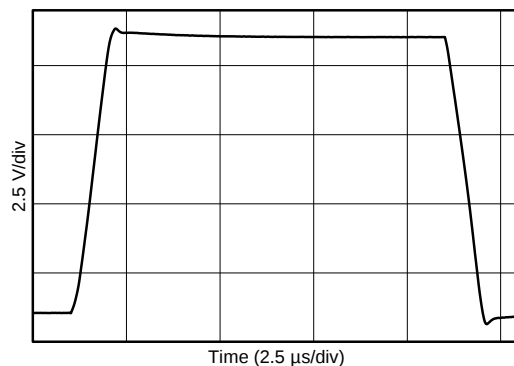


FIG 20. Channel Separation vs Frequency



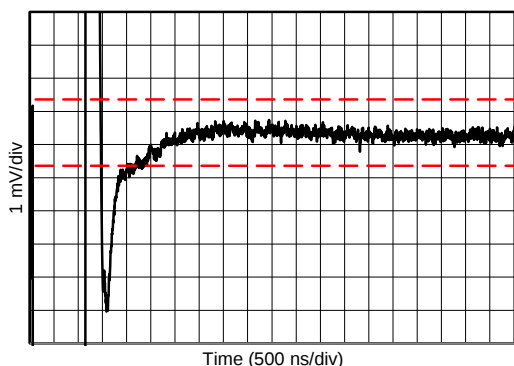
10-mV input step

FIG 21. Small-Signal Step Response



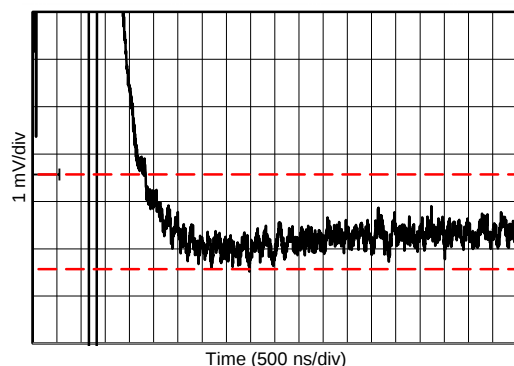
10-V input step

FIG 22. Large-Signal Step Response



10-V input step, 0.01% settling = $\pm 1\text{ mV}$

FIG 23. Rising-Edge Settling Time



10-V input step, 0.01% settling = $\pm 1\text{ mV}$

FIG 24. Falling-Edge Settling Time

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 12\text{ V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

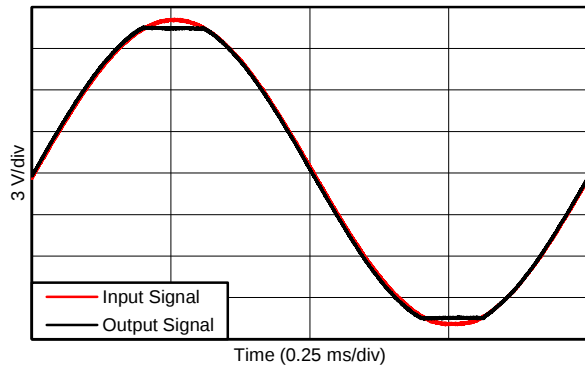


图 25. No Phase Reversal

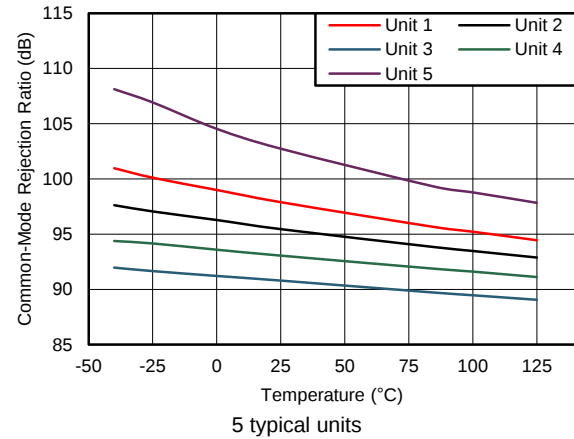


图 26. CMRR vs Temperature

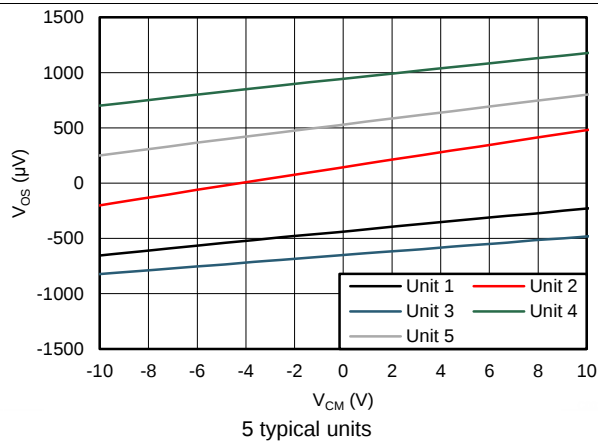


图 27. Output Offset Voltage vs Common-Mode Voltage

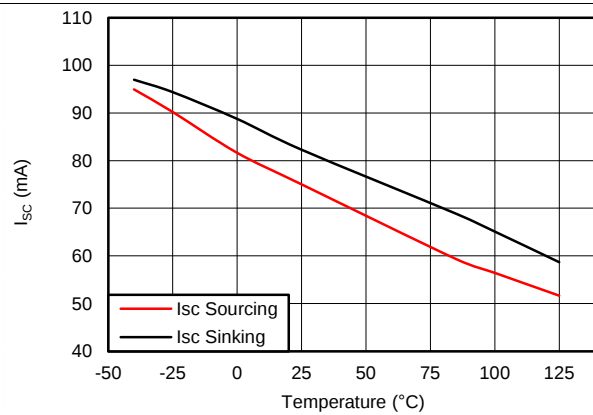


图 28. Short-Circuit Current vs Temperature

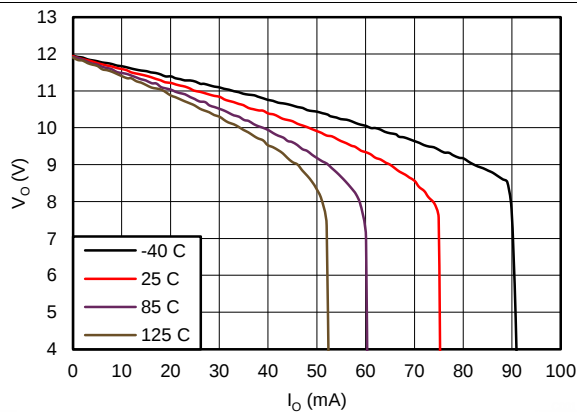


图 29. Positive Output Voltage vs Output Current

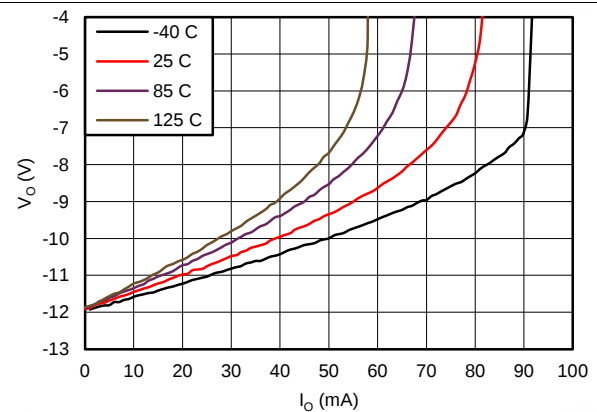


图 30. Negative Output Voltage vs Output Current

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 12\text{ V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

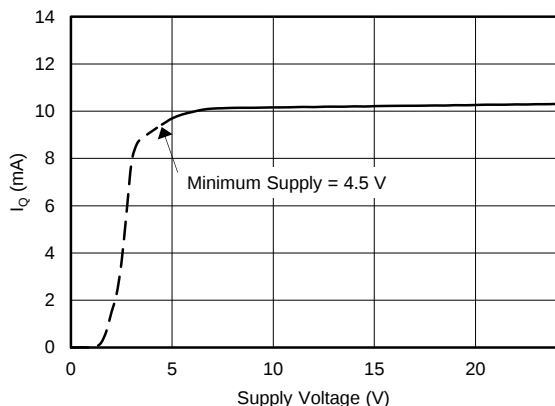


FIG 31. Quiescent Current vs Power Supply Voltage

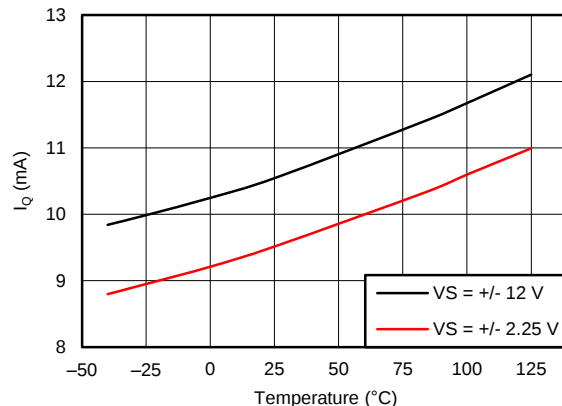


FIG 32. Quiescent Current vs Temperature

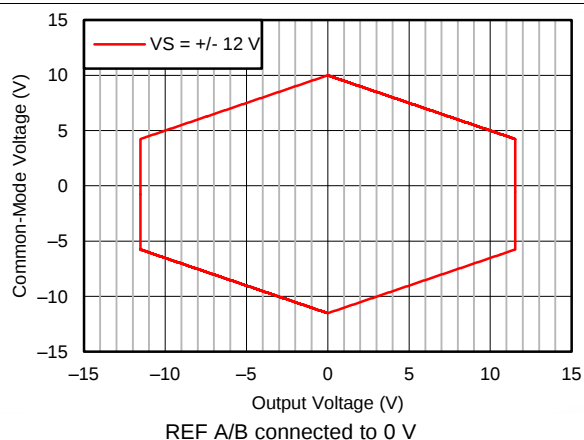


FIG 33. Input Common-Mode Voltage vs Output Voltage

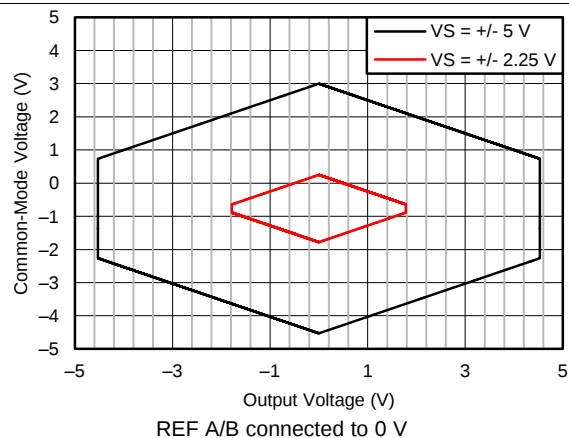


FIG 34. Input Common-Mode Voltage vs Output Voltage

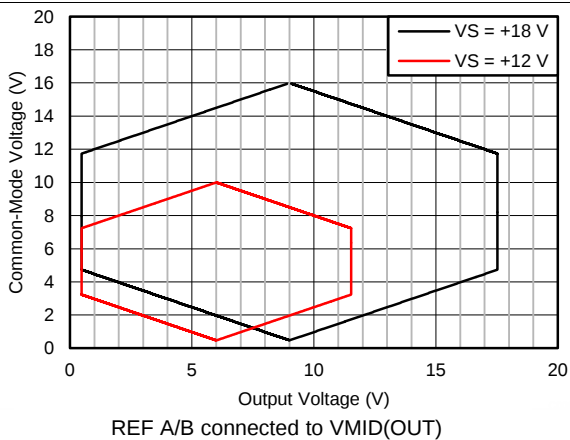


FIG 35. Input Common-Mode Voltage vs Output Voltage

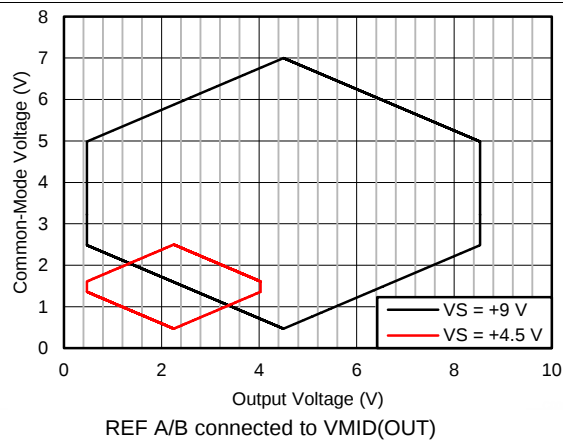


FIG 36. Input Common-Mode Voltage vs Output Voltage

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 12\text{ V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

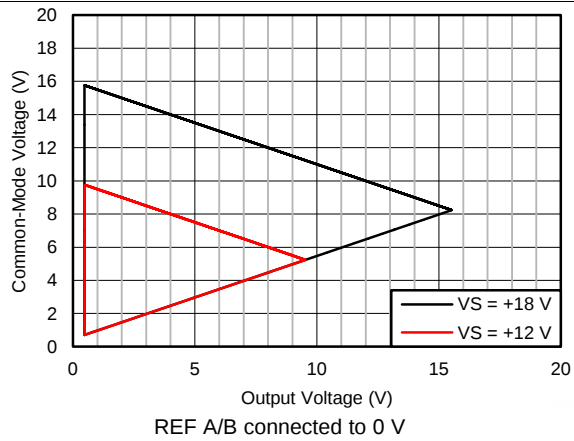


FIG 37. Input Common-Mode Voltage vs Output Voltage

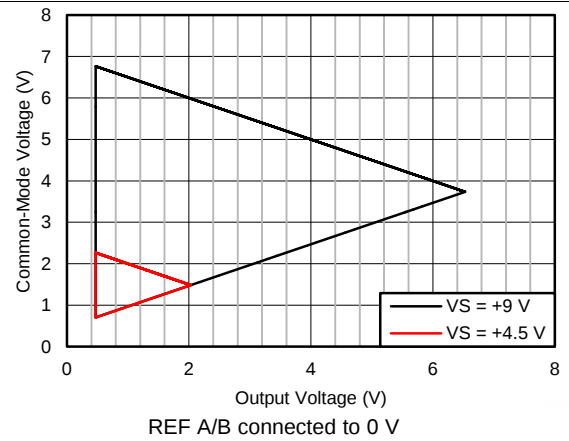


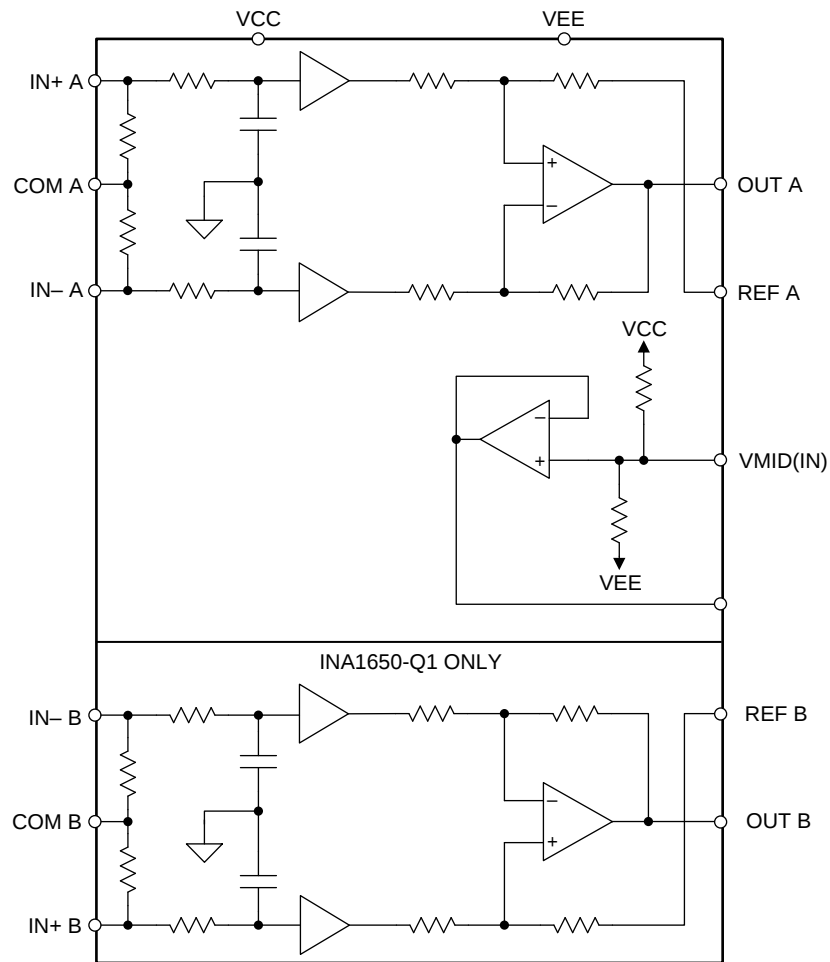
FIG 38. Input Common-Mode Voltage vs Output Voltage

7 Detailed Description

7.1 Overview

The INA165x-Q1 family combines high-performance audio operational amplifier cores with high-precision resistor networks to provide exceptional audio performance and rejection of noise that may be externally coupled into the audio signal path. The two line-receiver channels of the INA1650-Q1, and the single line receiver channel of the INA1651-Q1, use an instrumentation amplifier topology with a fixed unity gain to provide high input impedance and a high common-mode rejection ratio (CMRR). Unlike other line receiver products that use a simple four-resistor difference amplifier topology, the INA165x-Q1 topology provides excellent CMRR even with mismatched source impedances.

7.2 Functional Block Diagram

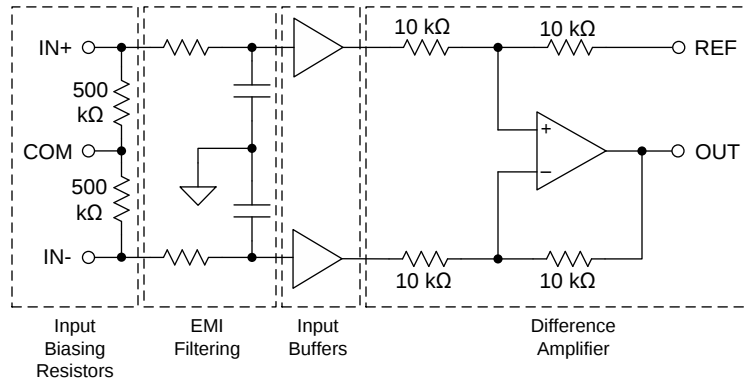


7.3 Feature Description

7.3.1 Audio Signal Path

Figure 39 highlights the basic elements present in the audio signal pathway of the INA165x-Q1 line receivers. The primary elements are input biasing resistors, electromagnetic interference (EMI) filtering, input buffers, and a difference amplifier. The primary role of an audio line receiver is to convert a differential input signal into a single-ended output signal while rejecting noise that is common to both inputs (common-mode noise). The difference amplifier (which consists of an op amp and four matched 10-kΩ resistors) accomplishes this task. The basic transfer function of the circuit is shown in Equation 1:

$$V_{OUT} = (V_{IN+} - V_{IN-}) + V_{REF} \quad (1)$$



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Figure 39. INA165x-Q1 Audio Signal Path (Single Channel Shown)

The input buffers prevent external resistances (such as those from the PCB, connectors, or cables) from ruining the precise matching of the internal 10-kΩ resistors that degrade the high common-mode rejection of the difference amplifier. As is typical of many amplifiers, a small bias current flows into or out of the buffer amplifier inputs. This current must flow to a common potential for the buffer to function properly. The input biasing resistors provide an internal pathway for this current to the COM pin. The COM pin connects to ground in a dual-supply system, or to the output of the internal supply divider, VMID(OUT), in single-supply applications. Finally, EMI filtering is added to the input buffers to prevent high-frequency interference signals from propagating through the audio signal pathway.

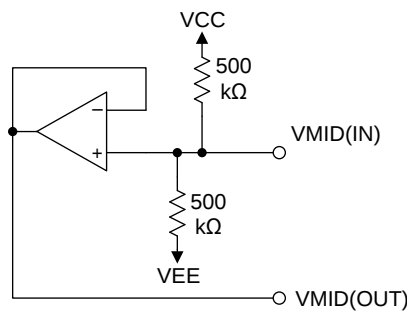
Feature Description (continued)

7.3.2 Supply Divider

The INA165x-Q1 have an integrated supply-divider circuit that biases the input common-mode voltage and output reference voltage to the halfway point between the applied power supply voltages. The nominal output voltage of the supply divider circuit is shown in 式 2:

$$V_{\text{MID(OUT)}} = \frac{V_{\text{CC}} + V_{\text{EE}}}{2} \quad (2)$$

Figure 40 illustrates the internal topology of the supply-divider circuit. The supply divider consists of two 500-kΩ resistors connected between the VCC and VEE pins of the INA165x-Q1. The noninverting input of a buffer amplifier is connected to the midpoint of the voltage divider that is formed by the 500-kΩ resistors. The buffer amplifier provides a low-impedance output that is required to bias the REF pins without degrading the CMRR. For dual-supply applications where the supply divider circuit is not used, no connection is required for the VMID(IN) or VMID(OUT) pins.



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Figure 40. Internal Supply Divider Circuit

Feature Description (continued)

7.3.3 EMI Rejection

The INA165x-Q1 use integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources (such as wireless communications) and densely-populated boards with a mix of analog signal-chain and digital components. The INA165x-Q1 devices are specifically designed to minimize susceptibility to EMI by incorporating an internal low-pass filter. Depending on the end-system requirements, additional EMI filters may be required near the signal inputs of the system; as well as incorporating known good practices, such as using short traces, low-pass filters, and damping resistors combined with parallel and shielded signal routing. Texas Instruments developed a method to accurately measure the immunity of an amplifier over a broad frequency spectrum, extending from 10 MHz to 6 GHz. This method uses an EMI rejection ratio (EMIRR) to quantify the ability of the INA165x-Q1 to reject EMI. [Figure 41](#) and [Figure 42](#) show the INA165x-Q1 EMIRR graph for both differential and common-mode EMI rejection across this frequency range. [Table 1](#) shows the EMIRR values for the INA165x-Q1 at frequencies commonly encountered in real-world applications. Applications listed in [Table 1](#) can be centered on or operated near the particular frequency shown.

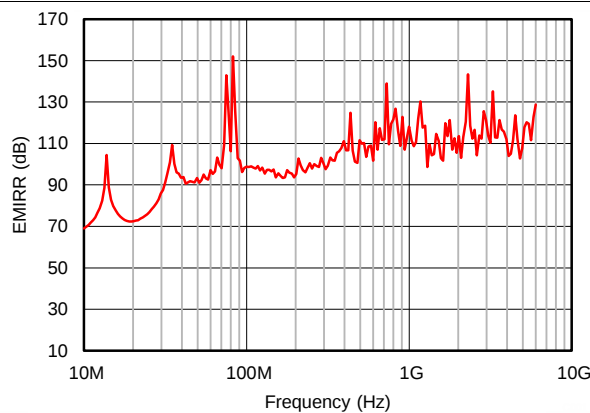


Figure 41. Common-Mode EMIRR Testing

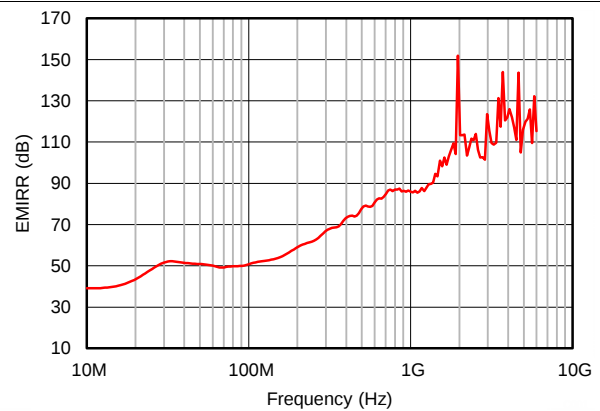


Figure 42. Differential Mode EMIRR Testing

Table 1. EMIRR for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	DIFFERENTIAL EMIRR	COMMON-MODE EMIRR
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh-frequency (UHF) applications	73 dB	111 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (up to 1.6 GHz), GSM, aeronautical mobile, UHF applications	86 dB	123 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	106 dB	121 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	112 dB	119 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	117 dB	121 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	116 dB	108 dB

7.3.4 Electrical Overstress

Designers often ask questions about the capability of an amplifier to withstand electrical overstress. These questions typically focus on the device inputs, but can involve the supply voltage pins or the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events, both before and during product assembly. A good understanding of basic ESD circuitry and the relevance of circuitry to an electrical overstress event is helpful. [Figure 43](#) illustrates the ESD circuits contained in the INA165x-Q1. The ESD protection circuitry involves several current-steering diodes that are connected from the input and output pins, and routed back to the internal power-supply lines. This protection circuitry is intended to remain inactive during normal circuit operation. The input pins of the INA165x-Q1 are protected with internal diodes that are connected to the power-supply rails. These diodes clamp the applied signal to prevent the input circuitry from damage. If the input signal voltage exceeds the power supplies by more than 0.3 V, limit the input signal current to less than 10 mA to protect the internal clamp diodes. A series input resistor can typically limit the current. Some signal sources are inherently current-limited and do not require limiting resistors.

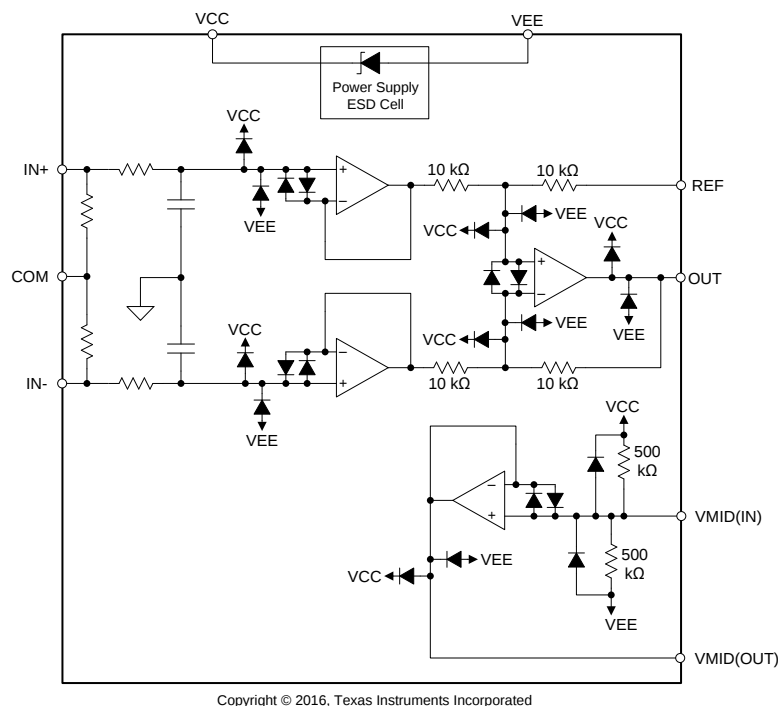


Figure 43. INA165x-Q1 Internal ESD Protection Circuitry (Single Channel and Supply-Divider Shown for Simplicity)

7.3.5 Thermal Shutdown

If the junction temperature of the INA165x-Q1 exceeds approximately 170°C, a thermal shutdown circuit disables the amplifier to protect the device from damage. The amplifier is automatically re-enabled after the junction temperature falls to less than the shutdown threshold temperature. If the condition that caused excessive power dissipation is not removed, the amplifier oscillates between the shutdown and enabled state until the output fault is corrected.

7.4 Device Functional Modes

7.4.1 Single-Supply Operation

The INA165x-Q1 can be used on single power supplies ranging from 4.5 V to 24 V. Use the COM and REF pins to level shift the internal voltages into a linear operating condition. Ideally, connecting the REF and COM pins to a midsupply potential, such as the VMID(OUT) pin, avoids saturating the output of the internal amplifiers.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

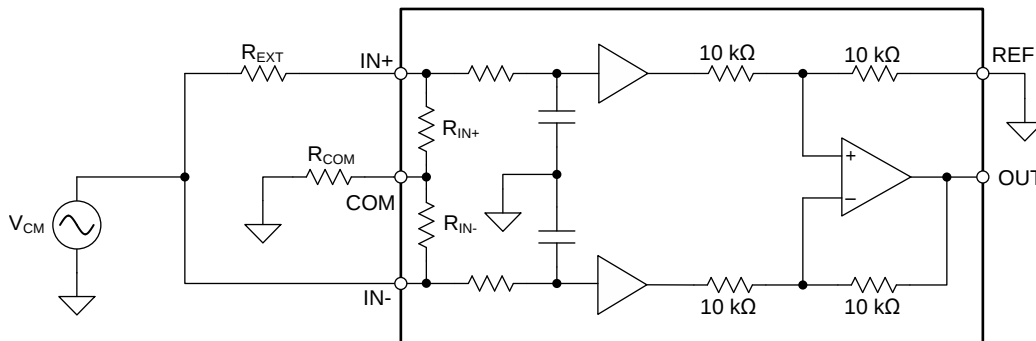
8.1 Application Information

8.1.1 Input Common-Mode Range

The linear input voltage range of the INA165x-Q1 input circuitry extends from 350 mV inside the negative supply voltage to 2 V below the positive supply, and maintains 85-dB (minimum) common-mode rejection throughout this range. The INA165x-Q1 operates over a wide range of power supplies and V_{REF} configurations; providing a comprehensive guide to common-mode range limits for all possible conditions is impractical. The common-mode range for most operating conditions is best calculated using the [INA common-mode range calculating tool](#).

8.1.2 Common-Mode Input Impedance

The high CMRR of many line receivers can degrade by impedance mismatches in the system. [Figure 44](#) shows a common-mode noise source (V_{CM}) connected to both inputs of a single channel of the INA165x-Q1. An external parasitic resistance (R_{EXT}) represents the mismatch in impedances between the common-mode noise source and the inputs of the INA165x-Q1. This mismatched impedance may be due to PCB layout, connectors, cabling, passive component tolerances, or the circuit topology. The presence of R_{EXT} in series with the $IN+$ input degrades the overall CMRR of the system because the voltage at $IN+$ is no longer equal to the voltage at $IN-$. Therefore, a portion of the common-mode noise converts to a differential signal and passes to the output.



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Figure 44. A Single Channel of the INA165x-Q1 Shown With Source Impedance Mismatch (R_{EXT}) and Optional Resistor (R_{COM})

While the INA165x-Q1 is significantly more resistant to these effects than typical line receivers, connecting a resistor (R_{COM}) from the COM pin to the system ground further improves CMRR performance. [Figure 45](#) shows the CMRR of the INA165x-Q1 (typical CMRR of 92 dB) for increasing source impedance mismatches. If the COM pin is connected directly to ground (R_{COM} equal to 0 Ω), a 20- Ω source impedance mismatch degrades the CMRR from 92 dB to 83.7 dB. However, if R_{COM} has a value of 1 M Ω , the CMRR only degrades to 89.6 dB, which is an improvement of approximately 6 dB.

Application Information (continued)

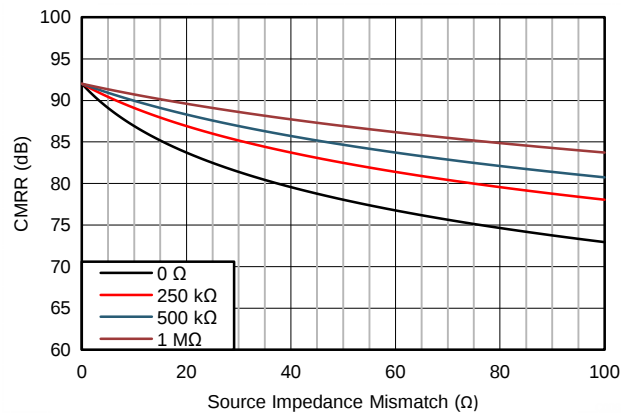


图 45. CMRR vs Source Impedance Mismatch for Different R_{COM} Values

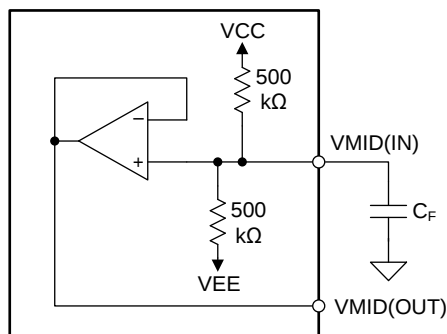
R_{COM} does not need to be a high-precision resistor with a very tight tolerance. Low-cost 5% or 1% resistors can be used with no degradation in overall performance. The addition of R_{COM} does not increase the noise of the audio signal path.

In single-supply systems where AC coupling is used at the inputs of the INA165x-Q1, adding R_{COM} lengthens the start-up time of the circuit. The input AC-coupling capacitors are charged to the midsupply voltage through the R_{COM} resistor, which may take a substantial amount of time if R_{COM} has a large value (such as 1 MΩ). Do not use R_{COM} in these systems if start-up time is a concern. In dual-supply systems with input AC-coupling capacitors, the capacitor voltage does not need to be charged to a midsupply point, because the capacitor voltage settles to ground by default. Therefore, R_{COM} does not increase start-up time in dual-supply systems.

8.1.3 Start-Up Time in Single-Supply Applications

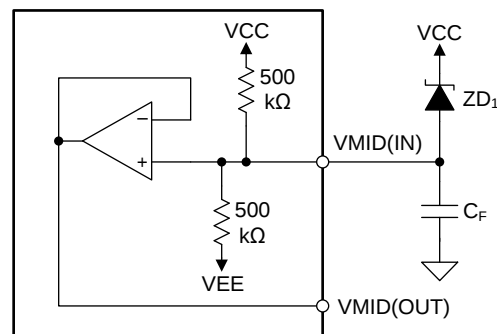
The internal supply divider of the INA165x-Q1 is constructed using two 500-kΩ resistors connected in series between the VCC and VEE pins. These resistors are matched on-chip to provide a reference voltage that is exactly one half of the power supply voltage. Noise from the power supplies and thermal noise from the resistors degrades the overall audio performance of the INA165x-Q1 if allowed to enter the signal path. Therefore, TI recommends a filter capacitor (C_F) is connected to the VMID(IN) pin, as shown in 图 46. The C_F capacitor forms a low-pass filter with the internal 500-kΩ resistors. Noise above the corner frequency of this filter is passed to ground and is removed from the audio signal path. The corner frequency of the filter is shown in 式 3:

$$f_{-3dB} = \frac{1}{2 \cdot \pi \cdot 250 \text{ k}\Omega \cdot C_F} \quad (3)$$



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图 46. Connect a Capacitor (C_F) to the VMID(IN) Pin to Reduce Noise from the Voltage Divider



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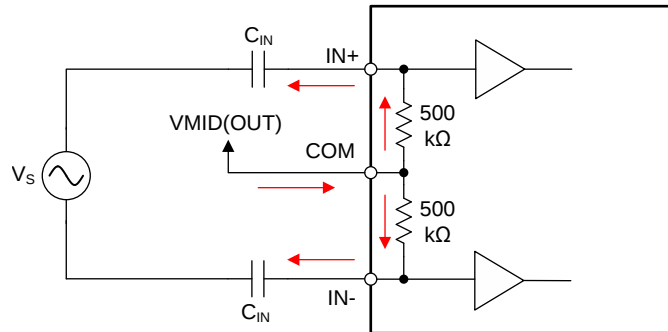
图 47. A Zener Diode (ZD1) Connected to the Positive Supply Can Decrease Start-Up Time

Application Information (continued)

When power is applied to the INA165x-Q1, the filter capacitor (C_F) charges through the internal 500-k Ω resistors. If the C_F capacitor has a large value, the time required for $V_{MID(OUT)}$ to reach the final midsupply voltage may be extensive. Adding a zener diode from the VMID(IN) pin to the positive power supply (as shown in [Figure 47](#)) reduces this time. The zener voltage must be slightly greater than one half of the power supply voltage.

Using large AC-coupling capacitors increases the start-up time of the line receiver circuit in single-supply applications. When power is applied, the AC-coupling capacitors begin to charge to the midsupply voltage applied to the COM pin through a current flowing through the input resistors as shown in [Figure 48](#). The INA165x-Q1 functions properly when the input common-mode voltage (and the capacitor voltage) is within the specified range. The time required for the input common-mode voltage to reach 98% of the final value is shown in [Equation 4](#):

$$t_{98\%} = 4 \cdot R \cdot C_{IN} = 4 \cdot 500 \text{ k}\Omega \cdot C_{IN} \quad (4)$$



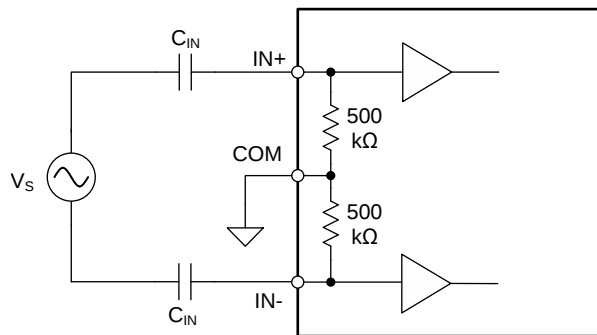
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Figure 48. AC-Coupling Capacitors Charge to the Mid-Supply Voltage Through the Input Resistors

8.1.4 Input AC Coupling

The signal path in most audio systems is typically AC-coupled to avoid the propagation of DC voltages, which can potentially damage loudspeakers or saturate power amplifiers. The capacitor values must be selected to pass the desired bandwidth of audio signals. The high-pass corner frequency is calculated with [Equation 5](#):

$$f_c = \frac{1}{2 \cdot \pi \cdot (2 \cdot R_{IN}) \cdot \frac{C_{IN}}{2}} = \frac{1}{2 \cdot \pi \cdot R_{IN} \cdot C_{IN}} \quad (5)$$



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Figure 49. AC-Coupling Capacitors Form a High-Pass Filter With INA165x-Q1 Input Resistors

Application Information (continued)

Although the input resistors of the INA165x-Q1 are matched typically within 0.01%, large capacitors are usually mismatched. The mismatch in the values of the AC-coupling capacitors causes the corner frequencies at the two signal inputs (IN+ and IN–) to be different, which can degrade CMRR at low frequency. For this reason, TI recommends placing the high-pass corner frequency well below the audio bandwidth and to use a resistor in series with the COM pin (R_{COM}), as shown in [Figure 44](#) if possible. See the [Common-Mode Input Impedance](#) section for more information on placing a resistor in series with the COM pin. [Figure 50](#) shows the effect of a 5% mismatch in the values of the input AC-coupling capacitors with and without an R_{COM} resistor. Comparing CMRR at 100 Hz: 1- μ F AC-coupling capacitors with a 5% mismatch degrade the CMRR to 75 dB, while 10- μ F capacitors and a 1-M Ω R_{COM} resistor shows 92 dB of CMRR.

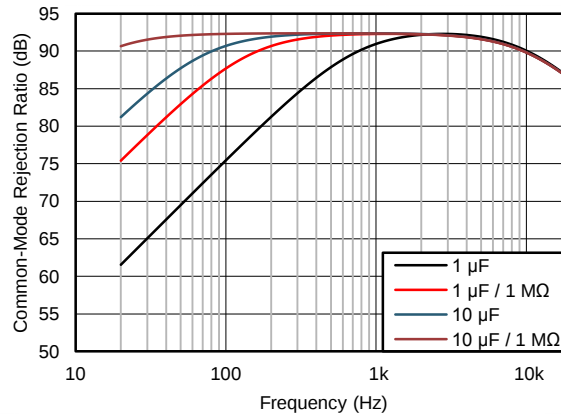
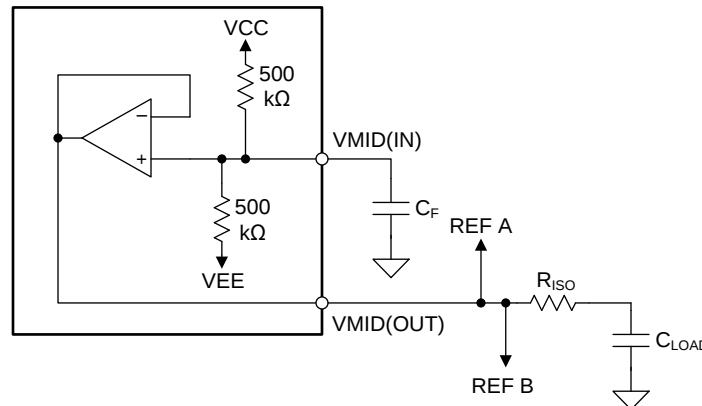


Figure 50. CMRR Degradation Due to a 5% Mismatch in AC-Coupling Capacitors

8.1.5 Supply Divider Capacitive Loading

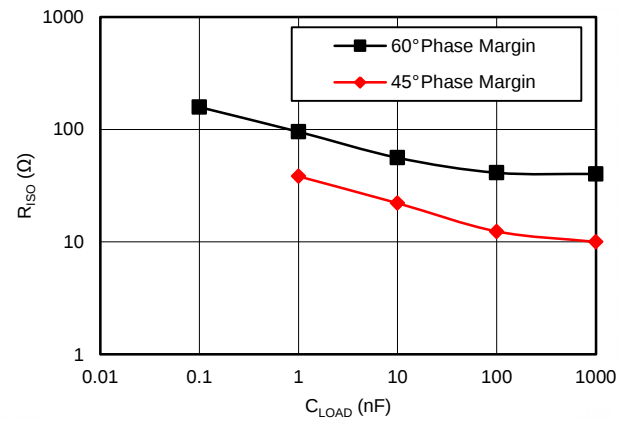
The VMID(OUT) pin of the INA165x-Q1 is stable with capacitive loads up to 150 pF. An isolation resistor (R_{ISO} in [Figure 51](#)), must be used if capacitive loads larger than 150 pF are connected to the VMID(OUT) pin. [Figure 51](#) shows the recommended configuration of an isolation resistor in series with the capacitive load. The REF pins of the INA165x-Q1 must connect directly to the VMID(OUT) pin before the isolation resistor. Any resistance placed between the VMID(OUT) pin and the reference pins degrades the CMRR of the device. [Figure 52](#) shows the recommended value for the isolation resistor for increasing capacitive loads.



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Figure 51. Place an Isolation Resistor Between the VMID(OUT) Pin and Large Capacitive Loads

Application Information (continued)



52. Recommended Isolation Resistor Value vs Capacitive Load

8.2 Typical Applications

The low noise and distortion of the INA165x-Q1 make the devices an excellent choice for a variety of applications in professional and consumer audio products. However, these same performance metrics make the INA165x-Q1 useful for industrial, test and measurement, and data-acquisition applications. The examples shown here are possible applications where the INA165x-Q1 provides exceptional performance.

8.2.1 Line Receiver for Differential Audio Signals in a Split-Supply System

The INA165x-Q1 are designed to require a minimum number of external components to achieve data sheet-level performance in audio line-receiver applications. [Figure 53](#) shows the INA165x-Q1 used as a differential audio line receiver in split-supply systems that are common in many audio applications. The line receiver recovers a differential audio signal that may have been affected by significant common-mode noise.

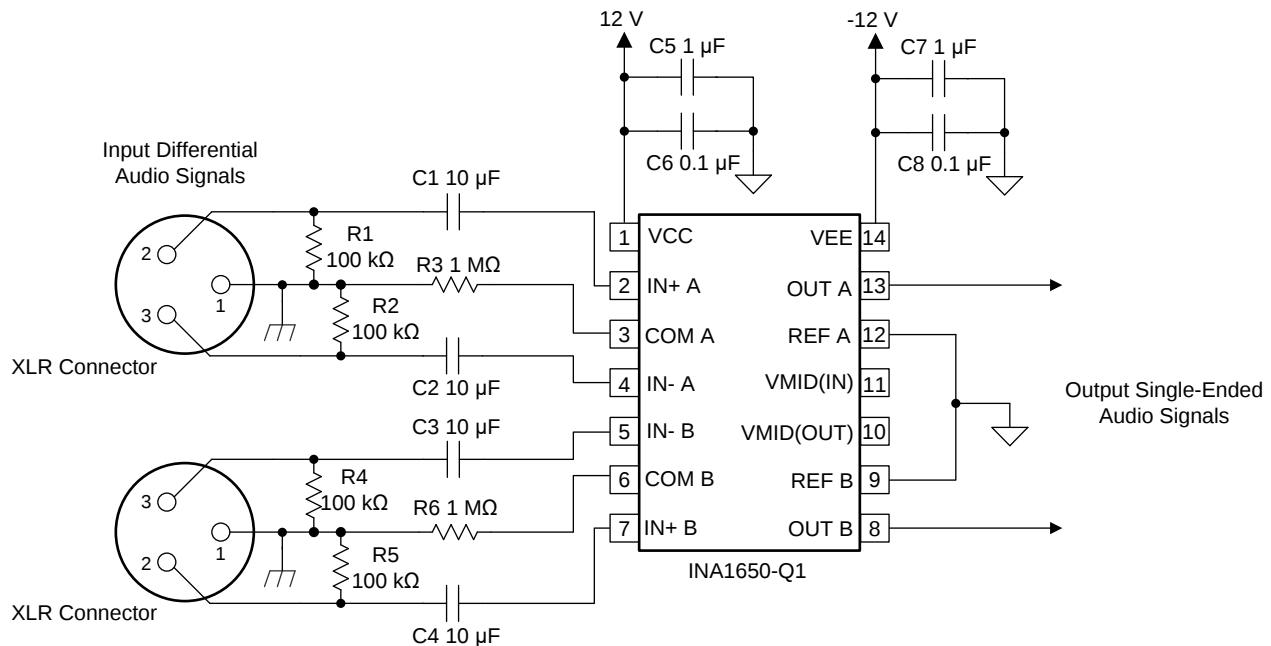


Figure 53. INA1650-Q1 Device Used as a Line Receiver for Differential Audio Signals in a Split-Supply System

Typical Applications (continued)

8.2.1.1 Design Requirements

- Power supply voltage: ± 12 V
- Frequency response: < 0.1 dB deviation from 20 Hz to 20 kHz
- Common-mode rejection ratio: > 80 dB at 1 kHz
- THD+N: < -100 dB (4-dBu input signal, 1-kHz fundamental, 90-kHz measurement bandwidth)

8.2.1.2 Detailed Design Procedure

The passive components shown in [Figure 53](#) are selected using the information given in the [Application Information](#) and [Layout Guidelines](#) sections. All 10- μ F input ac-coupling capacitors (C1, C2, C3, and C4) maximize the CMRR performance at low frequency, as shown in [Figure 50](#). The high-pass corner frequency for input signals meets the design requirement for frequency response, as [Equation 6](#) shows:

$$f_c = \frac{1}{2 \cdot \pi \cdot R_{IN} \cdot C_{IN}} = \frac{1}{2 \cdot \pi \cdot (500 \text{ k}\Omega) \cdot (10 \text{ }\mu\text{F})} = 0.032 \text{ Hz} \quad (6)$$

The 1-M Ω R_{COM} resistors (R3 and R4) further improve CMRR performance at low frequency. Resistors R1, R2, R4, and R5 provide a discharge pathway for the ac-coupling capacitors in the event that audio equipment with a dc offset voltage is connected to the inputs of the circuit. These resistors are optional and may degrade the CMRR performance with mismatches in source impedance. Finally, capacitors C5, C6, C7, and C8 provide a low-impedance pathway for power supply noise to pass to ground rather than interfering with the audio signal. No connection is necessary on the VMID(IN) and VMID(OUT) pins because the supply-divider circuit is not used in this particular application.

8.2.1.3 Application Curves

[Figure 54](#) through [Figure 59](#) illustrate the measured performance of the line receiver circuit. [Figure 54](#) shows the measured frequency response. The gain of the circuit is 0 dB as expected with 0.1-dB magnitude variation at 10 Hz. The measured CMRR of the circuit ([Figure 55](#)) at 1 kHz equals 94 dB without any source impedance mismatch. Adding a 10- Ω source impedance mismatch degrades the CMRR at 1 kHz to 92 dB. The high-frequency degradation of CMRR shown in [Figure 55](#) for the 10- Ω source impedance mismatch cases is due to the capacitance of the cables used for the measurement. The total harmonic distortion plus noise (THD+N) is plotted over frequency in [Figure 56](#). For a 4-dBu (1.23 V_{RMS}) input signal level, the THD+N remains flat at -101.6 dB (0.0008%) over the measured frequency range. Increasing the signal level to 20 dBu further decreases the THD+N to -113.2 dB (0.00022%) at 1 kHz, but the THD+N rises to greater than 7 kHz. Measuring the THD+N vs output amplitude ([Figure 57](#)) at 1 kHz shows a constant downward slope until the noise floor of the audio analyzer is reached at 5 V_{RMS} . The constant downward slope indicates that noise from the device dominates THD+N at this frequency instead of distortion harmonics. [Figure 58](#) and [Figure 59](#) confirm this conclusion. For a 4-dBu signal level, the second harmonic is barely visible above the noise floor at -140 dBu. Increasing the signal level to 20 dBu produces distortion harmonics above the noise floor. The largest harmonic in this case is the second at -111.2 dBu, or -131.2 dB relative to the fundamental.

Typical Applications (continued)

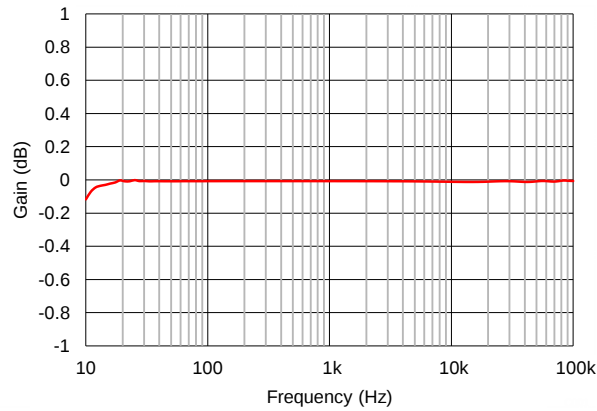


Figure 54. Frequency Response

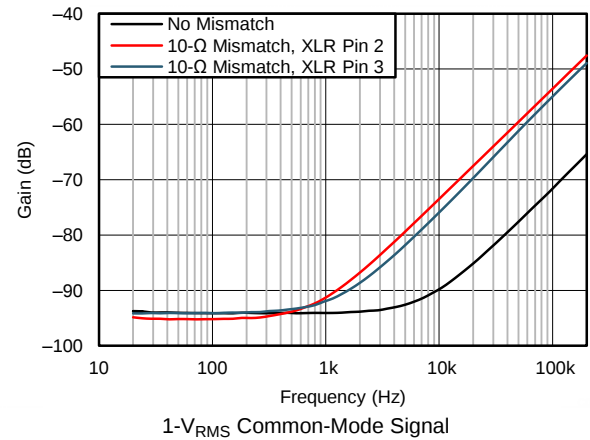


Figure 55. Common-Mode Rejection Ratio vs Frequency

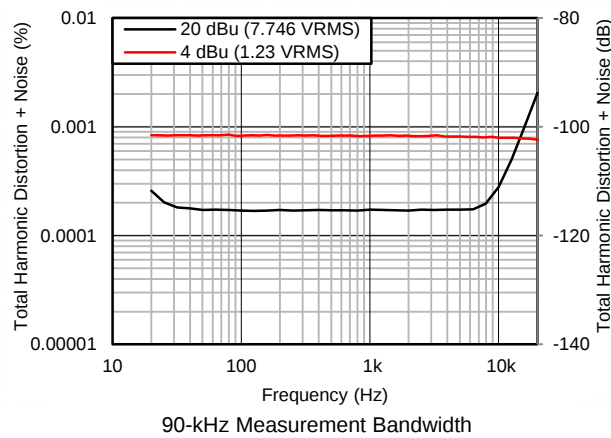


Figure 56. THD+N vs Frequency

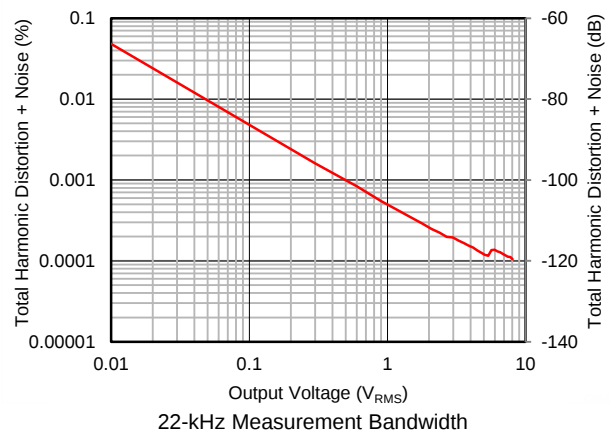


Figure 57. THD+N vs Amplitude

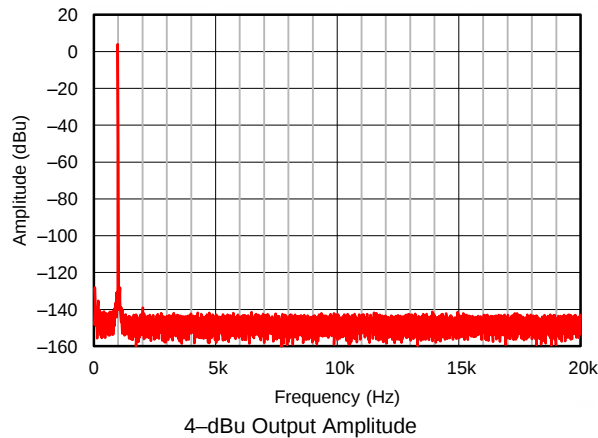


Figure 58. Output Spectrum

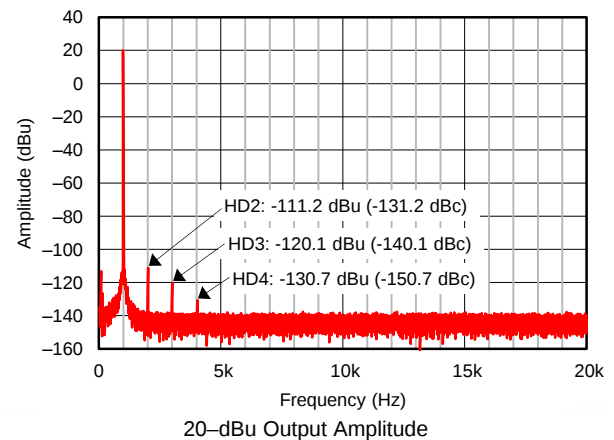


Figure 59. Output Spectrum

Typical Applications (continued)

8.2.2 Two-Channel Microphone Input for Automotive Infotainment Systems

The high CMRR, low-noise, and ease-of-use in single supply applications make the INA165x-Q1 an excellent choice for applications in automotive infotainment systems. [Figure 60](#) illustrates a high-CMRR input circuit for in-cabin microphones used for hands-free phone systems. The microphones are connected with matched bias resistors, R_{BIAS} , to preserve the high-CMRR performance of the INA165x-Q1. The exact value of the microphone bias voltage, V_{BIAS} , and the R_{BIAS} resistors depends on the particular microphones used. Bandwidth-limiting the audio signal to the range of frequencies for speech is common in hands-free systems. As shown in [Figure 60](#), all filtering components are placed at the output of the INA165x-Q1 rather than the input to preserve high CMRR. The values shown in [Figure 60](#) limit the signal bandwidth to approximately 100 Hz to 10 kHz.

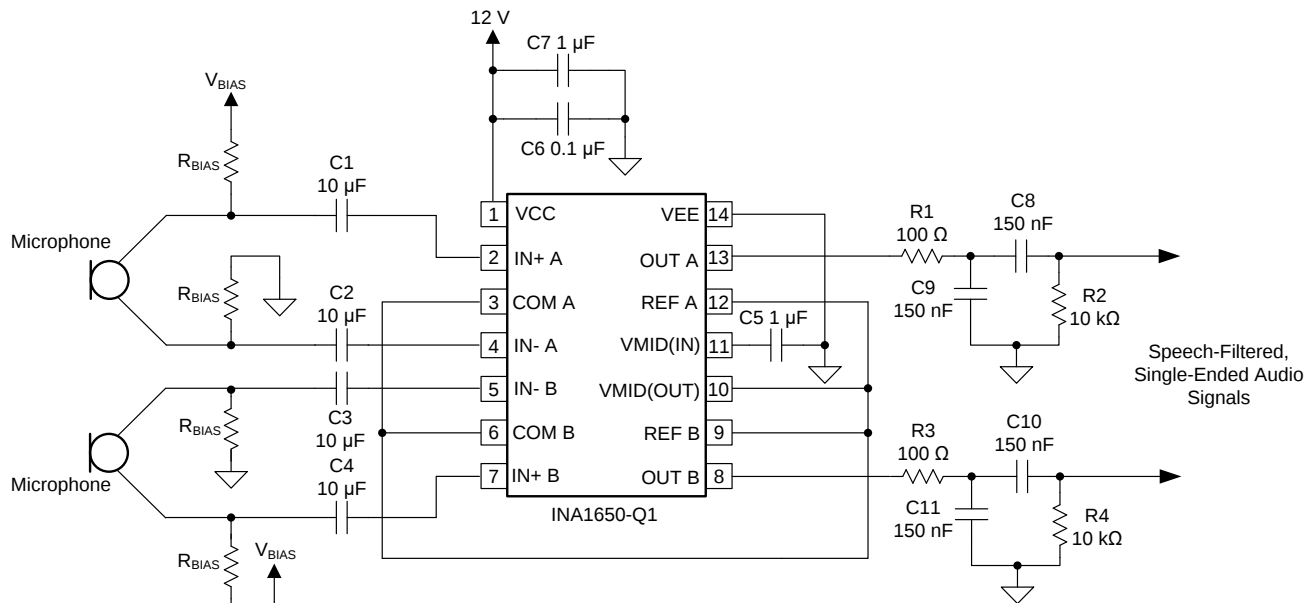


Figure 60. Two-channel Microphone Input for Automotive Infotainment Systems

Typical Applications (continued)

8.2.3 TRS Audio Interface in Single-Supply Applications

The INA165x-Q1 can be used for auxiliary audio inputs that may use a tip-ring-sleeve (TRS) connector where both audio channels share a common ground connection. [Figure 61](#) shows the INA1650-Q1 configured as a line receiver for a TRS interface to remove common-mode noise on the sleeve connection.

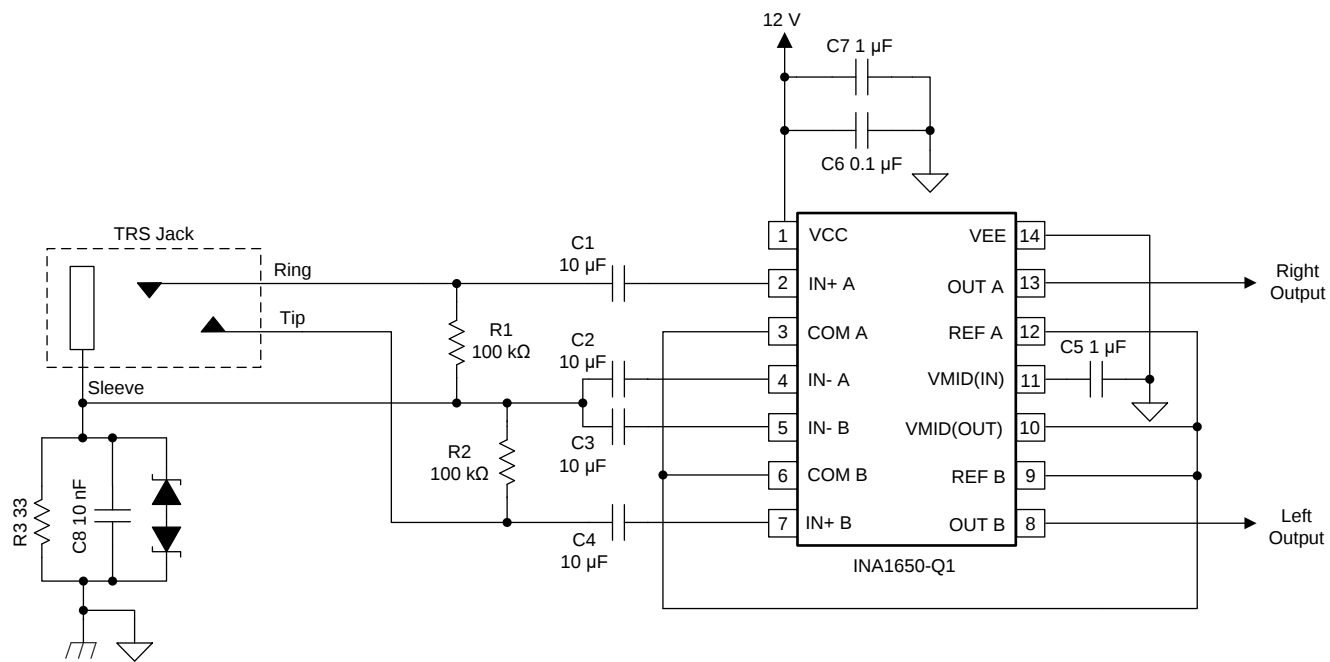


Figure 61. TRS Audio Interface in Single-Supply Applications

9 Power Supply Recommendations

The INA165x-Q1 operate from $\pm 2.25\text{-V}$ to $\pm 12\text{-V}$ supplies while maintaining excellent performance. However, some applications do not require equal positive and negative output voltage swing. With the INA165x-Q1, power-supply voltages do not need to be equal. For example, the positive supply can be set to 19 V with the negative supply at -5 V .

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Connect low-ESR, 1- μF and 0.1- μF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. Connecting bypass capacitors only from $V+$ to ground is acceptable in single-supply applications. Noise can propagate into analog circuitry through the power pins of this device. The bypass capacitors reduce the coupled noise by providing low-impedance pathways to ground.
- Connect the device REF pins to a low-impedance, low-noise, system reference point (such as an analog ground or the VMID(OUT) pin) with the shortest trace possible.
- Place the external components as close to the device as possible, as shown in [Figure 62](#) and [Figure 63](#).
- Use ground pours and planes to shield input signal traces and minimize additional noise introduced into the signal path.
- Keep the length of input traces equal and as short as possible. Route the input traces as a differential pair with as minimal spacing between them as possible.

10.2 Layout Example

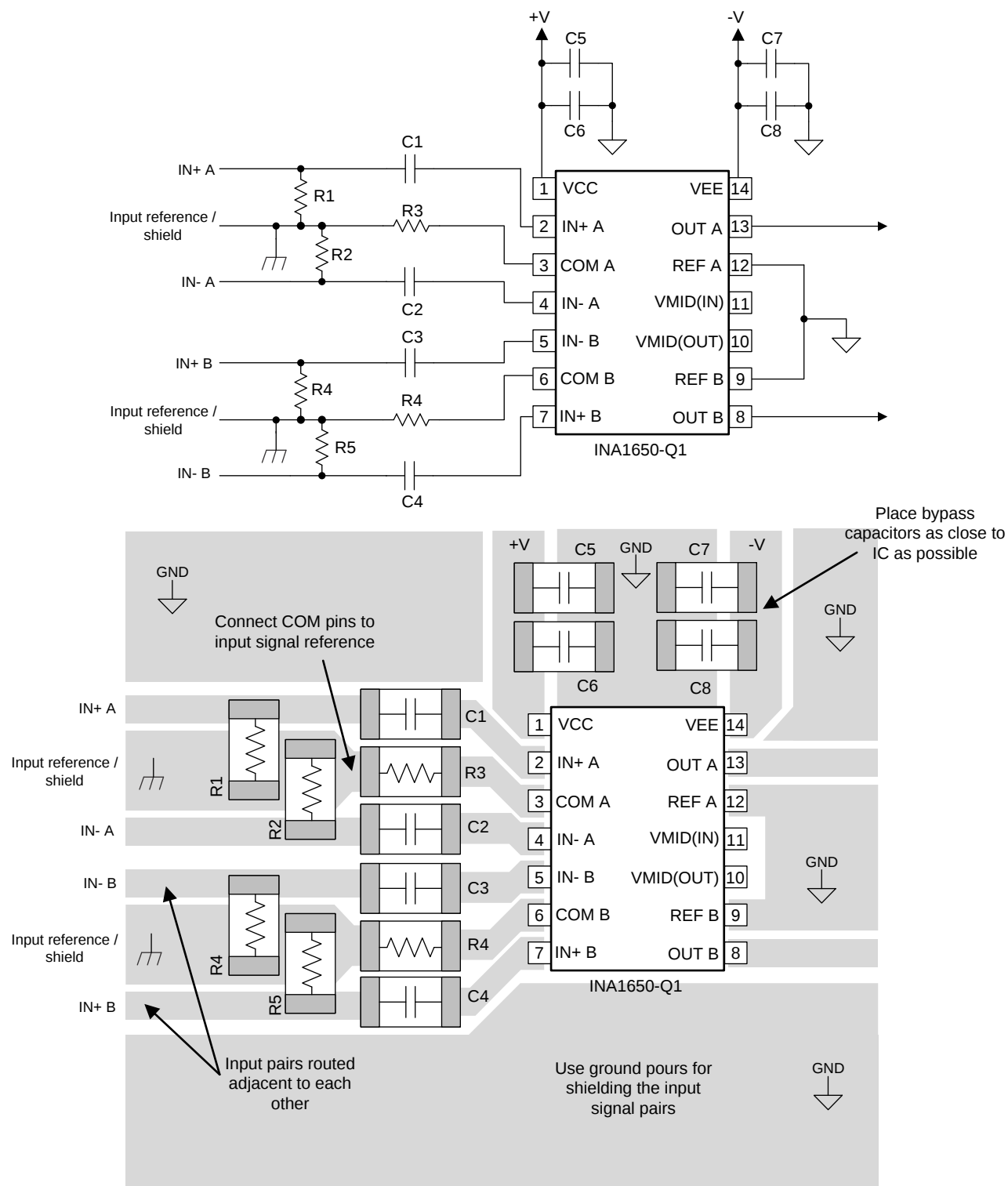


FIG 62. Layout Example for a Dual-Supply Line Receiver

Layout Example (continued)

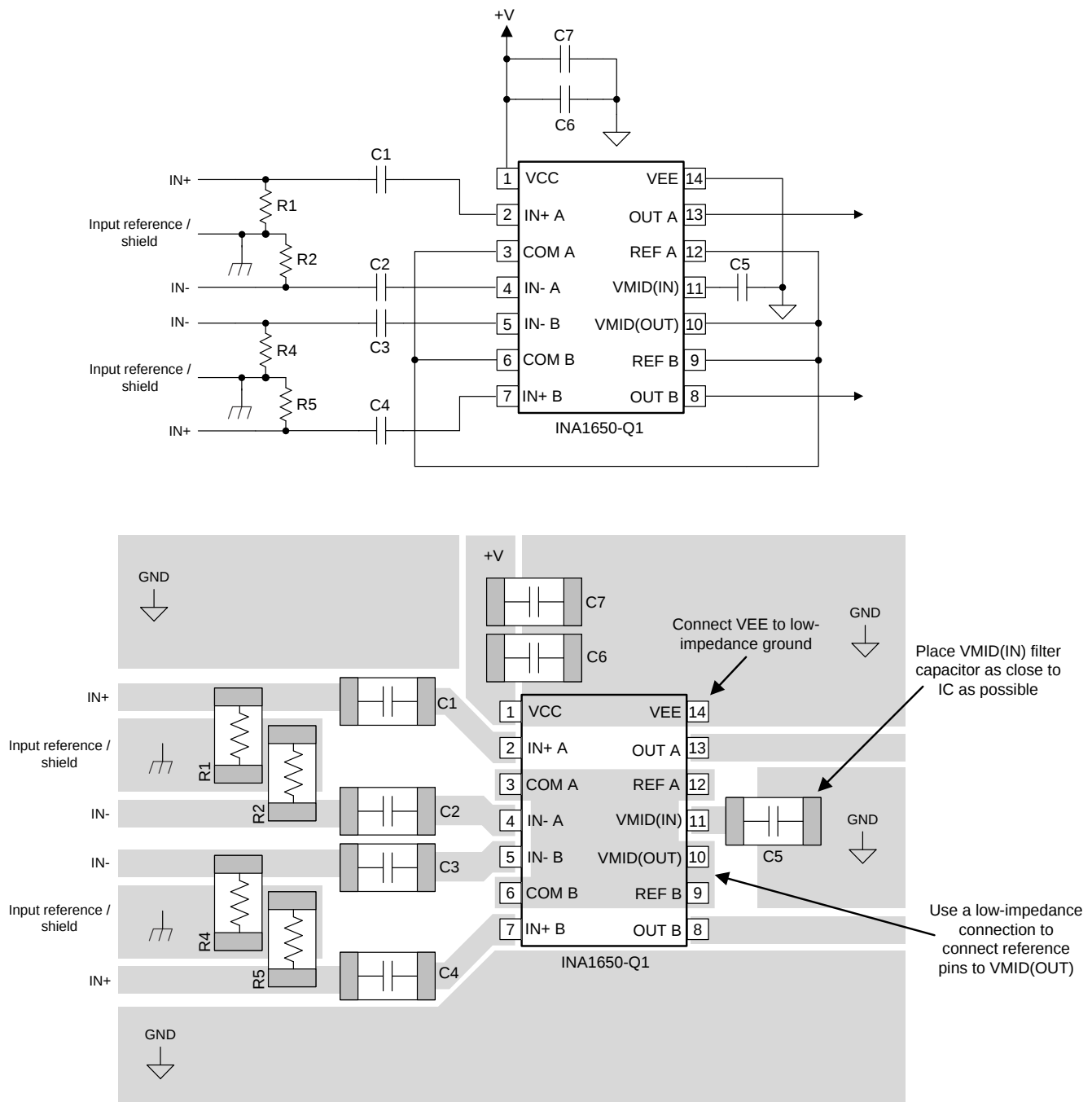


FIG 63. Layout Example for a Single-Supply Line Receiver

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 TINA-TI™(無料のダウンロード・ソフトウェア)

TINA™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。また、TINA-TIは、TINAソフトウェアの完全な機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには、SPICEの標準的なDC解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TIはWEBENCH® Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

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11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、[『回路基板のレイアウト技法』](#)
- テキサス・インスツルメンツ、[『On-Chip Thin Film Resistors Enable High-Performance Audio Circuitry』](#)テクニカル・ブリーフ (英語)

11.3 ドキュメントの更新通知を受け取る方法

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The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA1650QPWRQ1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IN1650A
INA1650QPWRQ1.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IN1650A
INA1651QPWRQ1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IN1651Q
INA1651QPWRQ1.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IN1651Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF INA1650-Q1, INA1651-Q1 :

- Catalog : [INA1650](#), [INA1651](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

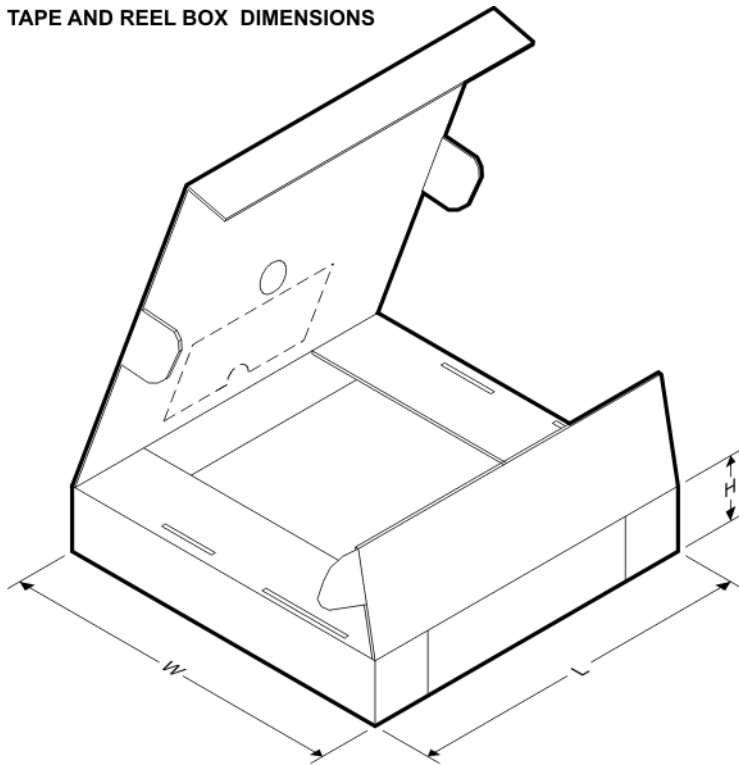
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA1650QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA1651QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA1650QPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0
INA1651QPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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