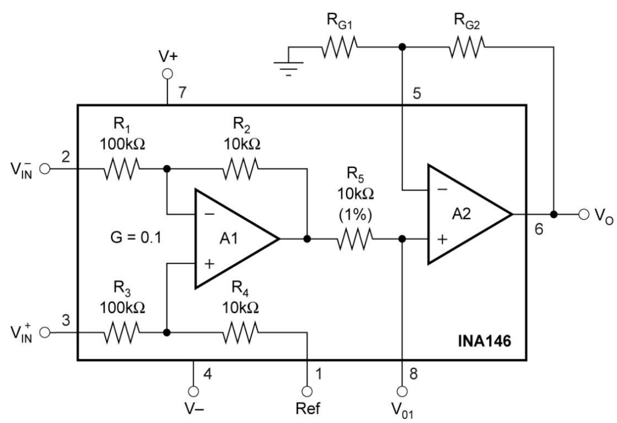
INA146 高電圧、プログラマブル ゲイン差動アンプ

1 特長

- 高い同相電圧:
  - 40V (V_S = 5V 時)
  - ±100V (V_S = ±15V 時)
- 差動ゲイン = 0.1V/V～100V/V:
  - 外付け抵抗により設定
- 低い静止電流:570μA
- 幅広い電源電圧範囲:
  - 単電源:4.5V～36V
  - 両電源:±2.25V～±18V
- 低ゲイン誤差:0.025%
- 大きい同相除去:80dB

2 アプリケーション

- バッテリ・セル形成とテスト機器
- AC ドライブ制御モジュール
- HVAC コントローラ
- 業務用オーディオ・アンプ (ラック・マウント)
- プログラマブル DC 電源
- データ・アクイジション (DAQ)



INA146 の概略ブロック図

3 概要

INA146 は高精度の差動アンプで、高い差動電圧を正確に減衰させ、高い同相電圧を除去して、一般的な信号処理電圧レベルとの互換性を確保できます。また、高電圧機能により、継承的に入力保護機能も備えていることになります。入力同相範囲が両方の電源レールを超えているため、INA146 は単電源と両電源の両方のアプリケーションに最適です。

レーザ トリミングされたオンチップの高精度抵抗により、高いゲイン精度と高い同相除去比を実現します。これらの抵抗の優れた TCR トラッキングにより、温度範囲全体にわたって高精度が維持されます。

出力アンプがユニティ ゲイン バッファとして使用されている場合、10:1 の差動アンプにより 0.1V/V のゲインが得られます。この構成では、最大 ±100V までの入力電圧を測定できます。0.1V/V を超えるゲインは、同相入力範囲に影響を与えることなく、外付けの抵抗ペアを使用して設定できます。

INA146 は、拡張工業用温度範囲 (-40℃～85℃) で動作が規定されている、SO-8 表面実装パッケージで供給されます。

パッケージ情報

部品番号	パッケージ (1)	規定温度範囲	パッケージ・サイズ (2)
INA146	SOIC (8)	-40℃～85℃	4.90mm × 6.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。

Table of Contents

1 特長.. 1
2 アプリケーション...1
3 概要.. 1
4 Pin Configuration and Functions..................................3
5 Specifications.. 4
5.1 Absolute Maximum Ratings..4
5.2 ESD Ratings 4
5.3 Recommended Operating Conditions.........................4
5.4 Thermal Information..4
5.5 Electrical Characteristics V_S = ±2.25 V to ±18 V.........5
5.6 Electrical Characteristics V_S = 5 V Single Supply.......6
5.7 Amplifier A1, A2 Performance....................................7
5.8 Typical Performance Curves......................................8
6 Application and Implementation................................. 11
6.1 Application Information...11
7 Device and Documentation Support............................17
7.1 サード・パーティ製品に関する免責事項.......................17
7.2 Documentation Support.. 17
7.3 ドキュメントの更新通知を受け取る方法........................ 17
7.4 サポート・リソース... 17
7.5 Trademarks... 17
7.6 静電気放電に関する注意事項.................................... 17
7.7 用語集... 17
8 Revision History... 18
9 Mechanical, Packaging, and Orderable Information.. 19

4 Pin Configuration and Functions

Top View SO-8

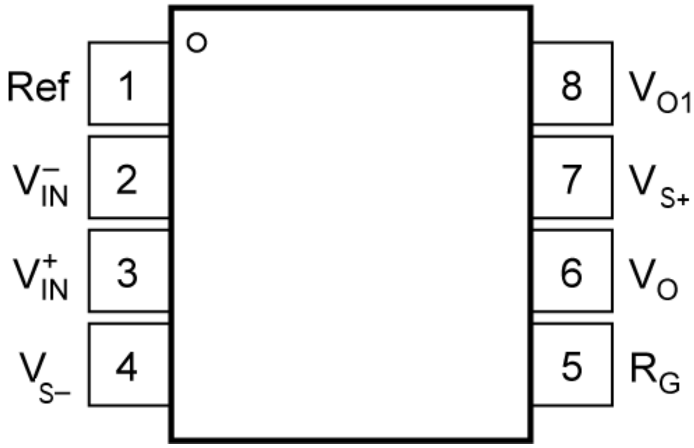


図 4-1. INA146 D Package, 8-Pin SOIC (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
Ref	1	I	Reference input. This pin must be driven by a low impedance source.
V_{IN-}	2	I	Negative (inverting) input
V_{IN+}	3	I	Positive (non-inverting) input
V_{S-}	4	−	Negative supply
R_G	5	I	Gain setting input. Place a resistor network between pin 1 and pin 5.
V_O	6	O	Output of amplifier A2
V_{S+}	7	−	Positive supply
V_{O1}	8	O	Output of amplifier A1

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_S	Supply voltage	Dual supply, $V_S = (V_{S+}) – (V_{S–})$		±18	V
		Single supply, $V_S = (V_{S+}) – 0$ V		36	
V_{IN+}, $V_{IN–}$	Signal input voltage			±100	V
	Signal input current			±1	mA
	Output short-circuit[(2)]		Continuous		
T_A	Operating temperature		–55	125	°C
T_{stg}	Storage temperature		–55	125	°C
T_J	Junction temperature			150	°C
	Lead temperature (soldering, 10 s)			240	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_S	Supply voltage	Single-supply	4.5	30	36	V
		Dual-supply	±2.25	±15	±18	
T_A	Specified temperature		–40		85	°C

5.4 Thermal Information

THERMAL METRIC[(1)]		INA146 SO-8 8 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	110.3	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	43.6	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	55.5	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	6.2	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	54.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics V_S = ±2.25 V to ±18 V

at T_A = 25°C, V_S = ±2.25 V to ±18 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 0.1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage, V_O	RTI, V_S = ±15 V, V_{CM} = 0 V			±1	±5	mV
	Offset voltage, V_{O1}	RTI			±1		mV
	Offset voltage drift	RTI, T_A = –40°C to 85°C			±10		μV/°C
PSRR	Power-supply rejection ratio	RTI, V_S = ±1.35 V to ±18 V			±100	±600	μV/V
V_{CM}	Common-mode voltage [1]	V_S = ±15 V, V_{IN} = 0 V		–100		100	V
CMRR	Common-mode voltage rejection	RTI, 11 (–V_S) < V_{CM} < 11 (V_S -1) , R_S = 0 Ω		70	80		dB
		T_A = –40°C to 85°C		64	74		
	Differential input impedance	Non-inverting input			110		kΩ
		Inverting input			91.7		
	Common-mode input impedance				55		kΩ
BIAS CURRENT							
I_B	Bias Current	V_{CM} = V_S / 2			±50		nA
I_{OS}	Offset Current				±5		nA
NOISE							
e_N	Voltage noise	RTI, f_B = 0.1 Hz to 10 Hz			12		μV_{PP}
		RTI, f = 1 kHz			550		$nV/\sqrt{Hz}$
GAIN							
	Gain			0.1		100	V/V
GE	Gain error	V_O = (V–) + 0.15 V to (V+) – 1 V, R_L = 100 kΩ, G = 1			±0.025	±0.1	%
		V_O = (V–) + 0.3 V to (V+) – 1.25 V, R_L = 10 kΩ, G = 1			±0.025	±0.1	
	Gain error drift[2]	T_A = –40°C to 85°C	V_O = (V–) + 0.25 V to (V+) – 1 V, R_L = 100 kΩ, G = 1		±1	±10	ppm/°C
			V_O = (V–) + 0.5 V to (V+) – 1.25 V, R_L = 10 kΩ, G = 1		±1	±10	
	Gain nonlinearity	V_O = (V–) + 0.3 V to (V+) – 1.25 V, G = 1			±0.001	±0.01	% of FSR
OUTPUT							
	Output voltage	R_L = 100 kΩ, G = 1		(V–) + 0.15		(V+) – 1	V
			T_A = –40°C to 85°C	(V–) + 0.25		(V+) – 1	
		R_L = 10 kΩ, G = 1		(V–) + 0.3		(V+) – 1.25	
			T_A = –40°C to 85°C	(V–) + 0.5		(V+) – 1.25	
C_L	Load capacitance	Stable operation			1		nF
I_{SC}	Short-circuit current	Continuous to V_S / 2			±15		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB	G = 0.1			550		kHz
		G = 1			50		
SR	Slew rate				0.3		V/μs
t_S	Settling time	To 0.1%,	V_O = 10 V-step		40		μs
		To 0.01%	V_O = 10 V-step		80		
	Overload recovery	50% input overload			40		μs
POWER SUPPLY							
I_Q	Quiescent current	V_{IN} = 0 V			±570	±700	μA
		T_A = –40°C to 85°C				±750	

(1) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.
(2) Specified by wafer test.

5.6 Electrical Characteristics V_S = 5 V Single Supply

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 0.1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage, V_O	RTI, V_{CM} = 0 V			±3	±10	mV
	Offset voltage, V_{O1}	RTI, V_{CM} = 0 V			±1		mV
	Offset voltage drift	RTI, T_A = –40℃ to 85℃			±10		µV/°C
PSRR	Power-supply rejection ratio	RTI, V_S = ±1.35 V to ±18 V			±100	±600	µV/V
V_{CM}	Common-mode voltage (1)	V_{IN} = 0 V		–25		19	V
CMRR	Common-mode voltage rejection	V_{CM} = –25 V to 19 V, R_S = 0 Ω		70	80		dB
		T_A = –40℃ to 85℃		64	74		
	Differential input impedance	Non-inverting input			110		kΩ
		Inverting input			91.7		
	Common-mode input impedance				55		kΩ
BIAS CURRENT							
I_B	Bias Current	V_{CM} = V_S / 2			±50		nA
I_{OS}	Offset Current	V_{CM} = V_S / 2			±5		nA
NOISE							
e_N	Voltage noise	RTO, f_B = 0.1 Hz to 10 Hz			12		$µV_{PP}$
		RTO, f = 1 kHz			550		nV/√Hz
GAIN							
	Gain			0.1		100	V/V
GE	Gain error	V_O = 0.15 V to 4 V, R_L = 100 kΩ			±0.025	±0.1	%
		V_O = 0.3 V to 3.75 V, R_L = 10 kΩ			±0.025	±0.1	
	Gain error drift(2)	T_A = –40°C to 85°C	V_O = 0.25 V to 4 V, R_L = 100 kΩ		±1	±10	ppm/°C
			V_O = 0.5 V to 3.75 V, R_L = 10 kΩ		±1	±10	
	Gain nonlinearity	V_O = 0.3 V to 3.75 V			±0.001	±0.01	% of FSR
OUTPUT							
	Output voltage	R_L = 100 kΩ		0.15		4	V
			T_A = –40℃ to 85℃	0.25		4	
		R_L = 10 kΩ		0.3		3.75	
			T_A = –40℃ to 85℃	0.5		3.75	
C_L	Load capacitance	Stable operation			1		nF
I_{SC}	Short-circuit current	Continuous to V_S / 2			±15		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB	G = 0.1			550		kHz
		G = 1			50		
SR	Slew rate				0.3		V/µs
t_S	Settling time	To 0.1%,	V_O = 10 V-step		40		µs
		To 0.01%	V_O = 10 V-step		80		
	Overload recovery	50% input overload			40		µs
POWER SUPPLY							
I_Q	Quiescent current	V_{IN} = 0 V			±570	±700	µA
		T_A = –40℃ to 85℃				±750	

(1) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.
(2) Specified by wafer test.

5.7 Amplifier A1, A2 Performance

at T_A = 25°C, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 0.1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{OS}	Offset voltage, V_O	RTI, V_S = ±15 V, V_{CM} = V_O = 0 V		±0.5		mV
	Offset voltage drift	RTI, T_A = –40℃ to 85℃		±1		μV/°C
V_{CM}	Common-mode voltage (1)	V_{IN} = V_O = 0 V		V_{S-} to (V_{S+}) –1		V
CMRR	Common-mode voltage rejection	V_{CM} = V_{S-} to (V_{S+}) –1		90		dB
GAIN						
A_{OL}	Open Loop Gain			110		dB
BIAS CURRENT						
I_B	Bias Current			±50		nA
I_{OS}	Offset Current			±5		nA
OUTPUT						
	Resistor at V_{O1}	Initial		10		kΩ
	Error at V_{O1}			±1		%
	Error drift at V_{O1}			±100		ppm/℃

(1) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.

5.8 Typical Performance Curves

At T_A = 25°C, V_S = ±15 V, G = 0.1, R_L = 10 kΩ connected to ground and Ref pin connected to ground, unless otherwise noted.

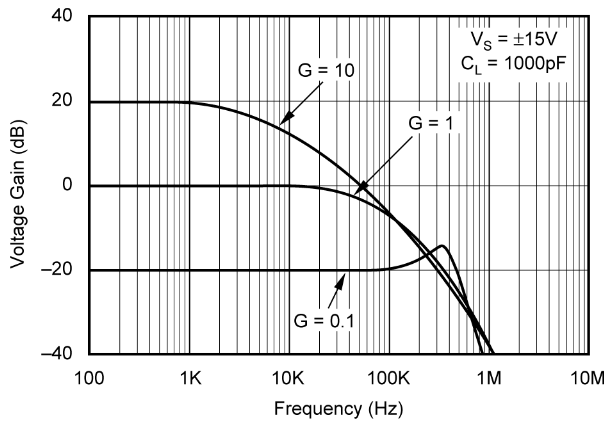


図 5-1. Gain vs Frequency

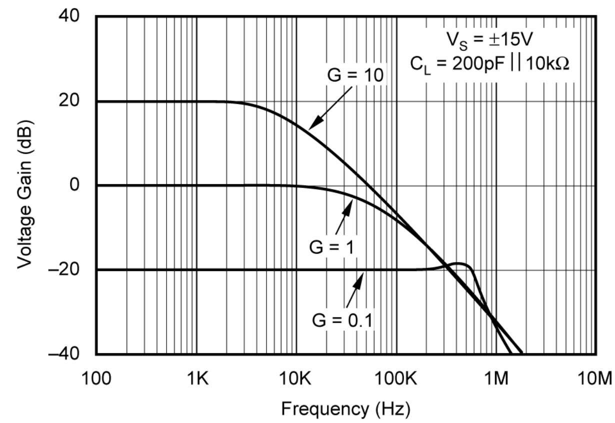


図 5-2. Gain vs Frequency

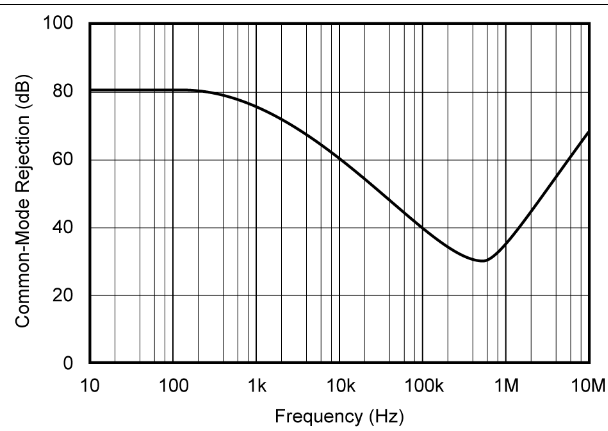


図 5-3. Common-mode Rejection vs Frequency

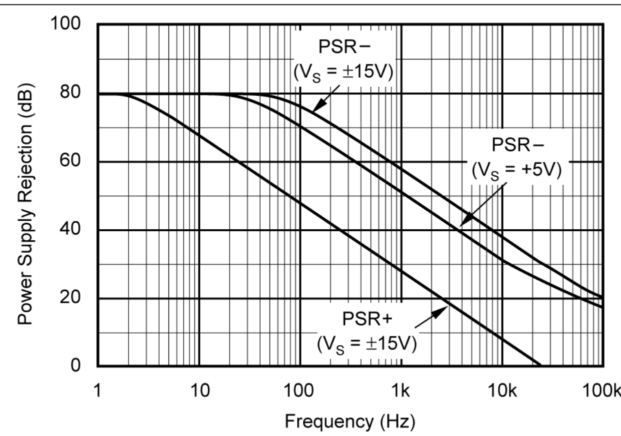


図 5-4. Power Supply Rejection vs Frequency

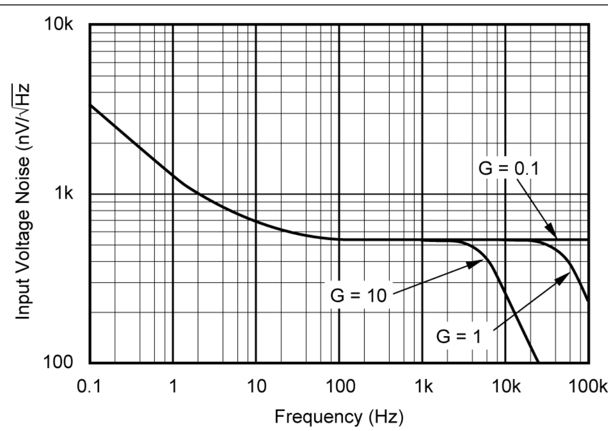


図 5-5. Input Voltage Noise Density

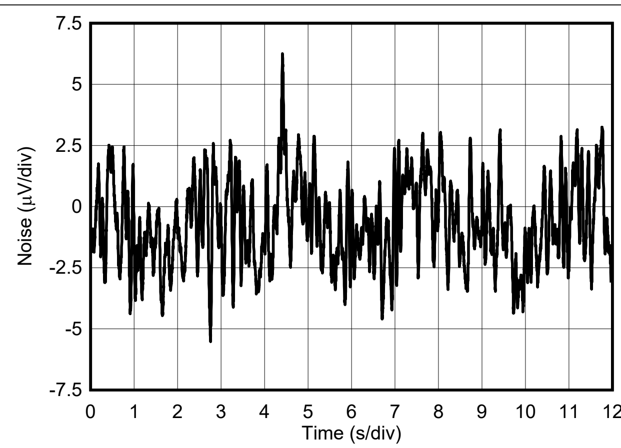


図 5-6. 0.1-Hz to 10-Hz Voltage Noise (Rti)

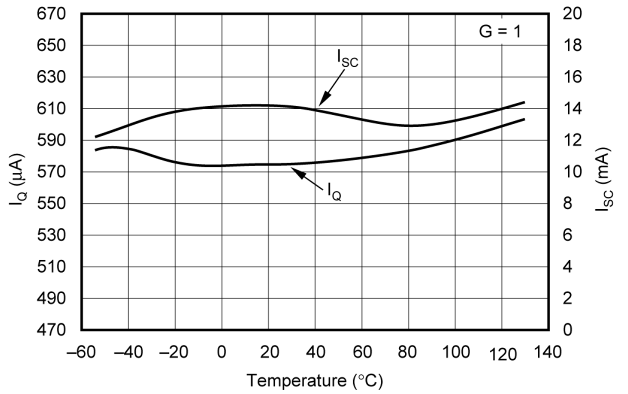


図 5-7. Quiescent Current and Short-circuit Current vs Temperature

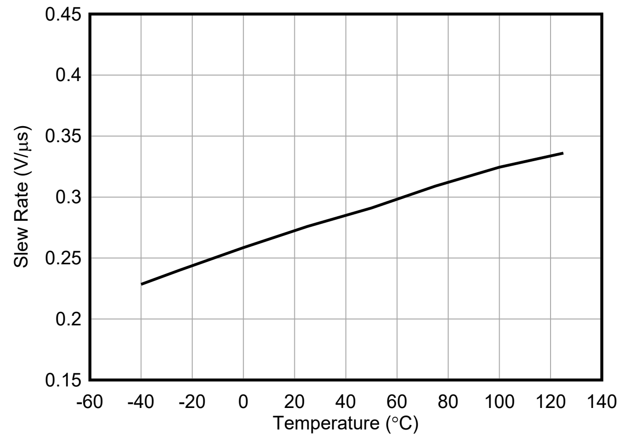


図 5-8. Slew Rate vs Temperature

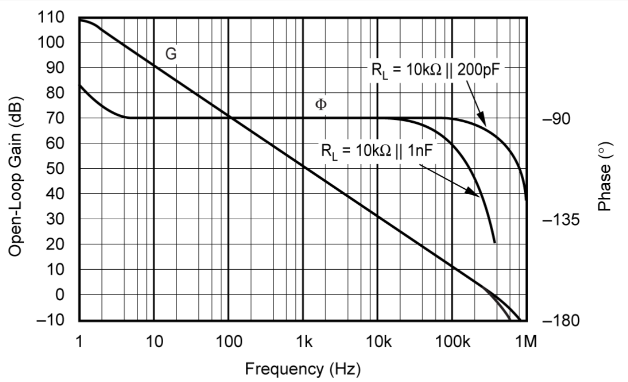


図 5-9. Gain and Phase vs Frequency Op Amp A1 and A2

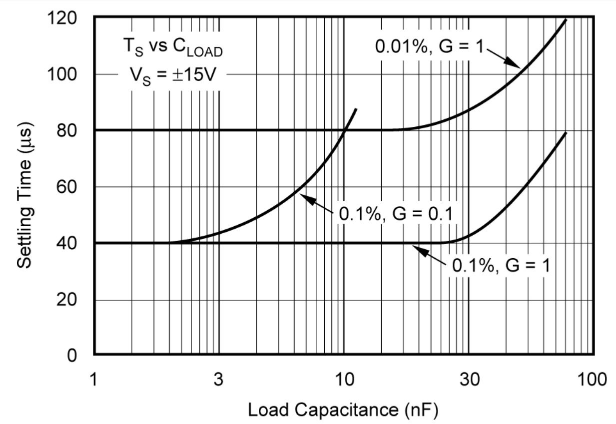


図 5-10. Settling Time vs Load Capacitance

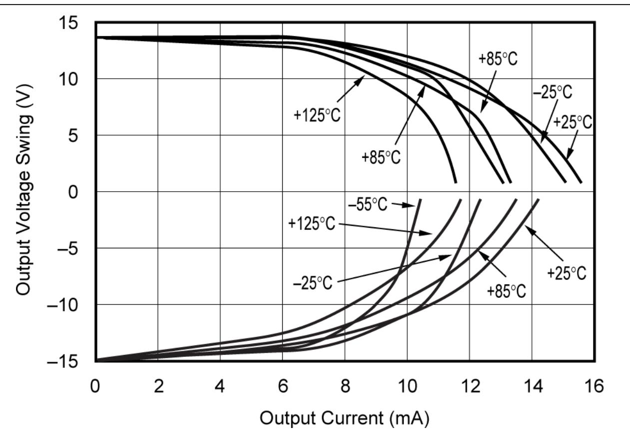


図 5-11. Maximum Output Voltage Swing vs Output Current

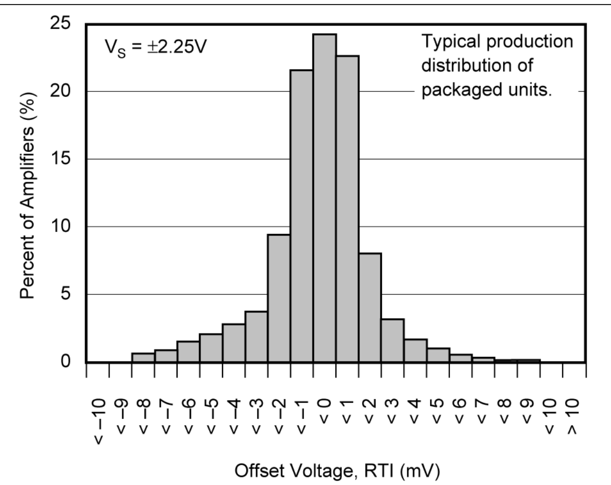


図 5-12. Offset Voltage Production Distribution

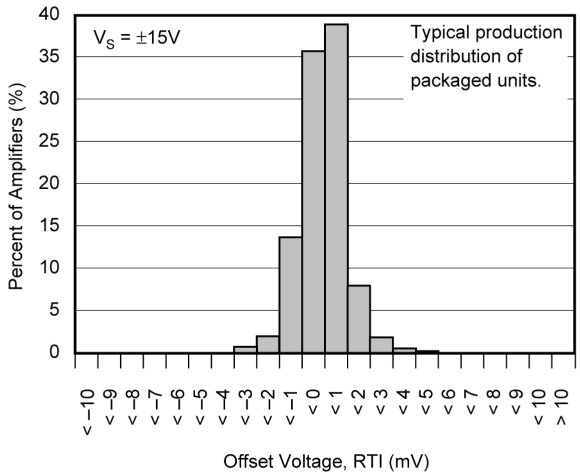


図 5-13. Offset Voltage Production Distribution

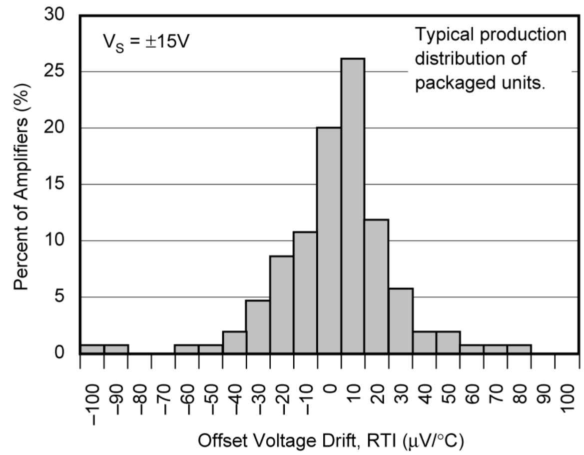


図 5-14. Offset Voltage Drift Production Distribution

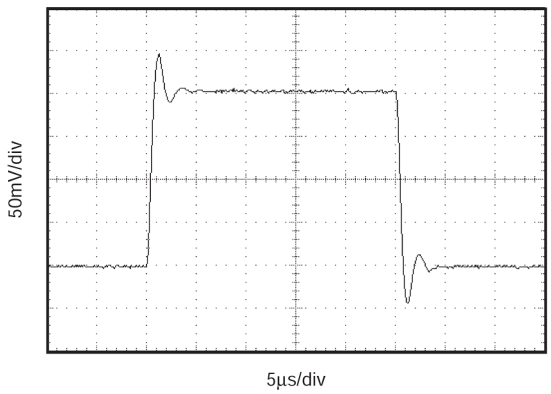


図 5-15. Small-signal Step Response (G = 0.1, R_L = 10 kΩ, C_L = 200 pF)

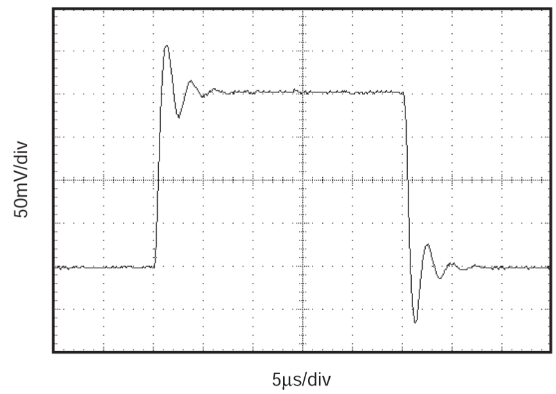


図 5-16. Small-signal Step Response (G = 0.1, C_L = 1000 pF)

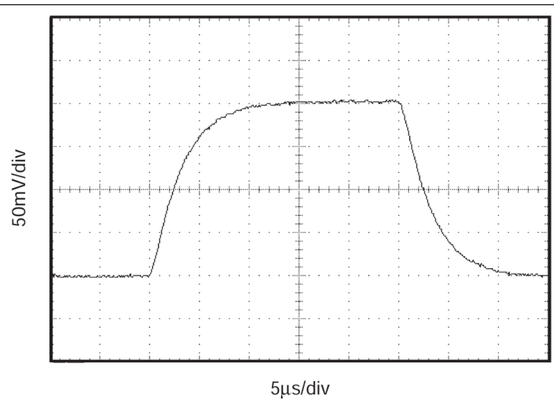


図 5-17. Small-signal Step Response (G = 1, C_L = 1000 pF)

図 5-18. Large-signal Step Response (G = 1, R_L = 10 kΩ, C_L = 200pF)

6 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

6.1 Application Information

The INA146 is a programmable gain difference amplifier consisting of a gain of 0.1 difference amplifier and a programmable-gain output buffer stage. Basic circuit connections are shown in 図 6-1. Power supply bypass capacitors must be connected close to pins 4 and 7, as shown. The amplifier is programmable in the range of G = 0.1 to G = 50 with two external resistors.

The output of A1 is connected to the noninverting input of A2 through a 10-kΩ resistor which is trimmed to ±1% absolute accuracy. The A2 input is available for applications such as a filter or a precision current source. See application figures for examples.

6.1.1 Operating Voltage

The INA146 is fully specified for supply voltages from ±2.25 V to ±18 V with key parameters specified over the temperature range –40°C to 85°C. The INA146 can be operated with single or dual supplies with excellent performance. Parameters that vary significantly with operating voltage, load conditions or temperature are shown in the typical performance curves.

6.1.2 Setting the Gain

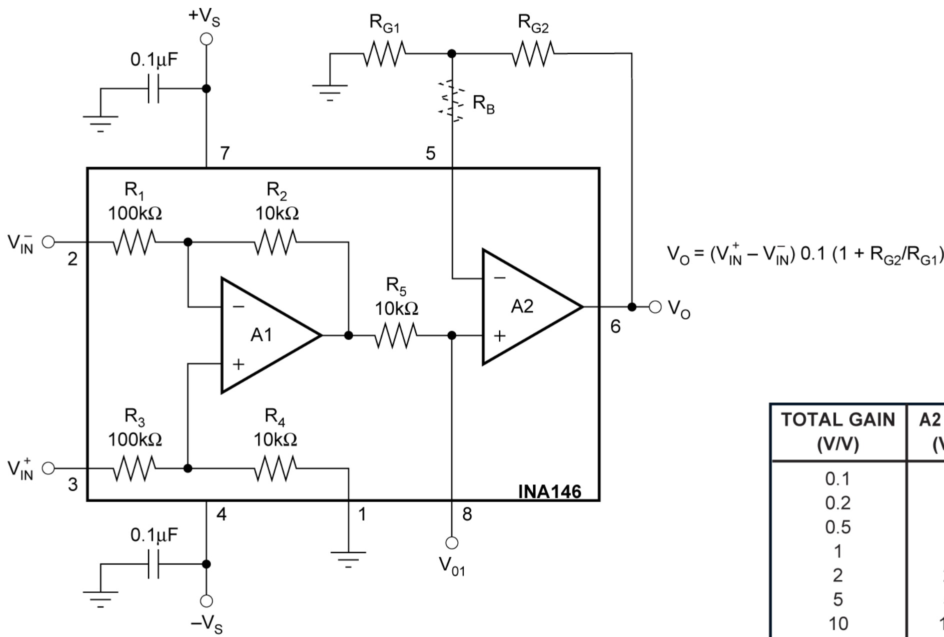
The gain of the INA146 is set by using two external resistors, R_{G1} and R_{G2}, according to the equation:

$$G = 0.1 \times (1 + R_{G2}/R_{G1})$$

For a total gain of 0.1, A2 is connected as a buffer amplifier with no R_{G1}. A feedback resistor, R_{G2} = 10 kΩ, must be used in the buffer connection. This provides bias current cancellation (in combination with internal R_5) to assure specified offset voltage performance. Commonly used values are shown in the table of 図 6-1. Resistor values for other gains must be chosen to provide a 10-kΩ parallel resistance.

6.1.3 Common-mode Range

The 10:1 input resistor ratio of the INA146 provides an input common-mode range that can extend well beyond the power supply rails. Exact range depends on the power supply voltage and the voltage applied to the Ref terminal (pin 1). For proper operation, the voltage at the non-inverting input of A1 (an internal node) must be within the linear operating range. The voltage is determined by the simple 10:1 voltage divider between pin 3 and pin 1. This voltage must be between V– and (V+) – 1 V.



TOTAL GAIN (V/V)	A2 GAIN (V/V)	STANDARD 1% RESISTORS R_{G1} (Ω)	R_{G2} (Ω)	R_B (Ω)
0.1	1	(None)	10k	—
0.2	2	20k	20k	—
0.5	5	12.4k	49.9k	—
1	10	11.0k	100k	—
2	20	10.5k	200k	—
5	50	10.2k	499k	—
10	100	10.2k	1M	—
20	200	499	100k	9.53k
50	500	100	49.9k	10k
100	1000	100	100k	10k

図 6-1. Basic Circuit Connections

6.1.4 Offset Trim

The INA146 is laser-trimmed for low offset voltage and drift. Most applications require no external offset adjustment. 図 6-2 shows an optional circuit for trimming the offset voltage. A voltage applied to the Ref terminal is summed with the output signal. This feature can be used to null offset voltage. To maintain good common-mode rejection, the source impedance of a signal applied to the Ref terminal must be less than 10 Ω and a resistor added to the positive input terminal must be 10 times that, or 100 Ω. Alternatively, the trim voltage can be buffered with an operational amplifier such as the OPA277.

6.1.5 Input Impedance

The input impedance of the INA146 is determined by the input resistor network and is approximately 100 kΩ. The source impedance at the two input terminals must be nearly equal to maintain good common-mode rejection. A 12-Ω mismatch in impedance between the two inputs causes the typical common-mode rejection to be degraded to approximately 72 dB. 図 6-7 shows a common application measuring power supply current through a shunt resistor. The source impedance of the shunt resistor, R_S, is balanced by an equal compensation resistor, R_C.

Source impedances greater than 800 Ω are not recommended, even if the source impedances are perfectly matched. Internal resistors are laser trimmed for accurate ratios, not to absolute values. Adding equal resistors greater than 800 Ω can cause a mismatch in the total resistor ratios, degrading CMR.

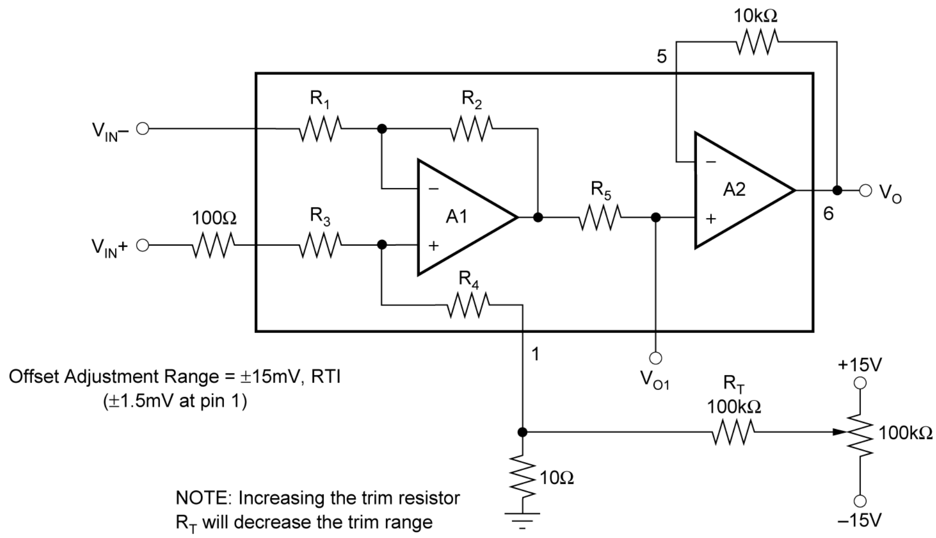
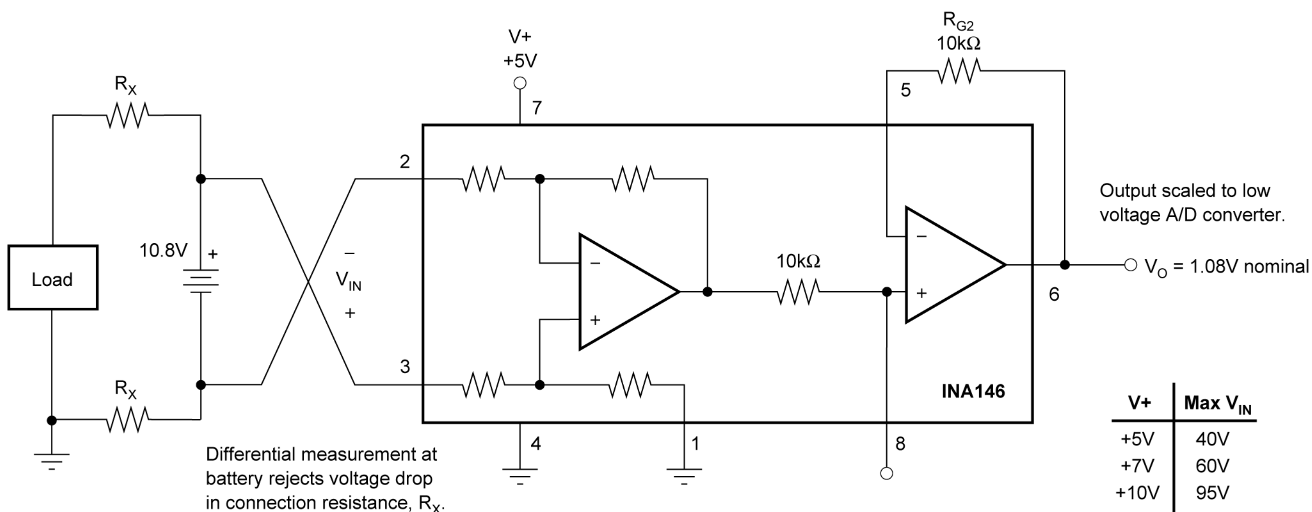


図 6-2. Optional Offset Trim Circuit



V+	Max V_{IN}
+5V	40V
+7V	60V
+10V	95V
≥ 11V	100V

図 6-3. Measuring Voltages Greater Than Supply Voltage

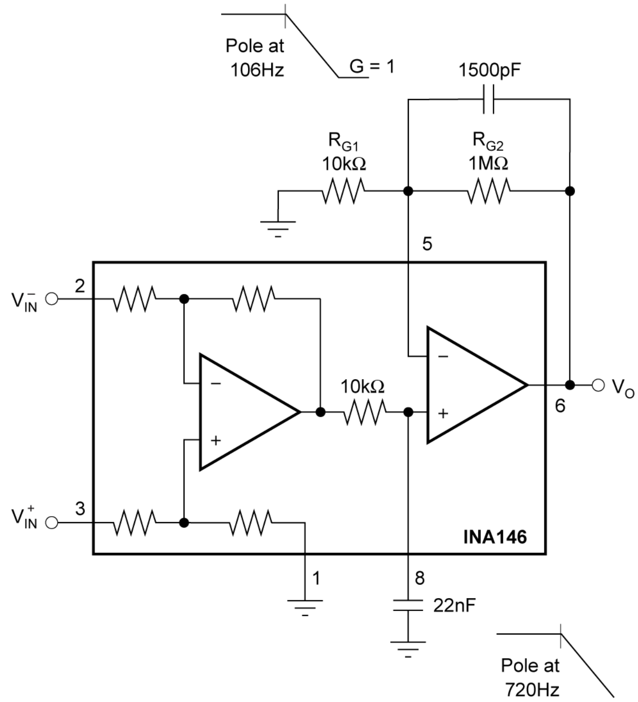


図 6-4. Noise Filtering

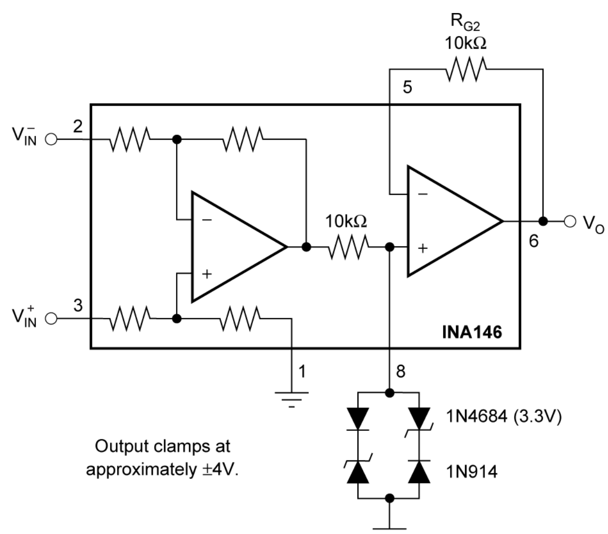


図 6-5. Output Clamp

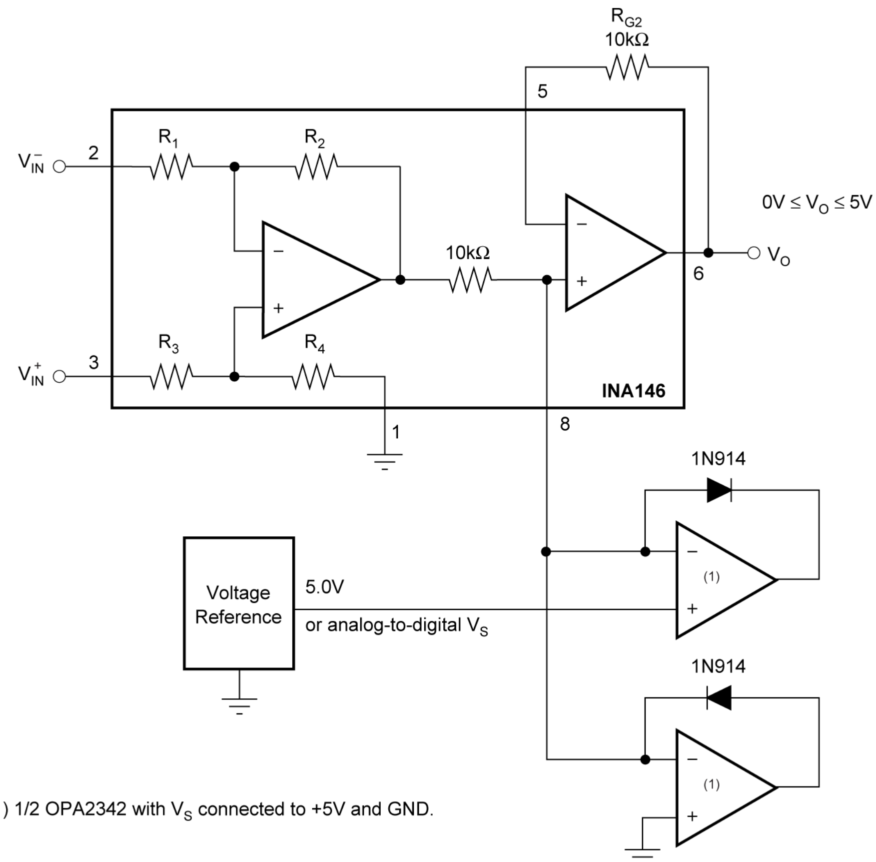


図 6-6. Precision Clamp

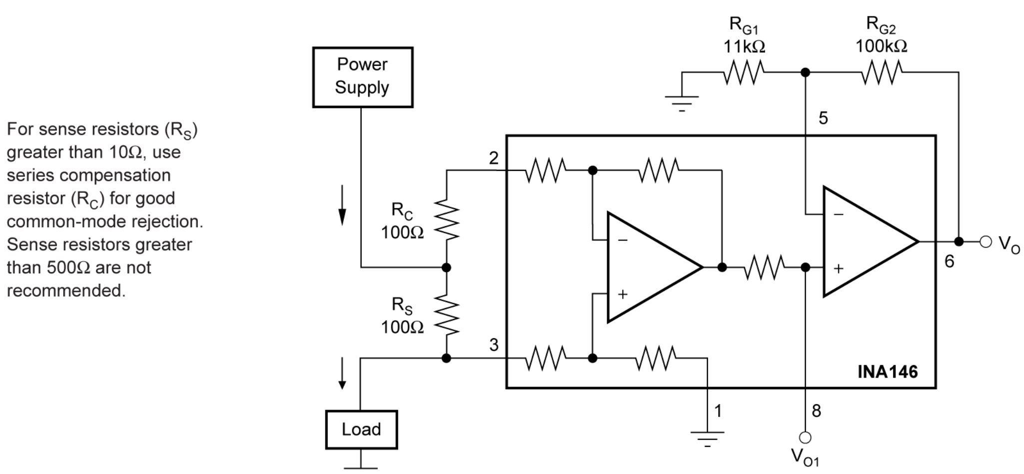


図 6-7. Current Monitor, G = 1

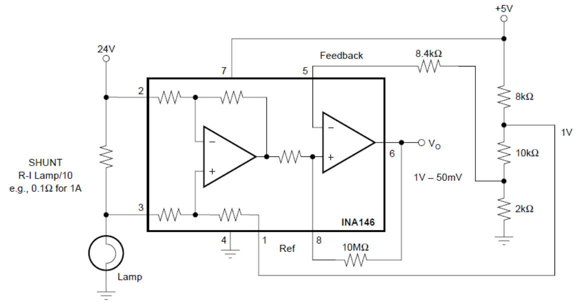


図 6-8. Comparator Output With Optional Hysteresis Application to Sense Lamp Burn-Out

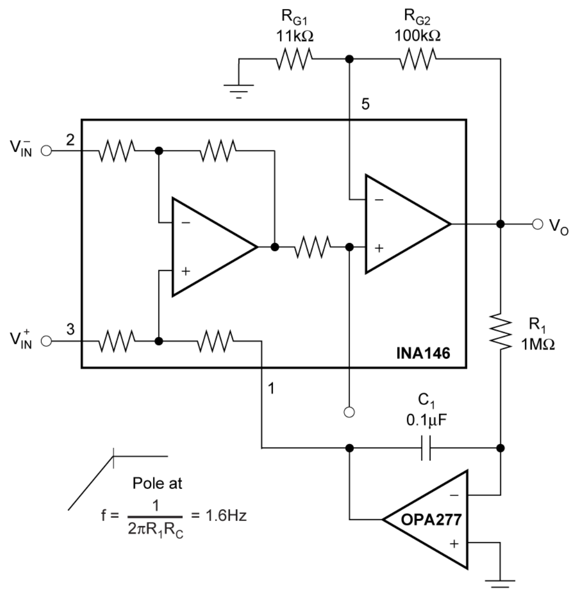


図 6-9. AC Coupling (DC Restoration)

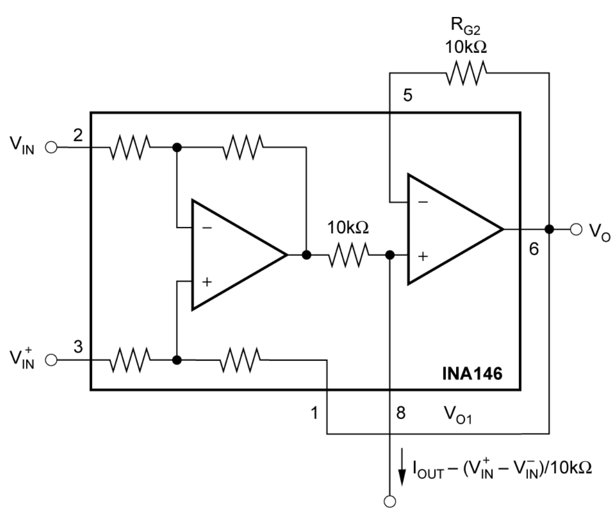


図 6-10. Precision Current Source

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

7.2 Documentation Support

7.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Comprehensive Error Calculation for Instrumentation Amplifiers*, application note
- Texas Instruments, *High-Voltage Signal Conditioning for Low Voltage ADCs*, application note
- Texas Instruments, *Analog Engineer's Calculator,* application

7.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

7.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

7.5 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

7.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

7.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

8 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 1999) to Revision A (October 2023) — Page

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新。 1
- Changed pin 7 from V+ to V_{S+} and pin 4 from V- to V_{S-} 3
- Added VREF = 0 V, VCM = VS / 2 "unless otherwise noted" conditions in *Electrical Characteristics* and *Typical Characteristics* for clarity 5
- Changed from Offset Voltage vs Power Supply to Power-supply rejection ratio for more clarity 5
- Change test condition V_{CM} formula for more clarity 5
- Added test condition "TA = –40°C to 85°C" for "Gain error vs temperature" in *Electrical Characteristics* and renamed to "Gain drift" for clarity 5
- Added test condition "T_A = -40℃ to 85℃" for Output over Temperature in Electrical Characteristics 5
- Added test condition "Continuous to VS / 2" short-circuit current specification in *Electrical Characteristics* for clarity 5
- Deleted redundant voltage range, operating temperature range, and specification temperature range specifications from *Electrical Characteristics* 5
- Added VREF = 0 V, VCM = VS / 2, to "unless otherwise noted" conditions in *Electrical Characteristics* and *Typical Characteristics* for clarity 6
- Changed from Offset Voltage vs Power Supply to Power-supply rejection ratio for more clarity 6
- Added test condition "TA = –40°C to 85°C" for "Gain error vs temperature" in *Electrical Characteristics* and renamed to "Gain drift" for clarity 6
- Added test condition "TA = –40°C to 85°C" to "Output voltage" in Electrical Characteristics 6
- Added test condition "Continuous to VS / 2" short-circuit current specification in *Electrical Characteristics* for clarity 6
- Deleted redundant voltage range, operating temperature range, and specification temperature range specifications from *Electrical Characteristics* 6
- Added V_{REF} = 0 V, V_{CM} = V_S / 2 to "unless otherwise noted" conditions in *Electrical Characteristics* and *Typical Characteristics* for clarity 7

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA146UA	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	INA 146UA
INA146UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 146UA
INA146UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 146UA
INA146UAE4	NRND	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

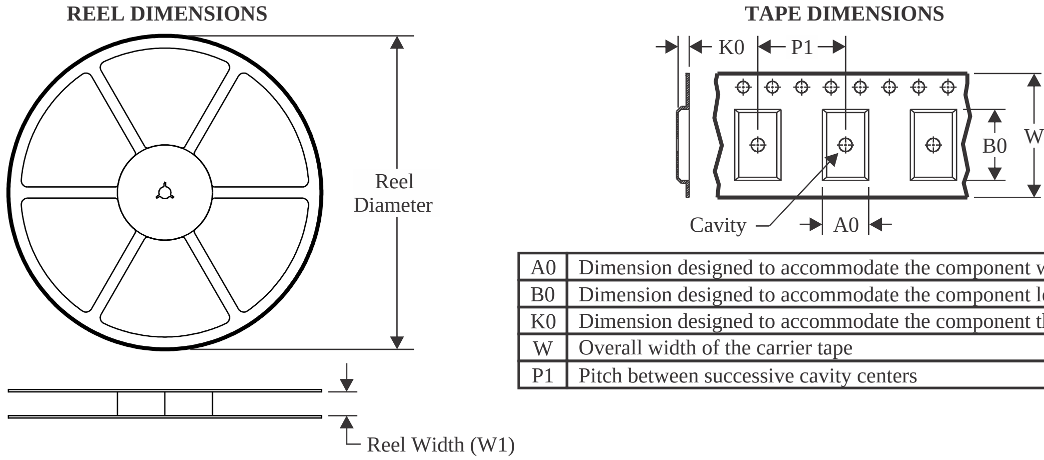
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

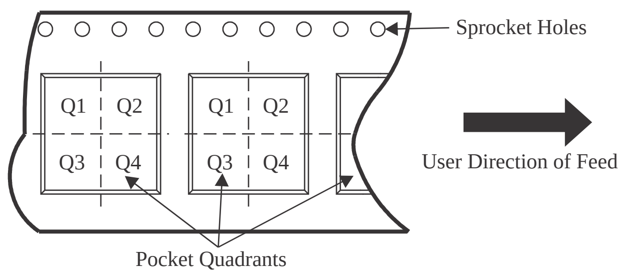
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



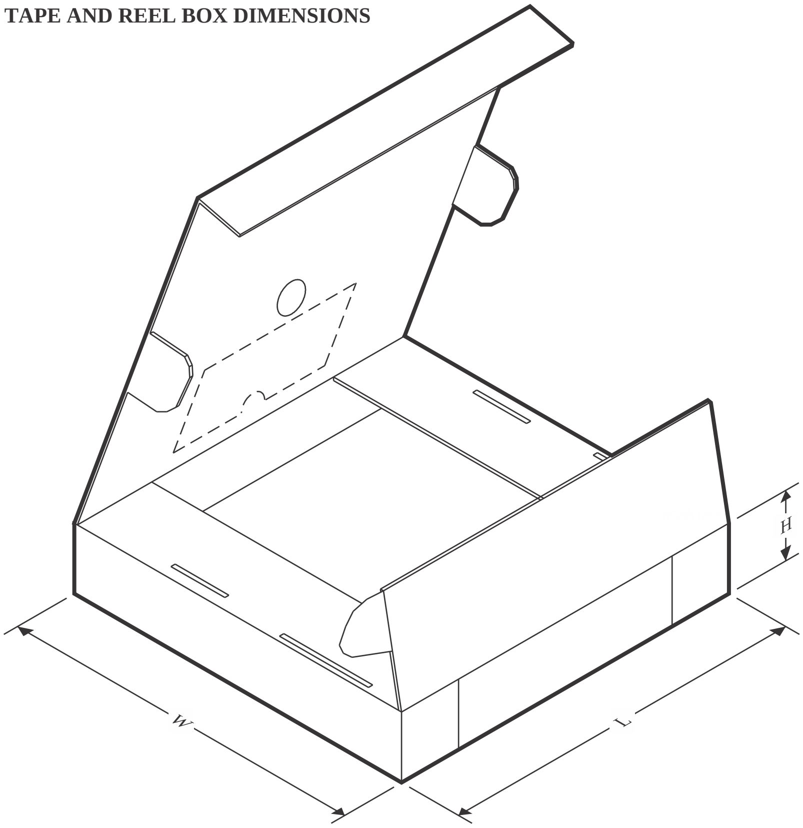
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA146UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA146UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265