INA141 高精度、低消費電力、G = 10V/V または 100V/V、計測アンプ

1 特長

- 低いオフセット電圧:
  - G = 100V/V で最大 50μV
- 低いドリフト:
  - G = 100V/V で最大 0.5μV/℃
- 高精度のゲイン:
  - G = 10V/V で ±0.05%
- 低い入力バイアス電流:
  - 5nA (最大値)
- 高い CMR:
  - 117dB (最小値)
- ±40V までの入力保護
- 広い電源電圧範囲:±2.25V～±18V
- 低い静止電流:750μA

2 アプリケーション

- 温度トランスミッタ
- 医療用計測機器
- データ・アクイジション (DAQ)
- プロセス分析 (pH、ガス、濃度、力、湿度)

3 概要

INA141 は、精度の優れた低消費電力の汎用計測アンプです。本デバイスは、用途が広い 3 オペアンプ設計を採用しており、サイズが小型であるため、広範なアプリケーションに非常に適しています。電流帰還入力回路により、高いゲインでも広い帯域幅が得られます (G = 100V/V で 200kHz)。

シンプルなピン接続により、外付け抵抗なしで 10V/V または 100V/V の高精度ゲインを設定できます。内部入力保護機能は、損傷なしに ±40V まで耐えられます。

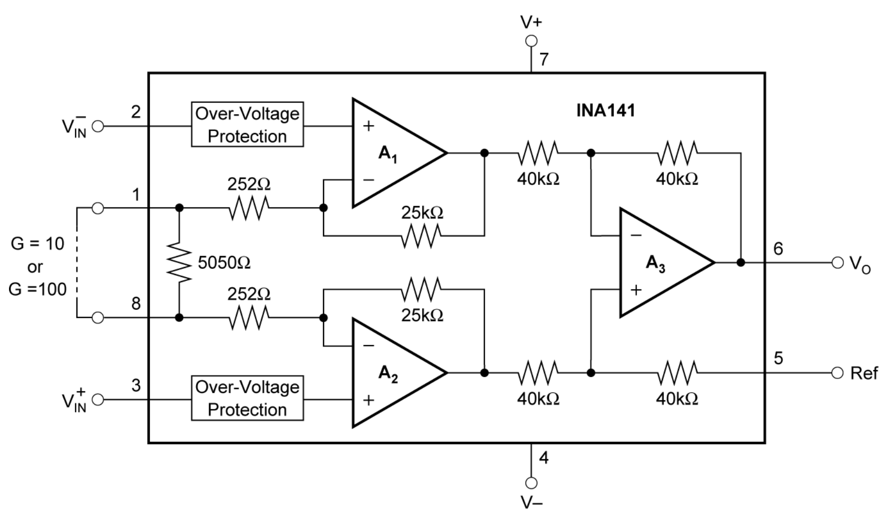
INA141 はレーザー・トリムにより、非常に低いオフセット電圧 (50μV) とドリフト係数 (0.5μV/℃)、高い同相除去 (G = 100V/V で 117dB) を実現しています。このデバイスは最低 ±2.25V の電源で動作し、静止電流はわずか 750μA です。

INA141 は 8 ピン SOIC パッケージで供給され、-40℃～+85℃の温度範囲で動作が規定されています。

パッケージ情報

部品番号	パッケージ(1)	パッケージ・サイズ (2)
INA141	D (SOIC、8)	4.9mm × 6mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



基本的な接続

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2000) to Revision A (August 2023) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- 「パッケージ情報」表、「ピン構成および機能」セクション、「仕様」セクション、「ESD 定格」セクション、「推奨動作条件」セクション、「熱に関する情報」セクション、「アプリケーションと実装」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 1
- データシートから PDIP パッケージを削除 1
- Added single supply specification to Absolute Maximum Ratings 5
- Added note that output short-circuit (to ground) means short-circuit to $V_S/2$ in Absolute Maximum Ratings 5
- Added "TA = –40°C to +85°C" test condition to Offset voltage vs temperature specification in the Electrical Characteristics and renamed to Offset voltage drift 6
- Added test conditions "VREF = 0 V, VCM = VS / 2 and G = 10 below the title 6
- Deleted common-mode voltage typical values in the Electrical Characteristics and combined to one line 6
- Added "TA = –40°C to +85°C" test condition to Bias current vs temperature specification in the Electrical Characteristics and renamed to Input bias current drift for clarity 6
- Added "TA = –40°C to +85°C" test condition to Offset current vs temperature specification in Electrical Characteristics and renamed to Input offset current drift for clarity 6
- Added "TA = –40°C to +85°C" test condition for Gain error vs temperature in the Electrical Characteristics and renamed to Gain drift for clarity 6
- Changed parameter names from "Voltage - Positive" and "Voltage - Negative" to "Output voltage" in the Electrical Characteristics 6
- Added "Continuous to VS / 2" test condition short-circuit current specification in the Electrical Characteristics for clarity 6
- Changed short-circuit current typical value from +6/-15 mA ±20 mA 6
- Changed bandwidth typical value from 1 MHz to 610 kHz in the Electrical Characteristics 6
- Changed slew rate typical value from 4 V/μs to 2 V/μs in the Electrical Characteristics 6
- Deleted redundant voltage range, operating temperature range, and specification temperature range specifications from Electrical Characteristics 6
- Changed Figure 6-2, *Common-Mode Rejection vs Frequency* 8
- Changed Figure 6-8, *Quiescent Current and Slew Rate vs Temperature* 8
- Changed *Output Voltage Swing vs Output Current* single plot to Figure 6-12, *Positive Output Voltage Swing vs Output Current* and Figure 6-12, *Negative Output Voltage Swing vs Output Current* 8
- Changed Figure 6-18, *Small-Signal Step Response* 8
- Changed Figure 6-19, *Large-Signal Step Response* 8
- Changed Figure 6-20, *0.1-Hz to 10-Hz Input-Referred Voltage Noise* 8
- Changed G from 1 to 10 V/V at the end of the *Application Information* section 12

- Deleted reference to *Input BIas Current vs Common-Mode Input Voltage* plot..14

5 Pin Configuration and Functions

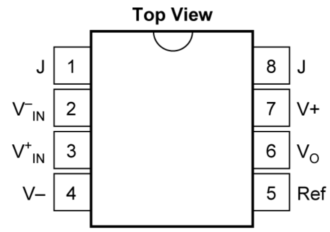


図 5-1. D Package, 8-Pin SOIC (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
J	1, 8	Input	Gain selection. G = 10 V/V if not shorted G = 100 V/V if shorted A resistance of 0.5 Ω decreases gain by 0.1%.
Ref	5	Input	Reference input. This pin must be driven by low impedance
V–	4	—	Negative supply
V+	7	—	Positive supply
V^{-}_{IN}	2	Input	Negative (inverting) input
V^{+}_{IN}	3	Input	Positive (noninverting) input
V_O	6	Output	Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_S	Supply voltage	Dual supply, V_S = (V+) – (V–)		±18	V
		Single supply, V_S = (V+) – 0 V		36	
	Input voltage			±40	V
	Output short-circuit (to ground)[2]		Continuous		
T_A	Operating temperature		–40	125	°C
T_{stg}	Storage temperature		–40	125	°C
T_J	Junction temperature			150	°C
	Lead temperature (soldering, 10 s)			300	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_S / 2.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_S	Supply voltage	Single-supply	4.5	30	36	V
		Dual-supply	±2.25	±15	±18	
T_A	Specified temperature		–40		85	°C

6.4 Thermal Information

THERMAL METRIC[1]		INA141	UNIT
		D (SOIC)	
		8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	150	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 10 V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
INPUT								
V_{OS}	Offset voltage (RTI)	INA141P, INA141U	G = 10 V/V			±50	±100	µV
			G = 100 V/V			±20	±50	
		INA141PA, INA141UA	G = 10 V/V			±50	±250	
			G = 100 V/V			±20	±125	
	Offset voltage drift (RTI)	T_A = –40°C to +85°C	INA141P, INA141U	G = 10 V/V		±0.5	±2	µV/°C
				G = 100 V/V		±0.2	±0.5	
			INA141PA, INA141UA	G = 10 V/V		±0.5	±2.5	
				G = 100 V/V		±0.2	±1.5	
PSRR	Power-supply rejection ratio (RTI)	V_S = ±2.25 V to ±18 V	INA141P, INA141U	G = 10 V/V		±2	±10	µV/V
				G = 100 V/V		±0.4	±1	
			INA141PA, INA141UA	G = 10 V/V		±2	±20	
				G = 100 V/V		±0.4	±3	
	Long-term stability	G = 10 V/V				0.5		µV/mo
		G = 100 V/V				0.2		µV/mo
	Input impedance	Differential				100 || 2		GΩ || pF
		Common-mode				100 || 9		
V_{CM}	Common-mode voltage[(1)]	V_O = 0 V			(V–) +2		(V+) – 2	V
CMRR	Common-mode rejection	V_{CM} = ±13 V, ΔR_S = 1 kΩ	INA141P, INA141U	G = 10 V/V	100	106		dB
				G = 100 V/V	117	125		
			INA141PA, INA141UA	G = 10 V/V	93	100		
				G = 100 V/V	110	120		
INPUT BIAS CURRENT								
I_B	Input bias current	INA141P, INA141U				±2	±5	nA
		INA141PA, INA141UA				±2	±10	
	Input bias current drift	T_A = –40°C to +85°C				±30		pA/°C
I_{OS}	Input offset current	INA141P, INA141U				±1	±5	nA
		INA141PA, INA141UA				±1	±10	nA
	Input offset current drift	T_A = –40°C to +85°C				±30		pA/°C
NOISE								
e_N	Voltage noise (RTI)	R_S = 0 Ω	G = 10 V/V	f = 10 Hz		22		nV/√Hz
				f = 100 Hz		13		
				f = 1 kHz		12		
				f_B = 0.1 Hz to 10 Hz		0.6		μV_{PP}
			G = 100 V/V	f = 10 Hz		10		nV/√Hz
				f = 100 Hz		8		
				f = 1 kHz		8		
				f_B = 0.1 Hz to 10 Hz		0.2		μV_{PP}
I_n	Current noise	f = 10 Hz				0.9		pA/√Hz
		f = 1 kHz				0.3		
		f_B = 0.1 Hz to 10 Hz				30		pA_{PP}

6.5 Electrical Characteristics (続き)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 10 V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
GAIN								
G	Gain				10		100	V/V
GE	Gain error	V_O = ±13.6 V	INA141P, INA141U	G = 10 V/V		±0.01	±0.05	%
				G = 100 V/V		±0.03	±0.075	
			INA141PA, INA141UA	G = 10 V/V		±0.01	±0.15	
				G = 100 V/V		±0.03	±0.15	
	Gain drift(6)	G = 10 V/V or 100 V/V, T_A = –40°C to +85°C				±2	±10	ppm/°C
	Gain nonlinearity	INA141P, INA141U	G = 10 V/V			±0.0003	±0.001	% of FSR
			G = 100 V/V			±0.0005	±0.002	
		INA141PA, INA141UA	G = 10 V/V			±0.0003	±0.002	
			G = 100 V/V			±0.0005	±0.004	
OUTPUT								
	Output voltage				(V–) + 1.4	(V±) ∓ 0.9	(V+) – 1.4	V
C_L	Load capacitance	Stable operation				1000		pF
I_{SC}	Short-circuit current	Continuous to V_S / 2				±20		mA
FREQUENCY RESPONSE								
BW	Bandwidth, –3 dB	G = 10 V/V				610		kHz
		G = 100 V/V				200		kHz
SR	Slew rate	G = 10 V/V, V_O = ±10 V				2		V/µs
t_S	Settling time	To 0.01%, V_O = ±5 V	G = 10 V/V			7		µs
			G = 100 V/V			9		
	Overload recovery	50% input overload				4		µs
POWER SUPPLY								
I_Q	Quiescent current	V_{IN} = 0 V				±750	±800	µA

(1) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.
(2) Specified by wafer test.

6.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, V_{REF} = 0 V, G = 10 V/V, VCM = V_S / 2, and R_L = 10 kΩ (unless otherwise noted)

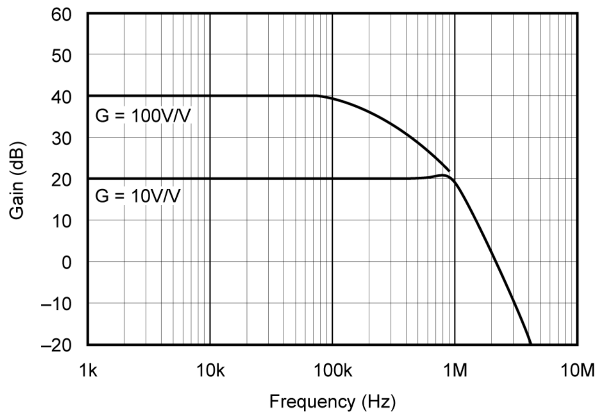


図 6-1. Gain vs Frequency

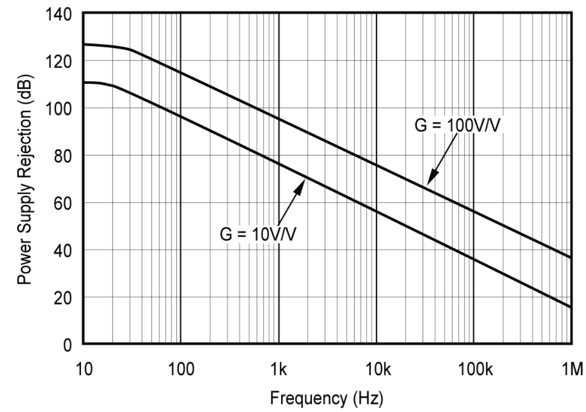


図 6-2. Common-Mode Rejection vs Frequency

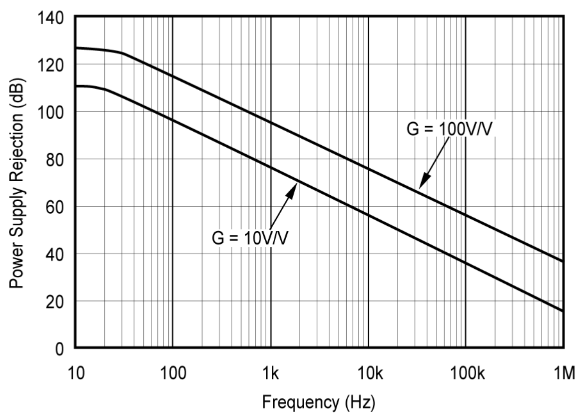


図 6-3. Positive Power Supply Rejection vs Frequency

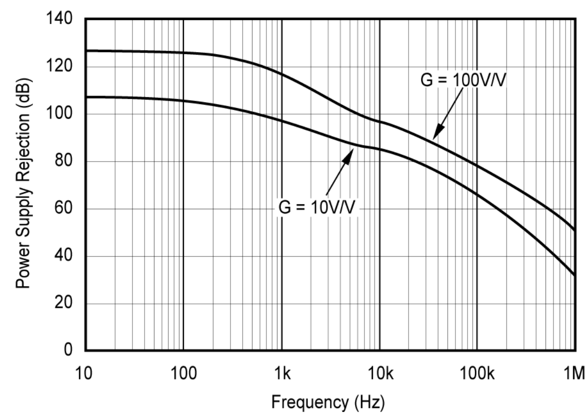


図 6-4. Negative Power Supply Rejection vs Frequency

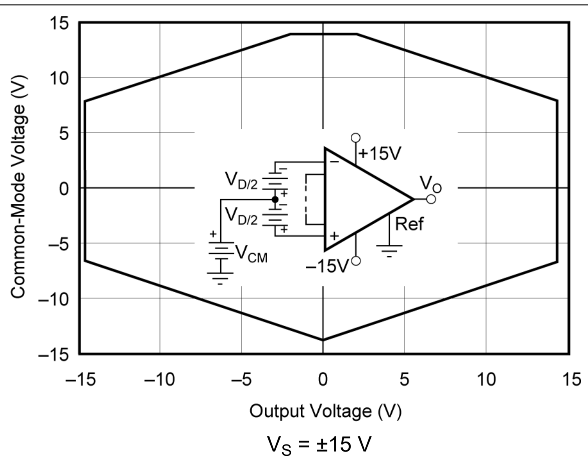


図 6-5. Input Common-Mode Range vs Output Voltage

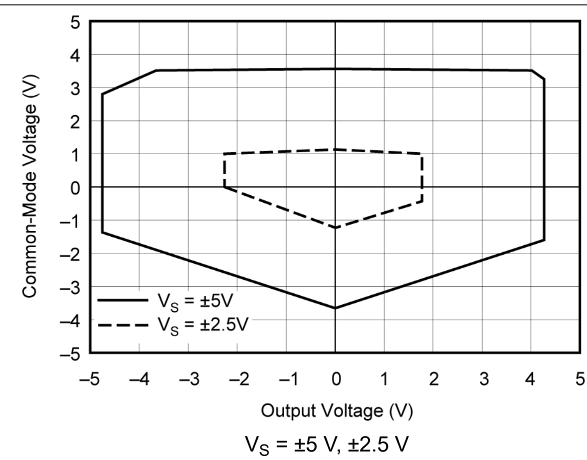


図 6-6. Input Common-Mode Range vs Output Voltage

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{REF} = 0 V, G = 10 V/V, VCM = V_S / 2, and R_L = 10 kΩ (unless otherwise noted)

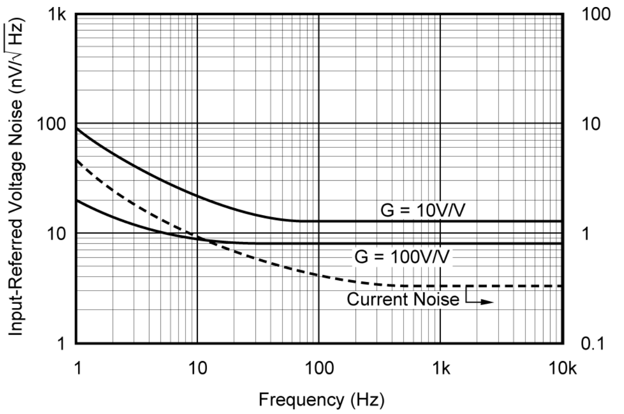


図 6-7. Input-Referred Noise vs Frequency

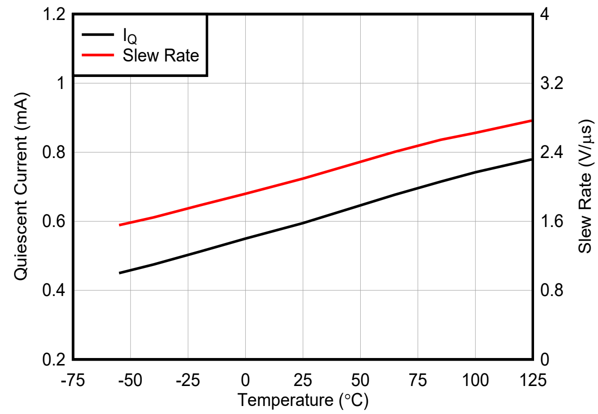


図 6-8. Quiescent Current and Slew Rate vs Temperature

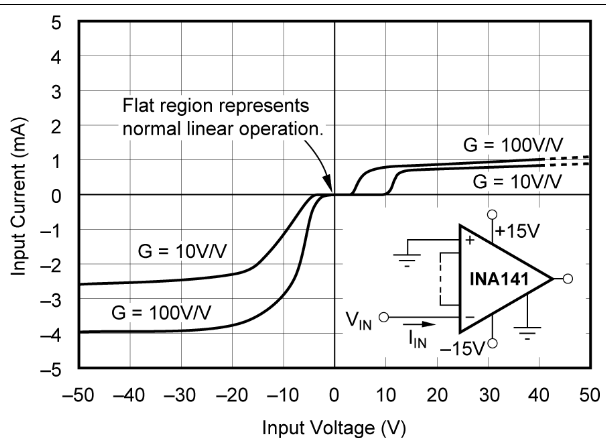


図 6-9. Input Overvoltage V/I Characteristics

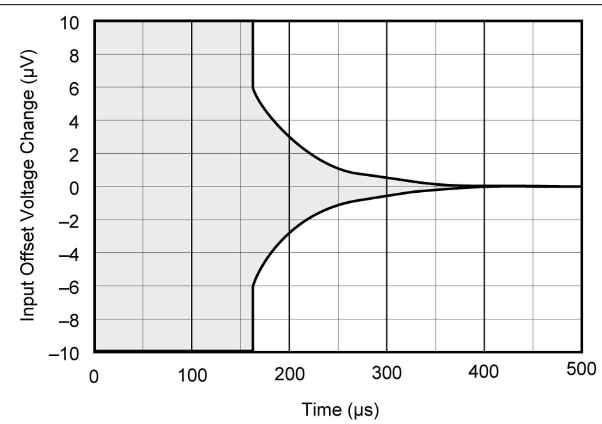


図 6-10. Input Offset Voltage Warmup

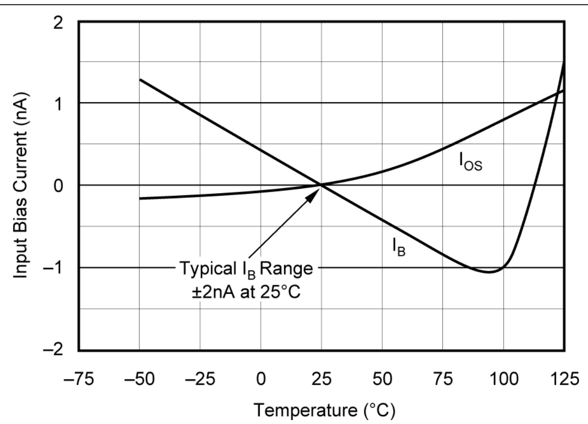


図 6-11. Input Bias Current vs Temperature

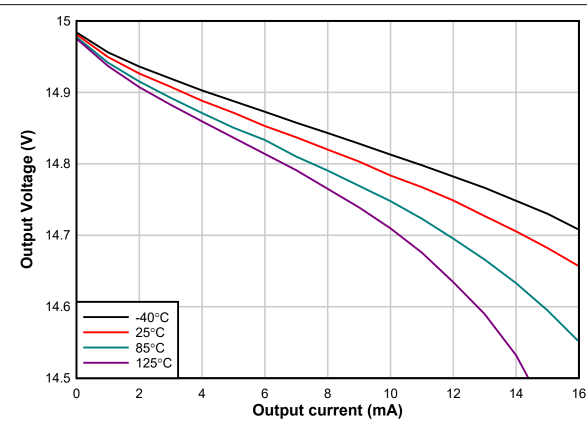


図 6-12. Positive Output Voltage Swing vs Output Current

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{REF} = 0 V, G = 10 V/V, VCM = V_S / 2, and R_L = 10 kΩ (unless otherwise noted)

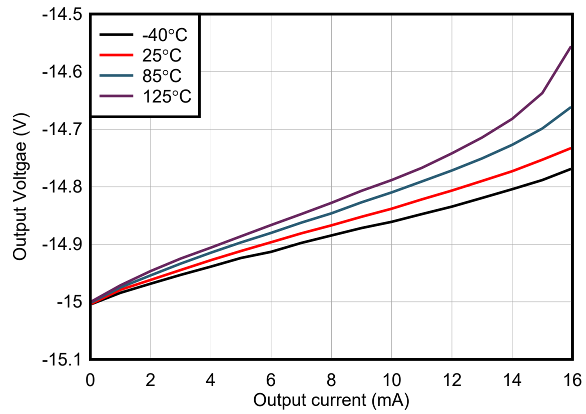


図 6-13. Negative Output Voltage Swing vs Output Current

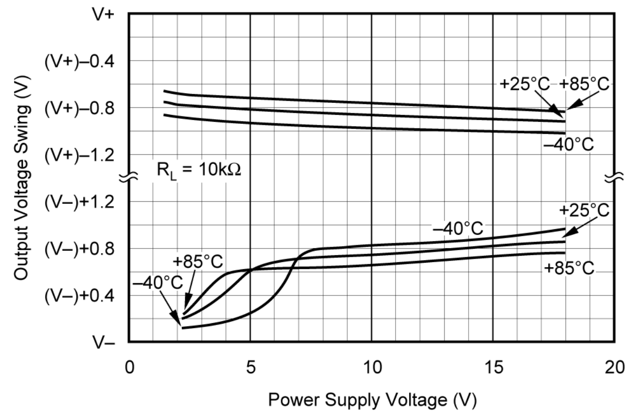


図 6-14. Output Voltage Swing vs Power Supply Voltage

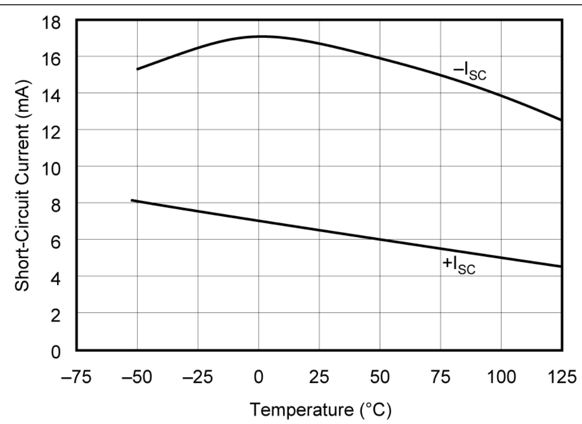


図 6-15. Short-circuit Output Current vs Temperature

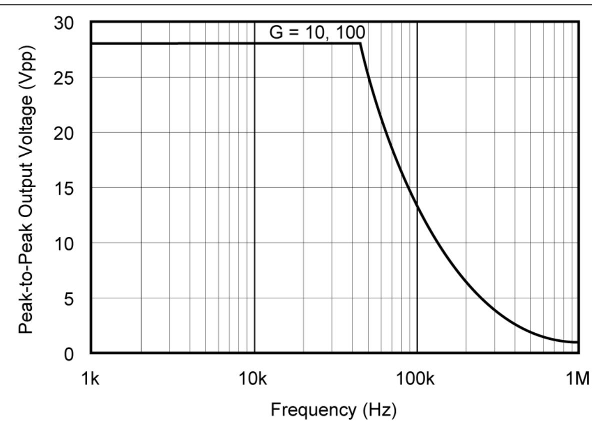


図 6-16. Maximum Output Voltage vs Frequency

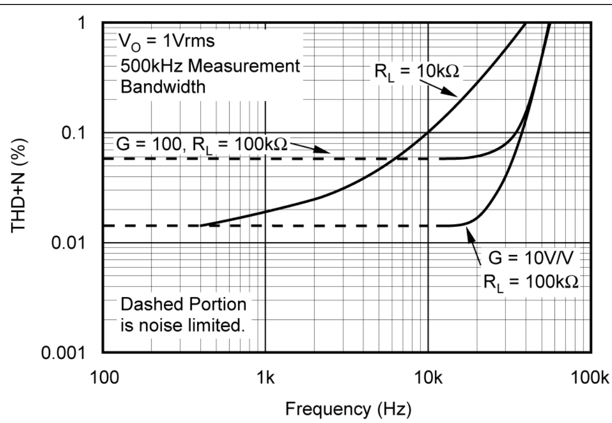


図 6-17. Total Harmonic Distortion + Noise vs Frequency

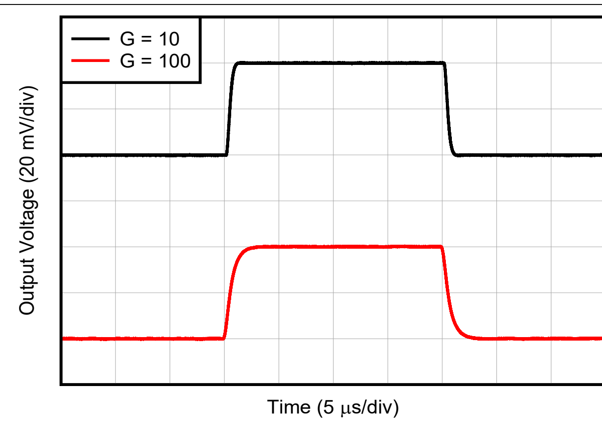


図 6-18. Small-Signal Step Response

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{REF} = 0 V, G = 10 V/V, VCM = V_S / 2, and R_L = 10 kΩ (unless otherwise noted)

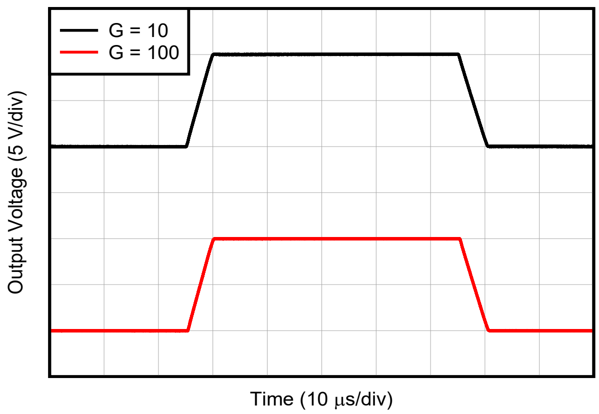


図 6-19. Large-Signal Step Response

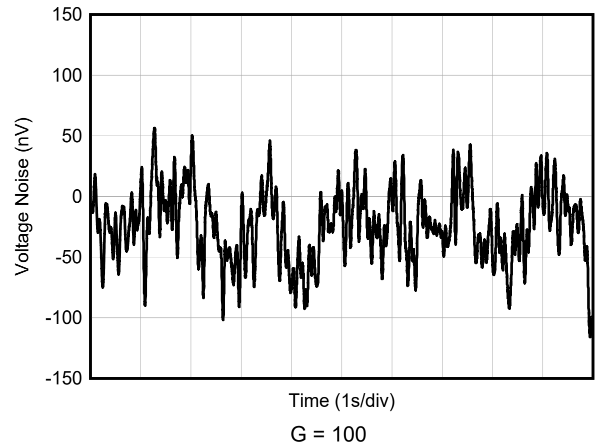


図 6-20. 0.1-Hz to 10-Hz Input-Referred Voltage Noise

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

図 7-1 shows the basic connections required for operation of the INA141. Applications with noisy or high impedance power supplies can require decoupling capacitors close to the device pins as shown.

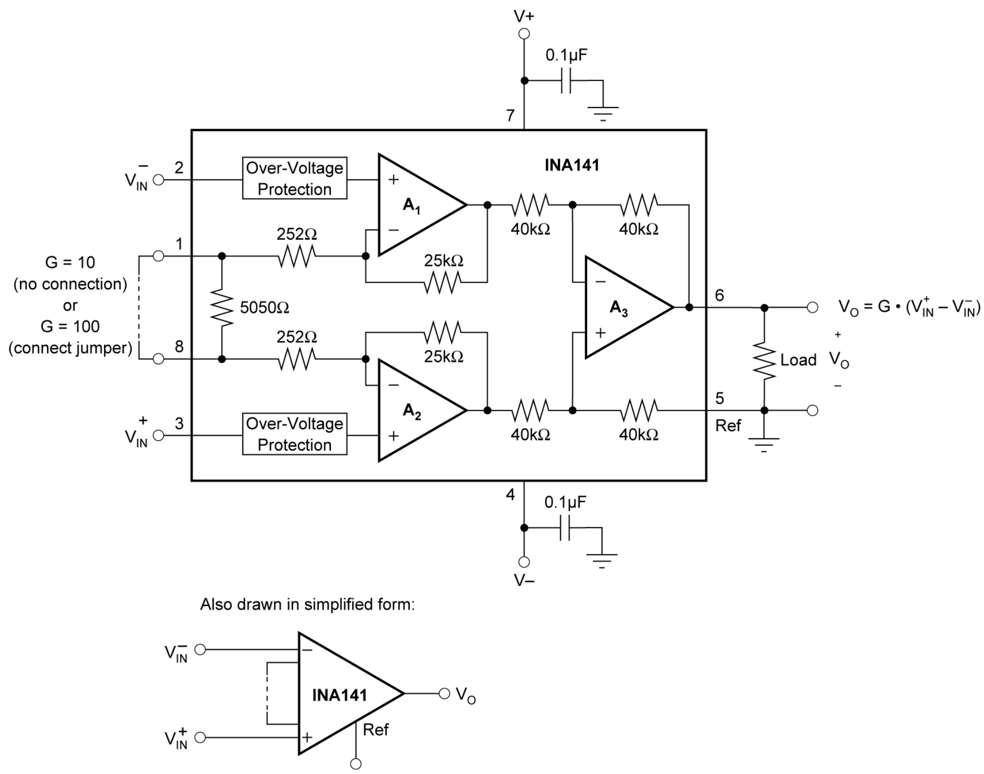


図 7-1. Basic Connections.

The output is referred to the output reference (Ref) pin, which is normally grounded. This connection must be low-impedance to maintain good common-mode rejection. A resistance of 8 Ω in series with the Ref pin causes a typical device to degrade to approximately 80 dB CMR (G = 10 V/V).

7.1.1 Setting the Gain

Gain is selected with a jumper connection (see 図 7-1). With no jumper installed, G = 10 V/V. With a jumper installed, G = 100 V/V. To preserve good gain accuracy, this jumper must have low series resistance. A resistance of 0.5 Ω in series with the jumper decreases the gain by 0.1%.

Internal resistor ratios are laser trimmed to provide excellent gain accuracy. Actual resistor values can vary by approximately ±25% from the nominal values shown.

Gains between 10 V/V and 100 V/V are achieved by connecting an external resistor to the jumper pins. However, this configuration is not recommended because the ±25% variation of internal resistor values makes the required external resistor value uncertain. A companion model, the INA128, features accurately trimmed internal resistors so that gains from 1 V/V to 10,000 V/V can be set with an external resistor.

7.1.2 Dynamic Performance

Typical performance curve *Gain vs Frequency* (図 6-1) shows that, despite the low quiescent current, the INA141 achieves wide bandwidth, even at G = 100 V/V. This wide bandwidth is a result of the current-feedback topology of the INA141. Settling time also remains excellent at G = 100 V/V.

7.1.3 Noise Performance

The INA141 provides very low noise in most applications. Low-frequency noise is approximately 0.2 μV_{PP} measured from 0.1 Hz to 10 Hz (G = 100 V/V). The INA141 provides dramatically improved noise when compared to state-of-the-art, chopper-stabilized amplifiers.

7.1.4 Offset Trimming

The INA141 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. 図 7-2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref pin is summed with the output. The op-amp buffer provides low impedance at the Ref pin to preserve good common-mode rejection.

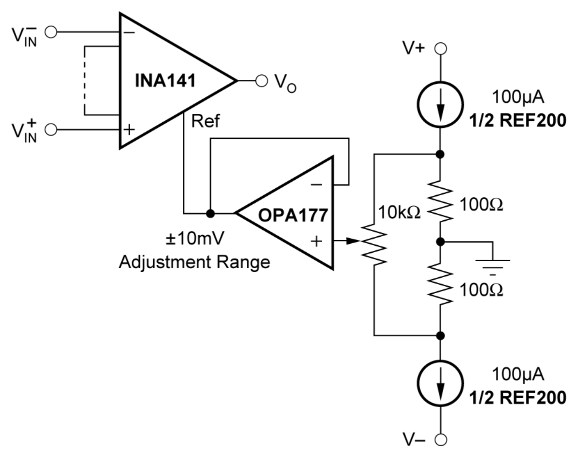


図 7-2. Optional Trimming of Output Offset Voltage.

7.1.5 Input Bias Current Return Path

The input impedance of the INA141 is extremely high—approximately 10^{10} Ω. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±2 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. 図 7-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA141 and the input amplifiers saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in 図 7-3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

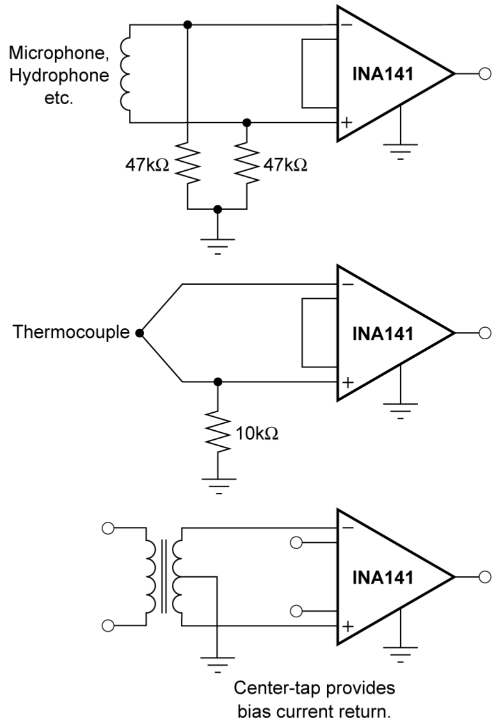


図 7-3. Providing an Input Common-Mode Current Path.

7.1.6 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA141 is from approximately 1.4 V less than the positive supply voltage to 1.7 V greater than the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2. Therefore, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage (see the *Input Common-Mode Range vs Output Voltage* plots, 図 6-5 and 図 6-6.

Input overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA141 is near 0 V even though both inputs are overloaded.

7.1.7 Low-Voltage Operation

The INA141 operates on power supplies as low as ±2.25V. Performance remains excellent with power supplies ranging from ±2.25 V to ±18 V. Most parameters vary only slightly through this supply voltage range—see Typical Performance Curves. Operation at a very low supply voltage requires careful attention to make sure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. The *Input Common-Mode Range vs Output Voltage* typical characteristics plots, 図 6-5 and 図 6-6, show the range of linear operation for ±15-V, ±5-V, and ±2.5-V supplies.

7.1.8 Input Protection

The inputs of the INA141 are individually protected for voltages up to ±40 V. For example, a condition of –40 V on one input and +40 V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors contributes excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.50 mA to 5 mA. The inputs are protected even if the power supplies are disconnected or turned off.

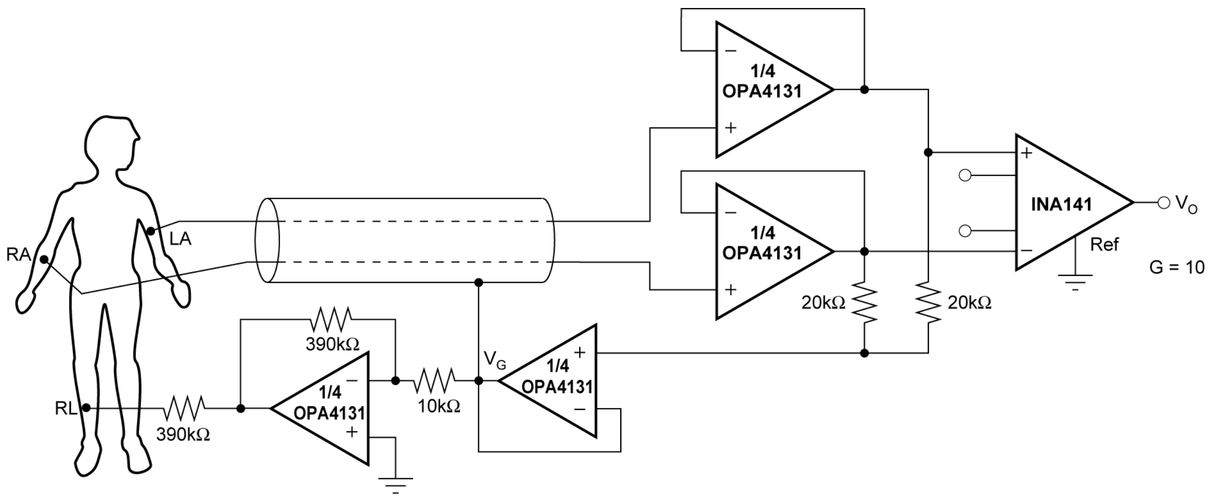


図 7-4. ECG Amplifier With Right-Leg Drive

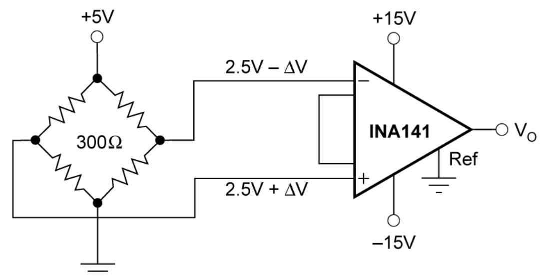


図 7-5. Bridge Amplifier

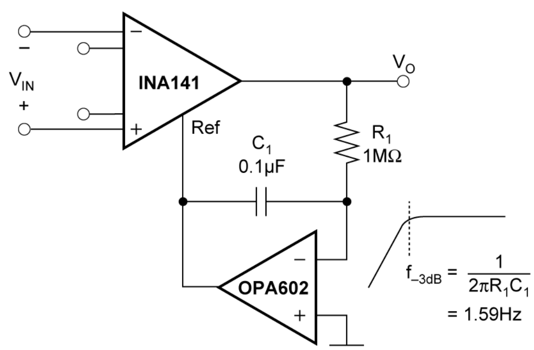
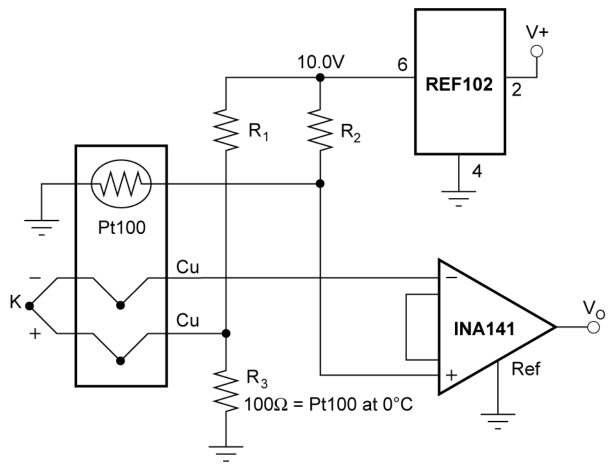
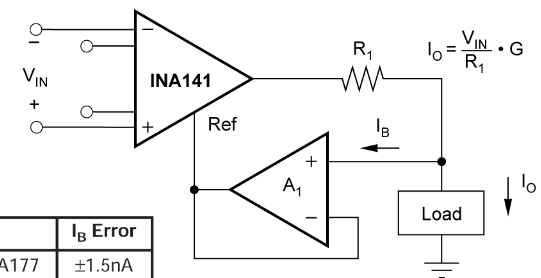


図 7-6. AC-Coupled Instrumentation Amplifier



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (μV/°C)	R_1, R_2
E	+ Chromel – Constantan	58.5	66.5kΩ
J	+ Iron – Constantan	50.2	76.8kΩ
K	+ Chromel – Alumel	39.4	97.6kΩ
T	+ Copper – Constantan	38.0	102kΩ

図 7-7. Thermocouple Amplifier With RTD Cold-Junction Compensation



A_1	I_B Error
OPA177	±1.5nA
OPA131	50pA
OPA602	±1pA
OPA128	±75fA

図 7-8. Differential Voltage-to-Current Converter

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 ドキュメントの更新通知を受け取る方法

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8.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA141U	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-	INA 141U
INA141U.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 141U
INA141U/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-	INA 141U
INA141U/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 141U
INA141UA	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 85	INA 141U A
INA141UA.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 141U A
INA141UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 85	INA 141U A
INA141UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 141U A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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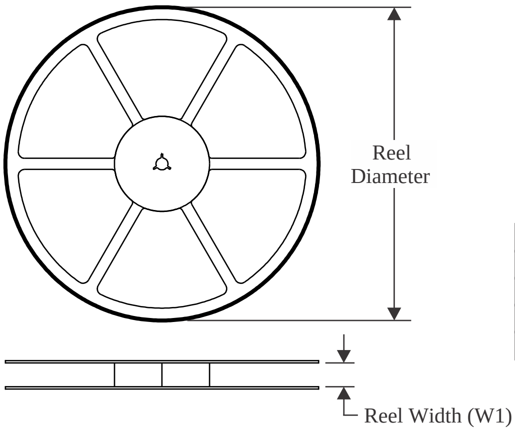
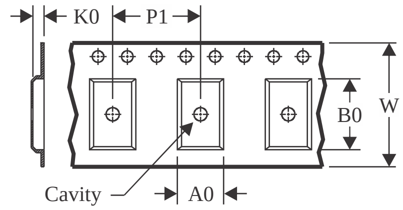
TAPE AND REEL INFORMATION

REEL DIMENSIONS

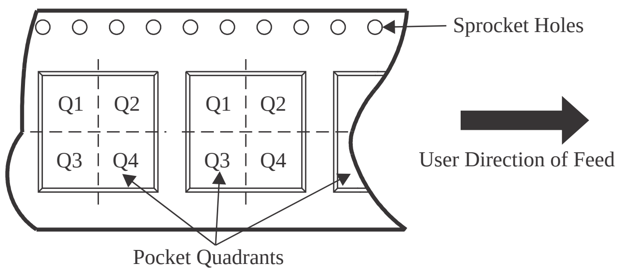


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

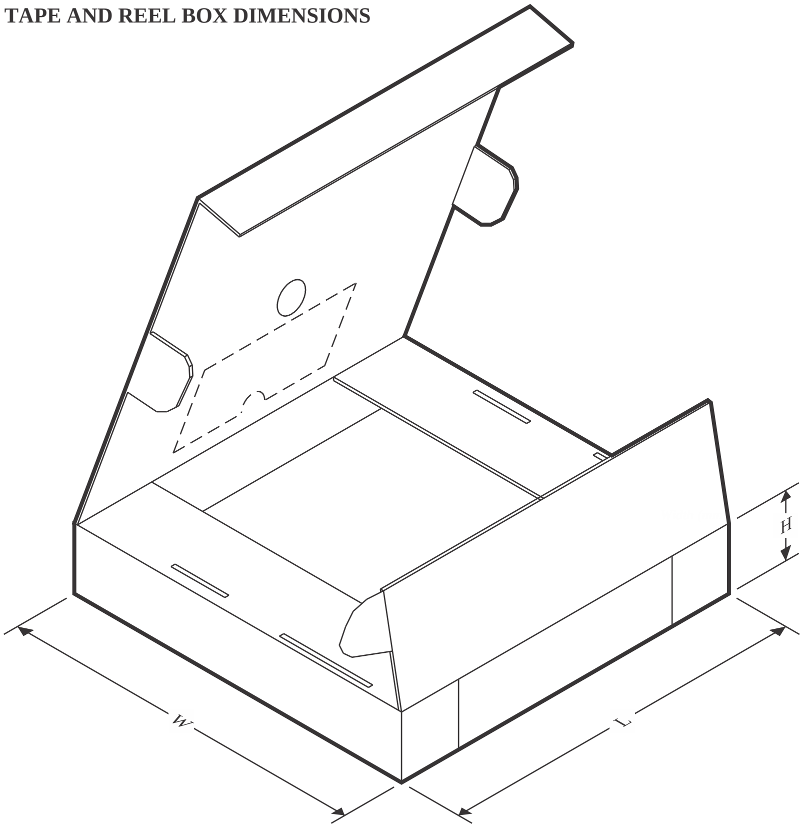
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA141U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA141UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

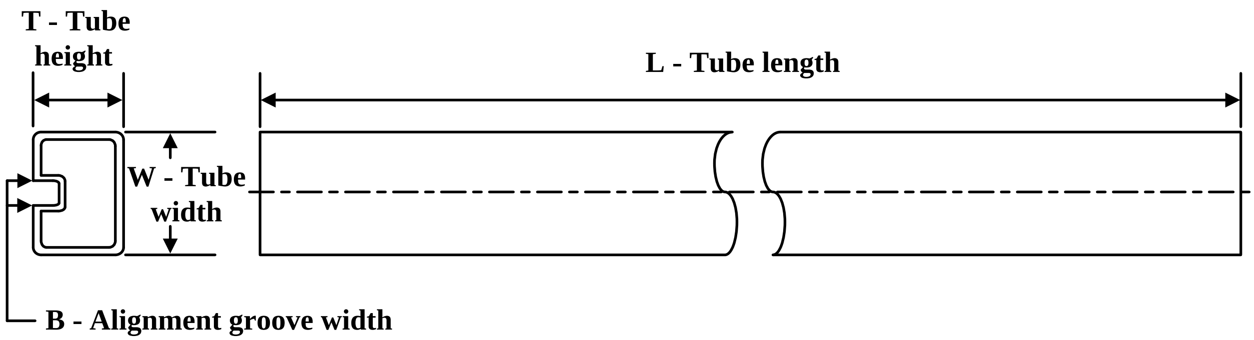
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA141U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
INA141UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA141U	D	SOIC	8	75	506.6	8	3940	4.32
INA141U.B	D	SOIC	8	75	506.6	8	3940	4.32
INA141UA	D	SOIC	8	75	506.6	8	3940	4.32
INA141UA.B	D	SOIC	8	75	506.6	8	3940	4.32

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