INA129-EP Precision, Low Power Instrumentation Amplifiers

1 Features

- Low Offset Voltage
- Low Input Bias Current
- High CMR: 95 dB (Typical)
- Inputs Protected to ±40 V
- Wide Supply Range: ±2.25 V to ±18 V
- Low Quiescent Current: 2 mA (Typical)

2 Applications

- Bridge Amplifier
- Thermocouple Amplifier
- RTD Sensor Amplifier
- Medical Instrumentation
- Data Acquisition
- Supports Extreme Temperature Applications:
  - Controlled Baseline
  - One Assembly and Test Site
  - One Fabrication Site
  - Available in Military (–55°C to +125°C) Temperature Range [(1)]
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability

(1) Custom temperature ranges available

3 Description

The INA129-EP device is a low power, general-purpose instrumentation amplifier offering excellent accuracy. The versatile 3-op amp design and small size make the device ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200 kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. The INA129-EP provides an industry-standard gain equation; the INA129-EP gain equation is compatible with the AD620.

The INA129-EP device is laser trimmed for very low offset voltage, drift, and high common-mode rejection (113 dB at G ≥ 100). It operates with power supplies as low as ±2.25 V, and quiescent current is only 750 μA–ideal for battery operated systems. Internal input protection can withstand up to ±40 V without damage.

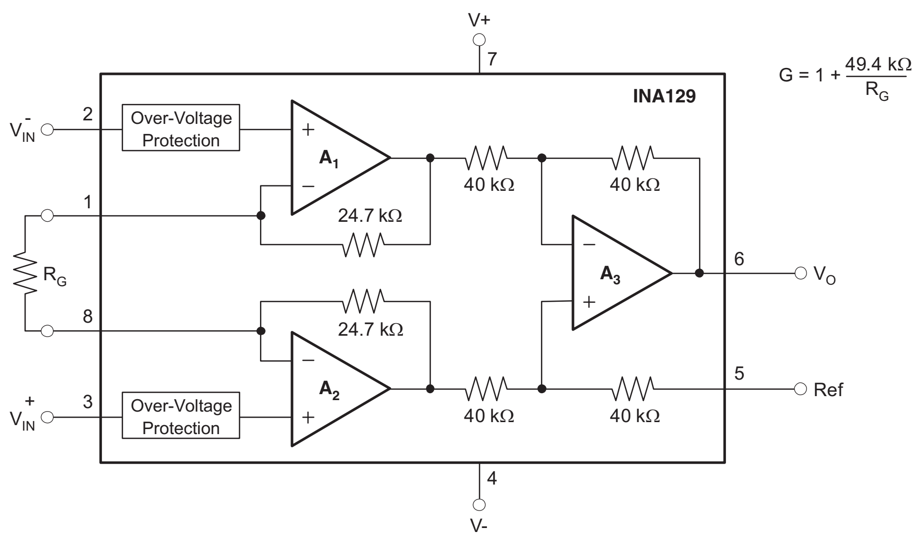
The INA129-EP is available in a 8-Pin SOIC surface-mount package specified for the –55°C to 125°C temperature range.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA129-EP	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

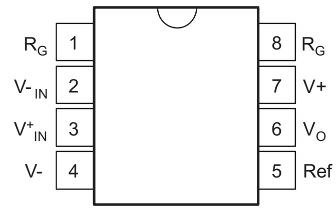
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2009) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed junction-to-ambient thermal resistance value for 8-pin DIP package, and updated SOIC package thermal information. ... 5

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View

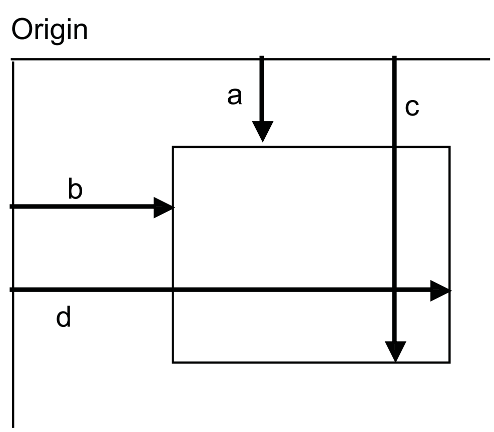


Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
Ref	5	I	Output voltage reference
RG	1, 8	O	Gain resistor connection
V+	7	Power	Positive power supply voltage from 2.25 V to 18 V
V–	4	Power	Negative power supply voltage from –2.25 V to –18 V
V+IN	3	I	Non-inverting input voltage
V–IN	2	I	Inverting input voltage
VO	6	O	Output voltage

Bare Die Information

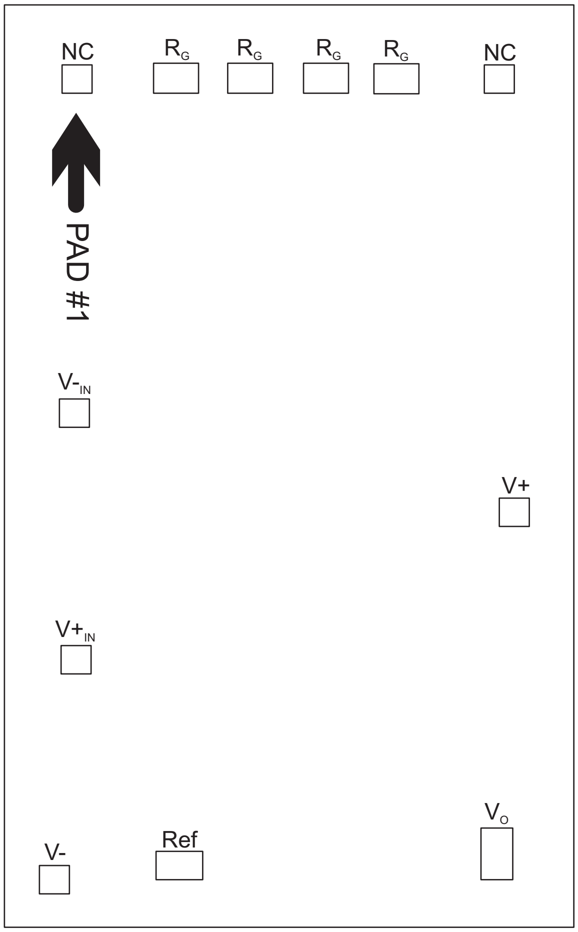
DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils	Silicon with backgrind	GND	Al-Si-Cu (0.5%)



Bond Pad Coordinates in Mils

DESCRIPTION	PAD NUMBER	a	b	c	d
NC	1	-57.4	-31.1	-53.3	-27
$V-_{IN}$	2	-9.85	-31.4	-5.75	-27.3
$V+_{IN}$	3	25.05	-31.4	29.15	-27.3
V-	4	56.2	-34.3	60.3	-30.2
Ref	5	53.75	-17.6	57.85	-11
V_O	6	50.35	27.8	56.95	31.9
V+	7	7.75	30.2	11.85	34.3
NC	8	-57.4	28.4	-53.3	32.5
R_G (1)	9	-57.4	13.4	-53.3	20
R_G (1)	10	-57.5	2.7	-53.4	9.3
R_G (1)	11	-57.5	-7.9	-53.4	-1.3
R_G (1)	12	-57.4	-18.6	-53.3	-12

(1) Pads 9 and 10 must both be bonded to a common point and correspond to package pin 8. Pads 11 and 12 must both be bonded to a common point and correspond to package pin 1.



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
V_S	Supply voltage		±18	V
	Analog input voltage		±40	V
	Output short-circuit (to ground)	Continuous		
T_A	Operating temperature	–55	125	°C
T_J	Junction temperature		150	°C
	Lead temperature (soldering, 10s)		300	°C
T_{stg}	Storage temperature	–55	125	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins [2]	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V power supply	±2.25	±15	±18	V
Input common-mode voltage range for V_O = 0	V - 2 V		V + –2 V	
T_A operating temperature INA129-EP	–55		125	°C

6.4 Thermal Information

THERMAL METRIC [1]		INA129-EP D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			T_A = 25°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT									
Offset Voltage, RTI									
Initial	T_A = 25°C				±100 ±800/G				μV
	Overtemperature							±150 ±2050/G	μV
vs power supply	T_A = 25°C, V_S = ±2.25 V to ±18 V				±1.6 ±175/G				μV/V
	Overtemperature							±1.8 ±175/G	μV/V
Long-term stability				±1 ±3/G					μV/mo
Impedance, differential				10^{10} || 2					Ω || pF
Common mode				10^{11}||9					Ω || pF
Common mode voltage range (1)	V_O = 0 V		(V+) − 2	(V+) − 1.4					V
			(V−) + 2	(V−) + 1.7					V
Safe input voltage					±40				V
Common-mode rejection	V_{CM} = ±13 V, ΔR_S = 1 kΩ	G = 1	75	86					dB
		Overtemperature				67			dB
		G = 10	93	106					dB
		Overtemperature				84			dB
		G = 100	113	125					dB
		Overtemperature				98			dB
		G = 1000	113	130					dB
		Overtemperature				98			dB
CURRENT									
Bias current				±2	±8				nA
	Overtemperature							±16	nA
Offset Current				±1	±8				nA
	Overtemperature							±16	nA
NOISE									
Noise voltage, RTI	G = 1000, R_S = 0 Ω	f = 10 Hz		10					nV/√Hz
		f = 100 Hz		8					nV/√Hz
		f = 1 kHz		8					nV/√Hz
		f_B = 0.1 Hz to 10 Hz		0.2					μVpp
Noise current	G = 1000, R_S = 0 Ω	f = 10 Hz		0.9					pA/√Hz
		f = 1 kHz		0.3					pA/√Hz
		f_B = 0.1 Hz to 10 Hz		30					pA_{PP}
GAIN									
Gain equation				1 + (49.4 kΩ/R_G)					V/V
Range of gain			1		10000				V/V

(1) Input common-mode range varies with output voltage — see *Typical Characteristics*.

Electrical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A = 25°C			T_A = 25°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Gain error		G = 1		±0.05%	±0.1%				
		Overtemperature						±0.15%	
		G = 10		±0.02%	±0.5%				
		Overtemperature						±0.65%	
		G = 100		±0.05%	±0.65%				
		Overtemperature						±1.1%	
		G = 1000		±0.5%	±2%				
Gain vs temperature(2)		G = 1		±1	±10				ppm/°C
49.4-kΩ resistance(2)(3)				±25	±100				ppm/°C
Nonlinearity		V_O = ±13.6 V, G = 1		±0.0001	±0.0018				% of FSR
		Overtemperature						±0.0035	
		G = 10		±0.0003	±0.0035				
		Overtemperature						±0.0055	
		G = 100		±0.0005	±0.0035				
		Overtemperature						±0.0055	
		G = 1000		±0.001	See (4)				
OUTPUT									
Voltage	Positive	R_L = 10 kΩ	(V+) − 1.4	(V+) − 0.9					V
	Negative	R_L = 10 kΩ	(V−) + 1.4	(V−) + 0.8					
Load capacitance stability				1000					pF
Short-circuit current				+6/−15					mA
FREQUENCY RESPONSE									
Bandwidth, −3 dB		G = 1		1300					kHz
		G = 10		700					
		G = 100		200					
		G = 1000		20					
Slew rate		V_O = ±10 V, G = 10		4					V/µs
Settling time, 0.01%		G = 1		7					µs
		G = 10		7					
		G = 100		9					
		G = 1000		80					
Overload recovery		50% overdrive		4					µs
POWER SUPPLY									
Voltage range			±2.25	±15	±18				V
Current, total		V_{IN} = 0 V		±700	±750				µA
		Overtemperature						±1200	
TEMPERATURE RANGE									
Specification			−55		125				°C
Operating			−55		125				°C

(2) Specified by wafer test.
(3) Temperature coefficient of the 49.4-kΩ term in the gain equation.
(4) Nonlinearity measurements in G = 1000 are dominated by noise. Typical nonlinearity is ±0.001%.

6.6 Typical Characteristics

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

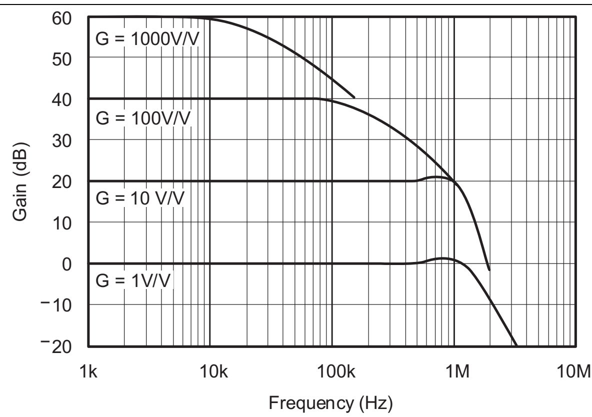


Figure 1. Gain vs Frequency

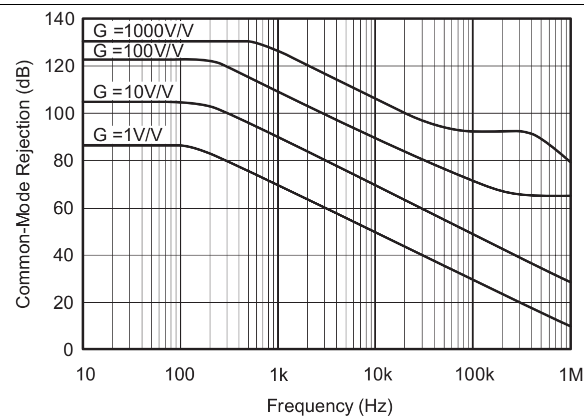


Figure 2. Common-Mode Rejection vs Frequency

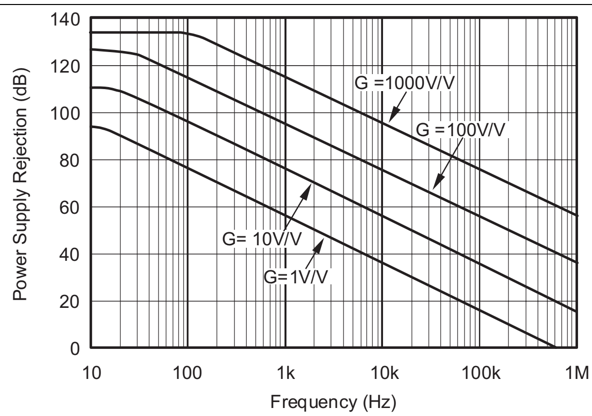


Figure 3. Positive Power-Supply Rejection vs Frequency

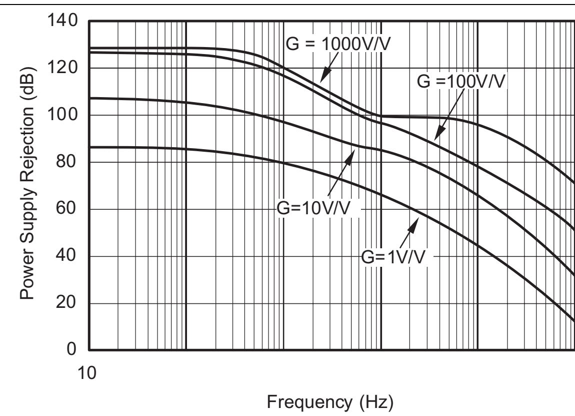
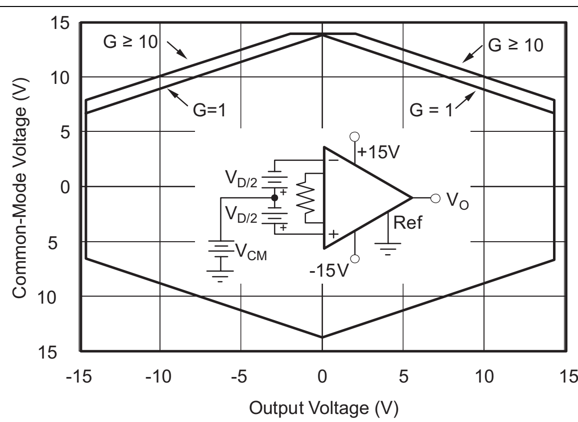
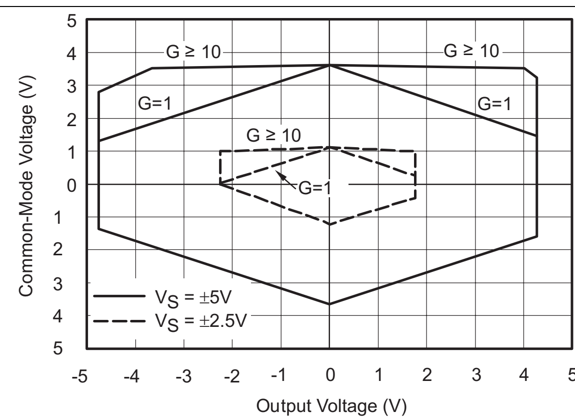


Figure 4. Negative Power-Supply Rejection vs Frequency



V_S = ±15 V

Figure 5. Input Common-Mode Range vs Output Voltage



V_S = ±5 V, ±2.5 V

Figure 6. Input Common-Mode Range vs Output Voltage

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

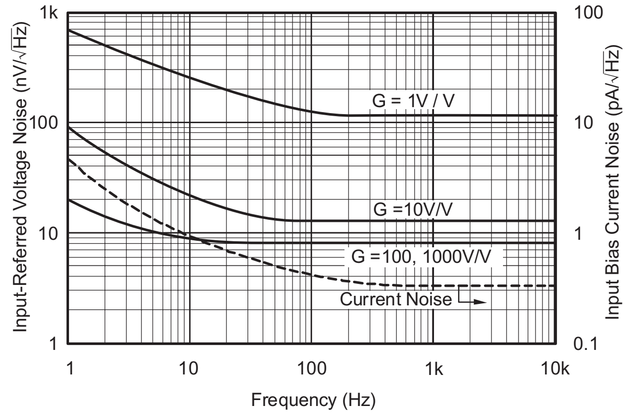


Figure 7. Input-Referred Noise vs Frequency

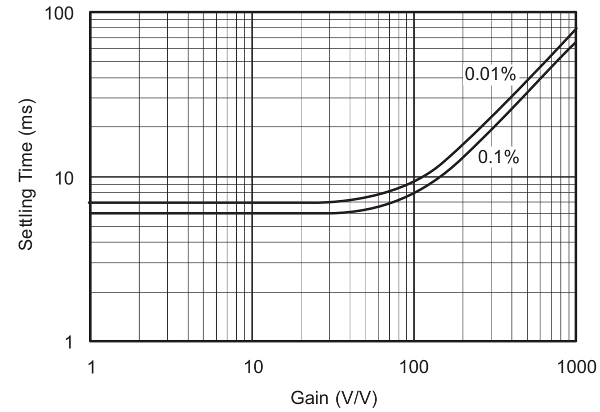


Figure 8. Settling Time vs Gain

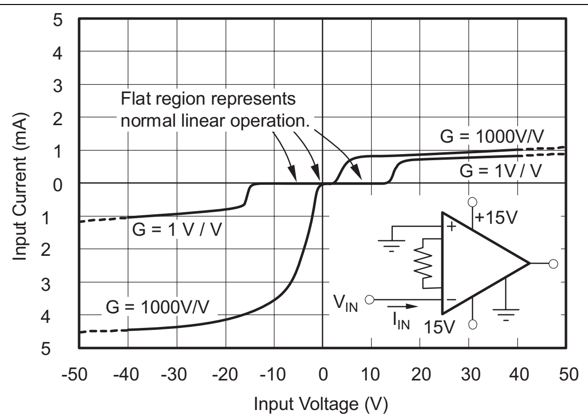


Figure 9. Input Overvoltage Voltage-to-Current Characteristics

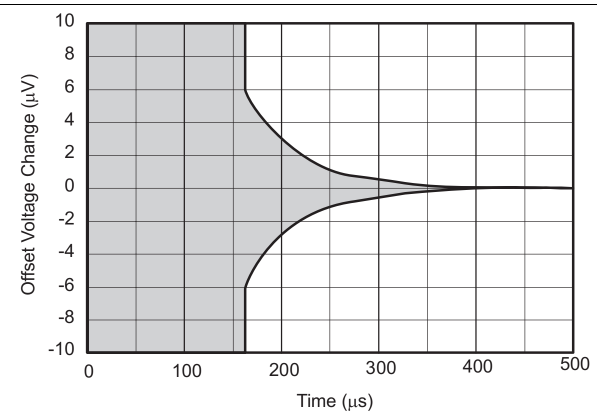


Figure 10. Input Offset Voltage Warm-Up

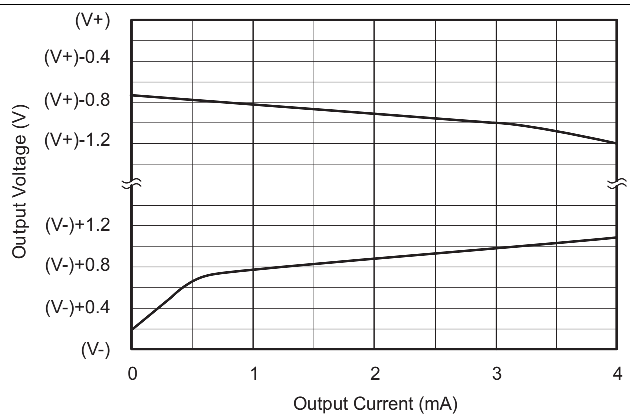


Figure 11. Output Voltage Swing vs Output Current

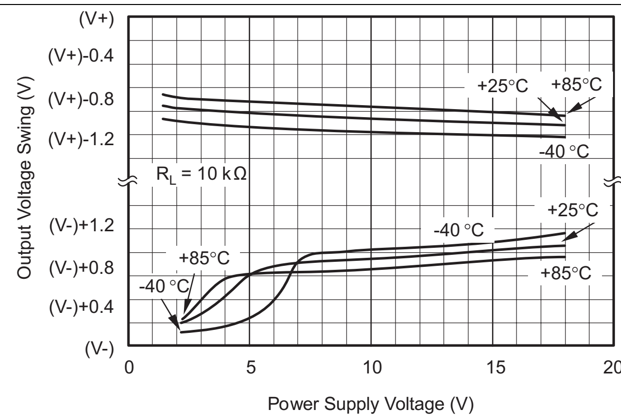


Figure 12. Output Voltage Swing vs Power Supply Voltage

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

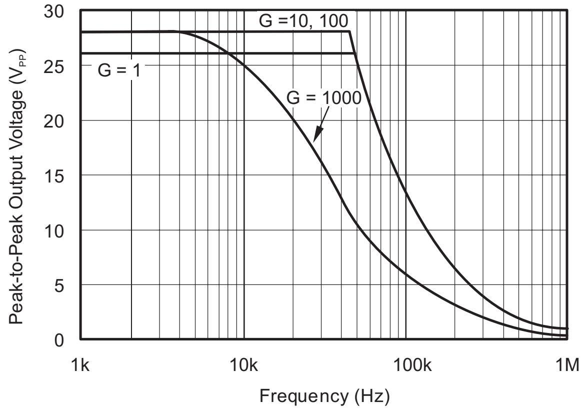


Figure 13. Maximum Output Voltage vs Frequency

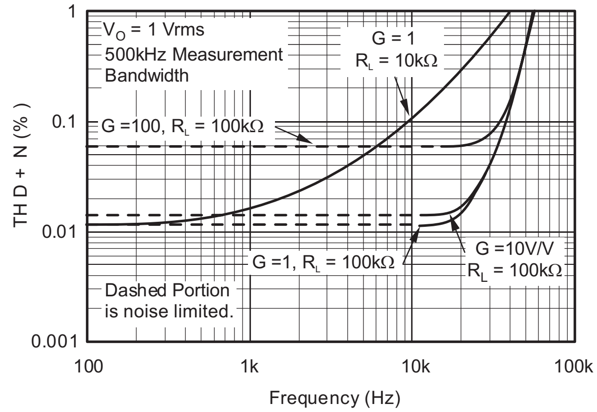


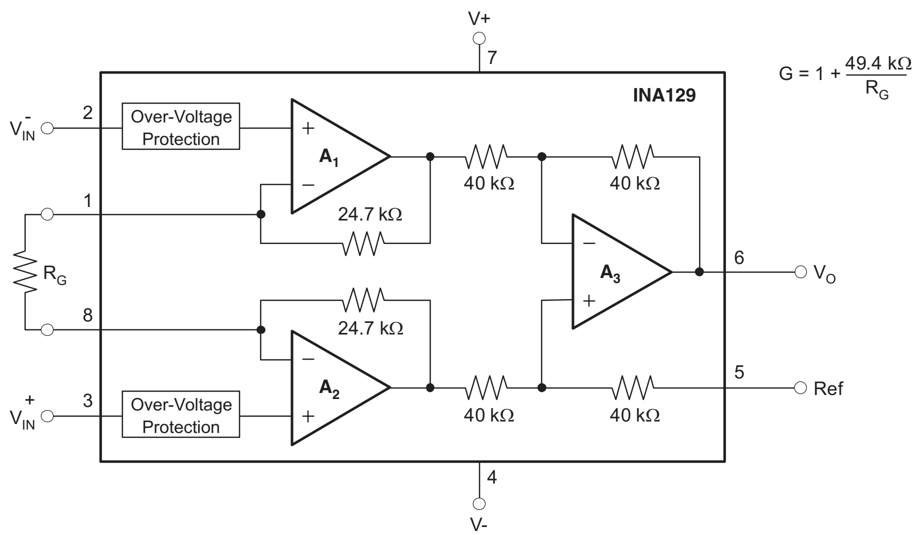
Figure 14. Total Harmonic Distortion + Noise vs Frequency

7 Detailed Description

7.1 Overview

The INA129-EP instrumentation amplifier is a type of differential amplifier that has been outfitted with input protection circuit and input buffer amplifiers, which eliminate the need for input impedance matching and make the amplifier particularly suitable for use in measurement and test equipment. Additional characteristics of the INA129-EP include a very low DC offset, low drift, low noise, very high open-loop gain, very high common-mode rejection ratio, and very high input impedances. The INA129-EP is used where great accuracy and stability of the circuit both short and long-term are required.

7.2 Functional Block Diagram



7.3 Feature Description

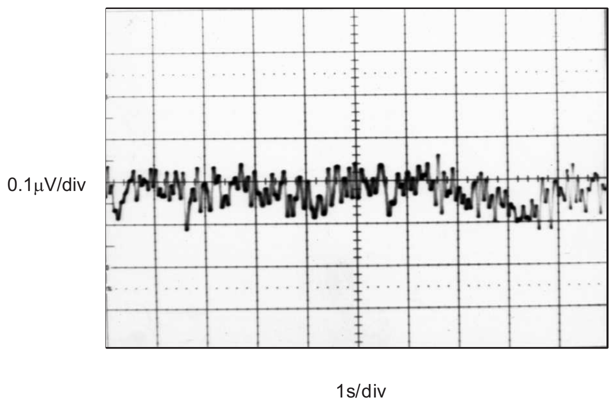
The INA129-EP device is a low power, general-purpose instrumentation amplifier that offers excellent accuracy. The versatile three-operational-amplifier design and small size make the amplifier ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth, even at high gain. A single external resistor sets any gain from 1 to 10,000. The INA129-EP device is laser trimmed for very low offset voltage (50 μV) and high common-mode rejection (93 dB at G ≥ 100). This device operates with power supplies as low as ±2.25 V, and quiescent current of 2 mA, typically. The internal input protection can withstand up to ±40 V without damage.

7.4 Device Functional Modes

A single external resistor sets the any gain from 1 to 10000. TI INA129-EP provides an industry standard gain equation, as highlighted in Figure 16.

7.4.1 Noise Performance

The INA129-EP provides very low noise in most applications. Low frequency noise is approximately 0.2 μVPP measured from 0.1 Hz to 10 Hz (G ≥ 100). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.



G ≥ 100

Figure 15. 0.1-Hz to 10-Hz Input-Referred Voltage Noise

7.4.2 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA129-EP is from approximately 1.4 V below the positive supply voltage to 1.7 V above the negative supply. As a differential input voltage causes the output voltage increase, however, the linear input range will be limited by the output voltage swing of amplifiers A1 and A2. So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage (see Figure 5 and Figure 6).

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of A3 will be near 0 V even though both inputs are overloaded.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA129-EP device measures small differential voltage with high common-mode voltage developed between the non-inverting and inverting input. The high-input voltage protection circuit in conjunction with high input impedance make the INA129-EP suitable for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

8.2 Typical Application

Figure 16 shows the basic connections required for operation of the INA129-EP. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 8 Ω in series with the Ref pin will cause a typical device to degrade to approximately 80 dB CMR (G = 1).

$$G = 1 + \frac{49.4k\Omega}{R_G}$$

DESIRED GAIN (V/V)	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	49.4K	49.9K
5	12.35K	12.4K
10	5489	5.49K
20	2600	2.61K
50	1008	1K
100	499	499
200	248	249
500	99	100
1000	49.5	49.9
2000	24.7	24.9
5000	9.88	9.76
10000	4.94	4.87

NC: No Connection

Also drawn in simplified form:

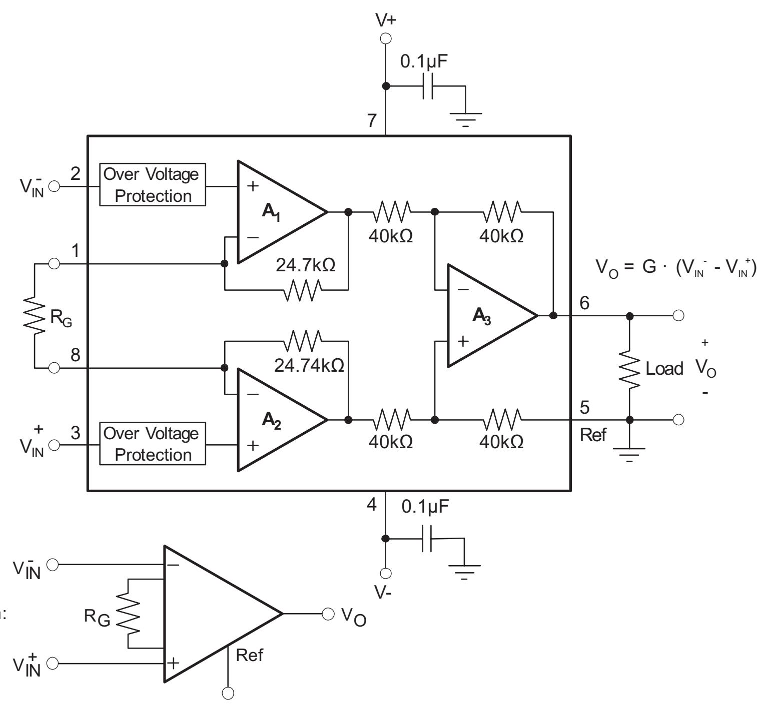


Figure 16. Basic Connections

8.2.1 Design Requirements

The device can be configured to monitor the input differential voltage when the gain of the input signal is set by the external resistor R_G. The output signal references to the REF pin. The most common application is where the output is referenced to ground when no input signal is present by connecting the REF pin to ground, as Figure 16 shows. When the input signal increases, the output voltage at the OUT pin increases, too.

Typical Application (continued)

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Gain

Gain is set by connecting a single external resistor, R_G, between pins 1 and 8.

$$G = 1 + \frac{49.4\ \text{k}\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 16.

The 49.9-kΩ term in Equation 1 comes from the sum of the two internal feedback resistors of A1 and A2. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these internal resistors are included in the gain accuracy and drift specifications of the INA129-EP.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from Equation 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

8.2.2.2 Dynamic Performance

Figure 1 shows that, despite its low quiescent current, the INA129-EP achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the input stage circuitry. Settling time also remains excellent at high gain.

8.2.2.3 Offset Trimming

The INA129-EP is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 17 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed with the output. The operational amplifier buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

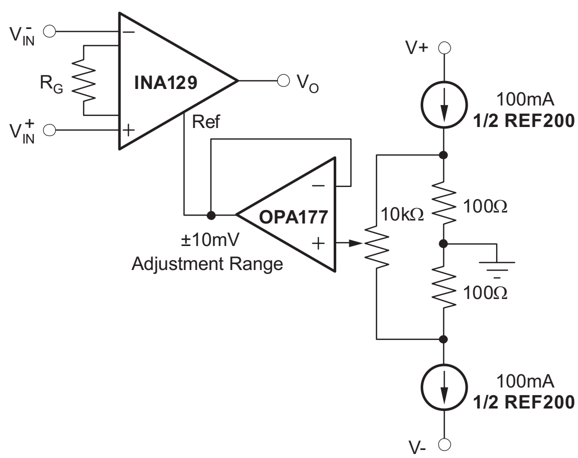


Figure 17. Optional Trimming of Output Offset Voltage

8.2.2.4 Input Bias Current Return Path

The input impedance of the INA129-EP is extremely high (approximately 10^{10} Ω). However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±2 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 18 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range, and the input amplifiers will saturate.

Typical Application (continued)

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 18). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

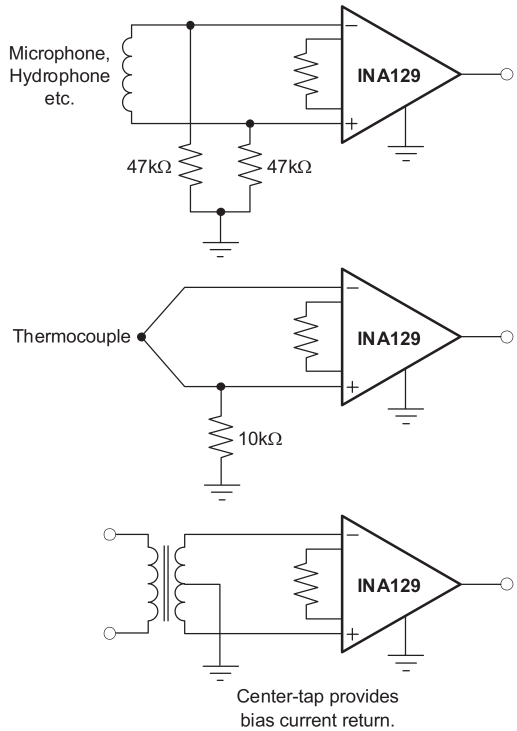
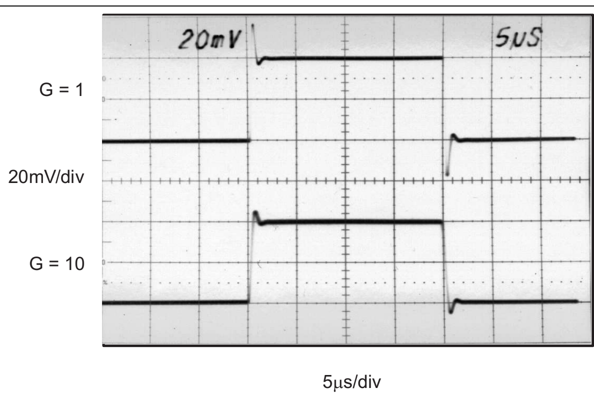


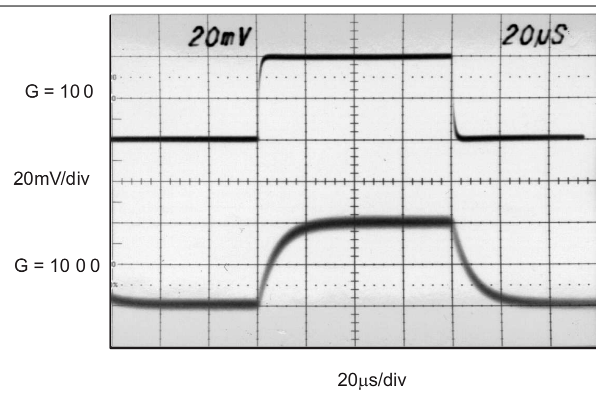
Figure 18. Providing an Input Common-Mode Current Path

8.2.3 Application Curves



G = 1, 10

Figure 19. Small Signal



G = 100, 1000

Figure 20. Small Signal

Typical Application (continued)

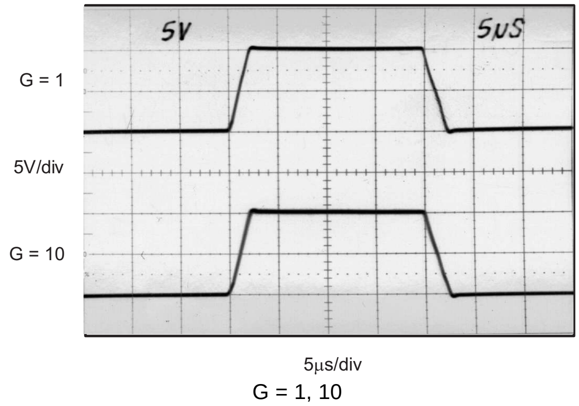


Figure 21. Large Signal

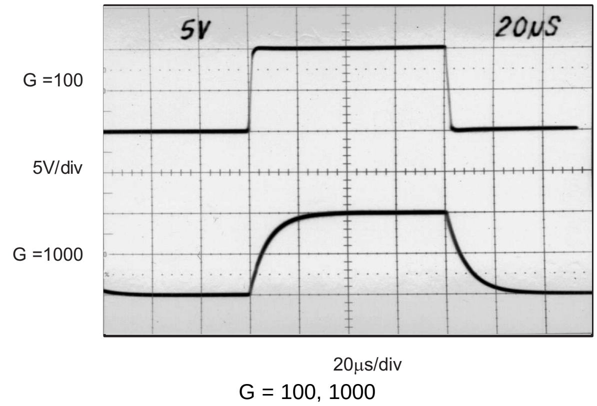


Figure 22. Large Signal

9 Power Supply Recommendations

The minimum power supply voltage for INA129-EP is ±2.25 V and the maximum power supply voltage is ±18 V. This minimum and maximum range covers a wide range of power supplies; but for optimum performance, ±15 V is recommended. TI recommends adding a bypass capacitor at the input to compensate for the layout and power supply source impedance.

9.1 Low Voltage Operation

The INA129-EP can be operated on power supplies as low as ±2.25 V. Performance remains excellent with power supplies ranging from ±2.25 V to ±18 V. Most parameters vary only slightly throughout this supply voltage range.

Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Figure 5 and Figure 6 show the range of linear operation for ±15 V, ±5 V, and ±2.5 V supplies.

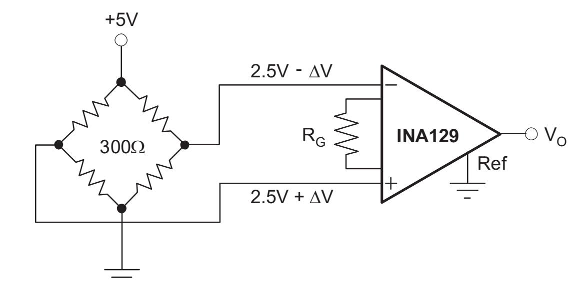


Figure 23. Bridge Amplifier

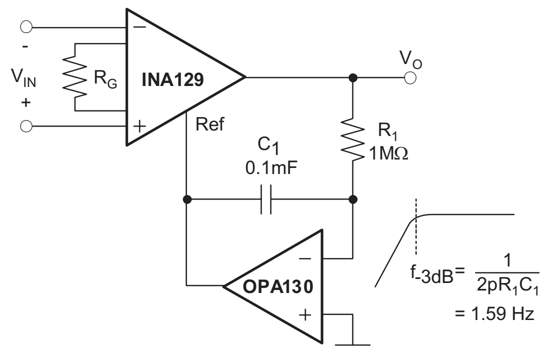
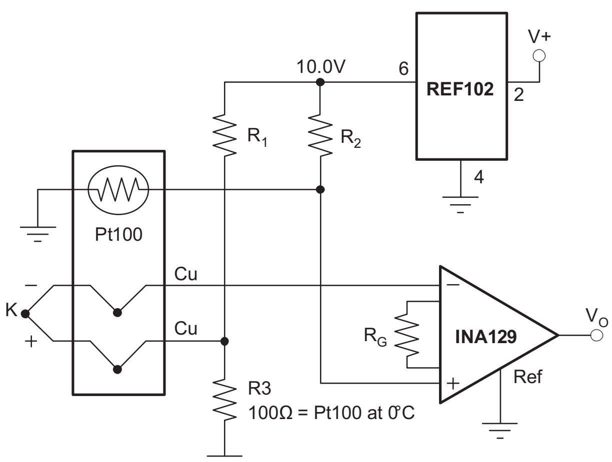
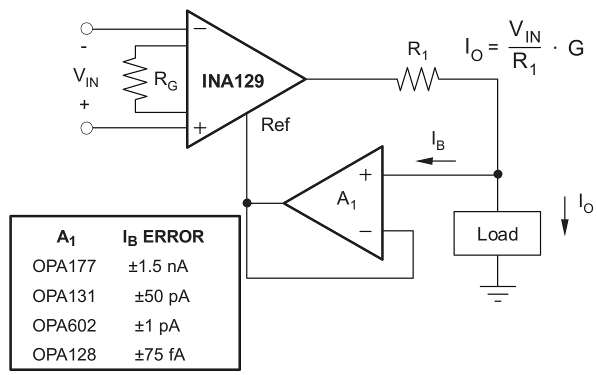


Figure 24. AC-Coupled Instrumentation Amplifier



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (mV/°C)	R_1, R_2
E	+Chromel -Constantan	58.5	66.5kW
J	+Iron -Constantan	50.2	76.8kW
K	+Chromel -Alumel	39.4	97.6kW
T	+Copper -Constantan	38	102kW

Figure 25. Thermocouple Amplifier With RTD Cold-Junction Compensation



A_1	I_B ERROR
OPA177	±1.5 nA
OPA131	±50 pA
OPA602	±1 pA
OPA128	±75 fA

Figure 26. Differential Voltage to Current Converter

Low Voltage Operation (continued)

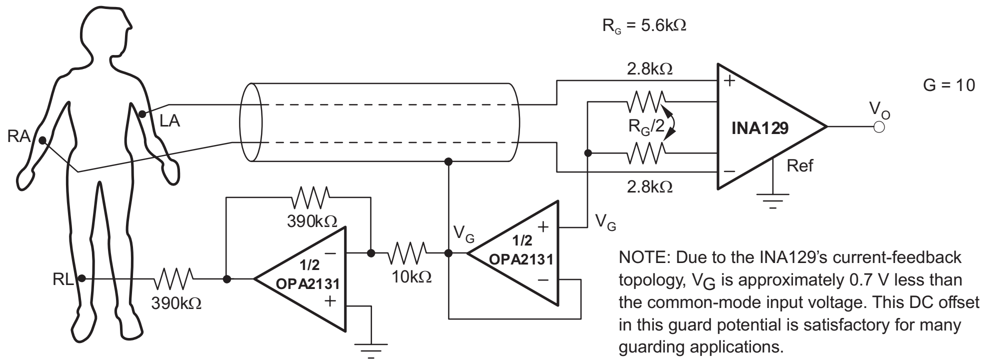


Figure 27. ECG Amplifier With Right-Leg Drive

10 Layout

10.1 Layout Guidelines

Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 μF to 1 μF. If necessary, additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. These decoupling capacitors must be placed between the power supply and INA129-EP device.

The gain resistor must be placed close to pin 1 and pin 8. This placement limits the layout loop and minimizes any noise coupling into the part.

10.2 Layout Example

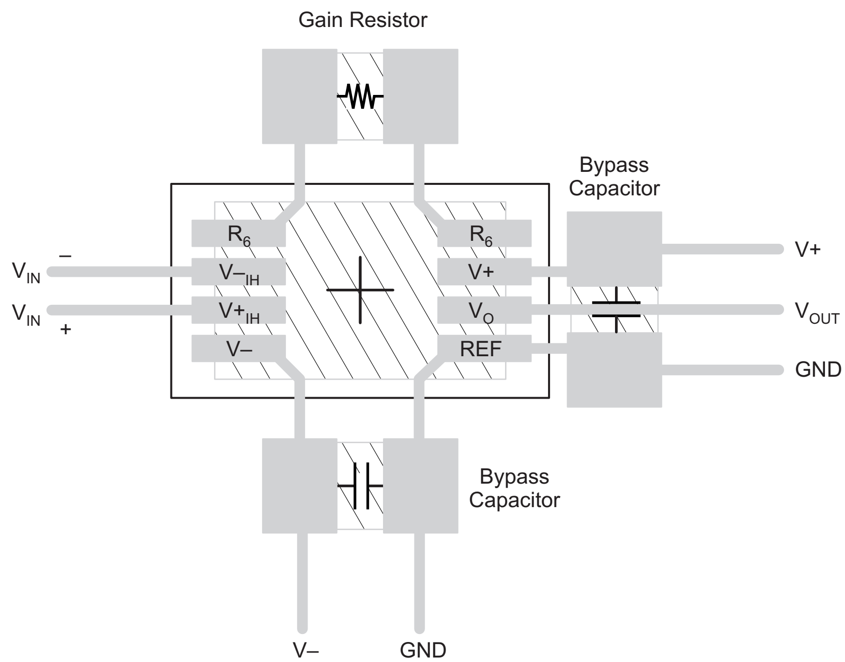


Figure 28. Recommended Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA129MDREP	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	129EP
INA129MDREP.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	129EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

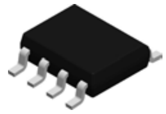
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA129-EP :

- Catalog : INA129

NOTE: Qualified Version Definitions:

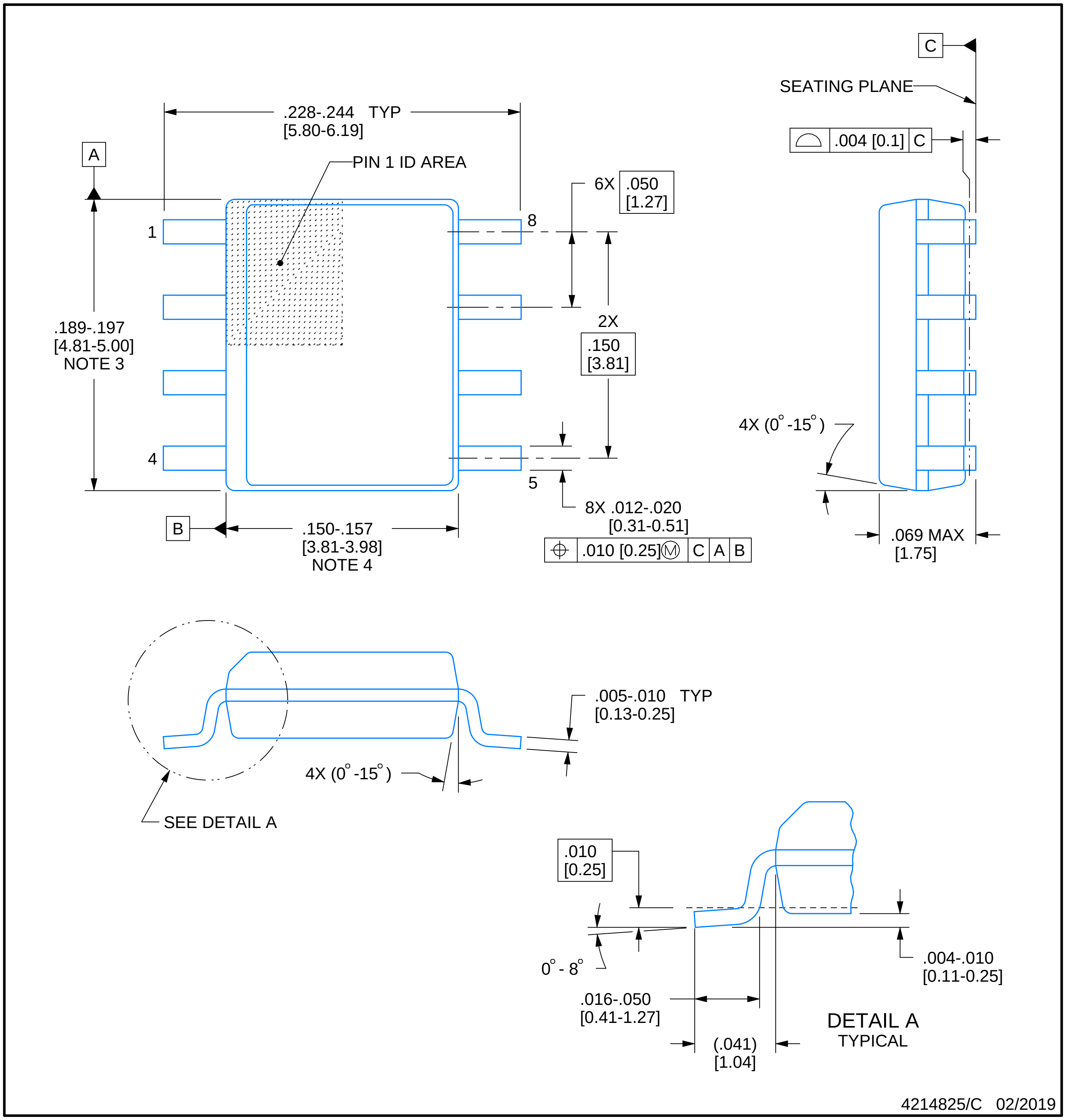
- Catalog - TI's standard catalog product



PACKAGE OUTLINE

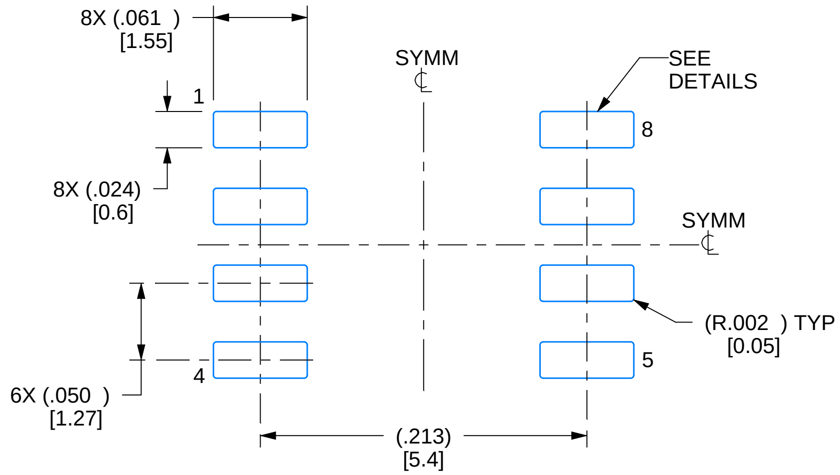
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

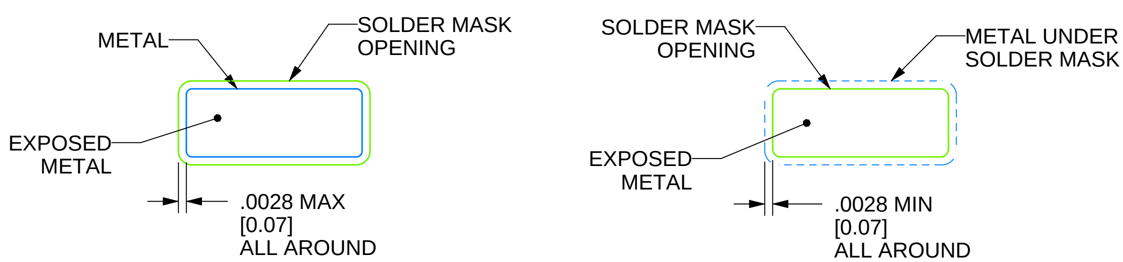


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

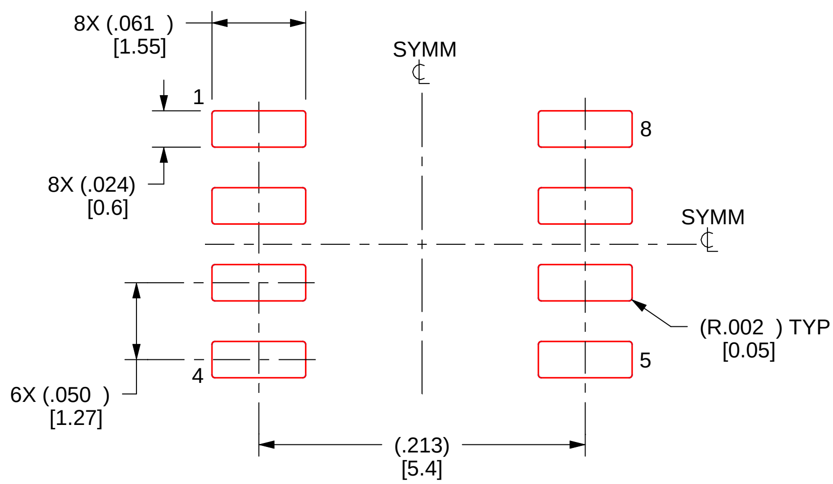
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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