



INA115

Precision INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50 μ V max
- LOW DRIFT: 0.25 μ V/ $^{\circ}$ C max
- LOW INPUT BIAS CURRENT: 2nA max
- HIGH COMMON-MODE REJECTION: 115dB min
- INPUT OVER-VOLTAGE PROTECTION: $\pm$ 40V
- WIDE SUPPLY RANGE: $\pm$ 2.25 TO $\pm$ 18V
- LOW QUIESCENT CURRENT: 3mA max
- SOL-16 SURFACE-MOUNT PACKAGE

APPLICATIONS

- SWITCHED-GAIN AMPLIFIER
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

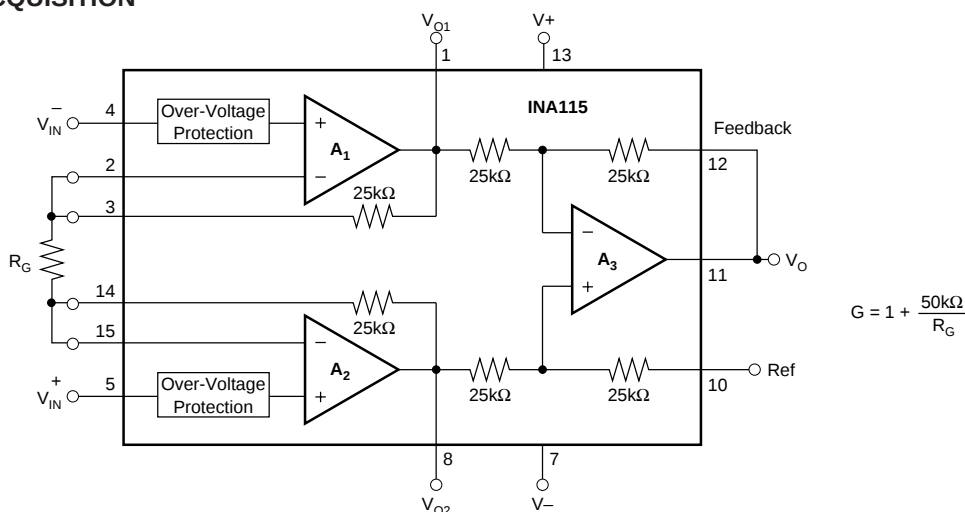
DESCRIPTION

The INA115 is a low cost, general purpose instrumentation amplifier offering excellent accuracy. Its versatile three-op amp design and small size make it ideal for a wide range of applications. Similar to the model INA114, the INA115 provides additional connections to the input op amps, A_1 and A_2 , which improve gain accuracy in high gains and are useful in forming switched-gain amplifiers.

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to $\pm$ 40V without damage.

The INA115 is laser trimmed for very low offset voltage (50 μ V), drift (0.25 μ V/ $^{\circ}$ C) and high common-mode rejection (115dB at $G=1000$). It operates with power supplies as low as $\pm$ 2.25V, allowing use in battery operated and single 5V supply systems. Quiescent current is 3mA maximum.

The INA115 is available in the SOL-16 surface-mount package, specified for the -40° C to $+85^{\circ}$ C temperature range.



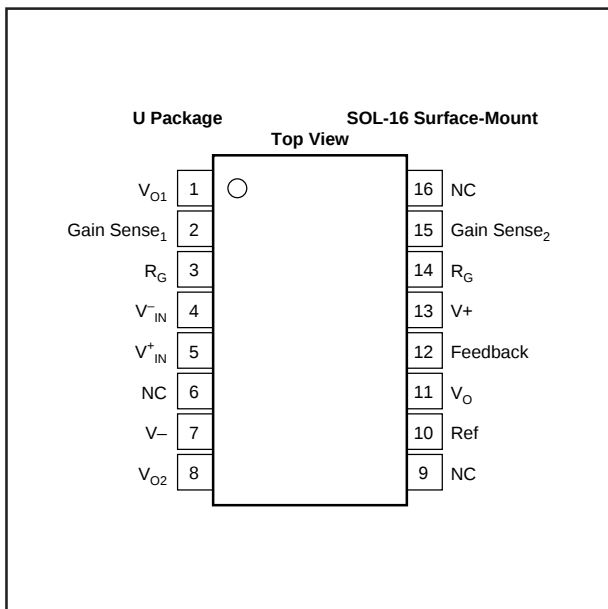
International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

ELECTRICAL

[illegible]

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation. (2) Output specifications are for output amplifier, A₃. A₁ and A₂ provide the same output voltage swing but have less output current drive. A₁ and A₂ can drive external loads of 25kΩ || 200pF.

PIN CONFIGURATIONS



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	−40°C to +125°C
Storage Temperature	−40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

PACKAGE/ORDERING INFORMATION

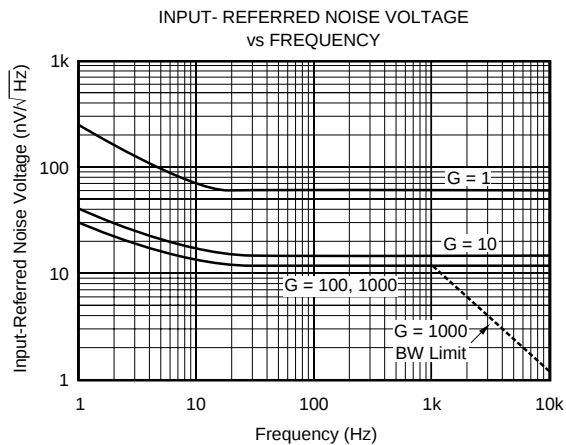
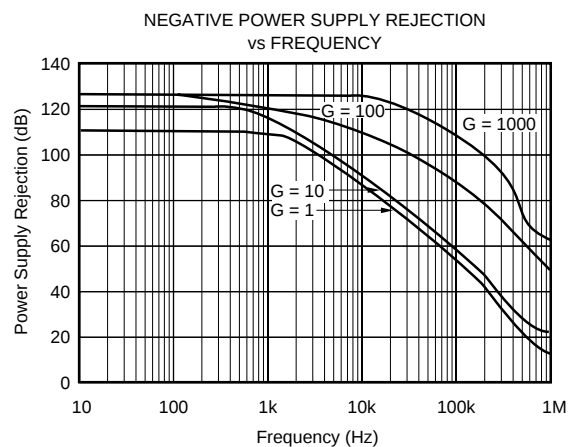
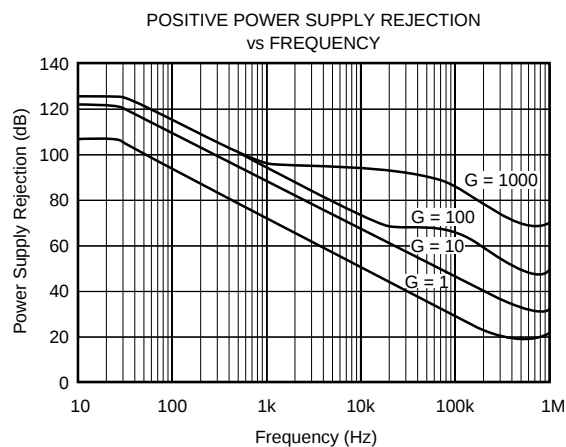
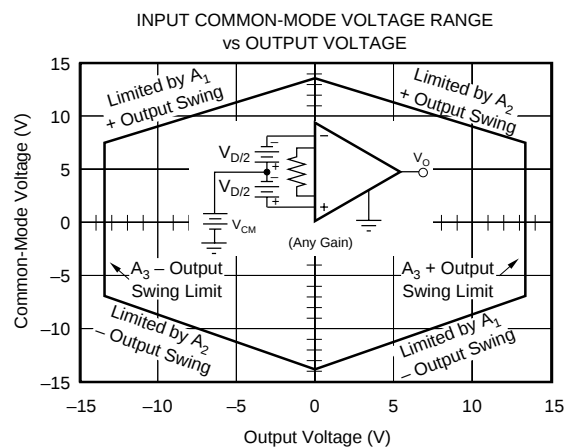
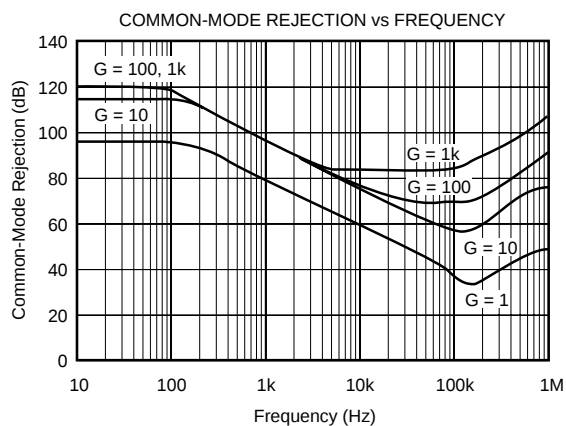
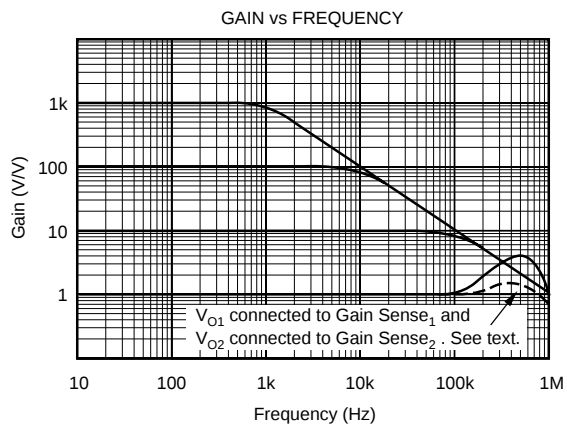
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
INA115AU	SOL-16 Surface-Mount	211	−40°C to +85°C
INA115BU	SOL-16 Surface-Mount	211	−40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

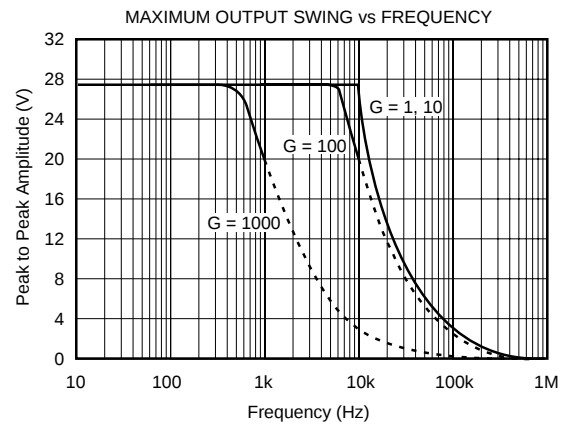
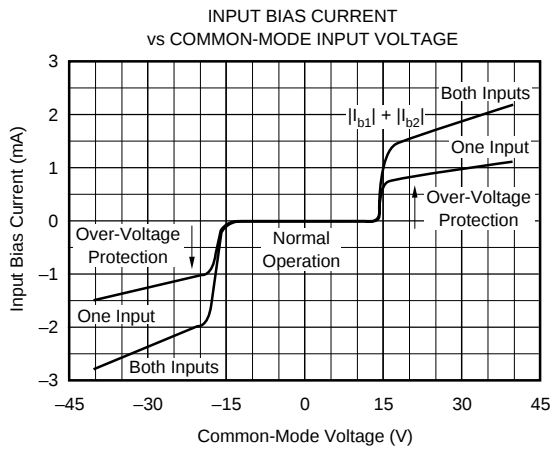
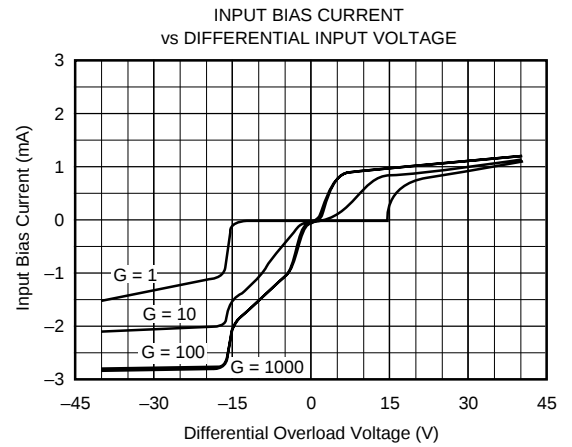
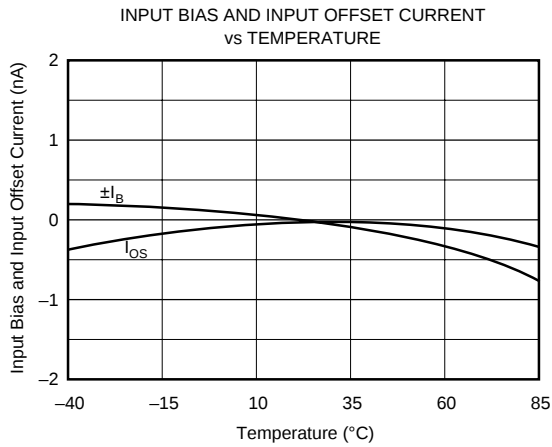
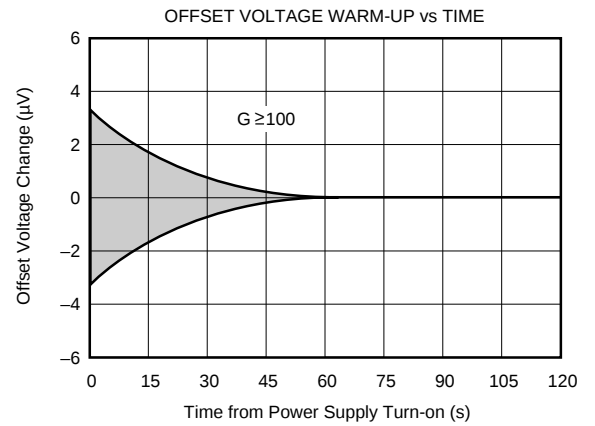
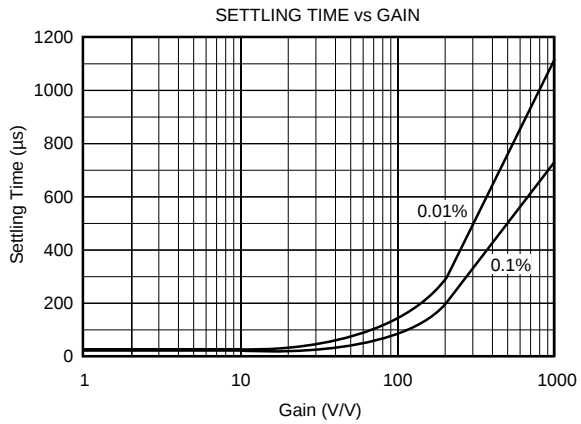
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



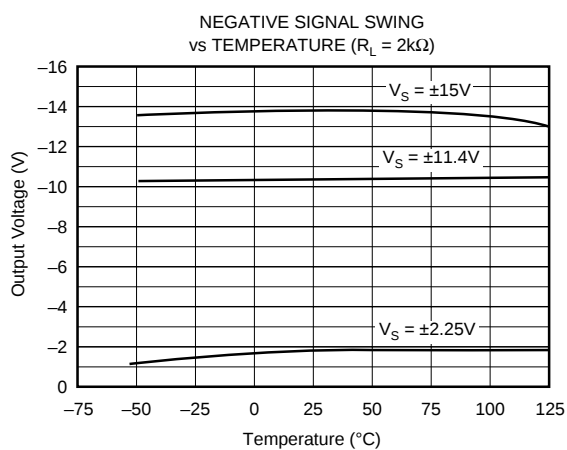
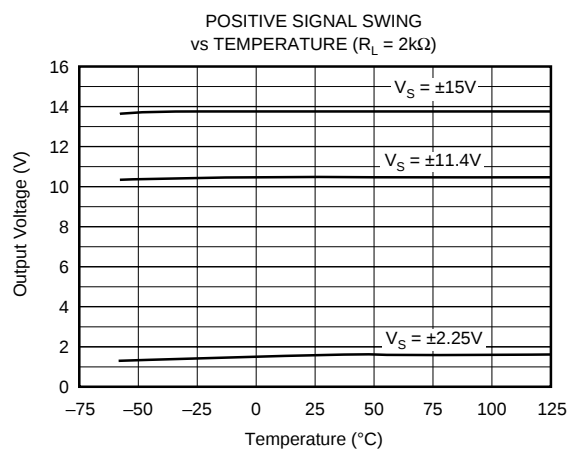
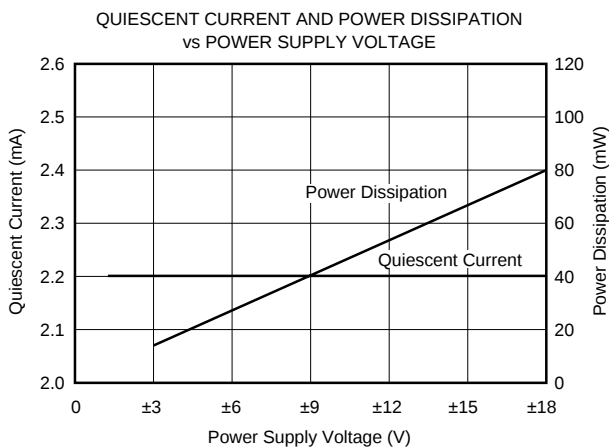
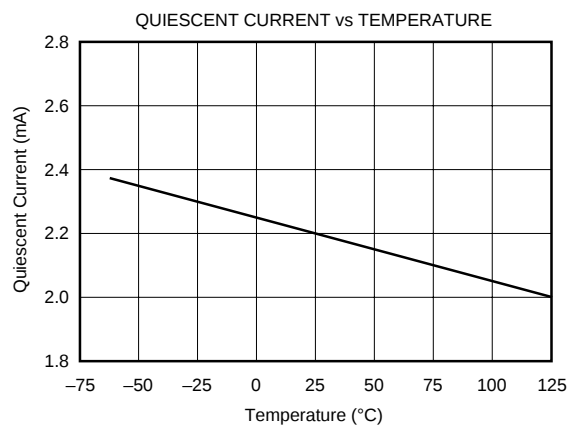
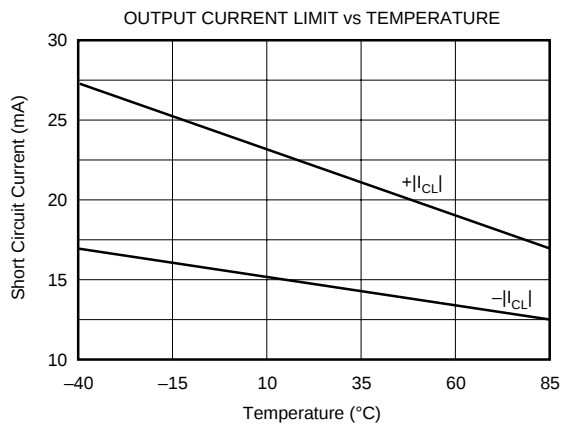
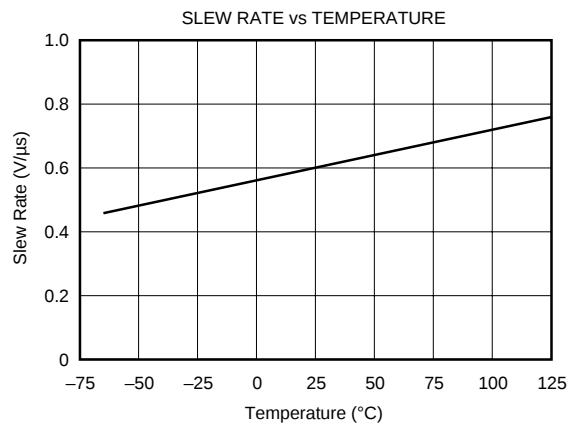
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

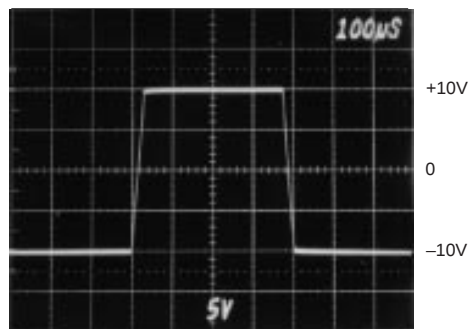
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



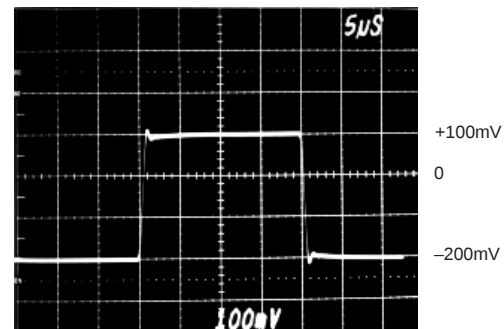
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

LARGE SIGNAL RESPONSE, $G = 1$

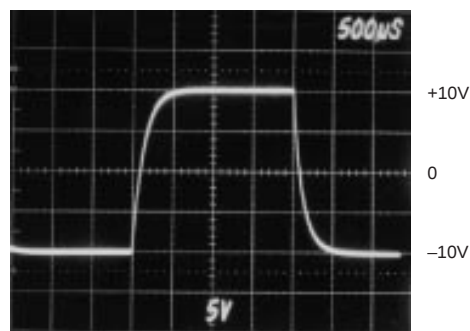


SMALL SIGNAL RESPONSE, $G = 1$

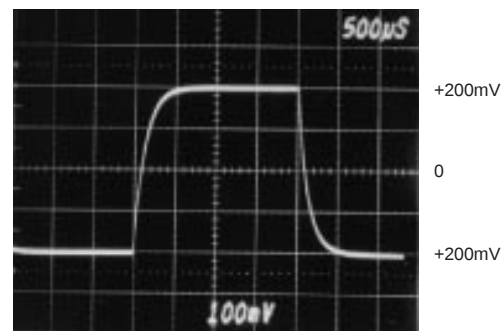


V_{O1} connected to Gain Sense₁ and
 V_{O2} connected to Gain Sense₂

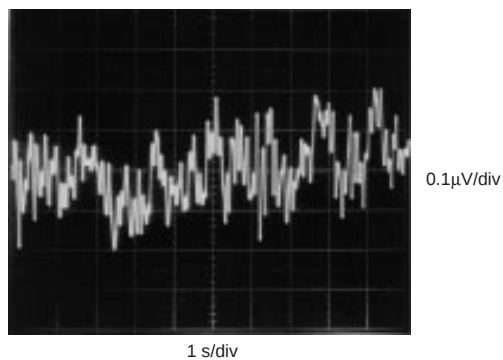
LARGE SIGNAL RESPONSE, $G = 1000$



SMALL SIGNAL RESPONSE, $G = 1000$



INPUT-REFERRED NOISE, 0.1 to 10Hz



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA115. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G=1).

The INA115 has a separate output sense feedback connection (pin 12). Pin 12 must be connected (normally to the output terminal, pin 11) for proper operation. The output sense connection can be used to sense the output voltage directly at the load for best accuracy.

SETTING THE GAIN

Gain of the INA115 is set by connecting a single external resistor, R_G :

$$G = 1 + \frac{50 \text{ k}\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

For G=1, no resistor is required, but connect pins 2-3 and connect pins 14-15. Gain peaking in G=1 can be reduced by shorting the internal 25kΩ feedback resistors (see typical performance curve Gain vs Frequency). To do this, connect pins 1-2-3 and connect pins 8-14-15.

The 50kΩ term in equation 1 comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA115.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. R_G 's contribution to gain error and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. The “force and sense” type connections illustrated in Figure 1 help reduce the effect of interconnection resistance.

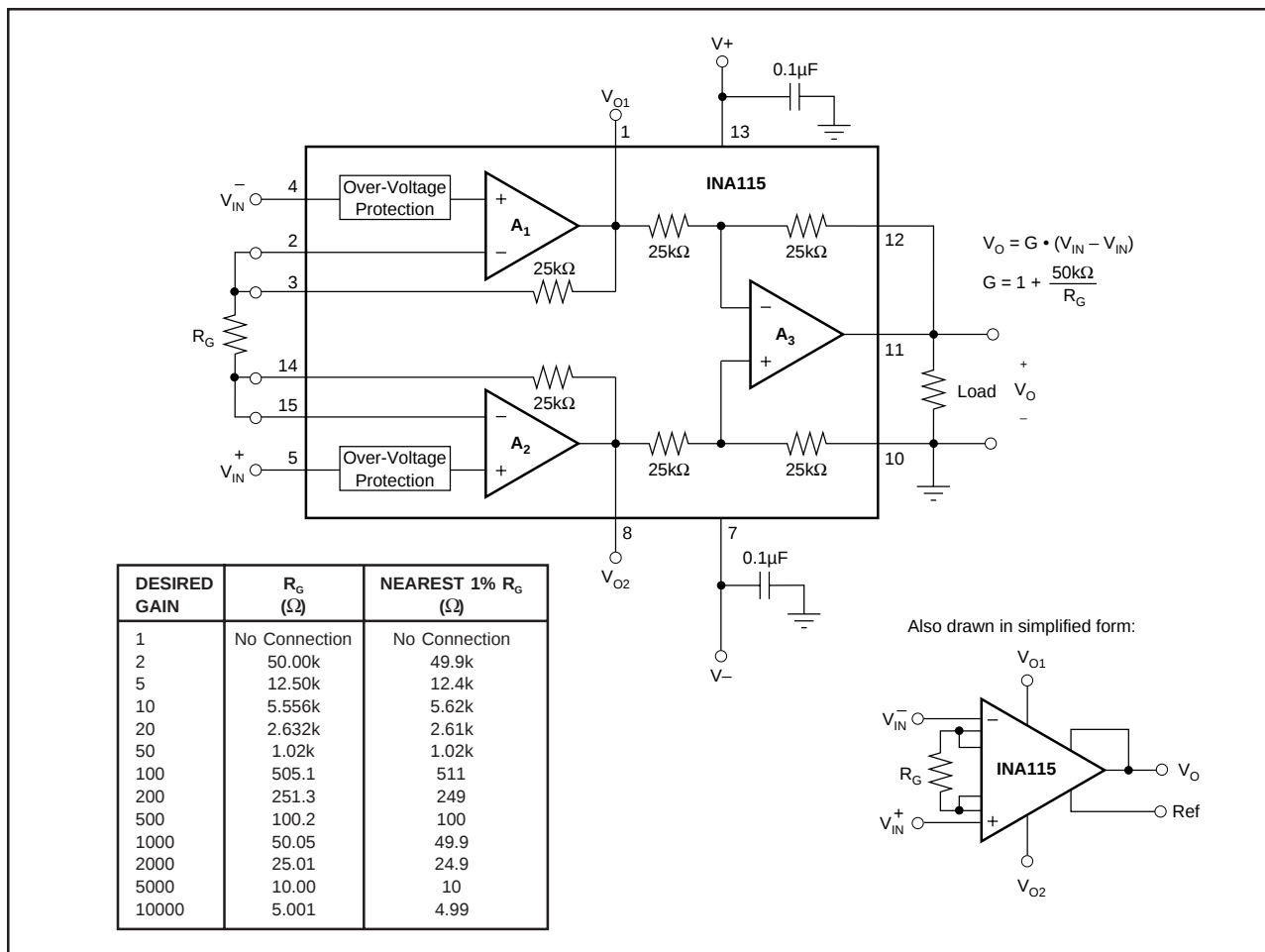


FIGURE 1. Basic Connections.

SWITCHED GAIN

Figure 2 shows a circuit for digital selection of four gains. Multiplexer “on” resistance does not significantly affect gain. The resistor values required for some commonly used gain steps are shown. This circuit uses the internal $25\text{k}\Omega$ feedback resistors, so the resistor values shown cannot be scaled to a different impedance level.

Figure 3 shows an alternative switchable gain configuration. This circuit does not use the internal $25\text{k}\Omega$ feedback resistors, so the nominal values shown can be scaled to other impedance levels. This circuit is ideal for use with a precision resistor network to achieve excellent gain accuracy and lowest gain drift.

NOISE PERFORMANCE

The INA115 provides very low noise in most applications. For differential source impedances less than $1\text{k}\Omega$, the INA103 may provide lower noise. For source impedances greater than $50\text{k}\Omega$, the INA111 FET-Input Instrumentation Amplifier may provide lower noise.

Low frequency noise of the INA115 is approximately $0.4\mu\text{Vp-p}$ measured from 0.1 to 10Hz. This is approximately one-tenth the noise of “low noise” chopper-stabilized amplifiers.

OFFSET TRIMMING

The INA115 is laser trimmed for very low offset voltage and drift. Most applications require no external offset adjustment. Figure 4 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering the trim voltage with an op amp as shown.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA115 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than $\pm 1\text{nA}$ (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA115 is to operate properly. Figure 5 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA115 and the input amplifiers will saturate. If the differential source resistance is low, a bias current return path can be connected to one input (see thermocouple example in Figure 5). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due bias current and better common-mode rejection.

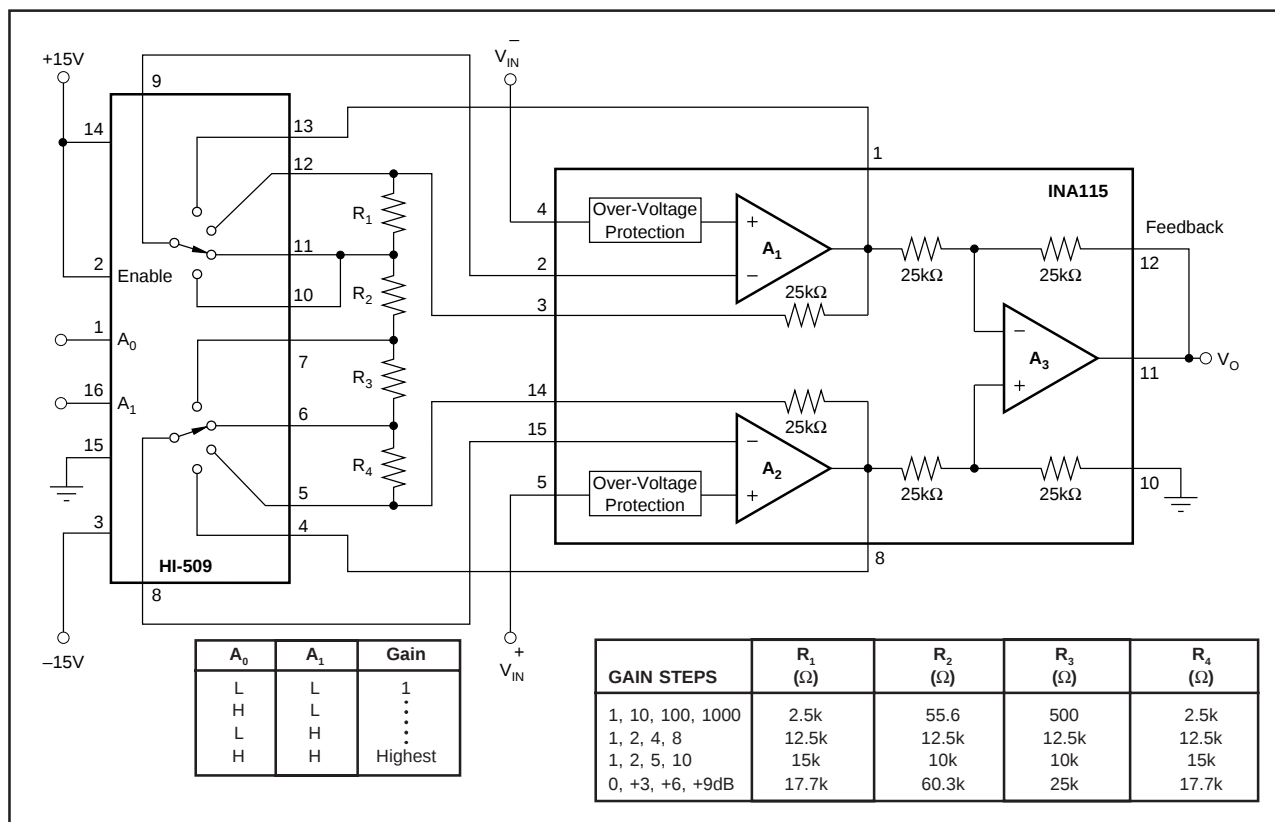


FIGURE 2. Switched-Gain Instrumentation Amplifier (minimum components).

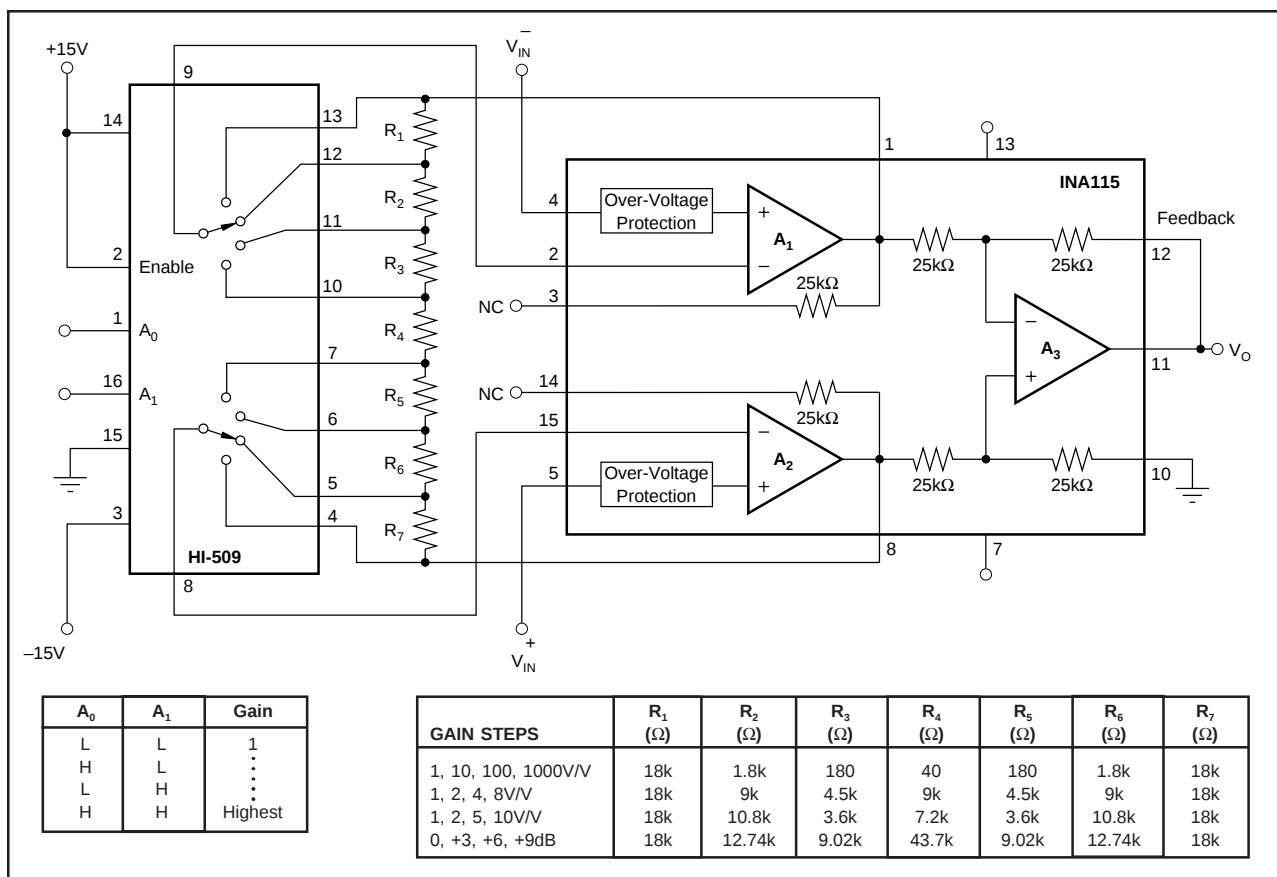


FIGURE 3. Switched-Gain Instrumentation Amplifier (improved gain drift).

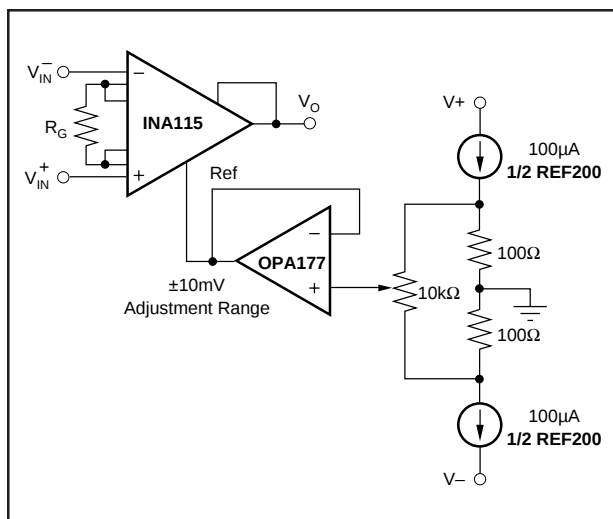


FIGURE 4. Optional Trimming of Output Offset Voltage.

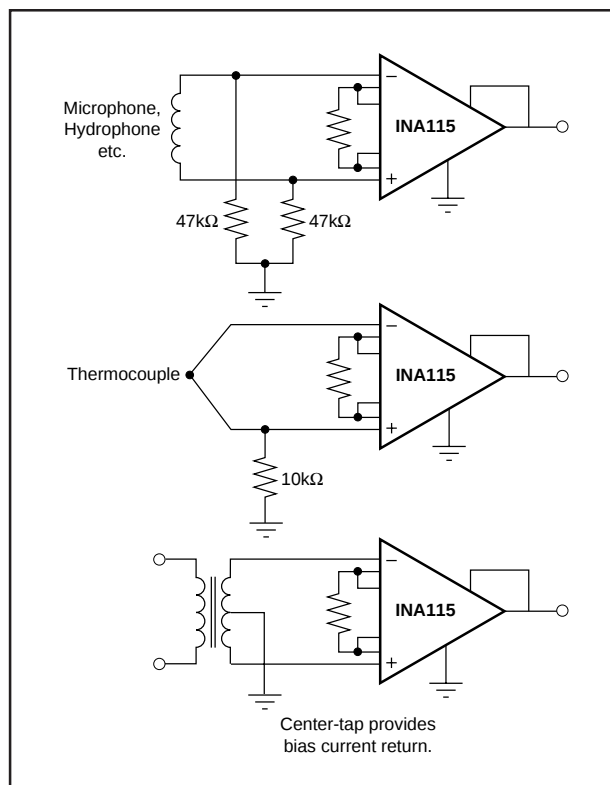


FIGURE 5. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA115 is approximately $\pm 13.75\text{V}$ (or 1.25V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers, A_1 and A_2 . The common-mode range is related to the output voltage of the complete amplifier—see performance curve “Input Common-Mode Range vs Output Voltage.”

A combination of common-mode and differential input signals can cause the output of A_1 or A_2 to saturate. Figure 6 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. Output swing capability of the input amplifiers, A_1 and A_2 is the same as the output amplifier, A_3 . For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA115 in a lower gain (see performance curve “Input Common-Mode Voltage Range vs Output Voltage”). If necessary, add gain after the INA115 to increase the voltage swing.

Input-overload often produces an output voltage that appears normal. For example, an input voltage of $+20\text{V}$ on one input and $+40\text{V}$ on the other input will obviously exceed the linear

common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA115 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the INA115 are individually protected for voltages up to $\pm 40\text{V}$. For example, a condition of -40V on one input and $+40\text{V}$ on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve “Input Bias Current vs Common-Mode Input Voltage” shows this input current limit behavior. The inputs are protected even if the power supply voltage is zero.

OTHER APPLICATIONS

See the INA114 data sheet for other applications circuits of general interest.

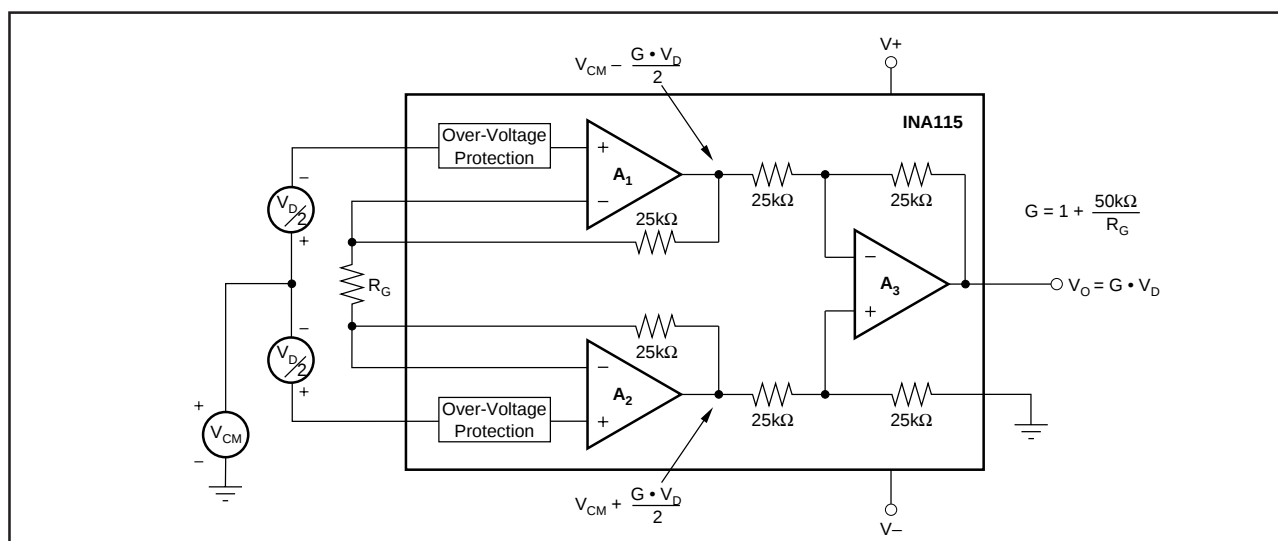


FIGURE 6. Voltage Swing of A_1 and A_2 .

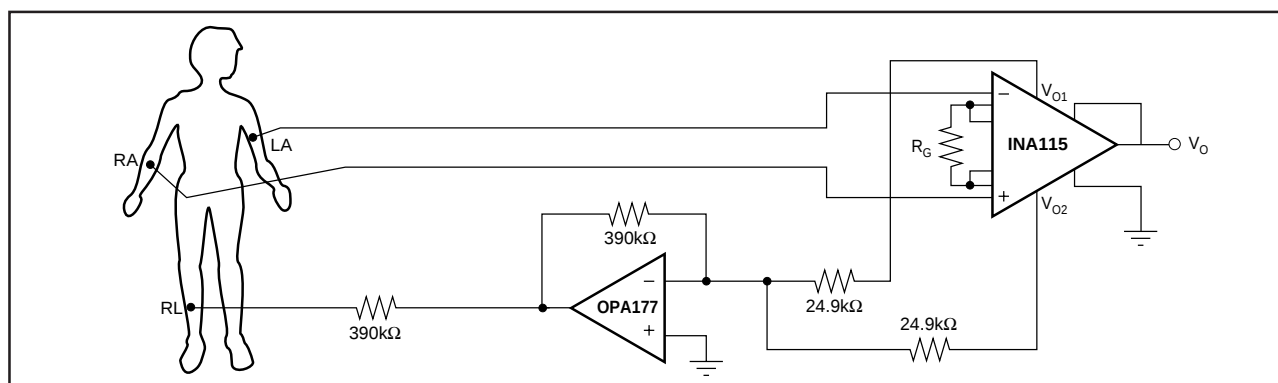


FIGURE 7. ECG Amplifier with Right Leg Drive.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA115AU	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	INA115AU
INA115AU.A	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	INA115AU
INA115AU/1K	Active	Production	SOIC (DW) 16	1000 LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-	INA115AU
INA115AU/1K.A	Active	Production	SOIC (DW) 16	1000 LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	INA115AU
INA115BU	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAUAG	Level-3-260C-168 HR	-	INA115BU
INA115BU.A	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	INA115BU

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA115AU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA115AU/1K	SOIC	DW	16	1000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA115AU	DW	SOIC	16	40	507	12.83	5080	6.6
INA115AU.A	DW	SOIC	16	40	507	12.83	5080	6.6
INA115BU	DW	SOIC	16	40	507	12.83	5080	6.6
INA115BU.A	DW	SOIC	16	40	507	12.83	5080	6.6

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated