拡張 I/O を備えた、FPC202 デュアル・ポート・コントローラ

1 特長

- 2 つのポートにわたる制御信号管理と I2C 集約に対応
- 各ポートで 4 つの LED ドライバと 12 の汎用 I/O
- 汎用出力を使用してポートあたり 5 つ以上の LED を駆動可能
- 複数の FPC202 を組み合わせることにより、合計 28 のポートを単一のホスト・インターフェイスから制御可能
- 別個の I2C マルチプレクサ、LED ドライバ、ピン数の多い FPGA/CPLD 制御デバイスが不要
- すべての低速制御信号をポートの近くで処理するため、PCB の配線の複雑性を低減
- I2C (最高 1MHz) または SPI (最高 10MHz) のホスト制御インターフェイスを選択可能
- 重要なユーザー指定のデータをモジュールから自動的にプリフェッチ
- ブロードキャスト・モードにより、すべての FPC202 コントローラにわたってすべてのポートへ同時に書き込み可能
- 先進の LED 機能によるポート・ステータスの表示、点滅や調光もプログラム可能
- 割り込みイベントをカスタマイズ可能
- 独立したホスト側 I/O 電圧：1.8V～3.3V
- 小型の QFN パッケージにより、PCB の裏側でポートの下に配置可能

2 アプリケーション

- ToR / 集約 / コア スイッチおよびルータ
- ワイヤレス インフラストラクチャのベースバンド ユニットおよびリモート ラジオ ユニット
- ネットワーク インターフェイス カード (NIC) およびホスト バス アダプタ (HBA)
- ストレージ カードおよびストレージ ラック
- SFP、QSFP、QSFP-DD、OSFP、Mini-SAS HD ポートの管理

3 概要

FPC202 デュアル ポート コントローラは、SFP、QSFP、Mini-SAS HD など一般的なポート タイプ用の低速信号アグリゲータとして機能します。FPC202 は 2 つのポートの低速制御信号および I2C 信号をすべて集約し、使いやすい単一の管理インターフェイスをホストに提供します (I2C または SPI)。複数の FPC202 を使用すると、ホストに対する 1 つの共通の制御インターフェイスを備えたポート数の多いアプリケーションが実現できます。

FPC202 は PCB の裏側でプレスフィット コネクタの下に配置できるよう設計されているため、配線が簡単に行えます。ポートの低速信号を、この局所化された方法で制御することにより、I/O 数の少ない制御デバイス (FPGA、CPLD、MCU) を使用でき、配線レイヤの密度が低減されるため、システムの BOM コストを削減できます。

FPC202 は標準の SFF-8431、SFF-8436、SFF-8449 低速管理インターフェイスに準拠しており、各ポートに専用の 100/400kHz I2C インターフェイスが搭載されています。ポート ステータス LED の駆動や電源スイッチの制御などの機能を実行するため、追加の汎用ピンも利用可能です。LED ドライバは、点滅や調光のプログラムなどの便利な機能を備えています。ホスト コントローラへのインターフェイスは、低電圧の I/O をサポートするために 1.8V～3.3V の独立電源で動作できます。

各ポートは、合計 4 つの LED ドライバ、12 の汎用 I/O、2 つのダウンストリーム I2C バスを備えています。この拡張 I/O セットにより、追加部品やシステム内機能の制御が可能になります。1 ポートにつき 4 つを超える LED が必要な場合は、汎用出力を使用して追加 LED を駆動できます。

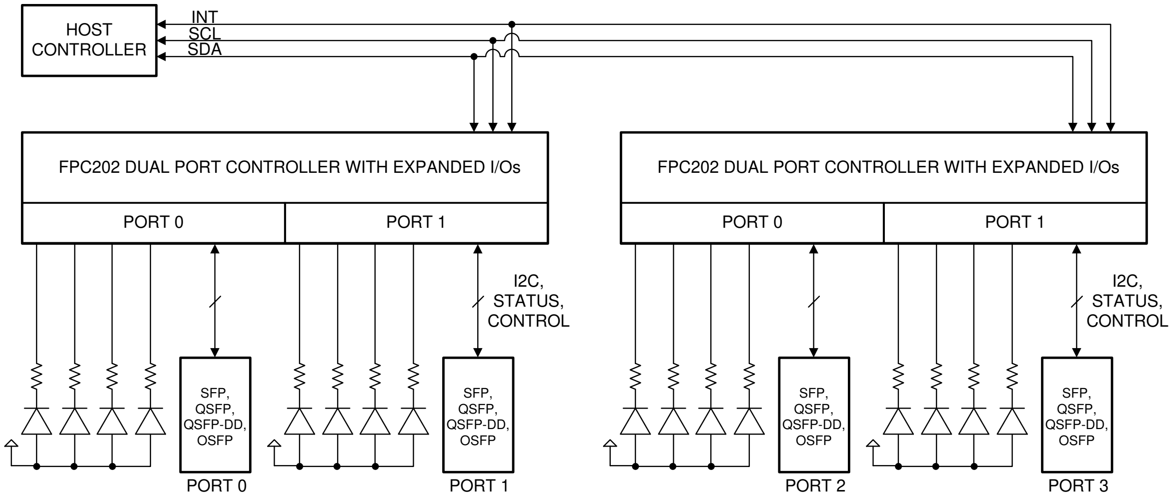
FPC202 は各モジュールでユーザーが指定したレジスタからデータをプリフェッチできるため、ホストは高速な I2C (最高 1MHz) または SPI (最高 10MHz) インターフェイスでデータへすぐにアクセスできます。さらに、FPC202 は制御下のポートのいずれかに関連する重要な、ユーザー構成可能なイベントが発生した場合、ホストへの割り込みをトリガできます。このため、モジュールを継続的にポーリングする必要はありません。

パッケージ情報

部品番号(1)	パッケージ(2)	パッケージ サイズ(3)
FPC202	RHU (WQFN、56)	11 mm × 5 mm

(1) 製品比較表を参照してください。
(2) 詳細は、セクション 11 を参照してください。
(3) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。



概略ブロック図

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4 Device Comparison Table

PART NUMBER	PORTS	LED DRIVERS PER PORT	GPIOs PER PORT	ACCESSIBLE DOWNSTREAM ADDRESSES
FPC202	2	4	12	All valid I2C addresses
FPC402	4	2	6	All valid I2C addresses
FPC401	4	2	6	MSA addresses: 0xA0, 0xA2

5 Pin Configuration and Functions

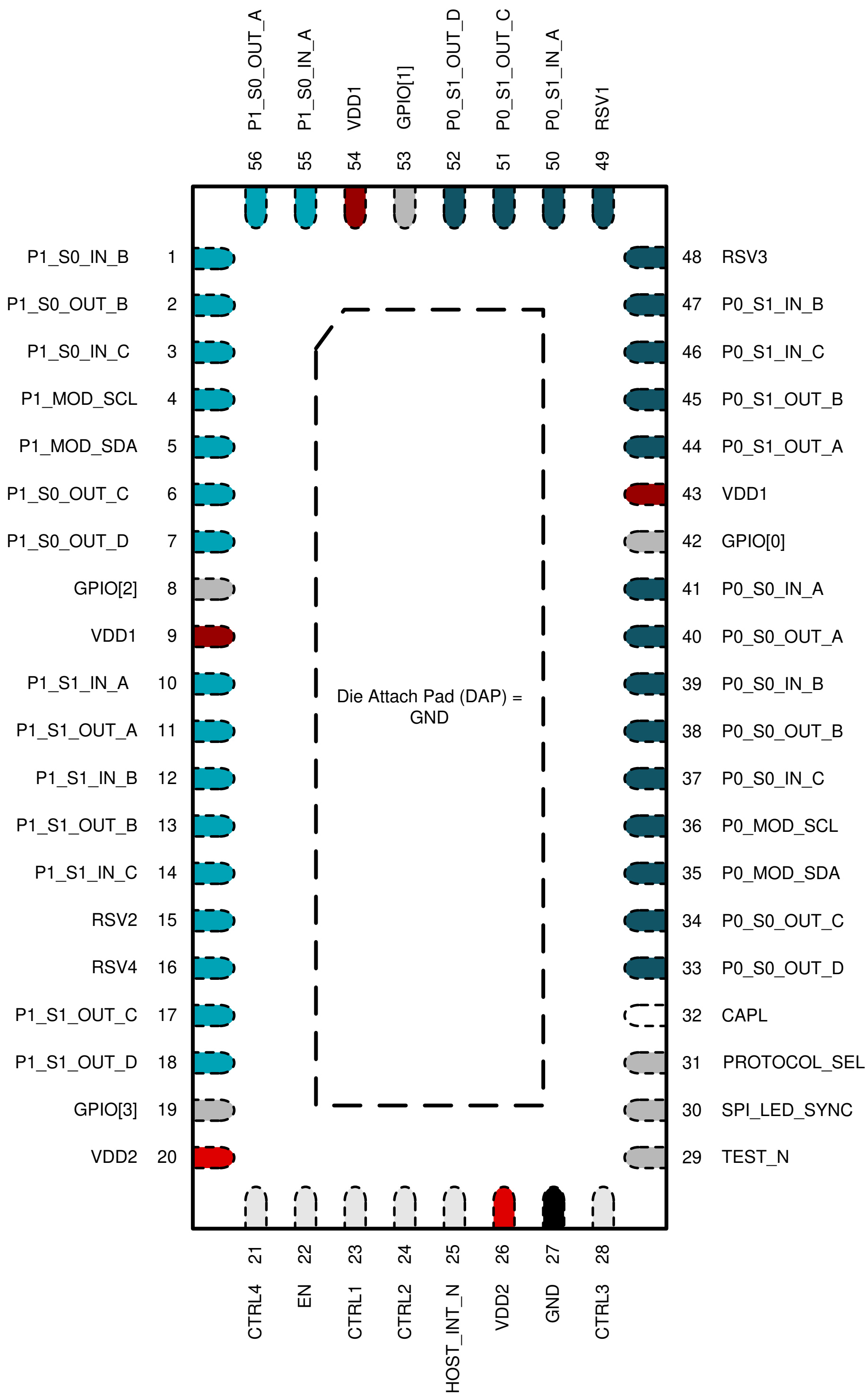

図 5-1. RHU Package, 56-Pin QFN (Top View)

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表 5-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
CAPL	32	O	Connect a single 2.2-µF capacitor to GND.
CTRL1	23	I/O	Host-side control interface. These pins are used to implement I2C or SPI depending on the PROTOCOL_SEL pin configuration. I2C mode (PROTOCOL_SEL = Float or High): CTRL1: SCL – I2C Clock input / open-drain output CTRL2: SDA – I2C Data input / open-drain output CTRL3: SET_ADDR_N – input, address assignment enable. Also used to receive external LED clock. CTRL4: ADDR_DONE_N – output, address assignment complete. Also used to transmit LED clock. SPI mode (PROTOCOL_SEL = GND): CTRL1: SCK – Serial clock input CTRL2: SS_N – Active-low slave select input CTRL3: MOSI – Master output/ slave input CTRL4: MISO – Master input / slave output
CTRL2	24	I/O	
CTRL3	28	I, Weak internal pull-up	
CTRL4	21	O	
EN	22	VDD2 I, Weak internal pull-up	Device enable. When EN=0, the FPC202 is in a power-down state and does not respond to the host-side control bus, nor does it perform port-side I2C accesses. When EN=VDD2 or Float, the FPC202 is fully enabled and will respond to the host-side control bus provided VDD1 and VDD2 power has been stable for at least T_{POR}. V_{IH} for this pin is referenced to VDD2. The minimum required assert and de-assert time is 12.5 µs.
GPIO[0]	42	VDD1 I/O	General-purpose I/O. Output high voltage (V_{OH}) and input high voltage (V_{IH}) are based on VDD1. Configured as input (high-Z) by default.
GPIO[1]	53		
GPIO[2]	8		
GPIO[3]	19		
GND	27, DAP	Power	Ground reference. The GND pins should be connected through a low-resistance path to the board GND plane.
HOST_INT_N	25	VDD1/VDD2 O, Open-Drain	Open-drain 3.3-V tolerant active-low interrupt output. It asserts low to interrupt the host. The events which trigger an interrupt are programmable through registers. This pin can be connected in a wired-OR fashion with other FPC202s' interrupt pins. A single pull-up resistor to VDD1 or VDD2 in the 2-kΩ to 5-kΩ range is adequate for the entire net.
P0_S0_IN_A	41	I, Weak internal pull-up	Low-speed port status input A. Example usage: SFP: Mod_ABS[1:0] QSFP: ModPrsL[1:0]
P1_S0_IN_A	55		
P0_S0_IN_B	39	I, Weak internal pull-up	Low-speed port status input B. Example usage: SFP: Tx_Fault[1:0] QSFP: IntL[1:0]
P1_S0_IN_B	1		
P0_S0_IN_C	37	I, Weak internal pull-up	Low-speed port status input C. Example usage: SFP: Rx_LOS[1:0] QSFP: N/A
P1_S0_IN_C	3		

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表 5-1. Pin Functions (続き)

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
P0_S1_IN_A	50	VDD1 I, Weak internal pull-up	General-purpose inputs. Input high voltage (V_{IH}) is based on VDD1.
P1_S1_IN_A	10		
P0_S1_IN_B	47		
P1_S1_IN_B	12		
P0_S1_IN_C	46		
P1_S1_IN_C	14		
P0_MOD_SCL	36	I/O, Open-Drain	I2C clock open-drain output to the module. External 2-kΩ to 5-kΩ pull-up resistor is required. This pin is 3.3-V LVCMOS tolerant.
P1_MOD_SCL	4		
P0_MOD_SDA	35	I/O, Open-Drain	I2C data input / open-drain output to the module. External 2-kΩ to 5-kΩ pull-up resistor is required. This pin is 3.3-V LVCMOS tolerant.
P1_MOD_SDA	5		
RSV1	49	I/O	Reserved. Must be left as no connect.
RSV2	15		
RSV3	48		
RSV4	16		
P0_S0_OUT_A	40	O	Low-speed port control output A. OUT_A is disabled by default (high-Z) and when enabled drives high logic unless reprogrammed. A 10-kΩ pull-up or pull-down resistor is recommended to set a default logic value before this output is enabled. See *セクション 7.3.3* for more details. Example usage: SFP: Tx_Disable[1:0] QSFP: ResetL[1:0]
P1_S0_OUT_A	56		
P0_S0_OUT_B	38	O	Low-speed port control output B. Output is disabled by default (high-Z) and when enabled drives low logic unless reprogrammed. A 10-kΩ pull-up or pull-down resistor is recommended to set a default logic value before this output is enabled. See *セクション 7.3.3* for more details. Example usage: SFP: RS[1:0] QSFP: LPMode[1:0]
P1_S0_OUT_B	2		
P0_S0_OUT_C	34	O	General-purpose outputs with special LED driving features for automatic blinking and dimming. Can be used to drive port status LED. This output is enabled and high logic by default at power-up. See *セクション 7.3.2* for more details. This pin requires a series resistor with a value of at least 33 Ω when driving an LED.
P1_S0_OUT_C	6		
P0_S0_OUT_D	33		
P1_S0_OUT_D	7		

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表 5-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
P0_S1_OUT_A	44	VDD1 O	General-purpose outputs. Output high voltage (V_{OH}) is based on VDD1.
P1_S1_OUT_A	11		
P0_S1_OUT_B	45		
P1_S1_OUT_B	13		
P0_S1_OUT_C	51	O	General-purpose outputs with special LED driving features for automatic blinking and dimming. Can be used to drive port status LED. This output is enabled and high logic by default at power-up. See *セクション 7.3.2* for more details. This pin requires a series resistor with a value of at least 33 Ω when driving an LED.
P1_S1_OUT_C	17		
P0_S1_OUT_D	52		
P1_S1_OUT_D	18		
PROTOCOL_SEL	31	I, Weak internal pull-up	Used to select between I2C and SPI host-side control interface. Float or High: Inter-IC Control (I2C) GND: Serial Peripheral Interface (SPI)
SPI_LED_SYNC	30	I/O	LED clock synchronization pin for SPI mode only. When using SPI as the host-side control interface (PROTOCOL_SEL=GND), connect all FPC202 SPI_LED_SYNC pins together. This ensures LED synchronization across all FPC202 devices. When using I2C as the host-side control interface, this pin can be floating. LED synchronization is ensured by other means in I2C mode.
TEST_N	29	I, Weak internal pull-up	TI test mode. Float or High: Normal operation GND: TI Test Mode
VDD1	9, 43, 54	Power	Main power supply, VDD1 = 3.3 V ± 5%. TI recommends connecting at least one 1-µF and one 0.1-µF de-coupling capacitors per VDD1 pin as close to the pin as possible.
VDD2	20, 26	Power	Power supply for host-side interface I/Os (CTRL[4:1]). VDD2 can be 1.8 V to 3.3 V ± 5%. If the host-side interface operates at 3.3 V, then VDD1 and VDD2 can be connected to the same 3.3-V ± 5% supply. TI recommends connecting at least one 1-µF and one 0.1-µF de-coupling capacitors per VDD2 pin as close to the pin as possible.

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
$VDD1_{ABSMAX}$	Supply voltage (VDD1)	–0.5	5	V
$VDD2_{ABSMAX}$	Supply voltage (VDD2)	–0.5	5	V
$VIO_{VDD1,ABSMAX}$	3.3-V LVCMOS I/O voltage (All pins except CTRL[4:1] and EN)	–0.5	5	V
$VIO_{VDD2,ABSMAX}$	VDD2 LVCMOS I/O voltage (CTRL[4:1] and EN pins only)	–0.5	5	V
$T_{J,ABSMAX}$	Junction temperature		150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
VDD1	Supply voltage, VDD1 to GND. DC plus AC power should not exceed these limits.	3.135	3.3	3.465	V
VDD2	Host-side interface supply voltage, VDD2 to GND. 1.8 to 3.3 V typical. DC plus AC power should not exceed these limits.	1.710	1.8, 2.5, 3.3	3.465	V
$t_{Ramp\text{-}VDD1}$	VDD1 supply ramp time, from 0 V to 3.135 V	1			ms
$t_{Ramp\text{-}VDD2}$	VDD2 supply ramp time, from 0 V to VDD2 – 5%	1			ms
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

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6.4 Thermal Information

THERMAL METRIC[(1)]		FPC202 RHU (QFN) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	6.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = -40 °C to 125 °C, VDD1 = 3.3 V ± 5%, VDD2 = 3.3 V ± 5% (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
W_{TOTAL}	Total device power dissipation	VDD1 = VDD2 = 3.3 V, Outputs sourcing maximum current; S0_OUT_C, S0_OUT_D, S1_OUT_C, and S1_OUT_D are OFF (V_{out} = High)		90	110	mW
		VDD1 = 3.3 V, VDD2 = 2.5 V, Outputs sourcing maximum current; S0_OUT_C, S0_OUT_D, S1_OUT_C, and S1_OUT_D are OFF (V_{out} = High)		100	110	mW
		VDD1 = 3.3 V, VDD2 = 1.8 V, Outputs sourcing maximum current; S0_OUT_C, S0_OUT_D, S1_OUT_C, and S1_OUT_D are OFF (V_{out} = High)		100	120	mW
I_{VDD1}	Current consumption for VDD1 supply	VDD1 = VDD2 = 3.3 V; S0_OUT_C, S0_OUT_D, S1_OUT_C, and S1_OUT_D are OFF (V_{out} = High)		26	31	mA
		VDD1 = VDD2 = 2.5 V; S0_OUT_C, S0_OUT_D, S1_OUT_C, and S1_OUT_D are OFF (V_{out} = High)		27	32	
		VDD1 = 3.3 V, VDD2 = 1.8 V; S0_OUT_C, S0_OUT_D, S1_OUT_C, and S1_OUT_D are OFF (V_{out} = High)		29	34	mA

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6.5 Electrical Characteristics (続き)

T_J = -40 °C to 125 °C, VDD1 = 3.3 V ± 5%, VDD2 = 3.3 V ± 5% (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD2}	Current consumption for VDD2 supply	VDD1 = VDD2 = 3.3 V, Outputs sourcing maximum current; S0_OUT_C, S0_OUT_D, S1_OUT_C, and S1_OUT_D are OFF (V_{out} = High)		0.2	0.35	mA
		VDD1 = 3.3 V, VDD2 = 2.5 V, Outputs sourcing maximum current; S0_OUT_C, S0_OUT_D, S1_OUT_C, and S1_OUT_D are OFF (V_{out} = High)		0.1	0.3	mA
		VDD1 = 3.3 V, VDD2 = 1.8 V, Outputs sourcing maximum current; S0_OUT_C, S0_OUT_D, S1_OUT_C, and S1_OUT_D are OFF (V_{out} = High)		0.1	0.25	mA
$I_{total-idle}$	Total device supply current consumption in idle mode				6.5	mA
LVCMOS I/O DC SPECIFICATIONS						
V_{IH}	High level input voltage	Applies to S0_IN_A, S0_IN_B, S0_IN_C, S1_IN_A, S1_IN_B, S1_IN_C, PROTOCOL_SEL, and GPIO[3:0]	2.0		3.465	V
		Applies to EN	0.7* VDD2		VDD2	
V_{IL}	Low level input voltage	Applies to S0_IN_A, S0_IN_B, S0_IN_C, S1_IN_A, S1_IN_B, S1_IN_C, PROTOCOL_SEL, GPIO[3:0], and EN	–0.3		0.8	V
V_{OH}	High level output voltage	Applies to S0_OUT_A, S0_OUT_B, and GPIO[3:0], I_{OH} = –2 mA	2.8		3.465	V
		Applies to S0_OUT_C, S0_OUT_D, S1_OUT_C, and S1_OUT_D, I_{OH} = –50 µA	2.5			
V_{OL}	Low level output voltage	Applies to S0_OUT_A, S0_OUT_B, and GPIO[3:0], I_{OL} = 2 mA	GND		0.4	V
		Applies to S0_OUT_C, S0_OUT_D, S1_OUT_C, and S1_OUT_D, I_{OL} = 18 mA	GND		0.4	
I_{IH}	High level input current	Applies to S0_IN_A, S0_IN_B, S0_IN_C, S1_IN_A, S1_IN_B, S1_IN_C, and GPIO[3:0]	–1		1	µA
I_{IL}	Low level input current	Applies to S0_IN_A, S0_IN_B, S0_IN_C, S1_IN_A, S1_IN_B, S1_IN_C	–220		–170	µA
		Applies to GPIO[3:0]	–1		1	µA
t_{SP-LS}	Pulse width of spikes that are suppressed by FPC202 input de-glitch filter on all IN_* low-speed pins	Pulses shorter than min are suppressed, and pulses longer than the max are not suppressed.	30		50	µs
DOWNSTREAM MASTER I2C ELECTRICAL CHARACTERISTICS (MOD_SCL AND MOD_SDA)						
V_{OL}	Low level output voltage	I_{OL} = 3 mA	GND		0.4	V
V_{IL}	Low level input voltage		–0.3		1.04	V
V_{IH}	High level input voltage		2.19		3.465	V
C_b (1)	I2C bus capacitive load	1.6 kΩ pull-up resistor max			200	pF
HOST-SIDE I2C ELECTRICAL CHARACTERISTICS (PROTOCOL_SEL=FLOAT/HIGH)						

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6.5 Electrical Characteristics (続き)

T_J = -40 °C to 125 °C, VDD1 = 3.3 V ± 5%, VDD2 = 3.3 V ± 5% (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high level voltage	SDA (CTRL2) and SCL (CTRL1)	0.7* VDD2		VDD2	V
V_{IL}	Input low level voltage	SDA (CTRL2) and SCL (CTRL1)			0.3* VDD2	V
C_{IN} (1)	Input pin capacitance	SDA (CTRL2) and SCL (CTRL1)		0.5	1	pF
V_{OL}	Low level output voltage	SDA (CTRL2) or SCL (CTRL1), IOL = 3 mA	GND		0.4	V
I_L	IL Leakage current	SDA (CTRL2) or SCL (CTRL1), VIN = VDD2	–1		1	µA
C_b (1)	I2C bus capacitive load				550	pF
HOST-SIDE SPI ELECTRICAL CHARACTERISTICS (PROTOCOL_SEL=GND)						
V_{IH}	Input high level voltage	SCK (CTRL1), SS_N (CTRL2), and MOSI (CTRL3)	0.7* VDD2			V
V_{IL}	Input low level voltage	SCK (CTRL1), SS_N (CTRL2), and MOSI (CTRL3)			0.3* VDD2	V
C_{IN} (1)	Input pin capacitance	SCK (CTRL1), SS_N (CTRL2), and MOSI (CTRL3)		0.5	1	pF
V_{OH}	High level output voltage	MISO (CTRL4) pin, IOH = –4 mA	0.7* VDD2			V
V_{OL}	Low level output voltage	MISO (CTRL4) pin, IOL = 4 mA	GND		0.4	V
I_L	Leakage current	MOSI (CTRL3)	–220		–170	µA
		SCK (CTRL1), SS_N (CTRL2), and MISO (CTRL4)	–1		1	µA
C_{MISO} (1)	MISO output capacitive load	MISO (CTRL4) pin			50	pF

(1) These parameters are not production tested.

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
GENERAL TIMING REQUIREMENTS						
T_{POR}	Internal power-on reset (PoR) time	Time between stable VDD1 power supply (VDD1 ≥ 3.3V - 5%) and de-assertion of internal PoR. The port-side and host-side control interfaces (I2C and/or SPI) are not operational during this time.	30		50	ms
HOST-SIDE SPI TIMING REQUIREMENTS (PROTOCOL_SEL =GND) (1) (2)						
f_{SPI}			0.1		10	MHz
$t_{HI\text{-}SCK}$				0.4 ÷ f_{SPI}		ns
$t_{LO\text{-}SCK}$				0.4 ÷ f_{SPI}		ns
$t_{HD\text{-}MOSI}$				1		ns
$t_{SU\text{-}MOSI}$				1		ns
$t_{HD\text{-}SSN}$				4		ns
$t_{SU\text{-}SSN}$				1.2		ns
$t_{OFF\text{-}SSN}$		For writes and local FPC202 register reads		1		
		For consecutive downstream (remote) register reads on the same port, assuming 400 KHz I2C		170		µs
		For consecutive downstream (remote) register reads on the same port, assuming 100 KHz I2C		620		
$t_{ODZ\text{-}MISO}$	MISO (CTRL4) driven-to-TRI_STATE time			32		ns
$t_{OZD\text{-}MISO}$	MISO (CTRL4) TRI_STATE-to-driven time			10		ns
t_{OD}	MISO (CTRL4) output delay time			15		ns
HOST-SIDE I2C TIMING REQUIREMENTS (PROTOCOL_SEL=FLOAT OR HIGH) (2) (3) (4)						
f_{SCL}	Host-side I2C clock frequency (CTRL1) in I2C mode		100		1000	kHz
t_{BUF}	Bus free time between STOP and START condition		0.5			µs
$t_{HD\text{-}STA}$	Hold time after (repeated) START condition. After this period, the first clock is generated.	After this period, the first clock can be generated by the master.	0.3			µs
$t_{SU\text{-}STA}$	Repeated START condition setup time		0.3			µs
$t_{SU\text{-}STO}$	STOP condition setup time		0.3			µs
$t_{HD\text{-}DAT}$	SDA (CTRL2) hold time		32			ns
$t_{SU\text{-}DAT}$	SDA (CTRL2) setup time	Applies to standard-mode I2C, 100 kHz	250			ns
	SDA (CTRL2) setup time	Applies to fast-mode I2C, 400 kHz	100			ns
	SDA (CTRL2) setup time	Applies to fast-mode plus I2C, 1000 kHz	50			ns
t_{LOW}	SCL (CTRL1) clock low time		0.5			µs
t_{HIGH}	SCL (CTRL1) clock high time		0.3			µs

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6.6 Timing Requirements (続き)

			MIN	NOM	MAX	UNIT
t_R	SDA (CTRL2) rise time, read	Applies to standard-mode I2C, 100 kHz			1000	ns
	SDA (CTRL2) rise time, read	Applies to fast-mode I2C, 400 kHz	20		300	ns
	SDA (CTRL2) rise time, read	Applies to fast-mode plus I2C, 1000 kHz			120	ns
t_F	SDA (CTRL2) fall time, read	Applies to standard-mode I2C, 100 kHz			300	ns
	SDA (CTRL2) fall time, read	Applies to fast-mode I2C, 400 kHz	4.4		300	ns
	SDA (CTRL2) fall time, read	Applies to fast-mode plus I2C, 1000 kHz	4.4		120	ns

(1) SPI operation is available T_{POR} milliseconds after VDD1 power up, provided EN = high or float and VDD2 is stable.
(2) These parameters are not production tested.
(3) I2C operation is available T_{POR} milliseconds after VDD1 power up, provided EN = high or float and VDD2 is stable.
(4) These specifications support I2C Rev 6 specifications

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DOWNSTREAM MASTER I2C SWITCHING CHARACTERISTICS						
f_{SCL}	SCL clock frequency	Applies to standard-mode I2C, 100 kHz	66	83	100	kHz
		Applies to fast-mode I2C, 400 kHz	264	332	400	kHz
$t_{LOW-SCL}$	SCL clock pulse width low period		1.3			µs
$t_{HIGH-SCL}$	SCL clock pulse width high period		0.6			µs
t_{BUF}	Time bus free before new transmission starts	Between STOP and START and between ACK and RESTART	20			µs
t_{HD-STA}	Hold time START operation		0.6			µs
t_{SU-STA}	Setup time START operation		0.6			µs
t_{HD-DAT}	Data hold time		0			µs
t_{SU-DAT}	Data setup time		0			µs
t_R	SCL and SDA rise time	100 KHz operation. From V_{IL} (Max) - 0.15 V to V_{IH} (Min) + 0.15 V.			300	ns
	SCL and SDA rise time	100 KHz operation. From V_{IL} (Max) - 0.15 V to V_{IH} (Min) + 0.15 V.			300	
t_F	SCL and SDA fall time	100 KHz operation. From V_{IH} (Min) + 0.15 V to V_{IL} (Max) - 0.15 V.			300	ns
	SCL and SDA fall time	400 KHz operation. From V_{IH} (Min) + 0.15 V to V_{IL} (Max) - 0.15 V.			300	
t_{SU-STO}	STOP condition setup time		0.6			µs
t_{SP-I2C} (1)	Pulse width of spikes that are suppressed by FPC202 input filter		0		50	ns

(1) These parameters are not production tested.

6.8 Typical Characteristics

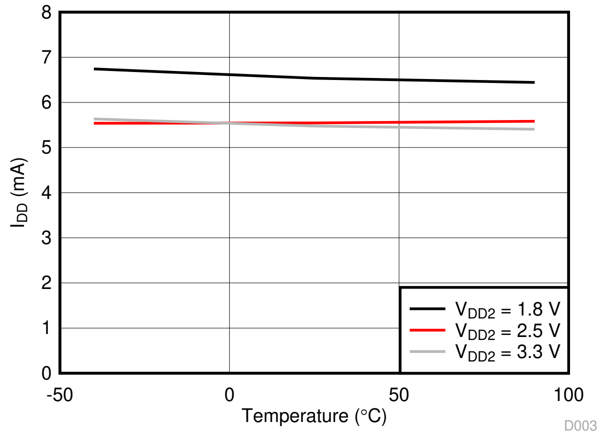

図 6-1. Static IDD1 vs. Ambient Temperature

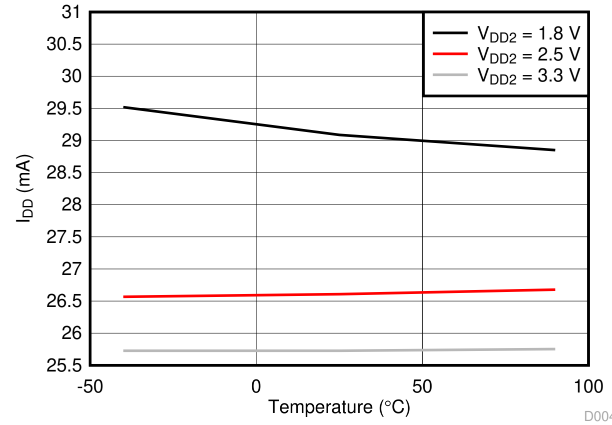

図 6-2. Dynamic IDD1 vs. Ambient Temperature

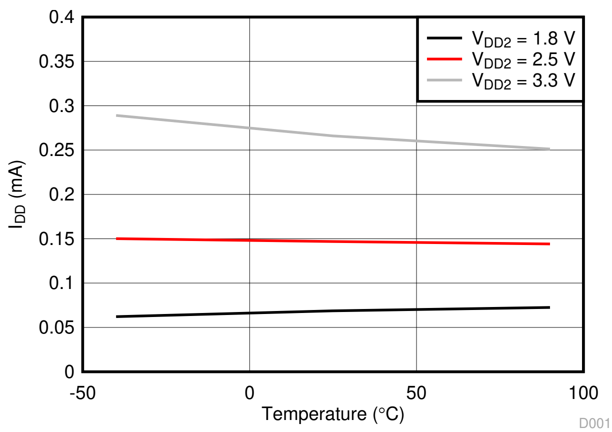

図 6-3. Static IDD2 vs. Ambient Temperature

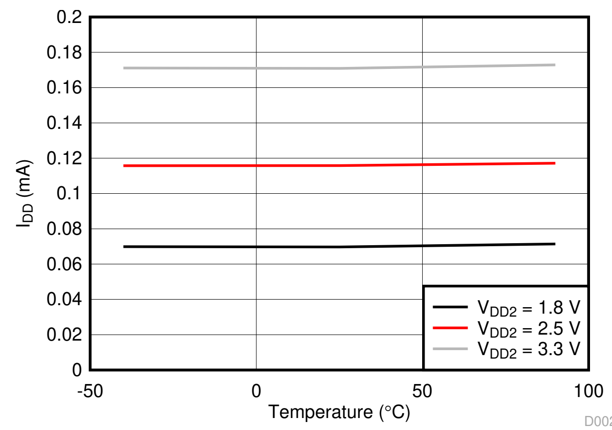

図 6-4. Dynamic IDD2 vs. Ambient Temperature

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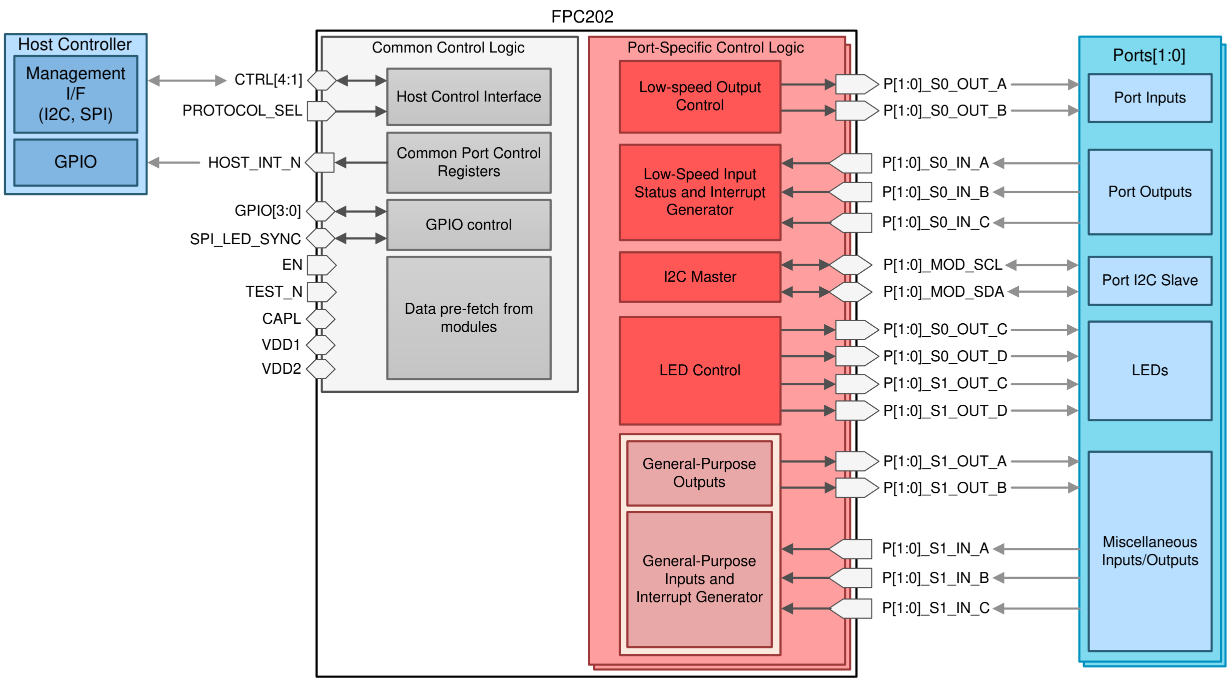
7 Detailed Description

7.1 Overview

The FPC202 is designed to interface with two ports and aggregate the I2C and low-speed control and status signals associated with these ports into a single host-side interface (I2C or SPI). Multiple FPC202s can be combined to support up to 28 total ports, all of which are controlled through the same host-side interface. This greatly reduces the number of signals which route to the host controller, saving valuable I/O resources, board routing space, and bill of materials (BOM) cost.

Functionally, the FPC202 is organized as shown in *セクション 7.2*. Two types of host-side control interfaces are supported (I2C and SPI) for controlling and monitoring the downstream ports. The FPC202 has four special outputs per downstream port (S0_OUT_C, S0_OUT_D, S1_OUT_C, and S1_OUT_D) which can be used to drive port status LEDs.

7.2 Functional Block Diagram



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7.3 Feature Description

The features of the FPC202 dual port controller include:

- *Host-Side Control Interface*
- *LED Control*
- *Low-Speed Output Signal Control*
- *Low-Speed Input Status and Interrupt Generation*
- *Downstream (Port-Side) I2C Master*
- *Data Pre-Fetch From Modules*
- *Scheduled Write*
- *Protocol Timeouts*
- *General-Purpose Inputs/Outputs*
- *Hot-Plug Support*

7.3.1 Host-Side Control Interface

The FPC202 has a single host-side interface which can be configured as one of two available protocols, depending on the pin strap value of the PROTOCOL_SEL pin:

- Inter-Integrated Circuit (I2C) up to 1 MHz Fast-mode Plus
- Serial Peripheral Interface (SPI) up to 10 MHz

These represent the two functional modes of operation for which the FPC202 can be configured. Refer to *セクション 7.4* for more details.

7.3.2 LED Control

The FPC202 uses four sets of outputs, P[1:0]_S0_OUT_C, P[1:0]_S0_OUT_D, P[1:0]_S1_OUT_C, and P[1:0]_S1_OUT_D to drive LEDs associated with the ports under its control. Most SFP and QSFP applications use one yellow and one green LED per port to indicate different link status such as link up, link down, and other link states. Some QSFP applications require one LED per lane, which equals four LEDs per port.

For applications requiring more than four LEDs per port, spare outputs (OUT_* and GPIO) can be used to drive additional LEDs in a mostly-static fashion. The blinking and dimming capabilities available on the S0_OUT_C, S0_OUT_D, S1_OUT_C, and S1_OUT_D pins are not available on the other FPC202 outputs.

LEDs should be connected to the FPC202 in an active-low fashion as shown in 図 7-1. When the S0_OUT_C, S0_OUT_D, S1_OUT_C, or S1_OUT_D pin drives a low voltage (V_{OL}), the LED is illuminated. When these pins drive a high voltage (V_{OH}), the LED is off. Bi-color LEDs can be connected in a similar fashion, and each LED should have its own current-limiting resistor. The current-limiting resistor value is selected by choosing the desired maximum current through the LED and the corresponding voltage drop from the LED's current vs. voltage plot. The sum of forward voltage drop of the LED, the voltage drop across the series resistor, and the maximum V_{OL} (0.5 V maximum for currents between 2 and 18 mA) is equal to the LED supply voltage. Note that S0_OUT_C, S0_OUT_D, S1_OUT_C, and S1_OUT_D are tri-stated while the device is held in reset (during POR or while the EN pin is low), and are enabled during normal operation and drive a high voltage by default.

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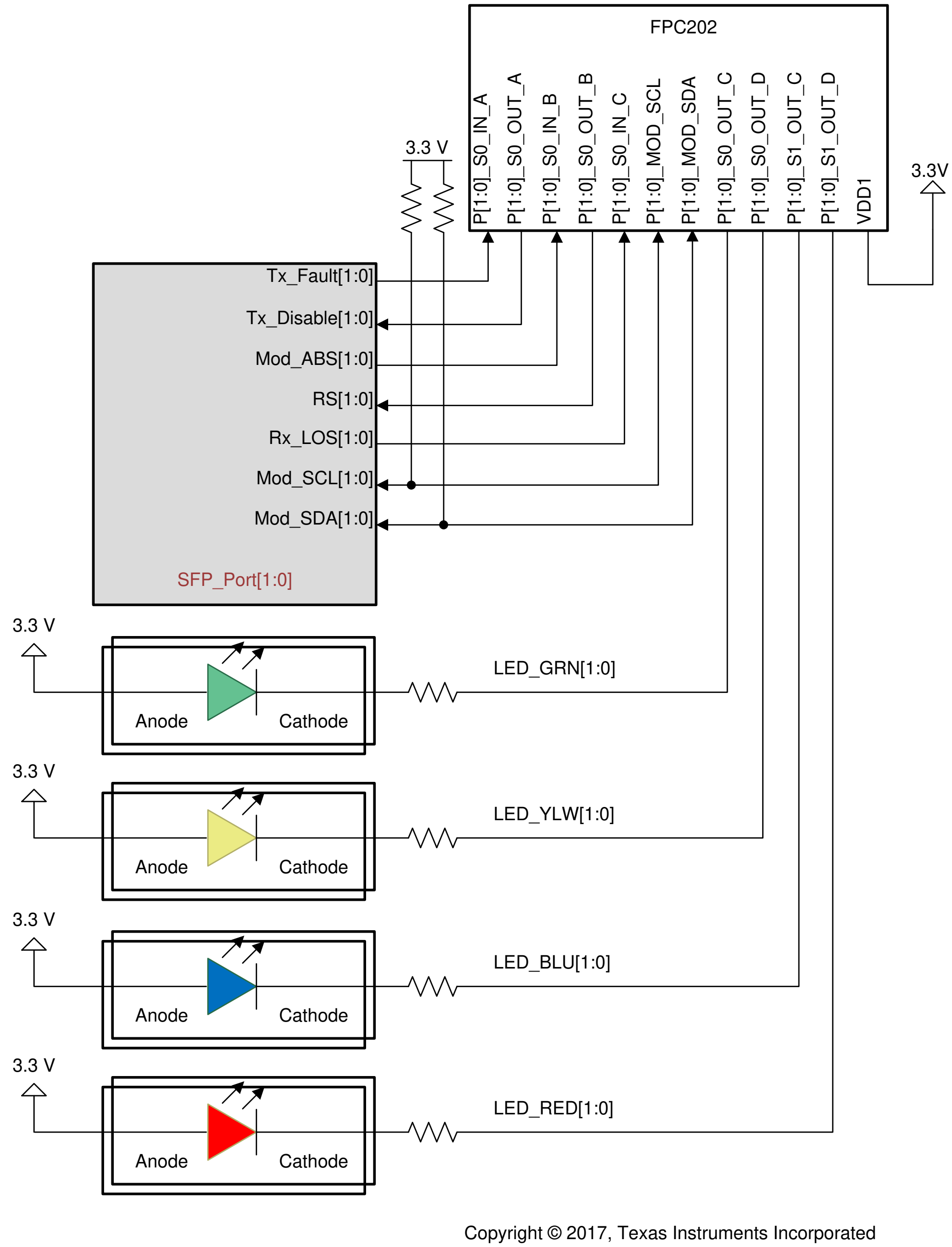

図 7-1. Example Connection Between S0_OUT_C, S0_OUT_D, S1_OUT_C, and S1_OUT_D and Active-Low LEDs

Each port under the FPC202's control has a set of registers that allow the user to configure each LED into one of the following states:

- ON
- OFF
- PWM (ON with programmable intensity)
- BLINK (with programmable blink duty cycle, frequency, and ON intensity)

LED blinking is configured by setting an on and an off time. Each of these times is configured separately and have a minimum value of 2.5 ms and a maximum value of 637.5 ms for a maximum blinking period of 1.275 seconds. The pulse width modulation (PWM) duty cycle has 256 settings where 0 is completely off, and 255 is maximum brightness. Note that the PWM is 0 by default and must be configured for the LEDs to be visible in BLINK or PWM modes.

LED blinking can be synchronized across both ports under the FPC202's control, and it can be synchronized across all ports in the system which are under the control of an FPC202. For SPI, cross-device synchronization utilizes the SPI_LED_SYNC pin. One device is configured to forward its internal LED clock to this pin, and all other devices are configured to receive an external LED clock on this pin. For I2C, the first device in the CTRL4 to CTRL3 pin daisy chain is configured to output its internal LED clock to the CTLR4 pin. All other devices are configured to receive an external LED clock from the CTRL3 pin and to output the clock to the CTRL4 pin.

7.3.2.1 Configurations with up to eight LEDs per port

In some applications it may be desirable to control more than four LEDs per port. In cases where the additional LEDs are relatively static in nature and blinking is not required, the FPC202's GPIO and unused OUT_* pins (for example, S1_OUT_A and S1_OUT_B) can be allocated for driving these LEDs in an active-low configuration. S0_OUT_C, S0_OUT_D, S1_OUT_C, and S1_OUT_D should be connected to LEDs requiring blinking and/or dimming, and up to four additional LEDs can be controlled per port from the GPIO, S1_OUT_A, and S1_OUT_B pins. 図 7-2 shows an example of how up to eight LEDs can be controlled per port.

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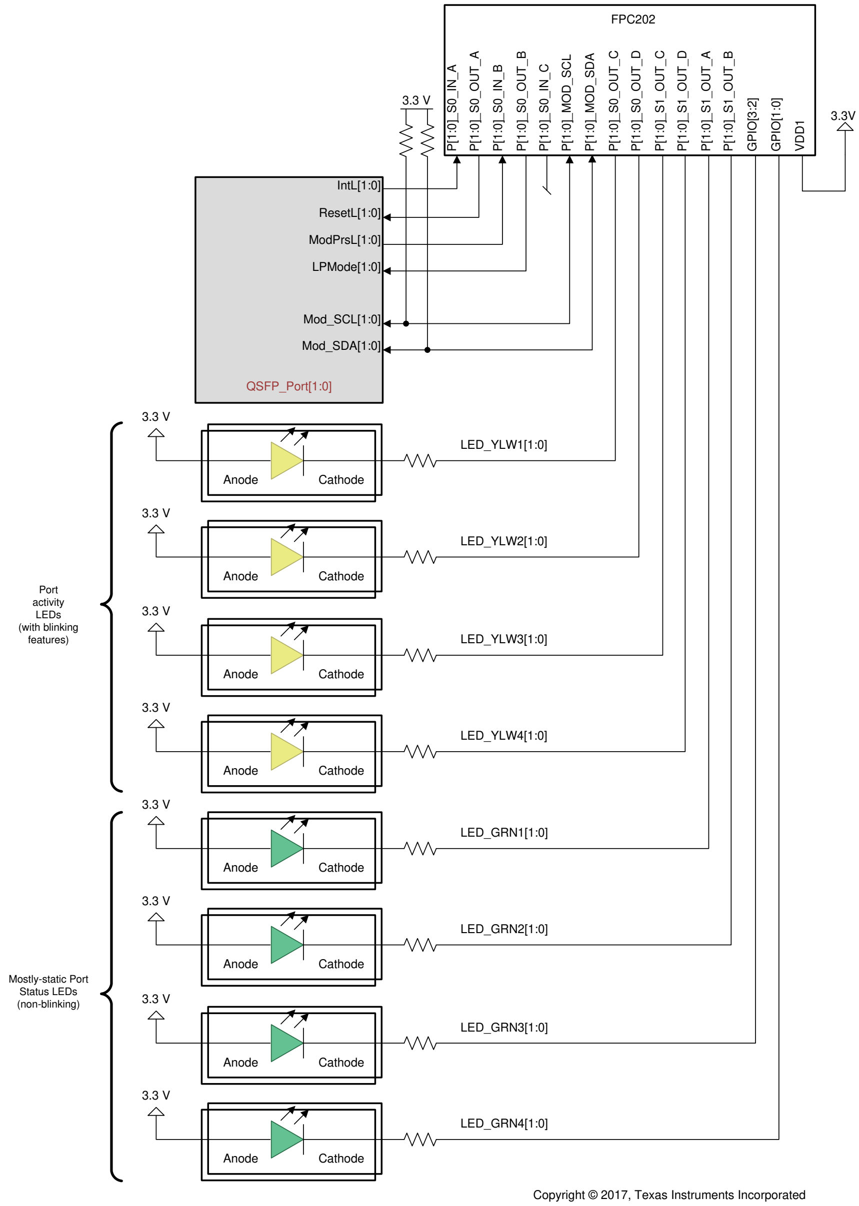

図 7-2. Example Configuration for Driving Eight LEDs Per Port

7.3.3 Low-Speed Output Signal Control

The FPC202 has four general-purpose outputs per port which can be used to drive the low-speed inputs to the module. The host controller can change the state of these outputs for each port individually, for all ports connected to a given FPC202 device simultaneously, or for all ports in the system simultaneously.

There are two configuration registers for these outputs. One register configures the enable state of the S0_OUT_A, S0_OUT_B, S1_OUT_A, and S1_OUT_B pins for every port, and by default the S0_OUT_A, S0_OUT_B, S1_OUT_A, and S1_OUT_B pins are disabled (tri-stated). The second register controls the output value for all S0_OUT_A, S0_OUT_B, S1_OUT_A, and S1_OUT_B pins, where S0_OUT_A/S1_OUT_A have default values of '1' and S0_OUT_B/S1_OUT_B have default values of '0'. The output values should be configured before the outputs are enabled. If a default value is desired during boot-up before these pins are enabled, a 10-kΩ pull-up or pull-down resistor is recommended (note that SFP and QSFP modules have internal pull-up and pull-downs on certain inputs). Note that if the VDD1 rail does not have power and there is an

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externally powered pull-up resistor connected to an output pin, the output pin will be pulled low until VDD1 is supplied.

An example signal connection is provided below. S0_OUT_A, S0_OUT_B, S1_OUT_A, and S1_OUT_B are not restricted to this port pin assignment, and they can be used to drive any 3.3-V signal required for the application, provided the I_{OH} and I_{OL} limits are met.

表 7-1. Example Connections for Low-Speed FPC202 Outputs to SFP/QSFP ports

PIN NAME	EXAMPLE CONNECTION		COMMENT
	SFP	QSFP	
S0_OUT_A	Tx_Disable	ResetL	
S0_OUT_B	RS0	LPMode	Alternatively, RS0 and RS1 be driven to the same level by using just one output.
S1_OUT_A	RS1	—	
S1_OUT_B	General-purpose output, available for any purpose		

7.3.4 Low-Speed Input Status and Interrupt Generation

The FPC202 has six general-purpose inputs per port which can be used to monitor the low-speed outputs from the module. The host controller can monitor the status of these signals for each port by reading the appropriate registers in the FPC202. In addition, the FPC202 can be configured to generate an interrupt to the host through the HOST_INT_N signal whenever one or more of the low-speed input signals change state. The interrupt can be configured to trigger on the falling edge, the rising edge, or both the falling and rising edges. A single register stores flags for which inputs and edges are responsible for the trigger.

The recommended signal connection is as follows. S0_IN_A, S0_IN_B, S0_IN_C, S1_IN_A, S1_IN_B, and S1_IN_C are not restricted to this port pin assignment, and in fact they can be used to monitor the status of any low-speed 3.3-V signal required for the application.

表 7-2. Example Connections for Low-Speed FPC202 Inputs to SFP/QSFP ports

PIN NAME	EXAMPLE CONNECTION		COMMENT
	SFP	QSFP	
S0_IN_A	Tx_Fault	IntL	
S0_IN_B	Mod_ABS	ModPrsL	
S0_IN_C	Rx_LOS	—	This pin is unused in QSFP applications, or it can be utilized as a general-purpose input.
S1_IN_A	General-purpose input, available for any purpose		
S1_IN_B	General-purpose input, available for any purpose		
S1_IN_C	General-purpose input, available for any purpose		

The events which trigger an active-low interrupt on the HOST_INT_N pin are user-configurable. Multiple FPC202s' HOST_INT_N pins can be connected together in a wired-or fashion. Interrupt generation can be configured as follows:

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表 7-3. Host-side interrupt options

INTERRUPT-TRIGGERING EVENT	PIN(S) MONITORED	EXAMPLE APPLICATION(1)
Rising edge	S0_IN_A	Indicates de-assertion of port-side interrupt (Tx_Fault or IntL).
	S0_IN_B	Indicates that a module has been removed.
	S0_IN_C	Indicates loss of optical signal (Rx_LOS) for SFP applications.
	S0_IN_A, S0_IN_B, or S0_IN_C	Indicates de-assertion of port-side interrupt, removal of module, or loss of optical signal (Rx_LOS).
	S1_IN_A	Indicates rising edge on S1_IN_A
	S1_IN_B	Indicates rising edge on S1_IN_B
	S1_IN_C	Indicates rising edge on S1_IN_C
	S1_IN_A, S1_IN_B, or S1_IN_C	Indicates rising edge on S1_IN_A, S1_IN_B, or S1_IN_C
Falling edge	S0_IN_A	Indicates assertion of port-side interrupt (Tx_Fault or IntL).
	S0_IN_B	Indicates that a module has been inserted.
	S0_IN_C	Indicates presence of optical signal (Rx_LOS) for SFP applications.
	S0_IN_A, S0_IN_B, or S0_IN_C	Indicates assertion of port-side interrupt, insertion of module, or presence of optical signal (Rx_LOS).
	S1_IN_A	Indicates falling edge on S1_IN_A
	S1_IN_B	Indicates falling edge on S1_IN_B
	S1_IN_C	Indicates falling edge on S1_IN_C
	S1_IN_A, S1_IN_B, or S1_IN_C	Indicates falling edge on S1_IN_A, S1_IN_B, or S1_IN_C
Rising or falling edge	S0_IN_A	Indicates assertion/de-assertion of port-side interrupt (Tx_Fault or IntL).
	S0_IN_B	Indicates that a module has been inserted/removed.
	S0_IN_C	Indicates presence/absence of optical signal (Rx_LOS) for SFP applications.
	S0_IN_A, S0_IN_B, or S0_IN_C	Indicates assertion/de-assertion of port-side interrupt, insertion/removal of module, or presence/absence of optical signal (Rx_LOS).
	S1_IN_A	Indicates rising/falling edge on S1_IN_A
	S1_IN_B	Indicates rising/falling edge on S1_IN_B
	S1_IN_C	Indicates rising/falling edge on S1_IN_C
	S1_IN_A, S1_IN_B, or S1_IN_C	Indicates rising/falling edge on S1_IN_A, S1_IN_B, or S1_IN_C

(1) Example applications assume that S0_IN_A, S0_IN_B, and S0_IN_C are connected to the downstream ports as per the example connection table, 表 7-2.

The FPC202 is also able to generate an interrupt based on pre-fetched data. This is known as a data-driven interrupt. The FPC202 monitors up to four bytes within the pre-fetched range for each port. For each of the bytes, the register offset address is programmed to a local FPC202 register as well as the enable bit fields which will trigger the interrupt. When one of the enabled bits of the four monitored bytes changes state from a '0' to a '1' and stays a '1' for two consecutive periodic pre-fetch cycles (0→1→1), the interrupt is generated and the periodic pre-fetch operation is halted. The FPC202 has four registers per port, which contain the sampled data from the bytes being monitored after the interrupt is triggered. To clear the interrupt, the trigger source byte's sampled data register is read. The periodic pre-fetch must be restarted after the interrupt is cleared with an I2C command. Because it takes two periodic pre-fetch cycles to trigger this interrupt, it may take up to 10 ms for the host to see the trigger after the downstream module's monitored bit field changes for the fastest periodic pre-fetch setting.

The FPC202 also has the ability to generate an interrupt if there is a mishap in the downstream I2C bus. The SDA bus and the SCL bus each have timers that will trigger an interrupt if they are held in a low state too long due to excessive clock stretching or a port error. Once the interrupt is triggered, it is cleared by issuing a port reset on the relevant port. These interrupts are known as *SCL Stuck* and *SDA Stuck* interrupts and can be configured individually for each port. By default, the *SCL Stuck* interrupt will trigger after the SCL bus is held low for 35 ms (typical). This value is configurable individually by port. The *SDA Stuck* interrupt will trigger after the SDA is held low for 1 s (typical). The user may issue a port reset sequence (9 consecutive SCL clock cycles with the last being an I2C stop condition) or module reset to restore the module to a known state.

When a host-side interrupt is triggered, the host must determine the source and cause of the interrupt. The recommended procedure for identifying the source and cause of an interrupt is as follows:

1. Read the FPC202 aggregated port interrupt flags of the first FPC202 instance to see which, if any, downstream port triggered the interrupt.
2. If this instance of the FPC202 has any aggregated port interrupts flagged, read all of the status registers to determine the source of the interrupt and clear it. If an *SCL Stuck* or *SDA Stuck* interrupt is triggered, a port reset must be issued and the periodic pre-fetch must be restarted. The host may also perform other housekeeping activities based on the interrupt, such as change the state of the LEDs after a module is no longer present.
3. Repeat steps 1 and 2 for the next FPC202 instance, until the HOST_INT_N bus is cleared.

This procedure applies to every FPC202 device which is wire-or'ed to the host-side interrupt signal. The total time required for the host to identify the source and cause of the interrupt for an implementation consisting of N total FPC202's, where all N HOST_INT_N outputs are wire-or'ed together, is as follows:

$T_{interrupt}$ = Delay between the IN_* pin changing state and the corresponding FPC202 device triggering an interrupt (50 µs max).

T_{read} = Time required to read a single register from N FPC202 devices.

For I2C mode, $T_{read} = (9*4*N)/F_{I2C}$, where F_{I2C} is the SCL clock frequency.

For SPI mode, $T_{read} = (29*2*N)/F_{SPI} + T_{OFF-SSN}$, where F_{SPI} is the SCK clock frequency, and $T_{OFF-SSN}$ is the SS_N off time.

$T_{total} = T_{interrupt} + 4*T_{read}$

表 7-4 gives some examples of T_{total} for different I2C/SPI frequencies and different values of N.

表 7-4. Example Calculations for Determining the Source and Cause of a Host-Side Interrupt

MODE	F_{I2C}	F_{SPI}	N	T_{read} (ms)	T_{total} (ms)
I2C	100 kHz	–	1	0.36	1.5
I2C	100 kHz	–	4	1.44	5.8
I2C	100 kHz	–	8	2.88	11.6
I2C	100 kHz	–	12	4.32	17.3
I2C	400 kHz	–	1	0.09	0.4

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表 7-4. Example Calculations for Determining the Source and Cause of a Host-Side Interrupt (続き)

MODE	F_{I2C}	F_{SPI}	N	T_{read} (ms)	T_{total} (ms)
I2C	400 kHz	–	4	0.36	1.5
I2C	400 kHz	–	8	0.72	2.9
I2C	400 kHz	–	12	1.08	4.4
I2C	1000 kHz	–	1	0.0036	0.1
I2C	1000 kHz	–	4	0.144	0.6
I2C	1000 kHz	–	8	0.288	1.2
I2C	1000 kHz	–	12	0.432	1.8
SPI	–	1 MHz	1	0.06	0.3
SPI	–	1 MHz	4	0.23	1.0
SPI	–	1 MHz	8	0.47	1.9
SPI	–	1 MHz	12	0.70	2.8
SPI	–	10 MHz	1	0.01	0.1
SPI	–	10 MHz	4	0.02	0.1
SPI	–	10 MHz	8	0.05	0.2
SPI	–	10 MHz	12	0.07	0.3

Request access to the *FPC202 Programmer's Guide* (SNLU229) here for more details on how to configure the interrupts.

7.3.5 Downstream (Port-Side) I2C Master

The FPC202 has two master I2C interfaces for managing up to two ports, referred to as "downstream" ports. Each downstream I2C interface can be configured to operate with an SCL clock frequency between 100 kHz and 400 kHz. The downstream I2C master supports clock stretching.

The SFF-8472 and SFF-8431 specifications define up to two logical device addresses per SFP port: 0xA0 and 0xA2. The SFF-8436 specification defines one logical device address per QSFP port: 0xA0. By default, both 0xA0 and 0xA2 are directly addressable by the upstream host controller. The directly accessible addresses may be modified through I2C writes to the FPC202 such that any valid I2C address is directly accessible. Refer to 表 7-6 (I2C) and 表 7-7 (SPI). The FPC202 uses this address mapping scheme to decode the port and device address and perform a downstream I2C read or write operation. This is known as a remote access. Remote accesses have the highest priority when accessing the downstream module. If there is an on-going periodic pre-fetch or scheduled write, these operations will be stopped at the next byte boundary and the remote access will be executed. The periodic pre-fetch or schedule write operation will be resumed after the remote access finishes. Note that the periodic pre-fetch will begin from the starting register offset of the pre-fetch range rather than where it left off during the interruption. If a remote access is attempted during an interrupt-driven pre-fetch, the interrupt-driven pre-fetch will finish and the remote access will be executed afterwards. If an autonomous access (pre-fetch or scheduled write) occurs during a remote access, the autonomous access will be executed after the remote access is completed.

All the bits of the downstream device address can be modified for direct read/write access, allowing communication with addresses 0x10, 0x20, ..., 0xE0, and 0xF0. Modified addresses cannot be used with other features such as pre-fetching and scheduled write. In SPI mode, accessing a register in the pre-fetched range from a modified address will return the pre-fetched value from the 0xA0 or 0xA2 address. To avoid this, the gate bit must be reset before attempting such an access.

7.3.6 Data Pre-Fetch From Modules

The FPC202 can be configured to pre-fetch data from each downstream port’s module. The pre-fetched data is stored locally in the FPC202's memory, allowing any downstream read operations in the pre-fetch range to be directly read from the FPC202 rather than waiting for the FPC202 to read from the downstream device through

I2C. The FPC202 can pre-fetch data from the ports on a one-time basis, a regular basis (periodic pre-fetch), or upon the occurrence of certain events (interrupt-driven pre-fetch).

For periodic pre-fetching, the period is configured in steps of 5 ms from 0 to 1.275 s, where 0 is a one-time pre-fetch. The pre-fetched range is determined by two settings, the pre-fetch length and the pre-fetch offset address. The FPC202 will pre-fetch beginning at the offset address for a length of bytes between 1 and 32. The target device address is set to either 0xA0 or 0xA2. Once configured, the start bit is set to begin periodic pre-fetching and the stop bit is set to stop pre-fetching. After a pre-fetch is completed, the gate bit is set to '0', and any attempted read operation in the pre-fetched range will return data from the FPC202's memory containing the last pre-fetched data. To modify the pre-fetched range or to stop the FPC202 from returning the data from memory, the gate bit must be reset to '1'. If the FPC202 receives a NACK during a pre-fetch attempt, the gate bit will automatically be reset. Each port has its own gate bit and separate memory and settings.

For interrupt-driven pre-fetch, the interrupt event can be configured for either the rising- or falling-edge of one of the IN_[A,B,C] input signals of a port. The pre-fetch range and target device address is configured similarly but independently of the periodic pre-fetch settings. Interrupt-driven pre-fetch also has a gate bit and memory independent of the periodic pre-fetch. Once an interrupt-driven pre-fetch occurs successfully, an interrupt is triggered on the HOST_INT_N pin and the aggregated interrupt flag for that port will be set. For the interrupt to be cleared and for another interrupt pre-fetch to occur, it must be re-armed with a register write. If the pre-fetch attempt is NACK'd, the gate bit will not be set, the interrupt will not be generated, and the interrupt-driven pre-fetch does not need to be re-armed. Note that the pre-fetched data from the interrupt-driven pre-fetch has precedence over the data from a periodic pre-fetch if they have overlapping pre-fetch ranges. The FPC202 will return data from the interrupt-driven pre-fetch even if the periodic pre-fetch data is more recent. When an interrupt-driven pre-fetch occurs, it is recommended that it is dealt with immediately by reading the pre-fetched data and re-arming it.

Request access to the *FPC202 Programmer's Guide* (SNLU229) here for more details on how to configure data pre-fetch.

7.3.7 Scheduled Write

The FPC202 has the ability to schedule a write operation on one or more downstream modules simultaneously by writing to local FPC202 registers. This operation, known as a scheduled write, allows for quicker writing by utilizing the faster host-side I2C rate. The host-side I2C bus is not held while the write occurs in the downstream I2C. This command may be broadcasted to all FPC202s to write to any combination of ports concurrently.

Scheduled writes can be directed to an individual port (port scheduled write) or to a group of two or more ports simultaneously (common scheduled write). The status of the port scheduled write or common scheduled write may be checked in a local FPC202 register. This register will reflect if the operation completed successfully, or if it was NACKed by the downstream module.

Scheduled write operations have a higher priority than periodic pre-fetch operations. This means that if a schedule write is sent while a periodic pre-fetch is on-going, the periodic pre-fetch will be stopped at the next byte boundary and the scheduled write will be executed. The periodic pre-fetch will resume on the next period. Note that it will begin reading at the start of the pre-fetch range rather than where the scheduled write occurred.

Request access to the *FPC202 Programmer's Guide* (SNLU229) here for more details on how to configure scheduled write.

7.3.8 Protocol Timeouts

The FPC202 has a watchdog timer to ensure that the I2C buses do not become permanently stuck. For example, if the host is performing a remote access on a downstream module, the FPC202 will clock stretch the host-side I2C while the downstream I2C transaction occurs. If the downstream module clock stretches for a very long time or any other error occurs that prevents the transaction from finishing, the host-side I2C will not become stuck. The watchdog timer is what prevents this from happening by setting a maximum time for the downstream transaction to complete; and if it does not complete, the timer expires and the FPC202 will NACK the host to terminate the transaction. By default, the timer is set to 3 ms and is programmable in steps of 1 ms up to 127

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ms. This timer may also be disabled, but this is not recommended as the I2C bus may become permanently stuck and a device reset will be necessary. Each port's I2C master also has a programmable watchdog timer which operates similarly to the host-side I2C watchdog timer.

When the host attempts a remote access transaction through I2C, after the I2C device ID has been ACKed, the FPC202 waits for the host to send a register offset address or a read/write command before downplaying it on the downstream port I2C. If the host becomes busy with something else and does not finish the I2C transaction, the FPC202 state machine will be stuck. There is a protocol timeout timer for each port to prevent this from happening. If the host does not finish the I2C transaction within this timer, the FPC202 will timeout and return to the idle state. This counter is 10 ms (typical) by default and is configurable in steps of 1 ms up to 255 ms.

Request access to the *FPC202 Programmer's Guide* (SNLU229) here for more details on how to configure protocol timeouts.

7.3.9 General-Purpose Inputs/Outputs

The FPC202 has multiple general purpose input/output pins which can be used to control auxiliary functions on the board through the same host-side control interface which is used to manage the ports. The GPIO pins can be configured as inputs or outputs through the FPC202 registers. One example use case for these GPIO pins is to control a power switch (for example, TPS2556 or TSP2557) to enable/disable power to the modules in order to manage power sequencing of the modules and prevent large inrush current at board power-up.

The GPIO pins and other OUT_* pins can be used with an external pull-up resistor to drive low-voltage I/Os on other devices. When used in this fashion, the GPIO/OUT_* pin would drive V_{OL} when set to logic ‘0’, and when set to high-impedance (tri-state), the pull-up resistor would pull the signal up to the appropriate I/O voltage. When using the GPIO/OUT_* pins for this purpose, it is important to drive logic ‘0’ and high-impedance only. Do not drive the pin to logic ‘1’ as it would risk damaging the I/O of the connected device.

図 7-3 shows an example configuration for using the GPIOs/OUT_* pins to drive 1.2-V I/Os on another device.

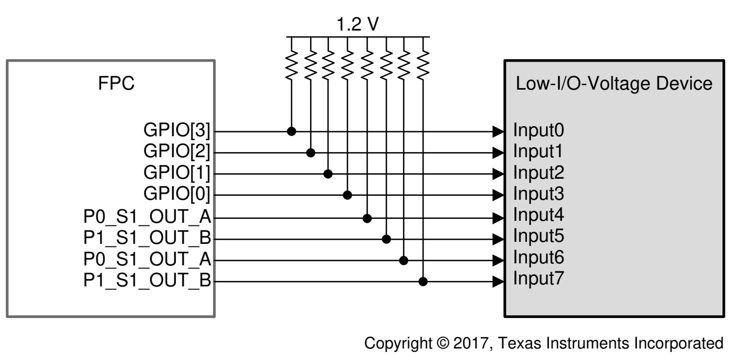

図 7-3. Example Use Of External Pull-Ups to Drive Low-I/O-Voltage Devices

The GPIO pins have a driver impedance of 10 Ω (typical). This is lower than the typical characteristic impedance of a transmission line and therefore may cause ringing due to the fast edge rate. The ringing duration is a function of the transmission line length and will typically be less than 100 ns. The magnitude of the overshoot is a function of the difference of driver impedance and impedance seen by the driver and may be as large as 5 V to GND for a transmission line with a characteristic impedance of 60 Ω. If ringing is a concern, a series resistor may be placed near the GPIO pin. A good rule of thumb for sizing the resistor is the difference of the transmission line characteristic impedance minus the driver impedance. For example, in the case of a 60 Ω transmission line impedance, a 50 Ω series resistor may be used to minimize ringing. Cases such as these may be simulated using the provided FPC202 IBIS model.

7.3.10 Hot-Plug Support

The FPC202 has features which enable it to support hot-plug applications.

- Power-on reset (PoR). The FPC202 is automatically held in reset until T_{POR} milliseconds have elapsed after VDD1 power supply is stable. The host-side control interface (I2C or SPI) should not be used prior to the completion of the PoR. Likewise, the port-side I2C interfaces are not exercised prior to the completion of the PoR.
- Enable pin (EN). When this pin is low, the FPC202 is held in reset. The host should hold this pin low until the host-side control interface (I2C or SPI) is fully connected and stable. This pin has a weak pull-up such that it can be left floating for applications which do not require hot-plug or manual enable control.
- Host-side I2C false START / false STOP tolerance. The FPC202 is designed to ignore false START and STOP conditions on the host-side I2C control interface.
- Port-side glitch suppression. The FPC202 is designed to suppress glitches from the port-side module lasting less than 30 µs (typical). This applies to all IN_* pins.

7.4 Device Functional Modes

The FPC202 has a single host-side control interface which can be configured as one of two available protocols, depending on the pin strap value of the PROTOCOL_SEL pin:

- Inter-Integrated Circuit (I2C) up to 1 MHz Fast-mode Plus
- Serial Peripheral Interface (SPI) up to 10 MHz

Depending on which functional mode is selected (SPI or I2C), the CTRL[4:1] pins will assume the corresponding behavior.

表 7-5. Host-Side Control Interface Options

HOST-SIDE INTERFACE	PROTOCOL_SEL	CTRL4	CTRL3	CTRL2	CTRL1
I2C	Float or High	ADDR_DONE_N	SET_ADDR_N	SDA	SCL
SPI	GND	MISO	MOSI	SS_N	SCK

7.4.1 I2C Host-Side Control Interface

If I2C is used as the host-side communication protocol, the maximum number of FPC202 devices which can share a single I2C bus is 14. This allows for controlling up to 28 downstream ports through a single I2C bus.

I2C is an addressed interface. To reduce pin count and simplify integration, the FPC202 has an auto-addressing scheme whereby all FPC202s in a system will take on a unique address without requiring dedicated address pins. This is accomplished by connecting one FPC202's CTRL4 (ADDR_DONE_N) pin to the subsequent FPC202's CTRL3 (SET_ADDR_N) pin. The first FPC202 will connect CTRL3 (SET_ADDR_N) to GND, and the final FPC202 will connect CTRL4 (ADDR_DONE_N) to GND, as shown in 図 7-4.

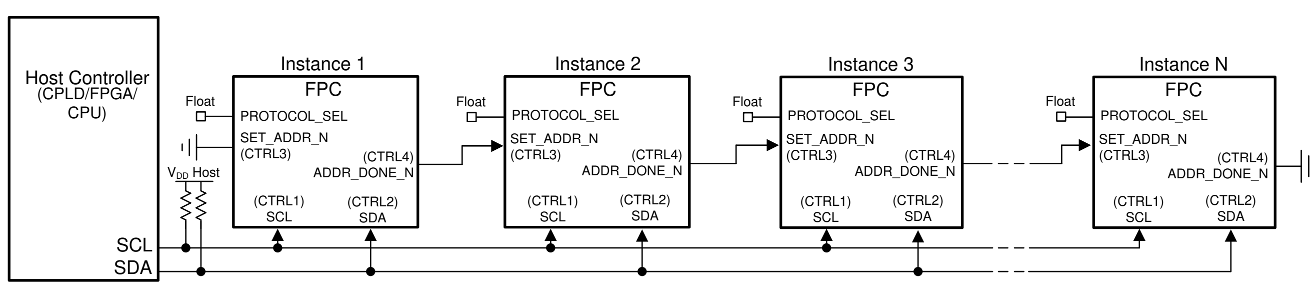

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図 7-4. FPC202 Connection Diagram For Unique Addressing in I2C Mode

For I2C host-side control interface implementations, the host controller must first configure each FPC202 device to have a unique address. The CTRL3 (SET_ADDR_N) pin is internally pulled to high logic (regardless of the EN pin status) and the FPC202 device will not respond to any I2C transactions until this pin is pulled low. Once it is driven to low logic, the device will respond to the default I2C 8-bit address (0x1E). A single I2C write to the FPC202 will reassign a new I2C address, and once this is done, the FPC202 will drive low logic with the CTRL4

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pin (ADDR_DONE_N) which allows the next FPC202 in the daisy chain to be programmed using the default address. Until this address re-assignment happens, the CTRL4 (ADDR_DONE_N) pin is high-Z.

This scheme allows each FPC202 to take a unique I2C address without any contention on the bus. The addresses may be programmed in any order except for the default 8-bit address (0x1E) which must be assigned to the last device in the daisy chain, or else two FPC202s will respond to 0x1E and there will be bus contention. The state of the CTRL3 (SET_ADDR_N) pin does not matter after the address is reprogrammed (this pin is then used to transfer the LED clock for blinking synchronization). Once the new address is programmed, it becomes fixed and may no longer be changed by a new register write. Only power cycling the device or toggling the EN pin will restore the device to the default re-programmable address.

The I2C address space for FPC202 applications is designed such that each FPC202, each port being controlled, and each logical device address within each port is accessible to the host controller through a unique I2C address. For a system where one or more FPC202s are used to control multiple ports (up to two ports per FPC202), the address of each FPC202 and the address of each each downstream port is shown in 表 7-6.

All FPC202 devices respond to 8-bit I2C address 0x02. This allows the host controller to broadcast write to all FPC202 devices simultaneously.

表 7-6. I2C 8-Bit Address Map

FPC202 INSTANCE NUMBER	FPC202 SELF-ADDRESS	PORT 0		PORT 1	
		PRIMARY DEVICE Default = 0xA0(1)	SECONDARY DEVICE Default = 0xA2(1)	PRIMARY DEVICE Default = 0xA0(1)	SECONDARY DEVICE Default = 0xA2(1)
ALL	0x02	–	–	–	–
0	0x04	0x20	0x22	0x28	0x2A
1	0x06	0x30	0x32	0x38	0x3A
2	0x08	0x40	0x42	0x48	0x4A
3	0x0A	0x50	0x52	0x58	0x5A
4	0x0C	0x60	0x62	0x68	0x6A
5	0x0E	0x70	0x72	0x78	0x7A
6	0x10	0x80	0x82	0x88	0x8A
7	0x12	0x90	0x92	0x98	0x9A
8	0x14	0xA0	0xA2	0xA8	0xAA
9	0x16	0xB0	0xB2	0xB8	0xBA
10	0x18	0xC0	0xC2	0xC8	0xCA
11	0x1A	0xD0	0xD2	0xD8	0xDA
12	0x1C	0xE0	0xE2	0xE8	0xEA
13	0x1E	0xF0	0xF2	0xF8	0xFA

(1) Device addresses are programmable. By default, the device 0 address is 0xA0 and the device 1 address is 0xA2. Request access to the *FPC202 Programmer's Guide* (SNLU229) here for more details.

The timing specification for an I2C transaction is described in 図 7-5.

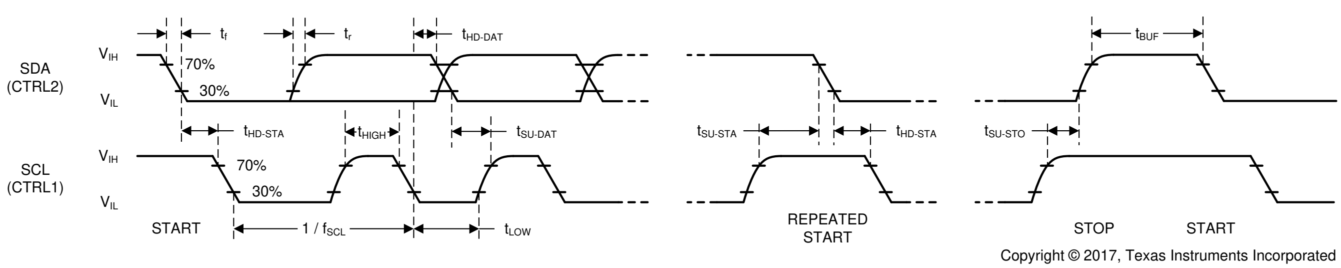

図 7-5. I2C Timing Diagram

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7.4.2 SPI Host-Side Control Interface

If SPI is used as the host-side communication protocol, the maximum number of FPC202 devices which can share a single SPI bus is technically unlimited. The read and write latency from/to the downstream ports will increase as the length of the SPI chain increases.

SPI does not require each FPC202 to have an address. The FPC202 devices are connected in a daisy-chain fashion as shown in 図 7-6. The first FPC202 will connect CTRL3 (MOSI) to the host controller's MOSI signal. CTRL4 (MISO) on the first FPC202 will connect to the subsequent FPC202's CTRL3 (MOSI) signal and so on until the final FPC202's CTRL4 (MISO) signal connects back to the host controller's MISO signal. All FPC202's will connect CTRL1 (SCK) and CTRL2 (SS_N) to the same SCK and SS_N pin on the host controller. For LED blink synchronization across multiple FPC202 devices, the SPI_LED_SYNC pin should be connected across all FPC202 devices in SPI mode. This is not necessary in I2C mode.

Each FPC202 device in the SPI chain will capture and act upon the command in its shift register when SS_N transitions from low (0) to high (1). The MOSI input is ignored and the MISO output is high impedance whenever SS_N is de-asserted high.

The prior SPI command, address, and data are shifted out on MISO as the current SPI command, address, and data are shifted in on MOSI. In all SPI transactions, the MISO output signal is enabled asynchronously whenever SS_N is asserted low.

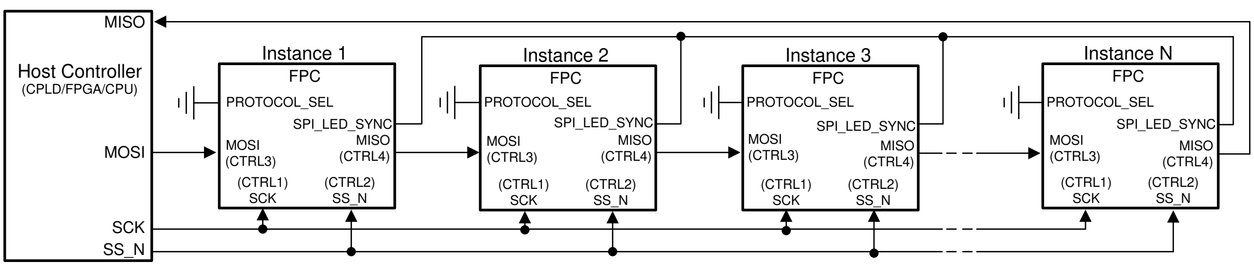

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図 7-6. FPC202 Connection Diagram For SPI Mode

The SPI address space for FPC202 applications is designed such that each port being controlled and each logical device address within each port is accessible to the host controller through a unique 12-bit address. For a system with up to N FPC202 devices on a single SPI chain, the full SPI address map is shown in 表 7-7.

表 7-7. SPI Address Map

FPC202 INSTANCE NUMBER	ADDRESS RANGE				
	PORT 0		PORT 1		FPC202 REGS
	PRIMARY DEVICE Default = 0xA0[(1)]	SECONDARY DEVICE Default = 0xA0[(1)]	PRIMARY DEVICE Default = 0xA0[(1)]	SECONDARY DEVICE Default = 0xA0[(1)]	
0	0x000 to 0x0FF	0x100 to 0x1FF	0x400 to 0x4FF	0x500 to 0x5FF	0x800 to 0x8FF
1					
2					
–					
N					

(1) Device addresses are programmable. By default, the device 0 address is 0xA0 and the device 1 address is 0xA2. Request access to the *FPC202 Programmer's Guide* (SNLU229) here for more details.

In SPI mode, the CTRL4 pin has a driver impedance of 60 Ω (typical). In order to minimize ringing due to the fast edge rate of the driver, it is recommended to match the transmission line characteristic impedance with the driver impedance. A series resistor near the driver pin (CTRL4) may be used to facilitate this impedance matching. If ringing is a concern, the IBIS model provided may be used for simulations.

7.4.2.1 SPI Frame Structure

Each SPI transaction to a single FPC202 device is 29 bits long and is framed by the assertion of SS_N (CTRL2) low. The MOSI (CTRL3) input is ignored and the MISO (CTRL4) output is high impedance whenever SS_N is de-asserted high. The prior SPI command, address, and data are shifted out on MISO as the current SPI command, address, and data are shifted in on MOSI. In all SPI transactions, the MISO output signal is enabled asynchronously whenever SS_N is asserted low.

表 7-8 shows the structure of a SPI frame. 図 7-7 shows an example implementation, including the internal SPI registers, for two FPC202 devices.

表 7-8. SPI Frame Structure

BIT	FIELD	DESCRIPTION
28	R/W	0: Write command 1: Read command This is the first bit shifted in on the MOSI input.
27:16	ADDR[11:0]	12-bit address field. See 表 7-7.
15	DATA[15]	Busy flag. For read operations, a '1' means the downstream port is busy. For write operations, DATA[15] is a don't care.
14	DATA[14]	Don't care.
13	DATA[13]	NACK received flag. A '1' means the FPC202 has received a NACK from the downstream port.
12	DATA[12]	Reject flag. A '1' means the FPC202 has rejected the previous command because it is busy servicing a prior command.
11:8	DATA[11:8]	Don't care.
7:0	DATA[7:0]	8-bit data field. DATA[0] is the last bit shifted in on the MOSI input.

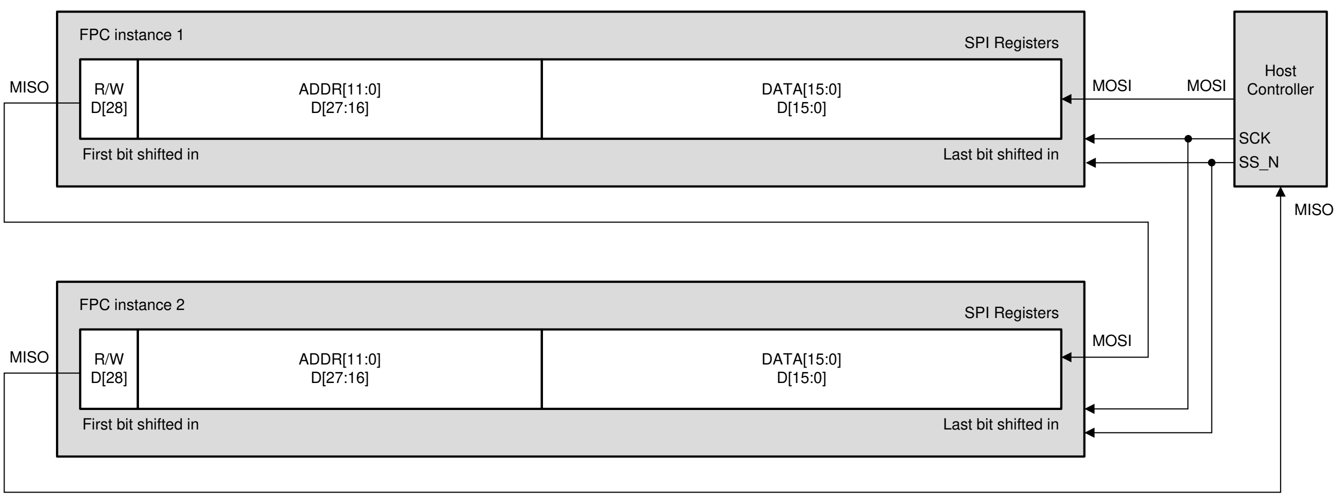

図 7-7. Example SPI Implementation For Two FPC202 Devices

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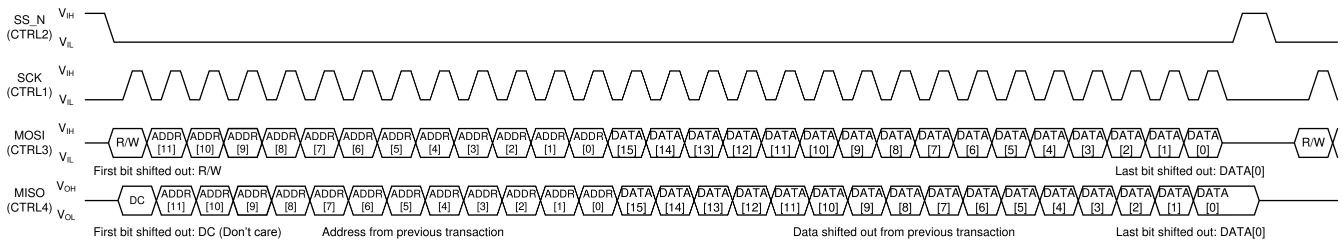

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図 7-8. Generic SPI Transaction

The timing specification for an SPI transaction is described in 図 7-9.

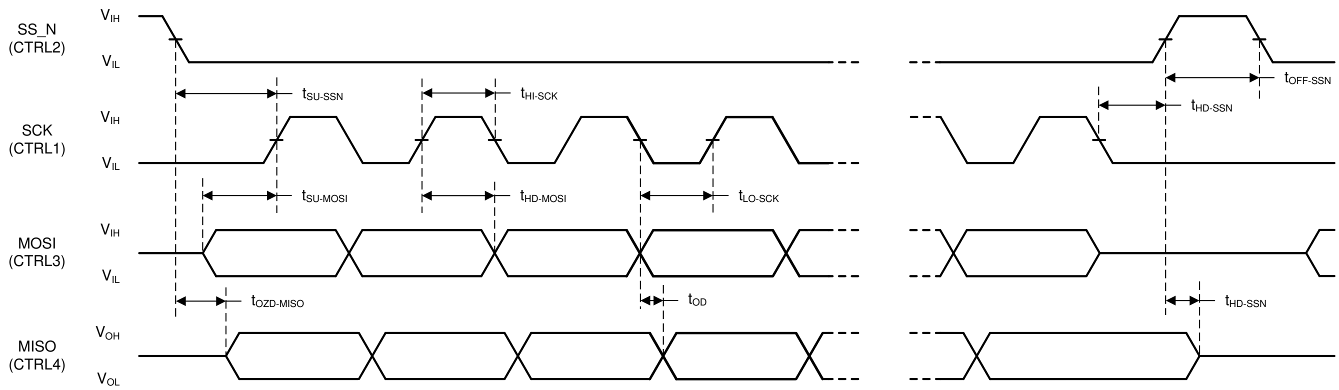

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図 7-9. SPI Timing Diagram

7.4.2.2 SPI Read Operation

Reading data from an FPC202 device requires two complete SPI transactions as shown in 図 7-10. In between these two transactions, the FPC202 fetches the requested information from either the local FPC202 registers or from the downstream port, depending on the address specified in the read transaction. Note that for downstream (also known as remote) register reads, the required time delay between the two transactions is longer:

- Local FPC202 register reads: $t_{OFF\text{-}SSN} \geq 1$ µs
- Downstream (remote) register reads: $t_{OFF\text{-}SSN} \geq 170$ µs assuming 400 kHz I2C; 620 µs assuming 100 kHz I2C

Also note that the second SPI transaction does not have to be a valid read or write operation and can instead be a dummy frame composed of all ones. This dummy frame is considered an invalid address by the FPC202 so it does not take any actions, but the read data from the prior frame still is shifted out and is valid. The use of a dummy frame is recommended when reading a single local FPC202 register because if a register is read twice using the same SPI frame, any self-clearing bits will be cleared in the second frame and the received data may be incorrect.

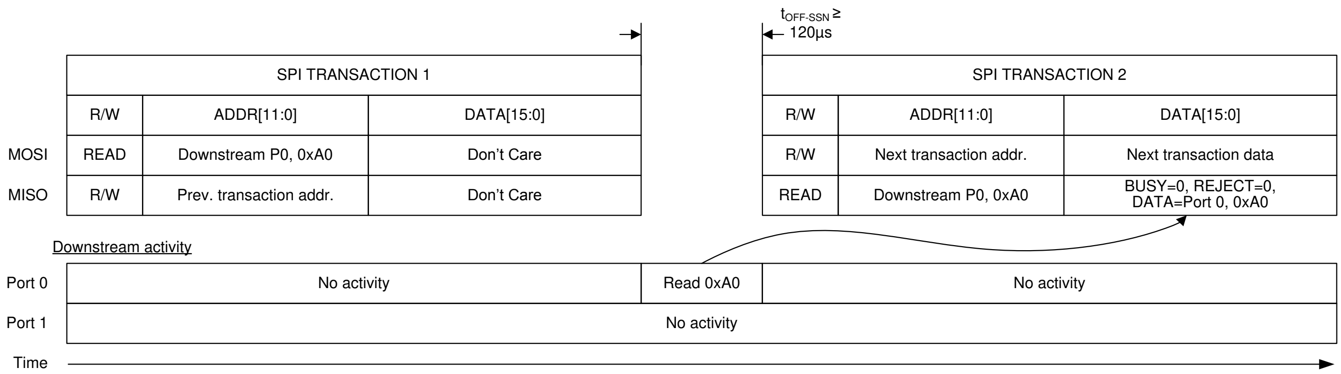

図 7-10. SPI Read Consisting of Two Separate SPI Transactions

For downstream (remote) register reads, where the FPC202 must translate a SPI read into an I2C read transaction with the downstream port, the most significant bit of the data returned on MISO indicates whether the downstream port is busy or not. If the second SPI read transaction is executed prematurely during a downstream (remote) read, the returned data will indicated BUSY = 1. When reading from a downstream port at an address that is not pre-fetched into local FPC202 memory, the time in between the first SPI transaction on a port, where the read is initiated, and the second SPI transaction on the same port, where the data is returned, must be at least 170 µs for a downstream I2C rate of 400 kHz and 620 µs for a downstream I2C rate of 100 kHz. 図 7-11 shows what happens when this prescribed delay is not followed.

If a back-to-back read transaction is issued to the same downstream port before the FPC202 has completed the first read transaction, then the subsequent transaction will contain status from the second read transaction with REJECT=1, which means that the second transaction was rejected due to the downstream I2C master being busy executing the first read transaction. 図 7-11 shows what happens when back-to-back reads are issued to the same downstream port without allowing enough time to complete the first read.

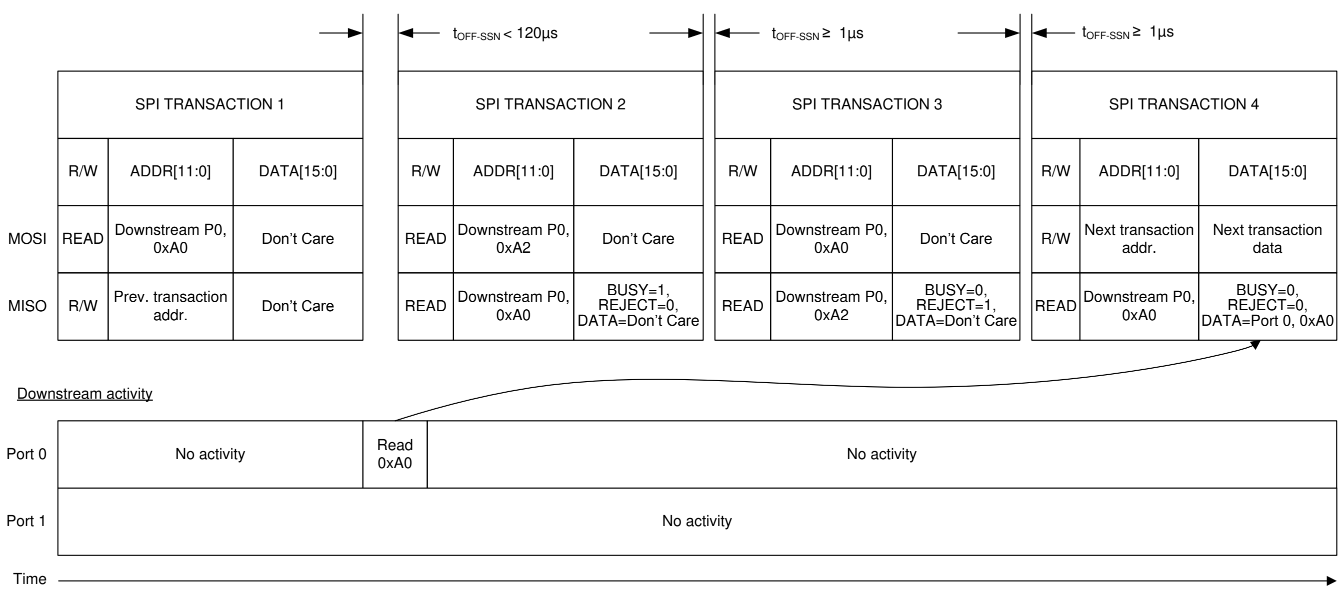

図 7-11. Back-to-Back SPI Reads From Same Port

7.4.2.3 SPI Write Operation

Writing data to an FPC202 device or the downstream ports under its management requires one SPI transactions. Multiple write transactions to downstream ports can proceed with minimal delay provided that different ports are being written to. If attempting to write data to the same downstream port, then the

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corresponding downstream access delay, $t_{OFF\text{-}SSN}$, is required. 図 7-12 shows an example of writing to both downstream ports in succession.

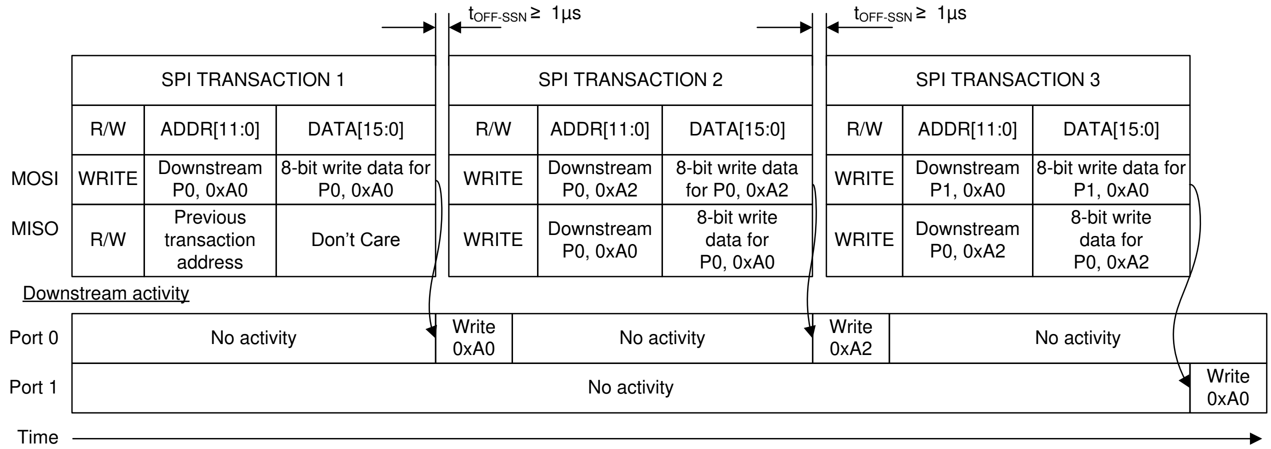

図 7-12. SPI Writes To Both Downstream Ports In Succession

7.5 Programming

Programming the FPC202 is accomplished through a single SPI or I2C interface, depending on the PROTOCOL_SEL pin state. To simplify configuration, a C function library is provided which can be integrated into the system software or used as a reference. The existence of basic SPI or I2C read and write functions is assumed within the provided C function library. The exact implementation of SPI or I2C read and write functions is beyond the scope of the C function library. Request access to the *FPC202 Programmer's Guide* (SNLU229) here for the register map and more details.

8 Application and Implementation

注

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8.1 Application Information

The FPC202 is general-purpose and can be used to control a variety of interfaces including, but not limited to, SFP, QSFP, Mini-SAS HD, and others. The following sections describe typical applications and their associated design considerations.

8.2 Typical Application

The FPC202 is typically used in the following application scenarios:

1. SFP/QSFP/QSFP-DD/OSFP port management
2. Mini-SAS HD port management

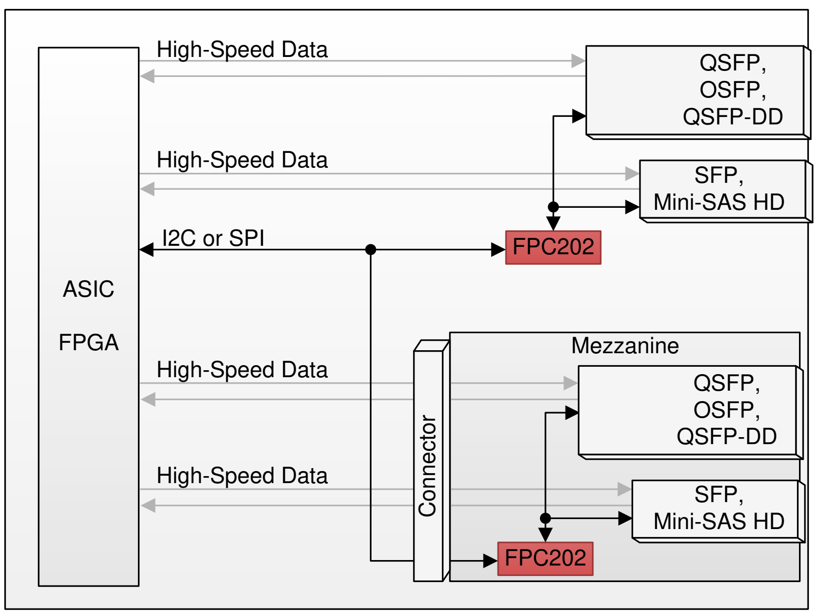

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図 8-1. Typical Uses For the FPC202 in a System

8.2.1 SFP/QSFP Port Management

The FPC202 can be used to manage the low-speed signals, I2C, and LEDs for multiple SFP and/or QSFP ports, up to two per FPC202 device. The FPC202 package is optimized to allow placement underneath an SFP or QSFP port on the opposite side of the board. This allows hardware designers to terminate all SFP/QSFP low-speed signals close to the port and route a single I2C or SPI interface back to the system controller (ASIC or FPGA). 図 8-2 shows an example of this application where two FPC202 devices are used to control two QSFP ports and two SFP ports, in addition to controlling LEDs and two TPS2556 power distribution switches. 図 8-3 shows an example schematic for the first two ports of this application.

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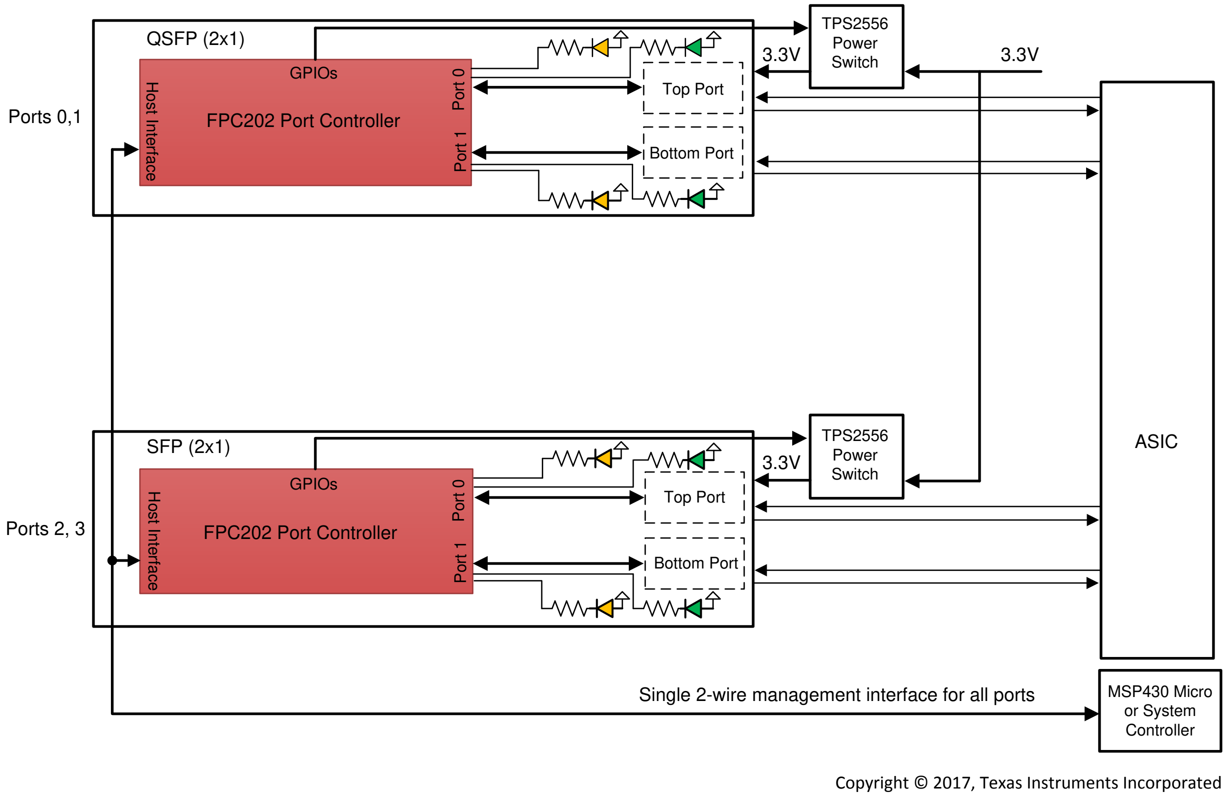


図 8-2. SFP/QSFP Application Block Diagram

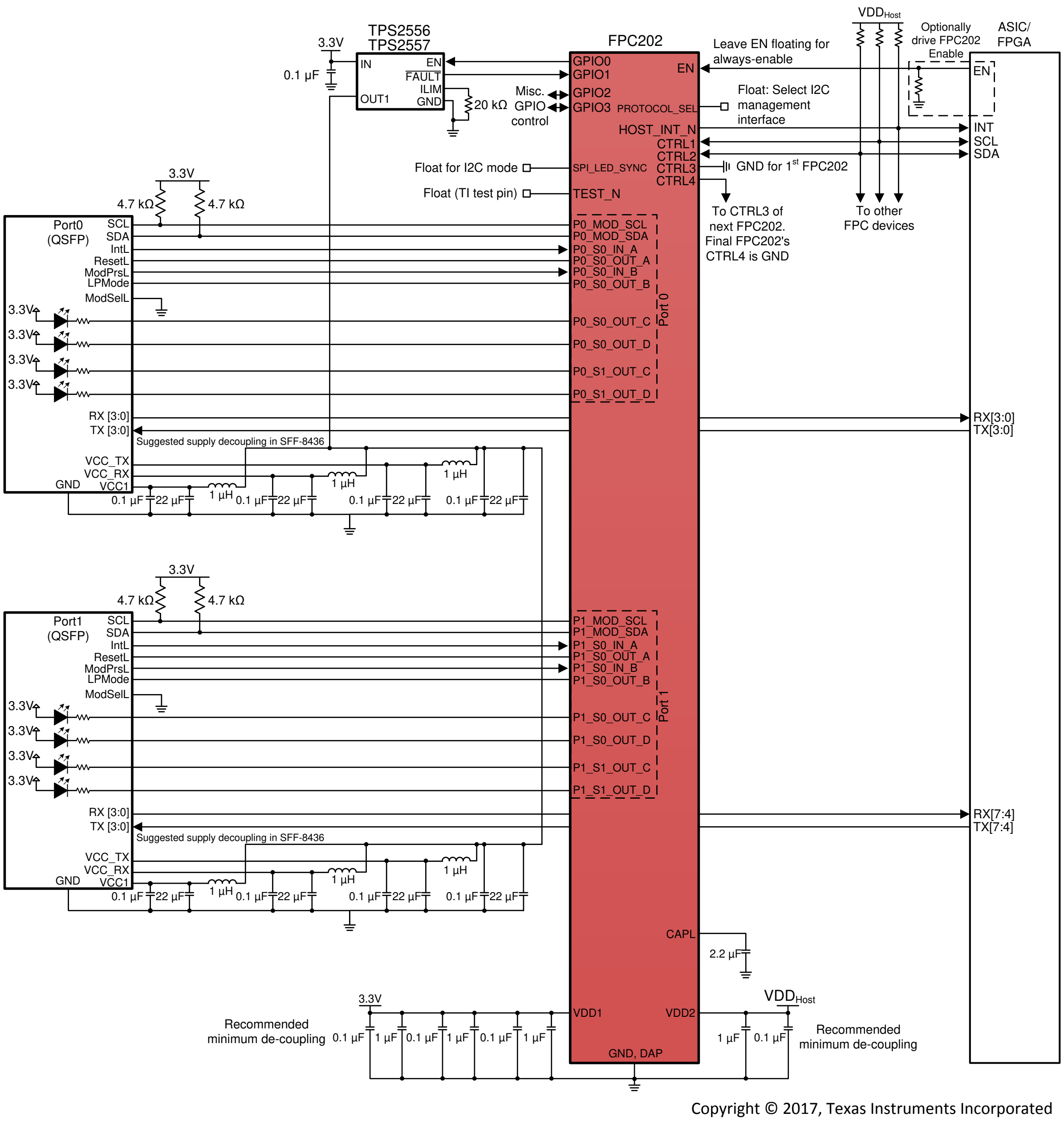


図 8-3. SFP/QSFP Application Schematic

8.2.1.1 Design Requirements

For this design example, the following guidelines outlined in 表 8-1 apply.

表 8-1. SFP/QSFP Application Design Guidelines

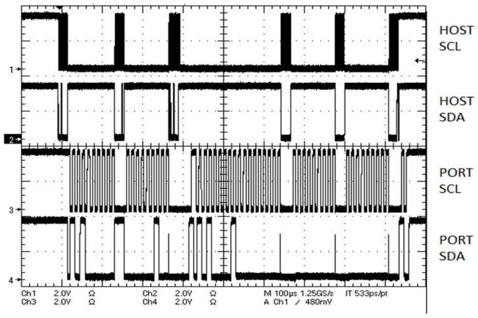
DESIGN PARAMETER	REQUIREMENT
FPC202 physical placement	The FPC202 package is small enough to fit underneath an SFP or QSFP cage, on the opposite side of the board. For SFP applications, such a placement leaves 4.6 mm of air gap between the FPC202 package edge and the SFP pressfit pins (assuming 14.25 mm pin-to-pin spacing for a stacked SFP cage). For QSFP applications, such a placement leaves 7.2 mm of air gap between the FPC202 package edge and the QSFP pressfit pins (assuming 19.5 mm pin-to-pin spacing for a stacked QSFP cage).
LED implementation	The FPC202 is designed to drive active-low LEDs which have their anode connected to the port-side 3.3-V supply. Refer to *セクション 7.3.2*.
Port-side I2C SDA and SCL pull-ups	As per the SFF-8431 and SFF-8436 specification, the port-side (downstream) SCL and SDA nets should be pulled up to 3.3 V using resistors in the 4.7-kΩ to 10-kΩ range.
QSFP ModSelL	QSFP provides a mechanism to enable or disable the port's I2C interface. Since the FPC202 has a separate I2C master to communicate with each port, the ModSelL input for every QSFP can be connected to GND, thereby permanently enabling each QSFP port's I2C bus.
SFP/QSFP port power supply de-coupling	Follow the SFF-8431 and SFF-8436 recommendations for power supply de-coupling.

8.2.1.2 Detailed Design Procedure

The design procedure for SFP/QSFP applications is as follows:

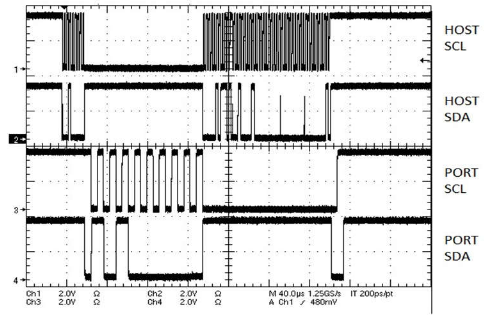
1. Determine the total number of ports in the system, N_{ports}, which require management through an FPC202 device. The minimum number of FPC202 devices required to support N_{ports} is ceiling{N_{ports}÷2}.
2. Determine which host-side control interface will be used to manage all FPC202 devices and all ports: I2C or SPI.
3. For I2C applications:
   a. Up to 14 FPC202 devices can share a single host-side I2C control bus. If more than 14 FPC202 devices are used, then more than one I2C control bus will be required.
   b. Care should be taken to make sure the I2C clock (SCL) and data (SDA) lines do not exceed the maximum bus capacitance defined in *セクション 6.5*. The bus capacitance will consist of the pin capacitance from each device connected plus the trace capacitance.
   c. Make sure appropriate pull-up resistors are selected for the I2C clock (SCL) and data (SDA) lines.
4. For SPI applications:
   a. When using SPI for host-side communications, technically there is no limit to the number of FPC202 devices which can exist on the SPI chain. However, the user should be aware that for SPI communication, skew is introduced between the SCK and MISO lines due to the propagation delay of the data through all of the devices and trace and then back to the host. It is up to the user to ensure that host's SPI timings are met after any skew due to propagation delay.
   b. Care should be taken to make sure the SPI clock (SCK) and data (MOSI and MISO) lines do not exceed the maximum bus capacitance defined in *セクション 6.5*. The bus capacitance will consist of the pin capacitance from each device connected plus the trace capacitance.
5. Route the low-speed inputs (P[1:0]_S*_IN_*), outputs (P[1:0]_S*_OUT_*), and I2C signals (P[1:0]_MOD_SCL / P[1:0]_MOD_SDA) from the FPC202 to the corresponding port or device, keeping all the signals for a given port grouped together. For example, if FPC202 port 1 is being used to control QSFP port 7, then all of QSFP port 7's low-speed signals, LED signals, and I2C signals should connect to FPC202 pins P1_S*_IN_*, P1_S*_OUT_*, and P1_MOD_SCL/P1_MOD_SDA.
6. Utilize the spare S*_IN_*, S*_OUT_*, and GPIO[3:0] signals to control miscellaneous functions on the board, like enabling and disabling a power switch.
7. For applications requiring hot-plug between the FPC202 and the host controller, control the FPC202 enable signal (EN, pin 22) such that EN is de-asserted low until VDD2 and the host-side control interface (I2C or SPI) is fully connected and stable.

8.2.1.3 Application Curves



Host-Side I2C: 400 kHz
Port I2C: 100 kHz
Approximate time to read three bytes: 820 μs

図 8-4. Downstream Read – Three Bytes Outside of Pre-Fetched Range



Host-Side I2C: 400 kHz
Port I2C: 100 kHz
Approximate time to read three bytes: 280 μs

図 8-5. Downstream Read – Three Bytes in the Pre-Fetched Range

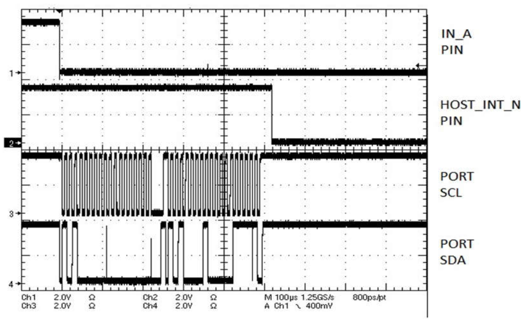


図 8-6. Interrupt-Driven Pre-Fetch

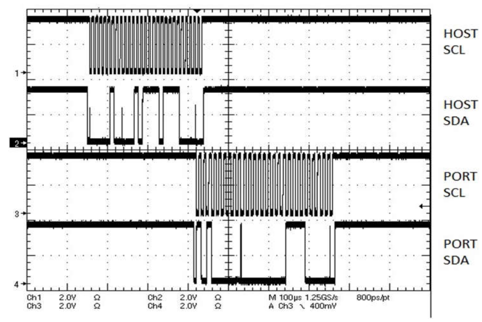


図 8-7. Scheduled Write Operation

8.3 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The port-side supply, VDD1, should be 3.3-V (typical) and should meet the recommended operating conditions outlined in *セクション 6.3* in terms of DC voltage, AC noise, and start-up ramp time. If using the FPC202 to control a power switch to enable/disable power to the front-port connectors, the FPC202 should be connected to 3.3-V power on the input side of the switch.
2. The host-side supply, VDD2, should be 1.8-V to 3.3-V (typical) and should meet the recommended operating conditions outlined in *セクション 6.3* in terms of DC voltage, AC noise, and start-up ramp time.
3. The maximum current draw for the FPC202 is provided in *セクション 6.5*. This figure can be used to calculate the maximum current the supply must provide.
4. The FPC202 does not require any special power supply filtering (that is, ferrite bead), provided the recommended operating conditions are met. Only standard de-coupling is required. Refer to セクション 5 for details concerning the recommended supply decoupling for each pin.

8.3.1 Power Supply Sequencing

There are no sequencing requirements for the VDD1 and VDD2 power supplies. Note, however, that the FPC202 will not respond to host-side communications (SPI or I2C) until both of the following conditions are met:

1. The internal power-on reset (PoR) is complete. Power-on reset lasts for T_{POR} milliseconds after the VDD1 supply reaches a stable voltage (refer to *セクション 6.6*).
2. The VDD2 (host-side) supply reaches a stable voltage.

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8.4 Layout

8.4.1 Layout Guidelines

The following guidelines should be followed when designing the layout:

1. Decoupling capacitors should be placed as close to the VDD1/VDD2 pins as possible.
2. The die attach pad (DAP) should have a low-impedance connection to the nearest GND plane. This is typically accomplished with vias connecting the surface GND plane to inner-layer GND planes. One recommended option is to place 14 vias spaced ≥1 mm apart in a seven by two grid as shown in 図 8-8.
3. When placing the FPC202 underneath an SFP or QSFP cage, on the opposite side of the PCB, as shown in 図 8-8, take note of the SFP/QSFP keep-out areas as well as any keep-out area required for the pressfit assembly tooling.
4. Pin 32 (CAPL) should have a low-impedance, low-inductance path to a 2.2-µF decoupling capacitor to GND. If space constraints force this capacitor to be placed away from the pin, then a wider metal trace (that is, 20 mil) to the capacitor, utilizing an inner layer if necessary, is recommended.
5. A GND pin is provided (pin 27) to make it easy to probe GND near the FPC202, especially in applications where the opposite side of the PCB is covered by an SFP or QSFP cage and therefore inaccessible. To maximize the benefit of this probe point, connect this pin to the local GND plane (that is, to the DAP and associated GND vias) through a low-impedance trace. In addition, it may be helpful to route a short trace to a probe point for easy access.

8.4.2 Layout Example

The following layout example shows how the FPC202 can be placed underneath a stacked SFP cage, on the opposite side of the PCB. In this example, the FPC202 is being used to control two SFP ports. For reference, a QSFP footprint, which is wider than the SFP footprint, is shown next to the stacked SFP cage. The FPC202 will also fit beneath a stacked QSFP, QSFP-DD, or OSFP cage. In this example, the FPC202 is using two of its GPIO pins to control a TPS2556 power distribution switch which is placed beneath the QSFP cage. Note that there are multiple ways to route the low-speed control signals and I2C signal between the cages and the FPC202. This example uses two inner layers to accomplish this routing.

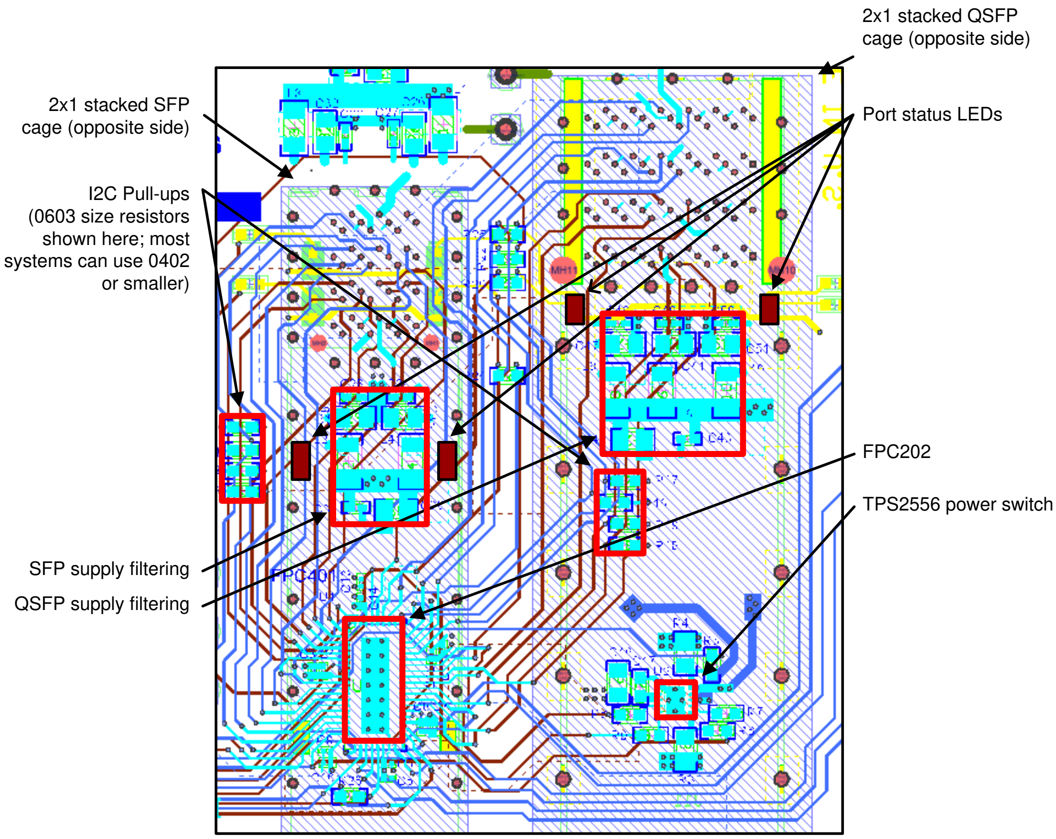

図 8-8. Layout Example

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *FPC202 Programmer's Guide*
- Texas Instruments, *FPC401 Evaluation Module (EVM) User's Guide*

Click here to request access to these documents in the FPC202 MySecure folder.

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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9.6 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (March 2022) to Revision B (January 2024) **Page**

- データシートの最初の公開リリース.. 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
FPC202RHUR	Active	Production	WQFN (RHU) | 56	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	FPC2
FPC202RHUR.A	Active	Production	WQFN (RHU) | 56	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	FPC2
FPC202RHUT	Active	Production	WQFN (RHU) | 56	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	FPC2
FPC202RHUT.A	Active	Production	WQFN (RHU) | 56	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	FPC2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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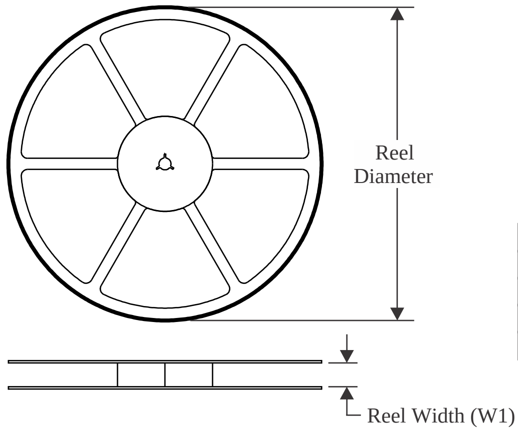
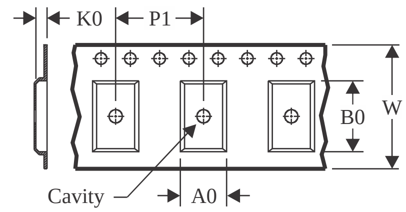
TAPE AND REEL INFORMATION

REEL DIMENSIONS

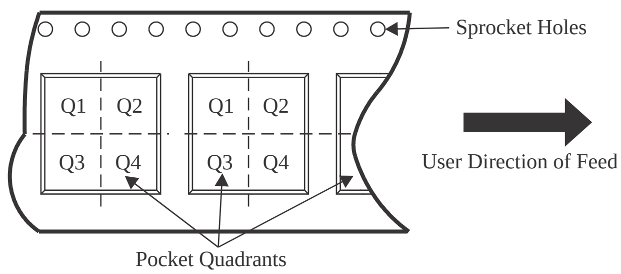


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

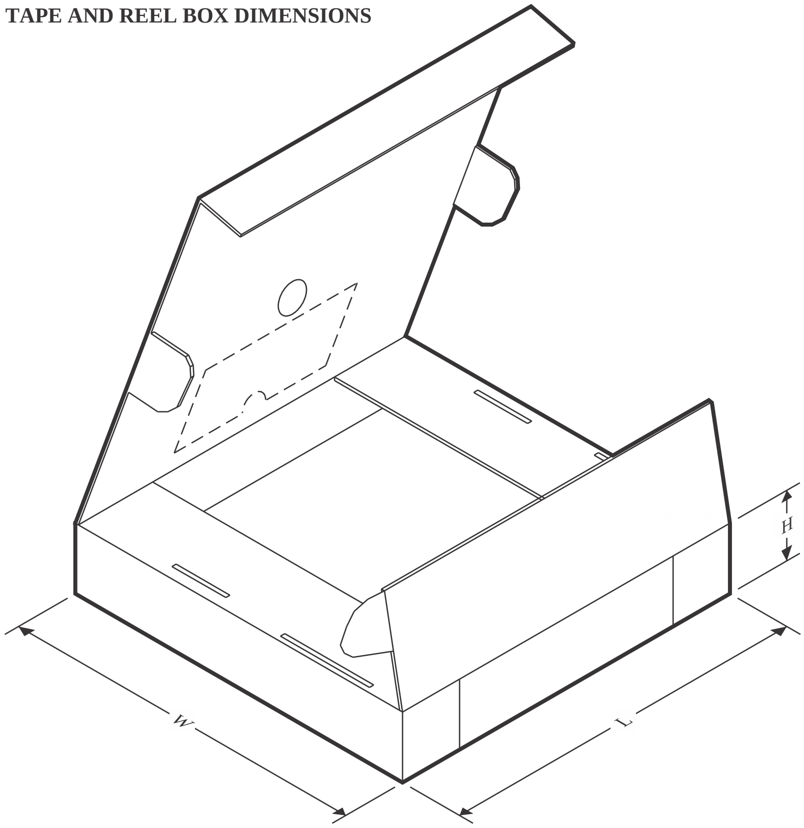
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

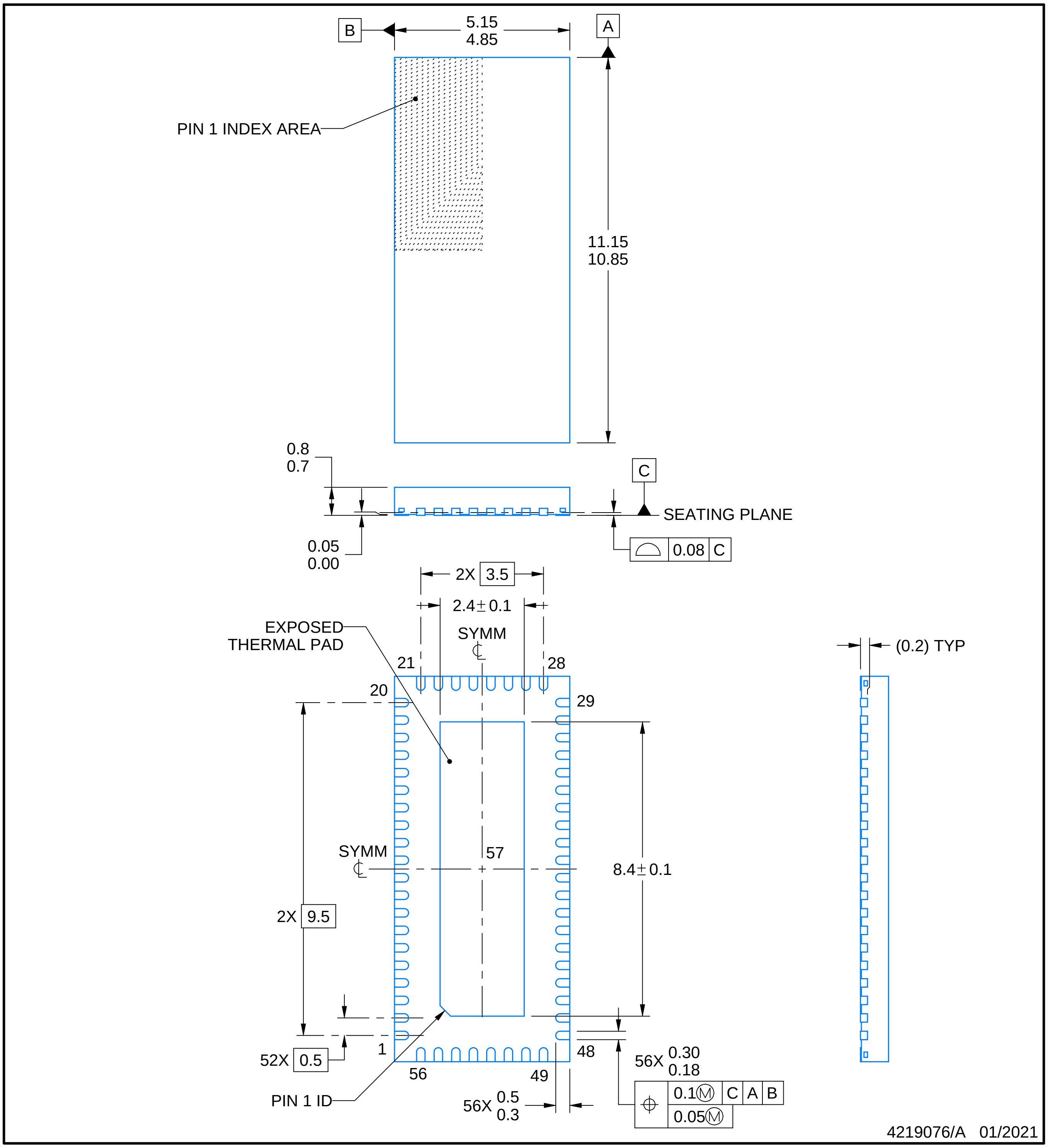
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
FPC202RHUR	WQFN	RHU	56	2000	330.0	24.4	5.3	11.3	1.0	8.0	24.0	Q1
FPC202RHUT	WQFN	RHU	56	250	178.0	24.4	5.3	11.3	1.0	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



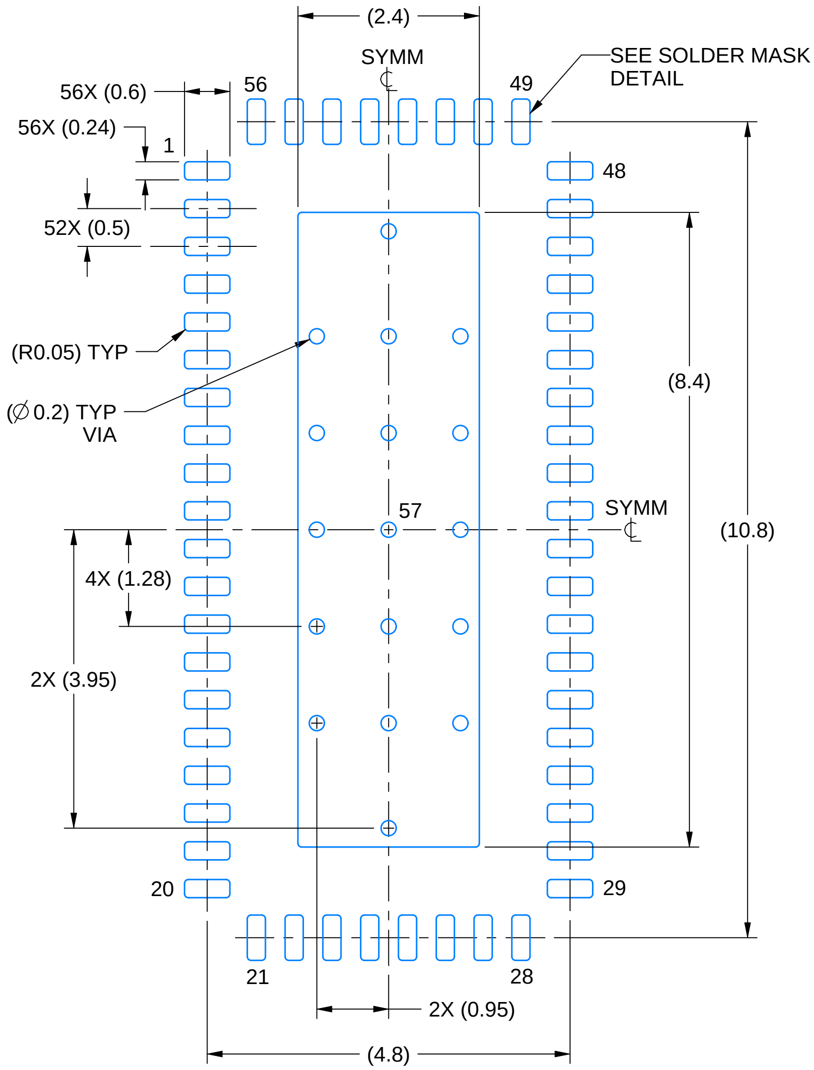
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
FPC202RHUR	WQFN	RHU	56	2000	356.0	356.0	45.0
FPC202RHUT	WQFN	RHU	56	250	213.0	191.0	55.0

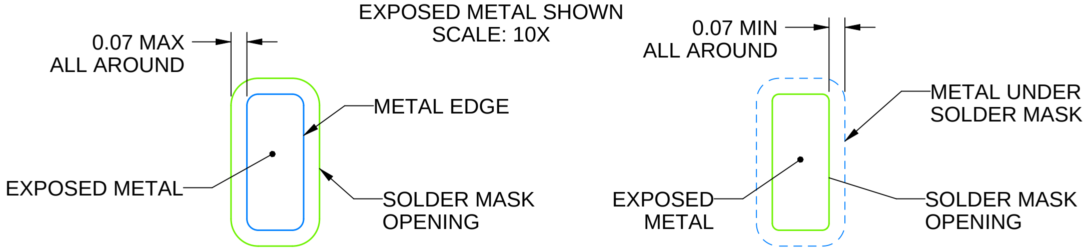


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON SOLDER MASK DEFINED (PREFERRED)

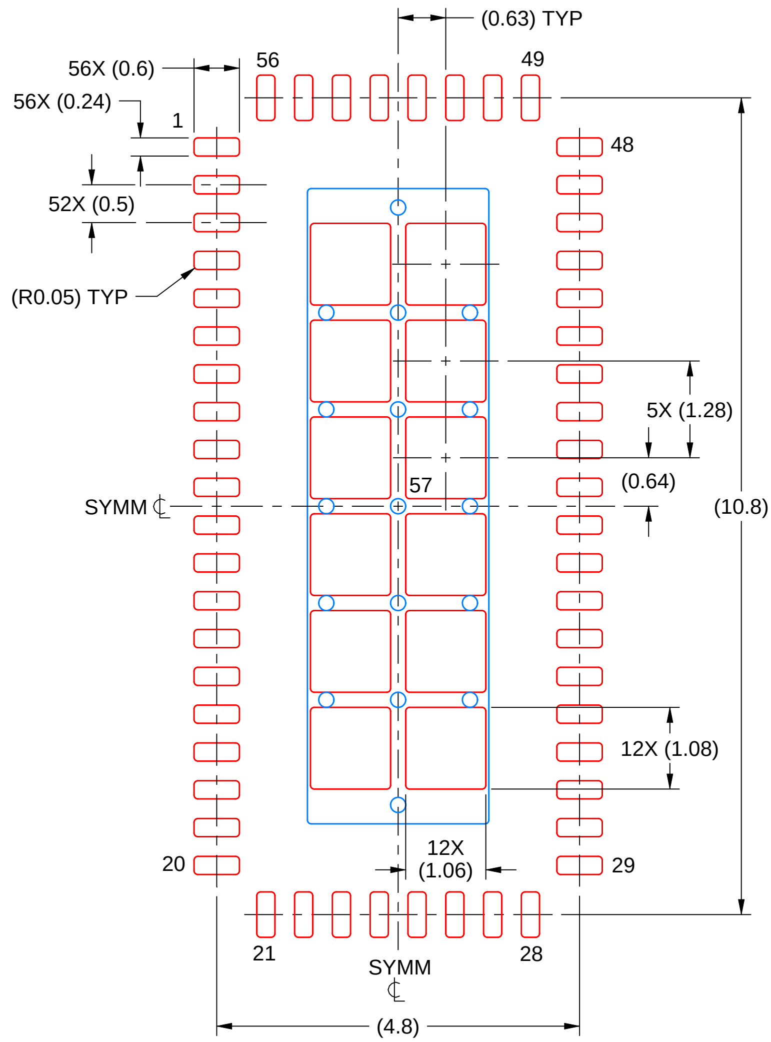
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219076/A 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219076/A 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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