FDC1004-Q1 4 チャネル キャパシタンス-デジタル コンバータ、静電容量式検出アプリケーション用

1 特長

- 車載アプリケーション認定済み
- 下記結果で AEC-Q100 認定済み
  - デバイス温度グレード 1:動作時周囲温度範囲 -40℃～125℃
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C5
- 入力範囲:±15pF
- 測定分解能:0.5fF
- 最大オフセット容量:100pF
- プログラム可能な出力レート:100/200/400S/s
- 最大シールド負荷:400pF
- 電源電圧:3.3 V
- 温度範囲:-40℃～125℃
- 消費電流:
  - アクティブ:750µA
  - スタンバイ:29µA
- インターフェイス:I^2C
- チャネル数:4

2 アプリケーション

- 近接センサ
- ジェスチャ認識
- 車載ドア / キック センサ
- 車載雨センサ
- リモートおよび直接液面センサ
- 高分解能金属プロファイリング
- 雨 / 霧 / 氷 / 雪センサ
- 材料サイズ検出

3 概要

接地コンデンサ センサを使用した静電容量式センシングは、低電力動作、低コスト、高分解能、非接触のセンシング技法であり、近接検出やジェスチャ認識から物質分析やリモートの液面検出まで、幅広いアプリケーションに適用可能です。静電容量式センシング システムのセンサには、任意の金属や導体が使用できるため、低コストで柔軟性の高いシステム設計が可能になります。

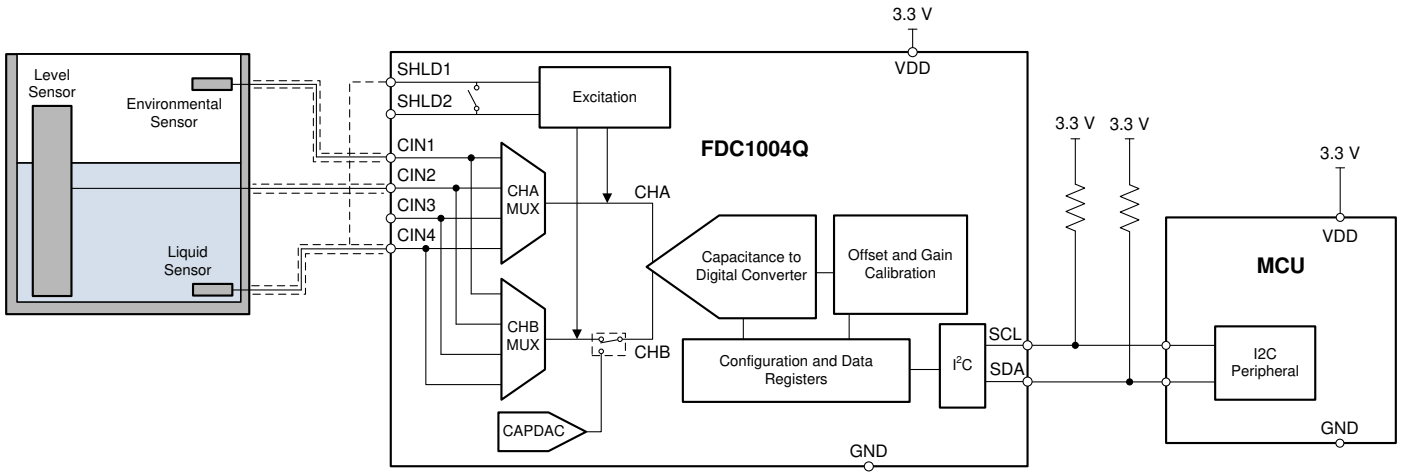
FDC1004-Q1 は、高分解能で AEC-Q100 認定済みの 4 チャネル キャパシタンス / デジタル コンバータであり、静電容量式センシング ソリューションの実装に適しています。各チャネルのフルスケール範囲は ±15pF で、最大 100pF のセンサ オフセット容量を処理できます。これらは内部でプログラムすることも、外付けコンデンサを使用して、時間の経過および温度による環境変化をトラッキングすることもできます。大きいオフセット静電容量特性により、リモート センサを使用可能です。

FDC1004-Q1 には、センサ シールド用のシールド ドライバも内蔵されているため、EMI 干渉を低減し、静電容量式センサのセンシング方向を絞ることが可能です。FDC1004-Q1 は小型フットプリントであるため、スペースの制約が厳しいアプリケーションで使用できます。FDC1004-Q1 は、10 ピンの VSSOP パッケージで供給され、量産時の光学検査が可能であり、MCU とのインターフェイス用に I^2C インターフェイスが搭載されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
FDC1004-Q1	DGS (VSSOP、10)	3mm × 4.9 mm

(1) 供給されているすべてのパッケージについては、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション

Table of Contents

4 Pin Configuration and Functions

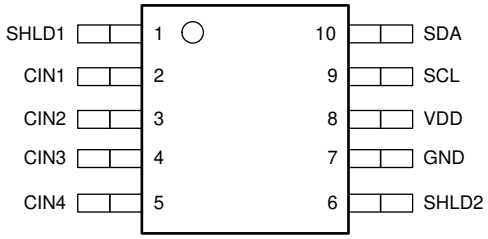


図 4-1. DGS Package 10 Pin VSSOP Top View

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
SHLD1	1	A	Capacitive Input Active AC Shielding.
CIN1	2	A	Capacitive Input. The measured capacitance is connected between the CIN1 pin and GND. If not used, leave this pin as an open circuit.
CIN2	3	A	Capacitive Input. The measured capacitance is connected between the CIN2 pin and GND. If not used, leave this pin as an open circuit.
CIN3	4	A	Capacitive Input. The measured capacitance is connected between the CIN3 pin and GND. If not used, leave this pin as an open circuit.
CIN4	5	A	Capacitive Input. The measured capacitance is connected between the CIN4 pin and GND. If not used, leave this pin as an open circuit.
SHLD2	6	A	Capacitive Input Active AC Shielding.
GND	7	G	Ground
VDD	8	P	Power Supply Voltage. Decouple this pin to GND, using a low impedance capacitor, for example in combination with a 1µF tantalum and a 0.1µF multilayer ceramic.
SCL	9	I	Serial Interface Clock Input. Connects to the controller clock line. Requires pullup resistor if not already provided elsewhere in the system.
SDA	10	I/O	Serial Interface Bidirectional Data. Connects to the controller data line. Requires a pullup resistor if not provided elsewhere in the system.

(1) P=Power, G=Ground, I=Input, O=Output, A=Analog, I/O=Bidirectional Input/Output

5 Specifications

5.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
Input voltage	VDD	–0.3	6	V
	SCL, SDA	–0.3	6	V
	at any other pin	–0.3	VDD+0.3	V
Input current	at any pin		3	mA
Junction temperature(2)			150	°C
Storage Temperature	T_{STG}	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (VDD-GND)	3	3.3	3.6	V
Temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		FDC1004-Q1 VSSOP (DGS) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.8	°C/W
$R_{\theta JC}$	Junction-to-case(top) thermal resistance	48.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

Over recommended operating temperature range, V_{DD} = 3.3V, for T_A = 25°C (unless otherwise noted). (1)

PARAMETER		TEST CONDITION	MIN(2)	TYP(3)	MAX(2)	UNIT
POWER SUPPLY						
I_{DD}	Supply current	Conversion mode; Digital input to VDD or GND		750	950	µA
		Standby; Digital input to VDD or GND		29	70	µA
CAPACITIVE INPUT						
ICR	Input conversion range			±15		pF
C_{OMAX}	Max input offset capacitance	per channel, Series resistance at CINn n=1.4 = 0 Ω		100		pF
RES	Effective resolution (5)	Sample rate = 100S/s (4)		16		bit
EON	Output noise	Sample rate = 100S/s (4)		33.2		aF/√Hz
ERR	Absolute error	after offset calibration		±6		fF
TcC_{OFF}	Offset deviation over temperature	-40°C < T < 125°C		46		fF
G_{ERR}	Gain error			0.2%		
tcG	Gain drift vs temperature	-40°C < T < 125°C		-37.5		ppm/°C
PSRR	DC power supply rejection	3V < V_{DD} < 3.6V, single-ended mode (channel vs GND)		13.6		fF/V
CAPDAC						
FR_{CAPDAC}	Full-scale range			96.9		pF
$TcCOFF_{CAPDAC}$	Offset drift vs temperature	-40°C < T < 125°C		30		fF
EXCITATION						
f	Frequency			25		kHz
V_{AC}	AC voltage across capacitance			2.4		Vpp
V_{DC}	Average DC voltage across capacitance			1.2		V
SHIELD						
DRV	Driver capability	*f* = 25kHz, SHLDn to GND, n = 1,2			400	pF

(1) Electrical Characteristics Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ=TA. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where TJ>TA. Absolute Maximum Ratings indicate junction temperature limits beyond which the device can be permanently degraded, either mechanically or electrically.
(2) Limits are ensured by testing, design, or statistical analysis at 25Degree C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values can vary over time and also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(4) No external capacitance connected.
(5) Effective resolution is the ratio of converter full scale range to RMS measurement noise.

5.6 I²C Interface Voltage Level

Over recommended operating free-air temperature range, V_{DD} = 3.3V, for T_A = T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage		0.7*V_{DD}			V
V_{IL}	Input low voltage				0.3*V_{DD}	V
V_{OL}	Output low voltage	Sink current 3mA			0.4	V
HYS	Hysteresis (1)		0.1*V_{DD}			V

(1) This parameter is specified by design and/or characterization and is not tested in production.

5.7 I²C Interface Timing

Over recommended operating free-air temperature range, V_{DD} = 3.3V, for $T_A = T_J$ = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	Clock frequency(1)		10		400	kHz
t_{LOW}	Clock low time(1)		1.3			µs
t_{HIGH}	Clock high time(1)		0.6			µs
$t_{HD;STA}$	Hold time (repeated) START condition(1)	After this period, the first clock pulse is generated	0.6			µs
$t_{SU;STA}$	Set-up time for a repeated START condition(1)		0.6			µs
$t_{HD;DAT}$	Data hold time(1) (2)		0			ns
$t_{SU;DAT}$	Data setup time(1)		100			ns
t_f	SDA fall time(1)	IL ≤ 3mA; CL ≤ 400pF			300	ns
$t_{SU;STO}$	Set-up time for STOP condition(1)		0.6			µs
t_{BUF}	Bus free time between a STOP and START condition(1)		1.3			µs
$t_{VD;DAT}$	Data valid time(1)				0.9	ns
$t_{VD;ACK}$	Data valid acknowledge time(1)				0.9	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter(1)				50	ns

(1) This parameter is specified by design and/or characterization and is not tested in production.
(2) The FDC1004-Q1 provides an internal 300ns minimum hold time to bridge the undefined region of the falling edge of SCL.

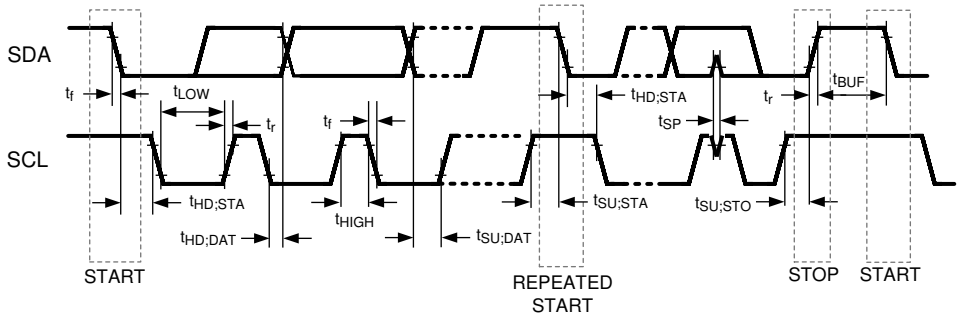


図 5-1. I²C Timing

5.8 Typical Characteristics

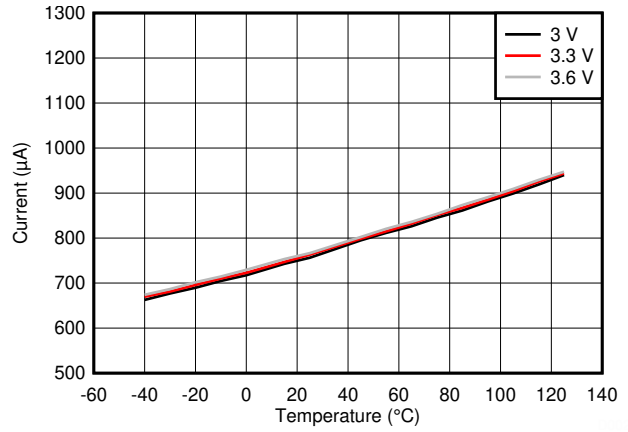


図 5-2. Active Conversion Mode Supply Current vs Temperature

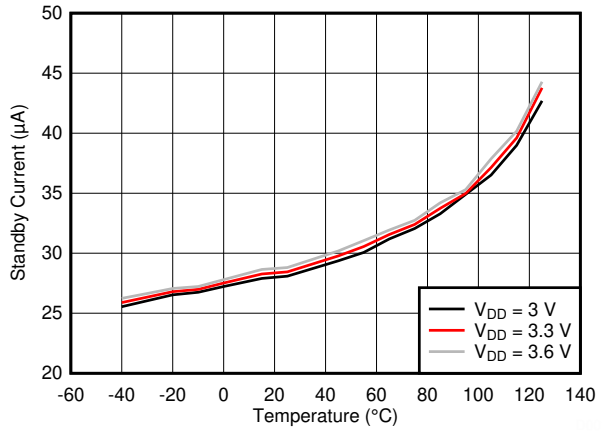


図 5-3. Standby Mode Supply Current vs Temperature

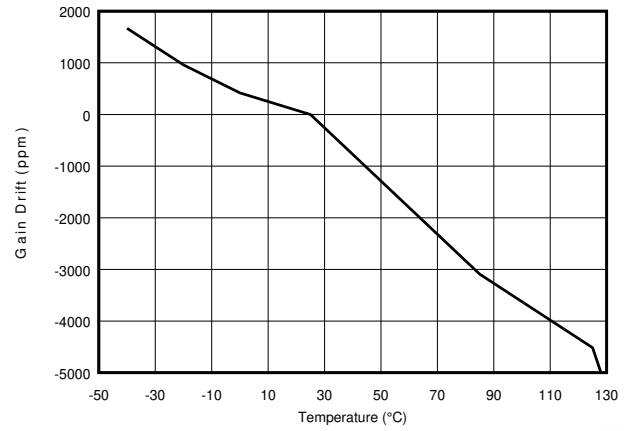
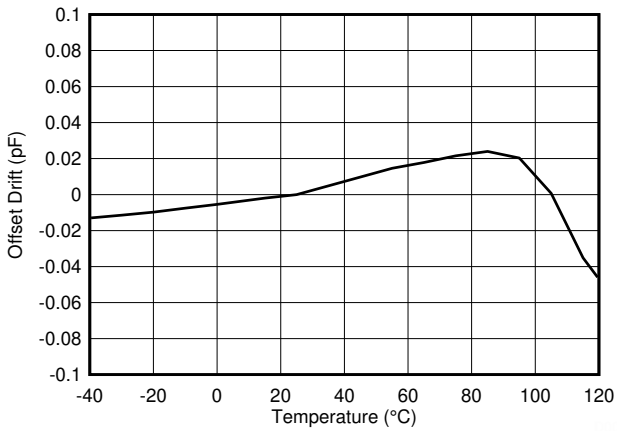
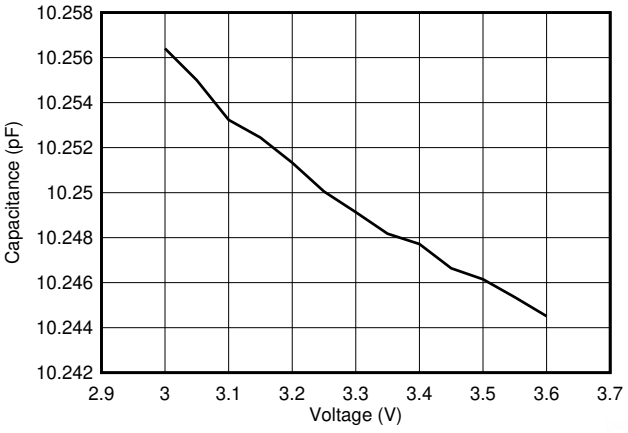


図 5-4. Gain Drift vs Temperature



CINn = open, where n = 1...4

図 5-5. Offset Drift vs Temperature



Capacitance Value = 10pF

図 5-6. Capacitance vs Voltage

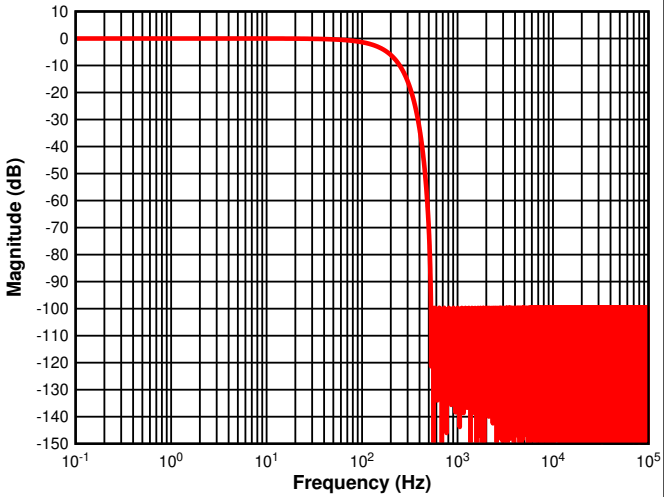


図 5-7. Frequency Response 100S/s

5.8 Typical Characteristics (continued)

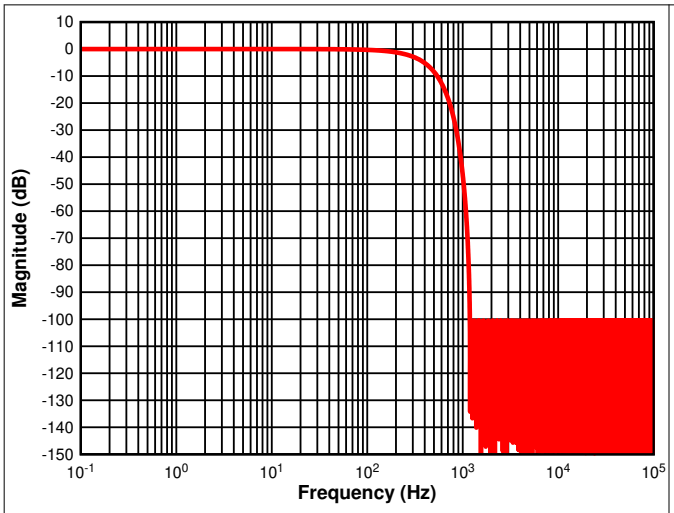


図 5-8. Frequency Response 200S/s

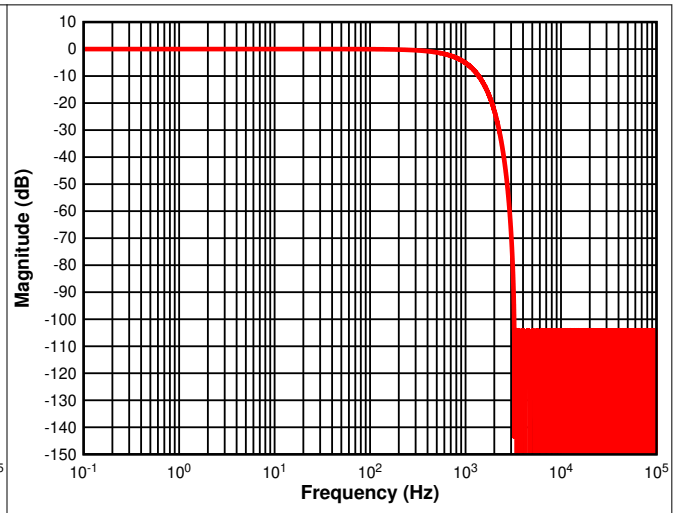


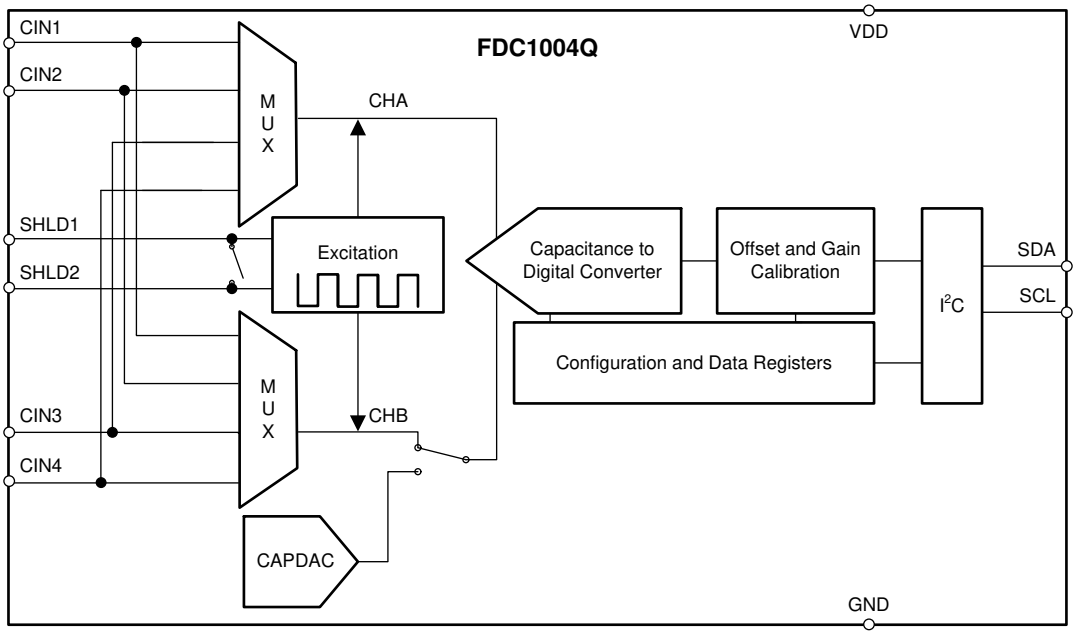
図 5-9. Frequency Response 400S/s

6 Detailed Description

6.1 Overview

The FDC1004-Q1 is a high-resolution, 4-channel capacitance-to-digital converter for implementing capacitive sensing solutions. Each channel has a full scale range of ±15pF and can handle a sensor offset capacitance of up to 100pF, which can be either programmed internally or can be an external capacitor for tracking environmental changes over time and temperature. The large offset capacitance capability allows for the use of remote sensors. The FDC1004-Q1 also includes shield drivers for sensor shields, which can reduce EMI interference and help focus the sensing direction of a capacitive sensor. The small footprint of the FDC1004-Q1 allows for use in space-constrained applications. For more information on the basics of capacitive sensing and applications, refer to *FDC1004: Basics of Capacitive Sensing and Applications* application note.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 The Shield

The FDC1004-Q1 measures capacitance between CINn and ground. That means any capacitance to ground on signal path between the FDC1004-Q1 CINn pins and sensor is included in the FDC1004-Q1 conversion result.

In some applications, the parasitic capacitance of the sensor connections can be larger than the capacitance of the sensor. If that parasitic capacitance is stable, the capacitance can be treated as a constant capacitive offset. However, the parasitic capacitance of the sensor connections can have significant variation due to environmental changes (such as mechanical movement, temperature shifts, humidity changes). These changes are seen as drift in the conversion result and can significantly compromise the system accuracy.

To eliminate the CINn parasitic capacitance to ground, the FDC1004-Q1 SHLDx signals can be used for shielding the connection between the sensor and CINn. The SHLDx output is the same signal waveform as the excitation of the CINn pin; the SHLDx is driven to the same voltage potential as the CINn pin. Therefore, there is no current between CINn and SHLDx pins, and any capacitance between these pins does not affect the CINn charge transfer. Ideally, the CINn to SHLD capacitance does not have any contribution to the FDC1004-Q1 result.

In differential measurements, SHLD1 is assigned to CHn and SHLD2 is assigned to CHm, where n < m. For instance in the measurement CIN1 – CIN2, where CHA = CIN1 and CHB = CIN2 (see 表 6-4), SHDL1 is assigned to CIN1 and SHDL2 is assigned to CIN2.

In a single ended configuration, such as CINn vs. GND, SHLD1 is internally shorted to SHLD2. In a single ended configuration, such as CINn versus GND with CAPDAC enabled, SHLD1 is assigned to the selected channel, SHLD2 is floating.

For best results, locate the FDC1004-Q1 as close as possible to the capacitive sensor. Minimize the connection length between the sensor and FDC1004-Q1 CINn pins and between the sensor ground and the FDC1004-Q1 GND pin. Shield the PCB traces to the CINn pins and connect the shielding to the FDC1004-Q1 SHLDx pins. In addition, if a shielded cable is used to connect the FDC1004-Q1 to the sensor, connect the shield to the appropriate SHLDx pin. In applications where only one SHLDx pin is used, the unused SHLDx pin can be left unconnected.

For more information on how to design a sensor with a shield, refer to the *Capacitive Sensing: Ins and Outs of Active Sensing* application note.

6.3.2 The CAPDAC

The FDC1004-Q1 full-scale input range is ±15pF. The part can accept a higher capacitance on the input and the common-mode or offset (constant component) capacitance can be balanced by the programmable on-chip CAPDACs. The CAPDAC can be viewed as a negative capacitance connected internally to the CINn pin. The relation between the input capacitance and output data can be expressed as DATA = (CINn – CAPDAC), n = 1...4. The CAPDACs have a 5-bit resolution, monotonic transfer function, are well matched to each other, and have a defined temperature coefficient.

6.3.3 Capacitive System Offset Calibration

The capacitive offset can be due to many factors including the initial capacitance of the sensor, parasitic capacitances of board traces, and the capacitance of any other connections between the sensor and the FDC.

The parasitic capacitances of the FDC1004-Q1 are calibrated out at production. If there are other sources of offset in the system, it can be necessary to calibrate the system capacitance offset in the application. Any offset in the capacitance input larger than ½ LSB of the CAPDAC should first be removed using the on-chip CAPDACs. Any residual offset of approximately 1pF can then be removed by using the capacitance offset calibration register. The offset calibration register is reloaded by the default value at power-on or after reset. Therefore, if the offset calibration is not repeated after each system power-up, the calibration coefficient value should be stored by the host controller and reloaded as part of the FDC1004-Q1 setup.

6.3.4 Capacitive Gain Calibration

The gain is factory calibrated up to ±15pF in the production for each part individually. The factory gain coefficient is stored in a one-time programmable (OTP) memory.

The gain can be temporarily changed by setting the Gain Calibration Register (registers 0x11 to 0x14) for the appropriate CINn pin, although the factory gain coefficient is restored after power-up or reset.

The part is tested and specified for use only with the default factory calibration coefficient. Adjusting the Gain calibration can be used to normalize the capacitance measurement of the CINn input channels.

6.4 Device Functional Modes

6.4.1 Single Ended Measurement

The FDC1004-Q1 can be used for interfacing to a single-ended capacitive sensor. In this configuration, connect the sensor to the input CINn (n = 1..4) pins of the FDC1004-Q1 and GND. The capacitance-to-digital convertor (without using the CAPDAC, CAPDAC= 0pF) measures the positive (or the negative) input capacitance in the range of 0pF to 15pF. The CAPDAC can be used for programmable shifting of the input range. In this case it is possible to measure input capacitance in the range of 0pF to ±15pF which are on top of an offset capacitance up to 100pF. In single ended measurements with CAPDAC disabled SHLD1 is internally shorted to SHLD2 (see 図 6-1); if CAPDAC is enabled SHLD2 is floating (see 図 6-2). The single ended mode is enabled when the CHB register of the Measurements configuration registers (see 表 6-4) are set to b100 or b111.

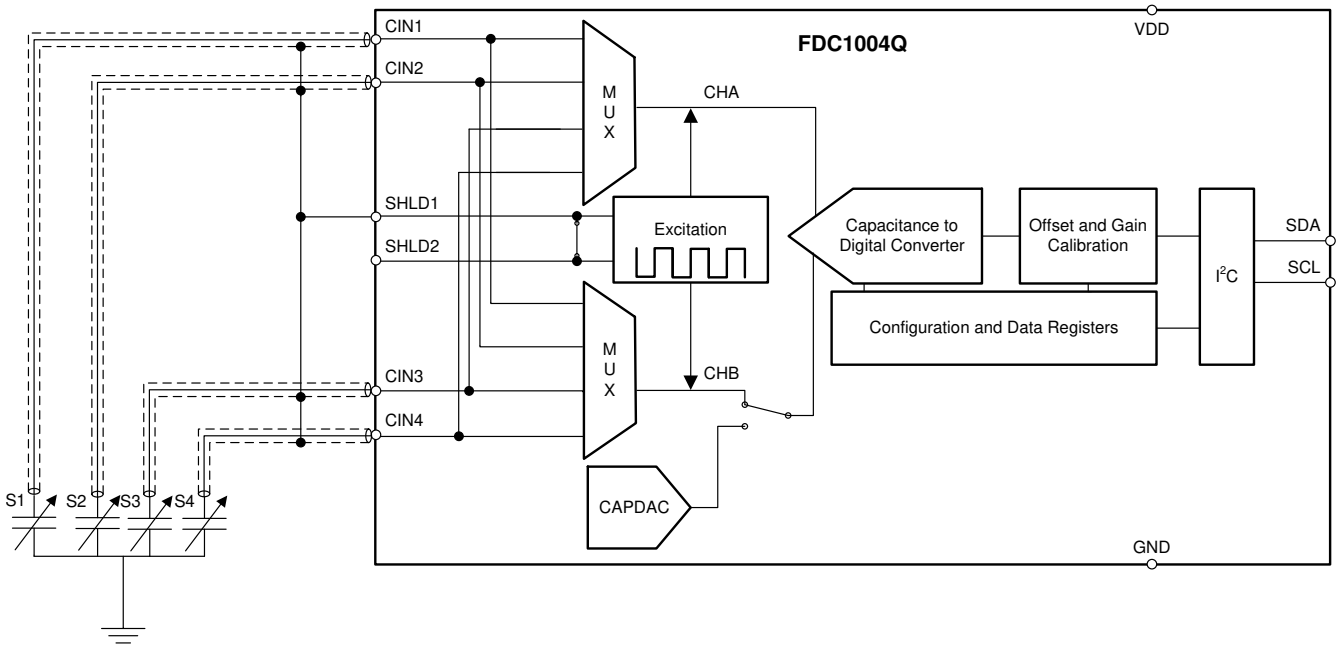


図 6-1. Single-Ended Configuration with CAPDAC Disabled

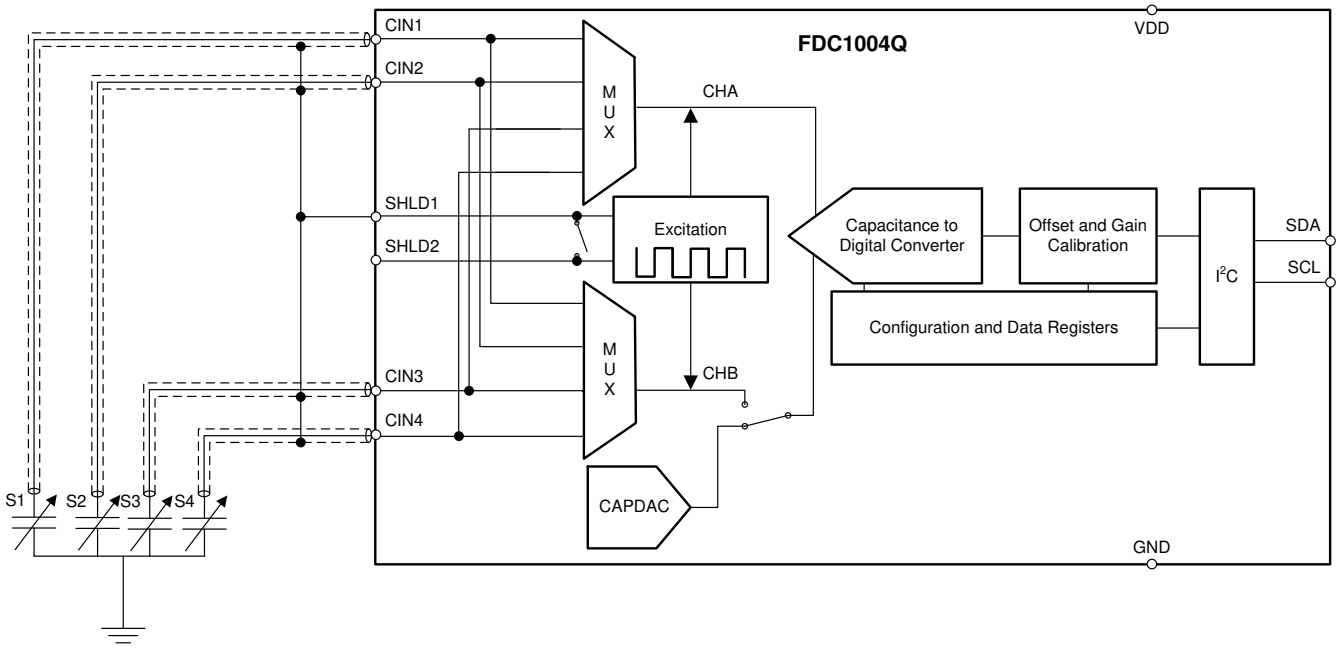


図 6-2. Single-Ended Configuration with CAPDAC Enabled

6.4.2 Differential Measurement

When the FDC1004-Q1 is used for interfacing to a differential capacitive sensor, each of the two input capacitances must be less than 115pF. In this configuration the CAPDAC is disabled. Keep the absolute value of the difference between the two input capacitances below 15pF to avoid introducing errors in the measurement. In differential measurements, SHLD1 is assigned to CHn and SHLD2 is assigned to CHm, where n < m. For instance in the measurement CIN1 – CIN2, where CHA = CIN1 and CHB = CIN2 (see 表 6-4), SHDL1 is assigned to CIN1 and SHDL2 is to CIN2. Differential sensors made with S1 versus S3 and S2 versus S4 are shown below in 図 6-3. S1 and S2 are alternatively connected to CHA and the S3 and S4 are alternatively

connected to CHB, the shield signals are connected as explained in previous paragraph. The FDC1004-Q1 performs a differential measurement when CHB field of the Measurements Configuration Registers (refer to 表 6-4) is less than to b100.

This configuration is very useful in applications where environment conditions need to be tracked. The differential measurement between the main electrode and the environment electrode makes the measurement independent of the environment conditions.

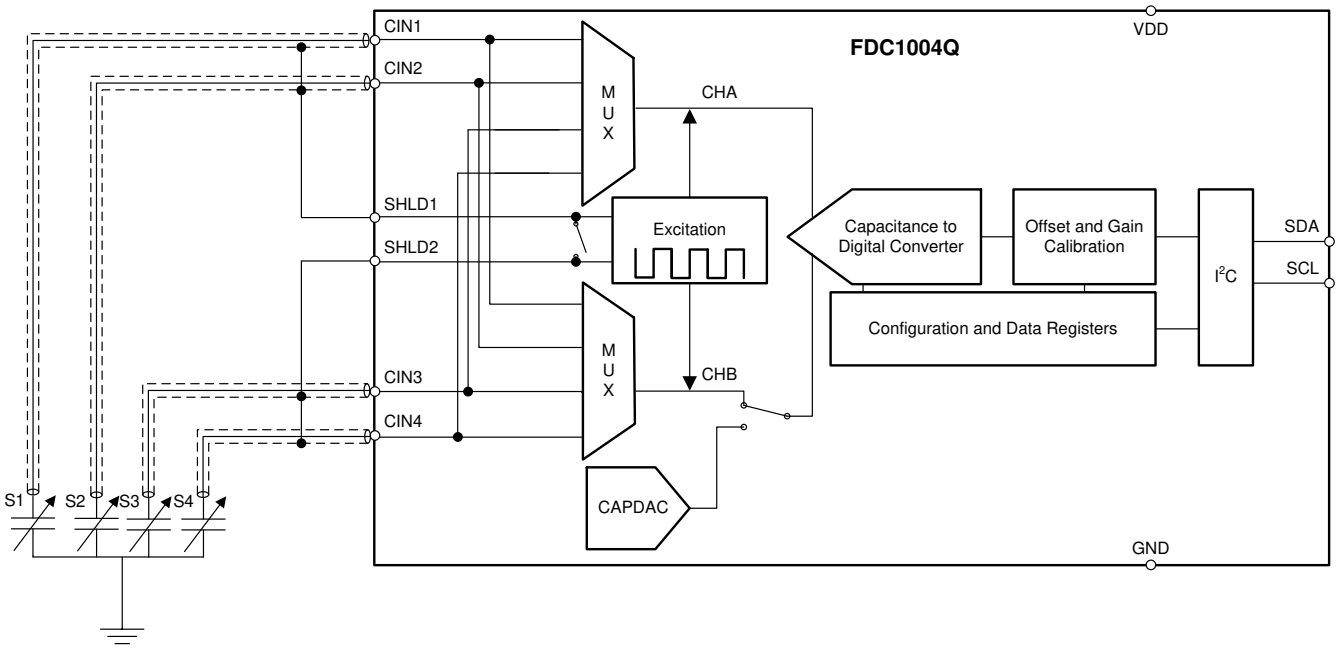


図 6-3. Differential Configuration

6.5 Programming

The FDC1004-Q1 operates only as a target device on the two-wire bus interface. Every device on the bus must have a unique address. Connection to the bus is made via the open-drain I/O lines, SDA, and SCL. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The FDC1004-Q1 supports fast mode frequencies 10kHz to 400kHz. All data bytes are transmitted MSB first.

6.5.1 Serial Bus Address

To communicate with the FDC1004-Q1, the controller must first address target devices via a target address byte. The target address byte consists of seven address bits and a direction bit that indicates the intent to execute a read or write operation. The seven bit address for the FDC1004-Q1 is (MSB first): b101 0000.

6.5.2 Read/Write Operations

Access a particular register on the FDC1004-Q1 by writing the appropriate value to the Pointer Register. The pointer value is the first byte transferred after the target address byte with the R/W bit low. Every write operation to the FDC1004-Q1 requires a value for the pointer register. When reading from the FDC1004-Q1, the last value stored in the pointer by a write operation is used to determine which register is read by a read operation. To change the pointer register for a read operation, a new value must be written to the pointer. This transaction is accomplished by issuing the target address byte with the R/W bit low, followed by the pointer byte. No additional data is required. The controller can then generate a START condition and send the target address byte with the R/W bit high to initiate the read command. Note that register bytes are sent MSB first, followed by the LSB. A write operation in a read only registers such as MANUFACTURER ID or SERIAL ID returns a NACK after each

data byte; read/write operation to unused address returns a NACK after the pointer; a read/write operation with incorrect I_2C address returns a NACK after the I^2C address.

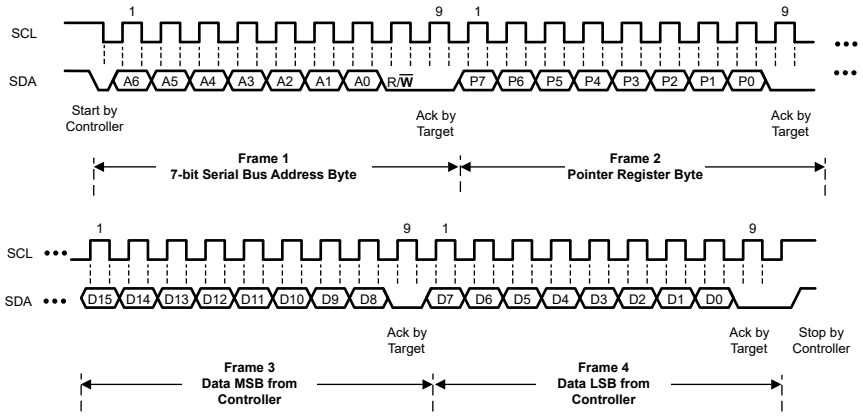


図 6-4. Write Frame

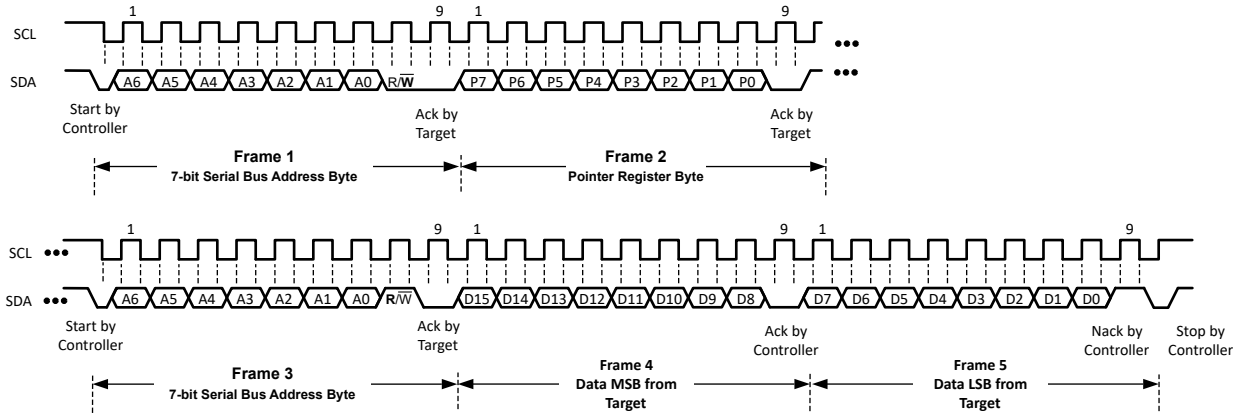


図 6-5. Read Frame

6.5.3 Device Usage

The basic usage model of the FDC1004-Q1 is to simply follow these steps:

1. Configure measurements (for details, refer to *Measurement Configuration*).
2. Trigger a measurement set (for details, refer to *Triggering Measurements*).
3. Wait for measurement completion (for details, refer to *Wait for Measurement Completion*).
4. Read measurement data (for details, refer to *Read of Measurement Result*).

6.5.3.1 Measurement Configuration

Configuring a measurement involves setting the input channels and the type of measurement (single-ended or differential).

The FDC1004-Q1 can be configured with up to 4 separate measurements, where each measurement can be any valid configuration (that is, a specific channel can be used in multiple measurements). There is a dedicated configuration register for each of the 4 possible measurements (for example, MEAS_CONF1 in register 0x08 configures measurement 1, MEAS_CONF2 in register 0x09 configures measurement 2, ...). Configuring only one measurement is allowed, and it can be one of the 4 possible measurement configurations.

1. Set up the input channels for each measurement. Determine which of the 4 measurement configuration registers to use (registers 0x08 to 0x0A) and set the following:

a. For single-ended measurement:
   i. Select the positive input pin for the measurement by setting the CHA field (bits[15:13]).
   ii. Set CAPDAC (bits[9:5]) if the channel offset capacitance is more than 15pF.
b. For a differential measurement:
   i. Select the positive input pin for the measurement by setting the CHA field (bits[15:13]).
   ii. Select the negative input pin for the measurement by setting the CHB field (bits[12:10]). Note that the CAPDAC setting has no effect for a differential measurement.

2. Determine the appropriate sample rate. The sample rate sets the resolution of the measurement. Lower the sample rate higher is the resolution of the measurement.

6.5.3.2 Triggering Measurements

For a single measurement, trigger the desired measurement (that is, which one of the configured measurements) when needed by:

1. Setting REPEAT (Register 0x0C:bit[8]) to 0.
2. Setting the corresponding MEAS_x field (Register 0x0C:bit[7:4]) to 1.
   - For example, to trigger a single measurement of Measurement 2 at a rate of 100S/s, set Address 0x0C to 0x0540.

Note that, at a given time, only one measurement of the configured measurements can be triggered in this manner (that is, MEAS_1 and MEAS_2 cannot both be triggered in a single operation).

The FDC1004-Q1 can also trigger a new measurement on the completion of the previous measurement (repeated measurements). This is set up by:

1. Setting REPEAT (Register 0x0C:bit[8]) to 1.
2. Setting the corresponding MEAS_x field (Register 0x0C:bit[7:4]) to 1.

When the FDC1004-Q1 is setup for repeated measurements, multiple configured measurements (up to a maximum of 4) can be performed in this manner, but Register 0x0C must be written in a single transaction.

6.5.3.3 Wait for Measurement Completion

Wait for the triggered measurements to complete. When the measurements are complete, the corresponding DONE_x field (Register 0x0C:bits[3:0]) is set to 1.

6.5.3.4 Read of Measurement Result

Read the result of the measurement from the corresponding registers:

- 0x00/0x01 for Measurement 1
- 0x02/0x03 for Measurement 2
- 0x04/0x05 for Measurement 3
- 0x06/0x07 for Measurement 4

The measurement results span 2 register addresses; both registers must be read to have a complete conversion result. The lower address (for example, 0x00 for Measurement 1) must be read first, then the upper address read afterwards (for example, 0x01 for Measurement 1).

When the measurement read is complete, the corresponding DONE_x field (Register 0x0C:bits[3:0]) returns to 0.

If an additional single triggered measurement is desired, simply perform the Trigger, Wait, Read steps again.

If the FDC1004-Q1 is set up for repeated measurements (Register 0x0C:bit[8]) = 1), the FDC1004-Q1 continuously measures until the REPEAT field (Register 0x0C:bit[8]) is set to 0, even if the results are not read back.

6.6 Register Maps

表 6-1. Register Map

Pointer	Register Name	Reset Value	Description
0x00	MEAS1_MSB	0x0000	MSB portion of Measurement 1

表 6-1. Register Map (続き)

Pointer	Register Name	Reset Value	Description
0x01	MEAS1_LSB	0x0000	LSB portion of Measurement 1
0x02	MEAS2_MSB	0x0000	MSB portion of Measurement 2
0x03	MEAS2_LSB	0x0000	LSB portion of Measurement 2
0x04	MEAS3_MSB	0x0000	MSB portion of Measurement 3
0x05	MEAS3_LSB	0x0000	LSB portion of Measurement 3
0x06	MEAS4_MSB	0x0000	MSB portion of Measurement 4
0x07	MEAS4_LSB	0x0000	LSB portion of Measurement 4
0x08	CONF_MEAS1	0x1C00	Measurement 1 Configuration
0x09	CONF_MEAS2	0x1C00	Measurement 2 Configuration
0x0A	CONF_MEAS3	0x1C00	Measurement 3 Configuration
0x0B	CONF_MEAS4	0x1C00	Measurement 4 Configuration
0x0C	FDC_CONF	0x0000	Capacitance to Digital Configuration
0x0D	OFFSET_CAL_CIN1	0x0000	CIN1 Offset Calibration
0x0E	OFFSET_CAL_CIN2	0x0000	CIN2 Offset Calibration
0x0F	OFFSET_CAL_CIN3	0x0000	CIN3 Offset Calibration
0x10	OFFSET_CAL_CIN4	0x0000	CIN4 Offset Calibration
0x11	GAIN_CAL_CIN1	0x4000	CIN1 Gain Calibration
0x12	GAIN_CAL_CIN2	0x4000	CIN2 Gain Calibration
0x13	GAIN_CAL_CIN3	0x4000	CIN3 Gain Calibration
0x14	GAIN_CAL_CIN4	0x4000	CIN4 Gain Calibration
0xFE	Manufacturer ID	0x5449	ID of Texas Instruments
0xFF	Device ID	0x1004	ID of FDC1004-Q1 device

Registers from 0x15 to 0xFD are reserved and should not be written to.

6.6.1 Registers

The FDC1004-Q1 has an 8-bit pointer used to address a given data register. The pointer identifies which of the data registers should respond to a read or write command on the two-wire bus. This register is set with every write command. A write command must be issued to set the proper value in the pointer before executing a read command. The power-on reset (POR) value of the pointer is 0x00.

6.6.1.1 Capacitive Measurement Registers

The capacitance measurement registers are 24-bit result registers in binary format (the 8 LSBs D[7:0] are always 0x00). The result of the acquisition is always a 24 bit value, while the accuracy is related to the selected conversion time (refer to). The data is encoded in a Two's complement format. The result of the measurement can be calculated by the following formula:

$$\text{Capacitance (pf)} = ((\text{Two's Complement (measurement [23:0])}) / 2^{19}) + C_{offset} \quad (1)$$

where

- C_{offset} is based on the CAPDAC setting.

6.6.2 Measurement Registers

表 6-2. Measurement Registers Description (0x00, 0x02, 0x04, 0x06)

Field Name	Bits	Description
MSB_MEASn(1)	[15:0]	Most significant 16 bits of Measurement n (read only)

(1) MSB_MEAS1 = register 0x00, MSB_MEAS2 = register 0x02, MSB_MEAS3 = register 0x04, MSB_MEAS4 = register 0x06

表 6-3. Measurement Registers Description (0x01, 0x03, 0x05, 0x07)

Field Name	Bits		Description
LSB_MEASn(1)	[15:8]		Least significant 8 bits of Measurement n (read only)
	[7:0]	Reserved	Reserved, always 0 (read only)

(1) LSB_MEAS1 = register 0x01, LSB_MEAS2 = register 0x03, LSB_MEAS3 = register 0x05, LSB_MEAS4 = register 0x07

6.6.3 Measurement Configuration Registers

These registers configure the input channels and CAPDAC setting for a measurement.

表 6-4. Measurement Configuration Registers Description (0x08, 0x09, 0x0A, 0x0B)

Field Name	Bits			Description
CHA(1) (2)	[15:13]	Positive input channel capacitive to digital converter	b000	CIN1
			b001	CIN2
			b010	CIN3
			b011	CIN4
CHB(1) (2)	[12:10]	Negative input channel capacitive to digital converter	b000	CIN1
			b001	CIN2
			b010	CIN3
			b011	CIN4
			b100	CAPDAC
			b111	DISABLED
CAPDAC	[9:5]	Offset Capacitance	b00000	0pF (minimum programmable offset)
			- - - - -	Configure the single-ended measurement capacitive offset: C_{offset} = CAPDAC x 3.125pF
			b11111	96.875pF (maximum programmable offset)
RESERVED	[04:00]	Reserved		Reserved, always 0 (read only)

(1) **It is not permitted to configure a measurement where the CHA field and CHB field hold the same value (for example, if CHA=b010, CHB cannot also be set to b010).**

(2) **It is not permitted to configure a differential measurement between CHA and CHB where CHA > CHB (for example, if CHA= b010, CHB cannot be b001 or b000).**

6.6.4 FDC Configuration Register

This register configures measurement triggering and reports measurement completion.

表 6-5. FDC Register Description (0x0C)

Field Name	Bits			Description
RST	[15]	Reset	0	Normal operation
			1	Software reset: write a 1 to initiate a device reset; after completion of reset, this field returns to 0
RESERVED	[14:12]	Reserved		Reserved, always 0 (read only)
RATE	[11:10]	Measurement Rate	b00	Reserved
			b01	100S/s
			b10	200S/s
			b11	400S/s
RESERVED	[9]	Reserved		Reserved, always 0 (read only)
REPEAT	[8]	Repeat Measurements	0	Repeat disabled
			1	Repeat enabled, all the enabled measurement are repeated
MEAS_1	[7]	Initiate Measurements	0	Measurement 1 disabled
			1	Measurement 1 enabled
MEAS_2	[6]	Initiate Measurements	0	Measurement 2 disabled
			1	Measurement 2 enabled
MEAS_3	[5]	Initiate Measurements	0	Measurement 3 disabled
			1	Measurement 3 enabled
MEAS_4	[4]	Initiate Measurements	0	Measurement 4 disabled
			1	Measurement 4 enabled
DONE_1	[3]	Measurement Done	0	Measurement 1 not completed
			1	Measurement 1 completed
DONE_2	[2]	Measurement Done	0	Measurement 2 not completed
			1	Measurement 2 completed
DONE_3	[1]	Measurement Done	0	Measurement 3 not completed
			1	Measurement 3 completed
DONE_4	[0]	Measurement Done	0	Measurement 4 not completed
			1	Measurement 4 completed

6.6.5 Offset Calibration Registers

These registers configure a digitized capacitance value in the range of –16pF to 16pF (maximum residual offset 250 aF) that can be added to each channel to remove parasitic capacitance due to external circuitry. In addition to the offset calibration capacitance which is a fine-tune offset capacitance, it is possible to support a larger offset by using the CAPDAC (for up to 100pF). These 16-bit registers are formatted as a fixed point number, where the first 5 bits represents the integer portion of the capacitance in Two's complement format, and the remaining 11 bits represent the fractional portion of the capacitance.

表 6-6. Offset Calibration Registers Description (0x0D, 0x0E, 0x0F, 0x10)

Field Name	Bits		Description
OFFSET_CALn(1)	[15:11]	Integer part	Integer portion of the Offset Calibration of Channel CINn
	[10:0]	Decimal part	Decimal portion of the Offset Calibration of Channel CINn

(1) OFFSET_CAL1 = register 0x0D, OFFSET_CAL2 = register 0x0E, OFFSET_CAL3 = register 0x0F, OFFSET_CAL4 = register 0x10

6.6.6 Gain Calibration Registers

These registers contain a gain factor correction in the range of 0 to 4 that can be applied to each channel to remove gain mismatch due to the external circuitry. This 16-bit register is formatted as a fixed point number, where the 2 MSBs of the GAIN_CALn register correspond to an integer portion of the gain correction, and the remaining 14 bits represent the fractional portion of the gain correction. The result of the conversion represents a number without dimensions.

The Gain can be set according to the following formula:

Gain = GAIN_CAL[15:0]/2^{14}

表 6-7. Gain Calibration Registers Description (0x11, 0x12, 0x13, 0x14)

Field Name	Bits		Description
GAIN_CALn(1)	[15:14]	Integer part	Integer portion of the Gain Calibration of Channel CINn
	[13:0]	Decimal part	Decimal portion of the Gain Calibration of Channel CINn

(1) GAIN_CAL1 = register 0x11, GAIN_CAL2 = register 0x12, GAIN_CAL3 = register 0x13, GAIN_CAL4 = register 0x14

6.6.7 Manufacturer ID Register

This register contains a factory-programmable identification value that identifies this device as being manufactured by Texas Instruments. This register distinguishes this device from other devices that are on the same I^2C bus. The manufacturer ID reads 0x5449.

表 6-8. Manufacturer ID Register Description (0xFE)

Field Name	Bits			Description
MANUFACTURER ID	[15:0]	Manufacturer ID	0x5449h	Texas instruments ID (read only)

6.6.8 Device ID Register

This register contains a factory-programmable identification value that identifies this device as a FDC1004-Q1. This register distinguishes this device from other devices that are on the same I^2C bus. The Device ID for the FDC1004-Q1 is 0x1004.

表 6-9. Device ID Register Description (0xFF)

Field Name	Bits			Description
DEVICE ID	[15:0]	Device ID	0x1004	FDC1004-Q1 Device ID (read only)

7 Applications and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

7.1.1 Liquid Level Sensor

The FDC1004-Q1 can be used to measure liquid level in non-conductive containers. Capacitive sensors can be attached to the outside of the container or be located remotely from the container, allowing for contact-less measurements. The working principle is based on a ratiometric measurement; 図 7-1 shows a possible system implementation which uses three electrodes. The Level electrode provides a capacitance value proportional to the liquid level. The Reference Environmental electrode and the Reference Liquid electrode are used as references. The Reference Liquid electrode accounts for the liquid dielectric constant and variation, while the Reference Environmental electrode is used to compensate for any other environmental variations that are not due to the liquid itself. Note that the Reference Environmental electrode and the Reference Liquid electrode are the same physical size (h_{REF}).

For this application, single-ended measurements on the appropriate channels are appropriate, as the tank is grounded.

Use the following formula to determine the liquid level from the measured capacitances:

$$Level = h_{ref} \frac{C_{Lev} - C_{Lev}(0)}{C_{RL} - C_{RE}}$$

where

- C_{RE} is the capacitance of the Reference Environmental electrode,
- C_{RL} is the capacitance of the Reference Liquid electrode,
- C_{Lev} is the current value of the capacitance measured at the Level electrode sensor,
- $C_{Lev}(0)$ is the capacitance of the Level electrode when the container is empty, and
- h_{REF} is the height in the desired units of the Container or Liquid Reference electrodes.

The ratio between the capacitance of the level and the reference electrodes allows simple calculation of the liquid level inside the container itself. Very high sensitivity values (that is, many LSB/mm) can be obtained due to the high resolution of the FDC1004-Q1, even when the sensors are located remotely from the container.

For more information on a robust liquid level sensing technique, refer to application note *Capacitive Sensing: Out-of-Phase Liquid Level Technique* application note and the (*TIDA-00317 Capacitive-Based Liquid Level Sensing Sensor Reference Design*).

7.2 Typical Application

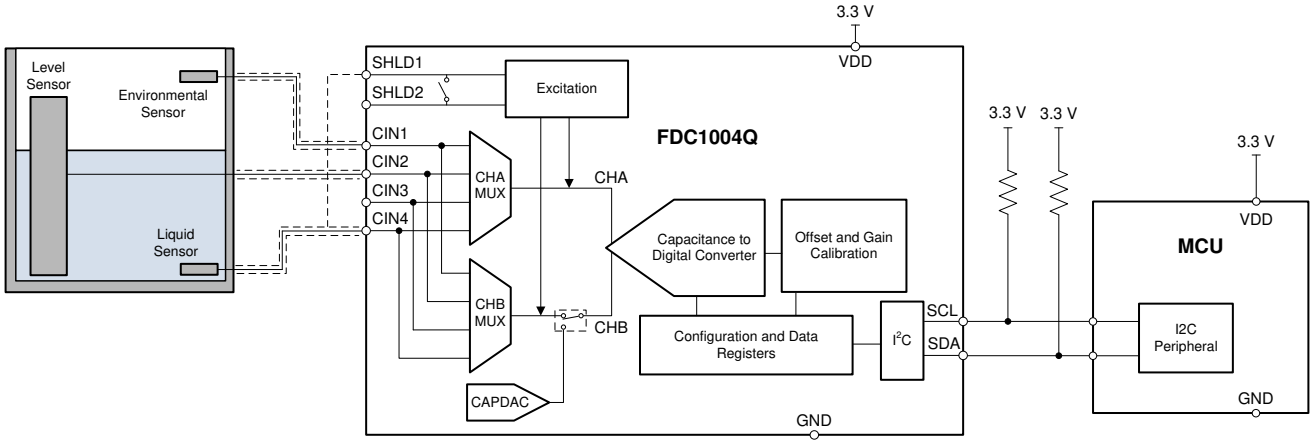


図 7-1. FDC1004-Q1 (Liquid Level Measurement)

7.2.1 Design Requirements

Make sure the liquid level measurement is independent of the liquid, which can be achieved using the 3-electrode design described above. Moreover, make sure the sensor is immune to environmental interferences such as a human body, other objects, or EMI. This can be achieved by shielding the side of the sensor which does not face the container.

7.2.2 Detailed Design Procedure

In capacitive sensing systems, the design of the sensor plays an important role in determining system performance and capabilities. In most cases the sensor is simply a metal plate that can be designed on the PCB.

The sensor used in this example is implemented with a two-layer PCB. On the top layer, which faces the tank, there are the 3 electrodes (Reference Environmental, Reference Liquid, and Level) with a ground plane surrounding the electrodes. The bottom layer is covered with a shield plane to isolate the electrodes from any external interference sources.

Depending on the shape of the container, the FDC1004-Q1 can be located on the sensor PCB to minimize the length of the traces between the input channels and the sensors and increase the immunity from EMI sources. In case the shape of the container or other mechanical constraints do not allow having the sensors and the FDC1004-Q1 on the same PCB, the traces which connect the channels to the sensor need to be shielded with the appropriate shield. In this design example all of the channels are shielded with SHLD1. For this configuration, the FDC1004-Q1 measures the capacitance of the 3 channels versus ground; and so the SHLD1 and SHLD2 pins are internally shorted in the FDC1004-Q1 (see *The Shield*).

7.2.3 Application Curve

The data shown below has been collected with the FDC1004QEVM. A liquid level sensor with 3 electrodes like the one shown in the schematic was connected to the EVM. The plot shows the capacitance measured by the 3 electrodes at different levels of liquid in the tank. The capacitance of the Reference Liquid (the RF trace in the graph below) and Reference Environmental (the RE trace) sensors have a steady value when the liquid is above their height while the capacitance of the level sensor (Level) increases linearly with the height of the liquid in the tank.

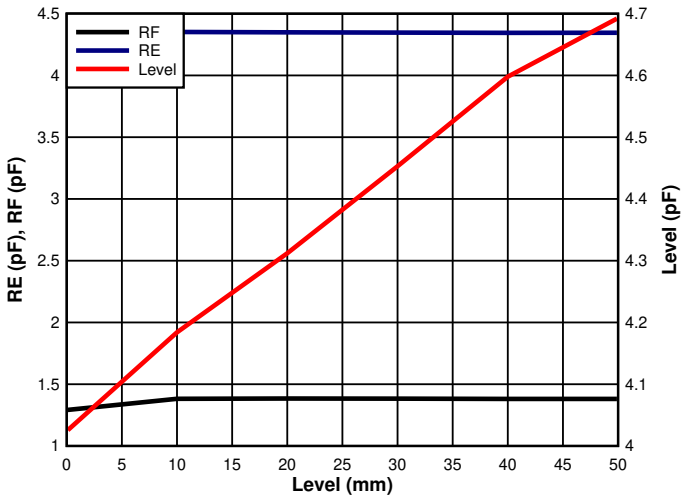


図 7-2. Electrode Capacitance vs Liquid Level

7.3 Best Design Practices

Avoid long traces to connect the sensor to the FDC1004-Q1. Short traces reduce parasitic capacitances between shield versus input channel and parasitic resistance between input channel versus GND and shield versus GND.

The sensor in many cases is simply a metal surface on a PCB, therefore the sensor must be protected with solder resist to avoid short circuits and limit any corrosion. Any change in the sensor can result in a change in system performance.

7.4 Initialization Set Up

At power on the device is in standby. The FDC1004-Q1 stays in this mode until a measurement is triggered.

7.5 Power Supply Recommendations

The FDC1004-Q1 requires a voltage supply within 3V and 3.6V. Two multilayer ceramic bypass X7R capacitors of 0.1µF and 1µF, respectively between VDD and GND pin are recommended. Make sure the 0.1µF capacitor is closer to the VDD pin than the 1µF capacitor.

7.6 Layout

7.6.1 Layout Guidelines

The FDC1004-Q1 measures the capacitances connected between the CINn (n=1..4) pins and GND. To get the best result, locate the FDC1004-Q1 as close as possible to the capacitive sensor. Minimize the connection length between the sensor and FDC1004-Q1 CINn pins and between the sensor ground and the FDC1004-Q1 GND pin. If a shielded cable is used for remote sensor connection, connect the shield to the SHLDm (m=1...2) pin according to the configured measurement.

7.6.2 Layout Example

図 7-3 below is optimized for applications where the sensor is not too far from the FDC1004-Q1. Each channel trace runs between 2 shield traces. This layout allows the measurements of 4 single ended capacitance or 2 differential capacitance. The ground plane needs to be far from the channel traces, it is mandatory around or below the I^2C pin.

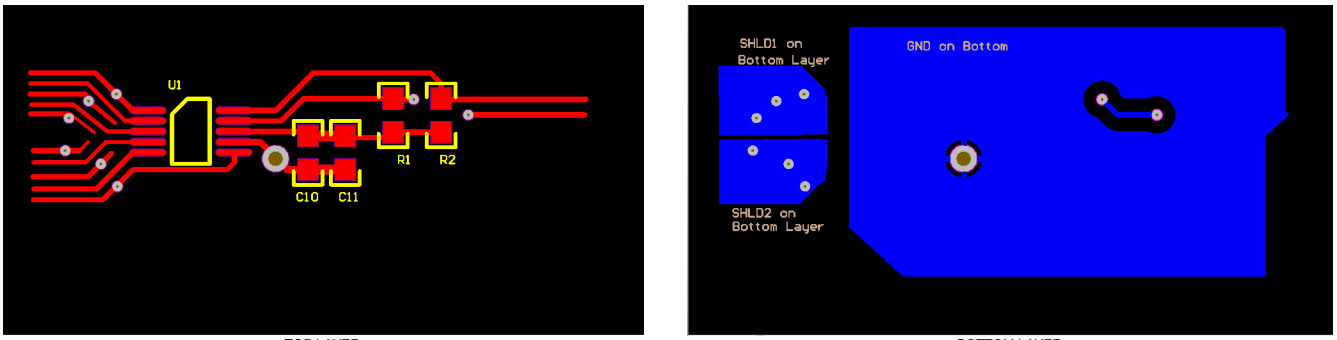


図 7-3. Layout

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *FDC1004: Basics of Capacitive Sensing and Applications* application note
- Texas Instruments, *Capacitive Sensing: Ins and Outs of Active Sensing* application note
- Texas Instruments, *Capacitive Sensing: Out-of-Phase Liquid Level Technique* application note
- Texas Instruments, *Capacitive Proximity Sensing Using the FDC1004* application note
- Texas Instruments, *Ice Buildup Detection Using TI's Capacitive Sensing Technology - FDC1004* application note

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

8.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

Changes from Revision * (April 2015) to Revision A (October 2024)	Page
• データシートのタイトルを『FDC1004Q 4 チャネル キャパシタンス-デジタル コンバータ、静電容量式検出ソリューション用』から『FDC1004-Q1 4 チャネル キャパシタンス-デジタル コンバータ、静電容量式検出アプリケーション用』に変更	1
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• I^2C に言及している場合、すべての旧式の用語をコントローラおよびターゲットに変更	1
• 「製品情報」表を「パッケージ情報」に変更	1
• Added Parameter not tested in production	6
• Changed CINx to CINn throughout	10

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
FDC1004QDGSRQ1	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	ZAOX
FDC1004QDGSRQ1.A	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	ZAOX
FDC1004QDGSTQ1	Obsolete	Production	VSSOP (DGS) | 10	-	-	Call TI	Call TI	-40 to 125	ZAOX

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF FDC1004-Q1 :

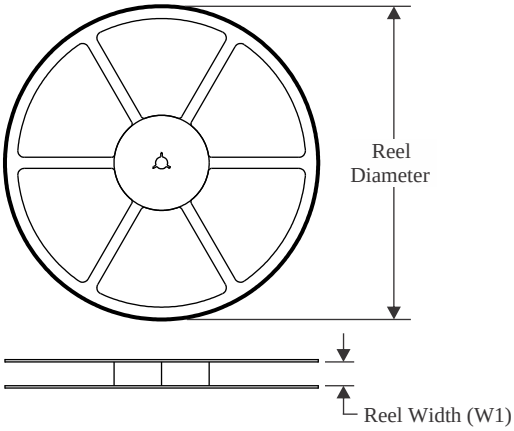
- Catalog : FDC1004

NOTE: Qualified Version Definitions:

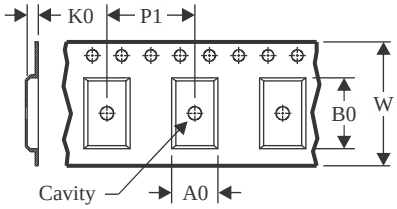
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

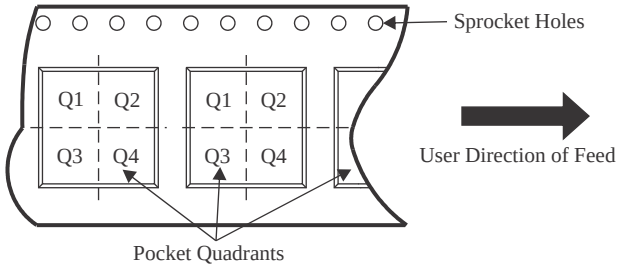


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

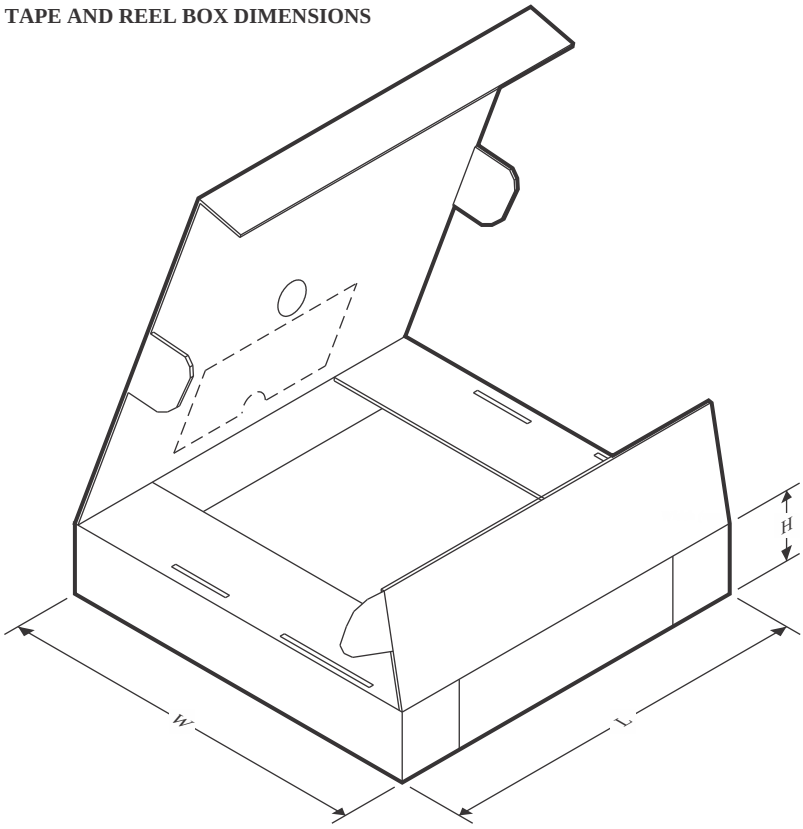
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
FDC1004QDGSRQ1	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

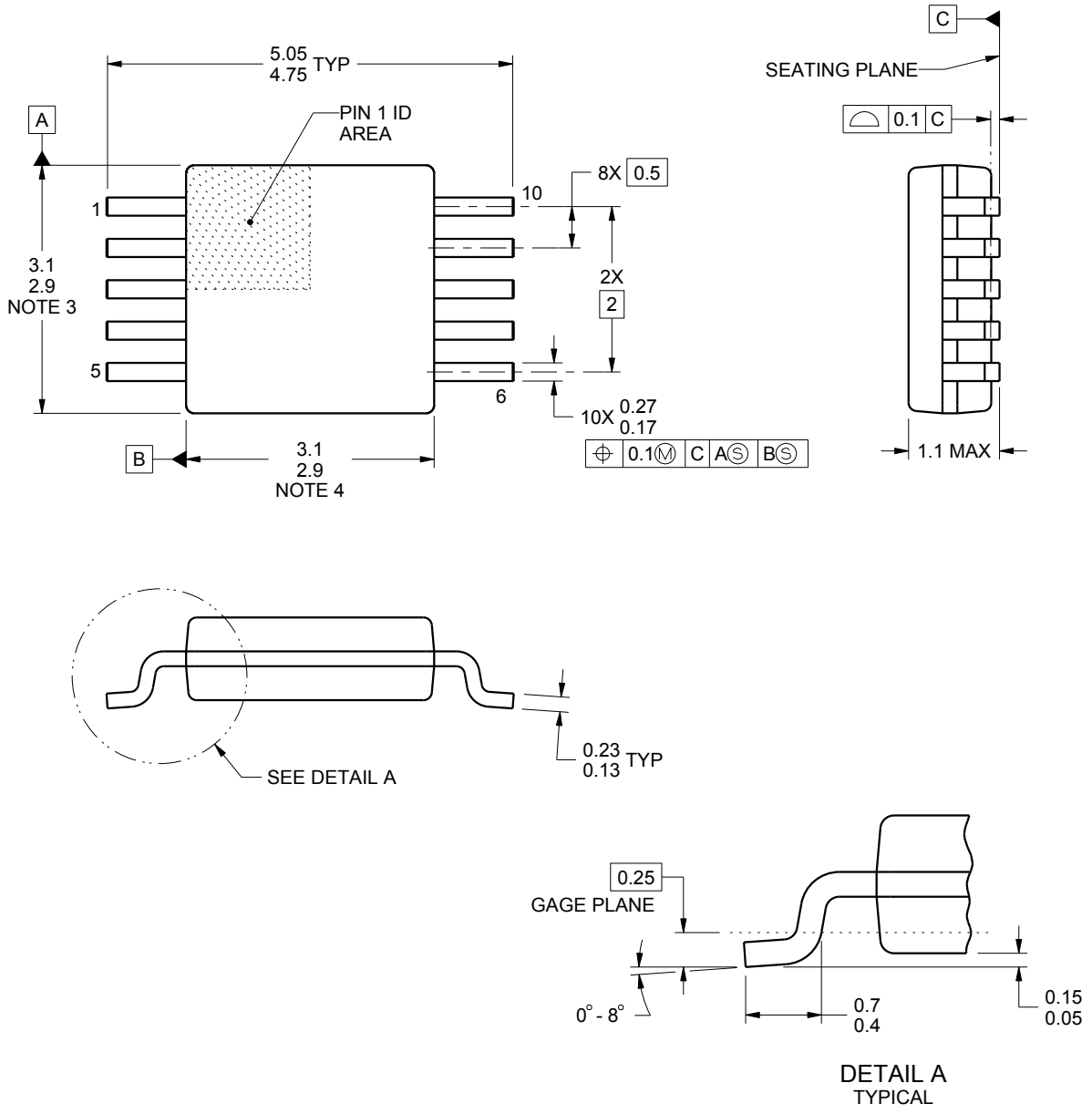
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
FDC1004QDGSRQ1	VSSOP	DGS	10	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGS0010A

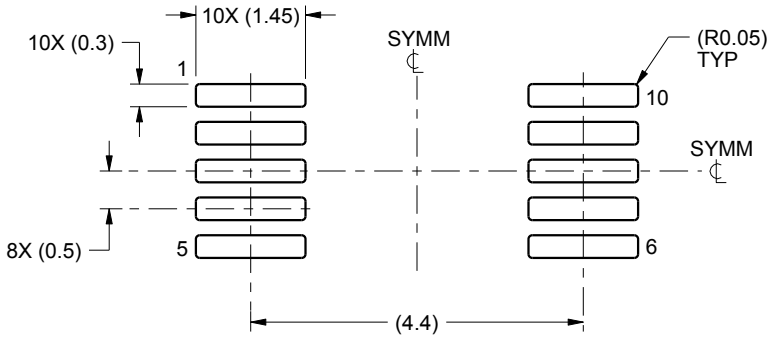
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

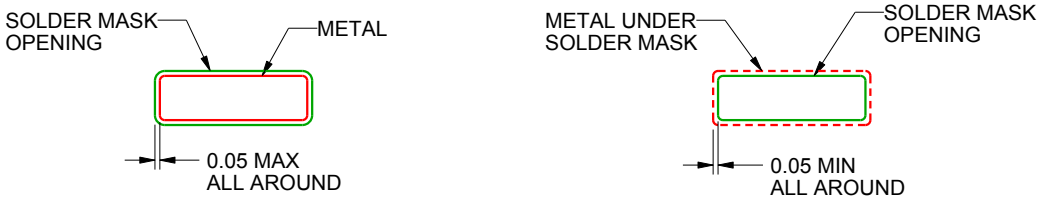


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

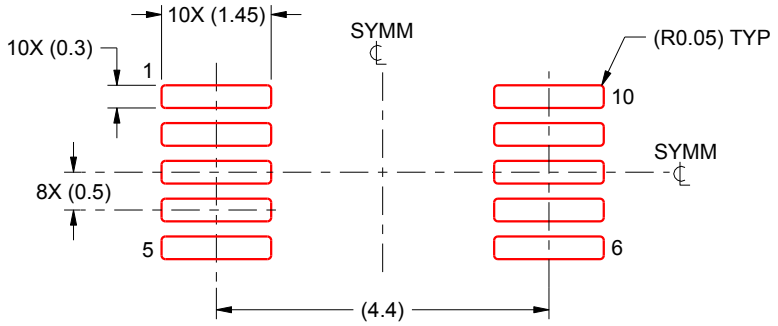


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265