

ESD1LIN24 24-V、1 チャネル ESD 保護ダイオード

1 特長

- IEC 61000-4-2 レベル 4 ESD 保護
 - 接触放電 $\pm 30\text{kV}$
 - 空中放電 $\pm 30\text{kV}$
- 強力なサージ保護:
 - IEC 61000-4-5 (8/20 μs): 4.3A
- 24V の動作電圧
- 双方向 ESD 保護
- 下流の部品を保護する低いクランピング電圧
- 温度範囲: $-55^{\circ}\text{C} \sim +150^{\circ}\text{C}$
- I/O 容量: 2.3pF (標準値)
- 業界標準パッケージで提供: SOD-323 (DYF)
- 自動光学検査 (AOI) に適したリード付きパッケージ

2 アプリケーション

- USB Power Delivery (USB-PD)
 - VBUS 保護
 - IO 保護
- 産業用制御ネットワーク:
 - LIN (Local Interconnect Network)
 - シングル・ライン CAN ESD 保護
 - DeviceNet
 - スマート・ディストリビューション・システム

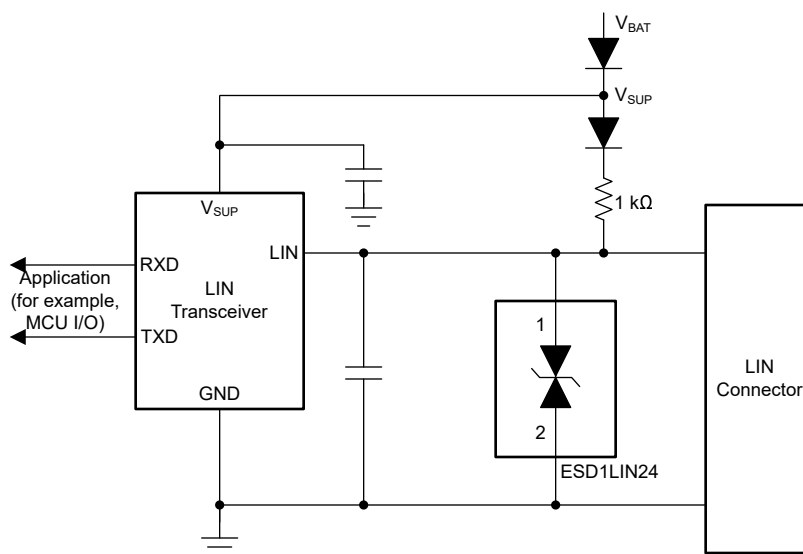
3 概要

ESD1LIN24 は、ローカル相互接続ネットワーク (LIN) 用のシングル・チャネル、低容量、双方向の ESD 保護デバイスです。このデバイスは、IEC 61000-4-2 国際規格に規定されている最大レベルを超える接触 ESD 衝撃 (接触 $\pm 30\text{kV}$ 、エアギャップ $\pm 30\text{kV}$) を吸収できるように仕様が規定されています。動的抵抗とクランプ電圧が低いため、過渡現象に対するシステム・レベルでの保護に役立ちます。安全システムには高いレベルの堅牢性と信頼性が要求されるため、この保護機能は重要です。

パッケージ情報 (1)

部品番号	パッケージ	本体サイズ (公称)
ESD1LIN24	DYF (SOD-323, 2)	2.50mm × 1.20mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション



Table of Contents

1 特長	1	8.4 Device Functional Modes.....	7
2 アプリケーション	1	9 Application and Implementation	8
3 概要	1	9.1 Application Information.....	8
4 Revision History	2	9.2 Typical Application.....	8
5 Pin Configuration and Functions	3	10 Power Supply Recommendations	9
6 Specifications	4	11 Layout	9
6.1 Absolute Maximum Ratings.....	4	11.1 Layout Guidelines.....	9
6.2 ESD Ratings—JEDEC Specification.....	4	11.2 Layout Example.....	10
6.3 ESD Ratings—IEC Specification.....	4	12 Device and Documentation Support	11
6.4 Recommended Operating Conditions.....	4	12.1 Documentation Support.....	11
6.5 Thermal Information.....	4	12.2 ドキュメントの更新通知を受け取る方法.....	11
6.6 Electrical Characteristics.....	5	12.3 サポート・リソース.....	11
7 Typical Characteristics – ESD1LIN24	6	12.4 Trademarks.....	11
8 Detailed Description	7	12.5 静電気放電に関する注意事項.....	11
8.1 Overview.....	7	12.6 用語集.....	11
8.2 Functional Block Diagram.....	7	13 Mechanical, Packaging, and Orderable Information	11
8.3 Feature Description.....	7		

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (November 2022) to Revision A (December 2022)	Page
• データシートステータスを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions

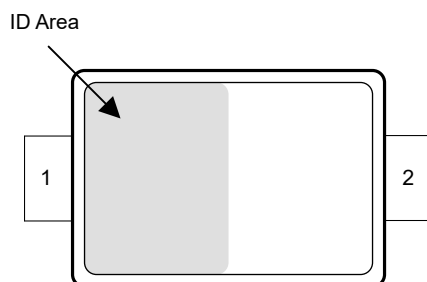


图 5-1. DYF Package, 2-Pin SOD-323 (Top View)

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
IO	1	I/O	ESD protected IO
GND	2	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Peak pulse	IEC 61000-4-5 Power (t_p - 8/20 μ s) at 25°C		159.1	W
	IEC 61000-4-5 current (t_p - 8/20 μ s) at 25°C		4.3	A
T_A	Operating free-air temperature	-55	150	°C
T_{stg}	Storage temperature	-65	155	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002 ⁽²⁾	± 1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air-gap Discharge, all pins	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-24		24	V
T_A	Operating free-air temperature	-55		150	°C

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		ESD1LIN24	UNIT
		DYF (SOD-323)	
		2 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	705.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	315	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	561.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	145	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	550.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

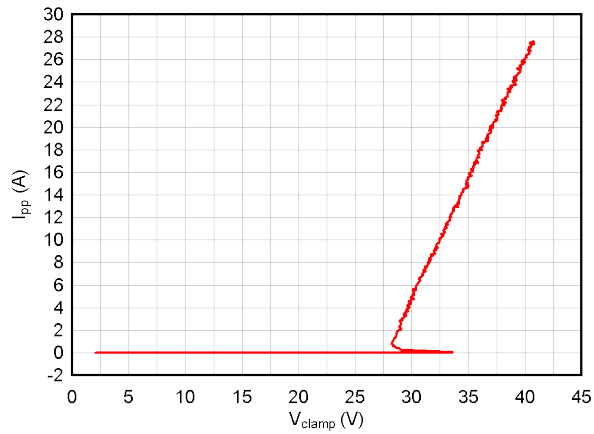
6.6 Electrical Characteristics

over $T_A = 25^\circ\text{C}$ (unless otherwise noted)

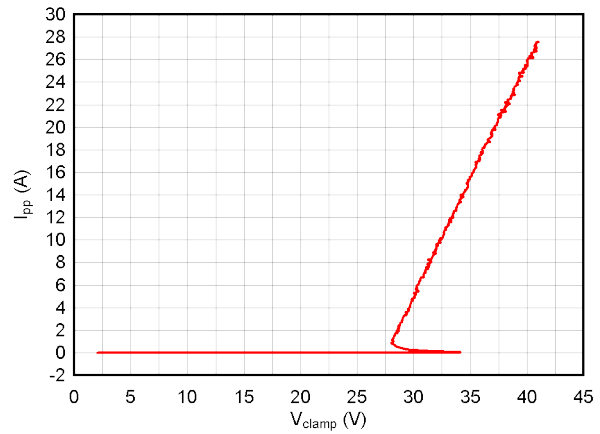
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage		-24		24	V
V_{BRF}	Breakdown voltage ⁽¹⁾	$I_{IO} = 10\text{ mA}$	25.5		35.5	V
V_{BRR}		$I_{IO} = -10\text{ mA}$	-35.5		-25.5	
V_{CLAMP}	Clamping voltage ⁽²⁾	$I_{PP} = 4.3\text{ A}$, $t_p = 8/20\text{ }\mu\text{s}$, from IO to GND		37	42	V
	Clamping voltage ⁽³⁾	$I_{PP} = 16\text{ A}$, TLP, from IO to GND		40		
I_{LEAK}	Leakage current, any IO pin to GND	$V_{IO} = \pm 24\text{ V}$	-50	1	50	nA
R_{DYN}	Dynamic resistance ⁽³⁾			0.5		Ω
C_L	Line capacitance, any IO to GND	$V_{IO} = 0\text{ V}$, $f = 1\text{ MHz}$, $V_{p-p} = 30\text{ mV}$		2.3	3.8	pF

- (1) V_{BRF} and V_{BRR} are defined as the voltage when $\pm 10\text{ mA}$ is applied in the positive-going direction, before the device latches into the snapback state.
- (2) Device stressed with $8/20\text{ }\mu\text{s}$ exponential decay waveform according to IEC 61000-4-5.
- (3) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

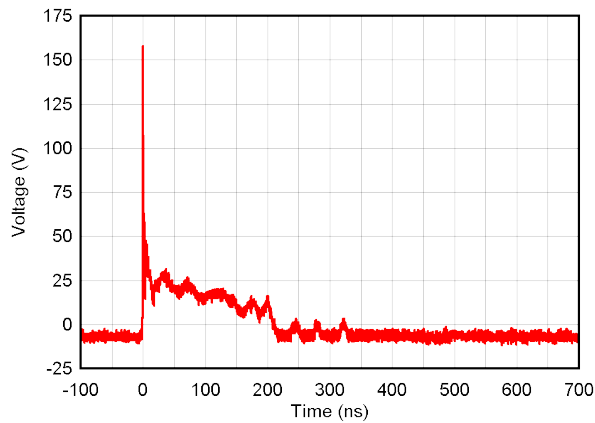
7 Typical Characteristics – ESD1LIN24



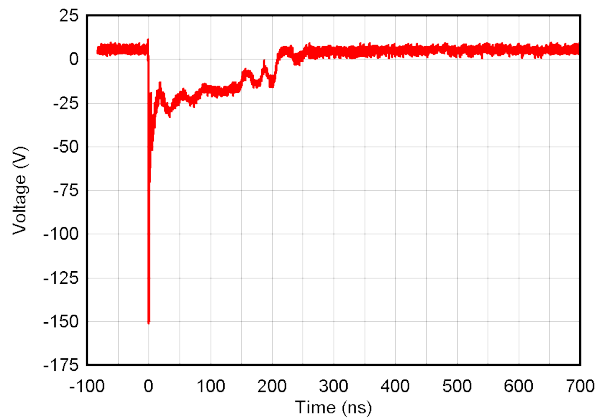
7-1. Positive TLP Curve



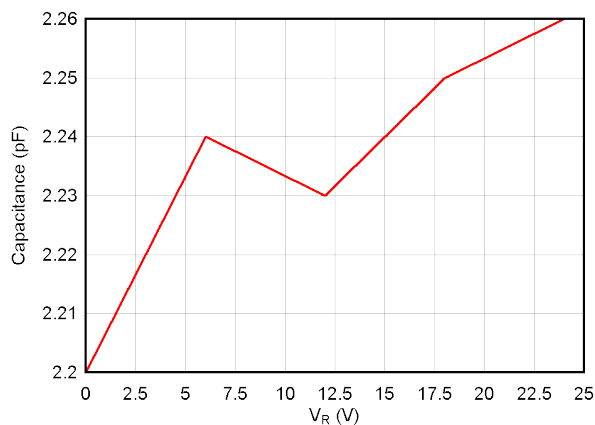
7-2. Negative TLP Curve



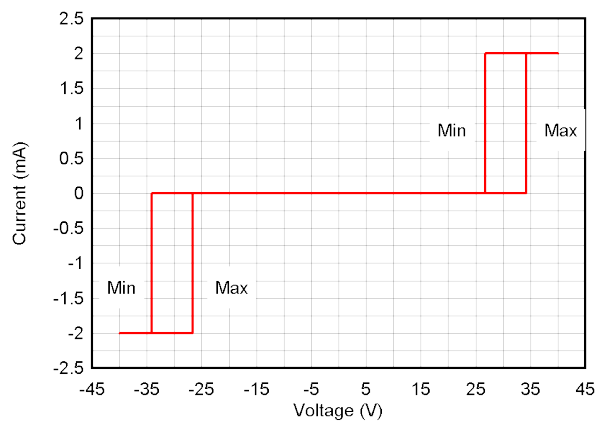
7-3. +8-kV Clamped IEC Waveform



7-4. -8-kV Clamped IEC Waveform



7-5. Capacitance vs. Bias Voltage



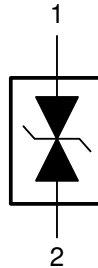
7-6. DC Voltage Sweep I-V Curve

8 Detailed Description

8.1 Overview

The ESD1LIN24 is a single-channel bidirectional ESD diode. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 standard. The low capacitance between the I/O pins make this device suitable for slower speed signals such as LIN, USB-PD, or industrial I/O applications. The surge current capability is suitable for VBUS protection or industrial I/Os requiring 4.3 A of surge current protection.

8.2 Functional Block Diagram



8.3 Feature Description

This clamping device has a small dynamic resistance, which makes the clamping voltage low when the device is actively protecting other circuits. The breakdown is bidirectional so these protection devices are a good fit for applications requiring positive and negative polarity protection. Low leakage allows the diode to conserve power when working below the V_{RWM} . The temperature range of -55°C to $+150^{\circ}\text{C}$ makes this device work at extensive temperatures in most environments. The leaded SOD-323 package is good for applications requiring automatic optical inspection (AOI).

8.3.1 IO Capacitance

The capacitance between the I/O pins is 2.3 pF. The capacitance of this device can support data rates up to 1 Gbps.

8.3.2 IEC 61000-4-5 Surge Protection

The I/O pins of this device have a surge rating of 4.3 A (8/20 μs waveform).

8.4 Device Functional Modes

The ESD1LIN24 is a single channel passive clamp that has low leakage during normal operation when the voltage between I/O and GND is below V_{RWM} , and activate when the voltage between I/O and GND goes above V_{BR} . During ESD events, transient voltages up to ± 30 kV can be clamped on either channel. When the voltages on the protected lines fall below the V_{HOLD} , the device reverts back to the low leakage passive state.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The ESD1LIN24 is a single channel TVS diode which is used to provide a path to ground for dissipating ESD events on USB-PD or industrial I/O lines. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP} , to a safe level for the protected IC.

9.2 Typical Application

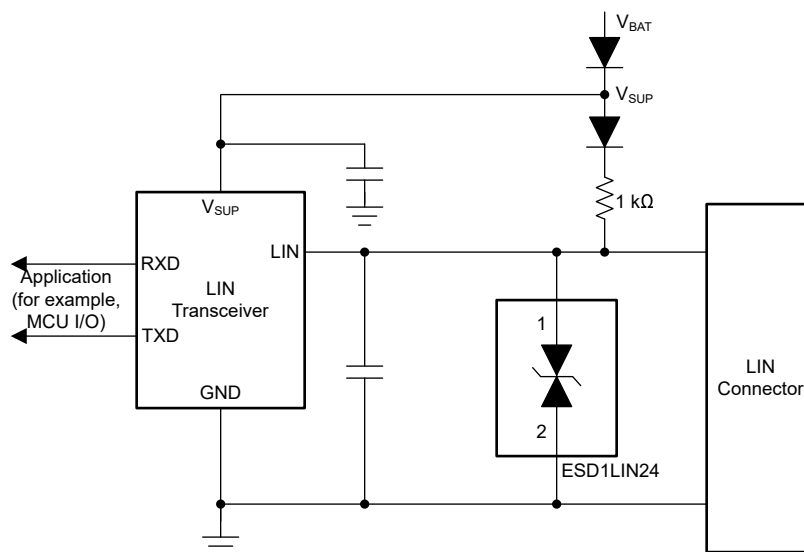


图 9-1. Typical Application

9.2.1 Design Requirements

For this design example, the ESD1LIN24 is used to provide ESD protection to a LIN transceiver. 表 9-1 lists the known design parameters for this application.

表 9-1. Design Parameters for Typical Applications

Design Parameter	Value
Diode configuration	Bidirectional
V_{IO} signal range	Up to 18 V
V_{RWM}	± 24 V
Jumpstart short to battery event on V_{IO}	± 24 V
Data rate	Up to 10 Mbps
Pullup resistor	1 k Ω

9.2.2 Detailed Design Procedure

The ESD1LIN24 has a V_{RWM} of ± 24 V to prevent the diode from being damaged during a short event. The bidirectional characteristic ensures both positive and negative polarity are protected. The low capacitance of 2.3 pF permits data rates up to 1 Gbps, which allows the designer to meet the requirements for LIN. The 1 k Ω and V_{SUP} diode allows the LIN signal to be pulled up to a diode drop below the battery voltage.

9.2.3 Application Curves

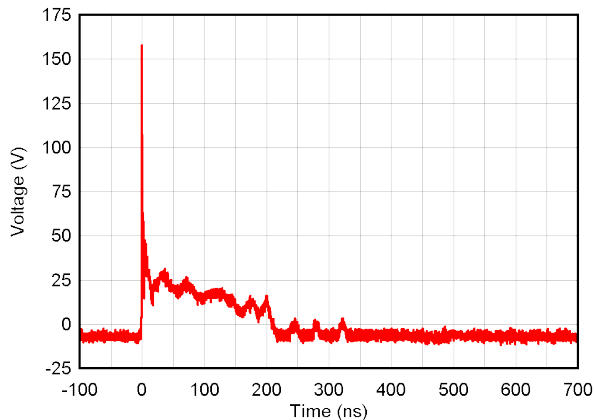


FIG 9-2. +8-kV Clamped IEC Waveform

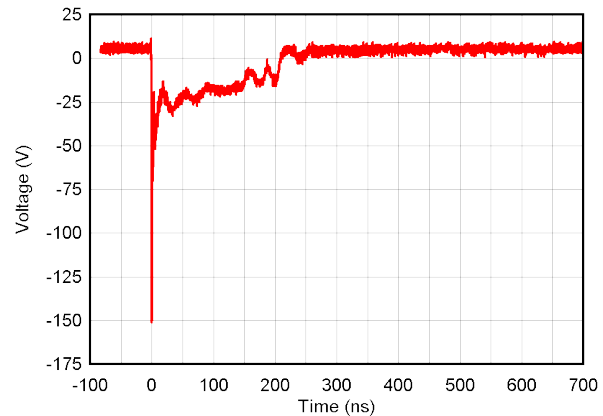


FIG 9-3. -8-kV Clamped IEC Waveform

10 Power Supply Recommendations

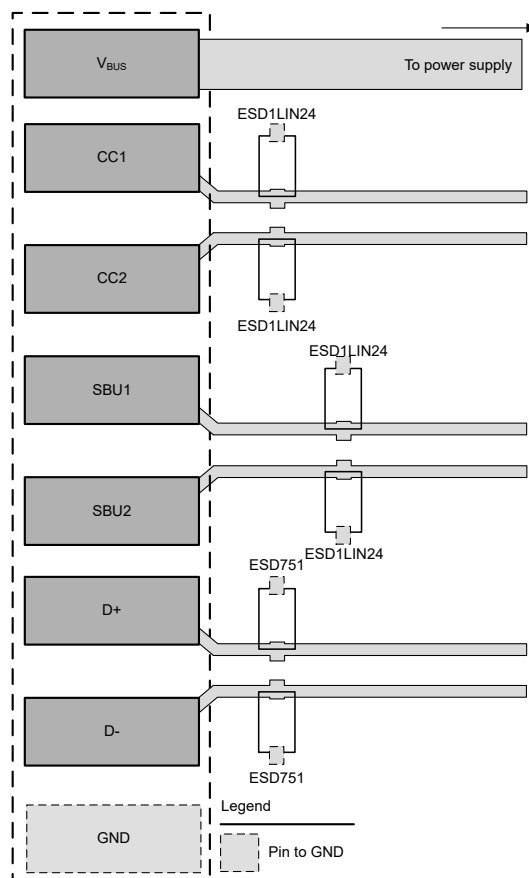
These devices are passive TVS diode-based ESD protection devices, therefore there is no requirement to power them. Ensure that the maximum voltage specifications for each pin is not violated.

11 Layout

11.1 Layout Guidelines

- The optimum placement of the device is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 1 or 2 is connected to ground, use a thick and short trace for this return path.

11.2 Layout Example



11-1. Layout Recommendation

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ESD Layout Guide application reports](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Picking ESD Diodes for Ultra High-Speed Data Lines application reports](#)
- Texas Instruments, [Reading and Understanding an ESD Protection data sheet](#)

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

12.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD1LIN24DYFR	Active	Production	SOT (DYF) 2	3000 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-50 to 150	2QJF
ESD1LIN24DYFR.B	Active	Production	SOT (DYF) 2	3000 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-50 to 150	2QJF

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ESD1LIN24 :

- Automotive : [ESD1LIN24-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated