

**DS92LV0421, DS92LV0422**

JAJSBE6D – MAY 2010 – REVISED DECEMBER 2016

**DS92LV042x 10MHz~75MHz、チャンネル・リンクIIシリアルライザおよび
デシリアルライザ、
LVDSパラレル・インターフェイス搭載**

1 特長

- ・ 5チャンネル(データ4 + クロック1)のチャネル・リンクLVDSパラレル・インターフェイスにより、10~75MHzの24ビット・データの3ビット制御をサポート
- ・ ACカップリングされたSTP相互接続(最大10m)
- ・ シリアライザおよびデシリアライザにターミネーションを内蔵
- ・ At-SpeedリンクBISTモードおよびレポート・ピン(オプション) I²C互換のシリアル制御バス
- ・ パワーダウン・モードにより消費電力を最小化
- ・ 1.8Vまたは3.3V互換のLVCMOS I/Oインターフェイス
- ・ HBM 8kV超
- ・ -40℃~85℃の温度範囲
- ・ シリアライザ(DS92LV0421)
 - － EMIを低減するデータ・スクランブラ
 - － ACカップリング用のDCバランス・エンコーダ
 - － 選択可能な出力VODと調整可能なディエンファシス
- ・ デシリアライザ(DS92LV0422)
 - － 高速なランダムデータ・ロック、リファレンス・クロック不要
 - － 入力レシーバのイコライゼーションを調整可能
 - － 出力パラレル・バスでのEMI最小化(SSCGおよびLVDS VODの選択)

2 アプリケーション

- ・ 組み込みのビデオおよびディスプレイ
- ・ 医療用画像処理および工場自動化
- ・ オフィス自動化(プリンタおよびスキャナ)
- ・ セキュリティおよびビデオ監視
- ・ 汎用データ通信

3 概要

DS92LV042xチップセットは、チャンネル・リンクLVDSビデオ・インターフェイス(LVDSデータ×4 + LVDSクロック)を、単一CMLペア上の高速シリアル化インターフェイスへ変換します。DS92LV042xにより、一般的なチャンネル・リンクまたはOpenLDI LVDS形式のデバイスを現在使用しているアプリケーションを、組み込みクロック・インターフェイスへシームレスにアップグレードできます。このシリアル・バス・スキーマにより、相互接続のコストを低減し、設計の問題を軽減できます。パラレルのOpenLDI LVDSにより、従来のシングルエンドのワイド・バス・インターフェイスと比較して、FPGA I/Oのピン数や基板の配線数が減少し、EMIの問題が軽減されます。

プログラム可能な転送ディエンファシス、受信のイコライゼーション、オンチップでのスクランブル処理、およびDC平衡化により、損失の多いケーブルやバックプレーンでも長距離の転送が可能になります。DS92LV0422は外部のリファレンス・クロックや特別な同期パターンを必要とせず、受信データへ自動的にロックするため、簡単なプラグ・アンド・ゴー操作が可能です。

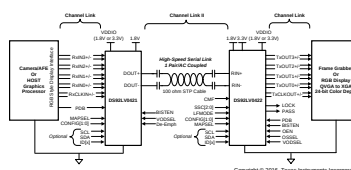
DS92LV042Xチップセットは、I²Cインターフェイスまたはピン経由でプログラム可能です。at-Speed BIST機能が組み込まれており、リンクの整合性を検証し、システム診断に使用できます。DS92LV0421およびDS92LV0422は、DS92LV2421またはDS92LV2422とそれぞれ互換に使用できます。これによって、設計者はホスト・デバイスと受信側のデバイスを、LVDSまたはLVCMOSインターフェイスで柔軟に接続できます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
DS92LV0421	WQFN (36)	6.00mm×6.00mm
DS92LV0422	WQFN (48)	7.00mm×7.00mm

(1) 提供されているすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーションのブロック図



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

English Data Sheet: [SNLS325](#)

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (April 2013) から Revision D に変更

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・ 「製品情報」表、「ピン構成および機能」セクション、「仕様」セクション、「ESD 定格」表、「熱に関する情報」表、「代表的特性」セクション、「詳細説明」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加	1
・ DS92LV024xチップセットに許容されるパラレル・インターフェイスとしてOpenLDI LVDS 追加	1
・ Changed RXIN and RXCLKIN to TXOUT and TXCLKOUT to correct pin name typos	6
・ Changed output state of deserializer when PDB = 1 to be TRI-STATE, not logic high	6
・ Deleted Power dissipation rows from the <i>Absolute Maximum Ratings</i> table	9
・ Changed Junction-to-ambient, $R_{\theta JA}$, values in <i>Thermal Information</i> table From: 27.4°C/W To: 33.8°C/W (NJK) and From: 27.7°C/W to: 28.8°C/W (RHS)	10
・ Changed Junction-to-case, $R_{\theta JC(top)}$, values in <i>Thermal Information</i> table From: 4.5°C/W To: 15.8°C/W (NJK) and From: 3.0°C/W To: 9.3°C/W (RHS)	10
・ Deleted note in <i>Electrical Characteristics: Serializer DC</i> table stating that conditions are verified by characterization or design and not tested in production, as this note only applies to a subset of tested parameters	10
・ Changed minimum and maximum value of serializer I_{IN} for LVDS receiver DC specification	10
・ Changed de-emphasis test condition for serializer I_{DD} supply current	11
・ Changed I_{OL} condition for serial bus V_{OL} parameter from 3 mA to 0.5 mA	13
・ Changed RPU = 10 kΩ condition for the Serial Control Bus Characteristics of t_R and t_F	13
・ Changed t_{PLD} footnote to include t_{DDL} parameter	14
・ Changed notation for serial bit stream UI footnote to clarify 1 UI = 1 / (28 × CLK)	14
・ Changed footnote for deserializer LVDS output units to clarify that parallel interface UI refers to Channel Link format (1 UI = 1 / [7 × CLK]) instead of Channel Link II format (1 UI = 1 / [28 × CLK])	15
・ Changed DS92LV0422 LVDS Transmitter Pulse Positions image to correct diagram labeling	18
・ Changed parallel interface description of deserializer From: wide parallel output bus To: Channel Link LVDS clock and data bus	28

改訂履歴 (continued)

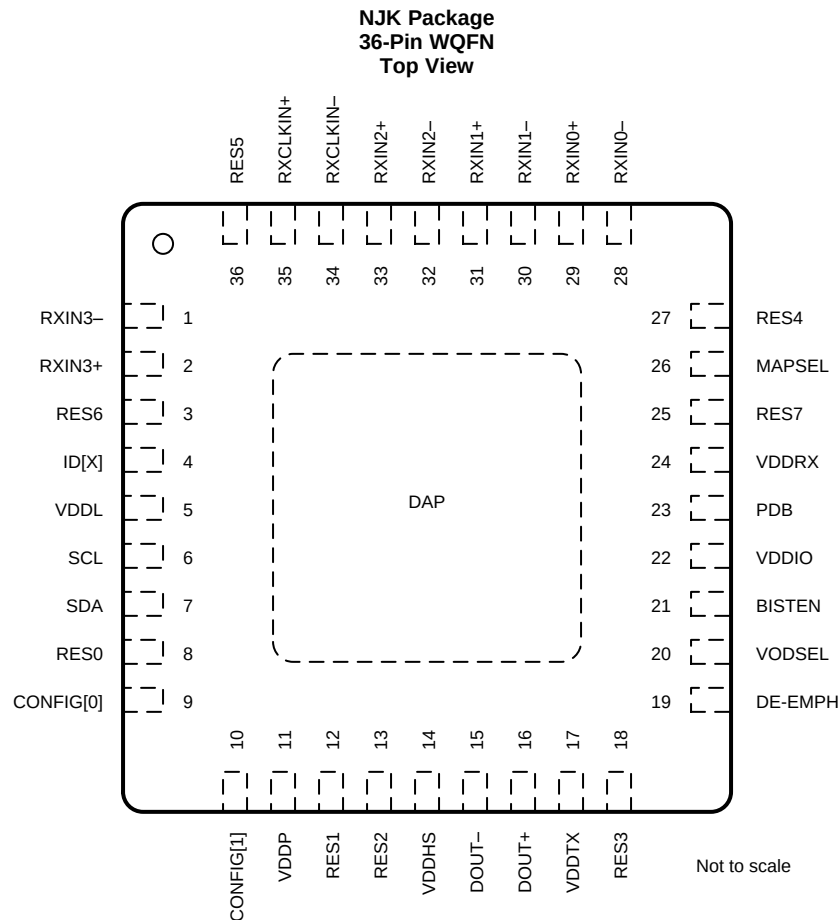
• Deleted support for output data and clock slew rate control	28
• Changed CMF cap recommendation from 0.1 μ F to 4.7 μ F	28
• Changed SSCG Configuration (LFMODE = L) table and SSCG Configuration (LFMODE = H) table to clarify correct SSC[2:0] behavior.....	29
• Changed PDB, OEN, and OSS_SEL Configuration table to clarify correct behavior with PDB, OEN, and OSS_SEL pins	31
• Changed BISTEN detail in BIST Waveforms image so that serializer and deserializer are generic	33
• Changed description of Serializer VODSEL from Reg 0x00[4] to Reg 0x00[5]	37
• Changed Serializer Reg 0x00[3:2] description from Reserved to Reverse-Compatibility Mode bits	37
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Revision B (April 2013) から Revision C に変更

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• ナショナル・セミコンダクターのデータシートのレイアウトをTIフォーマットに 変更	1
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5 Pin Configuration and Functions



Pin Functions: DS92LV0421

PIN		TYPE ⁽¹⁾	DESCRIPTION ⁽²⁾
NAME	NO.		
CHANNEL LINK PARALLEL INPUT INTERFACE			
RXCLKIN+	35	I	True LVDS Clock Input This pair must have a 100-Ω termination for standard LVDS levels.
RXCLKIN–	34	I	Inverting LVDS Clock Input This pair must have a 100-Ω termination for standard LVDS levels.
RXIN[3:0]+	2, 33, 31, 29	I	True LVDS Data Input This pair must have a 100-Ω termination for standard LVDS levels.
RXIN[3:0]–	1, 32, 30, 28	I	Inverting LVDS Data Input This pair must have a 100-Ω termination for standard LVDS levels.
CHANNEL LINK II SERIAL OUTPUT INTERFACE			
DOUT+	16	O	True Output, CML The output must be AC-coupled with a 0.1-μF capacitor.
DOUT–	15	O	Inverting Output, CML The output must be AC-coupled with a 0.1-μF capacitor.

(1) G = Ground, I = Input, O = Output, and P = Power

(2) 1= HIGH, 0 = LOW

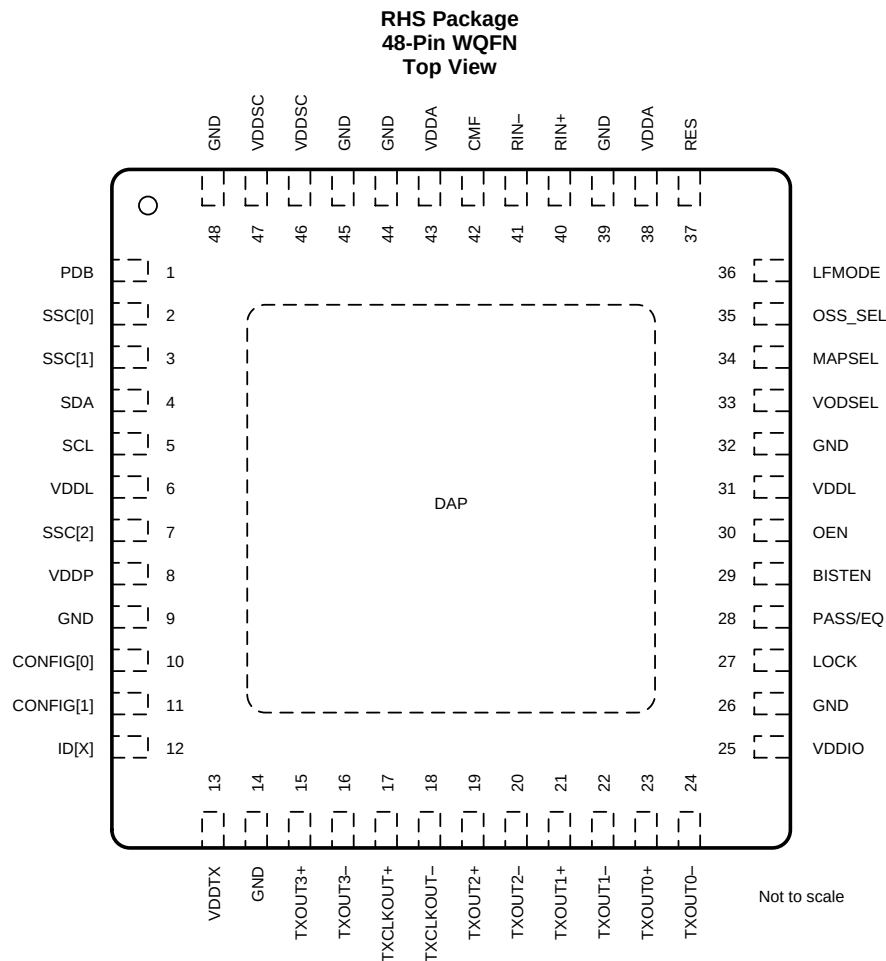
Pin Functions: DS92LV0421 (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION ⁽²⁾
NAME	NO.		
CONTROL AND CONFIGURATION			
CONFIG[1:0]	10, 9	I	Operating Modes: Pin or Register Control, LVCMOS with pulldown. Determines the device operating mode and interfacing device (see Table 10). CONFIG[1:0] = 00: Interfacing to DS92LV2422 or DS92LV0422, Control Signal Filter DISABLED CONFIG[1:0] = 01: Interfacing to DS92LV2422 or DS92LV0422, Control Signal Filter ENABLED CONFIG [1:0] = 10: Interfacing to DS90UR124, DS99R124Q-Q1 CONFIG [1:0] = 11: Interfacing to DS90C124
DE-EMPH	19	I	De-emphasis Control: Pin or Register Control, Analog with pullup. De-emphasis = Open (float) - disabled To enable De-emphasis, tie a resistor from this pin to Ground or control through register (see Table 2).
MAPSEL	26	I	Channel Link Map Select: Pin or Register Control, LVCMOS with pulldown. MAPSEL = 1, MSB on RXIN3± (see Figure 23). MAPSEL = 0, LSB on RXIN3± (see Figure 24).
PDB	23	I	Power-down Mode input, LVCMOS with pulldown. PDB = 1, serializer is enabled (normal operation). See Power Supply Recommendations for more information. PDB = 0, serializer is powered down When the serializer is in the power-down state, the driver outputs (DOUT±) are both logic high, the PLL is shut down, and IDD is minimized. Control Registers are RESET.
RES[7:0]	25, 3, 36, 27, 18, 13, 12, 8	I	<i>Reserved</i> (tie low), LVCMOS with pulldown.
VODSEL	20	I	Differential Driver Output Voltage Select: Pin or Register Control, LVCMOS with pulldown. VODSEL = 1, CML VOD is ±450 mV, 900 mVp-p (typical): long cable or de-emphasis applications VODSEL = 0, CML VOD is ±300 mV, 600 mVp-p (typical): short cable (no de-emphasis), low power mode
OPTIONAL BIST MODE			
BISTEN	21	I	BIST Mode: Optional, LVCMOS with pulldown. BISTEN = 1, BIST is enabled BISTEN = 0, BIST is disabled (normal operation)
OPTIONAL SERIAL BUS CONTROL			
ID[X]	4	I	Serial Control Bus Device ID Address Select: Optional, Analog Resistor to Ground and 10-kΩ pullup to 1.8-V rail (see Table 8).
SCL	6	I	Serial Control Bus Clock Input: Optional, LVCMOS (open-drain) SCL requires an external pullup resistor to V _{DDIO} .
SDA	7	I/O	Serial Control Bus Data Input or Output: Optional, LVCMOS (open-drain) SDA requires an external pullup resistor V _{DDIO} .
POWER AND GROUND ⁽³⁾			
DAP	GND	G	DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connect to the ground plane (GND) with at least 9 vias.
VDDHS	14	P	TX high-speed logic power, 1.8 V ±5%
VDDIO	22	P	LVCMOS I/O power and Channel Link I/O power, 1.8 V ±5% or 3.3 V ±10%
VDDL	5	P	Logic power, 1.8 V ±5%
VDDP	11	P	PLL power, 1.8 V ±5%
VDDR _X	24	P	RX power, 1.8 V ±5%
VDDTX	17	P	Output driver power, 1.8 V ±5%

- (3) The VDD (V_{DDn} and V_{DDIO}) supply ramp must be faster than 1.5 ms with a monotonic rise. If slower than 1.5 ms, a capacitor on the PDB pin is required to ensure PDB arrives after all the VDD supplies have settled to the recommended operating voltage.

DS92LV0421, DS92LV0422

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Pin Functions: DS92LV0422

PIN		TYPE ⁽¹⁾	DESCRIPTION ⁽²⁾
NAME	NO.		
CHANNEL LINK II SERIAL INPUT INTERFACE			
CMF	42	I	Common-mode filter, Analog VCM center-tap is a virtual Ground which may be AC-coupled to Ground to increase receiver common mode noise immunity. Recommended value is 4.7 μF or higher.
RIN+	40	I	True Input, CML The output must be AC-coupled with a 0.1-μF capacitor.
RIN–	41	I	Inverting Input, CML The output must be AC-coupled with a 0.1-μF capacitor.
CHANNEL LINK PARALLEL OUTPUT INTERFACE			
TXCLKOUT+	17	O	True LVDS Clock Output This pair must have a 100-Ω termination for standard LVDS levels.
TXCLKOUT–	18	O	Inverting LVDS Clock Output This pair must have a 100-Ω termination for standard LVDS levels.
TXOUT[3:0]+	15, 19, 21, 23	O	True LVDS Data Output This pair must have a 100-Ω termination for standard LVDS levels.
TXOUT[3:0]–	16, 20, 22, 24	O	Inverting LVDS Data Output This pair must have a 100-Ω termination for standard LVDS levels.

(1) G = Ground, I = Input, O = Output, and P = Power

(2) 1= HIGH, 0 = LOW

Pin Functions: DS92LV0422 (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION ⁽²⁾
NAME	NO.		
LVCMOS OUTPUTS			
LOCK	27	O	LOCK Status Output, LVCMOS LOCK = 1, PLL is locked, output stated determined by OEN. LOCK = 0, PLL is unlocked, output states determined by OSS_SEL and OEN. See Table 7 .
CONTROL AND CONFIGURATION			
CONFIG[1:0]	11, 10	I	Operating Modes: Pin or Limited Register Control, LVCMOS with pulldown. Determine the device operating mode and interfacing device. (see Table 10). CONFIG[1:0] = 00: Interfacing to DS92LV2421 or DS92LV0421, Control Signal Filter DISABLED CONFIG[1:0] = 01: Interfacing to DS92LV2421 or DS92LV0421, Control Signal Filter ENABLED CONFIG [1:0] = 10: Interfacing to DS90UR241, DS99R421 CONFIG [1:0] = 11: Interfacing to DS90C124
LFMODE	36	I	SSCG Low Frequency Mode: Pin or Register Control, LVCMOS with pulldown. LFMODE = 1, low frequency mode (TXCLKOUT = 10–20 MHz) LFMODE = 0, high frequency mode (TXCLKOUT = 20–65 MHz) SSCG not available above 65 MHz.
MAPSEL	34	I	Channel Link Map Select: Pin or Register Control, LVCMOS with pulldown. MAPSEL = 1, MSB on TXOUT3± (see Figure 23). MAPSEL = 0, LSB on TXOUT3± (see Figure 24).
OEN	30	I	Output Enable, LVCMOS with pulldown. See Table 7 for details.
OSS_SEL	35	I	Output Sleep State Select Input, LVCMOS with pulldown. See Table 7 for details.
PDB	1	I	Power-down Mode Input, LVCMOS with pulldown. PDB = 1, deserializer is enabled (normal operation). See Power Supply Recommendations for more information. PDB = 0, deserializer is powered down. When the deserializer is in the power-down state, the driver outputs (TXOUT±) are in TRI-STATE. Control Registers are RESET.
RES	37	I	Reserved (tie low), LVCMOS with pulldown.
SSC[2:0]	7, 3, 2	I	Spread Spectrum Clock Generation (SSCG) Range Select, LVCMOS with pulldown. See Table 5 and Table 6 .
VODSEL	33	I	Parallel LVDS Driver Output Voltage Select: Pin or Register Control, LVCMOS with pulldown. VODSEL = 1, LVDS VOD is ±400 mV, 800 mVp-p (typical) VODSEL = 0, LVDS VOD is ±250 mV, 500 mVp-p (typical)
CONTROL AND CONFIGURATION — STRAP PIN			
EQ	28 [PASS]	I	EQ Gain Control of Channel Link II Serial Input, STRAP, LVCMOS with pulldown EQ = 1, EQ gain is enabled (~13 dB) EQ = 0, EQ gain is disabled (~1.625 dB)
OPTIONAL BIST MODE			
BISTEN	29	I	BIST Mode: Optional, LVCMOS with pulldown. BISTEN = 1, BIST is enabled BISTEN = 0, BIST is disabled
PASS	28	O	PASS Output (BIST Mode): Optional, LVCMOS PASS =1, no errors detected PASS = 0, errors detected Leave open if unused. Route to a test point (pad) recommended.
OPTIONAL SERIAL BUS CONTROL			
ID[X]	12	I	Serial Control Bus Device ID Address Select: Optional, Analog Resistor to Ground and 10-kΩ pullup to 1.8-V rail (see Table 8).
SCL	5	I	Serial Control Bus Clock Input: Optional, LVCMOS (open drain) SCL requires an external pullup resistor to 3.3 V.
SDA	4	I/O	Serial Control Bus Data Input or Output: Optional, LVCMOS (open drain) SDA requires an external pullup resistor 3.3 V.

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Pin Functions: DS92LV0422 (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION ⁽²⁾
NAME	NO.		
POWER AND GROUND ⁽³⁾			
DAP	DAP	G	DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connect to the ground plane (GND) with at least 9 vias.
GND	9, 14, 26, 32, 39, 44, 45, 48	G	Ground
VDDA	38, 43	P	Analog power, 1.8 V ±5%
VDDIO	25	P	LVC MOS I/O power and Channel Link I/O power, 1.8 V ± 5% or 3.3 V ±10%
VDDL	6, 31	P	Logic power, 1.8 V ±5%
VDDP	8	P	PLL power, 1.8 V ±5%
VDDSC	46, 47	P	SSCG power, 1.8 V ±5%
VDDTX	13	P	Channel Link LVDS parallel output power, 3.3 V ±10%

- (3) The VDD (V_{DDn} and V_{DDIO}) supply ramp must be faster than 1.5 ms with a monotonic rise. If slower than 1.5 ms, a capacitor on the PDB pin is required to ensure PDB arrives after all the VDD supplies have settled to the recommended operating voltage.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

		MIN	MAX	UNIT
Supply voltage	V _{DDn} (1.8 V)	–0.3	2.5	V
	V _{DDIO}	–0.3	4	
	Serializer, V _{DDTX}	–0.3	2.5	
	Deserializer, V _{DDTX}	–0.3	4	
LVCMOS I/O voltage		–0.3	V _{DDIO} + 0.3	V
Serializer LVDS input voltage		–0.3	V _{DDIO} + 0.3	V
Deserializer LVDS output voltage		–0.3	V _{DDTX} + 0.3	V
Serializer CML driver output voltage		–0.3	V _{DDn} + 0.3	V
Deserializer CML receiver input voltage		–0.3	V _{DD} + 0.3	V
Junction temperature, T _J			150	°C
Storage temperature, T _{stg}		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) For soldering specifications, see *Absolute Maximum Ratings for Soldering* (SNOA549).

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±8000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1250	
	Machine Model	±250	
	IEC 61000-4-2, powered-up only contact discharge R _D = 330 Ω, C _S = 150 pF (R _{IN+} , R _{IN-})	>±8000	
	IEC 61000-4-2, powered-up only air-gap discharge R _D = 330 Ω, C _S = 150 pF (R _{IN+} , R _{IN-})	>±30000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DDn}	Supply voltage	1.71	1.8	1.89	V
V _{DDTX}	Supply voltage (serializer)	1.71	1.8	1.89	V
V _{DDTX}	Supply voltage (deserializer)	3	3.3	3.6	V
V _{DDIO}	LVCMOS supply voltage (1.8-V nominal)	1.71	1.8	1.89	V
V _{DDIO}	LVCMOS supply voltage (3.3-V nominal)	3	3.3	3.6	V
	Clock frequency	10		75	MHz
	Supply noise ⁽¹⁾			100	mV _{p-p}
T _A	Operating free-air temperature	–40	25	85	°C

- (1) Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC-coupled to the V_{DDn} (1.8 V) supply with amplitude = 100 mVp-p measured at the device V_{DDn} pins. Bit error rate testing of input to the serializer and output of the deserializer with 10 meter cable shows no error when the noise frequency on the serializer is less than 750 kHz. The deserializer, on the other hand, shows no error when the noise frequency is less than 400 kHz.

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC ⁽¹⁾		DS92LV0421	DS92LV0422	UNIT
		NJK (WQFN)	RHS (WQFN)	
		36 PINS	48 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽²⁾	33.8	28.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance ⁽²⁾	15.8	9.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	7.2	5.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.2	0.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	7.1	5.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	2.6	1.6	°C/W

 (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) Based on nine thermal vias.

6.5 Electrical Characteristics: Serializer DC

 over recommended operating supply and temperature ranges (unless otherwise noted)⁽¹⁾⁽²⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
LVCMOS INPUT DC SPECIFICATIONS								
V _{IH}	High-level input voltage	V _{DDIO} = 3 V to 3.6 V (PDB, VODSEL, MAPSEL, CONFIG[1:0], BISTEN pins)		2		V _{DDIO}	V	
		V _{DDIO} = 1.71 V to 1.89 V (PDB, VODSEL, MAPSEL, CONFIG[1:0], BISTEN pins)		0.65 × V _{DDIO}		V _{DDIO}		
V _{IL}	Low-level input voltage	V _{DDIO} = 3 V to 3.6 V (PDB, VODSEL, MAPSEL, CONFIG[1:0], BISTEN pins)		GND		0.8	V	
		V _{DDIO} = 1.71 V to 1.89 V (PDB, VODSEL, MAPSEL, CONFIG[1:0], BISTEN pins)		GND		0.35 × V _{DDIO}		
I _{IN}	Input current	V _{IN} = 0 V or V _{DDIO} (PDB, VODSEL, MAPSEL, CONFIG[1:0], BISTEN pins)	V _{DDIO} = 3 V to 3.6 V	–15	±1	15	μA	
			V _{DDIO} = 1.7 V to 1.89 V	–15	±1	15		
CHANNEL LINK PARALLEL LVDS RECEIVER DC SPECIFICATIONS								
V _{TH}	Differential threshold, high voltage	V _{CM} = 1.2 V (see Figure 1), RXIN[3:0]± and RXCLKIN± pins				100	mV	
V _{TL}	Differential threshold, low voltage	V _{CM} = 1.2 V (see Figure 1), RXIN[3:0]± and RXCLKIN± pins			–100		mV	
V _{ID}	Differential input voltage swing	V _{CM} = 1.2 V (see Figure 1), RXIN[3:0]± and RXCLKIN± pins			200		600	mV
V _{CM}	Common-mode voltage	V _{DDIO} = 3.3 V (RXIN[3:0]± and RXCLKIN± pins)			0	1.2	2.4	V
		V _{DDIO} = 1.8 V (RXIN[3:0]± and RXCLKIN± pins)			0	1.2	1.7	
I _{IN}	Input current	RXIN[3:0]± and RXCLKIN± pins			–15	±1	15	μA
CHANNEL LINK II SERIAL CML DRIVER DC SPECIFICATIONS								
V _{OD}	Differential output voltage	R _L = 100 Ω, de-emphasis = disabled (see Figure 3), DOUT+ and DOUT– pins	VODSEL = L	±225	±300	±375	mV	
			VODSEL = H	±350	±450	±550		
V _{ODp-p}	Differential output voltage (DOUT+) – (DOUT–)	R _L = 100 Ω, de-emphasis = disabled (see Figure 3), DOUT+ and DOUT– pins	VODSEL = L		600		mVp-p	
			VODSEL = H		900			
ΔV _{OD}	Output voltage unbalance	R _L = 100 Ω, de-emphasis = disabled, VODSEL = L (DOUT+ and DOUT– pins)				1	50	mV

 (1) Typical values represent most likely parametric norms at V_{DD} = 3.3 V, T_A = +25°C, and at the *Recommended Operation Conditions* at the time of product characterization and are not verified.

 (2) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD}, ΔV_{OD}, V_{TH}, and V_{TL}, which are differential voltages.

Electrical Characteristics: Serializer DC (continued)

over recommended operating supply and temperature ranges (unless otherwise noted)⁽¹⁾⁽²⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OS} Offset voltage (single-ended)	At TP A and B (see Figure 2), R _L = 100 Ω, de-emphasis = disabled (DOUT+ and DOUT– pins)	VODSEL = L	1.65		V
		VODSEL = H	1.575		
ΔV _{OS} Offset voltage unbalance (single-ended)	At TP A and B (see Figure 2), R _L = 100 Ω, de-emphasis = disabled (DOUT+ and DOUT– pins)		1		mV
I _{OS} Output short-circuit current	DOUT± = 0 V, de-emphasis = disabled, VODSEL = 0 (DOUT+ and DOUT– pins)		–36		mA
R _{TO} Internal output termination resistor	DOUT+ and DOUT– pins	80		120	Ω
SERIALIZER SUPPLY CURRENT					
I _{DDT1} Serializer supply current (includes load current)	R _L = 100 Ω, f = 75 MHz, checker board pattern (see Figure 15), de-emphasis = 3 kΩ, VODSEL = H, V _{DD} = 1.89 V (All V _{DD} pins)		84	100	mA
I _{DDIOT1} Serializer supply current (includes load current)	R _L = 100 Ω, f = 75 MHz de-emphasis = 3 kΩ, VODSEL = H, checker board pattern (see Figure 15)	V _{DDIO} = 1.89 V (V _{DDIO} pin)	3	5	mA
		V _{DDIO} = 3.6 V (V _{DDIO} pin)	10	13	
I _{DDT2} Serializer supply current (includes load current)	R _L = 100 Ω, f = 75 MHz, checker board pattern (see Figure 15), de-emphasis = 6 kΩ, VODSEL = L, V _{DD} = 1.89 V (All V _{DD} pins)		77	90	mA
I _{DDIOT2} Serializer supply current (includes load current)	R _L = 100 Ω, f = 75 MHz de-emphasis = 6 kΩ, VODSEL = L, checker board pattern (see Figure 15)	V _{DDIO} = 1.89 V (V _{DDIO} pin)	3	5	mA
		V _{DDIO} = 3.6 V (V _{DDIO} pin)	10	13	
I _{DDZ} Serializer supply current power-down	PDB = 0 V, all other LVCMOS inputs = 0 V, V _{DD} = 1.89 V (All V _{DD} pins)		100	1000	μA
I _{DDIOZ} Serializer supply current power-down	PDB = 0 V, all other LVCMOS inputs = 0 V	V _{DDIO} = 1.89 V (V _{DDIO} pin)	0.5	10	μA
		V _{DDIO} = 3.6 V (V _{DDIO} pin)	1	30	

6.6 Electrical Characteristics: Deserializer DC

over recommended operating supply and temperature ranges (unless otherwise noted)⁽¹⁾⁽²⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
3.3-V LVCMOS I/O DC SPECIFICATIONS (V_{DDIO} = 3 V to 3.6 V)					
V _{IH} High level input voltage	PDB, VODSEL, OEN, MAPSEL, LFMODE, SSC[2:0], and BISTEN pins	2		V _{DDIO}	V
V _{IL} Low level input voltage	PDB, VODSEL, OEN, MAPSEL, LFMODE, SSC[2:0], and BISTEN pins	GND		0.8	V
I _{IN} Input current	V _{IN} = 0 V or V _{DDIO} (PDB, VODSEL, OEN, MAPSEL, LFMODE, SSC[2:0], and BISTEN pins)	–15	±1	15	μA
V _{OH} High level output voltage	I _{OH} = –0.5 mA (LOCK and PASS pins)	V _{DDIO} – 0.2	V _{DDIO}		V
V _{OL} Low level output voltage	I _{OL} = 0.5 mA (LOCK and PASS pins)		GND	0.2	V
I _{OS} Output short-circuit current	V _{OUT} = 0 V (LOCK and PASS pins)		–10		mA
I _{OZ} TRI-STATE output current	PDB = 0 V, OSS_SEL = 0 V, V _{OUT} = 0 V or V _{DDIO} (LOCK and PASS pins)	–10		10	μA

(1) Typical values represent most likely parametric norms at V_{DD} = 3.3 V, T_A = +25°C, and at the *Recommended Operation Conditions* at the time of product characterization and are not verified.

(2) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD}, ΔV_{OD}, V_{TH}, and V_{TL}, which are differential voltages.

Electrical Characteristics: Deserializer DC (continued)

 over recommended operating supply and temperature ranges (unless otherwise noted)⁽¹⁾⁽²⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
1.8-V LVCMOS I/O DC SPECIFICATIONS (V _{DDIO} = 1.71 V to 1.89 V)							
V _{IH}	High level input voltage	PDB, VODSEL, OEN, MAPSEL, LFMODE, SSC[2:0], and BISTEN pins		0.65 × V _{DDIO}		V _{DDIO}	V
V _{IL}	Low level input voltage	PDB, VODSEL, OEN, MAPSEL, LFMODE, SSC[2:0], and BISTEN pins		GND		0.35 × V _{DDIO}	V
I _{IN}	Input current	V _{IN} = 0 V or V _{DDIO} (PDB, VODSEL, OEN, MAPSEL, LFMODE, SSC[2:0], and BISTEN pins)		−15	±1	15	μA
V _{OH}	High level output voltage	I _{OH} = −0.5 mA (LOCK and PASS pins)		V _{DDIO} − 0.2	V _{DDIO}		V
V _{OL}	Low level output voltage	I _{OL} = 0.5 mA (LOCK and PASS pins)		GND		0.2	V
I _{OS}	Output short-circuit current	V _{OUT} = 0 V (LOCK and PASS pins)		−3			mA
I _{OZ}	TRI-STATE output current	PDB = 0 V, OSS_SEL = 0 V, V _{OUT} = 0 V or V _{DDIO} (LOCK and PASS pins)		−15		15	μA
CHANNEL LINK PARALLEL LVDS DRIVER DC SPECIFICATIONS							
V _{OD}	Differential output voltage	R _L = 100 Ω (see Figure 3; TXOUT[3:0]± and TXCLKOUT± pins)	VODSEL = L	100	250	400	mV
			VODSEL = H	200	400	600	
V _{ODp-p}	Differential output voltage A to B	R _L = 100 Ω (see Figure 3; TXOUT[3:0]± and TXCLKOUT± pins)	VODSEL = L	500			mVp-p
			VODSEL = H	800			
ΔV _{OD}	Output voltage unbalance	R _L = 100 Ω (see Figure 3; TXOUT[3:0]± and TXCLKOUT± pins)		1		50	mV
V _{OS}	Offset voltage (single-ended)	R _L = 100 Ω (see Figure 3; TXOUT[3:0]± and TXCLKOUT± pins)	VODSEL = L	1	1.2	1.5	V
			VODSEL = H	1.2			
ΔV _{OS}	Offset voltage unbalance (single-ended)	R _L = 100 Ω (see Figure 3; TXOUT[3:0]± and TXCLKOUT± pins)		1		50	mV
I _{OS}	Output short-circuit current	R _L = 100 Ω, V _{OUT} = GND (TXOUT[3:0]± and TXCLKOUT± pins)		−5			mA
I _{OZ}	Output TRI-STATE current	R _L = 100 Ω, V _{OUT} = V _{DDTX} or GND (TXOUT[3:0]± and TXCLKOUT± pins)		−10		10	μA
CHANNEL LINK II SERIAL CML RECEIVER DC SPECIFICATIONS							
V _{TH}	Differential input threshold high voltage	V _{CM} = 1.2 V (Internal V _{BIAS}) (RIN+ and RIN- pins)				50	mV
V _{TL}	Differential input threshold low voltage	V _{CM} = 1.2 V (Internal V _{BIAS}) (RIN+ and RIN- pins)		−50			mV
V _{CM}	Common mode voltage, internal V _{BIAS}	RIN+ and RIN- pins		1.2			V
R _T	Input termination	RIN+ and RIN- pins		85	100	115	Ω
DESERIALIZER SUPPLY CURRENT							
I _{DD1}	Deserializer supply current (Includes load current)	75 MHz clock, checker board pattern (see Figure 15), VODSEL = H, SSCG[2:0] = 000'b, V _{DDn} = 1.89 V (All V _{DD(1.8)} pins)		88		100	mA
I _{DDTX1}	Deserializer supply current (Includes load current)	75 MHz clock, checker board pattern (see Figure 15), VODSEL = H, SSCG[2:0] = 000'b, V _{DDTX} = 3.6 V (V _{DDTX} pin)		40		50	mA
I _{DDIO1}	Deserializer supply current (Includes load current)	75 MHz clock, checker board pattern (see Figure 15), VODSEL = H, SSCG[2:0] = 000'b	V _{DDIO} = 1.89 V (V _{DDIO} pin)	0.3		0.8	mA
			V _{DDIO} = 3.6 V (V _{DDIO} pin)	0.8		1.5	
I _{DDZ}	Deserializer supply current power-down	PDB = 0 V, All other LVCMOS inputs = 0 V, V _{DDn} = 1.89 V (All V _{DD(1.8)} pins)		0.15		2	mA
I _{DDTXZ}	Deserializer supply current power-down	PDB = 0 V, All other LVCMOS inputs = 0 V, V _{DDTX} = 3.6 V (V _{DDTX} pin)		0.01		0.1	mA

Electrical Characteristics: Deserializer DC (continued)

over recommended operating supply and temperature ranges (unless otherwise noted)⁽¹⁾⁽²⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DDIOZ} Deserializer supply current power-down	PDB = 0 V, all other LVCMOS inputs = 0 V	$V_{DDIO} = 1.89\text{ V}$ (V_{DDIO} pin)	0.01	0.08	mA
		$V_{DDIO} = 3.6\text{ V}$ (V_{DDIO} pin)	0.01	0.08	

6.7 Electrical Characteristics: DC and AC Serial Control Bus

over 3.3-V supply and temperature ranges (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH} Input high-level voltage	SDA and SCL	$0.7 \times V_{DDIO}$		V_{DDIO}	V
V_{IL} Input low-level voltage	SDA and SCL	GND		$0.3 \times V_{DDIO}$	V
V_{HY} Input hysteresis			>50		mV
V_{OL} Output low-level voltage	SDA, $I_{OL} = 0.5\text{ mA}$	0		0.36	V
I_{IN} Input current	SDA or SCL, $V_{in} = V_{DDIO}$ or GND	-10		10	μA
t_R SDA rise time, READ	SDA, RPU = 10 k Ω , $C_b \leq 400\text{ pF}$ (see Figure 18)		800		ns
t_F SDA fall time, READ	SDA, RPU = 10 k Ω , $C_b \leq 400\text{ pF}$ (see Figure 18)		50		ns
$t_{SU,DAT}$ Set-up time, READ	See Figure 18		540		ns
$t_{HD,DAT}$ Hold time, READ	See Figure 18		600		ns
t_{SP} Input filter			50		ns
C_{IN} Input capacitance	SDA or SCL		<5		pF

6.8 Timing Requirements: Serial Control Bus

over 3.3-V supply and temperature ranges (unless otherwise noted)

		MIN	TYP	MAX	UNIT
f_{SCL} SCL clock frequency	Standard mode			100	kHz
	Fast mode			400	
t_{LOW} SCL low period	Standard mode	4.7			μs
	Fast mode	1.3			
t_{HIGH} SCL high period	Standard mode	4			μs
	Fast mode	0.6			
$t_{HD:STA}$ Hold time for a START or a repeated START condition (see Figure 18)	Standard mode	4			μs
	Fast mode	0.6			
$t_{SU:STA}$ Set-up time for a START or a repeated START condition (see Figure 18)	Standard mode	4.7			μs
	Fast mode	0.6			
$t_{HD,DAT}$ Data hold time (see Figure 18)	Standard mode	0		3.45	μs
	Fast mode	0		0.9	
$t_{SU,DAT}$ Data set-up time (see Figure 18)	Standard mode	250			μs
	Fast mode	100			
$t_{SU:STO}$ Set-up time for STOP (see Figure 18)	Standard mode	4			μs
	Fast mode	0.6			
t_{BUF} Bus free time between STOP and START (see Figure 18)	Standard mode	4.7			μs
	Fast mode	1.3			
t_r SCL and SDA rise time (see Figure 18)	Standard mode			1000	ns
	Fast mode			300	

Timing Requirements: Serial Control Bus (continued)

over 3.3-V supply and temperature ranges (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_f	SCL and SDA fall time (see Figure 18)	Standard mode		300	ns
		Fast mode		300	

6.9 Switching Characteristics: Serializer

over recommended operating supply and temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHANNEL LINK PARALLEL LVDS INPUT						
t_{RSP0}	LVDS Receiver Strobe Position (bit 0)	RXCLKIN = 75 MHz, RXIN[3:0] pins (see Figure 5)	0.57	0.95	1.33	ns
t_{RSP1}	LVDS Receiver Strobe Position (bit 1)	RXCLKIN = 75 MHz, RXIN[3:0] pins (see Figure 5)	2.47	2.85	3.23	ns
t_{RSP2}	LVDS Receiver Strobe Position (bit 2)	RXCLKIN = 75 MHz, RXIN[3:0] pins (see Figure 5)	4.37	4.75	5.13	ns
t_{RSP3}	LVDS Receiver Strobe Position (bit 3)	RXCLKIN = 75 MHz, RXIN[3:0] pins (see Figure 5)	6.27	6.65	7.03	ns
t_{RSP4}	LVDS Receiver Strobe Position (bit 4)	RXCLKIN = 75 MHz, RXIN[3:0] pins (see Figure 5)	8.17	8.55	8.93	ns
t_{RSP5}	LVDS Receiver Strobe Position (bit 5)	RXCLKIN = 75 MHz, RXIN[3:0] pins (see Figure 5)	10.07	10.45	10.83	ns
t_{RSP6}	LVDS Receiver Strobe Position (bit 6)	RXCLKIN = 75 MHz, RXIN[3:0] pins (see Figure 5)	11.97	12.35	12.73	ns
CHANNEL LINK II CML OUTPUT						
t_{LLHT}	Serializer output low-to-high transition time (see Figure 4)	$R_L = 100\ \Omega$, De-emphasis = disabled, VODSEL = 0	100	200	300	ps
		$R_L = 100\ \Omega$, De-emphasis = disabled, VODSEL = 1	100	200	300	
t_{LHLT}	Serializer output high-to-low transition time (see Figure 4)	$R_L = 100\ \Omega$, De-emphasis = disabled, VODSEL = 0	130	260	390	ps
		$R_L = 100\ \Omega$, De-emphasis = disabled, VODSEL = 1	100	200	300	
t_{XZD}	Serializer output active to OFF delay (see Figure 9) ⁽¹⁾			5	15	ns
t_{PLD}	Serializer PLL lock time (see Figure 7) ⁽¹⁾⁽²⁾⁽³⁾	$R_L = 100\ \Omega$		1.5	10	ms
t_{SD}	Serializer delay, latency (see Figure 10) ⁽¹⁾	$R_L = 100\ \Omega$		$147 \times T$	$148 \times T$	ns
t_{DJIT}	Serializer output total jitter (see Figure 12)	$R_L = 100\ \Omega$, De-emphasis = disabled, RANDOM pattern		0.3		UI ⁽⁴⁾
λ_{STXBW}	Serializer jitter transfer (function –3-dB bandwidth) ⁽¹⁾⁽⁵⁾	RXCLKIN = 43 MHz		2.2		MHz
		RXCLKIN = 75 MHz		3		
δ_{STX}	Serializer jitter transfer (function peaking) ⁽¹⁾⁽⁵⁾	RXCLKIN = 43 MHz		1		dB
		RXCLKIN = 75 MHz		1		

(1) Specification is verified by characterization and is not tested in production.

 (2) t_{PLD} and t_{DDL_T} is the time required by the serializer and deserializer to obtain lock when exiting power-down state with an active RXCLKIN.

 (3) When the serializer output is at TRI-STATE, the deserializer loses PLL lock. Resynchronization and Re-lock must occur before data transfer require t_{PLD} .

(4) UI: Unit Interval is equivalent to one serialized data bit width (1 UI = 1 / [28 × CLK]). The UI scales with clock frequency.

(5) Specification is verified by design and is not tested in production.

6.10 Switching Characteristics: Deserializer

over recommended operating supply and temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHANNEL LINK PARALLEL LVDS OUTPUT						
t_{DLHT}	Deserializer low-to-high transition time	$R_L = 100\ \Omega$ TXCLKOUT $\pm$, TXOUT[3:0] $\pm$ pins		0.3	0.6	ns
t_{DHLT}	Deserializer high-to-low transition time	$R_L = 100\ \Omega$ TXCLKOUT $\pm$, TXOUT[3:0] $\pm$ pins		0.3	0.6	ns
t_{DCCJ}	Cycle-to-cycle output jitter ⁽¹⁾⁽²⁾⁽³⁾	TXCLKOUT $\pm$ = 10 MHz		900	2100	ps
		TXCLKOUT $\pm$ = 75 MHz		75	125	
t_{TTP1}	LVDS Transmitter Pulse Position for bit 1	TXCLKOUT $\pm$ = 10 to 75 MHz (see Figure 6)		0		UI ⁽⁴⁾
t_{TTP0}	LVDS Transmitter Pulse Position for bit 0	TXCLKOUT $\pm$ = 10 to 75 MHz (see Figure 6)		1		UI ⁽⁴⁾
t_{TTP6}	LVDS Transmitter Pulse Position for bit 6	TXCLKOUT $\pm$ = 10 to 75 MHz (see Figure 6)		2		UI ⁽⁴⁾
t_{TTP5}	LVDS Transmitter Pulse Position for bit 5	TXCLKOUT $\pm$ = 10 to 75 MHz (see Figure 6)		3		UI ⁽⁴⁾
t_{TTP4}	LVDS Transmitter Pulse Position for bit 4	TXCLKOUT $\pm$ = 10 to 75 MHz (see Figure 6)		4		UI ⁽⁴⁾
t_{TTP3}	LVDS Transmitter Pulse Position for bit 3	TXCLKOUT $\pm$ = 10 to 75 MHz (see Figure 6)		5		UI ⁽⁴⁾
t_{TTP2}	LVDS Transmitter Pulse Position for bit 2	TXCLKOUT $\pm$ = 10 to 75 MHz (see Figure 6)		6		UI ⁽⁴⁾
t_{DD}	Deserializer delay, latency ⁽³⁾ (see Figure 11)	TXCLKOUT $\pm$ = 10 to 75 MHz (see Figure 6)		142 $\times$ T	143 $\times$ T	ns
t_{TPDD}	Deserializer power-down delay, active to OFF (see Figure 13)	TXCLKOUT $\pm$ = 75 MHz		6	10	ns
t_{TXZR}	Deserializer enable delay, OFF to active (see Figure 14)	TXCLKOUT $\pm$ = 75 MHz		40	55	ns
CHANNEL LINK II CML INPUT						
$t_{DDL T}$	Deserializer lock time ⁽⁵⁾ (see Figure 8)	TXCLKOUT $\pm$ = 10 MHz, SSCG = OFF		7		ms
		TXCLKOUT $\pm$ = 10 MHz, SSCG = ON		14		
		TXCLKOUT $\pm$ = 75 MHz, SSCG = OFF		6		
		TXCLKOUT $\pm$ = 65 MHz, SSCG = ON		8		
t_{DJIT}	Deserializer input jitter tolerance (see Figure 16)	EQ = OFF SSCG = OFF Jitter frequency > 10 MHz		>0.45		UI ⁽⁶⁾
LVCMOS OUTPUTS						
t_{CLH}	Deserializer low-to-high transition time (see Figure 4)	$C_L = 8\text{ pF}$ (LOCK and PASS pins)		10	15	ns
t_{CHL}	Deserializer high-to-low transition time (see Figure 4)	$C_L = 8\text{ pF}$ (LOCK and PASS pins)		10	15	ns
t_{PASS}	BIST PASS valid time, BISTEN = 1 (see Figure 17)	10 MHz (PASS pin)		220	230	ns
		75 MHz (PASS pin)		40	65	

(1) t_{DCCJ} is the maximum amount of jitter between adjacent clock cycles.

(2) Specification is verified by characterization and is not tested in production.

(3) Specification is verified by design and is not tested in production.

(4) UI: Unit Interval is equivalent to one serialized data bit width in the OpenLDI parallel interface format (1 UI = 1 / [7 $\times$ CLK]). The UI scales with clock frequency.

(5) t_{PLD} and $t_{DDL T}$ is the time required by the serializer and deserializer to obtain lock when exiting power-down state with an active RXCLKIN.

(6) UI – Unit Interval is equivalent to one serialized data bit width (1 UI = 1 / [28 $\times$ CLK]). The UI scales with clock frequency.

Switching Characteristics: Deserializer (continued)

over recommended operating supply and temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SSCG MODE					
f_{DEV}	Spread spectrum clocking deviation frequency ⁽³⁾	TXCLKOUT $\pm$ = 10 to 65 MHz, SSCG = ON		$\pm 0.5\%$	$\pm 2\%$
f_{MOD}	Spread spectrum clocking modulation frequency ⁽³⁾	TXCLKOUT $\pm$ = 10 to 65 MHz, SSCG = ON		8	100 kHz

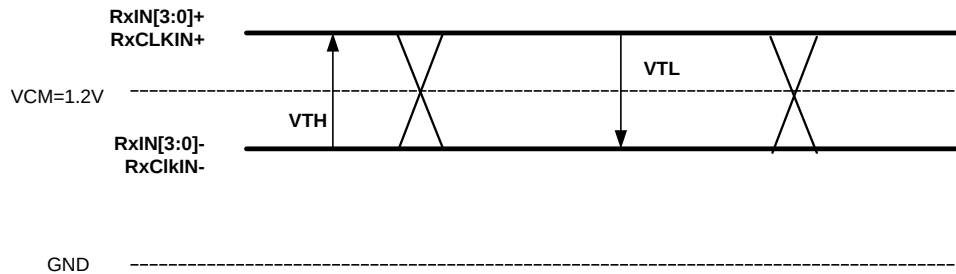


Figure 1. Channel Link DC VTH/VTL Definition

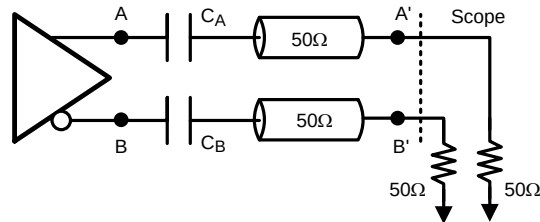


Figure 2. Output Test Circuit

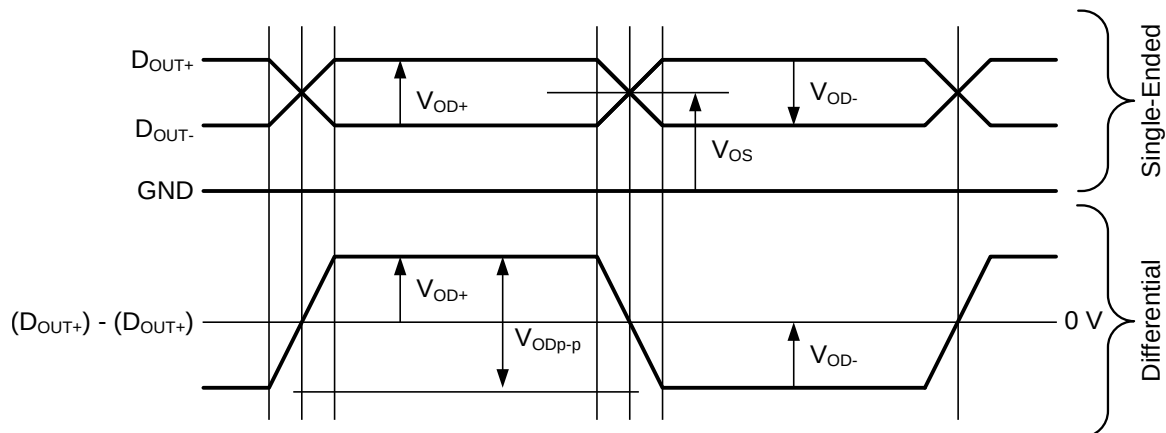


Figure 3. CML Output Waveforms

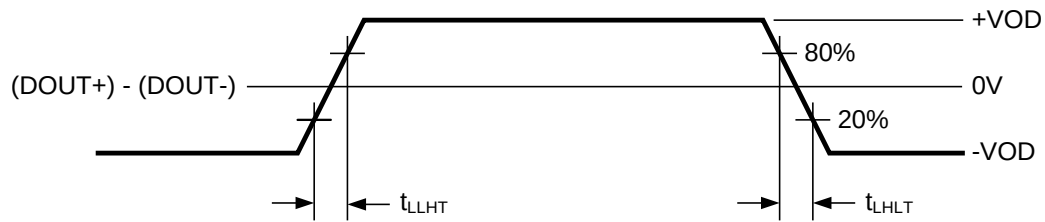


Figure 4. CML Output Transition Times

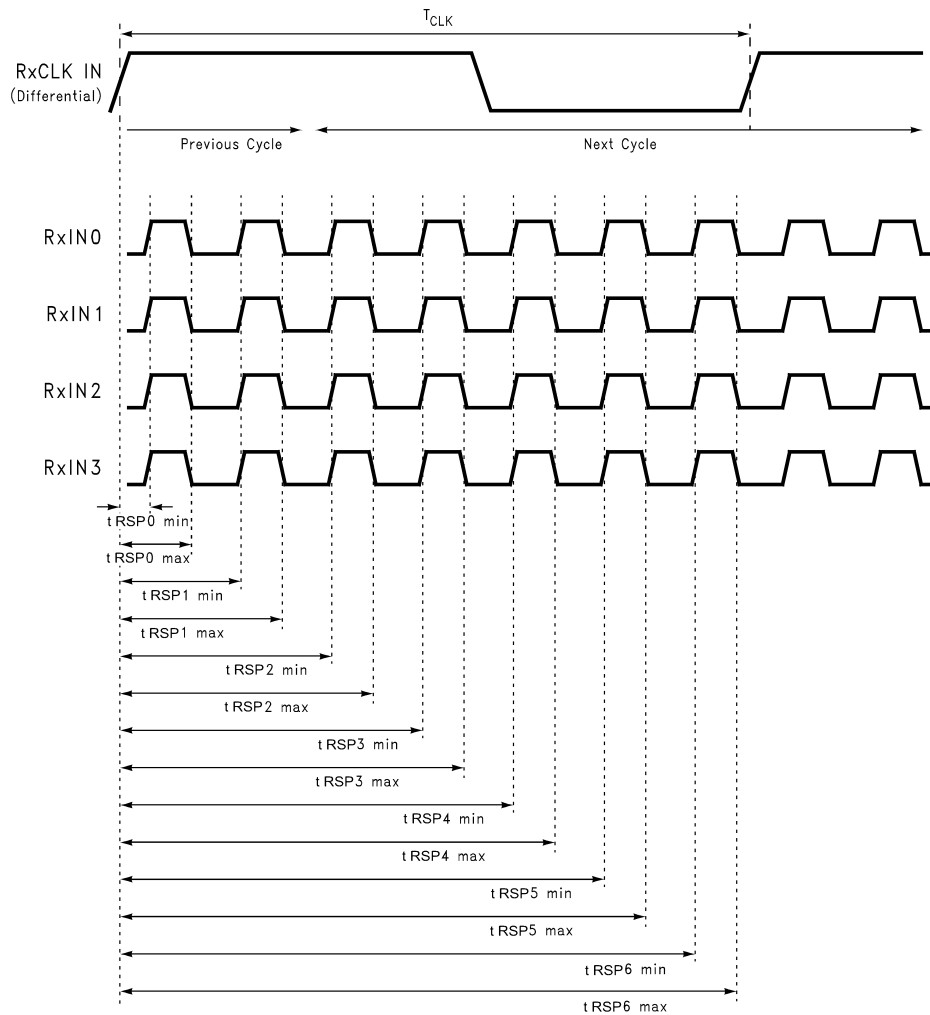
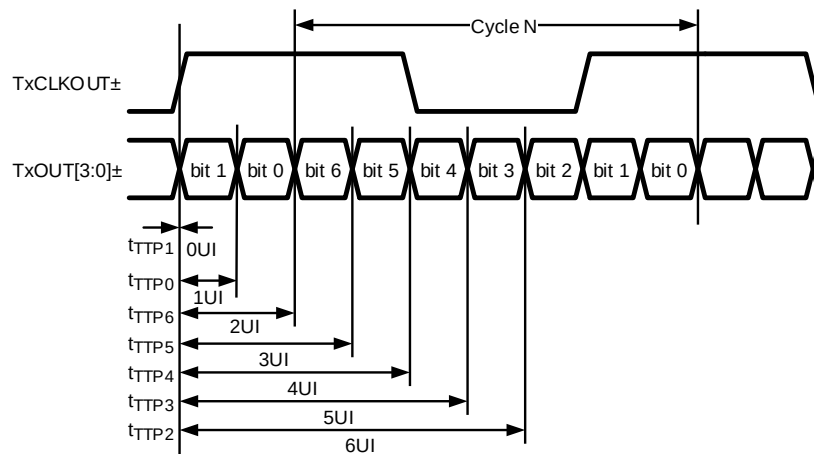
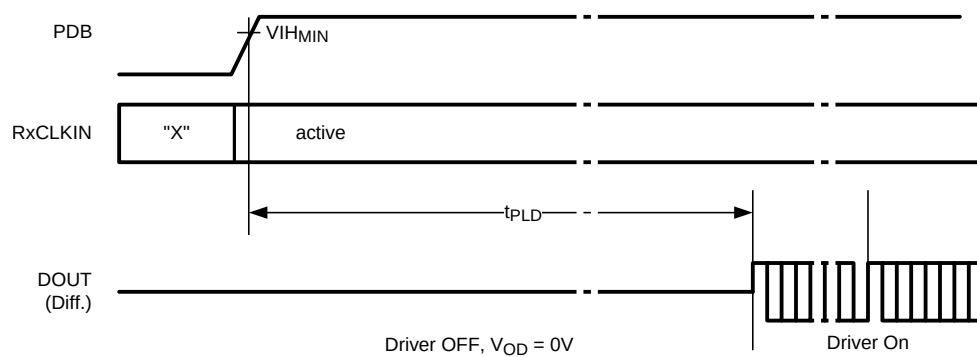
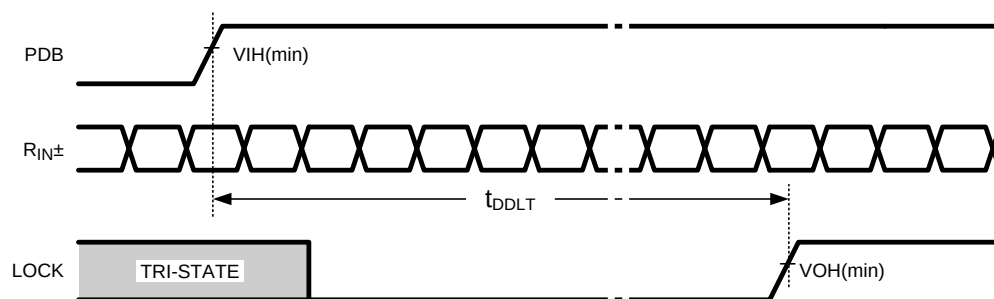


Figure 5. DS92LV0421 Channel Link Receiver Strobe Positions


Figure 6. DS92LV0422 LVDS Transmitter Pulse Positions

Figure 7. DS92LV0421 Lock Time

Figure 8. DS92LV0422 Lock Time

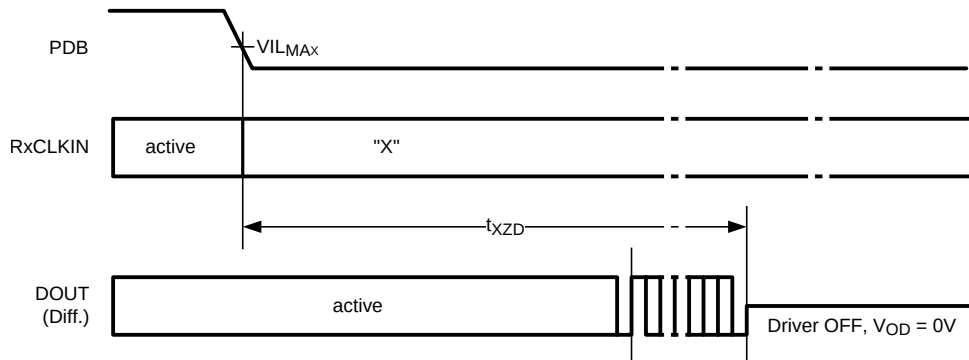


Figure 9. DS92LV0421 Disable Time

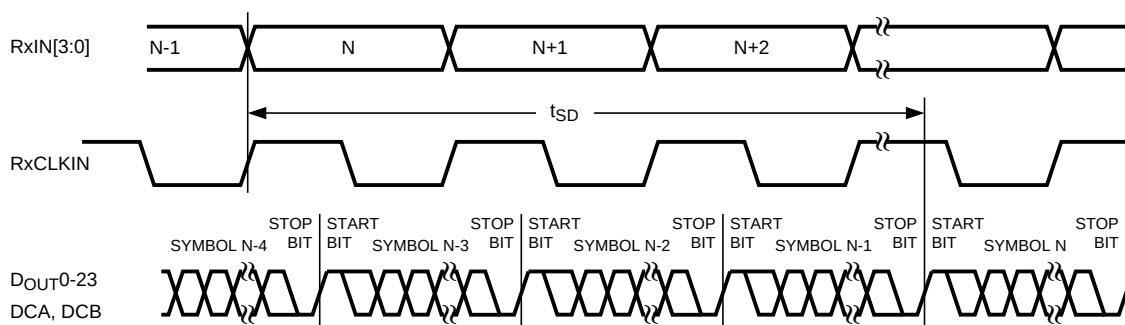


Figure 10. DS92LV0421 Latency Delay

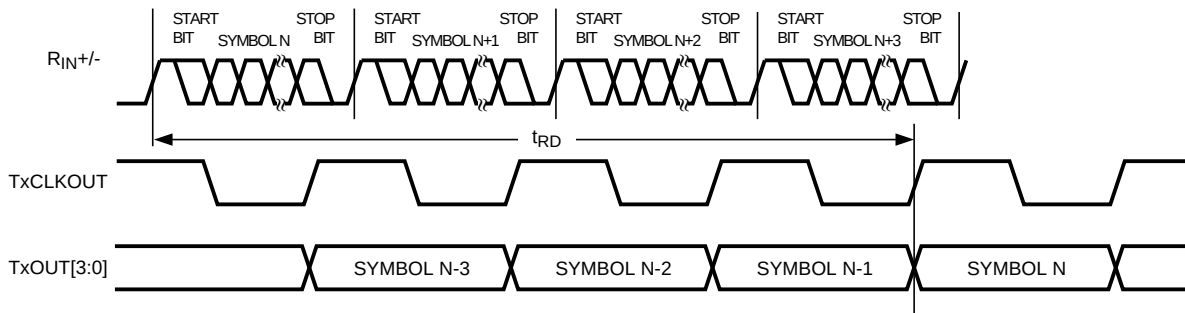


Figure 11. DS92LV0422 Latency Delay

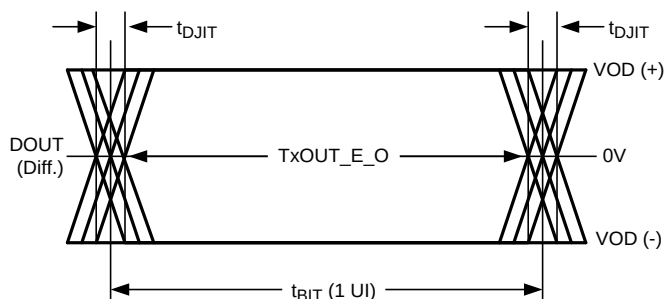
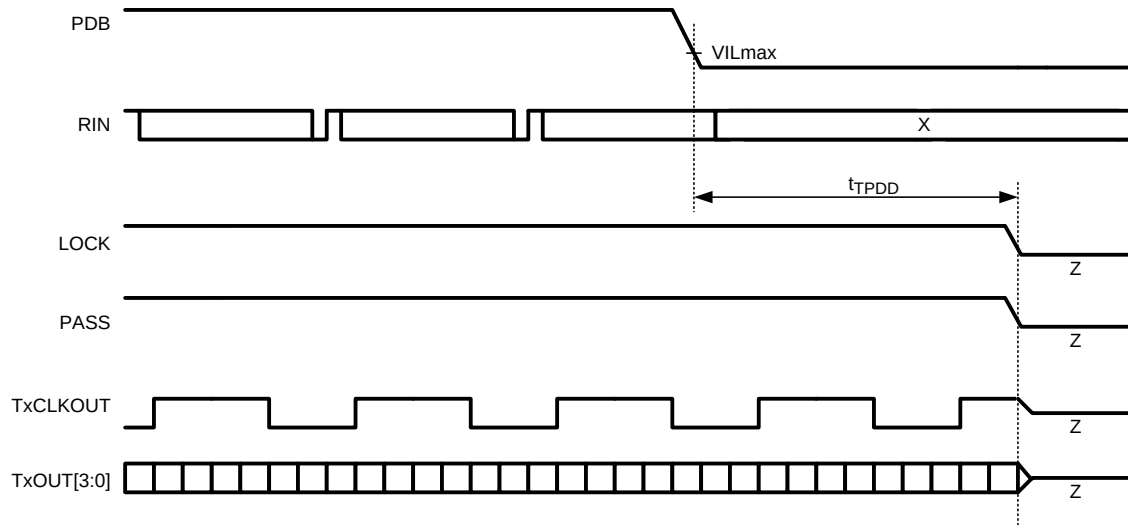
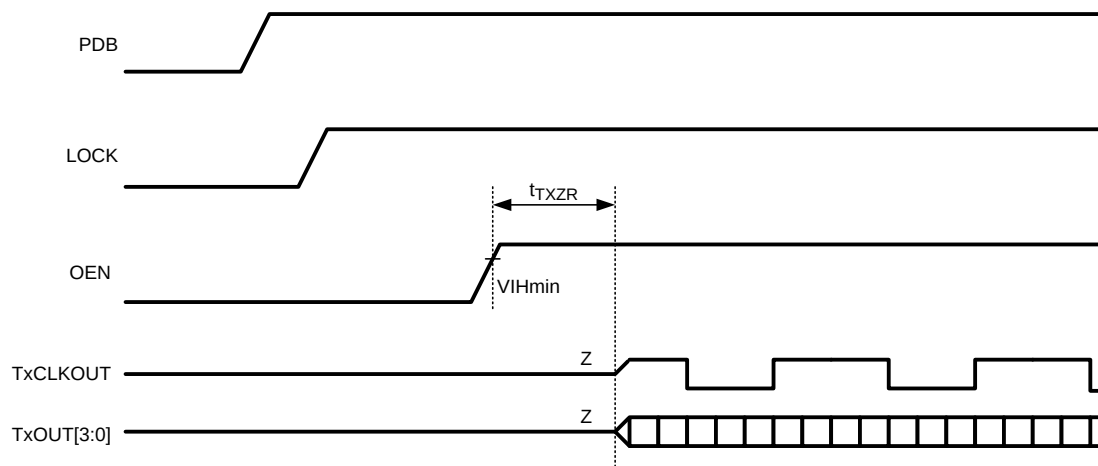
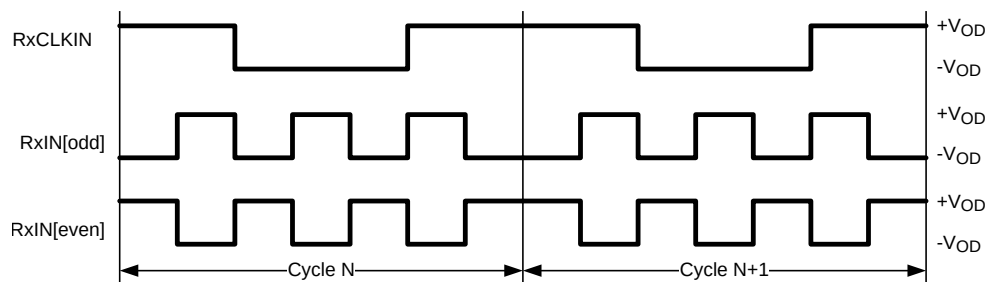


Figure 12. DS92LV0421 Output Jitter


Figure 13. DS92LV0422 Power-Down Delay

Figure 14. DS92LV0422 Enable Delay

Figure 15. Checkerboard Data Pattern

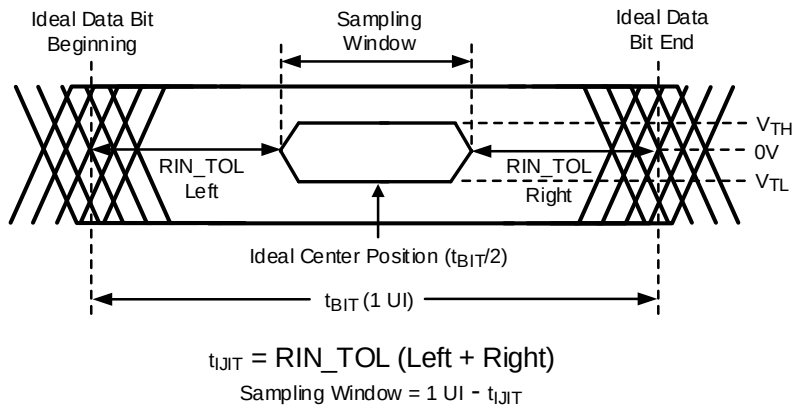


Figure 16. DS92LV0422 Receiver Input Jitter Tolerance

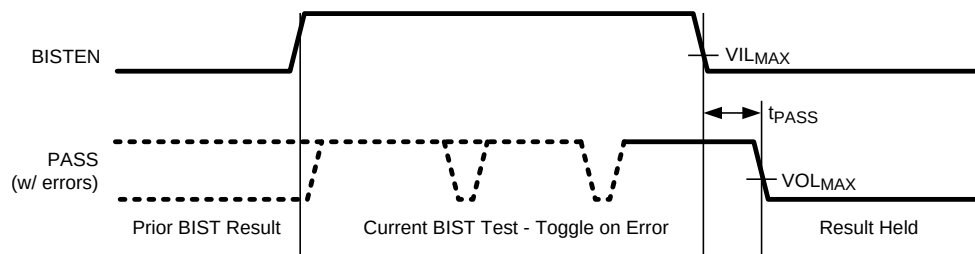


Figure 17. BIST PASS Waveform

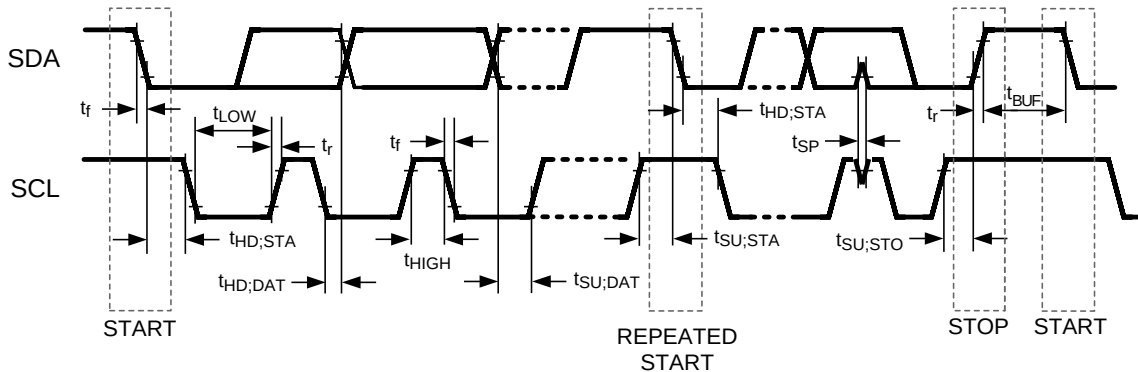
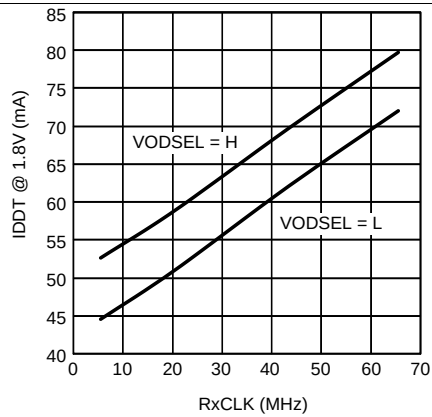
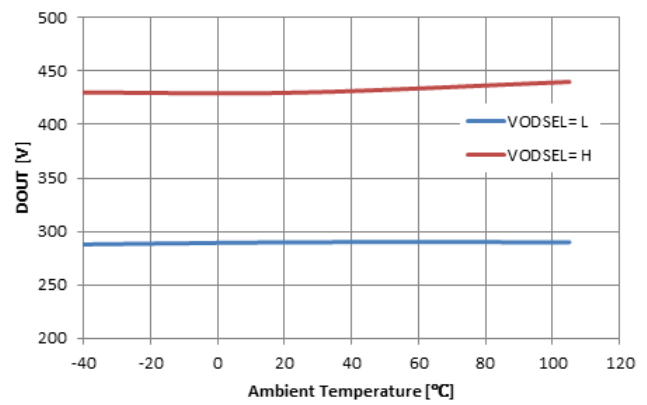


Figure 18. Serial Control Bus Timing Diagram

6.11 Typical Characteristics



**Figure 19. Typical IDD (1.8-V Supply)
vs RXCLKIN**



**Figure 20. Serializer DOUT Voltage
vs Ambient Temperature**

7 Detailed Description

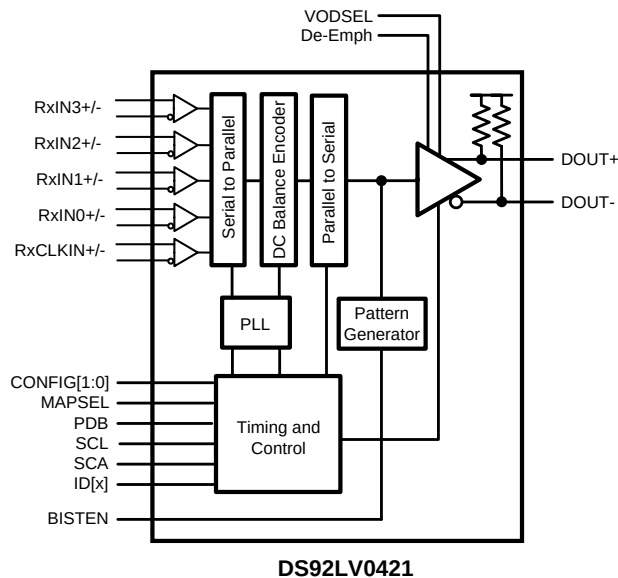
7.1 Overview

The DS92LV042x chipset transmits and receives 24 bits of data and 3 control signals, formatted as Channel Link LVDS data, over a single serial CML pair operating at 280 Mbps to 2.1 Gbps. The serial stream contains an embedded clock, video control signals, and the DC-balance information which enhances signal quality and supports AC coupling.

The deserializer can attain lock to a data stream without the use of a separate reference clock source, which greatly simplifies system complexity and overall cost. The deserializer also synchronizes to the serializer regardless of the data pattern, delivering true automatic *plug and lock* performance. It can lock to the incoming serial stream without the requirement of special training patterns or sync characters. The deserializer recovers the clock and data by extracting the embedded clock information, validating, and then deserializing the incoming data stream, providing a parallel Channel Link LVDS bus to the display, ASIC, or FPGA.

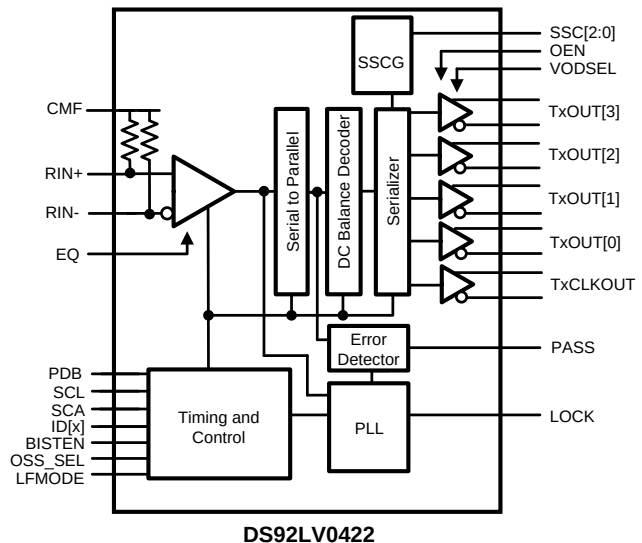
The DS92LV042x chipset can operate with up to 24 bits of raw data with three slower speed control bits encoded within the serial data stream. For applications that require less than the maximum 24 raw data bits per clock cycle, the user must ensure that all unused bit spaces or parallel LVDS channels are set to valid logic states, as all parallel lanes and 27 bit spaces are always sampled.

7.2 Functional Block Diagrams



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Figure 21. Serializer Block Diagram



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Figure 22. Deserializer Block Diagram

7.3 Feature Description

7.3.1 Parallel LVDS Data Transfer (Color Bit Mapping Select)

The DS92LV042x can be configured to accept or transmit 24-bit data with two different LVDS parallel interface mapping schemes:

- The normal Channel Link LVDS format (MSBs on LVDS Channel 3) can be selected by configuring the MAPSEL pin to high. See [Figure 23](#) for the normal Channel Link LVDS mapping.
- An alternate mapping scheme is available (LSBs on LVDS Channel 3) by configuring the MAPSEL pin to low. See [Figure 24](#) for the alternate LVDS mapping.

The mapping schemes can also be selected by register control. The alternate mapping scheme is useful in some applications where the receiving system, typically a display, requires the LSBs for the 24-bit color data to be sent on LVDS Channel 3.

NOTE

While the LVDS parallel interface has 28 bits defined, only 27 bits are recovered by the serializer and sent to the deserializer. This chipset supports 24-bit RGB plus the three video control signals. The 28th bit is not sampled, sent, or recovered.

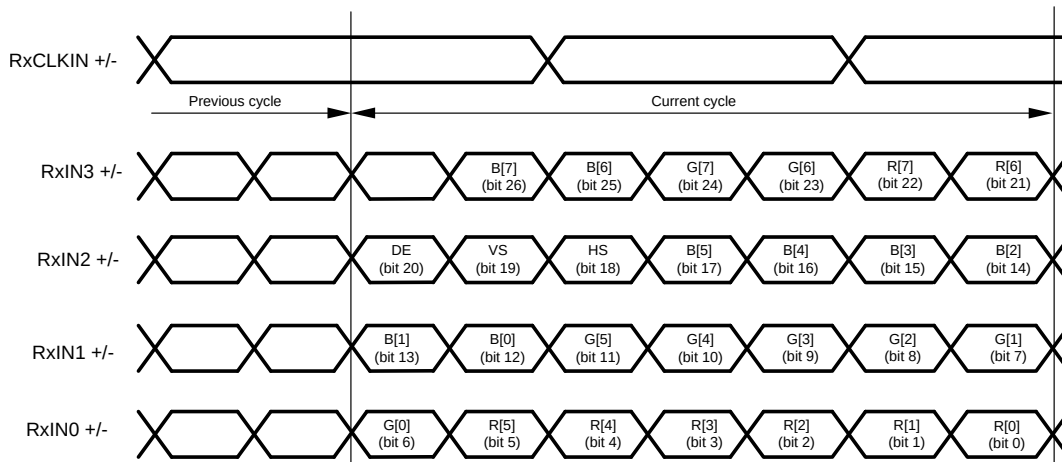


Figure 23. 8-Bit Channel Link Mapping: MSB's on RXIN3

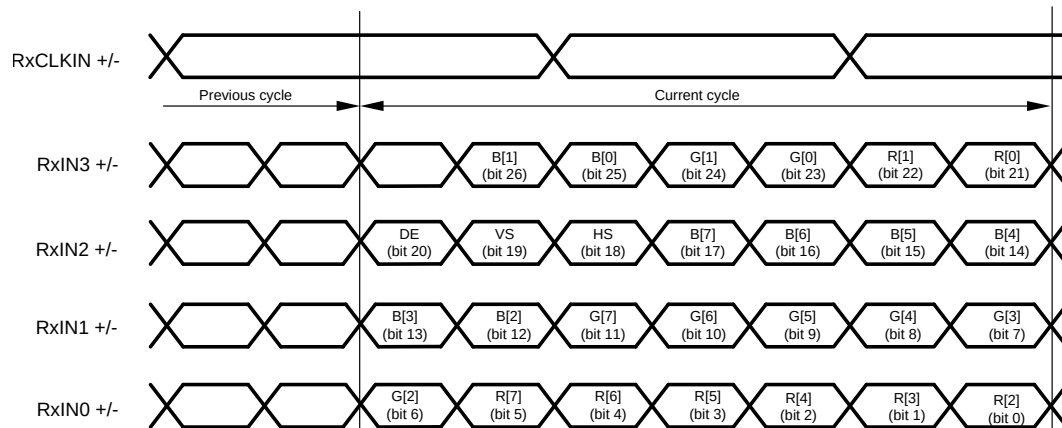


Figure 24. 8-Bit Channel Link Mapping: LSB's on RXIN3

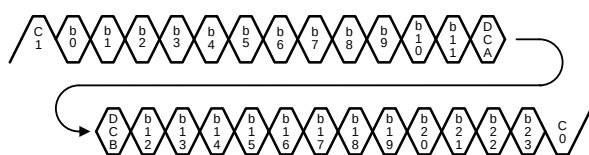
Feature Description (continued)

7.3.2 Serial Data Transfer

The DS92LV042x chipset transmits and receives a pixel of data in the following format: C1 and C0 represent the embedded clock in the serial stream. C1 is always high and C0 is always low. The b[23:0] contains the scrambled RGB data. DCB is the DC-Balanced control bit. DCB is used to minimize the short and long-term DC bias on the signal lines. This bit determines if the data is unmodified or inverted. DCA is used to validate data integrity in the embedded data stream and can also contain encoded control (VS, HS, DE). Both DCA and DCB coding schemes are generated by the serializer and decoded by the deserializer automatically. [Figure 25](#) illustrates the serial stream per clock cycle.

NOTE

[Figure 25](#) only illustrates the bits but does not actually represent the bit location, as the bits are scrambled and balanced continuously.



Feature Description (continued)

7.3.4 Serializer Functional Description

The serializer converts a Channel Link LVDS clock and data bus to a single serial output data stream and also acts as a signal generator for the chipset Built-In Self Test (BIST) mode. The device can be configured through external pins or through the optional serial control bus. The serializer features enhanced signal quality on the link by supporting: a selectable VOD level, a selectable de-emphasis for signal conditioning, and Channel Link II data coding that provides randomization, scrambling, and DC-balancing of the data. The serializer includes multiple features to reduce EMI associated with display data transmission. This includes the randomization and scrambling of the serial data and system spread spectrum clock support. The serializer includes power-saving features with a sleep mode, auto stop clock feature, and optional LVCMOS (1.8 V or 3.3 V) I/O compatibility (see also [Optional Serial Bus Control](#) and [Built-In Self Test \(BIST\)](#)).

7.3.4.1 Signal Quality Enhancers

7.3.4.1.1 Serializer VOD Select (VODSEL)

The serializer differential output voltage may be increased by setting the VODSEL pin high. When VODSEL is low, the DC VOD is at the standard (default) level. When VODSEL is high, the VOD is increased in level. The increased VOD is useful in extremely high noise environments and extra long cable length applications. When using de-emphasis, TI recommends setting VODSEL = H to avoid excessive signal attenuation, especially with the larger de-emphasis settings. This feature may be controlled by external pin or by register.

Table 1. Serializer Differential Output Voltage

INPUT	EFFECT	
	VOD (mV)	VOD (mVp-p)
L	±300	600
H	±450	900

7.3.4.1.2 Serializer De-Emphasis (DE-EMPH)

The de-emphasis pin controls the amount of de-emphasis beginning one full bit time after a logic transition that the serializer drives. This is useful to counteract loading effects of long or lossy cables. This pin must be left open if used for standard switching currents (no de-emphasis) or if used under register control. De-emphasis is selected by connecting a resistor on this pin to ground, with the R value between 0.5 kΩ and 1 MΩ, or by register setting. When using de-emphasis, TI recommends setting VODSEL = H.

Table 2. De-Emphasis Resistor Value

RESISTOR VALUE (kΩ)	DE-EMPHASIS SETTING
Open	Disabled
0.6	–12 dB
1	–9 dB
2	–6 dB
5	–3 dB

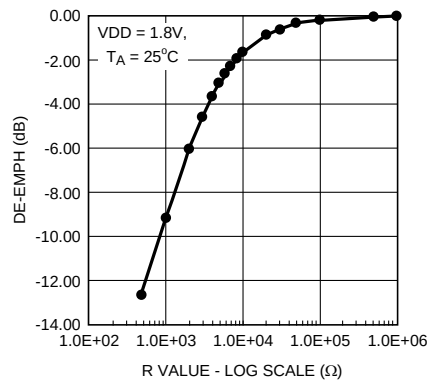


Figure 27. De-Emphasis vs R Value

7.3.4.2 EMI Reduction Features

7.3.4.2.1 Data Randomization and Scrambling

Channel Link II serializers and deserializers feature a three-step encoding process that enables the use of AC-coupled interconnects and also helps to manage EMI. The serializer first passes the parallel data through a scrambler which randomizes the data. The randomized data is then DC-balanced. The DC-balanced and randomized data then goes through a bit-shuffling circuit and is transmitted out on the serial line. This encoding process helps to prevent static data patterns on the serial stream. The resulting frequency content of the serial stream ranges from the parallel clock frequency to the Nyquist rate. For example, if the serializer and deserializer chipset is operating at a parallel clock frequency of 50 MHz, the resulting frequency content of the serial stream ranges from 50 MHz to 700 MHz ($50 \text{ MHz} \times 28 \text{ bits} = 1.4 \text{ GHz} / 2 = 700 \text{ MHz}$).

7.3.4.2.2 Serializer Spread Spectrum Compatibility

The serializer RXCLKIN is capable of tracking spread spectrum clocking (SSC) from a host source. The RXCLKIN accepts spread spectrum tracking up to 35-kHz modulation and ± 0.5 , ± 1 , or $\pm 2\%$ deviations (center spread). The maximum conditions for the RXCLKIN input are: a modulation frequency of 35 kHz and amplitude deviations of $\pm 2\%$ (4% total).

7.3.4.3 Power-Saving Features

7.3.4.3.1 Serializer Power-Down Feature (PDB)

The serializer has a PDB input pin to enable or power down the device. This pin is controlled by the host and is used to save power, disabling the link when the display is not required. In power-down mode, the high-speed driver outputs are both pulled to VDD and present a 0-V VOD state.

NOTE

In power-down, the optional serial bus control registers are RESET.

7.3.4.3.2 Serializer Stop Clock Feature

The serializer enters a low power SLEEP state when the RXCLKIN is stopped. A STOP condition is detected when the input clock frequency is less than 3 MHz. The clock must be held at a static low or high state. When the RXCLKIN starts again, the serializer locks to the valid input clock and then transmits the serial data to the deserializer.

NOTE

In STOP CLOCK SLEEP, the optional serial bus control registers values are RETAINED.

7.3.4.3.3 Serializer 1.8-V or 3.3-V VDDIO Operation

The serializer parallel control bus can operate with 1.8-V or 3.3-V levels (V_{DDIO}) for host compatibility. The 1.8-V levels offers lower noise (EMI) and also system power savings.

7.3.5 Deserializer Functional Description

The deserializer converts a single input serial data stream to a Channel Link LVDS clock and data bus and also provides a signal check for the chipset Built-In Self Test (BIST) mode. The device can be configured through external and strap pins or through the optional serial control bus. The deserializer features enhanced signal quality on the link by supporting an integrated equalizer on the serial input and Channel Link II data encoding which provides randomization, scrambling, and DC-balancing of the data. The deserializer includes multiple features to reduce EMI associated with display data transmission. This includes the randomization and scrambling of the data, Channel Link LVDS output interface, and output spread spectrum clock generation (SSCG) support. The deserializer includes power saving features with a power-down mode and optional LVCMOS (1.8-V) interface compatibility.

7.3.5.1 Signal Quality Enhancers

7.3.5.1.1 Deserializer Input Equalizer Gain (EQ)

The deserializer can enable receiver input equalization of the serial stream to increase the eye opening to the deserializer input.

NOTE

This function cannot be seen at the $RXIN\pm$ input. The equalization feature may be controlled by the external pin or by register.

Table 3. Receiver Equalization Configuration

EQ (STRAP OPTION)	EFFECT
L	~1.625 dB (OFF)
H	~13 dB

7.3.5.2 EMI Reduction Features

7.3.5.2.1 Deserializer VOD Select (VODSEL)

The differential output voltage of the Channel Link parallel interface is controlled by the VODSEL input.

Table 4. Deserializer Differential Output Voltage

INPUT	EFFECT	
	VOD (mV)	VOD (mVp-p)
VODSEL		
L	±250	500
H	±400	800

7.3.5.2.2 Deserializer Common-Mode Filter Pin (CMF) (Optional)

The deserializer provides access to the center tap of the internal termination. A capacitor may be placed on this pin for additional common-mode filtering of the differential pair. This can be useful in high-noise environments for additional noise rejection capability. A 4.7- μ F capacitor may be connected from this pin to Ground.

7.3.5.2.3 Deserializer SSCG Generation (Optional)

The deserializer provides an internally generated spread spectrum clock (SSCG) to modulate its outputs. Both clock and data outputs are modulated. This aids to lower system EMI. Output SSCG deviations of $\pm 2\%$ (4% total) at up to 100-kHz modulations are available (see [Table 5](#)). This feature may be controlled by external pins or by register.

NOTE

The deserializer supports the SSCG function with TXCLKOUT = 10 MHz to 65 MHz. When the TXCLKOUT = 65 MHz to 75 MHz, it is required to disable the SSCG function (SSC[2:0] = 000).

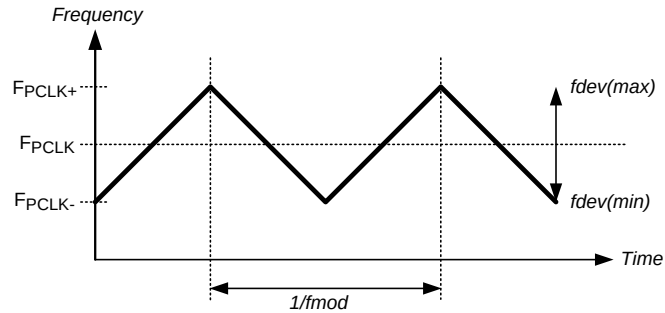


Figure 28. SSCG Waveform

Table 5. SSCG Configuration (LFMODE = L): Deserializer Output

SSC[2:0] INPUTS LFMODE = L (20 TO 65 MHz)			RESULT	
SSC2	SSC1	SSC0	fdev (%)	fmod (kHz)
L	L	L	Off	Off
L	L	H	±0.9	CLK/2168
L	H	L	±1.2	
L	H	H	±1.9	
H	L	L	±2.3	
H	L	H	±0.7	CLK/1300
H	H	L	±1.3	
H	H	H	±1.7	

Table 6. SSCG Configuration (LFMODE = H): Deserializer Output

SSC[2:0] INPUTS LFMODE = H (10 TO 20 MHz)			RESULT	
SSC2	SSC1	SSC0	fdev (%)	fmod (kHz)
L	L	L	Off	Off
L	L	H	±0.7	CLK/625
L	H	L	±1.3	
L	H	H	±1.8	
H	L	L	±2.2	
H	L	H	±0.7	CLK/385
H	H	L	±1.2	
H	H	H	±1.7	

7.3.5.2.4 Power-Saving Features

7.3.5.2.4.1 Deserializer Power-Down Feature (PDB)

The deserializer has a PDB input pin to enable or power down the device. This pin can be controlled by the system to save power, disabling the deserializer when the display is not required. An auto-detect mode is also available. In this mode, the PDB pin is tied high and the deserializer enters power-down when the serial stream stops. When the serial stream starts up again, the deserializer locks to the input stream, asserts the LOCK pin, and outputs valid data. In power-down mode, the LVDS data and clock output states are determined by the OSS_SEL status.

NOTE

In power-down, the optional serial bus control registers are RESET.

7.3.5.2.4.2 Deserializer Stop Stream SLEEP Feature

The deserializer enters a low power SLEEP state when the input serial stream is stopped. A STOP condition is detected when the embedded clock bits are not present. When the serial stream starts again, the deserializer then locks to the incoming signal and recovers the data.

NOTE

In STOP STREAM SLEEP, the optional serial bus control registers values are RETAINED.

7.3.5.2.4.3 Deserializer 1.8-V or 3.3-V VDDIO Operation

The deserializer parallel control bus can operate with 1.8-V or 3.3-V levels (V_{DDIO}) for target (display) compatibility. The 1.8-V levels offers lower noise (EMI) and also system power savings.

7.3.5.3 Deserializer Clock-Data Recovery Status Flag (LOCK), Output Enable (OEN), and Output State Select (OSS_SEL)

When PDB is driven high, the CDR PLL begins locking to the serial input, and LOCK goes from TRI-STATE to low (depending on the value of the OSS_SEL setting). After the DS92LV0422 completes its lock sequence to the input serial data, the LOCK output is driven high, indicating valid data and clock recovered from the serial input is available on the Channel Link outputs. The TXCLKOUT output is held at its current state at the change from OSC_CLK (if this is enabled through OSC_SEL) to the recovered clock (or vice versa).

NOTE

The Channel Link outputs may be held in an inactive state (TRI-STATE) through the use of the Output Enable pin (OEN).

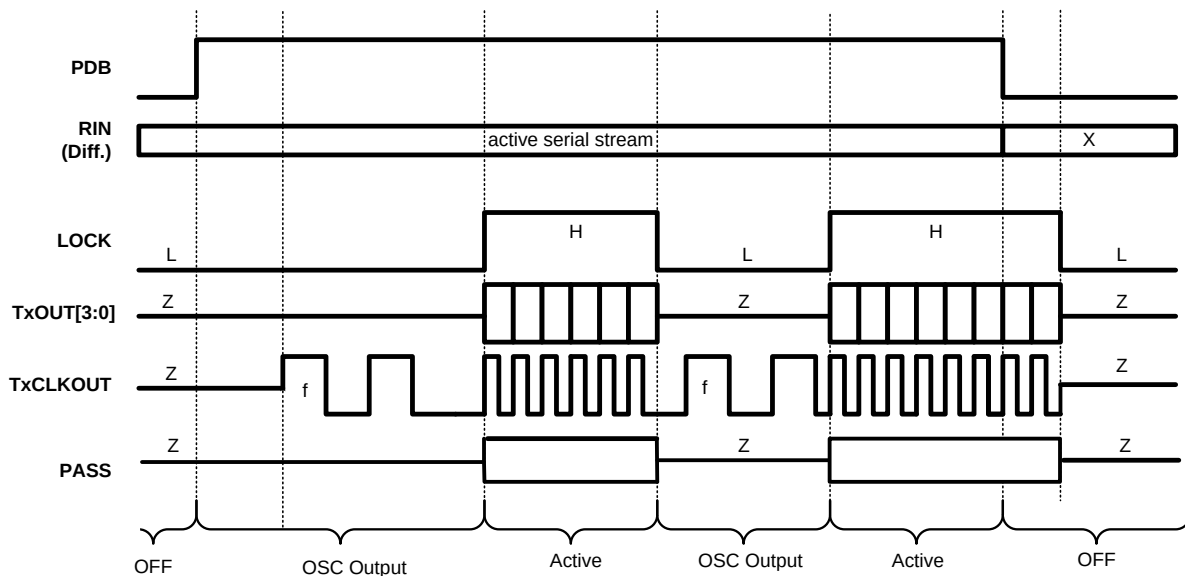
If there is a loss of clock from the input serial stream, LOCK is driven low and the state of the outputs are based on the OSS_SEL setting (configuration pin or register).

Table 7. PDB, OEN, and OSS_SEL Configuration (Deserializer Outputs)

SERIAL INPUT	INPUTS			OUTPUTS	
	PDB	OEN	OSS_SEL	LOCK	OTHER OUTPUTS
X	L	X	X	X	TXCLKOUT is TRI-STATE TXOUT[3:0] are TRI-STATE PASS is TRI-STATE
Static	H	X	L	L	TXCLKOUT is TRI-STATE TXOUT[3:0] are TRI-STATE PASS is HIGH
Static	H	L	H	L	TXCLKOUT is TRI-STATE TXOUT[3:0] are TRI-STATE PASS is TRI-STATE
Static	H	H	H	L	TXCLKOUT is TRI-STATE or Oscillator Output through Register bit TXOUT[3:0] are TRI-STATE PASS is TRI-STATE
Active	H	L	X	H	TXCLKOUT is TRI-STATE TXOUT[3:0] are TRI-STATE PASS is Active
Active	H	H	X	H	TXCLKOUT is Active TXOUT[3:0] are Active PASS is Active (Normal operating mode)

7.3.5.4 Deserializer Oscillator Output (Optional)

The deserializer provides an optional clock output when the input clock (serial stream) has been lost. This is based on an internal oscillator. The frequency of the oscillator may be selected. This feature may be controlled by external pin or by register.



CONDITIONS: OEN = H, OSS_SEL = H, and OSC_SEL not equal to 000.

Figure 29. TXCLKOUT Output Oscillator Option Enabled

7.3.6 Built-In Self Test (BIST)

An optional at-speed Built-In Self Test (BIST) feature supports the testing of the high-speed serial link. This is useful in the prototype stage, equipment production, in-system test, and for system diagnostics. In BIST mode, only an input clock is required along with control to the serializer and deserializer BISTEN input pins. The serializer outputs a test pattern (PRBS-7) and drives the link at speed. The deserializer detects the PRBS-7 pattern and monitors it for errors. A PASS output pin toggles to flag any payloads that are received with 1 to 24 errors. Upon completion of the test, the result of the test is held on the PASS output until reset (new BIST test or power-down). A high on PASS indicates NO ERRORS were detected. A low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin.

Inter-operability is supported between this Channel Link II device and all Channel Link II generations (Gen 1/2/3); see respective data sheets for details on entering BIST mode and control.

7.3.6.1 Sample BIST Sequence

See [Figure 30](#) for the BIST mode flow diagram.

Step 1: Place the serializer in BIST Mode by setting serializer BISTEN = H. BIST Mode is enabled through the BISTEN pin. An RXCLKIN is required for BIST. When the deserializer detects the BIST mode pattern and command (DCA and DCB code), the data and control signal outputs are shut off.

Step 2: Place the deserializer in BIST mode by setting the BISTEN = H. The deserializer is now in BIST mode and checks the incoming serial payloads for errors. If an error in the payload (1 to 24) is detected, the PASS pin switches low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To stop BIST mode, the deserializer BISTEN pin is set low. The deserializer stops checking the data, and the final test result is held on the PASS pin. If the test ran error free, the PASS output is high. If there is one or more errors detected, the PASS output is low. The PASS output state is held until a new BIST is run, the device is RESET, or powered down. The BIST duration is user controlled by the duration of the BISTEN signal.

Step 4: To return the link to normal operation, the serializer BISTEN input is set low. The link returns to normal operation.

[Figure 31](#) shows the waveform diagram of a typical BIST test for two cases. Case 1 is error-free, and Case 2 shows one with multiple errors. In most cases, it is difficult to generate errors due to the robustness of the link (differential data transmission and so forth), thus they may be introduced by greatly extending the cable length, faulting the interconnect, or reducing signal condition enhancements (de-emphasis, VODSEL, or Rx equalization).

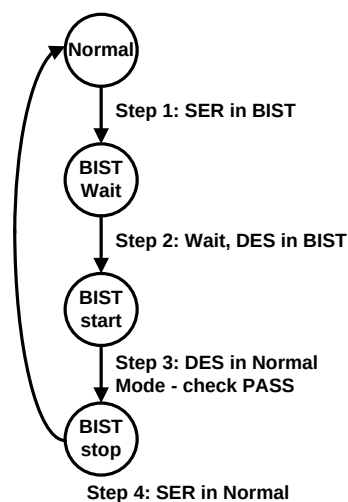


Figure 30. BIST Mode Flow Diagram

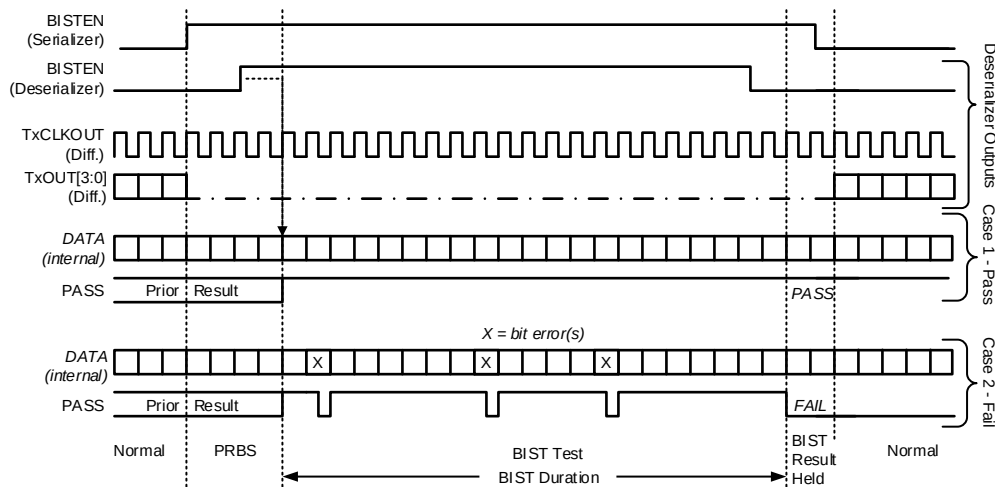


Figure 31. BIST Waveforms

7.3.6.2 BER Calculations

It is possible to calculate the approximate Bit Error Rate (BER). The following is required:

- Clock Frequency (MHz)
- BIST Duration (seconds)
- BIST Test Result (PASS)

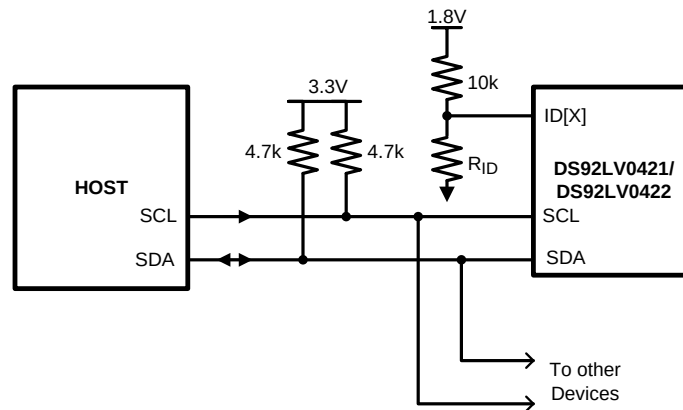
The BER is less than or equal to one over the product of 24 times the RXCLKIN rate times the test duration. If we assume a 65-MHz clock, a 10-minute (600 seconds) test, and a PASS, the BER is $\leq 1.07 \times 10^{-12}$.

BIST mode runs a check on the data payload bits. The LOCK pin also provides a link status. If the recovery of the C0 and C1 bits does not reconstruct the expected clock signal, the LOCK pin switches low. The combination of the LOCK and at-speed BIST PASS pin provides a powerful tool for system evaluation and performance monitoring.

7.3.7 Optional Serial Bus Control

The serializer and deserializer may also be configured by the use of a serial control bus that is I²C protocol-compatible. By default, the I²C Reg 0x00 = 0x00, and all configuration is set by control or strap pins. Writing Reg 0x00 = 0x01 enables or allows configuration by registers; this overrides the control or strap pins. Multiple devices may share the serial control bus, because multiple addresses are supported (see [Figure 32](#)).

The serial bus is comprised of three pins. The SCL is a serial bus clock input. The SDA is the serial bus data input or output signal. Both SCL and SDA signals require an external pullup resistor to V_{DDIO}. For most applications, a 4.7-kΩ pullup resistor to V_{DDIO} may be used. The resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled high or driven low.



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Figure 32. Serial Control Bus Connection

The third pin is the ID[X] pin. This pin sets one of four possible device addresses. Two different connections are possible:

- The pin may be pulled to V_{DD} (1.8 V, not V_{DDIO}) with a 10-k Ω resistor.
- The pin may be pulled to V_{DD} (1.8 V, not V_{DDIO}) with a 10-k Ω resistor and pulled down to ground with a recommended value R_{ID} resistor. This creates a voltage divider that sets the other three possible addresses.

See [Table 8](#) for the serializer and [Table 9](#) for the deserializer. Do not tie ID[X] directly to VSS.

Table 8. ID[X] Resistor Value: DS92LV0421 (Serializer)

RESISTOR R_{ID} k Ω ⁽¹⁾ (5% TOL)	ADDRESS 7'b	ADDRESS 8'b 0 APPENDED (WRITE)
0.47	7b' 110 1001 (h'69)	8b' 1101 0010 (h'D2)
2.7	7b' 110 1010 (h'6A)	8b' 1101 0100 (h'D4)
8.2	7b' 110 1011 (h'6B)	8b' 1101 0110 (h'D6)
Open	7b' 110 1110 (h'6E)	8b' 1101 1100 (h'DC)

(1) $R_{ID} \neq 0 \Omega$. Do not connect directly to VSS (GND). This is not a valid address.

Table 9. ID[X] Resistor Value – DS92LV0422 (Deserializer)

RESISTOR R_{ID} k Ω ⁽¹⁾ (5% TOL)	ADDRESS 7'b	ADDRESS 8'b 0 APPENDED (WRITE)
0.47	7b' 111 0001 (h'71)	8b' 1110 0010 (h'E2)
2.7	7b' 111 0010 (h'72)	8b' 1110 0100 (h'E4)
8.2	7b' 111 0011 (h'73)	8b' 1110 0110 (h'E6)
Open	7b' 111 0110 (h'76)	8b' 1110 1100 (h'EC)

(1) $R_{ID} \neq 0 \Omega$. Do not connect directly to VSS (GND). This is not a valid address.

The serial bus protocol is controlled by START, START-repeated, and STOP phases. A START occurs when SCL transitions low while SDA is high. A STOP occurs when SDA transitions high while SCL is also high (see Figure 33).

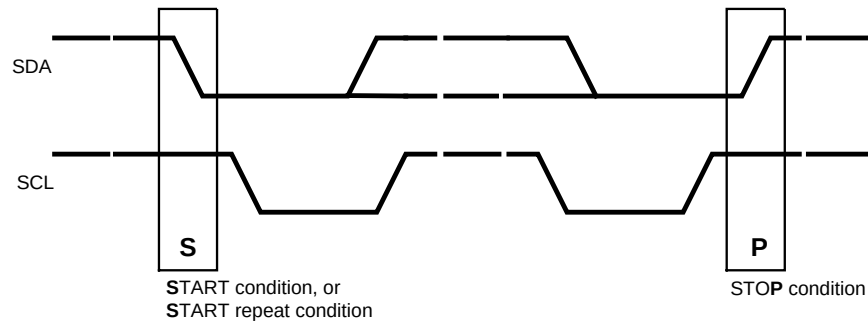


Figure 33. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match the slave address of a device, it Not-acknowledges (NACKs) the master by letting SDA be pulled high. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a start condition or a repeated start condition. All communication on the bus ends with a stop condition. A READ is shown in Figure 34 and a WRITE is shown in Figure 35.

NOTE

During initial power-up, a delay of 10 ms is required before the I²C responds.

If the serial bus is not required, the three pins may be left open (NC).

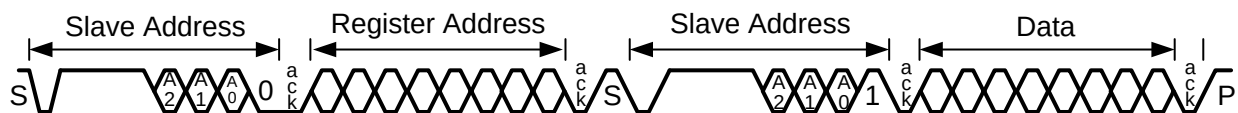


Figure 34. Serial Control Bus: READ



Figure 35. Serial Control Bus: WRITE

7.4 Device Functional Modes

7.4.1 Serializer and Deserializer Operating Modes and Reverse Compatibility (CONFIG[1:0])

The DS92LV042x chipset is compatible with other single serial lane Channel Link II or FPD-Link II devices. Configuration modes are provided for reverse compatibility with the DS90C241 or DS90C124 chipset (FPD-Link II Generation 1) and also the DS90UR241 / DS90UR124 chipset (FPD-Link II Generation 2) by setting the respective mode with the CONFIG[1:0] pins on the serializer or deserializer as shown in [Table 10](#) and [Table 11](#). This selection also determines whether the control signal filter feature is enabled or disabled in the normal mode. This feature may be controlled by external pin or by register.

Table 10. DS92LV0421 Serializer Modes

CONFIG1	CONFIG0	MODE	COMPATIBLE DESERIALIZER DEVICE
L	L	Normal Mode, Control Signal Filter disabled	DS92LV0422, DS92LV0412, DS92LV2422, DS92LV2412
L	H	Normal Mode, Control Signal Filter enabled	DS92LV0422, DS92LV0412, DS92LV2422, DS92LV2412
H	L	Reverse Compatibility Mode (FPD-Link II, GEN2)	DS90UR124, DS99R124Q-Q1
H	H	Reverse Compatibility Mode (FPD-Link II, GEN1)	DS90C124

Table 11. DS92LV0422 Deserializer Modes

CONFIG1	CONFIG0	MODE	COMPATIBLE SERIALIZER DEVICE
L	L	Normal Mode, Control Signal Filter disabled	DS92LV0421, DS92LV0411, DS92LV2421, DS92LV2411
L	H	Normal Mode, Control Signal Filter enabled	DS92LV0421, DS92LV0411, DS92LV2421, DS92LV2411
H	L	Reverse Compatibility Mode (FPD-Link II, GEN2)	DS90UR241, DS99R421
H	H	Reverse Compatibility Mode (FPD-Link II, GEN1)	DS90C241

7.5 Register Maps

Table 12. SERIALIZER: Serial Bus Control Registers

ADD (DEC)	ADD (HEX)	REGISTER NAME	BIT(S)	R/W	DEFAULT (BIN)	FUNCTION	DESCRIPTION
0	0	Serializer Config 1	7	R/W	0	Reserved	Reserved
			6	R/W	0	MAPSEL	0: LSB on RXIN3 1: MSB on RXIN3
			5	R/W	0	VODSEL	0: Low 1: High
			4	R/W	0	Reserved	Reserved
			3:2	R/W	00	CONFIG	00: Normal Mode, Control Signal Filter Disabled 01: Normal Mode, Control Signal Filter Enabled 10: DS90UR124, DS99R124Q-Q1 Reverse-Compatibility Mode (FPD-Link II, GEN2) 11: DS90C124 Reverse-Compatibility Mode (FPD-Link II, GEN1)
			1	R/W	0	SLEEP	Note – not the same function as PowerDown (PDB) 0: Normal Mode 1: Sleep Mode – Register settings retained.
			0	R/W	0	REG	0: Configurations set from control pins 1: Configuration set from registers (except I ² C_ID)
1	1	Device ID	7	R/W	0	REG ID	0: Address from ID[X] Pin 1: Address from Register
			6:0	R/W	1101000	ID[X]	Serial Bus Device ID, four IDs are: 7b '1101 001 (h'69) 7b '1101 010 (h'6A) 7b '1101 011 (h'6B) 7b '1101 110 (h'6E) All other addresses are reserved.
2	2	De-Emphasis Control	7:5	R/W	000	De-Emphasis Setting	000: set by external resistor 001: –1 dB 010: –2 dB 011: –3.3 dB 100: –5 dB 101: –6.7 dB 110: –9 dB 111: –12 dB
			4	R/W	0	De-Emphasis EN	0: De-emphasis Enabled 1: De-emphasis Disabled
			3:0	R/W	0000	Reserved	Reserved

Table 13. DESERIALIZER: Serial Bus Control Registers

ADD (DEC)	ADD (HEX)	REGISTER NAME	BIT(S)	R/W	DEFAULT (BIN)	FUNCTION	DESCRIPTION
0	0	Deserializer Config 1	7	R/W	0	LFMODE	0: 20 to 65 MHz SSCG Operation 1: 10 to 20 MHz SSCG Operation
			6	R/W	0	MAPSEL	Channel Link Map Select 0: LSB on TXOUT3± 1: MSB on TXOUT3±
			5	R/W	0	<i>Reserved</i>	<i>Reserved</i>
			4	R/W	0	<i>Reserved</i>	<i>Reserved</i>
			3:2	R/W	00	CONFIG	00: Normal Mode, Control Signal Filter Disabled 01: Normal Mode, Control Signal Filter Enabled 10: DS90UR241, DS99R421 Reverse-Compatibility Mode (FPD-Link II, GEN2) 11: DS90C241 Reverse-Compatibility Mode (FPD-Link II, GEN1)
			1	R/W	0	SLEEP	Note – not the same function as <i>PowerDown</i> (PDB) 0: Normal Mode 1: Sleep Mode – Register settings retained.
			0	R/W	0	REG Control	0: Configurations set from control or strap pins 1: Configuration set from registers (except I ² C_ID)
1	1	Device ID	7	R/W	0	REG ID	0: Address from ID[X] Pin 1: Address from Register
			6:0	R/W	1110000	ID[X]	Serial Bus Device ID, four IDs are: 7b' 111 0001 (h'71) 7b' 111 0010 (h'72) 7b' 111 0011 (h'73) 7b' 111 0110 (h'76) All other addresses are <i>reserved</i> .
2	2	Deserializer Features 1	7	R/W	0	OEN	Output Enable Input See Table 7
			6	R/W	0	OSS_SEL	Output Sleep State Select See Table 7
			5:4	R/W	00	<i>Reserved</i>	<i>Reserved</i>
			3	R/W	0	VODSEL	Differential LVDS Driver Output Voltage Select 0: LVDS VOD is ±250 mV, 500 mVp-p (typ) 1: LVDS VOD is ±400 mV, 800 mVp-p (typ)
			2:0	R/W	000	OSC_SEL	000: OFF 001: <i>Reserved</i> 010: 25 MHz ± 40% 011: 16.7 MHz ± 40% 100: 12.5 MHz ± 40% 101: 10 MHz ± 40% 110: 8.3 MHz ± 40% 111: 6.3 MHz ± 40%

Table 13. DESERIALIZER: Serial Bus Control Registers (continued)

ADD (DEC)	ADD (HEX)	REGISTER NAME	BIT(S)	R/W	DEFAULT (BIN)	FUNCTION	DESCRIPTION
3	3	Deserializer Features 2	7:5	R/W	000	EQ Gain	000: ~1.625 dB 001: ~3.25 dB 010: ~4.87 dB 011: ~6.5 dB 100: ~8.125 dB 101: ~9.75 dB 110: ~11.375 dB 111: ~13 dB
			4	R/W	0	EQ Enable	0: EQ = disabled 1: EQ = enabled
			3	R/W	0	Reserved	Reserved
			2:0	R/W	000	SSC	If LFMODE = 0 then: 000: SSCG OFF 001: fdev = ±0.9%, fmod = CLK/2168 010: fdev = ±1.2%, fmod = CLK/2168 011: fdev = ±1.9%, fmod = CLK/2168 100: fdev = ±2.3%, fmod = CLK/2168 101: fdev = ±0.7%, fmod = CLK/1300 110: fdev = ±1.3%, fmod = CLK/1300 111: fdev = ±1.7%, fmod = CLK/1300 If LFMODE = 1, then: 001: fdev = ±0.7%, fmod = CLK/625 010: fdev = ±1.3%, fmod = CLK/625 011: fdev = ±1.8%, fmod = CLK/625 100: fdev = ±2.2%, fmod = CLK/625 101: fdev = ±0.7%, fmod = CLK/385 110: fdev = ±1.2%, fmod = CLK/385 111: fdev = ±1.7%, fmod = CLK/385

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Display Application

The DS92LV042x chipset is intended for interface between a host (graphics processor) and a display. It supports a 24-bit color depth (RGB888) and up to 1024 × 768 display formats. In a RGB888 application, 24 color bits (R[7:0], G[7:0], and B[7:0]), Pixel Clock (PCLK), and three control bits (VS, HS, and DE) are supported across the serial link with RXCLKIN rates from 10 to 75 MHz. The chipset may also be used in 18-bit color applications. In this application, three to six general-purpose signals may also be sent from host to display.

8.1.2 Live Link Insertion

The serializer and deserializer devices support live link or cable hot plug applications. The automatic receiver lock to random data *plug and go* hot insertion capability allows the DS92LV0422 to attain lock to the active data stream during a live insertion event.

8.1.3 Alternate Color or Data Mapping

Color-mapped data pin names are provided to specify a recommended mapping for 24-bit and 18-bit applications. Seven (7) is assumed to be the MSB, and Zero (0) is assumed to be the LSB. While this is recommended, it is not required. When connecting to earlier generations of FPD-Link II serializer and deserializer devices, a color mapping review is recommended to ensure the correct connectivity is obtained. [Table 14](#) provides examples for interfacing between DS92LV0421 and different deserializers. [Table 15](#) provides examples for interfacing between DS92LV0422 and different serializers.

Table 14. Serializer Alternate Color or Data Mapping

CHANNEL LINK	BIT NUMBER	RGB (LSB EXAMPLE)	DS92LV2422	DS90UR124	DS99R124Q-Q1	DS90C124
RXIN3	Bit 26	B1	B1	N/A	N/A	N/A
	Bit 25	B0	B0			
	Bit 24	G1	G1			
	Bit 23	G0	G0			
	Bit 22	R1	R1			
	Bit 21	R0	R0			
RXIN2	Bit 20	DE	DE	ROUT20	TXOUT2	ROUT20
	Bit 19	VS	VS	ROUT19		ROUT19
	Bit 18	HS	HS	ROUT18		ROUT18
	Bit 17	B7	B7	ROUT17		ROUT17
	Bit 16	B6	B6	ROUT16		ROUT16
	Bit 15	B5	B5	ROUT15		ROUT15
	Bit 14	B4	B4	ROUT14		ROUT14

Application Information (continued)
Table 14. Serializer Alternate Color or Data Mapping (continued)

CHANNEL LINK	BIT NUMBER	RGB (LSB EXAMPLE)	DS92LV2422	DS90UR124	DS99R124Q-Q1	DS90C124
RXIN1	Bit 13	B3	B3	ROUT13	TXOUT1	ROUT13
	Bit 12	B2	B2	ROUT12		ROUT12
	Bit 11	G7	G7	ROUT11		ROUT11
	Bit 10	G6	G6	ROUT10		ROUT10
	Bit 9	G5	G5	ROUT9		ROUT9
	Bit 8	G4	G4	ROUT8		ROUT8
	Bit 7	G3	G3	ROUT7		ROUT7
RXIN0	Bit 6	G2	G2	ROUT6	TXOUT0	ROUT6
	Bit 5	R7	R7	ROUT5		ROUT5
	Bit 4	R6	R6	ROUT4		ROUT4
	Bit 3	R5	R5	ROUT3		ROUT3
	Bit 2	R4	R4	ROUT2		ROUT2
	Bit 1	R3	R3	ROUT1		ROUT1
	Bit 0	R2	R2	ROUT0		ROUT0
N/A	N/A	N/A	N/A	ROUT23 ⁽¹⁾	OS2 ⁽¹⁾	ROUT23 ⁽¹⁾
				ROUT22 ⁽¹⁾	OS1 ⁽¹⁾	ROUT22 ⁽¹⁾
				ROUT21 ⁽¹⁾	OS0 ⁽¹⁾	ROUT21 ⁽¹⁾
DS92LV0421 SETTINGS	MAPSEL = 0		CONFIG[1:0] = 00	CONFIG[1:0] = 10		CONFIG[1:0] = 11

(1) These bits are not supported by the DS92LV0421.

Table 15. Deserializer Alternate Color or Data Mapping

CHANNEL LINK	BIT NUMBER	RGB (LSB EXAMPLE)	DS92LV2421	DS90UR241	DS99R421	DS90C241
TXOUT3	Bit 26	B1	B1	N/A	N/A	N/A
	Bit 25	B0	B0			
	Bit 24	G1	G1			
	Bit 23	G0	G0			
	Bit 22	R1	R1			
	Bit 21	R0	R0			
TXOUT2	Bit 20	DE	DE	DIN20	RXIN2	DIN20
	Bit 19	VS	VS	DIN19		DIN19
	Bit 18	HS	HS	DIN18		DIN18
	Bit 17	B7	B7	DIN17		DIN17
	Bit 16	B6	B6	DIN16		DIN16
	Bit 15	B5	B5	DIN15		DIN15
	Bit 14	B4	B4	DIN14		DIN14
TXOUT1	Bit 13	B3	B3	DIN13	RXIN1	DIN13
	Bit 12	B2	B2	DIN12		DIN12
	Bit 11	G7	G7	DIN11		DIN11
	Bit 10	G6	G6	DIN10		DIN10
	Bit 9	G5	G5	DIN9		DIN9
	Bit 8	G4	G4	DIN8		DIN8
	Bit 7	G3	G3	DIN7		DIN7

DS92LV0421, DS92LV0422

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Table 15. Deserializer Alternate Color or Data Mapping (continued)

CHANNEL LINK	BIT NUMBER	RGB (LSB EXAMPLE)	DS92LV2421	DS90UR241	DS99R421	DS90C241
TXOUT0	Bit 6	G2	G2	DIN6	RXIN0	DIN6
	Bit 5	R7	R7	DIN5		DIN5
	Bit 4	R6	R6	DIN4		DIN4
	Bit 3	R5	R5	DIN3		DIN3
	Bit 2	R4	R4	DIN2		DIN2
	Bit 1	R3	R3	DIN1		DIN1
	Bit 0	R2	R2	DIN0		DIN0
N/A	N/A	N/A	N/A	DIN23 ⁽¹⁾	OS2 ⁽¹⁾	DIN23 ⁽¹⁾
				DIN22 ⁽¹⁾	OS1 ⁽¹⁾	DIN22 ⁽¹⁾
				DIN21 ⁽¹⁾	OS0 ⁽¹⁾	DIN21 ⁽¹⁾
DS92LV0422 SETTINGS	MAPSEL = 0		CONFIG[1:0] = 00	CONFIG[1:0] = 10		CONFIG[1:0] = 11

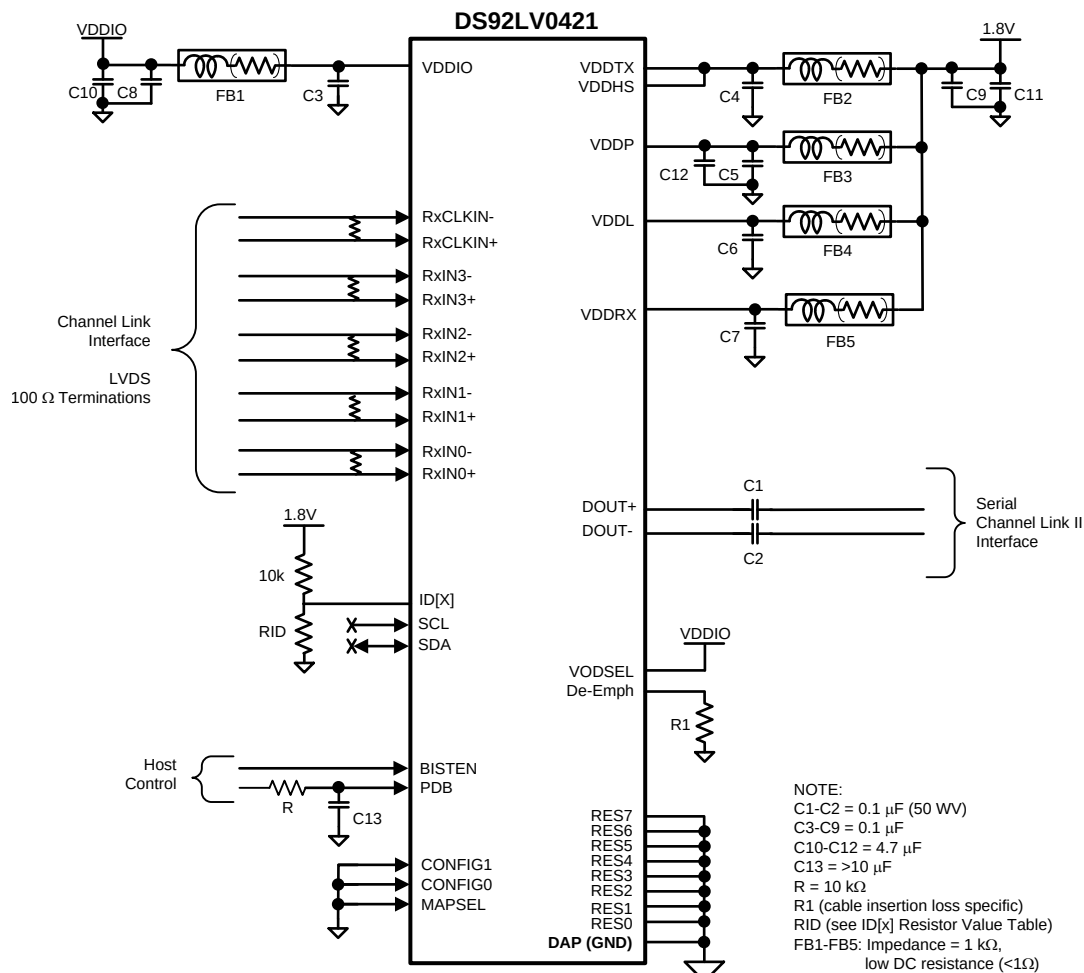
(1) These bits are not supported by the DS92LV0422.

8.2 Typical Application

8.2.1 DS92LV0421 Typical Connection

Figure 36 shows a typical application of the DS92LV0421 serializer in pin control mode for a 24-bit application. The LVDS inputs require external 100- Ω differential termination resistors. The CML outputs require 0.1- μ F, AC-coupling capacitors to the line. The line driver includes internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, four 0.1- μ F capacitors and a 4.7- μ F capacitor must be used for local device bypassing. Ferrite beads are placed on the power lines for effective noise suppression. System GPO (General Purpose Output) signals control the PDB and BISTEN pins. A delay cap is placed on the PDB signal to delay the enabling of the device until power is stable.

The application assumes connection to the companion deserializer (DS92LV0422), and therefore the configuration pins CONFIG[1:0] are also both tied low. In this example, the cable is long, and therefore the VODSEL pin is tied high and a De-Emphasis value is selected by the resistor R1. The interface to the host is with 1.8-V LVCMOS levels, thus the VDDIO pin is connected also to the 1.8-V rail. The optional serial bus control is not used in this example, thus the SCL, SDA and ID[X] pins can be left open.



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Figure 36. DS92LV0421 Typical Connection Diagram

Typical Application (continued)

8.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 16](#) as the input parameters.

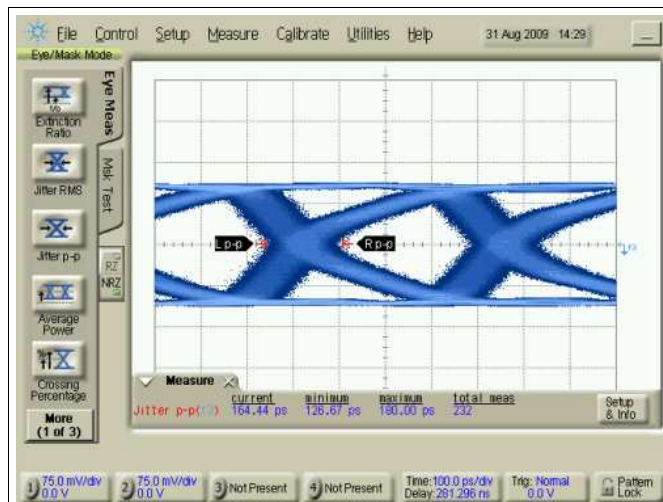
Table 16. Design Parameters

PARAMETER	VALUE
VDDIO	1.8 V or 3.3 V
VDDL, VDDP, VDDHS, VDDTX, VDDRX	1.8 V
AC Coupling Capacitor for DOUT±	100 nF

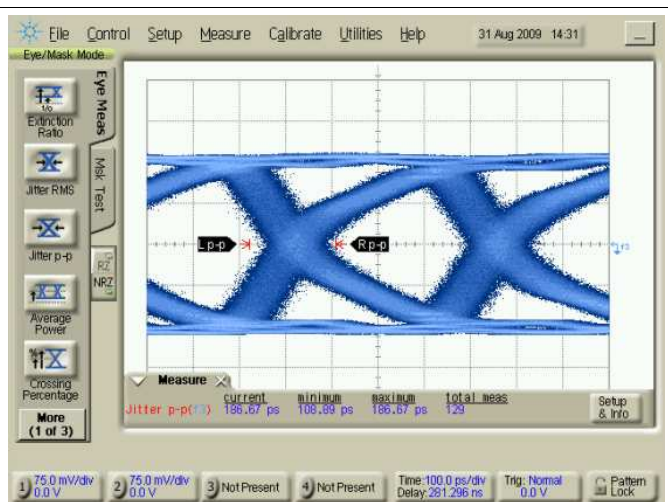
8.2.1.2 Detailed Design Procedure

The DOUT± outputs require 100-nF, AC-coupling capacitors to the line. Channel-Link data input pairs require an external 100-Ω termination for standard LVDS levels. The power supply filter capacitors are placed near the power supply pins. A smaller capacitance capacitor must be placed closer to the power supply pins. Adding a ferrite bead is optional, and if used, TI recommends using a ferrite bead with 1-kΩ impedance and low DC resistance (less than 1 Ω). The VODSEL pin is tied to VDDIO for long cable applications. The de-emphasis pin may connect a resistor to Ground (see [Table 2](#)). The PDB and BISTEN pins are assumed to be controlled by a microprocessor. The PDB must remain in a low state until all power supply voltages reach the final voltage. The CONFIG[1:0] pins are set depending on operating modes and backward compatibility (see [Table 10](#)). The MAPSEL pin sets the mapping scheme (see [Figure 23](#) and [Figure 24](#)). The SCL, SDA, and ID[X] pins can be left open when these serial bus control pins are unused. The RES[7:0] pins and DAP must be tied to Ground.

8.2.1.3 Application Curves



**Figure 37. Serializer CML Output Stream,
RXCLKIN = 65 MHz, VODSEL = L**

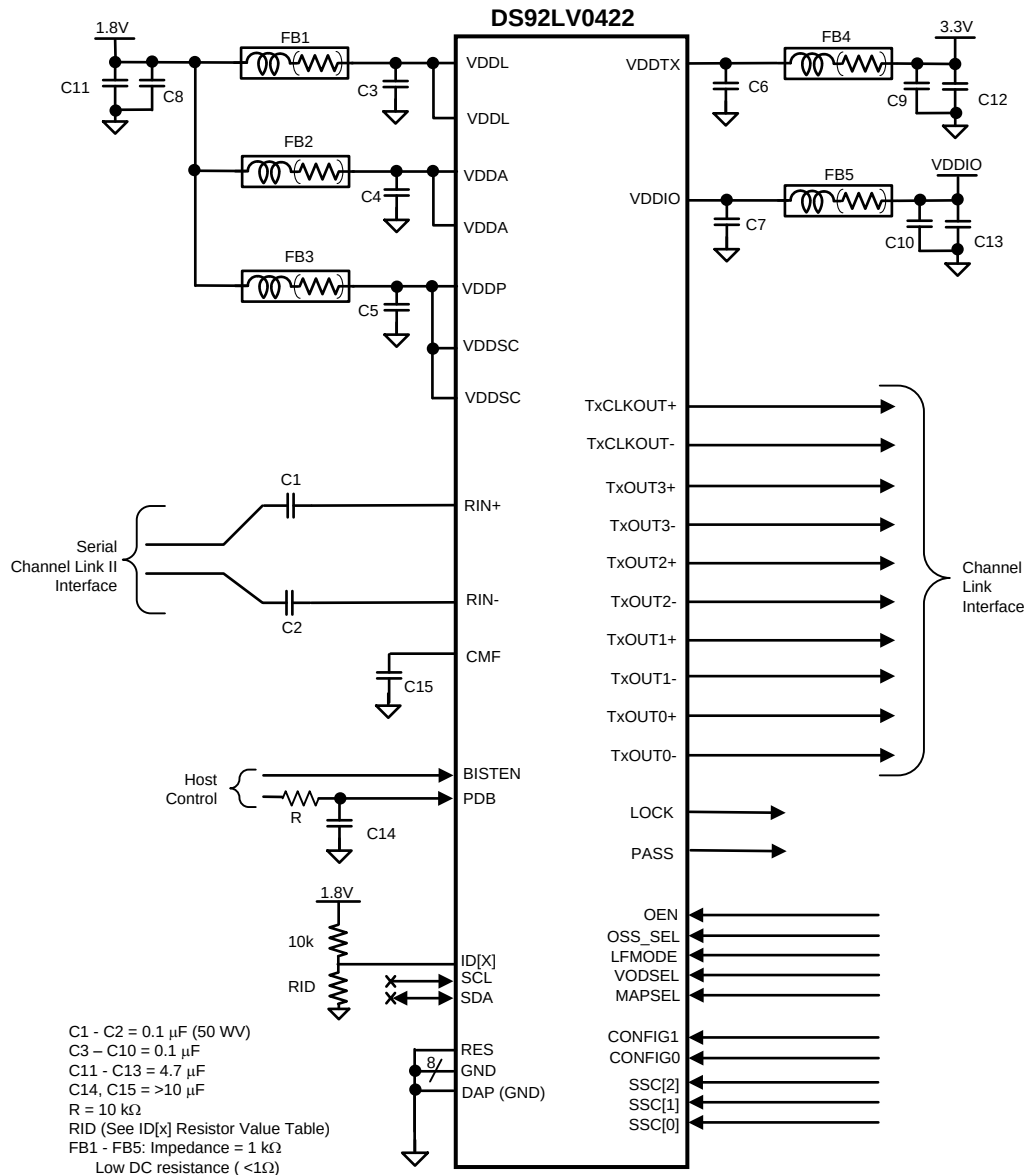


**Figure 38. Serializer CML Output Stream,
RXCLKIN = 65 MHz, VODSEL = H**

8.2.2 DS92LV0422 Typical Application

Figure 39 shows a typical application of the DS92LV0422 for a 24-bit application. The CML inputs require 0.1- μ F, AC-coupling capacitors to the line, and the receiver provides internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, four 0.1- μ F capacitors and a 4.7- μ F capacitor must be used for local device bypassing. Ferrite beads are placed on the power lines for effective noise suppression. System GPO (General Purpose Output) signals control the PDB and BISTEN pins. A delay cap is placed on the PDB signal to delay the enabling of the device until power is stable.

The application assumes connection to the companion serializer (DS92LV0421), and therefore the configuration pins CONFIG[1:0] are also both tied low. The interface to the host is with 1.8-V LVCMOS levels, thus the VDDIO pin is connected also to the 1.8-V rail. The optional serial bus control is not used in this example, thus the SCL, SDA, and ID[X] pins can be left open.



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Figure 39. DS92LV0422 Typical Connection Diagram

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 17 as the input parameters.

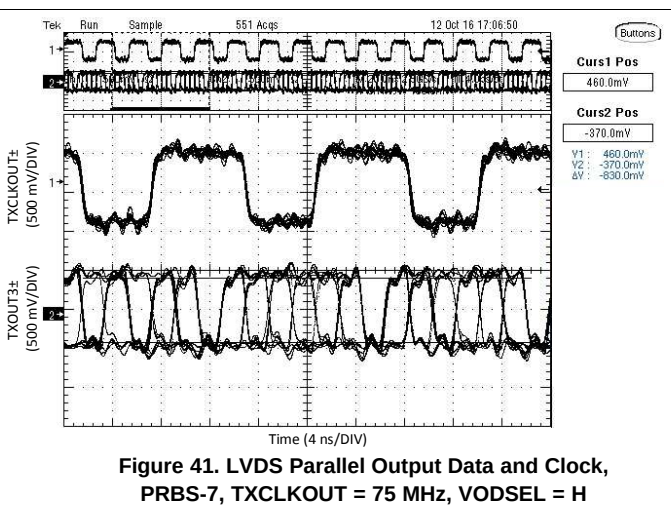
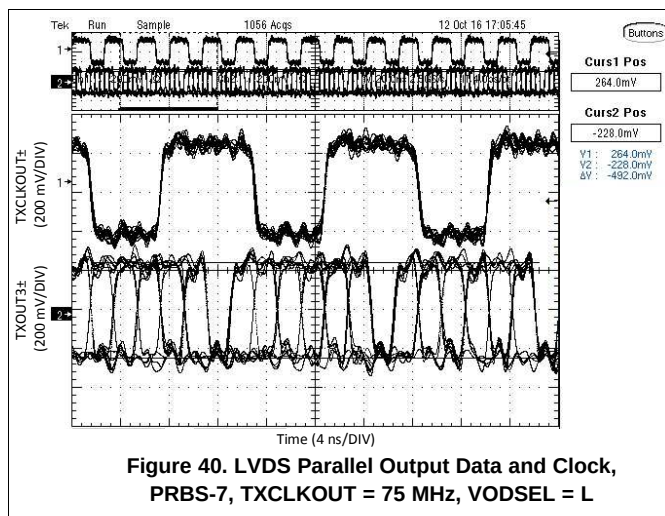
Table 17. Design Parameters

PARAMETER	VALUE
VDDIO	1.8 V or 3.3 V
VDDL, VDDP, VDDSC, VDDA	1.8 V
VDDTX	3.3 V
AC Coupling Capacitor for RIN±	100 nF

8.2.2.2 Detailed Design Procedure

The RIN± inputs require 100-nF, AC-coupling capacitors to the line. The power supply filter capacitors are placed near the power supply pins. A smaller capacitance capacitor must be placed closer to the power supply pins. The device has one configuration pin (EQ) called a strap pin, which is pulled down by default. For a high state, use a 10-kΩ resistor pullup to VDDIO. The PDB and BISTEN pins are assumed to be controlled by a microprocessor. The PDB must remain in a low state until all power supply voltages reach the final voltage. The SCL, SDA, and ID[X] pins can be left open when these serial bus control pins are unused. The RES pin and DAP must be tied to Ground.

8.2.2.3 Application Curves



9 Power Supply Recommendations

The VDD (V_{DDn} and V_{DDIO}) supply ramp must be faster than 1.5 ms with a monotonic rise. If slower than 1.5 ms, a capacitor on the PDB pin is required to ensure PDB arrives after all the VDD supplies have settled to the recommended operating voltage. When the PDB pin is pulled to V_{DDIO}, TI recommends using a 10-kΩ pullup and a 22-μF cap to Ground to delay the PDB input signal.

10 Layout

10.1 Layout Guidelines

Circuit board layout and stack-up for the LVDS serializer and deserializer devices must be designed to provide low-noise power feed to the device. Good layout practice also separates high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback, and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power or ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies and makes the value and placement of external bypass capacitors less critical. External bypass capacitors must include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 μF to 0.1 μF . Tantalum capacitors may be in the 2.2- μF to 10- μF range. Voltage rating of the tantalum capacitors must be at least 5x the power supply voltage being used.

Surface-mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, place the smaller value closer to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50- μF to 100- μF range and smooths low frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane, with vias on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four-layer board with a power and ground plane. Place LVCMOS signals away from the CML lines to prevent coupling from the LVCMOS lines to the CML lines. Closely-coupled differential lines of 100 Ω are typically recommended for LVDS interconnects. The closely coupled lines help to ensure that coupled noise appears as common mode and thus is rejected by the receivers. The tightly coupled lines also radiate less.

10.1.1 WQFN (LLP) Stencil Guidelines

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the LLP (WQFN) package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown in [Figure 42](#) and [Figure 43](#).

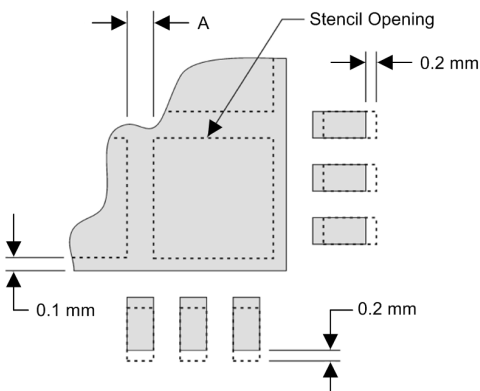
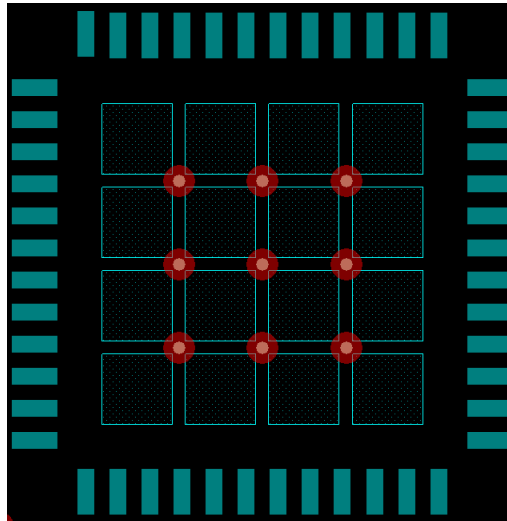


Figure 42. No Pullback LLP, Single Row Reference Diagram

Layout Guidelines (continued)

Table 18. No Pullback LLP Stencil Aperture Summary for DS92LV0421 and DS92LV0422

DEVICE	PIN COUNT	MKT DWG	PCB I/O PAD SIZE (mm)	PCB PITCH (mm)	PCB DAP SIZE (mm)	STENCIL I/O APERTURE (mm)	STENCIL DAP APERTURE (mm)	NUMBER OF DAP APERTURE OPENINGS	GAP BETWEEN DAP APERTURE (Dim A mm)
DS92LV0421	36	SQA36A	0.25 × 0.6	0.5	4.6 × 4.6	0.25 × 0.7	1.0 × 1.0	16	0.2
DS92LV0422	48	SQA48A	0.25 × 0.6	0.5	5.1 × 5.1	0.25 × 0.7	1.1 × 1.1	16	0.2


Figure 43. 48-Pin WQFN Stencil Example of Via and Opening Placement

Information on the WQFN style package is provided in [Leadless Leadframe Package \(LLP\) Application Report \(SNOA401\)](#).

10.1.2 Transmission Media

The serializer and deserializer chipset is intended to be used in a point-to-point configuration through a PCB trace or through twisted pair cable. The serializer and deserializer provide internal terminations for a clean signaling environment. The interconnect for LVDS must present a differential impedance of 100 Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Shielded or unshielded cables may be used depending upon the noise environment and application requirements.

10.1.3 LVDS Interconnect Guidelines

See [AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines](#) (SNLA008) and [AN-905 Transmission Line RAPIDESIGNER Operation and Applications Guide](#) (SNLA035) for full details.

- Use 100-Ω coupled differential pairs
- Use the S, 2S, 3S rule in spacings
 - S = space between the pair
 - 2S = space between pairs
 - 3S = space to LVCMOS signal
- Minimize the number of vias
- Use differential connectors when operating above 500-Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the Tx outputs and Rx inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual, available in PDF format from the TI website at: www.ti.com/lvds.

10.2 Layout Example

The following PCB layout examples are derived from the layout design of the LV04EVK01 Evaluation Module. These graphics and additional layout description are used to demonstrate both proper routing and proper solder techniques when designing in the serializer and deserializer pair.

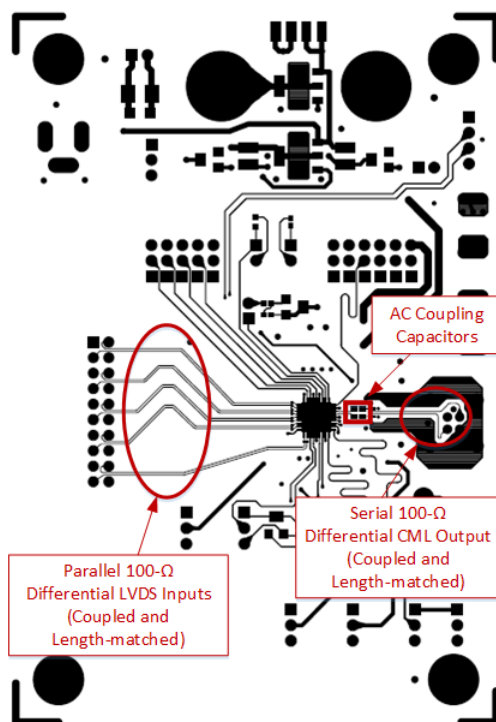


Figure 44. DS92LV0421 Serializer Example Layout

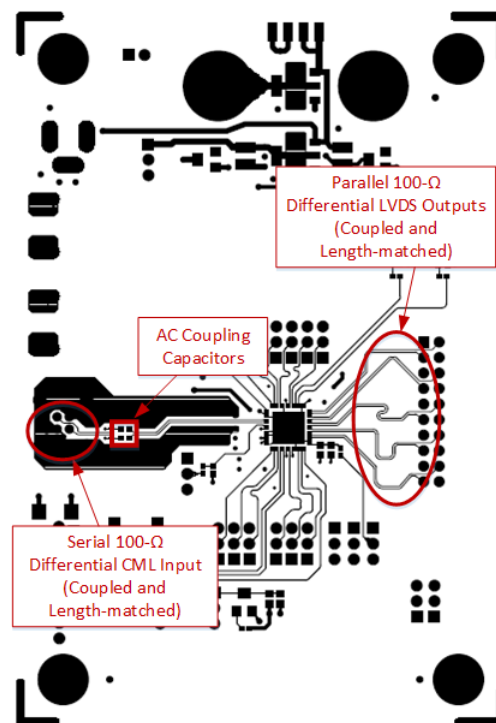


Figure 45. DS92LV0422 Deserializer Example Layout

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

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11.1.2 開発サポート

開発サポートについては、以下を参照してください。

[LVDS/M-LVDS/ECL/CMLの概要](#)

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- 『ハンダ付けの絶対最大定格』(SNOA549)
- 『リードレス・リードフレーム・パッケージ(LLP)』アプリケーション・レポート(SNOA401)
- 『AN-1108チャンネル・リンクPCBと相互接続デザイン・インのガイドライン』(SNLA008)
- 『AN-905転送ラインRAPIDESIGNER操作およびアプリケーション・ガイド』(SNLA035)

11.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 19. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
DS92LV0421	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DS92LV0422	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

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11.8 用語集

SLYZ022 — TI用語集.

この用語集には、用語や略語の一覧および定義が記載されています。

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS92LV0421SQ/NOPB	Active	Production	WQFN (NJK) 36	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0421
DS92LV0421SQ/NOPB.A	Active	Production	WQFN (NJK) 36	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0421
DS92LV0421SQE/NOPB	Active	Production	WQFN (NJK) 36	250 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0421
DS92LV0421SQE/NOPB.A	Active	Production	WQFN (NJK) 36	250 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0421
DS92LV0421SQX/NOPB	Active	Production	WQFN (NJK) 36	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0421
DS92LV0421SQX/NOPB.A	Active	Production	WQFN (NJK) 36	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0421
DS92LV0422SQ/NOPB	Active	Production	WQFN (RHS) 48	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0422
DS92LV0422SQ/NOPB.A	Active	Production	WQFN (RHS) 48	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0422
DS92LV0422SQE/NOPB	Active	Production	WQFN (RHS) 48	250 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0422
DS92LV0422SQE/NOPB.A	Active	Production	WQFN (RHS) 48	250 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0422
DS92LV0422SQX/NOPB	Active	Production	WQFN (RHS) 48	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0422
DS92LV0422SQX/NOPB.A	Active	Production	WQFN (RHS) 48	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0422

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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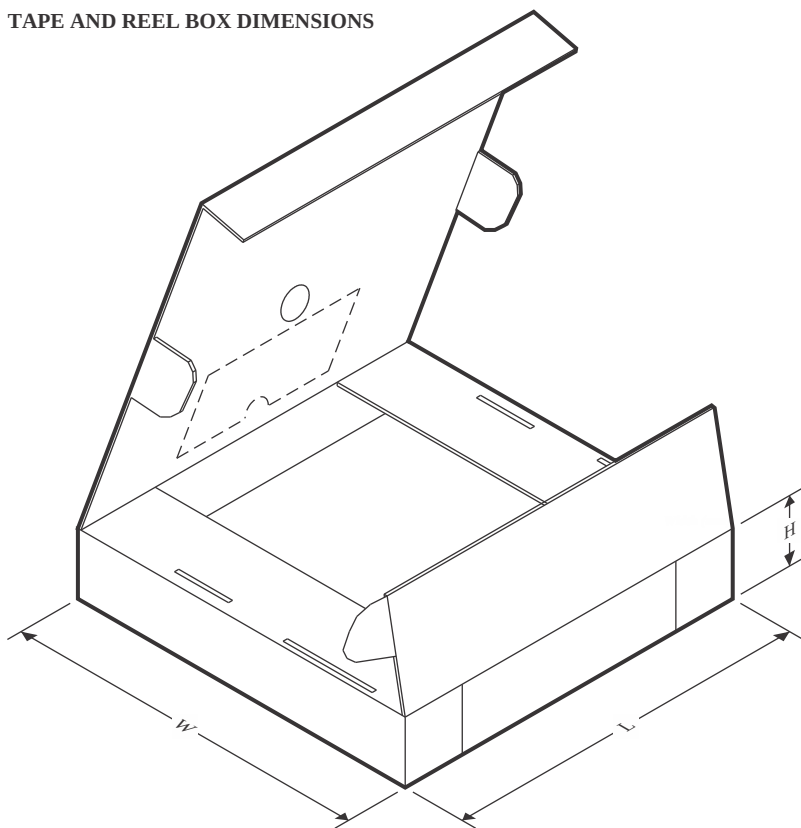
TAPE AND REEL INFORMATION



*All dimensions are nominal

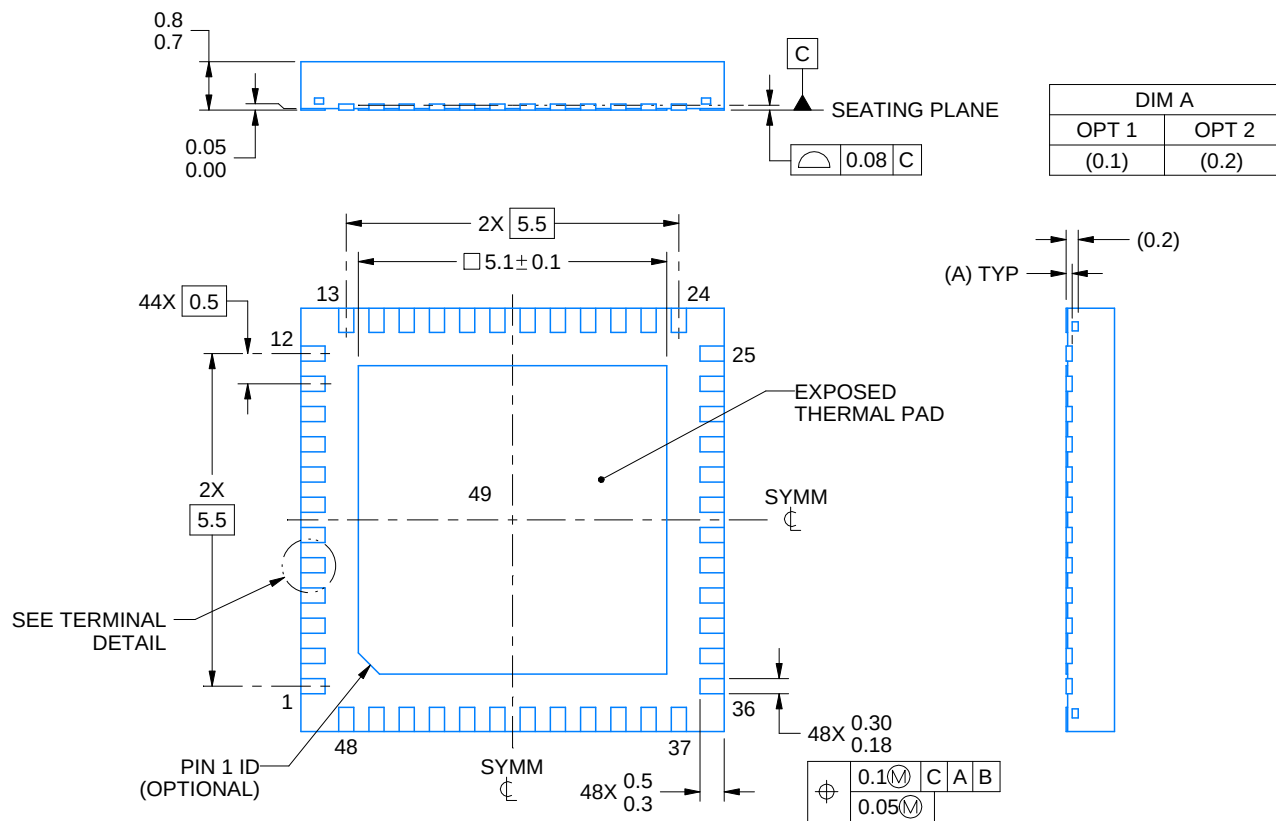
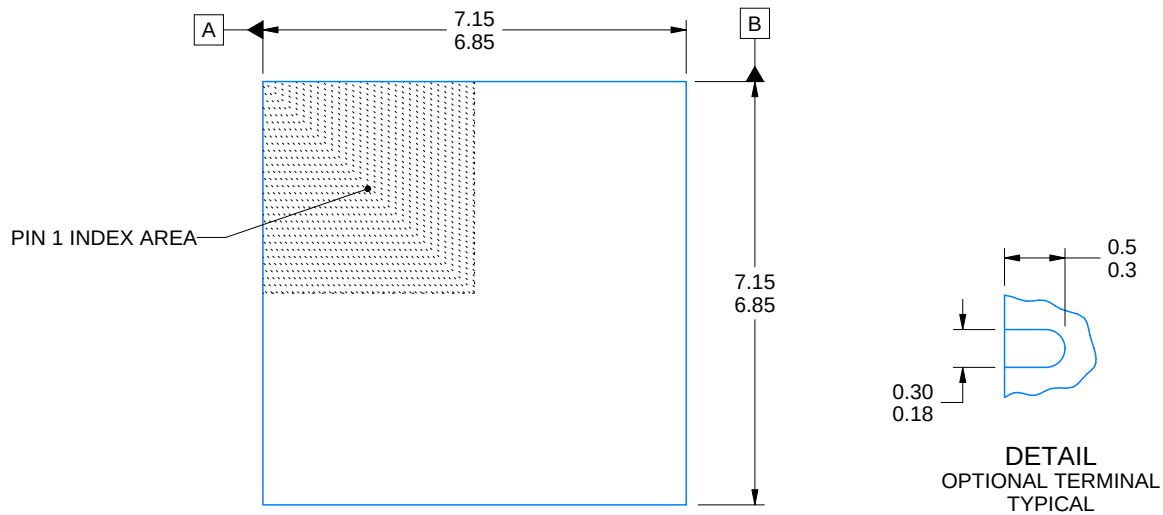
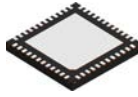
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS92LV0421SQ/NOPB	WQFN	NJK	36	1000	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS92LV0421SQE/NOPB	WQFN	NJK	36	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS92LV0421SQX/NOPB	WQFN	NJK	36	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS92LV0422SQ/NOPB	WQFN	RHS	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS92LV0422SQE/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS92LV0422SQX/NOPB	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS92LV0421SQ/NOPB	WQFN	NJK	36	1000	356.0	356.0	36.0
DS92LV0421SQE/NOPB	WQFN	NJK	36	250	208.0	191.0	35.0
DS92LV0421SQX/NOPB	WQFN	NJK	36	2500	356.0	356.0	36.0
DS92LV0422SQ/NOPB	WQFN	RHS	48	1000	356.0	356.0	36.0
DS92LV0422SQE/NOPB	WQFN	RHS	48	250	208.0	191.0	35.0
DS92LV0422SQX/NOPB	WQFN	RHS	48	2500	356.0	356.0	36.0



4214990/B 04/2018

NOTES:

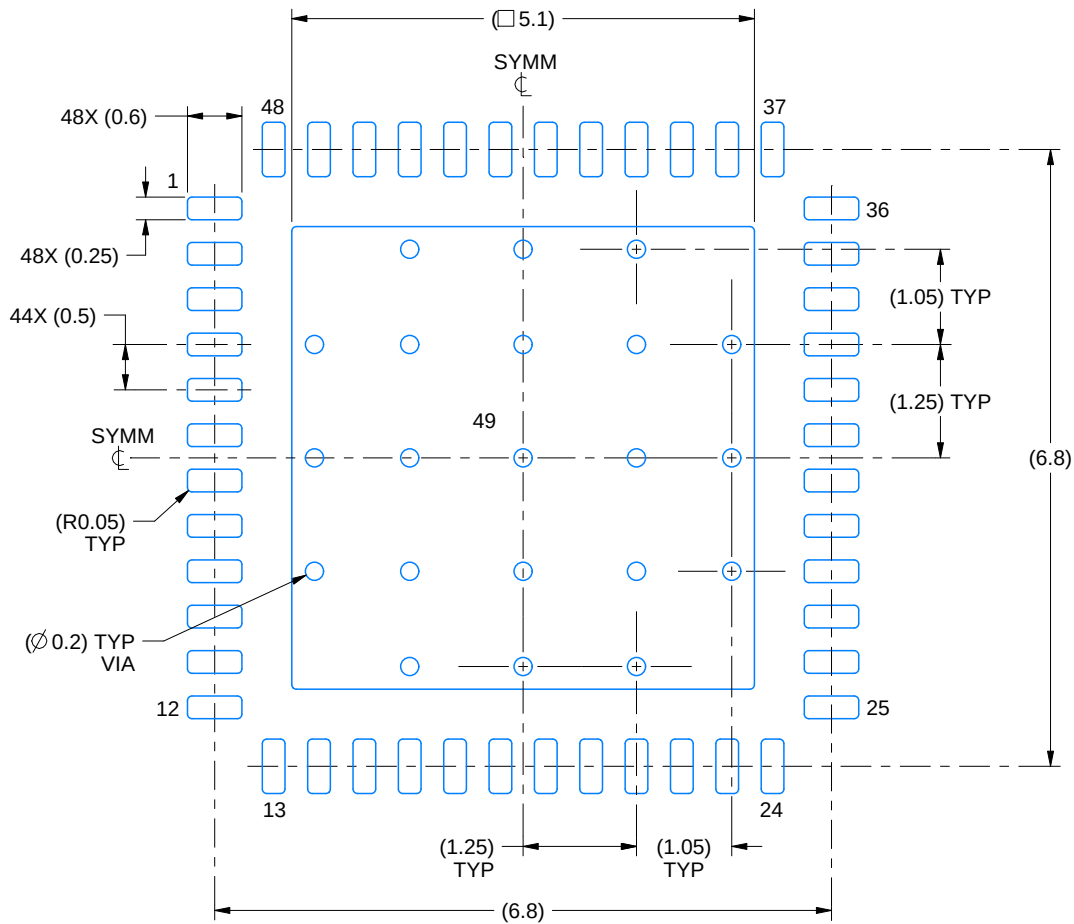
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

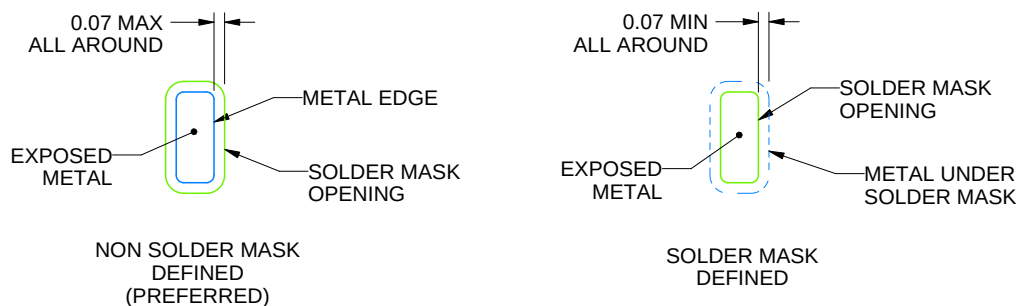
RHS0048A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

4214990/B 04/2018

NOTES: (continued)

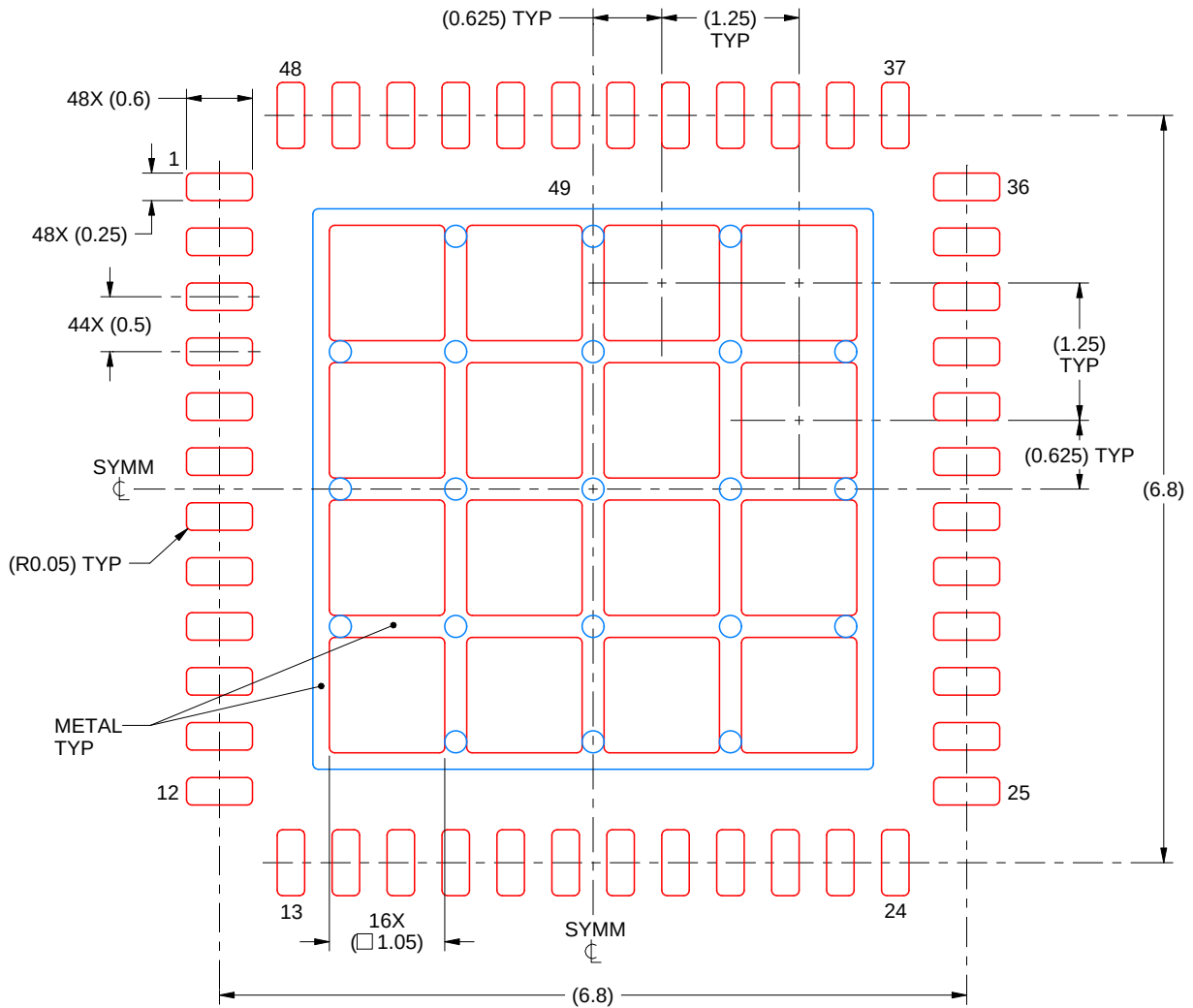
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHS0048A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

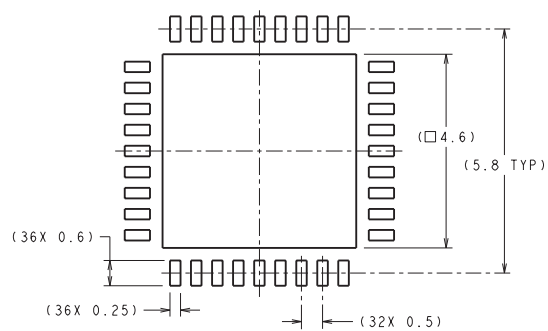
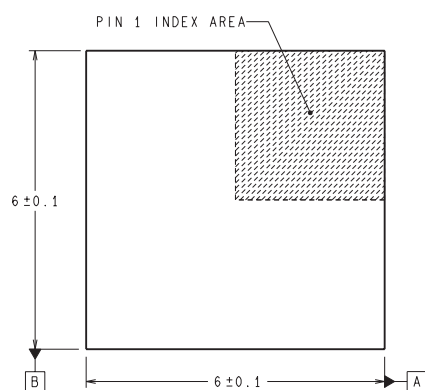
EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4214990/B 04/2018

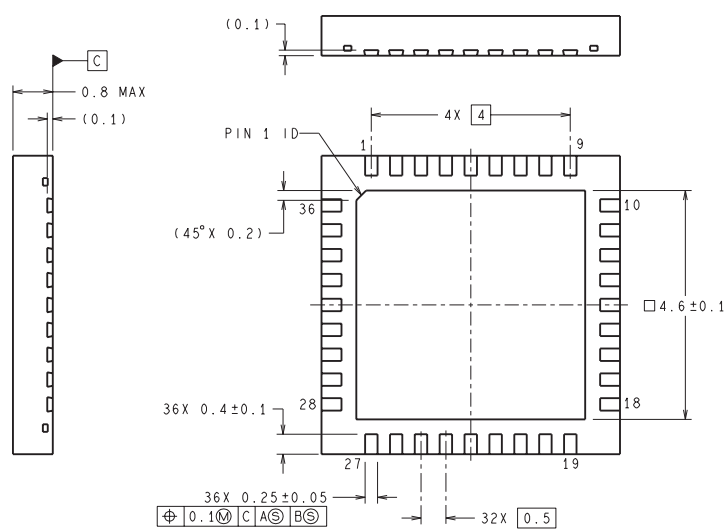
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

NJK0036A

**RECOMMENDED LAND PATTERN**

DIMENSIONS ARE IN MILLIMETERS
 DIMENSIONS IN () FOR REFERENCE ONLY



SQA36A (Rev A)

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