# DS90LVRA2-Q1 車載対応、LVDS デュアル差動ライン レシーバ

## 1 特長

- 車載アプリケーション向けに AEC-Q100 および AEC-Q006 認定済み
  - 温度グレード 2:-40℃～+105℃
- 600Mbps (300MHz) のスイッチング レート
- 50ps の差動スキュー (標準値)
- 0.1ns のチャネル間スキュー (標準値)
- 1.8V～3.3V の電源に対応
- フロースルーのピン配置
- 電源オフ時に高インピーダンスになる LVDS 入力
- 出力スルーレート制御
- LVDS 入力は LVDS/CML/LVPECL 信号に対応
- ANSI/TIA/EIA-644 規格に準拠
- DS90LV028A-Q1 とピン互換

## 2 アプリケーション

- 車載用インフォテインメントおよびクラスタ
- 車載ヘッド ユニット

## 3 概要

DS90LVRA2-Q1 は、デュアル CMOS 差動ライン レシーバであり、広い入力同相範囲、高いデータ レート、スルーレート制御付き CMOS 出力を必要とするアプリケーション向けに設計されています。このデバイスは、低電圧差動信号 (LVDS) テクノロジを活用して、600Mbps (300MHz) のデータ速度をサポートするよう設計されています。

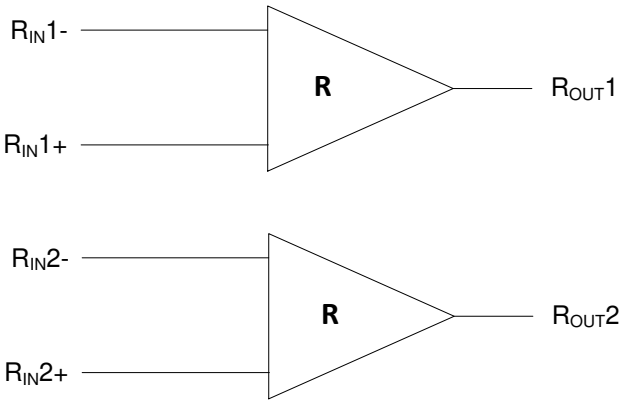
DS90LVRA2-Q1 は、低電圧 (標準値 350mV) の差動入力信号を受信し、電源電圧に応じて 1.8V から 3.3V CMOS 出力レベルへ変換します。DS90LVRA2-Q1 は、フロースルー設計を採用しており、PCB レイアウトが容易です。

DS90LVRA2-Q1 およびこれと対になる LVDS ライン ドライバ DS90LV027AQ は、消費電力の大きい PECL/ECL デバイスの新しい代替品として、高速のポイント ツー ポイント インターフェイス アプリケーションに使用できます。

**パッケージ情報**

| 部品番号 | パッケージ(1) | パッケージ サイズ(2) |
|---|---|---|
| DS90LVRA2-Q1 | DEM (WSON、8) | 2mm × 2mm |

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値で、該当する場合はピンも含まれます。




**機能図**

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# 4 Pin Configuration and Functions

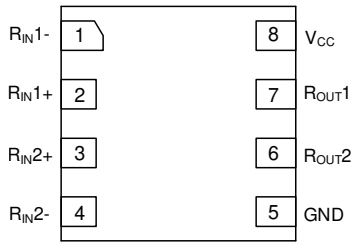



**図 4-1. DEM Package, WSON 8 Pin (Top View)**

**表 4-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND | 5 | G | Ground pin |
| $R_{IN}1-$ | 1 | I | Inverting receiver input pin |
| $R_{IN}2-$ | 4 | I | |
| $R_{IN}1+$ | 2 | I | Non-inverting receiver input pin |
| $R_{IN}2+$ | 3 | I | |
| $R_{OUT}2$ | 6 | O | Receiver output pin |
| $R_{OUT}1$ | 7 | O | |
| $V_{CC}$ | 8 | P | Power supply pin |

(1) I = input, O = output, G = ground

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage ($V_{CC}$) | | –0.3 | 4 | V |
| Input Voltage ($R_{IN}$+, $R_{IN}$–) | | –5 | 6 | V |
| Differential Voltage ($R_{IN}$+ - $R_{IN}$–) for LVDS | | 0 | 3 | V |
| Output Voltage ($R_{OUT}$) | | –0.3 | 3.6 | V |
| Lead Temperature Range Soldering | (4 sec.) | | 260 | °C |
| Maximum Junction Temperature | | | 135 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011(2) | ±1000 | |

(1) AEC Q100-002 HBM ESD Classification Level 2
(2) AEC Q100- 011 CDM ESD Classification Level C4A

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage (3.3V mode) | 3.0 | 3.3 | 3.6 | V |
| $V_{CC}$ | Supply voltage (2.5V mode) | 2.25 | 2.5 | 2.75 | V |
| $V_{CC}$ | Supply voltage (1.8V mode) | 1.62 | 1.80 | 1.98 | V |
| $V_R$ | Receiver input voltage (LVDS) | 0 | | 3.0 | V |
| $T_A$ | Operating free-air temperature | -40 | | 105 | °C |
| $T_{PCB}$ | PCB temperature (1mm away from device) | | | 112 | °C |
| $T_J$ | Junction temperature | | | 125 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | DEM (WSON) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 143.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 77.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 69.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 5.0 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 69.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{ITH}$ | Differential input high threshold | $V_{IB}$ = -4 V or 5V, $V_{CC}$ = 1.62 V to 3.6 V | | | 100 | mV |
| $V_{ITL}$ | Differential input low threshold | | -100 | | | |
| $V_{HYS}$ | Differential input voltage hysteresis, $V_{IT1} – V_{IT2}$ | $V_{CC}$ = 1.62 V to 3.6 V | 20 | 40 | 120 | mV |
| $V_{CM\_RANGE}$ | Input common mode voltage range | $V_{CC}$ = 1.62 - 1.98V | -1 | 1.2 | 2 | V |
| | | $V_{CC}$ = 2.3 - 2.7 V | -2.5 | 1.2 | 3 | V |
| | | $V_{CC}$ = 3.0 - 3.6 V | -4 | 1.2 | 5 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –4mA, $V_{CC}$ = 1.8V ± 10% | 1.3 | | | V |
| | | $I_{OH}$ = –4mA, $V_{CC}$ = 2.5V ± 10% | 1.8 | | | V |
| | | $I_{OH}$ = –4mA, $V_{CC}$ = 3.3V ± 10% | 2.6 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4mA, $V_{CC}$ = 1.8V ± 10% | | | 0.2 | V |
| | | $I_{OL}$ = 4mA, $V_{CC}$ = 2.5V ± 10% | | | 0.3 | V |
| | | $I_{OL}$ = 4mA, $V_{CC}$ = 3.3V ± 10% | | | 0.4 | V |
| $I_{CC\_ACTIVE}$ | Supply current | $V_{CC}$ = 3.6 V, No load, Steady-state, $V_{ID}$=200mV/-200mV | | | 25 | mA |
| | | $V_{CC}$ = 2.7 V, No load, Steady-state, $V_{ID}$=200mV/-200mV | | | 25 | mA |
| | | $V_{CC}$ = 1.98V, No load, Steady-state, $V_{ID}$=200mV/-200mV | | | 25 | mA |
| $I_I$ | Input current (A or B inputs) | $V_I$ = -1.0 V, Other input open | | | ±35 | µA |
| | | $V_I$ = 2.4 V, Other input open | | | ±20 | µA |
| | | $V_I$ = –4 V, Other input open (split between 85℃) (±80 µA) | | | ±120 | µA |
| | | $V_I$ = 5V, Other input open | | | ±40 | µA |
| $I_{I(OFF)}$ | Power-off output current (Y or Z outputs) | $V_Y$ or $V_Z$ = 1.98V, $V_{CC}$ = 0 V | | | ±20 | µA |
| $I_{I(OFF)}$ | Power-off input current (A or B inputs) | $V_A$ or $V_B$ = -1 V or 2.0 V, $V_{CC}$ = 0 V | | | ±30 | µA |
| | | $V_A$ or $V_B$ = –4 or 5V, $V_{CC}$ = 0 V | | | ±70 | µA |
| | | $V_A$ or $V_B$ = 0 V or 2.4 V, $V_{CC}$ = 0 V | | | ±30 | µA |

## 5.6 Switching Characteristics

$V_{ID}$ = 200mV, $C_L$ = 10pF and over operating temperature ranges, unless otherwise specified. (1) (2)

| Symbol | Parameter | Conditions | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PHLD}$ | Differential Propagation Delay High to Low | $V_{CC}$ = 1.8V ± 10%, trf = 1ns | 2.5 | 4.4 | 7.7 | ns |
| | | $V_{CC}$ = 2.5V ± 10%, trf = 1ns | 2.2 | 3.3 | 5.1 | ns |
| | | $V_{CC}$ = 3.3V ± 10%, trf = 1ns | 1.9 | 2.9 | 4.1 | ns |
| $t_{PLHD}$ | Differential Propagation Delay Low to High | $V_{CC}$ = 1.8V ± 10%, trf = 1ns | 2.7 | 4.4 | 7.7 | ns |
| | | $V_{CC}$ = 2.5V ± 10%, trf = 1ns | 2.4 | 3.4 | 5.1 | ns |
| | | $V_{CC}$ = 3.3V ± 10%, trf = 1ns | 2.2 | 3.1 | 4.1 | ns |
| $t_{SKD1\_S}$ | Differential Pulse Skew ($t_{PHLD}$ – $t_{PLHD}$) (3) | $V_{CC}$ = 1.8V ± 10%, trf = 1ns | -680 | | 680 | ps |
| | | $V_{CC}$ = 2.5V ± 10%, trf = 1ns | -500 | | 500 | ps |
| | | $V_{CC}$ = 3.3V ± 10%, trf = 1ns | -610 | | 610 | ps |
| $t_{SKD1\_400M}$ | Differential Pulse Skew ($t_{PHLD}$ – $t_{PLHD}$ )(3) | $V_{CC}$ = 1.8V ± 10%, trf = 0.25ns, 400Mbps | -1990 | | 1990 | ps |
| | | $V_{CC}$ = 2.5V ± 10%, trf = 0.25ns, 400Mbps | -1400 | | 1400 | ps |
| | | $V_{CC}$ = 3.3V ± 10%, trf = 0.25ns, 400Mbps | -1800 | | 1800 | ps |
| $t_{SKD2}$ | Differential Channel-to-Channel Skew (4) | $V_{CC}$ = 1.8V ± 10%, trf = 0.25ns | | | 0.6 | ns |
| | | $V_{CC}$ = 2.5V ± 10%, trf = 0.25ns | | | 0.3 | ns |
| | | $V_{CC}$ = 3.3V ± 10%, trf = 0.25ns | | | 0.3 | ns |
| $t_{SKD3}$ | Differential Part to Part Skew (5) | $V_{CC}$ = 1.8V ± 10%, trf = 0.25ns | | | 3.0 | ns |
| | | $V_{CC}$ = 2.5V ± 10%, trf = 0.25ns | | | 1.7 | ns |
| | | $V_{CC}$ = 3.3V ± 10%, trf = 0.25ns | | | 1.2 | ns |
| $t_R$ | Rise Time | $V_{CC}$ = 1.8V | 250 | 500 | 740 | ps |
| | | $V_{CC}$ = 2.5V | 250 | 390 | 740 | ps |
| | | $V_{CC}$ = 3.3V | 250 | 450 | 740 | ps |
| $t_F$ | Fall Time | $V_{CC}$ = 1.8V | 250 | 560 | 740 | ps |
| | | $V_{CC}$ = 2.5V | 250 | 360 | 740 | ps |
| | | $V_{CC}$ = 3.3V | 250 | 400 | 740 | ps |
| $f_{MAX}$ | Maximum Operating Frequency (11) | | 300 | | | MHz |

(1) $C_L$ includes probe and jig capacitance.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, $Z_O$ = 50Ω, $t_r$ and $t_f$ (0% to 100%) ≤ 3ns for $R_{IN}$.
(3) $t_{SKD1}$ is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of the same channel.
(4) $t_{SKD2}$ is the differential channel-to-channel skew of any event on the same device. This specification applies to devices having multiple receivers within the integrated circuit.
(5) $t_{SKD3}$, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same $V_{CC}$ and within 5°C of each other within the operating temperature range.
(6) $f_{MAX}$ generator input conditions: $t_r$ = $t_f$ < 1ns (0% to 100%), 50% duty cycle, differential (1.05V to 1.35 peak to peak). Output criteria: 60%/40% duty cycle, $V_{OL}$ (max), $V_{OH}$ (min), load = 15pF (stray plus probes).

## 5.7 Typical Characteristics

$T_A$ = 25°C, Load = 5pF (unless otherwise notes)

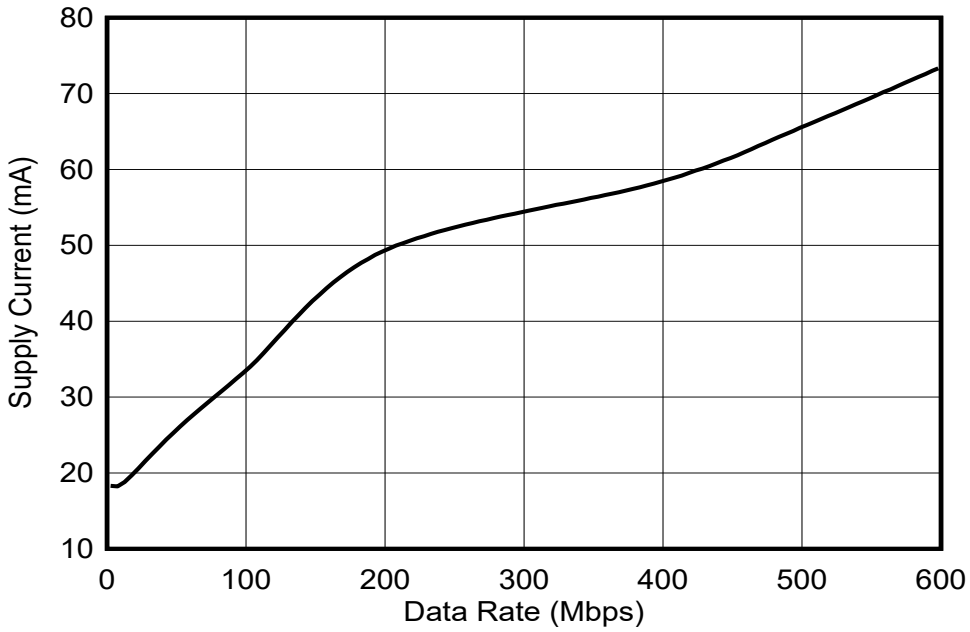



**図 5-1. Power Supply Current vs Data Rate ($V_{CC}$ = 1.8V, 2 Channels)**

# 6 Parameter Measurement Information

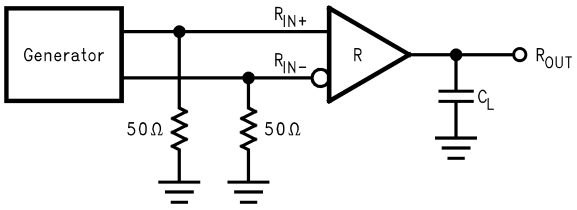



**図 6-1. Receiver Propagation Delay and Transition Time Test Circuit**

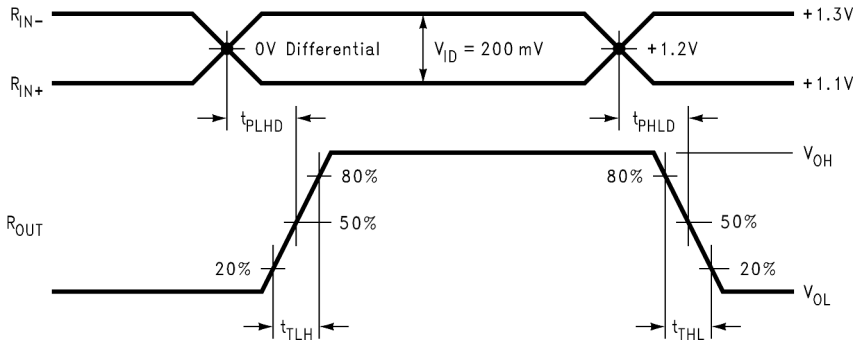


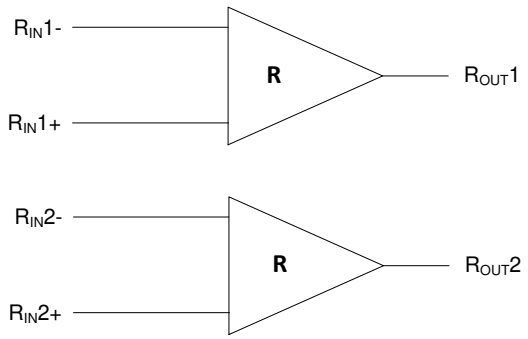

**図 6-2. Receiver Propagation Delay and Transition Time Waveforms**

# 7 Detailed Description

## 7.1 Overview

図 8-1 shows how LVDS drivers and receivers are intended to be used primarily in a simple point-to-point configuration. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the source through a impedance controlled 100Ω differential PCB traces. Use a termination resistor of 100Ω and place it as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

The DS90LVRA2-Q1 differential line receiver is capable of detecting signals as low as 100mV over a common-mode range of −4V to 5V ($V_{CC}$ at 3.3V). The common voltage range is related to the LVDS driver offset voltage, which is typically +1.2V. The differential signal from the LVDS driver is centered around the +1.2V offset voltage and may shift around this center point. The shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of +0V to +3V (measured from each pin to ground).

## 7.4 Device Functional Modes

**表 7-1. Truth Table**

| INPUTS(1) | OUTPUT |
|---|---|
| $V_{ID} \geq 100mV$ | H |
| $V_{ID} \leq -100mV$ | L |
| $-100mV \leq V_{ID} \leq 100mV$ | Undetermined |

(1) $V_{ID} = [R_{IN}+] - [R_{IN}-]$

# 8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

For general application guidelines and hints about LVDS drivers and receivers, refer to the *LVDS application notes and design guides*.

## 8.2 Typical Application

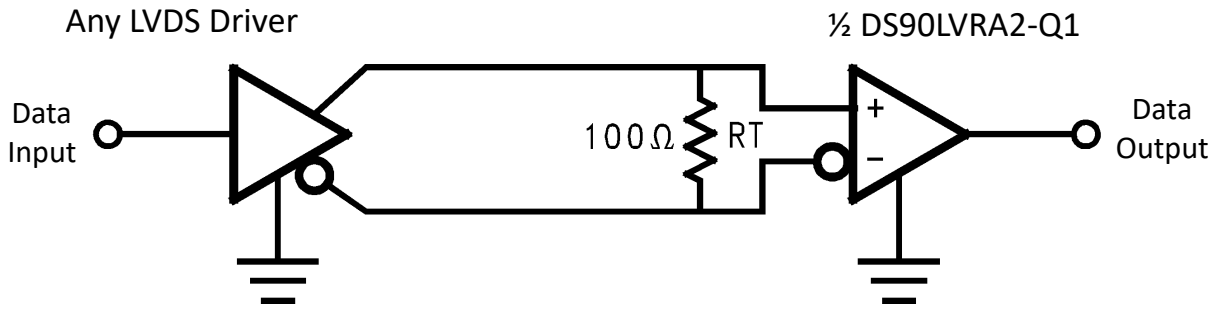



**図 8-1. Balanced System Point-to-Point Application**

### 8.2.1 Design Requirements

When using LVDS devices, it is important to specify controlled impedance PCB traces. All components of the transmission media must have a matched differential impedance of 100Ω and must not introduce major impedance discontinuities.

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Power Decoupling Recommendations*

Bypass capacitors must be used on power pins. It is recommended to use surface mount high frequency ceramic 0.1µF and 0.01µF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10µF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

#### *8.2.2.2 Termination*

Use a termination resistor that best matches the differential impedance or the transmission line. The resistor should be between 90Ω and 110Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work correctly without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice. Surface mount 1% resistors are the best

PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10mm (12mm maximum).

#### 8.2.2.3 Input Failsafe Biasing

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to $V_{DD}$ through a pull up resistor and ties the negative LVDS input pin to GND by a pull down resistor. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. Set the common-mode bias point to approximately 1.2V so that it is compatible with the internal circuitry. For more information, refer to application note AN-1194 *Failsafe Biasing of LVDS Interfaces*.

#### 8.2.2.4 Probing LVDS Transmission Lines

Always use high impedance (> 100kΩ), low capacitance (< 2pF) scope probes with a wide bandwidth (1GHz) scope. Improper probing will give deceiving results.

### 8.2.3 Application Curves

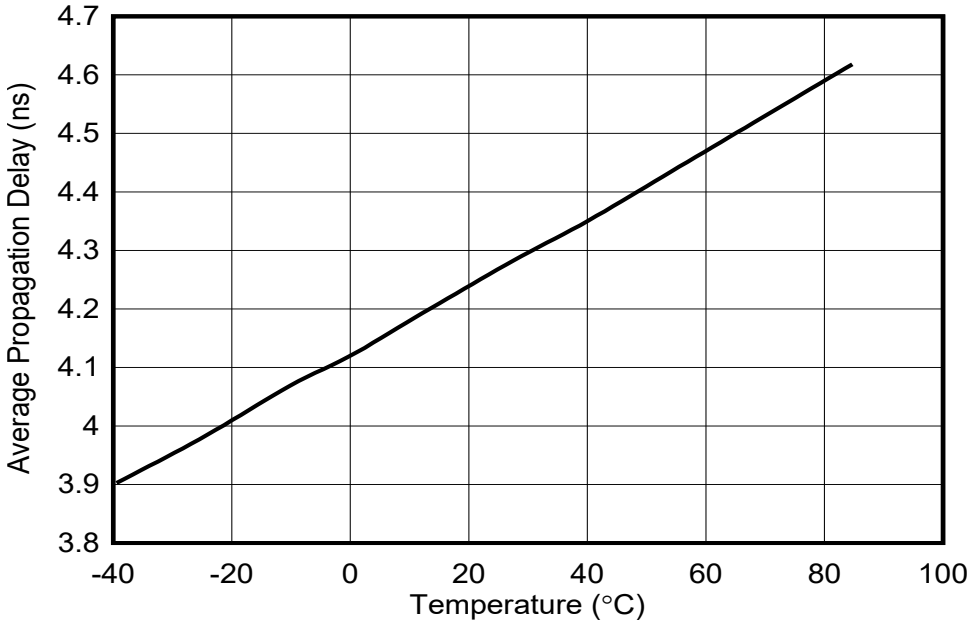



**図 8-2. Propagation Delay vs Temperature ($V_{CC}$ = 1.8V, Load = 10pF, Average of 2 Channels)**

## 8.3 Power Supply Recommendations

Bypass capacitors must be used on power pins. TI recommends using high-frequency, ceramic, 0.1µF and 0.01µF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed-circuit board improves decoupling. Multiple vias must be used to connect the decoupling capacitors to the power planes. A 10µF bulk capacitor, 35V (or greater) solid tantalum capacitor must be connected at the power entry point on the printed-circuit board between the supply and ground.

## 8.4 Layout

### 8.4.1 Layout Guidelines

#### 8.4.1.1 Differential Traces

Use controlled impedance traces which match the differential impedance of your transmission trace and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and make sure noise is coupled as common-mode. In fact, differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode, which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. It is important to note: skew between the signals of a pair means a phase difference between signals, which destroys the magnetic field cancellation benefits of differential signals and EMI, will result. (Note that the velocity of propagation, v = c/E $_r$ where c (the speed of light) = 0.2997mm/ps or 0.0118in/ps). Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowed.

#### *8.4.1.2 PC Board Considerations*

Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, and TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL signals may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers, which are isolated by one or more power or ground planes.

### 8.4.2 Layout Examples

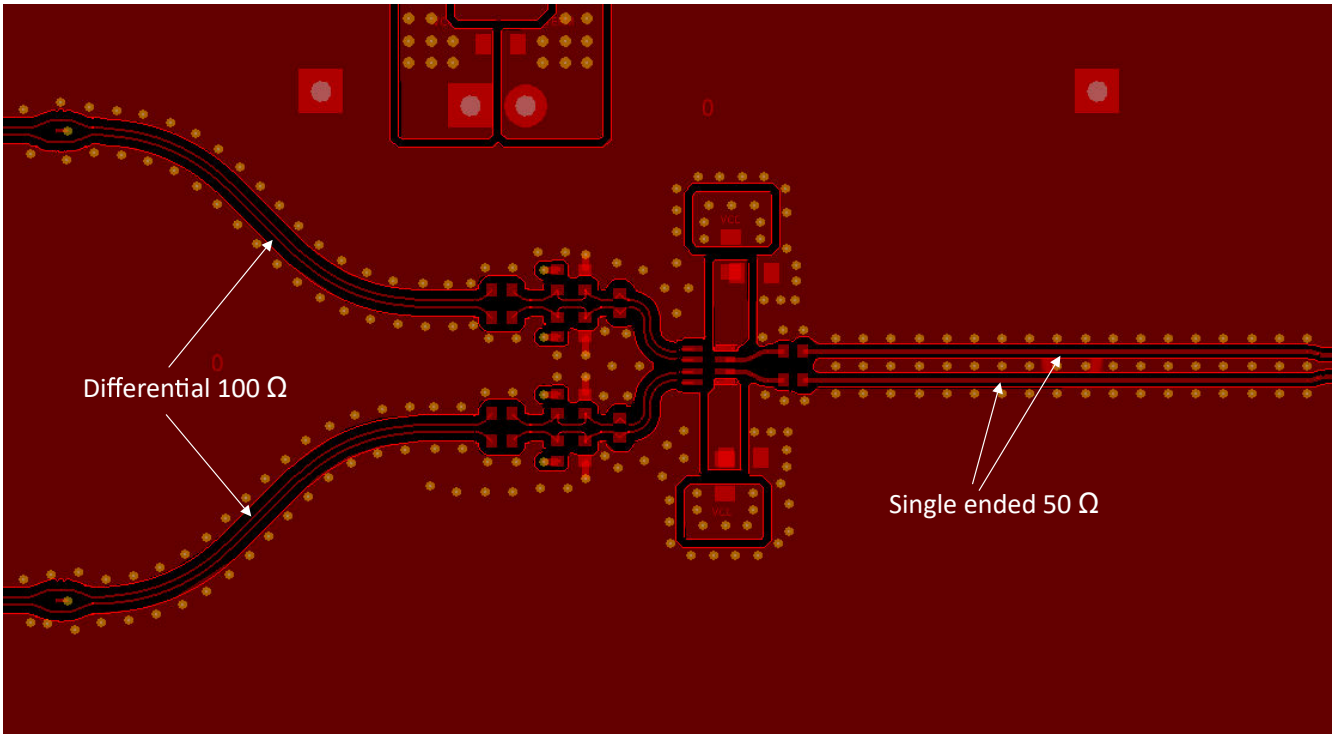



**図 8-3. EVM Layout**

# 9 Device and Documentation Support

## 9.1 Documentation Support

### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Failsafe Biasing of LVDS Interfaces* application note

## 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

## 9.3 サポート・リソース

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## 9.4 Trademarks

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## 9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 10 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| December 2023 | * | Initial Release |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| D9LVRA2DEMRQ1 | Active | Production | WSON (DEM) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LR2Q |
| D9LVRA2DEMRQ1.A | Active | Production | WSON (DEM) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LR2Q |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF DS90LVRA2-Q1 :**

- Catalog : DS90LVRA2

NOTE: Qualified Version Definitions:

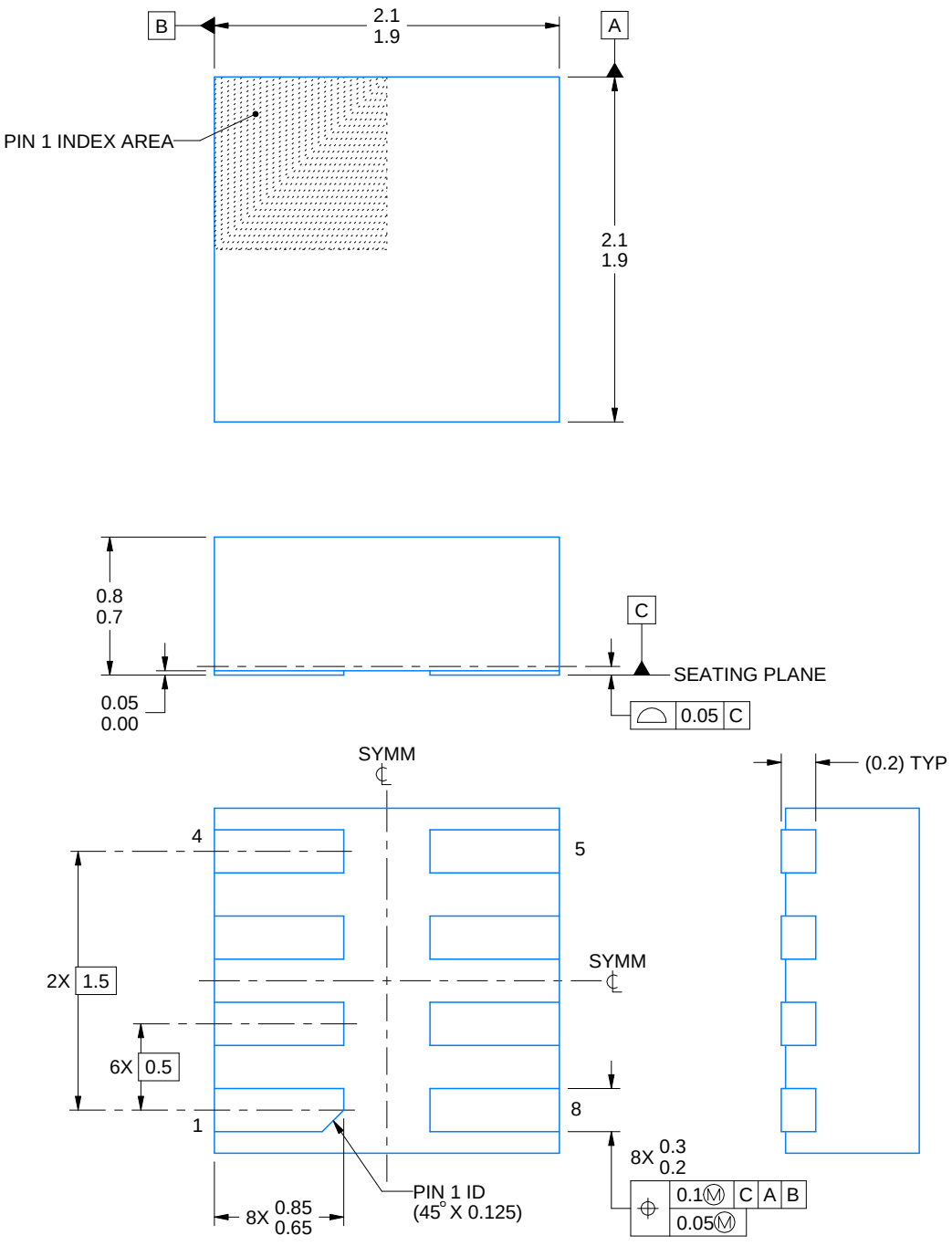
- Catalog - TI's standard catalog product

# DEM0008A

# PACKAGE OUTLINE

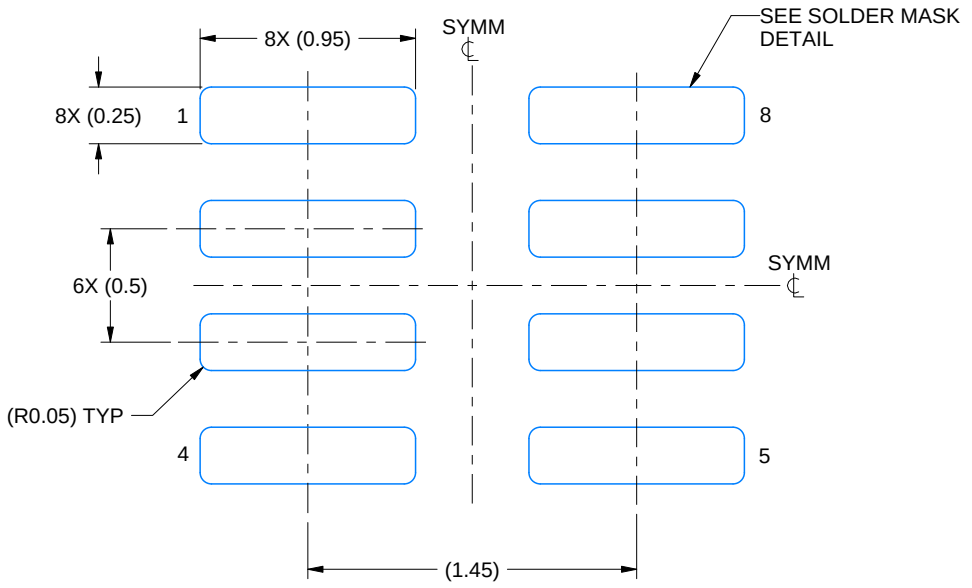
## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

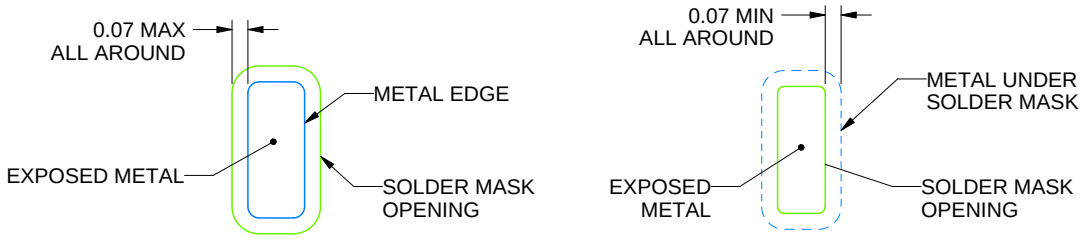



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X




SOLDER MASK DETAILS

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NOTES: (continued)

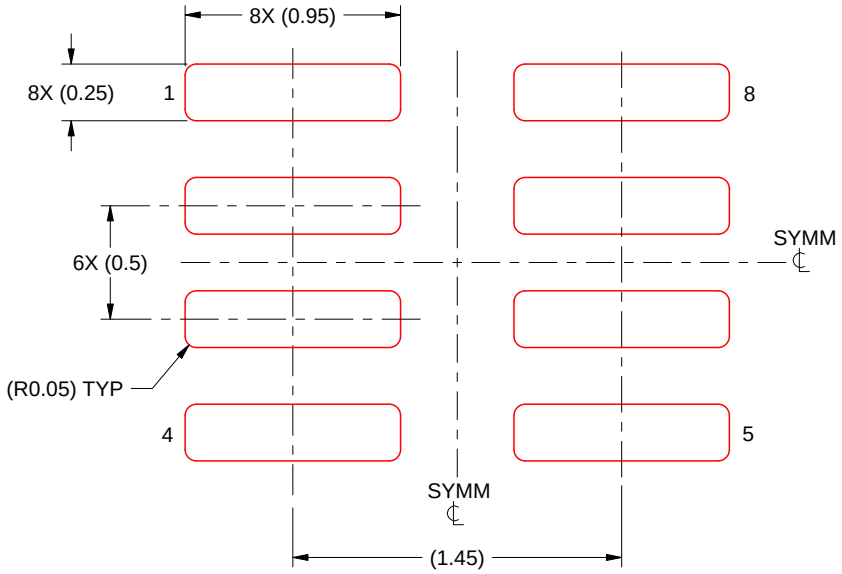
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DEM0008A

## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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