

## DS90LV028A-Q1 車載対応、LVDS デュアル差動ライン・レシーバ

### 1 特長

- 車載アプリケーション向けに AEC-Q100 認定済み
  - 温度グレード 2: -40°C ~ +105°C
- 400Mbps (200MHz) を超えるスイッチング速度
- 差動スキュー: 50ps (標準値)
- チャンネル間スキュー: 0.1ns (標準値)
- 最大伝搬遅延: 2.5ns
- 3.3V 電源の設計
- フロースルーのピン配置
- 電源オフ時に高インピーダンスになる LVDS 入力
- 低消費電力の設計 (静的電圧 3.3V で 18mW)
- LVDS 入力は LVDS/CML/LVPECL 信号に対応
- ANSI/TIA/EIA-644 規格に準拠

### 2 アプリケーション

- 電子 POS (EPOS) アプリケーション
- 車載用インフォテインメントおよびクラスタ
- 車載用ヘッド・ユニット

### 3 概要

DS90LV028A-Q1 はデュアル CMOS 差動ライン・レシーバで、超低消費電力、低ノイズ、高いデータ速度を必要とするアプリケーション用に設計されています。このデバイスは、低電圧差動信号 (LVDS) テクノロジーを活用し、400Mbps (200MHz) を超えるデータ速度をサポートするように設計されています。

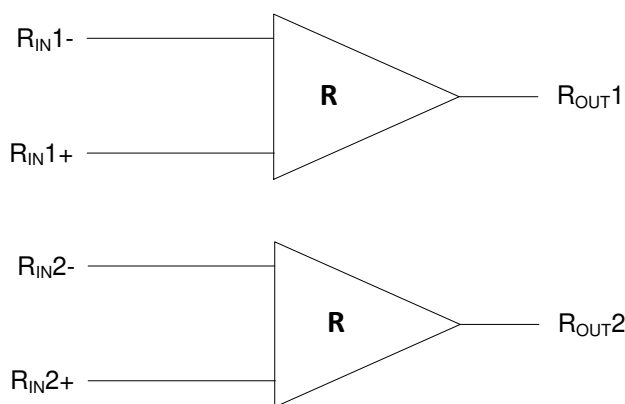
DS90LV028A-Q1 は低電圧 (標準値 350mV) の差動入力信号を受信し、3V CMOS 出力レベルへ変換します。DS90LV028A-Q1 にはフロースルー設計が採用されているため、PCB レイアウトが容易です。

DS90LV028A-Q1 と、対になる LVDS ライン・ドライバ DS90LV027AQ は、消費電力の大きい PECL/ECL デバイスの新しい代替品として、高速のポイント・ツー・ポイント・インターフェイス・アプリケーションに使用できます。

#### 製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
DS90LV028A-Q1	WSO (DQF 8)	2.00mm × 2.00mm

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ダイアグラム



## Table of Contents

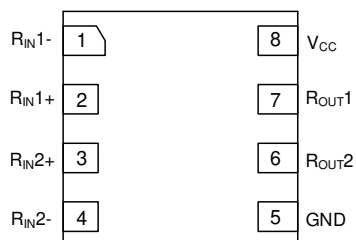
<b>1 特長</b> .....	<b>1</b>	<b>8.2 Functional Block Diagram</b> .....	<b>10</b>
<b>2 アプリケーション</b> .....	<b>1</b>	<b>8.3 Feature Description</b> .....	<b>10</b>
<b>3 概要</b> .....	<b>1</b>	<b>8.4 Device Functional Modes</b> .....	<b>10</b>
<b>4 Revision History</b> .....	<b>2</b>	<b>9 Application and Implementation</b> .....	<b>11</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	9.1 Application Information.....	11
Pin Functions.....	3	9.2 Typical Application.....	11
<b>6 Specifications</b> .....	<b>4</b>	<b>10 Power Supply Recommendations</b> .....	<b>13</b>
6.1 Absolute Maximum Ratings.....	4	<b>11 Layout</b> .....	<b>14</b>
6.2 ESD and Latch-Up Ratings.....	4	11.1 Layout Guidelines.....	14
6.3 Recommended Operating Conditions.....	4	11.2 Layout Examples.....	14
6.4 Thermal Information.....	4	<b>12 Device and Documentation Support</b> .....	<b>15</b>
6.5 Electrical Characteristics.....	5	12.1 Support Resources.....	15
6.6 Switching Characteristics.....	5	12.2 Trademarks.....	15
6.7 Typical Performance Curves.....	6	12.3 静電気放電に関する注意事項.....	15
<b>7 Parameter Measurement Information</b> .....	<b>9</b>	12.4 Glossary.....	15
<b>8 Detailed Description</b> .....	<b>10</b>	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>16</b>
8.1 Overview.....	10		

## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
August 2020	*	Initial Release

## 5 Pin Configuration and Functions



✎ 5-1. DQF Package WSON 8 Pin Top View

### Pin Functions

Pin Number	Name	Description
1	$R_{IN1-}$	Inverting receiver input pin
4	$R_{IN2-}$	
2	$R_{IN1+}$	Non-inverting receiver input pin
3	$R_{IN2+}$	
6	$R_{OUT2}$	Receiver output pin
7	$R_{OUT1}$	
8	$V_{CC}$	Power supply pin, +3.3V +/- 0.3V
5	GND	Ground pin

## 6 Specifications

### 6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Supply Voltage ( $V_{CC}$ )		-0.3	4	V
Input Voltage ( $R_{IN+}$ , $R_{IN-}$ )		-0.3	3.9	V
Output Voltage ( $R_{OUT}$ )		-0.3	$V_{CC}+0.3$	V
Lead Temperature Range Soldering	(4 sec.)		260	°C
Maximum Junction Temperature			125	°C
Storage temperature, $T_{slg}$		-65	150	°C

### 6.2 ESD and Latch-Up Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1250	
I-Test+	Positive I-Test Latch-Up	Positive I-Test Latchup, per AEC Q100-004 at maximum ambient temperature (all signal pins)	+100	mA
I-Test-	Negative I-Test Latch-Up	Negative I-Test Latchup, per AEC Q100-004 at maximum ambient temperature (all signal pins except pin 3)	-100	mA
		Negative I-Test Latchup, per AEC Q100-004 at maximum ambient temperature (pin 3)	-70	mA

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage ( $V_{CC}$ )	+3.0	+3.3	+3.6	V
Receiver Input Voltage	+0.5		+2.1	V
Operating Free Air Temperature ( $T_A$ )	-40	25	105	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DS90LV028A-Q1	UNIT
		DQF (WSON)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	104.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	33.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.6	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	0.3	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	27.4	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. <sup>(1)</sup> <sup>(2)</sup>



Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
$V_{TH}$	Differential Input High Threshold	$V_{CM}^{(1)} = +1.2\text{ V}, 0.5 + ( V_{ID} /2)\text{ V}, 2.1 - ( V_{ID} /2)^{(2)}$	$R_{IN+}, R_{IN-}$			+100	mV
$V_{TL}$	Differential Input Low Threshold			-100			mV
$I_{IN}$	Input Current	$V_{IN} = +2.8\text{ V}$		-10	$\pm 1$	+10	$\mu\text{A}$
		$V_{IN} = 0\text{ V}$		-10	$\pm 1$	+10	$\mu\text{A}$
		$V_{IN} = +3.6\text{ V}$		-20		+20	$\mu\text{A}$
$V_{OH}$	Output High Voltage	$I_{OH} = -0.4\text{ mA}, V_{ID}^{(2)} = +200\text{ mV}$	$R_{OUT}$	2.7	3.1		V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2\text{ mA}, V_{ID}^{(2)} = -200\text{ mV}$			0.3	0.5	V
$I_{OS}$	Output Short Circuit Current	$V_{OUT} = 0\text{ V}^{(3)}$		-100	-50	-15	mA
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18\text{ mA}$		-1.5	-0.8		V
$I_{CC}$	No Load Supply Current	$V_{ID}^{(2)} = +200\text{ mV}$ or $-200\text{ mV}$	$V_{CC}$		5.4	9	mA

(1)  $V_{CM}$  is input common mode voltage  $[(V_{RIN+} + V_{RIN-})/2]$

(2)  $V_{ID}$  is input differential voltage  $(V_{RIN+} - V_{RIN-})$

## 6.6 Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. <sup>(2)</sup> <sup>(4)</sup> <sup>(5)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PHLD}$	Differential Propagation Delay High to Low	$C_L = 15\text{ pF}$	1.0	1.6	2.5	ns
$t_{PLHD}$	Differential Propagation Delay Low to High	$V_{ID} = 200\text{ mV}$	1.0	1.7	2.5	ns
$t_{SKD1}$	Differential Pulse Skew $ t_{PHLD} - t_{PLHD} $ <sup>(6)</sup>	(  7-1 and  7-2)	0	50	650	ps
$t_{SKD2}$	Differential Channel-to-Channel Skew-same device <sup>(7)</sup>		0	0.1	0.5	ns
$t_{SKD3}$	Differential Part to Part Skew <sup>(8)</sup>		0		1.0	ns
$t_{SKD4}$	Differential Part to Part Skew <sup>(9)</sup>		0		1.5	ns
$t_{TLH}$	Rise Time			325	800	ps
$t_{THL}$	Fall Time			225	800	ps
$f_{MAX}$	Maximum Operating Frequency <sup>(10)</sup>			250		MHz

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified (such as  $V_{ID}$ ).

(2) All typicals are given for:  $V_{CC} = +3.3\text{ V}$  and  $T_A = +25^\circ\text{C}$ .

(3) Output short circuit current ( $I_{OS}$ ) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

(4)  $C_L$  includes probe and jig capacitance.

(5) Generator waveform for all tests unless otherwise specified:  $f = 1\text{ MHz}$ ,  $Z_O = 50\Omega$ ,  $t_r$  and  $t_f$  (0% to 100%)  $\leq 3\text{ ns}$  for  $R_{IN}$ .

(6)  $t_{SKD1}$  is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of the same channel.

(7)  $t_{SKD2}$  is the differential channel-to-channel skew of any event on the same device. This specification applies to devices having multiple receivers within the integrated circuit.

(8)  $t_{SKD3}$ , part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same  $V_{CC}$  and within  $5^\circ\text{C}$  of each other within the operating temperature range.

(9)  $t_{SKD4}$ , part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over the recommended operating temperature and voltage ranges, and across process distribution.  $t_{SKD4}$  is defined as  $|\text{Max} - \text{Min}|$  differential propagation delay.

(10)  $f_{MAX}$  generator input conditions:  $t_r = t_f < 1\text{ ns}$  (0% to 100%), 50% duty cycle, differential (1.05V to 1.35 peak to peak). Output criteria: 60%/40% duty cycle,  $V_{OL}$  (max 0.4V),  $V_{OH}$  (min 2.7V), load = 15 pF (stray plus probes).

## 6.7 Typical Performance Curves

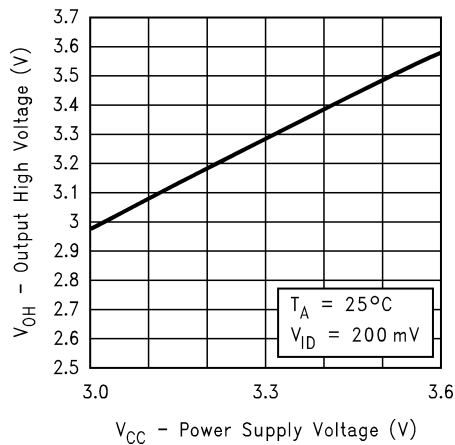


FIG 6-1. Output High Voltage vs Power Supply Voltage

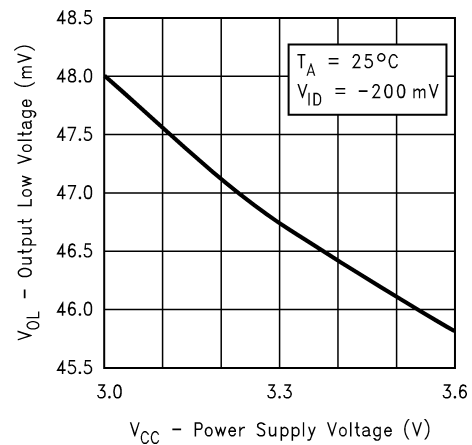


FIG 6-2. Output Low Voltage vs Power Supply Voltage

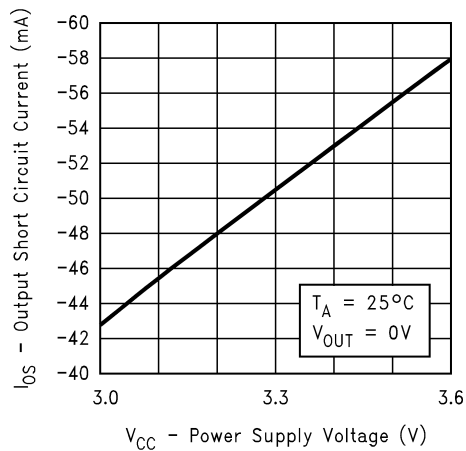


FIG 6-3. Output Short Circuit Current vs Power Supply Voltage

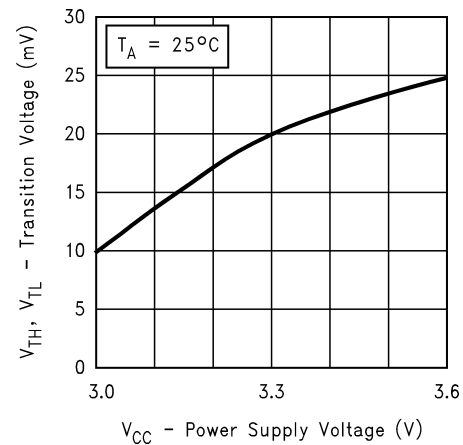


FIG 6-4. Differential Transition Voltage vs Power Supply Voltage

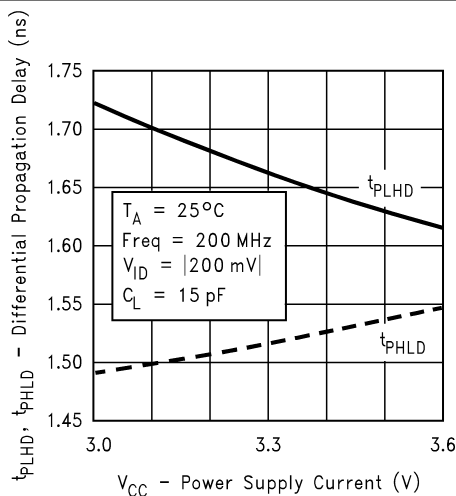


FIG 6-5. Differential Propagation Delay vs Power Supply Voltage

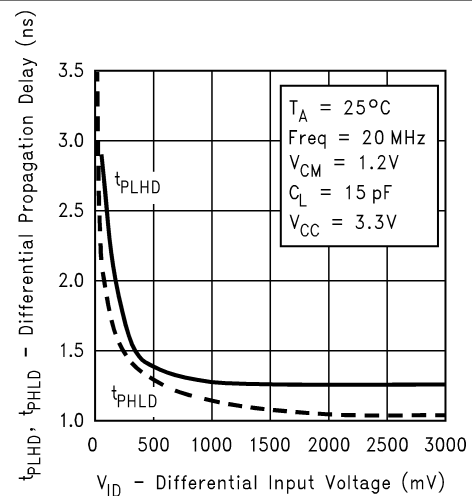
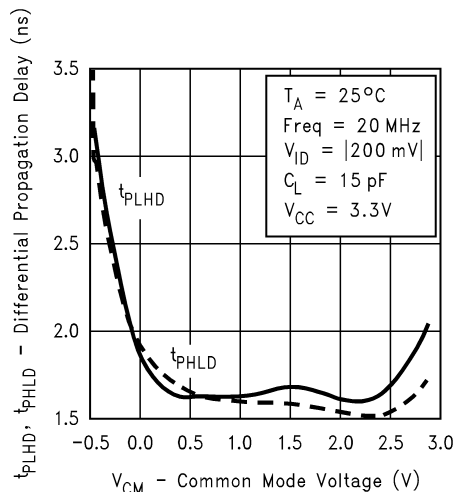
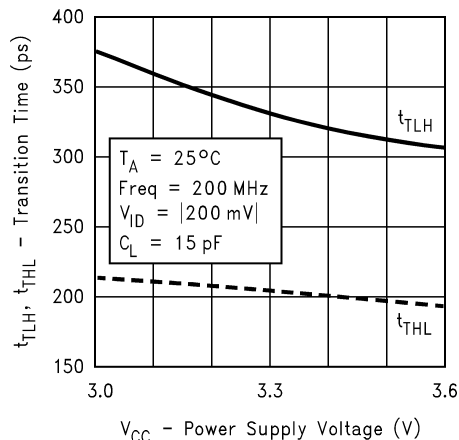


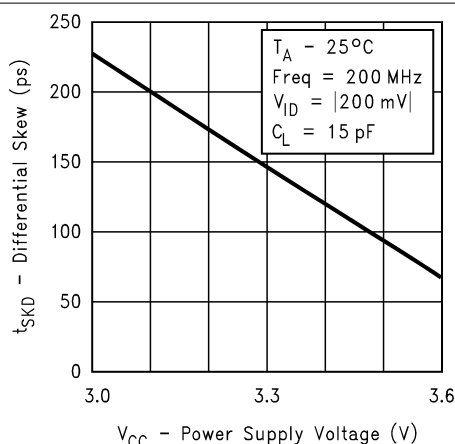
FIG 6-6. Differential Propagation Delay vs Differential Input Voltage



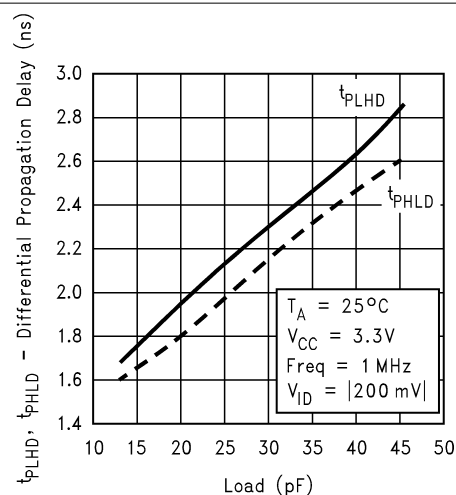
**Figure 6-7. Differential Propagation Delay vs Common-Mode Voltage**



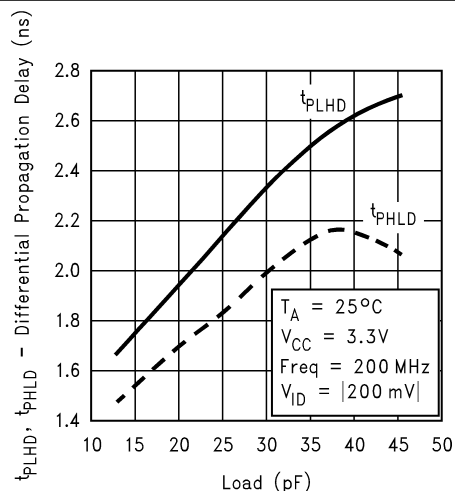
**Figure 6-8. Transition Time vs Power Supply Voltage**



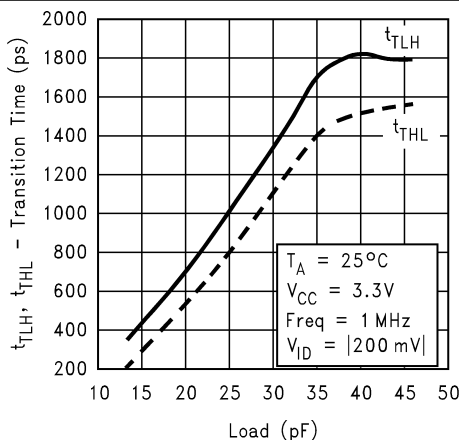
**Figure 6-9. Differential Skew vs Power Supply Voltage**



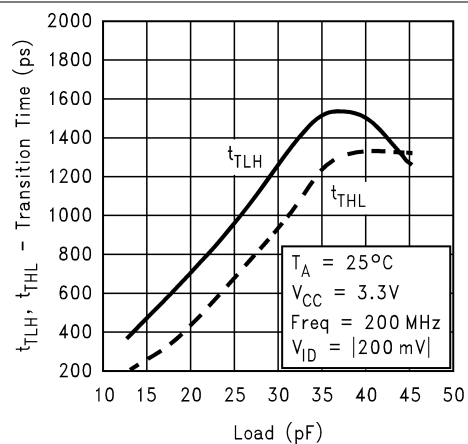
**Figure 6-10. Differential Propagation Delay vs Load**



**Figure 6-11. Differential Propagation Delay vs Load**



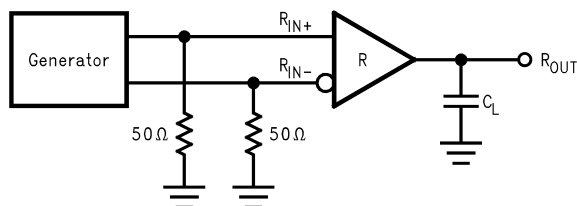
**Figure 6-12. Transition Time vs Load**



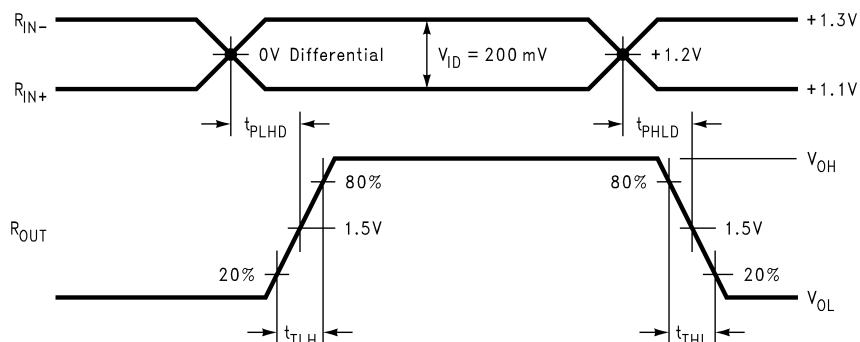
**6-13. Transition Time vs Load**



## 7 Parameter Measurement Information



**7-1. Receiver Propagation Delay and Transition Time Test Circuit**



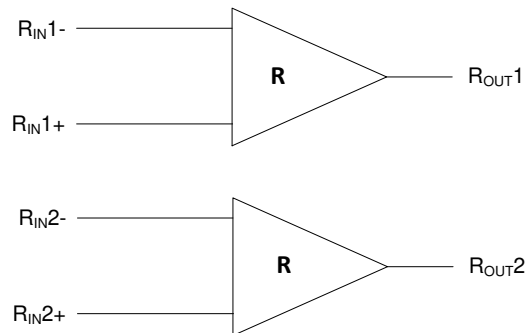
**7-2. Receiver Propagation Delay and Transition Time Waveforms**

## 8 Detailed Description

### 8.1 Overview

LVDS drivers and receivers are intended to be primarily used in a simple point-to-point configuration as is shown in [Figure 9-1](#). This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the source through a impedance controlled 100  $\Omega$  differential PCB traces. A termination resistor of 100  $\Omega$  should be used, and is located as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The DS90LV028A-Q1 differential line receiver is capable of detecting signals as low as 100 mV, over a common-mode range of  $0.5 + (V_{ID}/2)$  V to  $2.1 - (V_{ID}/2)$  V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift  $\pm 0.5$ V around this center point. The  $\pm 0.5$ V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of +0.5V to +2.1V (measured from each pin to ground). The device will operate for receiver input voltages up to  $V_{CC}$ , but exceeding  $V_{CC}$  will turn on the ESD protection circuitry which will clamp the bus voltages.

### 8.4 Device Functional Modes

表 8-1. Truth Table

INPUTS	OUTPUT
$[R_{IN+}] - [R_{IN-}]$	$R_{OUT}$
$V_{ID} \geq 0.1V$	H
$V_{ID} \leq -0.1V$	L
$-0.1V \leq V_{ID} \leq 0.1V$	? <sup>(1)</sup>

(1) ? indicates state is indeterminate

## 9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

General application guidelines and hints for LVDS drivers and receivers may be found in the [LVDS application notes and design guides](#).

### 9.2 Typical Application

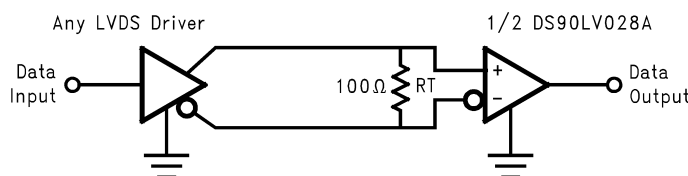


图 9-1. Balanced System Point-to-Point Application

#### 9.2.1 Design Requirements

When using LVDS devices, it is important to remember to specify controlled impedance PCB traces. All components of the transmission media must have a matched differential impedance of 100  $\Omega$ . They must not introduce major impedance discontinuities.

#### 9.2.2 Detailed Design Procedure

##### 9.2.2.1 Power Decoupling Recommendations

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1  $\mu\text{F}$  and 0.01  $\mu\text{F}$  capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10  $\mu\text{F}$  (35 V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

##### 9.2.2.2 Termination

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor should be between 90  $\Omega$  and 110  $\Omega$ . Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work correctly without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% resistors are the best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10 mm (12 mm MAX).

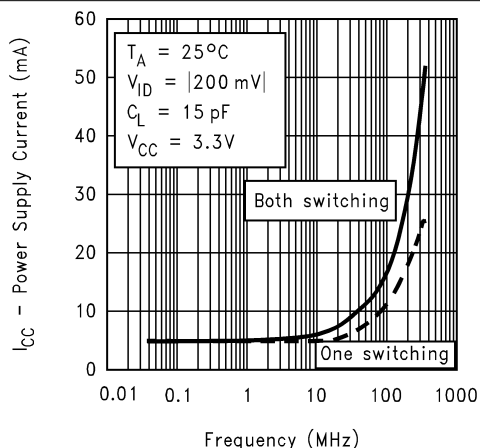
##### 9.2.2.3 Input Failsafe Biasing

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to VDD thru a pull up resistor and the negative LVDS input pin is tied to GND by a pull down resistor. The pull up and pull down resistors should be in the 5 k $\Omega$  to 15 k $\Omega$  range to minimize loading and waveform distortion to the driver. The common-mode bias point ideally should be set to approximately 1.2 V to be compatible with the internal circuitry. Please refer to application note AN-1194, "Failsafe Biasing of LVDS Interfaces" ([SNLA051](#)) for more information.

### 9.2.2.4 Probing LVDS Transmission Lines

Always use high impedance ( $> 100\text{ k}\Omega$ ), low capacitance ( $< 2\text{ pF}$ ) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

### 9.2.3 Application Curves



 **9-2. Power Supply Current vs Frequency**

## 10 Power Supply Recommendations

Bypass capacitors must be used on power pins. TI recommends using high-frequency, ceramic, 0.1- $\mu$ F and 0.01- $\mu$ F capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed-circuit board improves decoupling. Multiple vias must be used to connect the decoupling capacitors to the power planes. A 10- $\mu$ F bulk capacitor, 35-V (or greater) solid tantalum capacitor must be connected at the power entry point on the printed-circuit board between the supply and ground.

## 11 Layout

### 11.1 Layout Guidelines

#### 11.1.1 Differential Traces

Use controlled impedance traces which match the differential impedance of your transmission trace and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation,  $v = c/E_r$  where  $c$  (the speed of light) = 0.2997 mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

#### 11.1.2 PC Board Considerations

Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL signals may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

### 11.2 Layout Examples

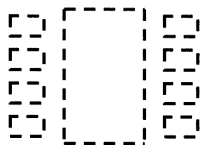


FIG 11-1. WSON Thermal Land Pad and Pin Pads

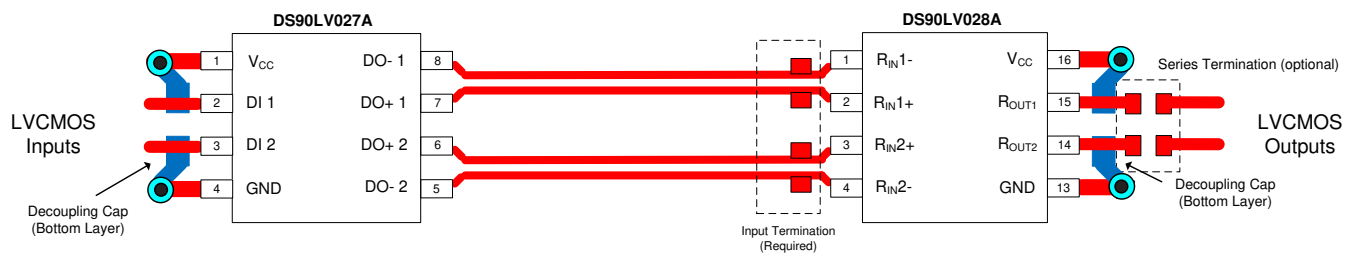


FIG 11-2. Simplified DS90LV027A and DS90LV028A Layout

## 12 Device and Documentation Support

### 12.1 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.2 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 12.3 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 12.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">DS90LV028AQDQFRQ1</a>	Active	Production	WSO (DQF)   8	3000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D28Q
DS90LV028AQDQFRQ1.B	Active	Production	WSO (DQF)   8	3000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D28Q
<a href="#">DS90LV028AQDQFTQ1</a>	Active	Production	WSO (DQF)   8	250   SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D28Q
DS90LV028AQDQFTQ1.B	Active	Production	WSO (DQF)   8	250   SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	D28Q

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF DS90LV028A-Q1 :**

- Catalog : [DS90LV028A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

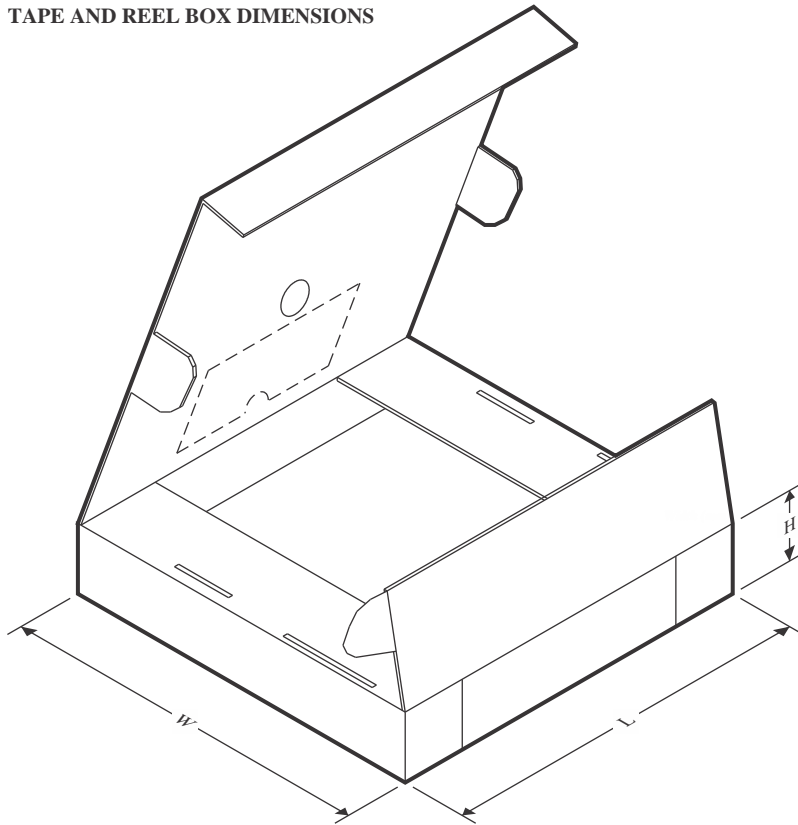
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV028AQDQFRQ1	WSO	DQF	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q1
DS90LV028AQDQFTQ1	WSO	DQF	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV028AQDQFRQ1	WS0N	DQF	8	3000	205.0	200.0	33.0
DS90LV028AQDQFTQ1	WS0N	DQF	8	250	205.0	200.0	33.0

NOTES:

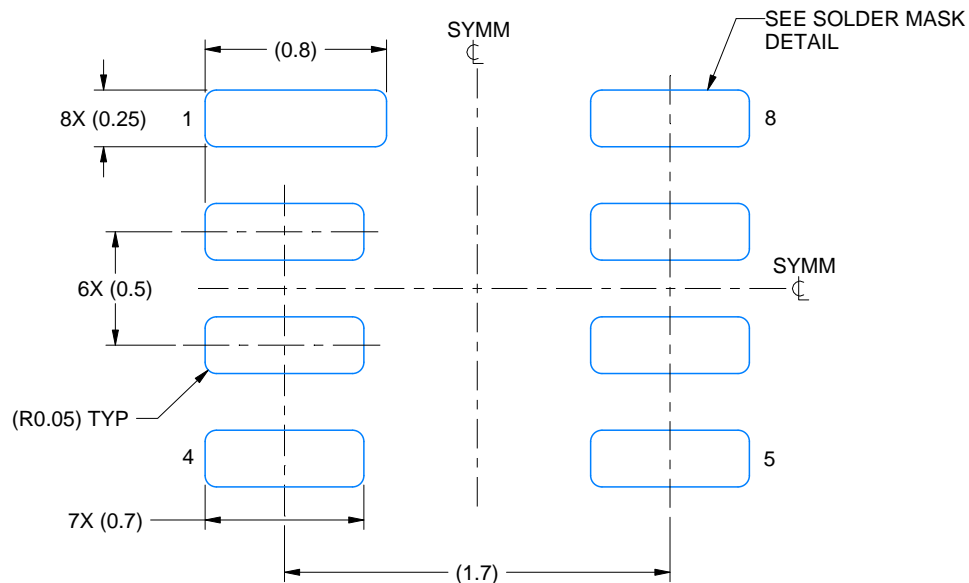
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

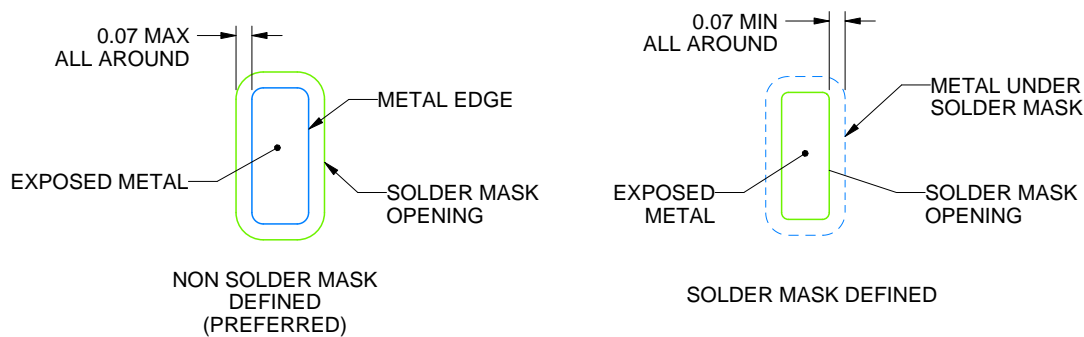
DQF0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 30X



SOLDER MASK DETAILS

4220563/A 03/2021

NOTES: (continued)

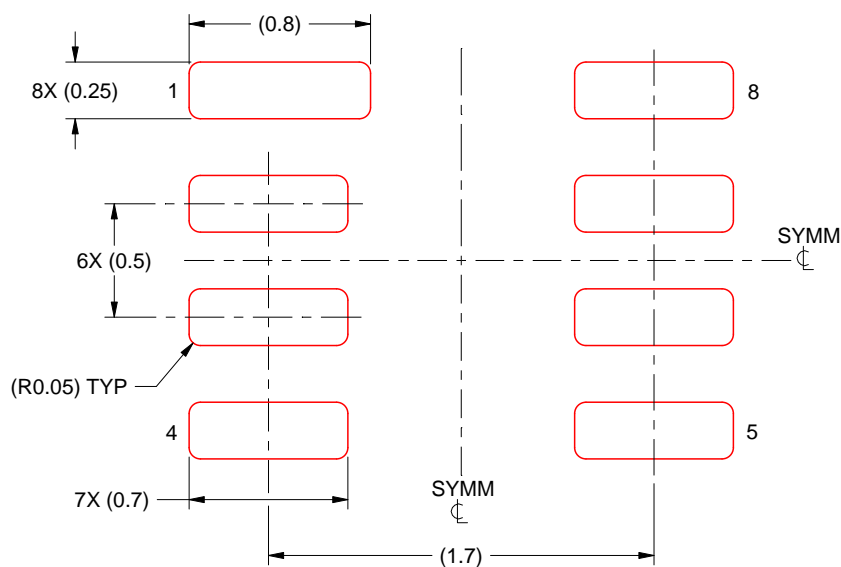
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

# EXAMPLE STENCIL DESIGN

DQF0008A

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 30X

4220563/A 03/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](#) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日：2025 年 10 月