

## +3.3V Programmable LVDS Transmitter 18-Bit Flat Panel Display (FPD) Link -65 MHz

Check for Samples: [DS90CF363B](#)

### FEATURES

- No Special Start-up Sequence Required between Clock/Data and /PD Pins. Input Signal (Clock and Data) can be Applied Either Before or After the Device is Powered.
- Support Spread Spectrum Clocking up to 100KHz Frequency Modulation & Deviations of  $\pm 2.5\%$  Center Spread or  $-5\%$  Down Spread.
- "Input Clock Detection" Feature will Pull all LVDS Pairs to Logic Low when Input Clock is Missing and when /PD Pin is Logic High.
- 18 to 68 MHz Shift Clock Support
- Best-in-Class Set & Hold Times on TxINPUTs
- Tx Power Consumption < 130 mW (typ) @65MHz Grayscale
- 40% Less Power Dissipation than BiCMOS Alternatives
- Tx Power-Down Mode < 37 $\mu$ W (typ)
- Supports VGA, SVGA, XGA and Dual Pixel SXGA.
- Narrow Bus Reduces Cable Size and Cost
- Up to 1.3 Gbps Throughput
- Up to 170 Megabytes/sec Bandwidth

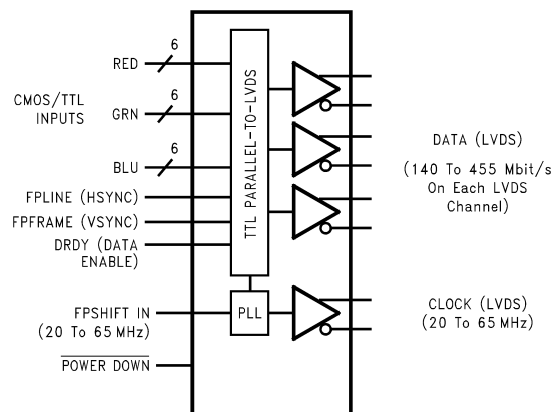
- 345 mV (typ) Swing LVDS Devices for Low EMI
- PLL Requires no External Components
- Compatible with TIA/EIA-644 LVDS Standard
- Low Profile 48-lead TSSOP Package
- Improved Replacement for:
  - SN75LVDS84, DS90CF363A

### DESCRIPTION

The DS90CF363B transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. At a transmit clock frequency of 65 MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 170 Mbytes/sec. The DS90CF363B is fixed as a Falling edge strobe transmitter and will interoperate with a Falling edge strobe Receiver (DS90CF366) without any translation logic.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

### Block Diagram



**Figure 1. DS90CF363B**  
See Package Number DGG0048A



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings <sup>(1)(2)</sup>

|   | Value                      | Unit |
|---|----------------------------|------|
| Supply Voltage ( $V_{CC}$ )                       | -0.3 to +4                 | V    |
| CMOS/TTL Input Voltage                            | -0.3 to ( $V_{CC} + 0.3$ ) | V    |
| LVDS Driver Output Voltage                        | -0.3 to ( $V_{CC} + 0.3$ ) | V    |
| LVDS Output Short Circuit Duration                | Continuous                 |      |
| Junction Temperature                              | +150                       | °C   |
| Storage Temperature                               | -65 to +150                | °C   |
| Lead Temperature (Soldering, 4 sec)               | +260                       | °C   |
| Maximum Package Power Dissipation Capacity @ 25°C |                            |      |
| DGG-48 (TSSOP) Package: DS90CF363B                | 1.98                       | W    |
| Package Derating: DS90CF363B                      | 16 mW/°C above +25°C       |      |
| ESD Rating (HBM, 1.5 kΩ, 100 pF)                  | 7                          | kV   |
| ESD Rating (EIAJ, 0Ω, 200 pF)                     | 500                        | V    |

- (1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be verified. They are not meant to imply that the device should be operated at these limits. Electrical Characteristics specify conditions for device operation.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

## Recommended Operating Conditions

|  | Min | Nom | Max | Units            |
|--|-----|-----|-----|------------------|
| Supply Voltage ( $V_{CC}$ )              | 3.0 | 3.3 | 3.6 | V                |
| Operating Free Air Temperature ( $T_A$ ) | -10 | +25 | +70 | °C               |
| Supply Noise Voltage ( $V_{CC}$ )        |     |     | 200 | mV <sub>PP</sub> |
| TxCLKIN frequency                        | 18  |     | 68  | MHz              |

## Electrical Characteristics <sup>(1)</sup>

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol                     | Parameter   | Conditions                                      | Min  | Typ <sup>(2)</sup> | Max             | Units |
|----------------------------|---|---|------|--------------------|-----------------|-------|
| CMOS/TTL DC SPECIFICATIONS |   |   |      |                    |                 |       |
| V <sub>IH</sub>            | High Level Input Voltage                                      |   | 2.0  |                    | V <sub>CC</sub> | V     |
| V <sub>IL</sub>            | Low Level Input Voltage                                       |   | GND  |                    | 0.8             | V     |
| V <sub>CL</sub>            | Input Clamp Voltage   | I <sub>CL</sub> = -18 mA                        |      | -0.79              | -1.5            | V     |
| I <sub>IN</sub>            | Input Current   | V <sub>IN</sub> = 0.4V, 2.5V or V <sub>CC</sub> |      | +1.8               | +10             | μA    |
|                            |   | V <sub>IN</sub> = GND                           | -10  | 0                  |                 | μA    |
| LVDS DC SPECIFICATIONS     |   |   |      |                    |                 |       |
| V <sub>OD</sub>            | Differential Output Voltage                                   | R <sub>L</sub> = 100Ω                           | 250  | 345                | 450             | mV    |
| ΔV <sub>OD</sub>           | Change in V <sub>OD</sub> between complimentary output states |   |      |                    | 35              | mV    |
| V <sub>OS</sub>            | Offset Voltage <sup>(3)</sup>                                 |   | 1.13 | 1.25               | 1.38            | V     |
| ΔV <sub>OS</sub>           | Change in V <sub>OS</sub> between complimentary output states |   |      |                    | 35              | mV    |
| I <sub>OS</sub>            | Output Short Circuit Current                                  | V <sub>OUT</sub> = 0V, R <sub>L</sub> = 100Ω    |      | -3.5               | -5              | mA    |

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except  $V_{OD}$  and  $\Delta V_{OD}$ ).
- (2) Typical values are given for  $V_{CC} = 3.3$  V and  $T_A = +25^\circ\text{C}$  unless specified otherwise.
- (3)  $V_{OS}$  previously referred as  $V_{CM}$ .

## Electrical Characteristics<sup>(1)</sup> (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol                            | Parameter                                  | Conditions   | Min        | Typ <sup>(2)</sup> | Max | Units |
|-----------------------------------|--|--|------------|--------------------|-----|-------|
| I <sub>oz</sub>                   | Output TRI-STATE Current                   | Power Down = 0V,<br>V <sub>OUT</sub> = 0V or V <sub>CC</sub>   |            | ±1                 | ±10 | μA    |
| <b>TRANSMITTER SUPPLY CURRENT</b> |  |  |            |                    |     |       |
| ICCTW                             | Transmitter Supply Current<br>Worst Case   | R <sub>L</sub> = 100Ω,<br>C <sub>L</sub> = 5 pF,<br>Worst Case Pattern<br>(Figure 2 and Figure 5 ) "<br>Typ " values are given for<br>V <sub>CC</sub> = 3.6V and T <sub>A</sub> =<br>+25°C, " Max " values are<br>given for V <sub>CC</sub> = 3.6V and T <sub>A</sub> =<br>-10°C   | f = 25 MHz |                    | 29  | 40 mA |
|                                   |  |  | f = 40 MHz |                    | 34  | 45 mA |
|                                   |  |  | f = 65 MHz |                    | 42  | 55 mA |
| ICCTG                             | Transmitter Supply Current<br>16 Grayscale | R <sub>L</sub> = 100Ω,<br>C <sub>L</sub> = 5 pF,<br>16 Grayscale Pattern<br>(Figure 3 and Figure 5 ) "<br>Typ " values are given for<br>V <sub>CC</sub> = 3.6V and T <sub>A</sub> =<br>+25°C, " Max " values are<br>given for V <sub>CC</sub> = 3.6V and T <sub>A</sub> =<br>-10°C | f = 25 MHz |                    | 28  | 40 mA |
|                                   |  |  | f = 40 MHz |                    | 32  | 45 mA |
|                                   |  |  | f = 65 MHz |                    | 39  | 50 mA |
| ICCTZ                             | Transmitter Supply Current<br>Power Down   | Power Down = Low<br>Driver Outputs in TRI-STATE under<br>Power Down Mode   |            | 11                 | 150 | μA    |

## Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter                                     | Min   | Typ  | Max   | Units |
|--------|---|-------|------|-------|-------|
| TCIT   | TxCLK IN Transition Time (Figure 6 )          |       |      | 5     | ns    |
| TCIP   | TxCLK IN Period (Figure 7 )                   | 14.7  | T    | 50.0  | ns    |
| TCIH   | TxCLK IN High Time (Figure 7 )                | 0.35T | 0.5T | 0.65T | ns    |
| TCIL   | TxCLK IN Low Time (Figure 7 )                 | 0.35T | 0.5T | 0.65T | ns    |
| TXIT   | TxIN, and Power Down pin transition Time      | 1.5   |      | 6.0   | ns    |
| TXPD   | Minimum pulse width for Power Down pin signal | 1     |      |       | us    |

## Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter   | Min           | Typ   | Max   | Units    |
|--------|---|---------------|-------|-------|----------|
| LLHT   | LVDS Low-to-High Transition Time (Figure 5 )                            |               | 0.75  | 1.4   | ns       |
| LHLT   | LVDS High-to-Low Transition Time (Figure 5 )                            |               | 0.75  | 1.4   | ns       |
| TPPos0 | Transmitter Output Pulse Position for Bit 0 (Figure 12 ) <sup>(1)</sup> | f = 65<br>MHz | -0.20 | 0     | +0.20 ns |
| TPPos1 | Transmitter Output Pulse Position for Bit 1                             |               | 2.00  | 2.20  | 2.40 ns  |
| TPPos2 | Transmitter Output Pulse Position for Bit 2                             |               | 4.20  | 4.40  | 4.60 ns  |
| TPPos3 | Transmitter Output Pulse Position for Bit 3                             |               | 6.39  | 6.59  | 6.79 ns  |
| TPPos4 | Transmitter Output Pulse Position for Bit 4                             |               | 8.59  | 8.79  | 8.99 ns  |
| TPPos5 | Transmitter Output Pulse Position for Bit 5                             |               | 10.70 | 10.99 | 11.19 ns |
| TPPos6 | Transmitter Output Pulse Position for Bit 6                             |               | 12.99 | 13.19 | 13.39 ns |

(1) The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. This parameter is functionality tested only on Automatic Test Equipment (ATE).

## Transmitter Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter  |            | Min   | Typ               | Max   | Units |
|--------|--|------------|-------|-------------------|-------|-------|
| TPPos0 | Transmitter Output Pulse Position for Bit 0 (Figure 12) <sup>(1)</sup>   | f = 40 MHz | -0.25 | 0                 | +0.25 | ns    |
| TPPos1 | Transmitter Output Pulse Position for Bit 1  |            | 3.32  | 3.57              | 3.82  | ns    |
| TPPos2 | Transmitter Output Pulse Position for Bit 2  |            | 6.89  | 7.14              | 7.39  | ns    |
| TPPos3 | Transmitter Output Pulse Position for Bit 3  |            | 10.46 | 10.71             | 10.96 | ns    |
| TPPos4 | Transmitter Output Pulse Position for Bit 4  |            | 14.04 | 14.29             | 14.54 | ns    |
| TPPos5 | Transmitter Output Pulse Position for Bit 5  |            | 17.61 | 17.86             | 18.11 | ns    |
| TPPos6 | Transmitter Output Pulse Position for Bit 6  |            | 21.18 | 21.43             | 21.68 | ns    |
| TPPos0 | Transmitter Output Pulse Position for Bit 0 (Figure 12) <sup>(1)</sup>   | f = 25MHz  | -0.45 | 0                 | +0.45 | ns    |
| TPPos1 | Transmitter Output Pulse Position for Bit 1  |            | 5.26  | 5.71              | 6.16  | ns    |
| TPPos2 | Transmitter Output Pulse Position for Bit 2  |            | 10.98 | 11.43             | 11.88 | ns    |
| TPPos3 | Transmitter Output Pulse Position for Bit 3  |            | 16.69 | 17.14             | 17.59 | ns    |
| TPPos4 | Transmitter Output Pulse Position for Bit 4  |            | 22.41 | 22.86             | 23.31 | ns    |
| TPPos5 | Transmitter Output Pulse Position for Bit 5  |            | 28.12 | 28.57             | 29.02 | ns    |
| TPPos6 | Transmitter Output Pulse Position for Bit 6  |            | 33.84 | 34.29             | 34.74 | ns    |
| TSTC   | TxIN Setup to TxCLK IN (Figure 7 )   |            | 2.5   |                   |       | ns    |
| THTC   | TxIN Hold to TxCLK IN (Figure 7 )  |            | 0.5   |                   |       | ns    |
| TCCD   | TxCLK IN to TxCLK OUT Delay (Figure 8 ) 50% duty cycle input clock is assumed, T <sub>A</sub> = -10°C, and 65MHz for " Min ", T <sub>A</sub> = 70°C, and 25MHz for " Max ", V <sub>CC</sub> = 3.6V |            | 3.011 |                   | 6.082 | ns    |
| SSCG   | Spread Spectrum Clock support; Modulation frequency with a linear profile <sup>(2)</sup>   | f = 25 MHz |       | 100KHz ± 2.5%/-5% |       |       |
|        |  | f = 40 MHz |       | 100KHz ± 2.5%/-5% |       |       |
|        |  | f = 65 MHz |       | 100KHz ± 2.5%/-5% |       |       |
| TPLLS  | Transmitter Phase Lock Loop Set (Figure 9 )  |            |       |                   | 10    | ms    |
| TPDD   | Transmitter Power Down Delay (Figure 11 )  |            |       |                   | 100   | ns    |

(2) Care must be taken to ensure TSTC and THTC are met so input data are sampling correctly. This SSCG parameter only shows the performance of tracking Spread Spectrum Clock applied to TxCLK IN pin, and reflects the result on TxCLKOUT+ and TxCLK- pins.

## AC Timing Diagrams

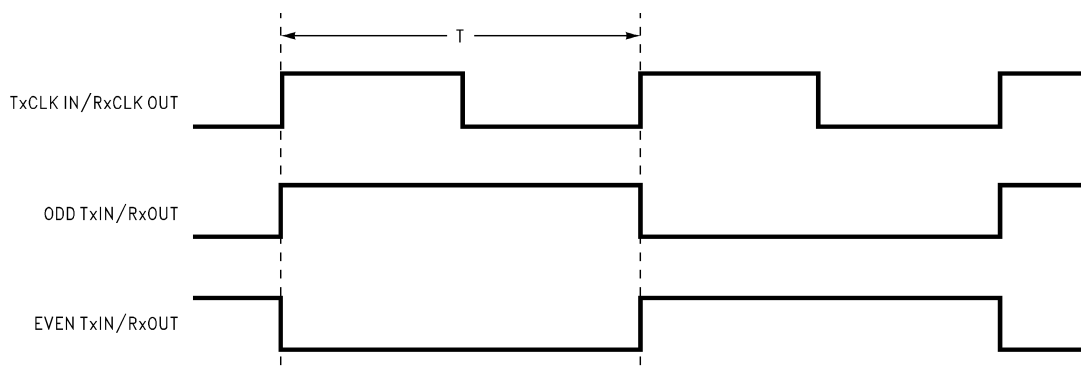


Figure 2. "Worst Case" Test Pattern

| Device Pin Name    | Signal  | Signal Pattern | Signal Frequency   |
|--------------------|---------|----------------|--------------------|
| TxCLK IN/RxCLK OUT | Dot Clk |                | f                  |
| TxIN0/RxOUT0       | R0      |                | f/16               |
| TxIN1/RxOUT1       | R1      |                | f/8                |
| TxIN2/RxOUT2       | R2      |                | f/4                |
| TxIN3/RxOUT3       | R3      |                | f/2                |
| TxIN4/RxOUT4       | R4      |                | Steady State, Low  |
| TxIN5/RxOUT5       | R5      |                | Steady State, Low  |
| TxIN6/RxOUT6       | G0      |                | f/16               |
| TxIN7/RxOUT7       | G1      |                | f/8                |
| TxIN8/RxOUT8       | G2      |                | f/4                |
| TxIN9/RxOUT9       | G3      |                | f/2                |
| TxIN10/RxOUT10     | G4      |                | Steady State, Low  |
| TxIN11/RxOUT11     | G5      |                | Steady State, Low  |
| TxIN12/RxOUT12     | B0      |                | f/16               |
| TxIN13/RxOUT13     | B1      |                | f/8                |
| TxIN14/RxOUT14     | B2      |                | f/4                |
| TxIN15/RxOUT15     | B3      |                | f/2                |
| TxIN16/RxOUT16     | B4      |                | Steady State, Low  |
| TxIN17/RxOUT17     | B5      |                | Steady State, Low  |
| TxIN18/RxOUT18     | HSYNC   |                | Steady State, High |
| TxIN19/RxOUT19     | VSYNC   |                | Steady State, High |
| TxIN20/RxOUT20     | ENA     |                | Steady State, High |

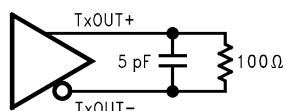
The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

The 16 grayscale test pattern tests device power consumption for a “typical” LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

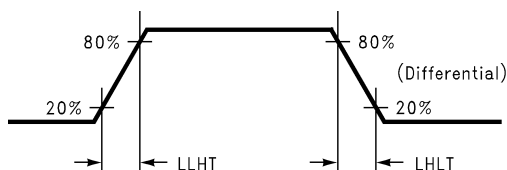
Figure 2 and Figure 3 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Recommended pin to signal mapping. Customer may choose to define differently.

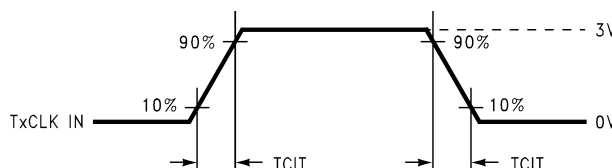
**Figure 3. “16 Grayscale” Test Pattern**



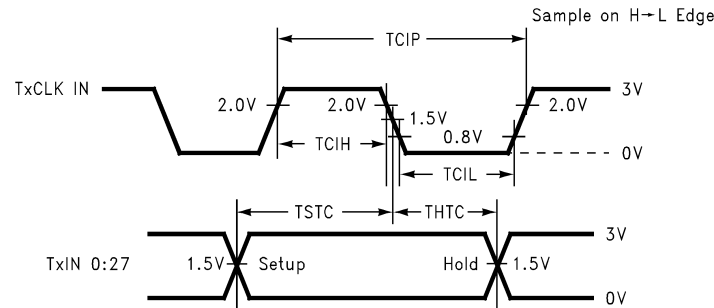
**Figure 4. DS90CF363B (Transmitter) LVDS Output Load**



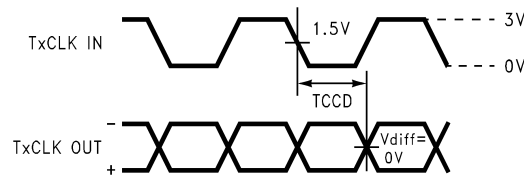
**Figure 5. DS90CF363B (Transmitter) LVDS Transition Times**



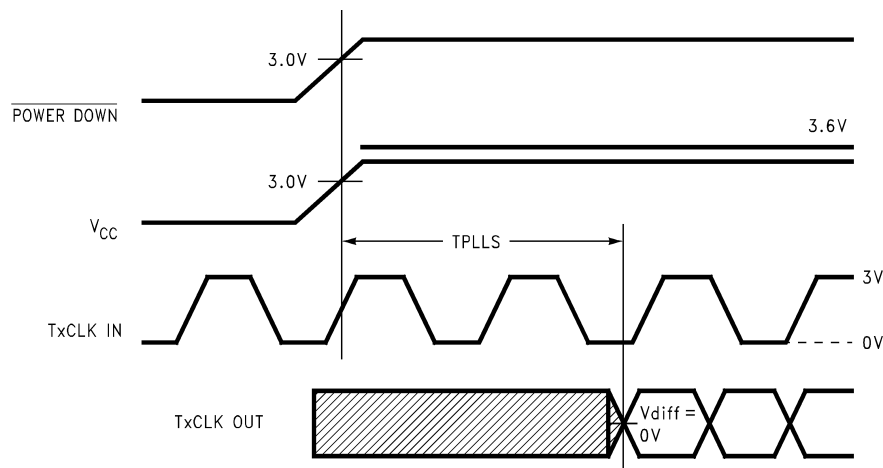
**Figure 6. DS90CF363B (Transmitter) Input Clock Transition Time**



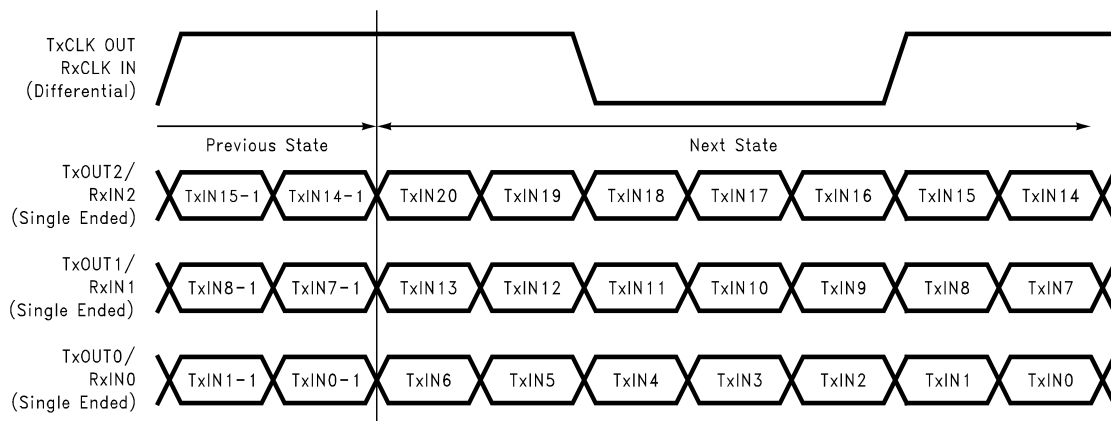
**Figure 7. DS90CF363B (Transmitter) Setup/Hold and High/Low Times (Falling Edge Strobe)**



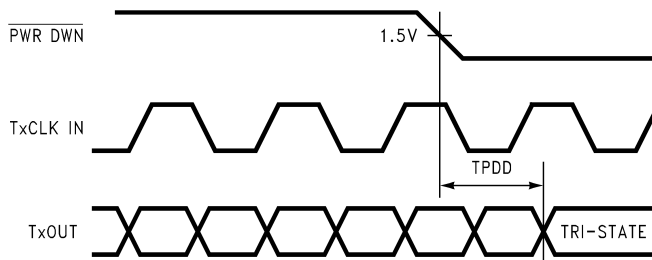
**Figure 8. DS90CF363B (Transmitter) Clock In to Clock Out Delay (Falling Edge Strobe)**



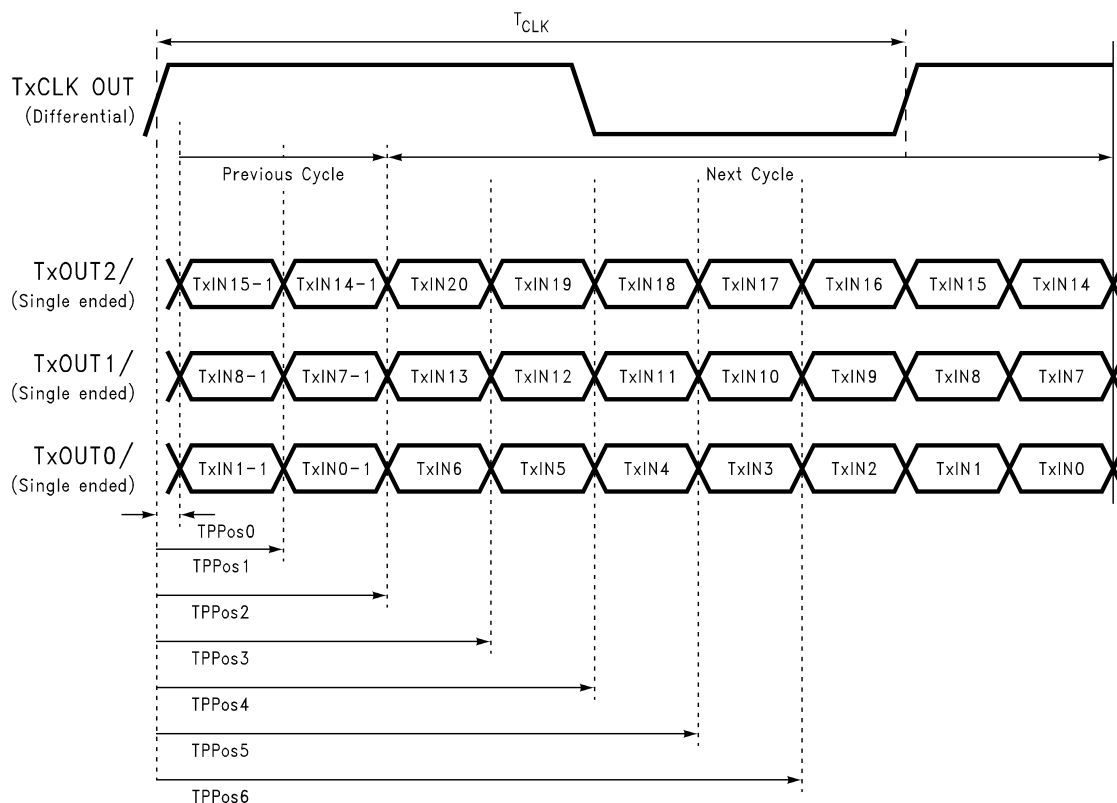
**Figure 9. DS90CF363B (Transmitter) Phase Lock Loop Set Time**



**Figure 10. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs**



**Figure 11. Transmitter Power Down Delay**



**Figure 12. Transmitter LVDS Output Pulse Position Measurement**

**DS90CF363B PIN DESCRIPTIONS — FPD LINK TRANSMITTER**

| Pin Name             | I/O | No. | Description   |
|----------------------|-----|-----|---|
| TxIN                 | I   | 21  | TTL level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable). |
| TxOUT+               | O   | 3   | Positive LVDS differential data output.   |
| TxOUT-               | O   | 3   | Negative LVDS differential data output.   |
| FPSHIFT IN           | I   | 1   | TTL level clock input. The falling edge acts as data strobe. Pin name TxCLK IN.   |
| TxCLK OUT+           | O   | 1   | Positive LVDS differential clock output.  |
| TxCLK OUT-           | O   | 1   | Negative LVDS differential clock output.  |
| PWR DOWN             | I   | 1   | TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down. See <a href="#">Applications Information</a> .     |
| V <sub>CC</sub>      | I   | 4   | Power supply pins for TTL inputs.   |
| GND                  | I   | 4   | Ground pins for TTL inputs.   |
| PLL V <sub>CC</sub>  | I   | 1   | Power supply pin for PLL.   |
| PLL GND              | I   | 2   | Ground pins for PLL.  |
| LVDS V <sub>CC</sub> | I   | 1   | Power supply pin for LVDS outputs.  |
| LVDS GND             | I   | 3   | Ground pins for LVDS outputs.   |
| NC                   |     | 1   | No connect  |

**APPLICATIONS INFORMATION**

The DS90CF363B are backward compatible with the DS90C363/DS90CF363A and are a pin-for-pin replacement.

This device may also be used as a replacement for the DS90CF563 (5V, 65MHz) and DS90CF561 (5V, 40MHz) FPD-Link Transmitters with certain considerations/modifications:

1. Change 5V power supply to 3.3V. Provide this supply to the V<sub>CC</sub>, LVDS V<sub>CC</sub> and PLL V<sub>CC</sub> of the transmitter.

**TRANSMITTER INPUT PINS**

The DS90CF363B transmitter input and control inputs accept 3.3V LVTTTL/LVCMOS levels. They are not 5V tolerant.

**TRANSMITTER INPUT CLOCK/DATA SEQUENCING**

The DS90CF363B does not require any special requirement for sequencing of the input clock/data and PD (PowerDown) signal. The DS90CF363B offers a more robust input sequencing feature where the input clock/data can be inserted after the release of the PD signal. In the case where the clock/data is stopped and reapplied, such as changing video mode within Graphics Controller, it is not necessary to cycle the PD signal. However, there are in certain cases where the PD may need to be asserted during these mode changes. In cases where the source (Graphics Source) may be supplying an unstable clock or spurious noisy clock output to the LVDS transmitter, the LVDS Transmitter may attempt to lock onto this unstable clock signal but is unable to do so due to the instability or quality of the clock source. The PD signal in these cases should then be asserted once a stable clock is applied to the LVDS transmitter. Asserting the PWR DOWN pin will effectively place the device in reset and disable the PLL, enabling the LVDS Transmitter into a power saving standby mode. However, it is still generally a good practice to assert the PWR DOWN pin or reset the LVDS transmitter whenever the clock/data is stopped and reapplied but it is not mandatory for the DS90CF363B.

**SPREAD SPECTRUM CLOCK SUPPORT**

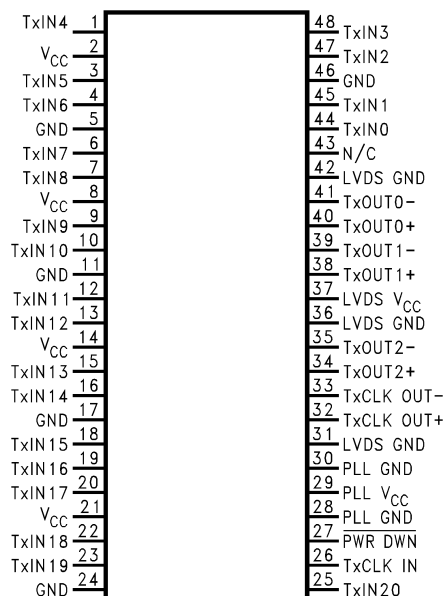
The DS90CF363B can support Spread Spectrum Clocking signal type inputs. The DS90CF363B outputs will accurately track Spread Spectrum Clock/Data inputs with modulation frequencies of up to 100KHz (max.) with either center spread of  $\pm 2.5\%$  or down spread -5% deviations.

**POWER SOURCES SEQUENCE**

In typical applications, it is recommended to have V<sub>CC</sub>, LVDS V<sub>CC</sub> and PLL V<sub>CC</sub> from the same power source with three separate de-coupling bypass capacitor groups. There is no requirement on which VCC entering the device first.

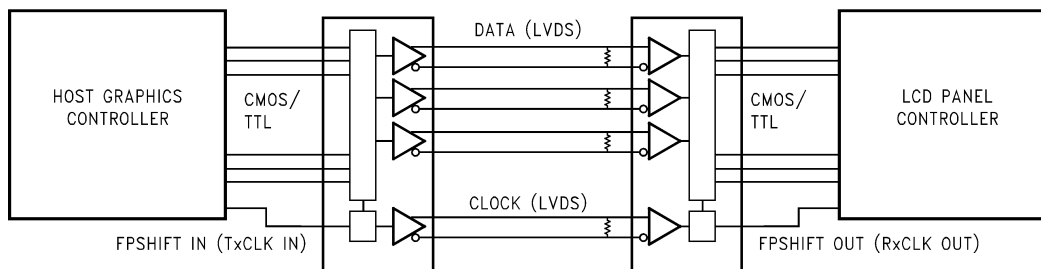


## Pin Diagram



**Figure 13.**

## Typical Application



REVISION HISTORY

| Changes from Revision C (April 2013) to Revision D         | Page              |
|--|-------------------|
| • Changed layout of National Data Sheet to TI format ..... | <a href="#">9</a> |

## PACKAGING INFORMATION

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">DS90CF363BMT/NOPB</a>  | Active        | Production           | TSSOP (DGG)   48 | 38   TUBE             | Yes         | SN                                   | Level-2-260C-1 YEAR               | -10 to 70    | DS90CF363BMT        |
| DS90CF363BMT/NOPB.A                | Active        | Production           | TSSOP (DGG)   48 | 38   TUBE             | Yes         | SN                                   | Level-2-260C-1 YEAR               | -10 to 70    | DS90CF363BMT        |
| <a href="#">DS90CF363BMTX/NOPB</a> | Active        | Production           | TSSOP (DGG)   48 | 1000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -10 to 70    | DS90CF363BMT        |
| DS90CF363BMTX/NOPB.A               | Active        | Production           | TSSOP (DGG)   48 | 1000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -10 to 70    | DS90CF363BMT        |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS90CF363BMTX/NOPB | TSSOP        | DGG             | 48   | 1000 | 330.0              | 24.4               | 8.6     | 13.2    | 1.6     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

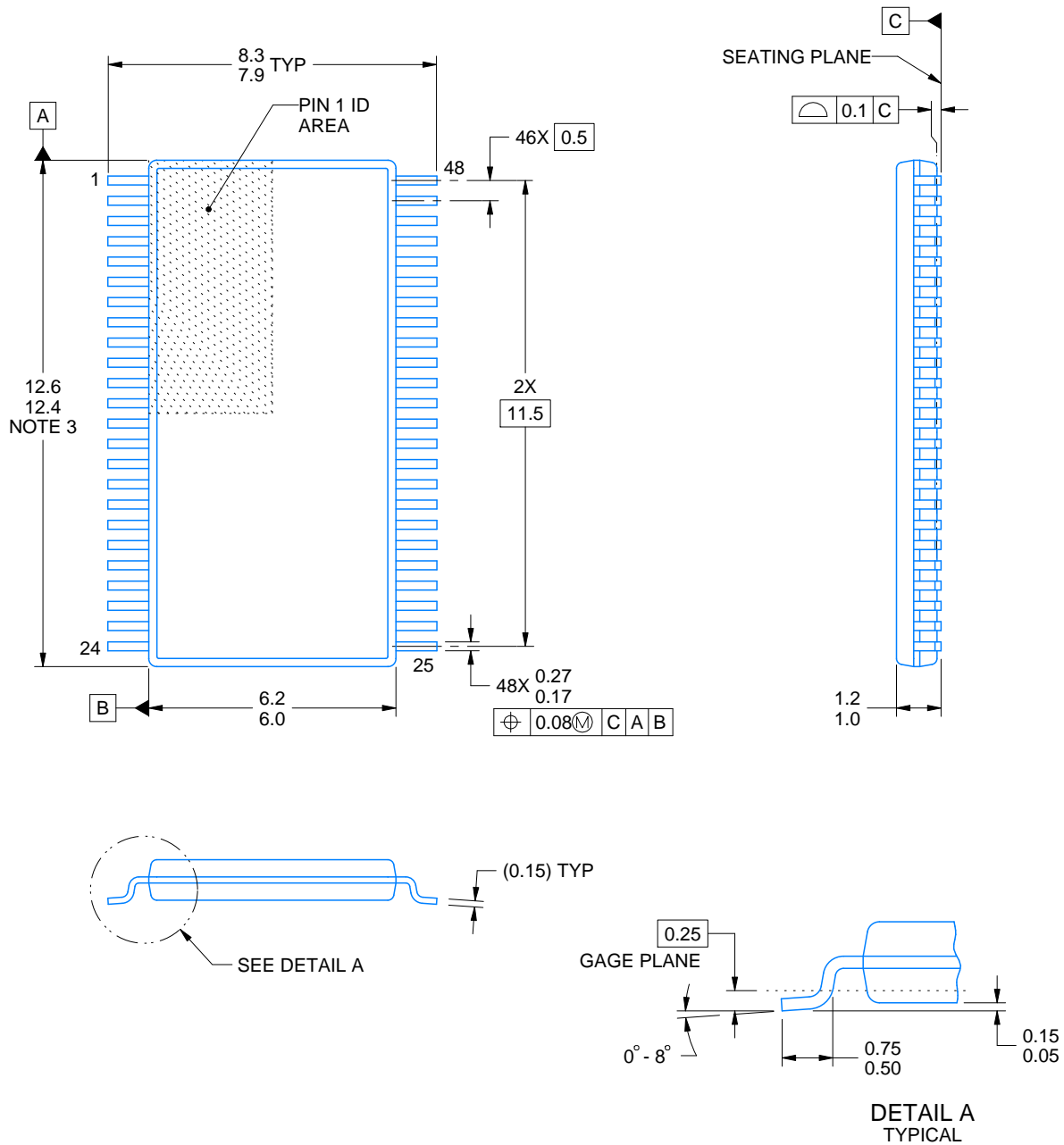
| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS90CF363BMTX/NOPB | TSSOP        | DGG             | 48   | 1000 | 356.0       | 356.0      | 45.0        |

## TUBE



\*All dimensions are nominal

| Device              | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| DS90CF363BMT/NOPB   | DGG          | TSSOP        | 48   | 38  | 495    | 10     | 2540   | 5.79   |
| DS90CF363BMT/NOPB.A | DGG          | TSSOP        | 48   | 38  | 495    | 10     | 2540   | 5.79   |



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## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

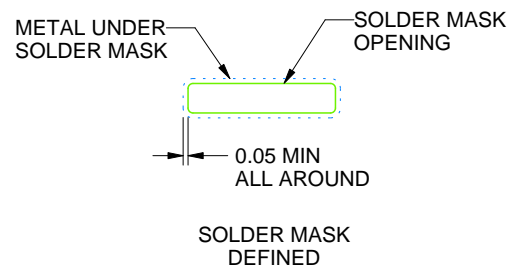
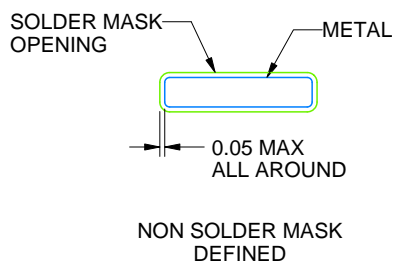
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

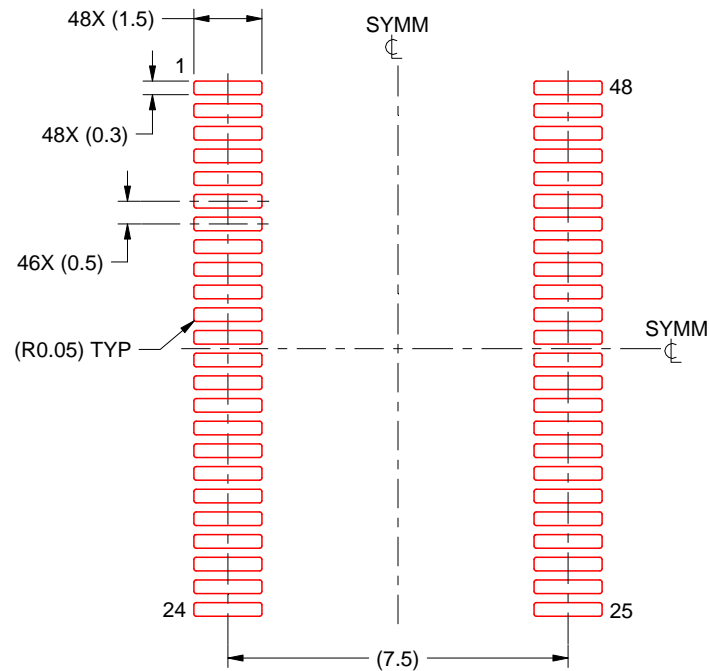


# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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