DS160PR421 PCIe® 4.0 16Gbps 4 チャネル・リニア・リドライバ、2：1 マルチプレクサ 内蔵

1 特長

- 2:1 マルチプレクサを内蔵したクワッド・チャネル PCIe 4.0 リニア・リドライバ / リピータ
- UPI、DisplayPort、SAS、SATA、XFI 互換のプロトコル非依存リニア・ドライバ
- 3.3V 単一電源レール
- 120mW/チャネルの低有効電力
- ヒートシンク不要
- 8GHz で最大 17dB のイコライゼーションを実現し、最大 42dB の PCIe 4.0 チャネルを処理可能
- 入力 -13dB、出力 -15dB の優れた差動反射損失
- 小さい付加ランダム・ジッタ (PRBS データ):70fs
- 短いレイテンシ:80ps
- 自動レシーバ検出機能と、PCIe リンク・トレーニングのシームレスなサポート
- ピン制御または SMBus/I²C によるデバイス構成
- ピンによる マルチプレクサ の選択
- デマルチプレクサ製品 DS160PR412
- -40℃～85℃の接合部温度範囲
- 3.5mm × 9mm 42 ピン、0.5mm ピッチの WQFN パッケージ、

2 アプリケーション

- デスクトップ PC / マザーボード
- ラック・サーバー
- マイクロサーバー / タワー・サーバー
- 高性能コンピューティング
- ハードウェア・アクセラレータ
- ネットワーク接続ストレージ (NAS)
- ストレージ・エリア・ネットワーク (SAN) とホスト・バス・アダプタ (HBA) カード
- ネットワーク・インターフェイス・カード (NIC)

3 概要

DS160PR421 は、4 チャネルのリニア・リドライバで、マルチプレクサ (mux) が内蔵されています。低消費電力高性能リニア・リドライバは、PCIe 4.0 やその他のインターフェイスをサポートするよう設計されています。

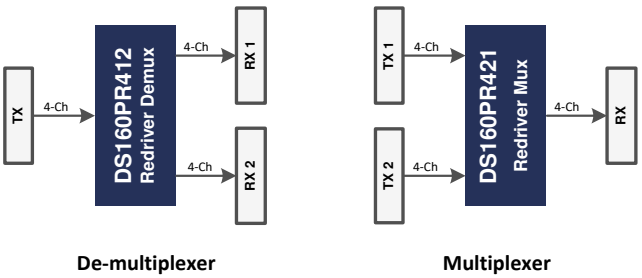
DS160PR421 レシーバは、連続時間リニア・イコライザ (CTLE) を搭載し、高周波数での昇圧を実現しています。イコライザは、相互接続媒体 (例:PCB 配線、ケーブル) に起因する符号間干渉 (ISI) によって完全に閉じた入力アイ・パターンを開くことができます。リニア・リドライバとパッシブ・チャネル全体は、最良の送信 / 受信イコライゼーション設定を実現するためにリンク・トレーニングされており、最良の電気的リンクと可能な限り最小のレイテンシを実現します。チャネル間クロストークが小さく、付加ジッタが小さく、反射損失特性が非常に優れた本デバイスは、リンク内でほとんど受動素子のように振舞います。このデバイスは、内部リニア電圧レギュレータを備えており、高速データ・パス用にクリーンな電源を供給し、基板上の電源ノイズへの高い耐性を実現します。

DS160PR421 は、量産時に高速テストを実施しており、信頼性の高い大量生産に対応しています。また、このデバイスは AC および DC ゲインの変動が小さいため、大容量プラットフォームを展開する際の一貫したイコライゼーションにも対応しています。

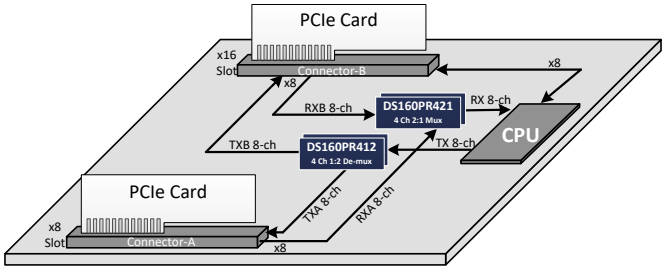
製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
DS160PR421	WQFN (42)	3.5mm × 9mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



De-multiplexer　　Multiplexer



PCIe Lane Muxing

アプリケーション使用事例

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
February 2021	*	Initial release

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5 Pin Configuration and Functions

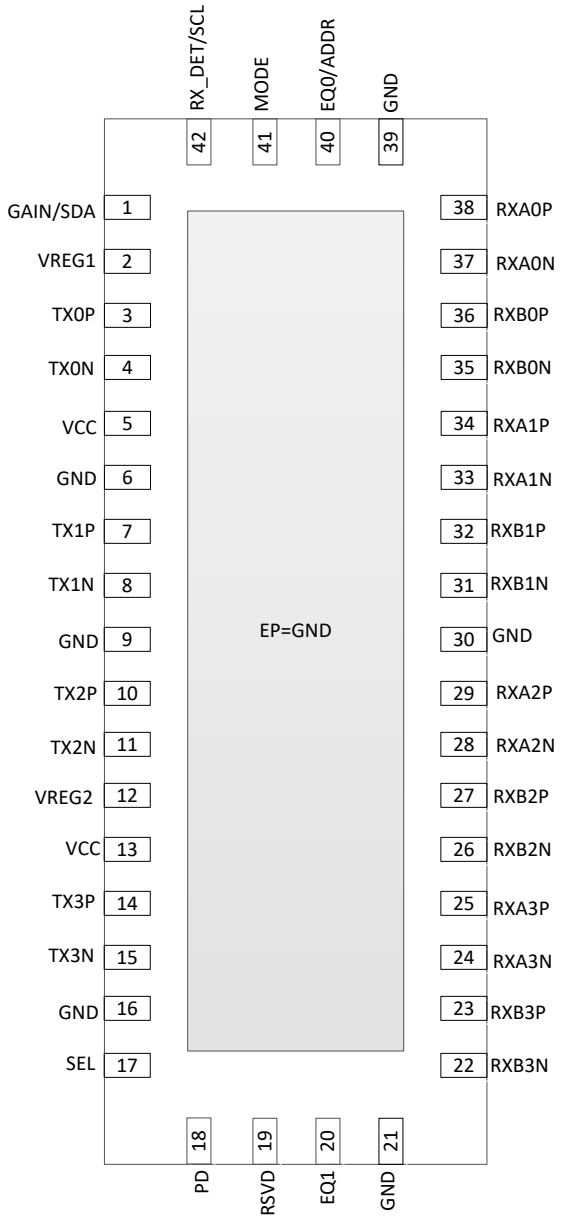

図 5-1. RUA Package 42-Pin WQFN Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
MODE	41	I, 4-level	Sets device control configuration modes. 4-level IO pin as defined in 表 7-3. The pin can be exercised at device power up or in normal operation mode. L0: **Pin Mode** – device control configuration is done solely by strap pins. L1 or L2: **SMBus/I²C Slave Mode** – device control configuration is done by an external controller with SMBus/I²C master. This pin along with ADDR pin sets devices slave address. L3 (Float): RESERVED – TI internal test mode.
EQ0 /ADDR	40	I, 4-level	In **Pin Mode:** The EQ0 and EQ1 pins sets receiver linear equalization CTLE (AC gain) for all channels according to 表 7-1. These pins are sampled at device power-up only. In **SMBus/I²C Mode:** The ADDR pin in conjunction with MODE pin sets SMBus / I²C slave address according to 表 7-4. The pin is sampled at device power-up only.
EQ1	20	I, 4-level	
GAIN /SDA	1	I, 4-level / IO	**In Pin Mode**: DC gain (broadbad gain including high frequency) from the input to the output of the device for all channels. Note the device also provides AC (high frequency) gain in the form of equalization controlled by EQ pins or SMBus/I²C registers. **In SMBus/I²C Mode**: 3.3 V SMBus/I²C data. External pullup resistor such as 4.7 kΩ required for operation.
GND	EP, 6, 9, 16, 21, 30, 39	P	Ground reference for the device. EP: the Exposed Pad at the bottom of the QFN package. It is used as the GND return for the device. The EP should be connected to ground plane(s) through low resistance path. A via array provides a low impedance path to GND. The EP also improves thermal dissipation.
RSVD	19	O	TI internal test pin. Keep no connect.
PD	18	I, 3.3-V LVCMOS	2-level logic controlling the operating state of the redriver. Active in both **Pin Mode** and **SMBus/I²C Mode**. The pin is used part of PCIe RX_DET state machine as outlined in 表 7-2. High: Power down for all channels Low: Power up, normal operation for all channels
RX_DET /SCL	42	I, 4-level / IO	In **Pin Mode:** Sets receiver detect state machine options according to 表 7-2. The pin is sampled at device power-up only. In **SMBus/I²C Mode:** 3.3 V SMBus/I²C clock. External pullup resistor such as 4.7 kΩ required for operation.
RXA0N	37	I	Inverting differential RX input – Port A, Channel 0.
RXA0P	38	I	Noninverting differential RX input – Port A, Channel 0.
RXA1N	33	I	Inverting differential RX input – Port A, Channel 1.
RXA1P	34	I	Noninverting differential RX input – Port A, Channel 1.
RXA2N	28	I	Inverting differential RX input – Port A, Channel 2.
RXA2P	29	I	Noninverting differential RX input – Port A, Channel 2.
RXA3N	24	I	Inverting differential RX input – Port A, Channel 3.
RXA3P	25	I	Noninverting differential RX input – Port A, Channel 3.
RXB0N	35	I	Inverting differential RX input – Port B, Channel 0.
RXB0P	36	I	Noninverting differential RX input – Port B, Channel 0.
RXB1N	31	I	Inverting differential RX input – Port B, Channel 1.
RXB1P	32	I	Noninverting differential RX input – Port B, Channel 1.
RXB2N	26	I	Inverting differential RX input – Port B, Channel 2.
RXB2P	27	I	Noninverting differential RX input – Port B, Channel 2.
RXB3N	22	I	Inverting differential RX input – Port B, Channel 3.
RXB3P	23	I	Noninverting differential RX input – Port B, Channel 3.

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表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SEL	17	I, 3.3 V LVCMOS	Selects the mux path. Active in both **Pin Mode** and **SMBus/I²C Mode**. Note the SEL pin must be exercised in system implementations for mux selection between Port A vs Port B. The pin is used part of PCIe RX_DET state machine as outlined in 表 7-2. L: Port A selected. H: Port B selected.
TX0N	4	O	Inverting differential TX output, Channel 0.
TX0P	3	O	Noninverting differential TX output, Channel 0.
TX1N	8	O	Inverting differential TX output, Channel 1.
TX1P	7	O	Noninverting differential TX output, Channel 1.
TX2N	11	O	Inverting differential TX output, Channel 2.
TX2P	10	O	Noninverting differential TX output, Channel 2.
TX3N	15	O	Inverting differential TX output, Channel 3.
TX3P	14	O	Noninverting differential TX output, Channel 3.
VCC	5, 13	P	Power supply, VCC = 3.3 V ± 10%. The VCC pins on this device should be connected through a low-resistance path to the board VCC plane.
VREG1	2	P	Internal regulator output. Must add decoupling capacitor of 0.22 µF near the pin. Do not route the pin beyond the decoupling capacitor. Do not connect to VREG2. Do not use as a power supply for any other component on the board.
VREG2	12	P	Internal regulator output. Must add decoupling caps of 0.22 µF near the pin. Do not route the pin beyond the decoupling capacitor. Do not connect to VREG1. Do not use as a power supply for any other component on the board.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC_{ABSMAX}	Supply Voltage (VCC)	–0.5	4.0	V
$VIO_{CMOS,ABSMAX}$	3.3 V LVCMOS and Open Drain I/O voltage	–0.5	4.0	V
$VIO_{4LVL,ABSMAX}$	4-level Input I/O voltage	–0.5	2.75	V
$VIO_{HS-RX,ABSMAX}$	High-speed I/O voltage (RXnP, RXnN)	–0.5	3.2	V
$VIO_{HS-TX,ABSMAX}$	High-speed I/O voltage (TXnP, TXnN)	–0.5	2.75	V
$T_{J,ABSMAX}$	Junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage, VCC to GND	DC plus AC power should not exceed these limits	3.0	3.3	3.6	V
N_{VCC}	Supply noise tolerance[1]	DC to <50 Hz, sinusoidal			250	mVpp
		50 Hz to 500 kHz, sinusoidal			100	mVpp
		500 kHz to 2.5 MHz, sinusoidal			33	mVpp
		>2.5 MHz, sinusoidal			10	mVpp
$T_{RampVCC}$	VCC supply ramp time	From 0 V to 3.0 V	0.150		100	ms
T_J	Operating junction temperature		–40		125	°C
T_A	Operating ambient temperature		–40		85	°C
PW_{LVCMOS}	Minimum pulse width required for the device to detect a valid signal on LVCMOS inputs	PD, SEL	200			uS
VCC_{SMBUS}	SMBus/I²C SDA and SCL Open Drain Termination Voltage	Supply voltage for open drain pull-up resistor			3.6	V
F_{SMBus}	SMBus/I²C clock (SCL) frequency in SMBus slave mode		10		400	kHz
VID_{LAUNCH}	Source differential launch amplitude		800		1200	mVpp

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6.4 Thermal Information

THERMAL METRIC[1]		DS160PR421 RUA, 42 Pins	UNIT
$R_{\theta JA\text{-}High\ K}$	Junction-to-ambient thermal resistance	26.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report.

6.5 DC Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
$POWER_{CH}$	Active power **per channel**	GAIN1/0 = L3		120		mW
		GAIN1/0 = L0		110		mW
I_{ACTIVE}	Device current consumption when four channels are active	GAIN1/0 = L3, PD = L		145	190	mA
I_{STBY}	Device current consumption in standby power mode	All channels disabled (PD = H)		30	45	mA
V_{REG}	Internal regulator output			2.5		V
Control IO						
V_{IH}	High level input voltage	SDA, SCL, PD, SEL pins	2.1			V
V_{IL}	Low level input voltage	SDA, SCL, PD, SEL pins			1.08	V
V_{OH}	High level output voltage	$R_{pull\text{-}up}$ = 4.7 kΩ (SDA, SCL pins)	2.1			V
V_{OL}	Low level output voltage	I_{OL} = –4 mA (SDA, SCL pins)			0.4	V
$I_{IH,SEL}$	Input high leakage current for SEL pin	V_{Input} = VCC			80	µA
I_{IH}	Input high leakage current	V_{Input} = VCC, (SCL, SDA, PD pins)			10	µA
I_{IL}	Input low leakage current	V_{Input} = 0 V, (SCL, SDA, PD, SEL pins)	-10			µA
$I_{IH,FS}$	Input high leakage current for fail safe input pins	V_{Input} = 3.6 V, VCC = 0 V, (SCL, SDA, PD, SEL pins)			200	µA
$C_{IN\text{-}CTRL}$	Input capacitance	SDA, SCL, PD, SEL pins		1.5		pF
4 Level IOs (MODE, GAIN, EQ0, EQ1, RX_DET pins)						
I_{IH_4L}	Input high leakage current, 4 level IOs	VIN = 2.5 V			10	µA
I_{IL_4L}	Input low leakage current for all 4 level IOs except MODE.	VIN = GND	-10			µA
$I_{IL\_4L,MODE}$	Input low leakage current for MODE pin	VIN = GND	-200			µA
Receiver						
$V_{RX\text{-}DC\text{-}CM}$	RX DC Common Mode (CM) Voltage	Device is in active or standby state		2.5		V
$Z_{RX\text{-}DC}$	Rx DC Single-Ended Impedance			50		Ω
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$	DC input CM input impedance during Reset or power-down	Inputs are at CM voltage	20			kΩ
Transmitter						
$Z_{TX\text{-}DIFF\text{-}DC}$	DC Differential Tx Impedance	Impedance of Tx during active signaling, VID,diff = 1Vpp		100		Ω

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over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TX-DC-CM}$	Tx DC common mode Voltage			0.75		V
$I_{TX-SHORT}$	Tx Short Circuit Current	Total current the Tx can supply when shorted to GND			90	mA

6.6 High Speed Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver						
$RL_{RX-DIFF}$	Input differential return loss	50 MHz to 1.25 GHz		-25		dB
		1.25 GHz to 2.5 GHz		-22		dB
		2.5 GHz to 4.0 GHz		-21		dB
		4.0 GHz to 8.0 GHz		-14		dB
XT_{RX}	Receive-side pair-to-pair isolation	Pair-to-pair isolation (SDD21) between two adjacent active receiver pairs from 10 MHz to 8 GHz.		-47		dB
Transmitter						
$V_{TX-AC-CM-PP}$	Tx AC Peak-to-Peak Common Mode Voltage	Measured with lowest EQ, GAIN = L3; PRBS-7, 16 Gbps, over at least 10^6 bits using a bandpass-Pass Filter from 30 Khz - 500 Mhz			50	mVpp
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle	$V_{TX-CM-DC} = \lvert V_{OUTn+} + V_{OUTn-}\rvert/2$, Measured by taking the absolute difference of $V_{TX-CM-DC}$ during PCIe state L0 and Electrical Idle	0		100	mV
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between V_{OUTn+} and V_{OUTn-} during L0	Measured by taking the absolute difference of V_{OUTn+} and V_{OUTn-} during PCIe state L0			10	mV
$V_{TX-IDLE-DIFF-AC-p}$	AC Electrical Idle Differential Output Voltage	Measured by taking the absolute difference of V_{OUTn+} and V_{OUTn-} during Electrical Idle, Measured with a band-pass filter consisting of two first-order filters. The High-Pass and Low-Pass -3-dB bandwidths are 10 kHz and 1.25 GHz, respectively - zero at input	0		10	mV
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Output Voltage	Measured by taking the absolute difference of V_{OUTn+} and V_{OUTn-} during Electrical Idle, Measured with a first-order Low-Pass Filter with –3-dB bandwidth of 10 kHz	0		5	mV
$V_{TX-RCV-DETECT}$	Amount of Voltage change allowed during Receiver Detection	Measured while Tx is sensing whether a low-impedance Receiver is present. No load is connected to the driver output	0		600	mV
$RL_{TX-DIFF}$	Output differential return loss	50 MHz to 1.25 GHz		-20		dB
		1.25 GHz to 2.5 GHz		-18		dB
		2.5 GHz to 4.0 GHz		-18		dB
		4.0 GHz to 8.0 GHz		-16		dB
XT_{TX}	Transmit-side pair-to-pair isolation	Minimum pair-to-pair isolation (SDD21) between two adjacent active transmitter pairs from 10 MHz to 8 GHz.		-48		dB
Device Datapath						
$T_{PLHD/PHLD}$	Input-to-output latency (propagation delay) through a data channel	For either Low-to-High or High-to-Low transition		80	110	ps

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over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	Between any two lanes within a single transmitter.	-20		20	ps
$T_{RJ-DATA}$	Additive Random Jitter with data	Difference between through redriver and baseline setup. 16Gbps PRBS15. Minimal input/output channels. Minimum EQ. 800 mVpp-diff input swing.		70		fs
$T_{RJ-INTRINSIC}$	Intrinsic additive Random Jitter with clock	Difference between through redriver and baseline setup. 8 Ghz CK. Minimal input/output channels. Minimum EQ. 400 mVpp-diff input swing.		90		fs
$JITTER_{TOTAL-DATA}$	Additive Total Jitter with data	Difference between through redriver and baseline setup. 16 Gbps PRBS15. Minimal input/output channels. Minimum EQ. 800 mVpp-diff input swing.		4		ps
$JITTER_{TOTAL-INTRINSIC}$	Intrinsic additive Total Jitter with clock	Difference between through redriver and baseline setup. 8 Ghz CK. Minimal input/output channels. Minimum EQ. 800 mVpp-diff input swing.		1		ps
DCGAIN	DC flat gain input to output	Minimum EQ, GAIN = L0		-4.2		dB
		Minimum EQ, GAIN = L1		-1.8		dB
		Minimum EQ, GAIN = L2		0.25		dB
		Minimum EQ, GAIN = L3 (Float)		2.0		dB
$EQ-MAX_{8G}$	EQ boost at max setting (EQ INDEX = 15)	AC gain at 8 GHz relative to gain at 100 MHz.		17		dB
$DCGAIN_{VAR}$	DC gain variation	GAIN = L2, minimum EQ setting. Max-Min.	-2.3		1.7	dB
$EQGAIN_{VAR}$	EQ boost variation	At 8 Ghz. GAIN1/0 = L2, maximum EQ setting. Max-Min.	-3.3		3.7	dB
LIN_{DC}	Output DC Linearity	GAIN = L3 (defauult). 128T pattern at 2.5 Gbps.		1000		mVpp
LIN_{AC}	Output AC Linearity	GAIN = L3 (default). 1T pattern at 16 Gbps.		750		mVpp

6.7 SMBUS/I2C Timing Charateristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Slave Mode						
t_{SP}	Pulse width of spikes which must be suppressed by the input filter				50	ns
t_{HD-STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated		0.6			µs
t_{LOW}	LOW period of the SCL clock		1.3			µs
T_{HIGH}	HIGH period of the SCL clock		0.6			µs
t_{SU-STA}	Set-up time for a repeated START condition		0.6			µs
t_{HD-DAT}	Data hold time		0			µs
T_{SU-DAT}	Data setup time		0.1			µs
t_r	Rise time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10pF		120		ns

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_f	Fall time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10pF		2		ns
t_{SU-STO}	Set-up time for STOP condition		0.6			µs
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
t_{VD-DAT}	Data valid time				0.9	µs
t_{VD-ACK}	Data valid acknowledge time				0.9	µs
C_b	capacitive load for each bus line				400	pF

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6.8 Typical Characteristics

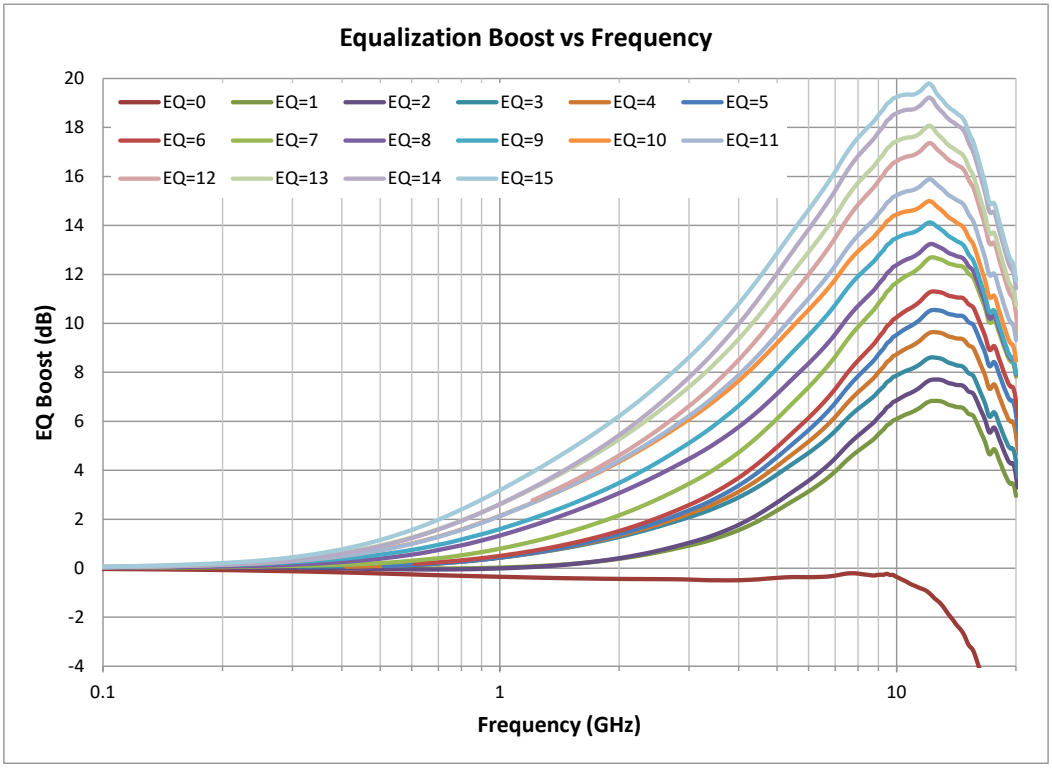

図 6-1. Typical EQ Boost vs Frequency

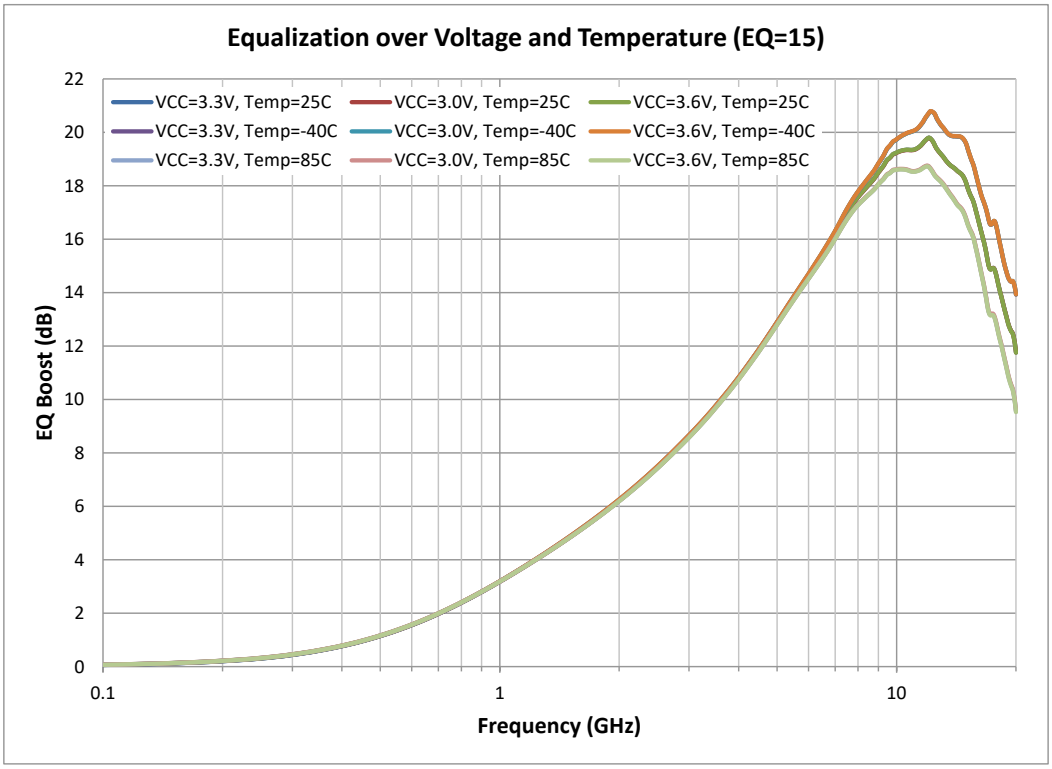

図 6-2. Typical EQ Boost over Voltage and Temperature with EQ=15

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6.8 Typical Characteristics

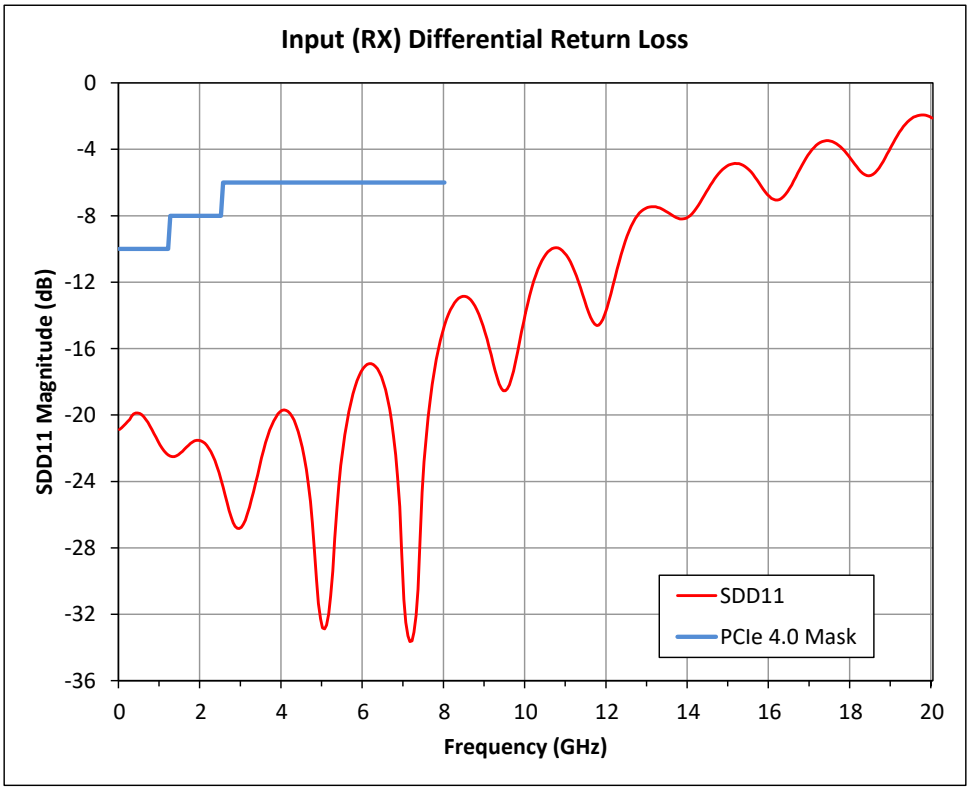

図 6-3. Typical RX Differential Return Loss

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6.8 Typical Characteristics

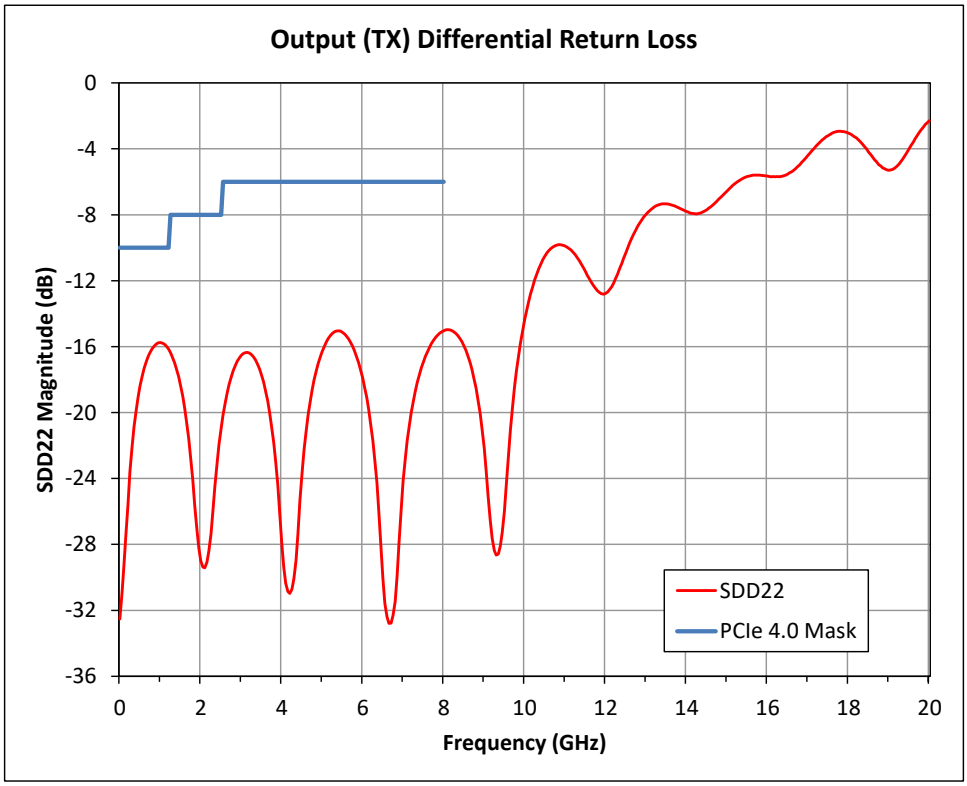

図 6-4. Typical TX Differential Return Loss

6.8 Typical Characteristics

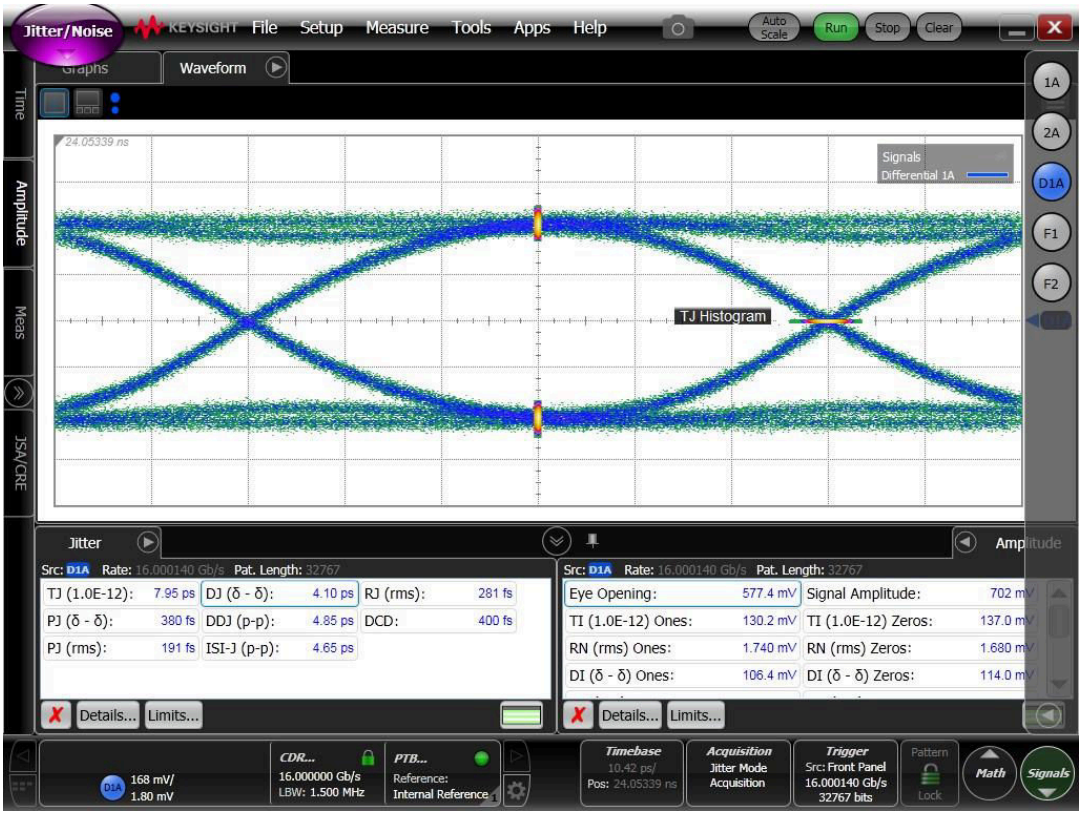

図 6-5. Typical Jitter Characteristics - Top: 16Gbps PRBS15 Input to the Device, Bottom: Output of the Device.

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7 Detailed Description

7.1 Overview

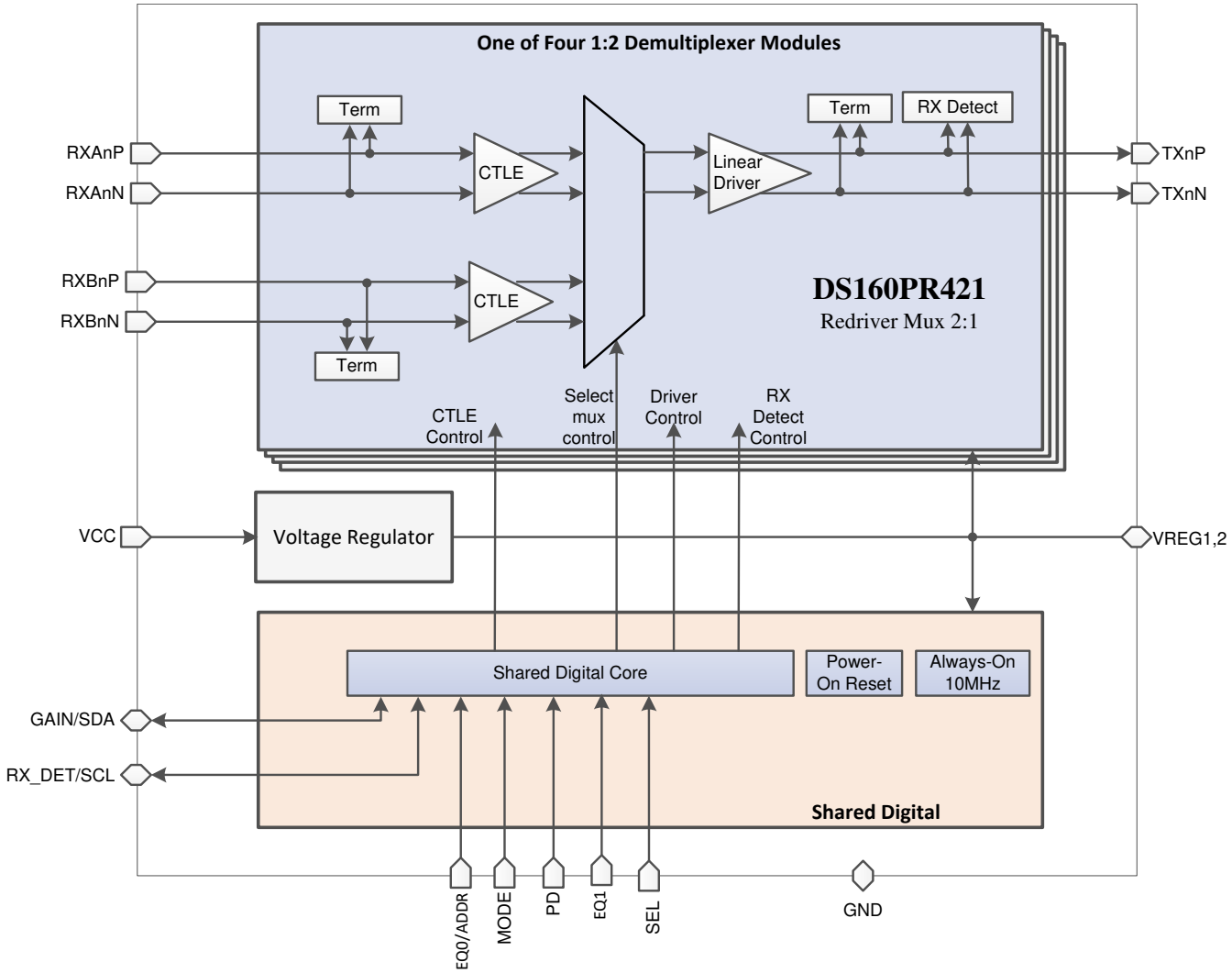
The DS160PR421 is a four channel linear redriver with ingrated multiplexer (mux). The low-power high-performance linear repeater or redriver is designed to support PCIe 1.0/2.0/3.0/4.0. The device is a protocol agnostic linear redriver that can operate for interfaces up to 16 Gbps.

The DS160PR421 can be configured two different ways:

Pin Mode – device control configuration is done solely by strap pins. Pin mode is expected to be good enough for many system implementation needs.

SMBus/I^{2}C Slave Mode - provides most flexibility. Requires a SMBus/I^{2}C master device to configure DS160PR421 though writing to its slave address.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Linear Equalization

The DS160PR421 receivers feature a continuous-time linear equalizer (CTLE) that applies high-frequency boost to help equalize the frequency-dependent insertion loss effects of the passive channel. 表 7-1 shows available equalization boost through EQ control pins (EQ1 and EQ0), when in Pin Control mode (MODE = L0).

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表 7-1. Equalization Control Settings

EQUALIZATION SETTING			TYPICAL EQ BOOST (dB)	
EQ INDEX	EQ1	EQ0	@ 4 GHz	@ 8 GHz
0	L0	L0	0.0	-0.1
1	L0	L1	1.5	4.5
2	L0	L2	2.0	5.5
3	L0	L3	2.5	6.5
4	L1	L0	2.7	7.0
5	L1	L1	3.0	8.0
6	L1	L2	4.0	9.0
7	L1	L3	5.0	10.0
8	L2	L0	6.0	11.0
9	L2	L1	7.0	12.0
10	L2	L2	7.5	12.5
11	L2	L3	8.0	13.0
12	L3	L0	8.5	14.0
13	L3	L1	9.5	15.0
14	L3	L2	10.0	16.0
15	L3	L3	11.0	17.0

The equalization of the device can also be set by writing to SMBus/I^{2}C registers in slave mode. Refer to the *DS160PR412/421 Programming Guide* for details.

7.3.2 Flat Gain

The GAIN pin can be used to set the overall datapath flat gain (broadbabd gain including high frequency) of the DS160PR421 when the device is in Pin Mode. The default recommendation for most systems will be GAIN = L3 (float).

The flat gain and equalization of the DS160PR421 must be set such that the output signal swing at DC and high frequency does not exceed the DC and AC linearity ranges of the devices, respectively.

Note the device also provides AC (high frequency) gain in the form of equalization controlled by EQ pins or SMBus/I^{2}C registers.

7.3.3 Receiver Detect State Machine

The DS160PR421 deploys an RX detect state machine that governs the RX detection cycle as defined in the PCI express specifications. At device power up or through manually triggered event using PD or SEL pin or writing to the relevant I^{2}C/SMBus register, the redriver determines whether or not a valid PCI express termination is present at the far end of the link. The RX_DET pin of DS160PR421 provides additional flexibility for system designers to appropriately set the device in desired mode according to 表 7-2. For the PCIe application the RX_DET pin can be left floating for default settings.

Note power up ramp or PD/SEL event triggers RX detect for all four channels. In applications where DS160PR421 channels are used for multiple PCIe links, the RX detect function can be performed for individual channels through writing in appropriate I^{2}C/SMBus registers.

表 7-2. Receiver Detect State Machine Settings

PD	RX_DET	RX Common-mode Impedance	COMMENTS
L	L0	Always 50 Ω	PCI Express RX detection state machine is disabled. Recommended for non PCIe interface use case where the DS160PR421 is used as buffer with equalization.
L	L3 (Float)	Pre Detect: Hi-Z Post Detect: 50 Ω.	TX polls every ≈150 µs until valid termination is detected. RX CM impedance held at Hi-Z until detection Reset by asserting PD high for 200 µs then low.

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表 7-2. Receiver Detect State Machine Settings (continued)

PD	RX_DET	RX Common-mode Impedance	COMMENTS
H	X	Hi-Z	Reset Channels and set their RX impedance to Hi-Z

7.4 Device Functional Modes

7.4.1 Active PCIe Mode

The device is in normal operation with PCIe state machine enabled by RX_DET = L3 (float). This mode is recommended for PCIe use cases. In this mode PD pin is driven low in a system (for example by PCIe connector "PRSNT" signal). In this mode, the device redrives and equalizes PCIe RX or TX signals to provide better signal integrity.

7.4.2 Active Buffer Mode

The device is in normal operation with PCIe state machine disabled by RX_DET = L0. This mode is recommended for non-PCIe use cases. In this mode the device is working as a buffer to provide linear equalization to improve signal integrity.

7.4.3 Standby Mode

The device is in standby mode invoked by PD = H. In this mode, the device is in standby mode conserving power.

7.5 Programming

7.5.1 Control and Configuration Interface

7.5.1.1 Pin Mode

The DS160PR421 can be fully configured through pin-strap pins. In this mode the device uses 2-level and 4-level pins for device control and signal integrity optimum settings.

7.5.1.1.1 Four-Level Control Inputs

The DS160PR421 has five (EQ0, EQ1, GAIN, MODE, and RX_DET) 4-level inputs pins that are used to control the configuration of the device. These 4-level inputs use a resistor divider to help set the 4 valid levels and provide a wider range of control settings. External resistors must be of 10% tolerance or better. The EQ0, EQ1, GAIN, and RX_DET pins are sampled at power-up only. The MODE pin can be exercised at device power up or in normal operation mode.

表 7-3. 4-Level Control Pin Settings

LEVEL	SETTING
L0	1 kΩ to GND
L1	13 kΩ to GND
L2	59 kΩ to GND
L3	F (Float)

7.5.1.2 SMBUS/I²C Register Control Interface

If MODE = L2 (SMBus / I²C slave control mode), the DS160PR421 is configured for best signal integrity through a standard I²C or SMBus interface that may operate up to 400 kHz. The slave address of the DS160PR421 is determined by the pin strap settings on the ADDR and MODE pins. The eight possible slave addresses (7-bit) for each channel banks of the device are shown in 表 7-4. In SMBus/I²C modes the SCL, SDA pins must be pulled up to a 3.3 V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7 kΩ is a good first approximation for a bus capacitance of 10 pF.

Refer to the *DS160PR412/421 Programming Guide* for details.

表 7-4. SMBUS/I2C Slave Address Settings

MODE	ADDR	7-bit Slave Address Channels 0-1	7-bit Slave Address Channels 2-3
L1	L0	0x18	0x19

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表 7-4. SMBUS/I2C Slave Address Settings (continued)

MODE	ADDR	7-bit Slave Address Channels 0-1	7-bit Slave Address Channels 2-3
L1	L1	0x1A	0x1B
L1	L2	0x1C	0x1D
L1	L3	0x1E	0x1F
L2	L0	0x20	0x21
L2	L1	0x22	0x23
L2	L2	0x24	0x25
L2	L3	0x26	0x27

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS160PR421 is a high-speed linear repeater with integrated mux. The device extends the reach of a differential channels impaired by loss from transmission media like PCBs and cables. It can be deployed in a variety of different systems. The following sections outline typical applications and their associated design considerations.

8.2 Typical Applications

The DS160PR421 is a PCI Express linear redriver that can also be configured as interface agnostic redriver by disabling its RX detect feature. The device can be used in wide range of interfaces including:

- PCI Express
- Ultra Path Interconnect (UPI)
- SATA
- SAS
- Display Port

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8.2.1 PCIe x8 Lane Switching

The DS160PR412 and DS160PR421 and can be used in desktop motherboard applications to switch PCIe lanes from a CPU in to one of the two PCIe CEM connectors. 図 8-1 shows a simplified schematic for the configuration. Two DS160PR412 demultiplex eight TX channels from CPU into one of the two PCIe slots. On the other hand two DS160PR421 multiplex eight RX channels from one of the two PCIe slots to CPU.

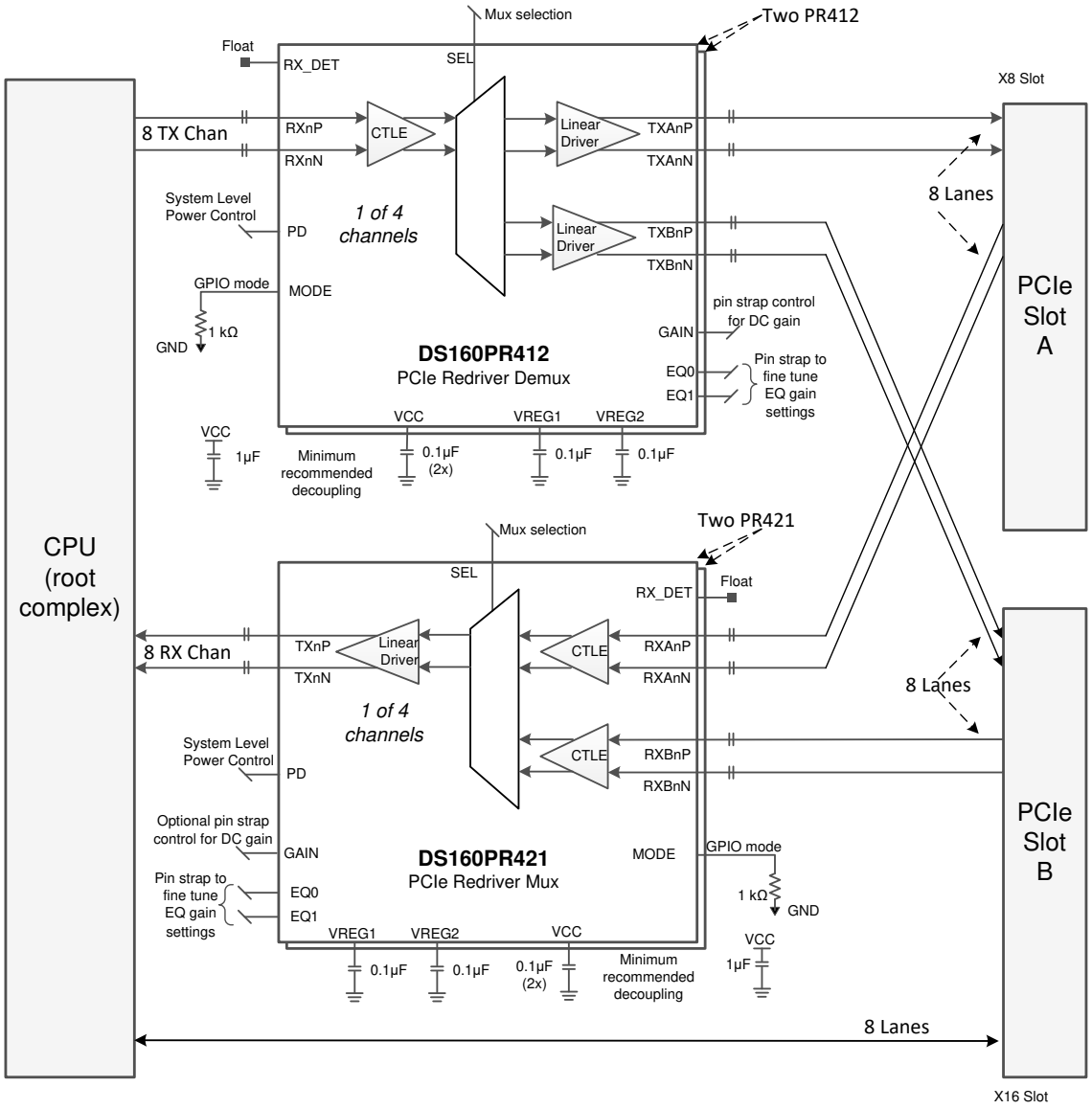

図 8-1. Simplified Schematic for PCIe Lane Switching for PC Desktop Application

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8.2.1.1 Design Requirements

As with any high-speed design, there are many factors which influence the overall performance. The following list indicates critical areas for consideration during design.

- Use 85 Ω impedance traces when interfacing with PCIe CEM connectors. Length matching on the P and N traces should be done on the single-ended segments of the differential pair.
- Use a uniform trace width and trace spacing for differential pairs.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- For Gen 3.0 and Gen 4.0, AC-coupling capacitors of 220 nF are recommended, set the maximum body size to 0402, and add a cutout void on the GND plane below the landing pad of the capacitor to reduce parasitic capacitance to GND.
- Back-drill connector vias and signal vias to minimize stub length.
- Use reference plane vias to ensure a low inductance path for the return current.

8.2.1.2 Detailed Design Procedure

In PCIe Gen 4.0 and Gen 3.0 applications, the specification requires Rx-Tx link training to establish and optimize signal conditioning settings at 16 Gbps and 8 Gbps, respectively. In link training, the Rx partner requests a series of FIR – pre-shoot and de-emphasis coefficients (10 Presets) from the Tx partner. The Rx partner includes 7-levels (6 dB to 12 dB) of CTLE followed by a single tap DFE. The link training would pre-condition the signal, with an equalized link between the root-complex and endpoint.

Note that there is no link training in PCIe Gen 1.0 (2.5 Gbps) or PCIe Gen 2.0 (5.0 Gbps) applications. The DS160PR421 is placed in between the Tx and Rx. It helps extend the PCB trace reach distance by boosting the attenuated signals with its equalization, which allows the user to recover the signal by the downstream Rx more easily.

For operation in Gen 4.0 and Gen 3.0 links, the DS160PR421 transmit outputs are designed to pass the Tx Preset signaling onto the Rx for the PCIe Gen 4.0 or Gen 3.0 link to train and optimize the equalization settings. The suggested setting for the device is GAIN = L3 (default). Adjustments to the EQ setting should be performed based on the channel loss to optimize the eye opening in the Rx partner. The Tx equalization presets or CTLE and DFE coefficients in the Rx can also be adjusted to further improve the eye opening.

8.2.1.3 Pin-to-pin Passive versus Redriver Option

For eight lane PCIe lane muxing application a topology is illustrated where two DS160PR412 and two DS160PR421 are used. There are system use cases where the PCIe link loss is low enough that a signal conditioner such as linear redrivers may not be needed. In such use cases system engineers may consider passive mux to achieve same lane muxing topology. The four channel passive mux/demux TMUXHS4412 is pin-to-pin (p2p) compatible with the DS160PR412 and DS160PR421 . This p2p component availability provides great flexibility for system implementation engineers where the need for redriver is not completely clear. 図 8-2 illustrates p2p passive vs redriver option to implement PCIe lane switching.

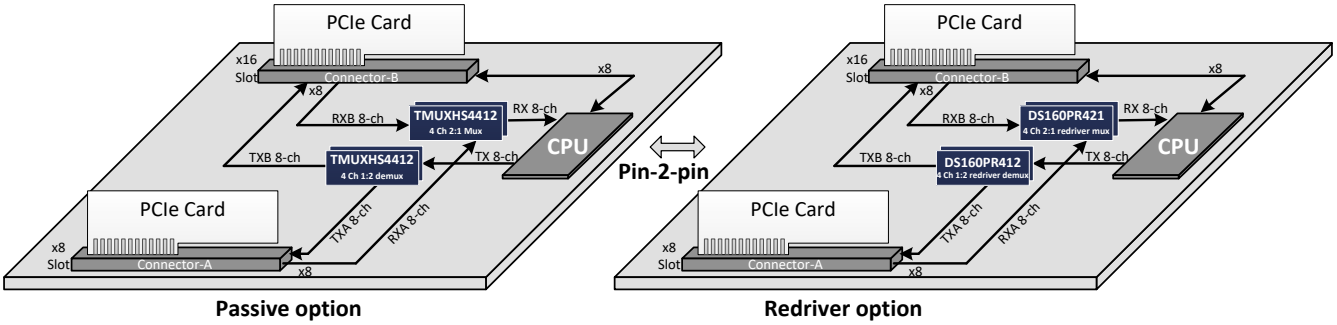

図 8-2. Pin-to-pin passive vs redriver option for PCIe lane switching

8.2.1.4 Application Curves

The DS160PR421 is a linear redriver that can be used to extend channel reach of a PCIe link. Normally, PCIe-compliant TX and RX are equipt with signal-conditioning functions and can handle channel losses of up to 28 dB at 8 GHz. In real implementation the channel reach is often lower. With the DS160PR421 in the link, the total channel loss between a PCIe root complex and an end-point can be extended up to 42 dB at 8 GHz.

図 8-3 shows an electric link that models a single channel of a PCIe link and eye diagrams measured at different locations along the link. The source that models a PCIe Transmitter sends a 16 Gbps PRBS-15 signal with P7 presets. After a transmission channel with –30 dB at 8 GHz insertion loss, the eye diagram is fully closed. The DS160PR421 with its CTLE set to the maximum (17 dB boost) together with the source TX equalization compensates for the losses of the pre-channel (TL1) and opens the eye at the output of the device.

The post-channel (TL2) losses mandate the use of PCIe RX equalization functions such as CTLE and DFE that are normally available in a PCIe-compliant receiver.

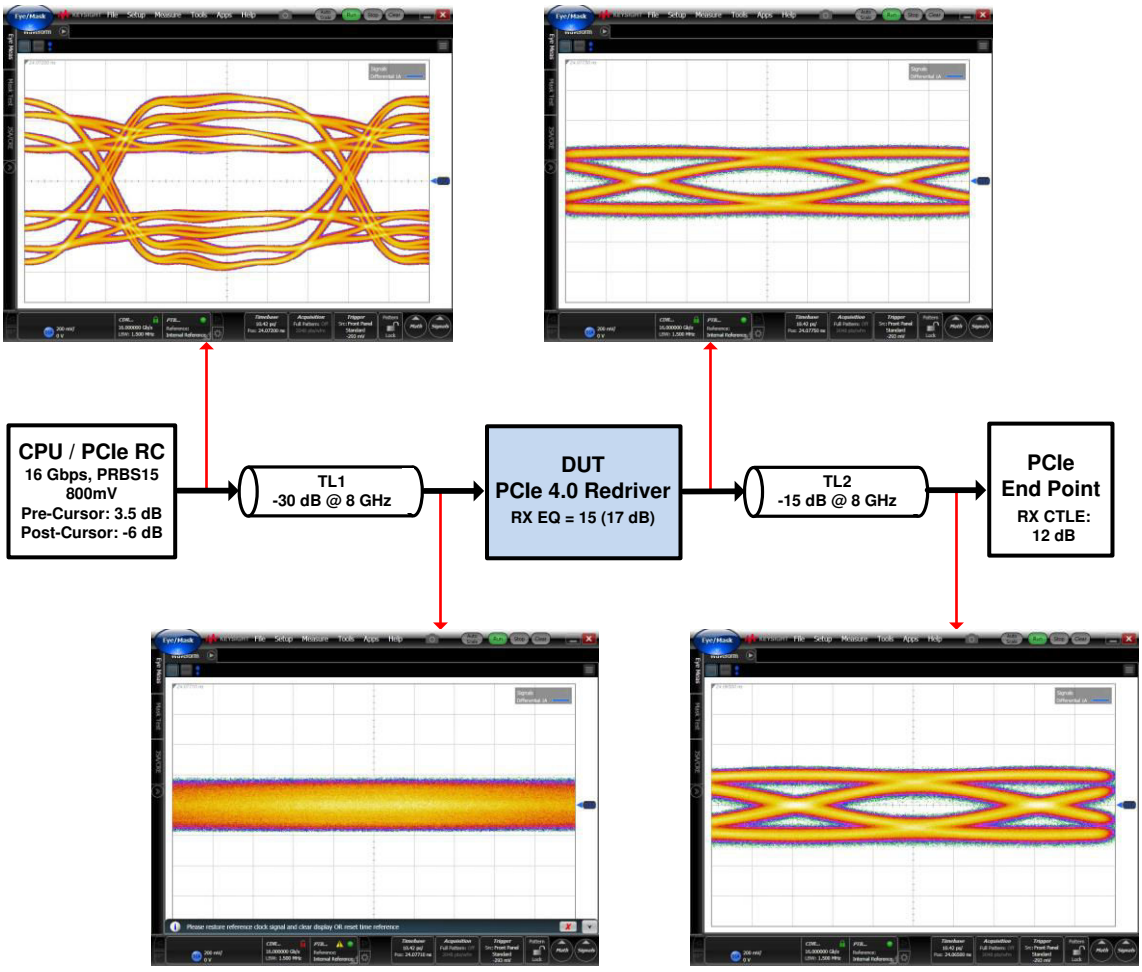

図 8-3. PCIe 4.0 Link Reach Extension Using the DS160PR421

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8.2.2 DisplayPort Application

The DS160PR421 can be used as a four channel DisplayPort (DP) redriver mux for data rates up to 20 Gbps. To use the device in a non-PCIe application, the RX_DET pin must be pin-strapped to GND with 1 kΩ resistor (L0).

The inverted DisplayPort HPD signal can be used to put the device into standby mode by using its PD pin. Note in a DisplayPort link a sink can use HPD line to create an interrupt for its link partner source. If HPD signal is used for power management an RC filter must be installed to filter out HPD interrupt signals.

The device is a linear redriver which is agnostic to DP link training. The DP link training negotiation between a display source and sink stays effective through the device . The redriver becomes part of the electrical channel along with passive traces, cables, and so forth, resulting into optimum source and sink parameters for best electrical link.

図 8-4 shows a simplified schematic for DisplayPort multiplexing application using DS160PR421. Auxiliary and Hot plug detect (HPD) are muxed outside of DS160PR412. If system use case requires implementing DP power states, the device must be controlled by the I^2C or the pin-strap pins.

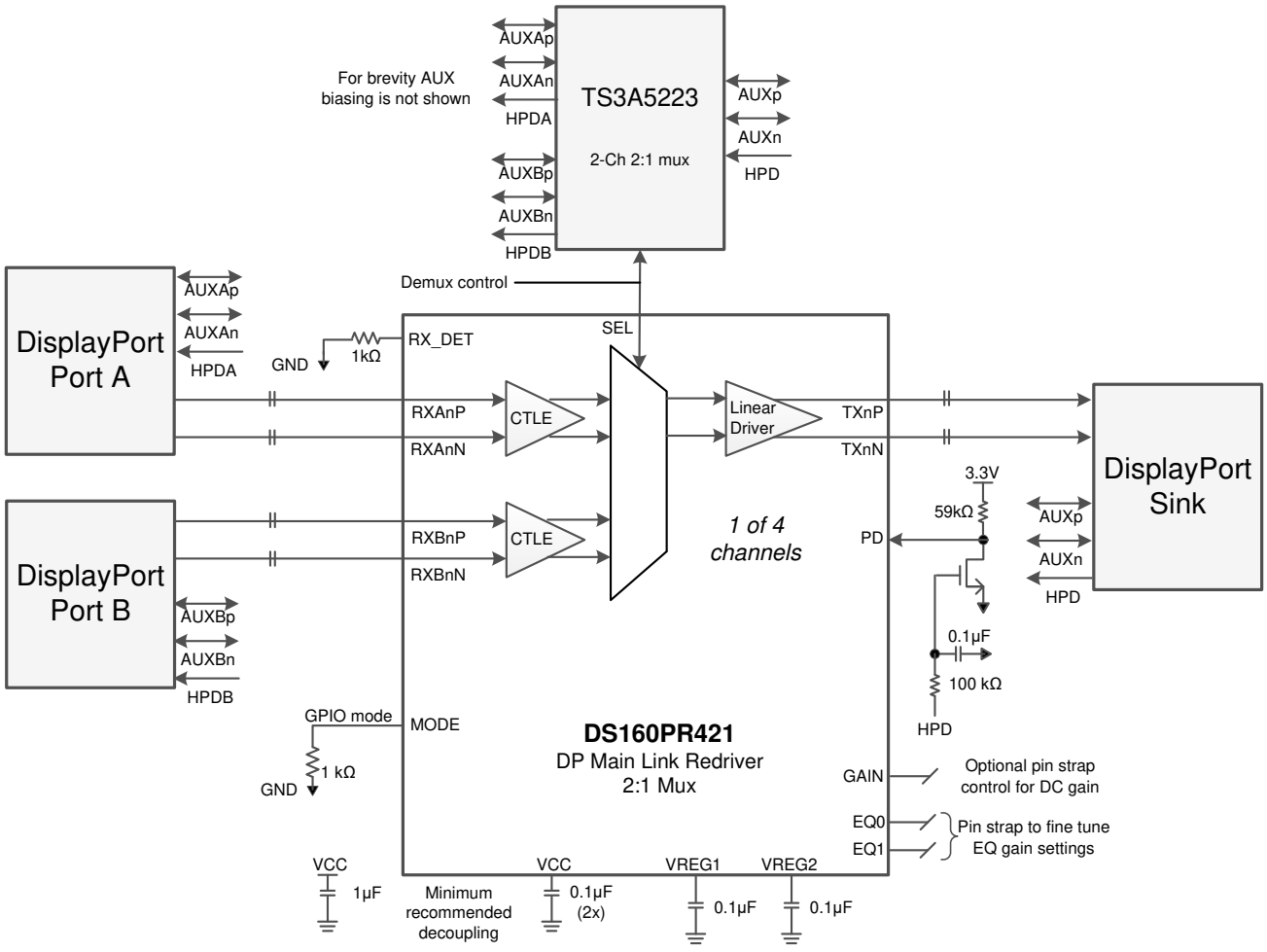

図 8-4. Simplified Schematic for DisplayPort Multiplexer Application

9 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the operating conditions outlined in the recommended operating conditions section in terms of DC voltage, AC noise, and start-up ramp time.
2. The DS160PR421 does not require any special power supply filtering, such as ferrite beads, provided that the recommended operating conditions are met. Only standard supply decoupling is required. Typical supply decoupling consists of a 0.1 µF capacitor per VCC pin, one 1.0 µF bulk capacitor per device, and one 10 µF bulk capacitor per power bus that delivers power to one or more devices. The local decoupling (0.1 µF) capacitors must be connected as close to the VCC pins as possible and with minimal path to the device ground pad.
3. The DS160PR421 voltage regulator output pins require decoupling caps of 0.1 µF near each pins. The regulator is only for internal use. Do not use to provide power to any external component.

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10 Layout

10.1 Layout Guidelines

The following guidelines should be followed when designing the layout:

1. Decoupling capacitors should be placed as close to the VCC pins as possible. Placing the decoupling capacitors directly underneath the device is recommended if the board design permits.
2. High-speed differential signals TXnP/TXnN and RXnP/RXnN should be tightly coupled, skew matched, and impedance controlled.
3. Vias should be avoided when possible on the high-speed differential signals. When vias must be used, take care to minimize the via stub, either by transitioning through most/all layers or by back drilling.
4. GND relief can be used (but is not required) beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. GND vias should be placed directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board.

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11 Layout Example

図 11-1 shows DS320PR421 layout example.

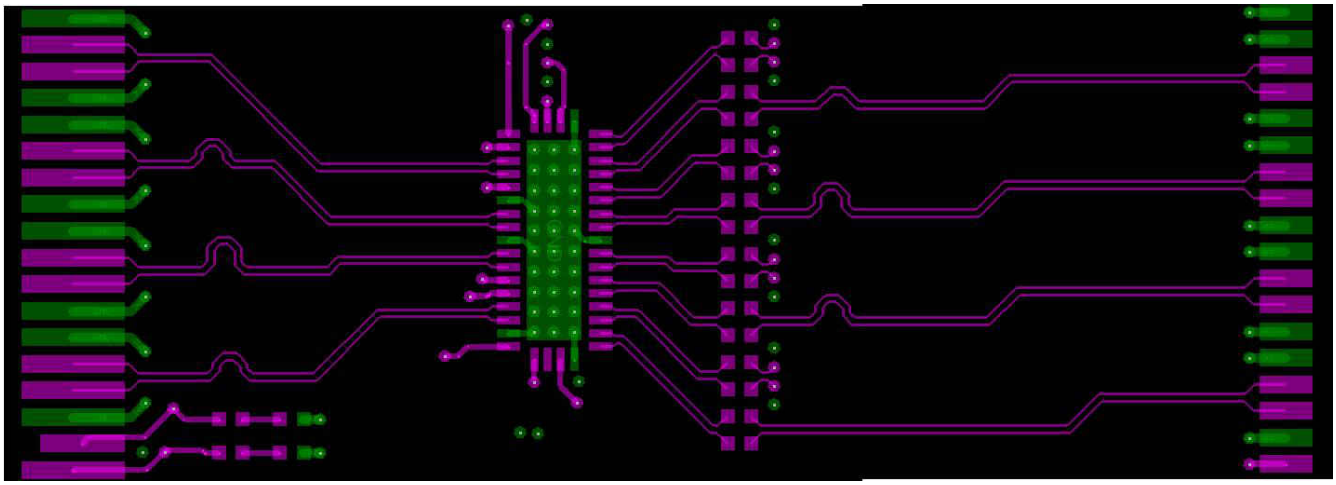

図 11-1. DS320PR421 layout example

図 11-2 shows a layout illustration where two DS320PR412 and two DS320PR421 are used to switch 8 lanes between two PCIe slots.

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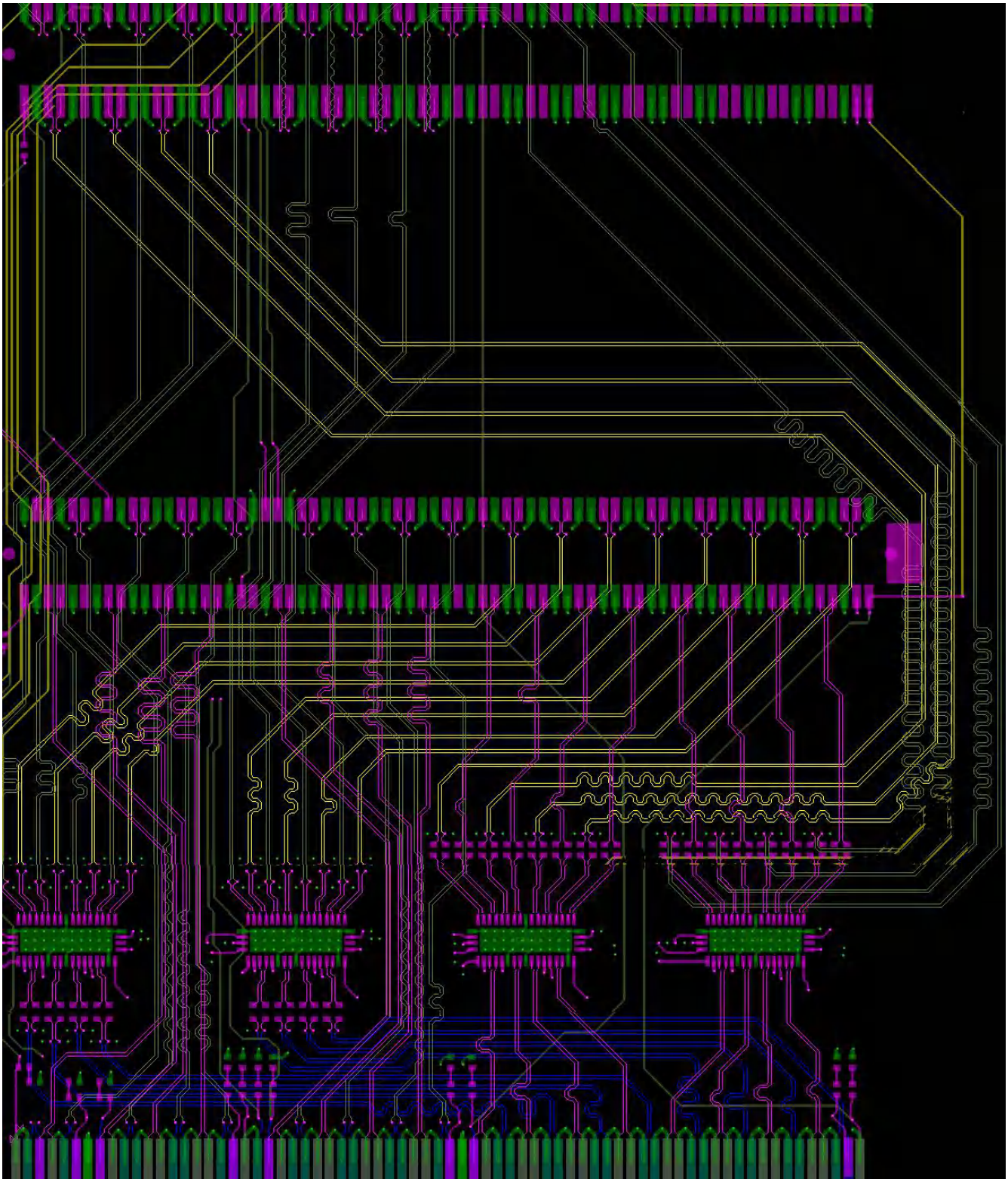

図 11-2. Layout example for PCIe lane muxing application

12 Device and Documentation Support

12.1 ドキュメントの更新通知を受け取る方法

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS160PR421RUAR	Active	Production	WQFN (RUA) | 42	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PR421
DS160PR421RUAR.B	Active	Production	WQFN (RUA) | 42	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
DS160PR421RUAT	Active	Production	WQFN (RUA) | 42	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PR421
DS160PR421RUAT.B	Active	Production	WQFN (RUA) | 42	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

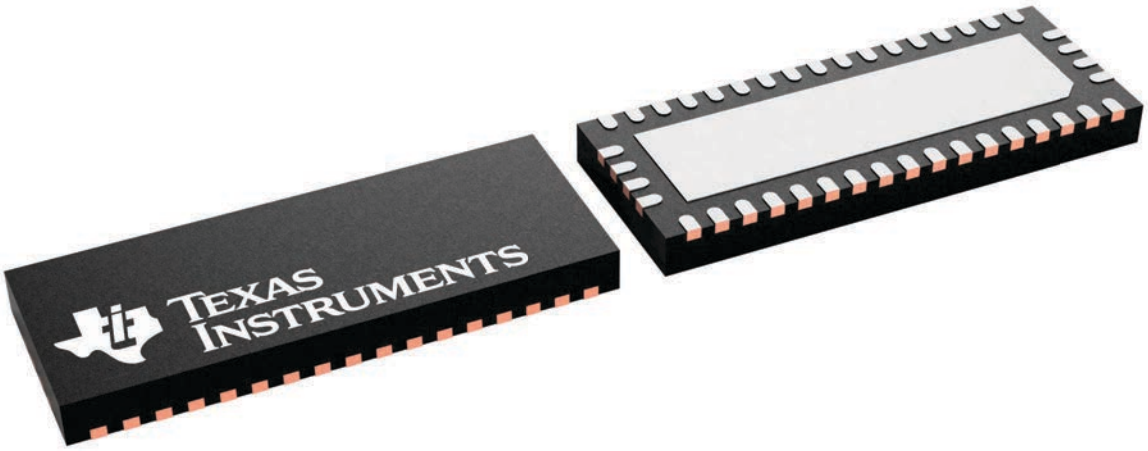
RUA 42

WQFN - 0.8 mm max height

9 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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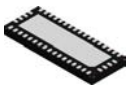
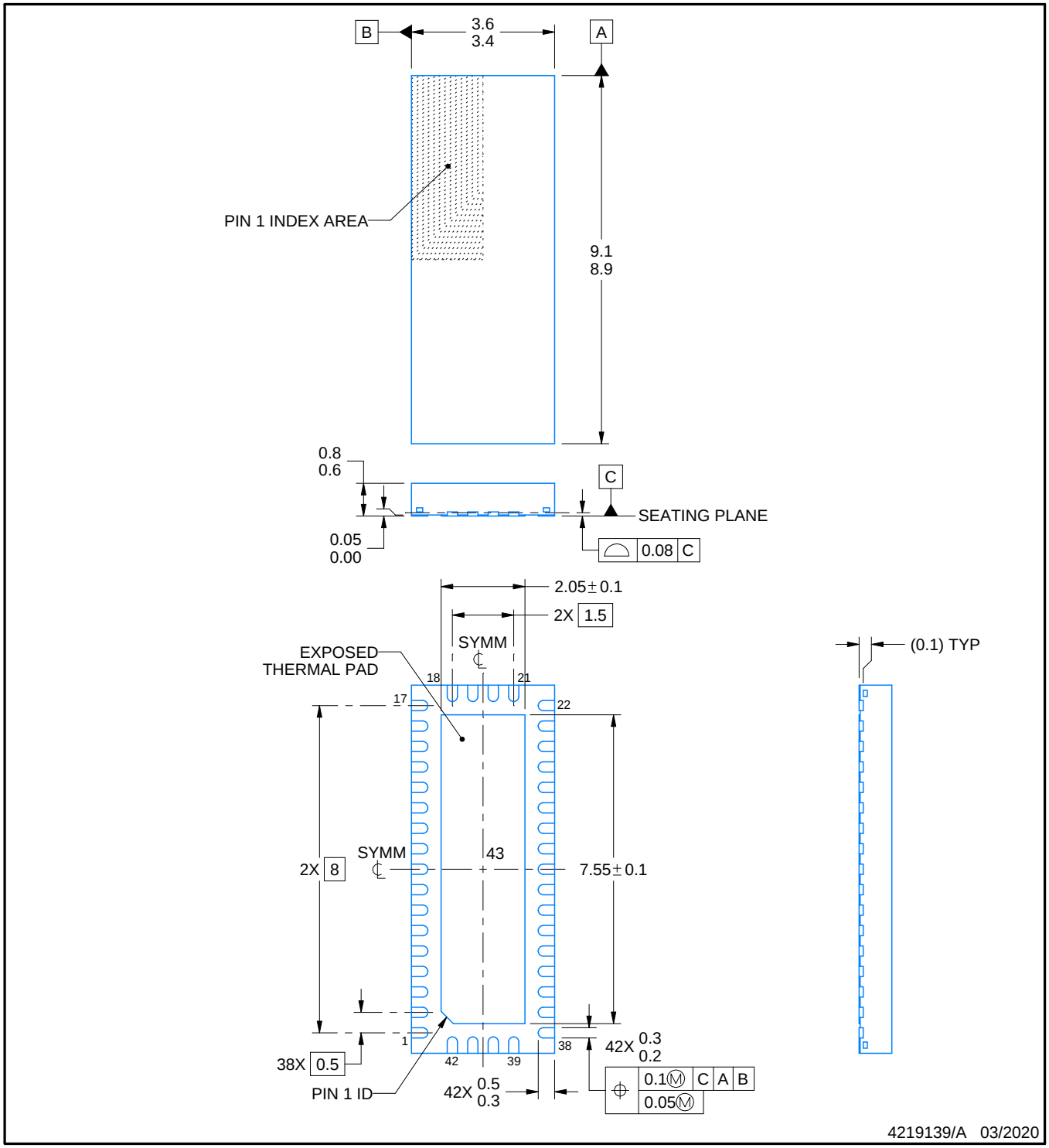
PACKAGE OUTLINE

RUA0042A



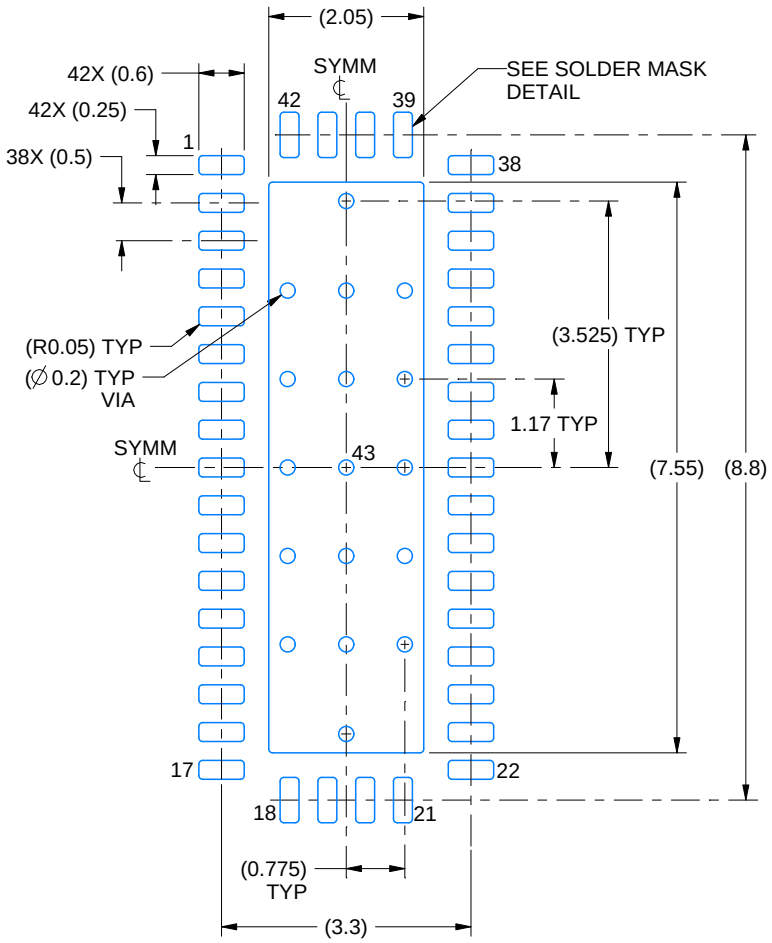
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

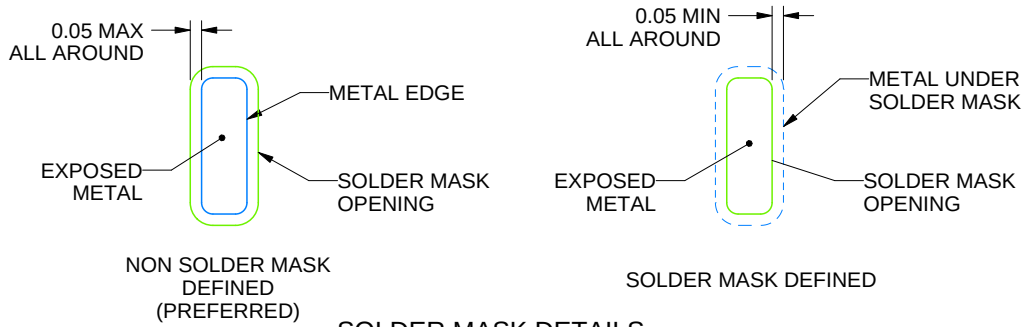


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

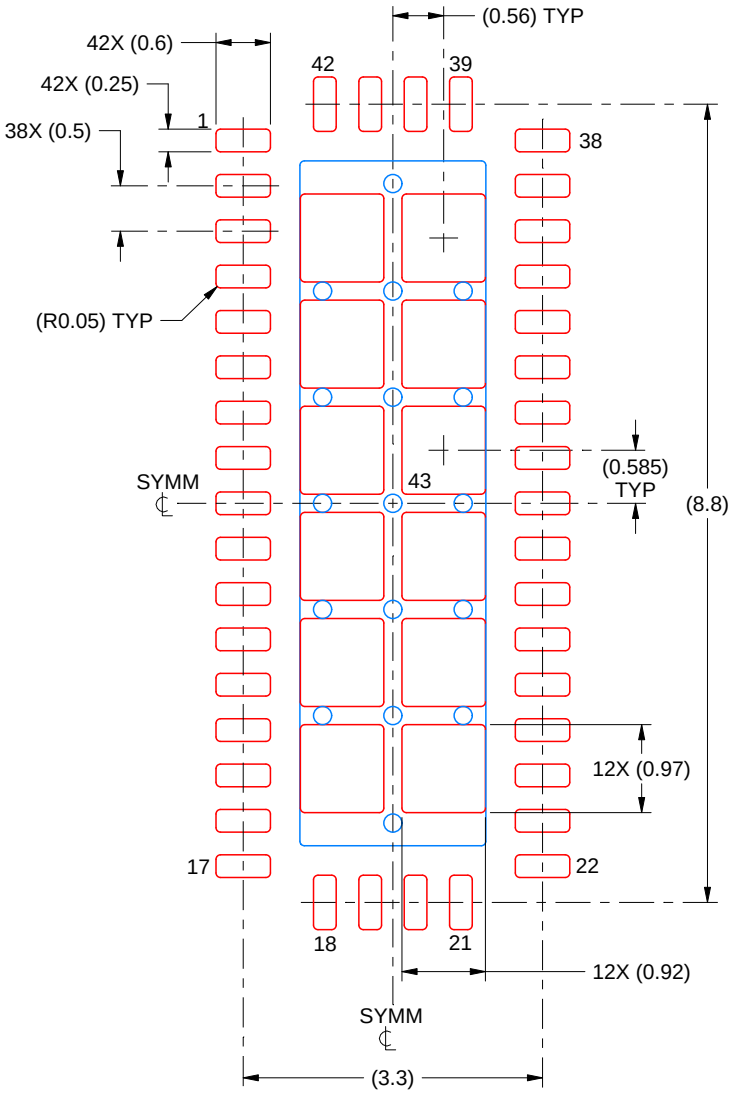
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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