TEXAS INSTRUMENTS
DRV8871-Q1
JAJSD16 – MARCH 2017

DRV8871-Q1 3.6Aブラシ付きDCモータ・ドライバ、電流センス内蔵 (PWM制御)

1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み：
  - デバイス温度グレード1: 動作時周囲温度範囲 –40°C～+125°C
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベルC4B
- Hブリッジ・モータ・ドライバ
  - 1台のDCモータ、ステッピング・モータの1つの巻線、またはその他の負荷を駆動
- 6.8V～45Vの広い動作電圧範囲
- 標準値565mΩの直流オン抵抗(ハイサイドとローサイド)
- 3.6Aのピーク駆動電流
- PWM制御インターフェイス
- センス抵抗不要の電流レギュレーション
- 低消費電力のスリープ・モード
- 小さなパッケージと占有面積
  - 8ピンHSOP: PowerPAD™
  - 4.9 × 6 mm
- 保護機能を内蔵
  - VM低電圧誤動作防止(UVLO)
  - 過電流保護(OCP)
  - サーマル・シャットダウン(TSD)
  - エラーからの自動復旧

2 アプリケーション

- 車載インフォテインメント
- HUDプロジェクタの調整
- 電動シフター・ノブ
- オンボード充電器

3 概要

DRV8871-Q1デバイスは、プリンタ、家電機器、産業用機器、その他小型機械用のブラシ付きDCモータ・ドライバです。2つのロジック入力がHブリッジ・ドライバを制御します。ドライバは4つのNチャネルMOSFETで構成され、最大ピーク電流3.6Aまでのモータを双方向制御します。入力をパルス幅変調(PWM)し電流減衰モードを選択してモータ回転数を制御できます。両方の入力を"L"にすると低消費電力スリープ・モードになります。

DRV8871-Q1デバイスには、高度な電流レギュレーション回路が搭載されており、アナログ基準電圧や、外付けのセンス抵抗を必要としません。この新たなソリューションは、標準の低コストで低消費電力の抵抗を使用して、電流スレッショルドを設定できます。電流を既知のレベルに制限できるため、システムに必要な電力を大幅に低減でき、特にモータの始動時やストール時に、安定した電圧を維持するため必要なバルク容量も低減できます。

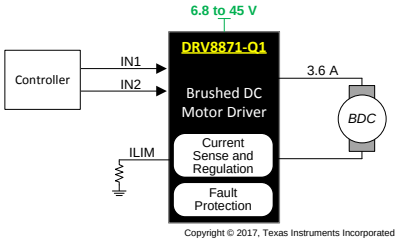
このデバイスは、低電圧(UVLO)、過電流(OCP)、過熱(TSD)などのフォルトや短絡から完全に保護されています。エラー状態が解消されると、デバイスは自動的に通常動作状態に復帰します。

製品情報 (1)

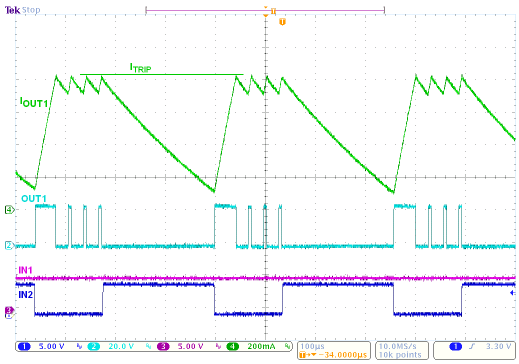
型番	パッケージ	本体サイズ(typ)
DRV8871-Q1	HSOP (8)	4.90mm×6.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



ピーク電流のレギュレーション



目次

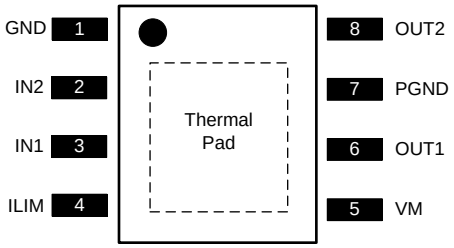
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	改訂内容	注
2017年3月	*	初版

5 Pin Configuration and Functions

DDA Package
8-Pin HSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION	
NAME	NO.			
GND	1	PWR	Logic ground	Connect to board ground
ILIM	4	I	Current limit control	Connect a resistor to ground to set the current chopping threshold
IN1	3	I	Logic inputs	Controls the H-bridge output. Has internal pulldowns (see 表 1).
IN2	2			
OUT1	6	O	H-bridge output	Connect directly to the motor or other inductive load.
OUT2	8			
PGND	7	PWR	High-current ground path	Connect to board ground.
VM	5	PWR	6.8-V to 45-V power supply	Connect a 0.1-µF bypass capacitor to ground, as well as sufficient bulk capacitance, rated for the VM voltage.
PAD	—	—	Thermal pad	Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	50	V
Logic input voltage (IN1, IN2)	–0.3	7	V
Continuous phase node pin voltage (OUT1, OUT2)	–0.7	VM + 0.7	V
Current sense input pin voltage (ISEN)(2)	–0.5	1	V
Output current (100% duty cycle)	0	3.5	A
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transients of ±1 V for less than 25 ns are acceptable

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 4, 5, and 8)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VM	Power supply voltage	6.8	45	V
V_I	Logic input voltage (IN1, IN2)	0	5.5	V
f_{PWM}	Logic input PWM frequency (IN1, IN2)	0	200 (1)	kHz
I_{peak}	Peak output current (2)	0	3.6	A
T_A	Operating ambient temperature (2)	–40	125	°C

(1) The voltages applied to the inputs should have at least 800 ns of pulse width to ensure detection. Typical devices require at least 400 ns. If the PWM frequency is 200 kHz, the usable duty cycle range is 16% to 84%.
(2) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC (1)		DRV8871-Q1 DDA (HSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over recommended operating conditions unless otherwise noted. Typical limits apply for T_A = 25°C and V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VM)						
VM	VM operating voltage		6.8		45	V
I_{VM}	VM operating supply current			3	10	mA
$I_{VMSLEEP}$	VM sleep current	VM = 12 V			13	µA
t_{ON} (1)	Turnon time	VM > V_{UVLO} with IN1 or IN2 high		40	50	µs
LOGIC-LEVEL INPUTS (IN1, IN2)						
V_{IL}	Input logic-low voltage				0.5	V
V_{IH}	Input logic-high voltage		1.6			V
V_{HYS}	Input logic hysteresis			0.5		V
I_{IL}	Input logic-low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic-high current	V_{IN} = 3.3 V		33	100	µA
R_{PD}	Pulldown resistance	To GND		100		kΩ
t_{PD}	Propagation delay	INx to OUTx change (see 図 6)		0.7	1	µs
t_{sleep}	Time to sleep	Inputs low to sleep		1	1.5	ms
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
$R_{DS(ON)}$	High-side FET on resistance	VM = 24 V, I = 1 A, f_{PWM} = 25 kHz		307	610	mΩ
$R_{DS(ON)}$	Low-side FET on resistance	VM = 24 V, I = 1 A, f_{PWM} = 25 kHz		258	500	mΩ
t_{DEAD}	Output dead time			250		ns
V_d	Body diode forward voltage	I_{OUT} = 1 A		0.8	1	V
CURRENT REGULATION						
V_{ILIM}	Constant for calculating current regulation (see 式 1)	VM = 24 V, I_{OUT} = 1 A	59	64	69	kV
t_{OFF}	PWM off-time			25		µs
t_{BLANK}	PWM blanking time			2		µs
PROTECTION CIRCUITS						
V_{UVLO}	VM undervoltage lockout	VM falls until UVLO triggers		6.3	6.5	V
		VM rises until operation recovers		6.4	6.7	
$V_{UV,HYS}$	VM undervoltage hysteresis	Rising to falling threshold		180		mV
I_{OCP}	Overcurrent protection trip level		3.7	4.5	6.6	A
t_{OCP}	Overcurrent deglitch time			2		µs
t_{RETRY}	Overcurrent retry time			3		ms
T_{SD}	Thermal shutdown temperature		155	180		°C
T_{HYS}	Thermal shutdown hysteresis			40		°C

(1) t_{ON} applies when the device initially powers up, and when it exits sleep mode.

6.6 Typical Characteristics

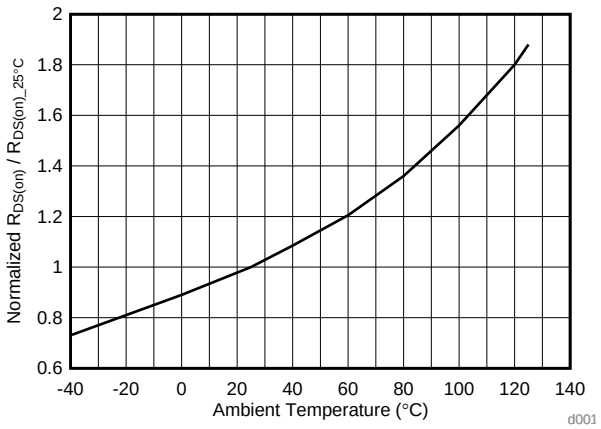


図 1. $R_{DS(on)}$ vs Temperature

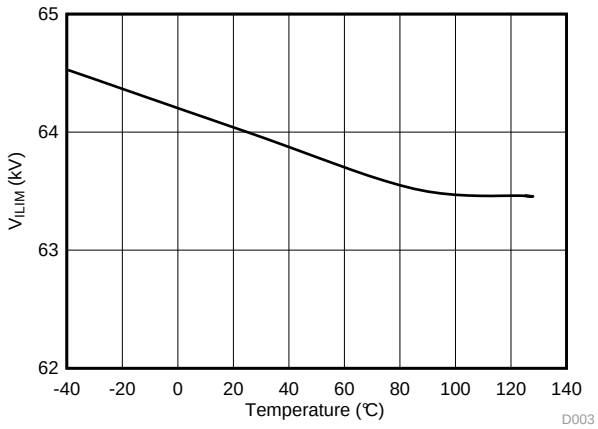


図 2. V_{ILIM} vs Temperature

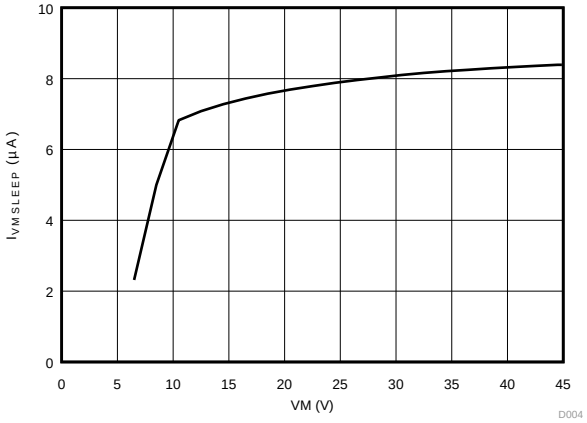


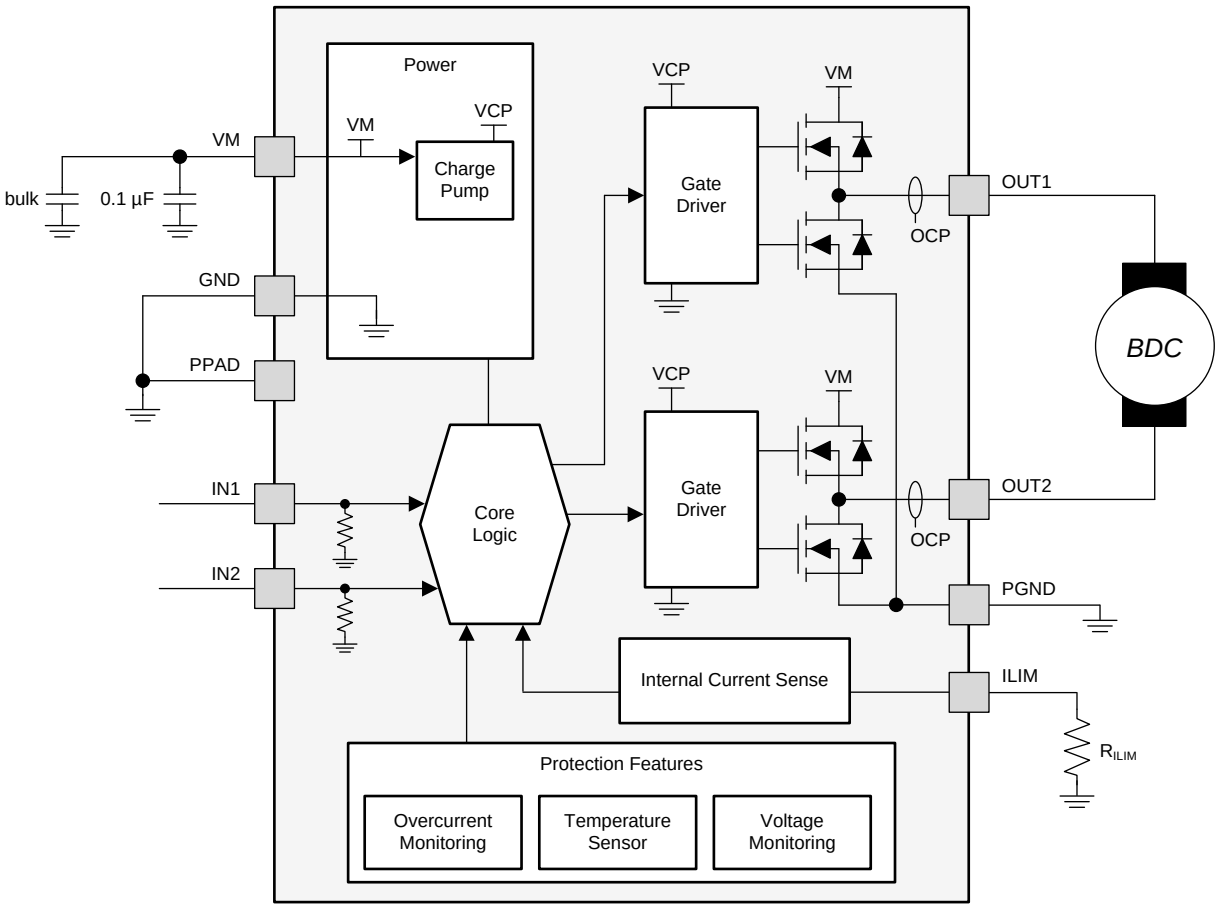
図 3. $I_{VMSLEEP}$ vs VM at 25°C

7 Detailed Description

7.1 Overview

The DRV8871-Q1 device is an optimized 8-pin device for driving brushed DC motors with 6.8 to 45 V and up to 3.6-A peak current. The integrated current regulation restricts motor current to a predefined maximum. Two logic inputs control the H-bridge driver, which consists of four N-channel MOSFETs that have a typical $R_{ds(on)}$ of 565 mΩ (including one high-side and one low-side FET). A single power input, VM, serves as both device power and the motor winding bias voltage. The integrated charge pump of the device boosts VM internally and fully enhances the high-side FETs. Motor speed can be controlled with pulse-width modulation, at frequencies between 0 to 100 kHz. The device has an integrated sleep mode that is entered by bringing both inputs low. An assortment of protection features prevent the device from being damaged if a system fault occurs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Bridge Control

The DRV8871-Q1 output consists of four N-channel MOSFETs that are designed to drive high current. They are controlled by the two logic inputs IN1 and IN2, according to 表 1.

表 1. H-Bridge Control

IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	High-Z	High-Z	Coast; H-bridge disabled to High-Z (sleep entered after 1 ms)
0	1	L	H	Reverse (Current OUT2 → OUT1)
1	0	H	L	Forward (Current OUT1 → OUT2)
1	1	L	L	Brake; low-side slow decay

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM, it typically works best to switch between driving and braking. For example, to drive a motor forward with 50% of its max RPM, IN1 = 1 and IN2 = 0 during the driving period, and IN1 = 1 and IN2 = 1 during the other period. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for *fast current decay* is also available. The input pins can be powered before VM is applied.

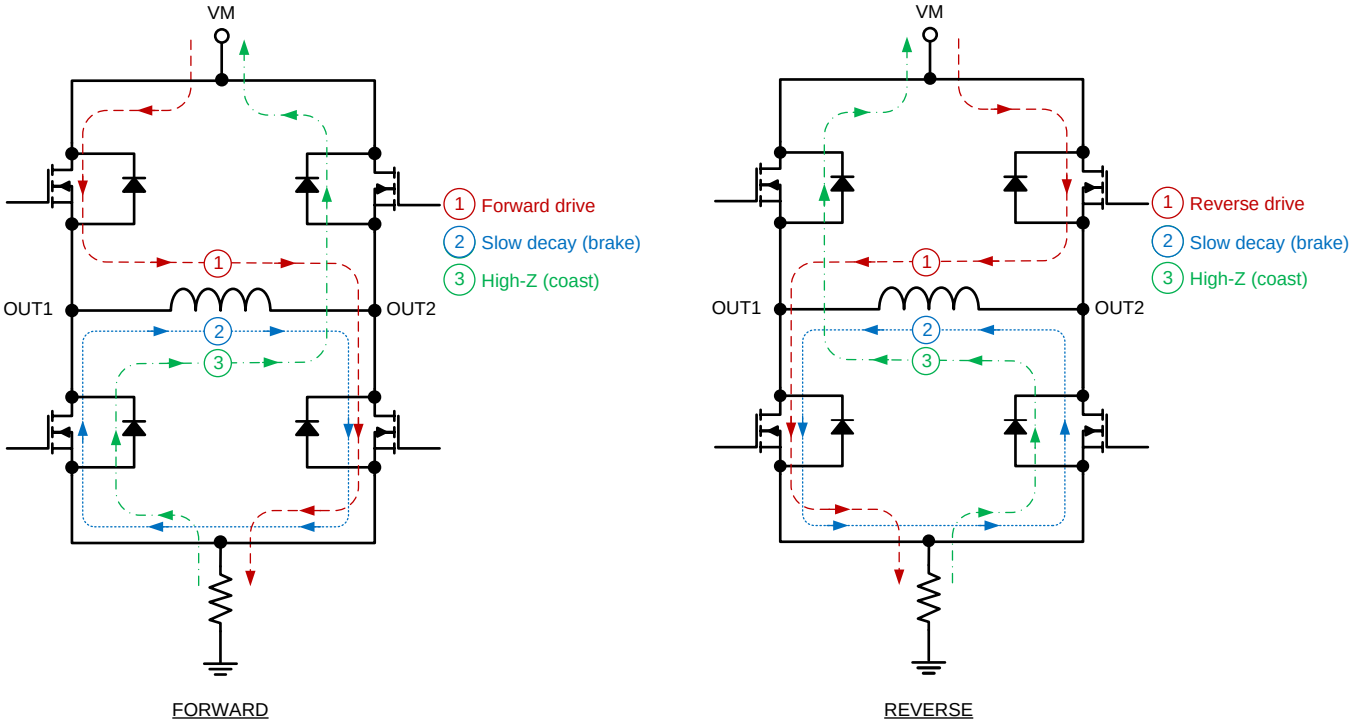


図 4. H-Bridge Current Paths

7.3.2 Sleep Mode

When IN1 and IN2 are both low for time t_{SLEEP} (typically 1 ms), the DRV8871-Q1 device enters a low-power sleep mode, where the outputs remain High-Z and the device uses $I_{VMSLEEP}$ (microamps) of current. If the device is powered up while both inputs are low, sleep mode is immediately entered. After IN1 or IN2 are high for at least 5 µs, the device will be operational 50 µs (t_{ON}) later.

7.3.3 Current Regulation

The DRV8871-Q1 device limits the output current based on a standard resistor attached to pin ILIM, according to this equation:

$$I_{TRIP}\ (A) = \frac{V_{ILIM}\ (kV)}{R_{ILIM}\ (k\Omega)} = \frac{64\ (kV)}{R_{ILIM}\ (k\Omega)} \quad (1)$$

For example, if R_{ILIM} = 32 kΩ, the DRV8871-Q1 device limits motor current to 2 A no matter how much load torque is applied. The minimum allowed R_{ILIM} is 15 kΩ. System designers should always understand the min and max I_{TRIP}, based on the R_{ILIM} resistor component tolerance and the DRV8871-Q1 specified V_{ILIM} range.

When I_{TRIP} has been reached, the device enforces slow current decay by enabling both low-side FETs, and it does this for time t_{OFF} (typically 25 µs).

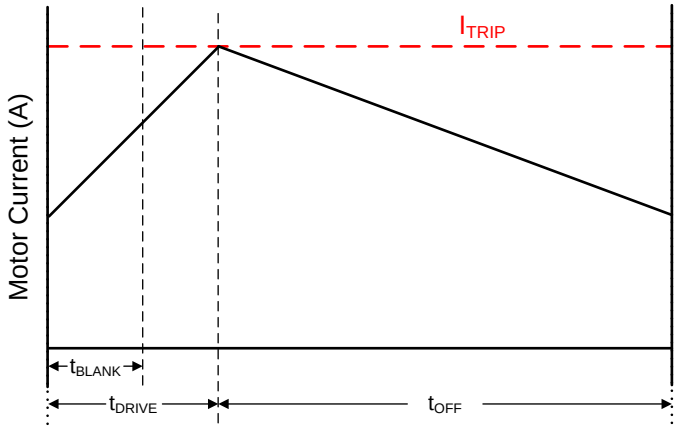


図 5. Current Regulation Time Periods

After t_{OFF} has elapsed, the output is re-enabled according to the two inputs INx. The drive time (t_{DRIVE}) until reaching another I_{TRIP} event heavily depends on the VM voltage, the motor's back-EMF, and the motor's inductance.

7.3.4 Dead Time

When an output changes from driving high to driving low, or driving low to driving high, dead time is automatically inserted to prevent shoot-through. t_{DEAD} is the time in the middle when the output is High-Z. If the output pin is measured during t_{DEAD}, the voltage will depend on the direction of current. If current is leaving the pin, the voltage will be a diode drop below ground. If current is entering the pin, the voltage will be a diode drop above VM. This diode is the body diode of the high-side or low-side FET.

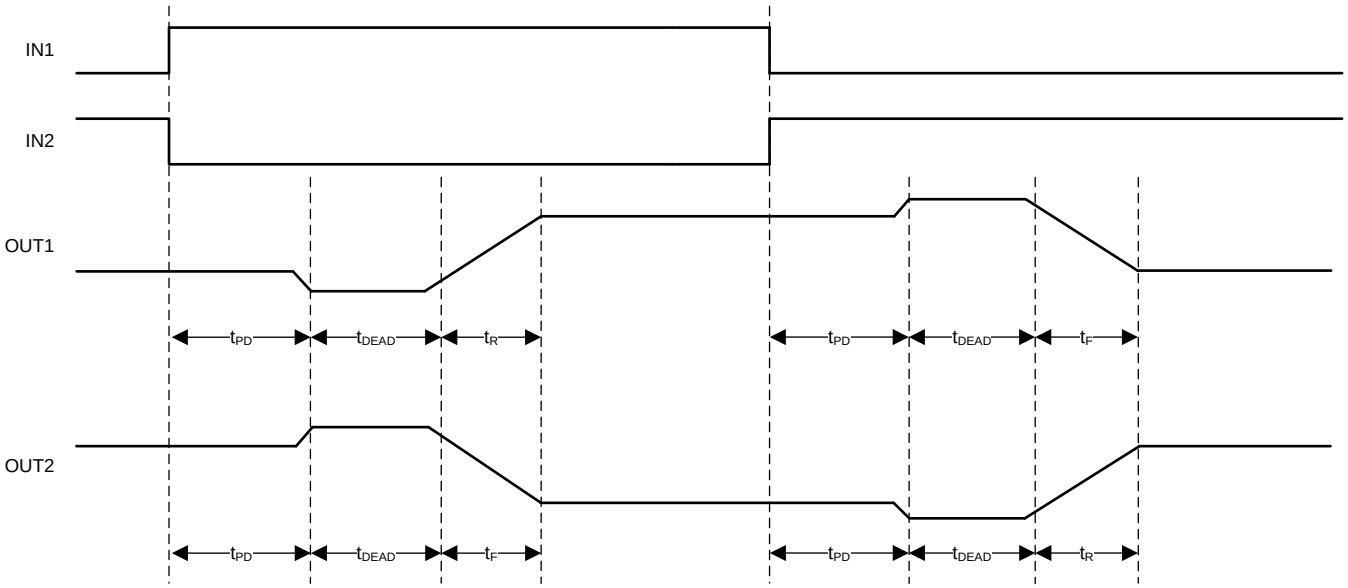


図 6. Propagation Delay Time

7.3.5 Protection Circuits

The DRV8871-Q1 device is fully protected against VM undervoltage, overcurrent, and overtemperature events.

7.3.5.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge will be disabled. Operation will resume when VM rises above the UVLO threshold.

7.3.5.2 Overcurrent Protection (OCP)

If the output current exceeds the OCP threshold I_{OCP} for longer than t_{OCP}, all FETs in the H-bridge are disabled for a duration of t_{RETRY}. After that, the H-bridge will be re-enabled according to the state of the INx pins. If the overcurrent fault is still present, the cycle repeats; otherwise normal device operation resumes.

7.3.5.3 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled. After the die temperature has fallen to a safe level, operation automatically resumes.

表 2. Protection Functionality

FAULT	CONDITION	H-BRIDGE STATUS	RECOVERY
VM undervoltage lockout (UVLO)	$VM < V_{UVLO}$	Disabled	$VM > V_{UVLO}$
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	Disabled	t_{RETRY}
Thermal Shutdown (TSD)	$T_J > 150°C$	Disabled	$T_J < T_{SD} – T_{HYS}$

7.4 Device Functional Modes

The DRV8871-Q1 device can be used in multiple ways to drive a brushed DC motor.

7.4.1 PWM With Current Regulation

This scheme uses all of the device capabilities. I_{TRIP} is set above the normal operating current, and high enough to achieve an adequate spin-up time, but low enough to constrain current to a desired level. Motor speed is controlled by the duty cycle of one of the inputs, while the other input is static. Brake/slow decay is typically used during the off-time.

7.4.2 PWM Without Current Regulation

If current regulation is not needed, a 15-kΩ to 18-kΩ resistor should be used on pin ILIM. This mode provides the highest possible peak current: up to 3.6 A for a few hundred milliseconds (depending on PCB characteristics and the ambient temperature). If current exceeds 3.6 A, the device might reach overcurrent protection (OCP) or overtemperature shutdown (TSD). If that happens, the device disables and protects itself for about 3 ms (t_{RETRY}) and then resumes normal operation.

7.4.3 Static Inputs With Current Regulation

IN1 and IN2 can be set high and low for 100% duty cycle drive, and I_{TRIP} can be used to control the current, speed, and torque capability of the motor.

7.4.4 VM Control

In some systems it is desirable to vary VM as a means of changing motor speed. See *Motor Voltage* for more information.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8871-Q1 device is typically used to drive one brushed DC motor.

8.2 Typical Application

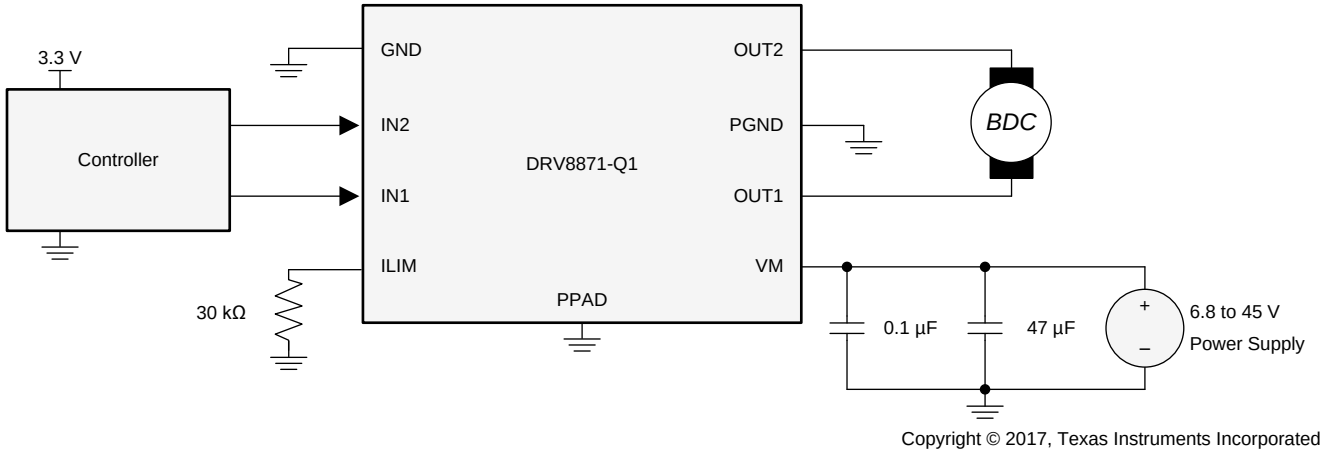


図 7. Typical Connections

8.2.1 Design Requirements

表 3 lists the design parameters.

表 3. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	V_M	24 V
Motor RMS current	I_{RMS}	0.8 A
Motor startup current	I_{START}	2 A
Motor current trip point	I_{TRIP}	2.1 A
ILIM resistance	R_{ILIM}	30 kΩ
PWM frequency	f_{PWM}	5 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.2.2 Drive Current

The current path is through the high-side sourcing DMOS power driver, motor winding, and low-side sinking DMOS power driver. Power dissipation losses in one source and sink DMOS power driver are shown in the following equation.

$$P_D = I^2 \left(R_{DS(on)Source} + R_{DS(on)Sink} \right) \quad (2)$$

The DRV8871-Q1 device has been measured to be capable of 2-A RMS current at 25°C on standard FR-4 PCBs. The max RMS current varies based on the PCB design, ambient temperature, and PWM frequency. Typically, switching the inputs at 200 kHz compared to 20 kHz causes 20% more power loss in heat.

8.2.3 Application Curves

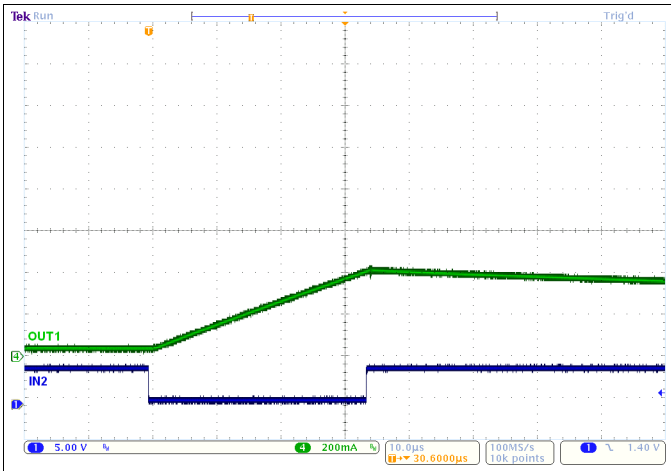


図 8. Current Ramp With a 2-Ω, 1 mH, RL Load and VM = 12 V

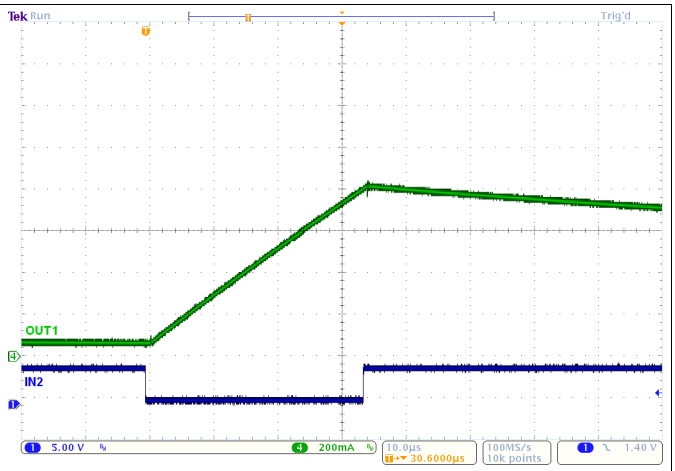


図 9. Current Ramp With a 2-Ω, 1 mH, RL Load and VM = 24 V

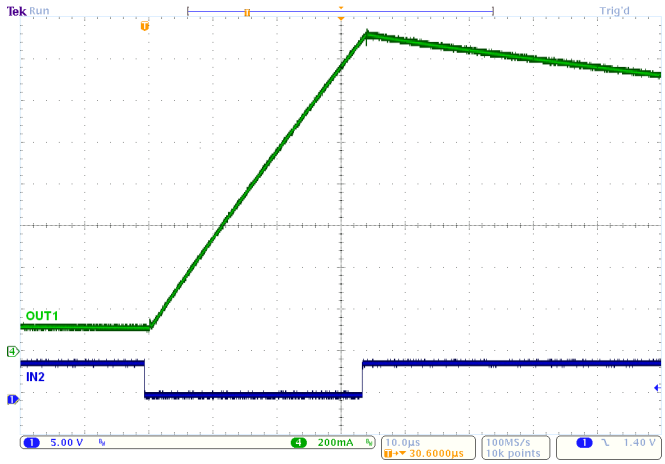


図 10. Current Ramp With a 2-Ω, 1 mH, RL Load and VM = 45 V

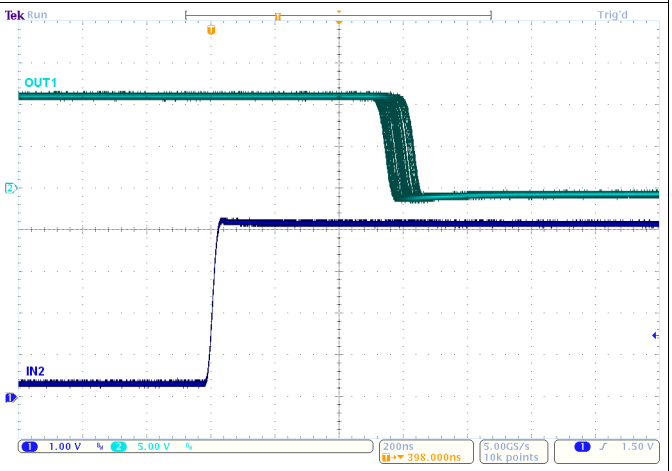


図 11. t_{PD}

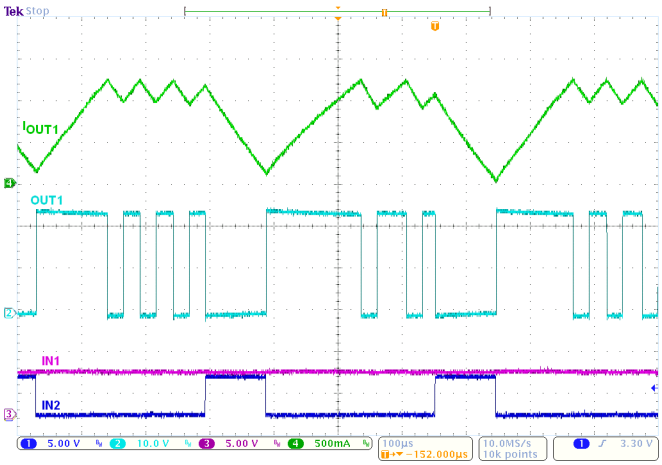


図 12. Current Regulation With R_{ILIM} = 50.5 kΩ

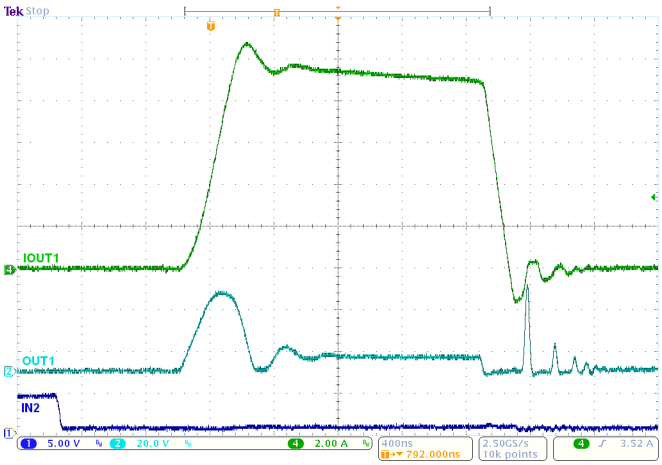


図 13. OCP With 45 V and the Outputs Shorted Together

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. In general, having have more bulk capacitance is beneficial, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system reponds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

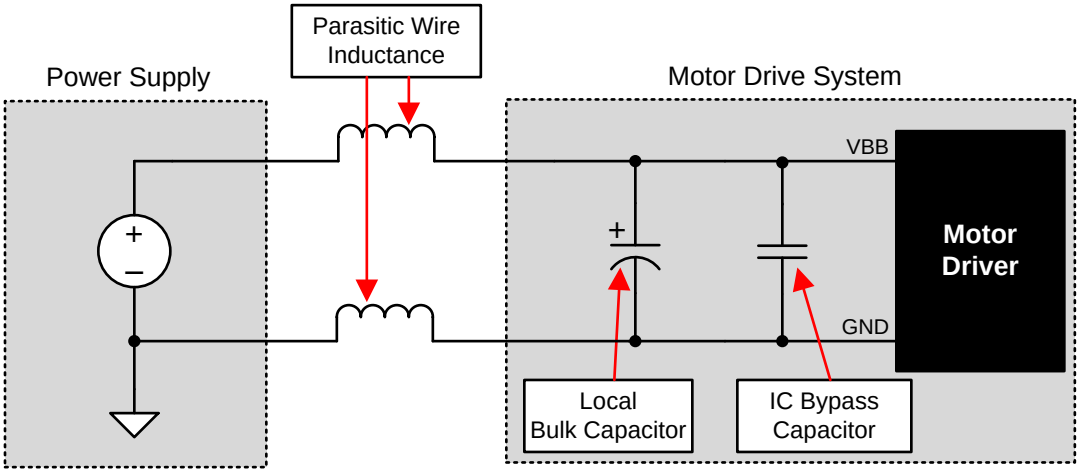


図 14. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

10.2 Layout Example

Recommended layout and component placement is shown in 図 15

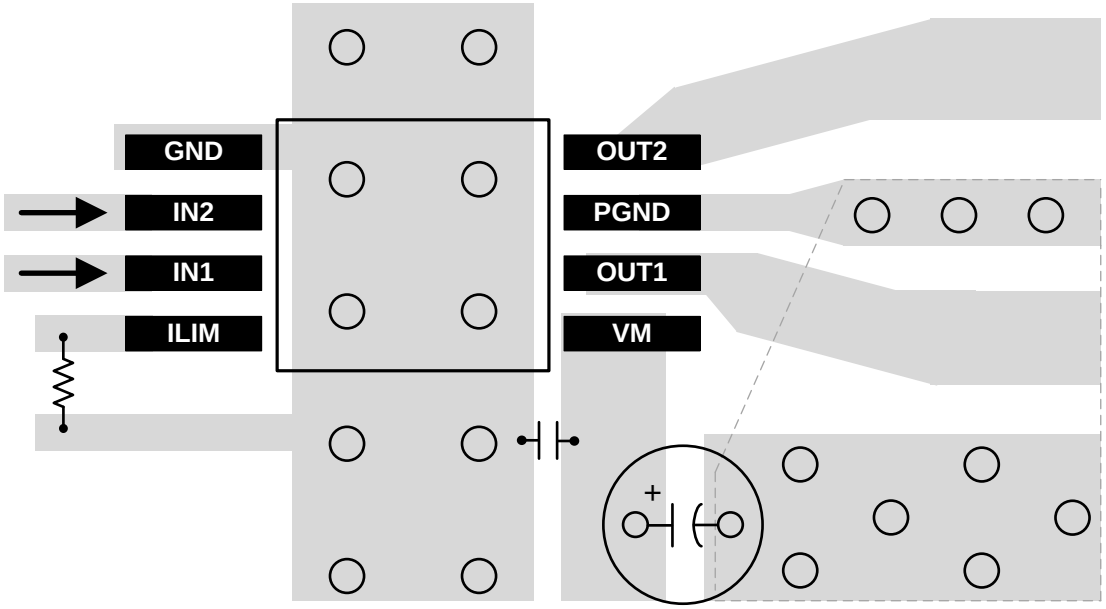


図 15. Layout Recommendation

10.3 Thermal Considerations

The DRV8871-Q1 device has thermal shutdown (TSD) as described in the *Thermal Shutdown (TSD)* section. If the die temperature exceeds approximately 175°C, the device is disabled until the temperature drops below the temperature hysteresis level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high of an ambient temperature.

10.4 Power Dissipation

Power dissipation in the DRV8871-Q1 device is dominated by the power dissipated in the output FET resistance, $R_{DS(on)}$. Use the equation in the *Drive Current* section to calculate the estimated average power dissipation when driving a load.

Note that at startup, the current is much higher than normal running current; this peak current and its duration must be also be considered.

Power Dissipation (continued)

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

注

$R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. This fact must be taken into consideration when sizing the heatsink.

The power dissipation of the DRV8871-Q1 device is a function of RMS motor current and the FET resistance ($R_{DS(ON)}$) of each output.

$$\text{Power} \approx I_{RMS}^2 \times \left(\text{High-side } R_{DS(ON)} + \text{ Low-side } R_{DS(ON)}\right) \quad (3)$$

For this example, the ambient temperature is 58°C, and the junction temperature reaches 80°C. At 58°C, the sum of $R_{DS(ON)}$ is about 0.72 Ω. With an example motor current of 0.8 A, the dissipated power in the form of heat will be $0.8\ A^2 \times 0.72\ \Omega = 0.46$ W.

The temperature that the DRV8871-Q1 device reaches depends on the thermal resistance to the air and PCB. It is important to solder the device PowerPAD to the PCB ground plane, with vias to the top and bottom board layers, in order dissipate heat into the PCB and reduce the device temperature. In the example used here, the DRV8871-Q1 device had an effective thermal resistance $R_{\theta JA}$ of 48°C/W, and:

$$T_J = T_A + (P_D \times R_{\theta JA}) = 58°C + (0.46\ W \times 48°C/W) = 80°C \quad (4)$$

10.4.1 Heatsinking

The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this connection can be accomplished by adding a number of vias to connect the thermal pad to the ground plane.

On PCBs without internal planes, a copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to *PowerPAD™ Thermally Enhanced Package* (SLMA002) and *PowerPAD Made Easy™* (SLMA004), available at www.ti.com. In general, the more copper area that can be provided, the more power can be dissipated.

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- *『電流再循環および減衰モード』*
- *『モータ・ドライバの消費電力の計算』*
- *『DRV8871評価モジュール』*
- *『放熱特性の優れたPowerPAD™パッケージ』*
- *『PowerPAD™の簡単な使用法』*
- *『モータ・ドライバの電流定格について』*

11.2 ドキュメントの更新通知を受け取る方法

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11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8871DDARQ1	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	8871Q
DRV8871DDARQ1.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	8871Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF DRV8871-Q1 :

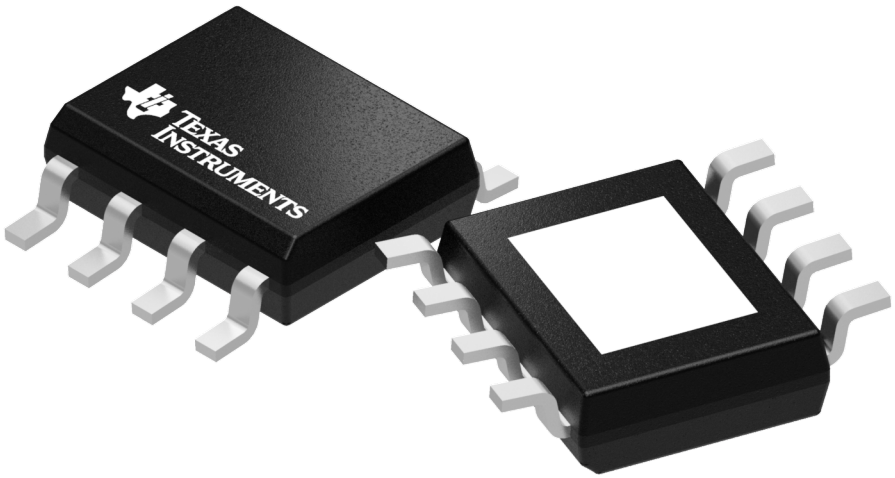
- Catalog : DRV8871

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

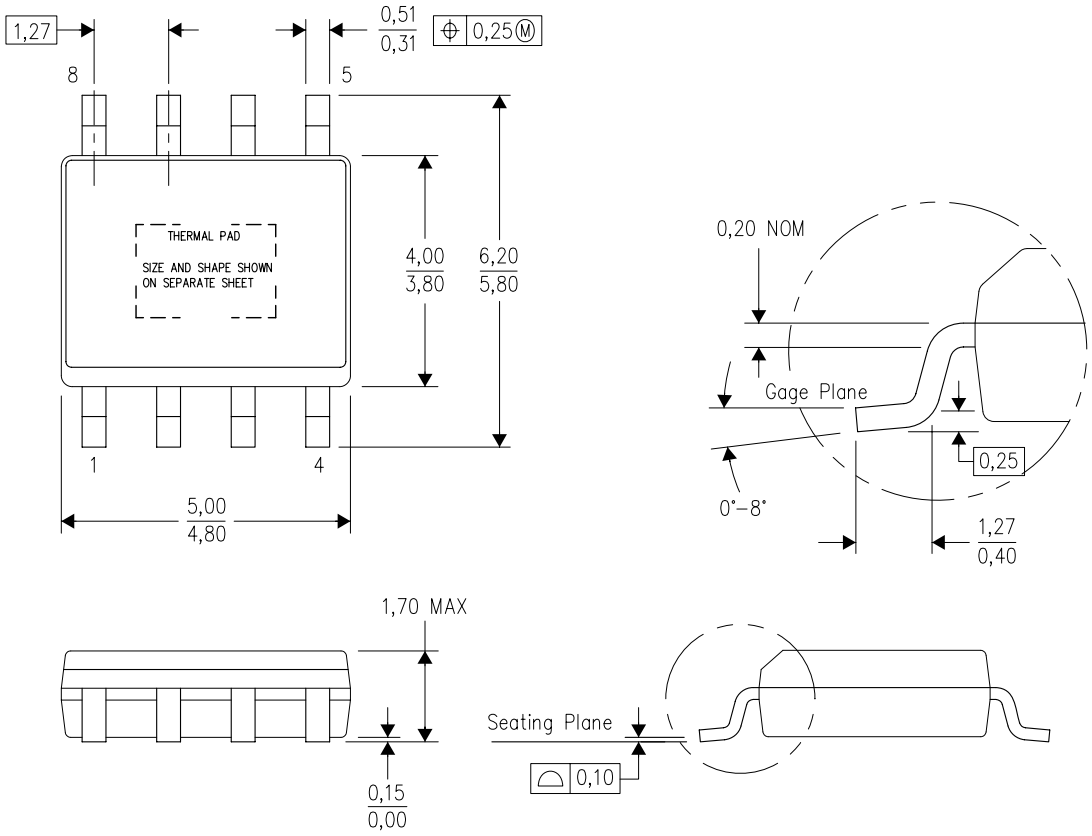
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

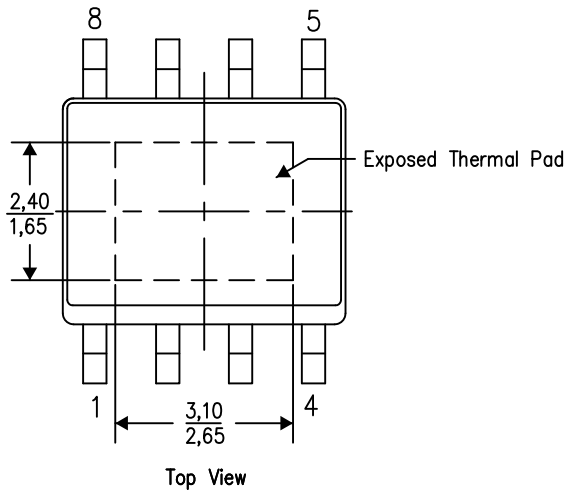
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

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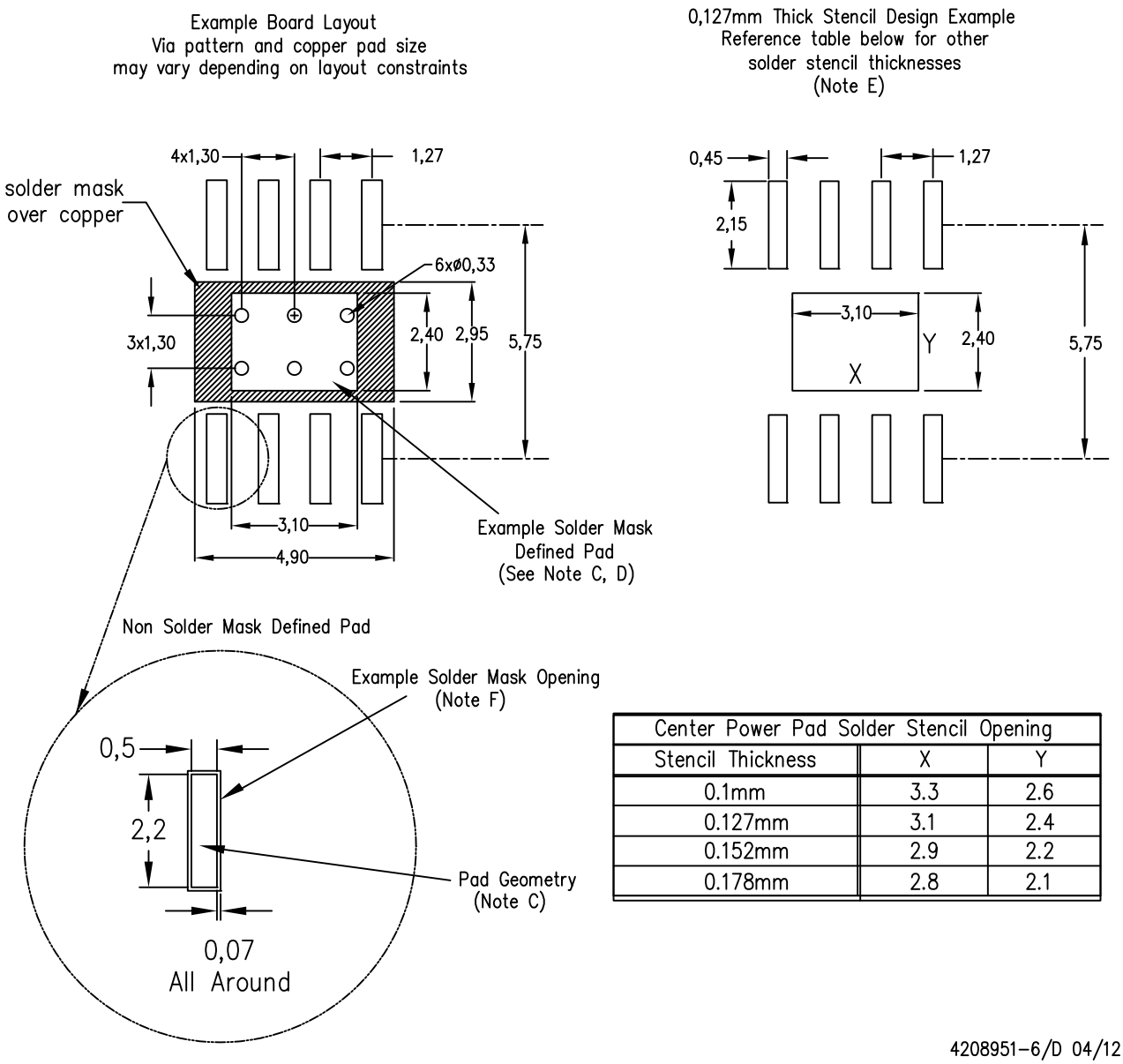
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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