参考資料

TEXAS INSTRUMENTS

DRV8353M 100V 3 相スマート・ゲート・ドライバ

1 特長

- 9～100V、トリプル・ハーフブリッジ・ゲート・ドライバ
  - 拡張 T_A 動作 (-55℃～125℃)
  - (オプション) トリプル・ローサイド電流シャント・アンプ
- スマート・ゲート・ドライブ・アーキテクチャ
  - 調整可能なスルーレート制御による EMI 性能の向上
  - V_{GS} ハンドシェイクおよび最小限のデッド・タイム挿入により貫通電流を回避
  - 50mA～1A のピーク・ソース電流
  - 100mA～2A のピーク・シンク電流
  - 強力なプルダウンにより dV/dt を低減
- ゲート・ドライバ電源を内蔵
  - ハイサイド・ダブラー・チャージ・ポンプによる 100% PWM デューティ・サイクル制御
  - ローサイドのリニア・レギュレータ
- トリプル電流シャント・アンプ内蔵
  - 可変ゲイン (5、10、20、40V/V)
  - 双方向または単方向のサポート
- 6x、3x、1x、および独立 PWM モード
  - 120° センサ付き動作をサポート
- SPI またはハードウェア・インターフェイスを利用可能
- 低消費電力のスリープ・モード (V_{VM} = 48V で 20μA)
- 保護機能内蔵
  - VM 低電圧誤動作防止 (UVLO)
  - ゲート駆動電源低電圧 (GDUV)
  - MOSFET V_{DS} 過電流保護 (OCP)
  - MOSFET 貫通電流防止
  - ゲート・ドライバのフォルト (GDF)
  - 熱警告およびシャットダウン (OTW/OTSD)
  - フォルト状態インジケータ (nFAULT)

2 アプリケーション

- 3 相のブラシレス DC (BLDC) モータ・モジュール
- ファン、ブロワ、ポンプ

3 概要

DRV8353M ファミリのデバイスは、3 相ブラシレス DC (BLDC) モータ・アプリケーション向けの高度に統合されたゲート・ドライバです。BLDC モータの磁界方向制御 (FOC)、正弦波電流制御、および台形電流制御に適しています。このデバイス・バリエーションにはオプションとして、各種のモータ制御方式をサポートするための内蔵電流シャント・アンプと、ゲート・ドライバや外部コントローラに給電するための降圧レギュレータが用意されています。

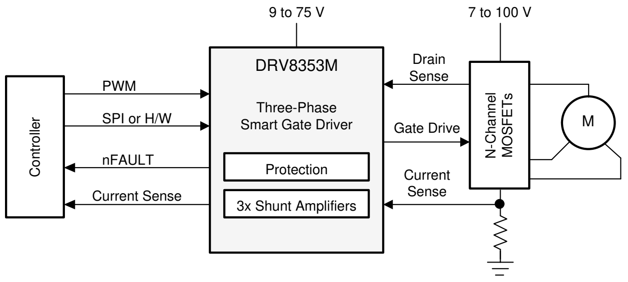
DRV8353M はスマート・ゲート・ドライブ (SGD) アーキテクチャを使用して、通常は MOSFET スルーレート制御および保護回路に必要となる外付け部品の数を減らしています。また、SGD アーキテクチャによりデッド・タイムが最適化されて貫通電流状況が防止され、MOSFET のスルーレート制御により電磁気干渉 (EMI) を柔軟に低減でき、V_{GS} 監視によってゲートの短絡状況に対する保護を行えます。ゲートの強力なプルダウン回路は、望ましくない dV/dt 寄生ゲート・ターンオンの防止に役立ちます。

各種の PWM 制御モード (6x、3x、1x、および独立) がサポートされており、外部コントローラと簡単に接続できます。これらのモードにより、モータ・ドライバ PWM 制御信号のために必要なコントローラ出力の数を減らすことができます。このファミリのデバイスには 1x PWM モードも含まれており、内部ブロックの通信テーブルを使用して、BLDC モータの単純なセンサ付き台形制御に使用できます。

表 3-1. 製品情報

部品番号	パッケージ	本体サイズ (公称)
DRV8353M	WQFN (40)	6.00mm×6.00mm

1. 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

English Data Sheet: SLVSFO2

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

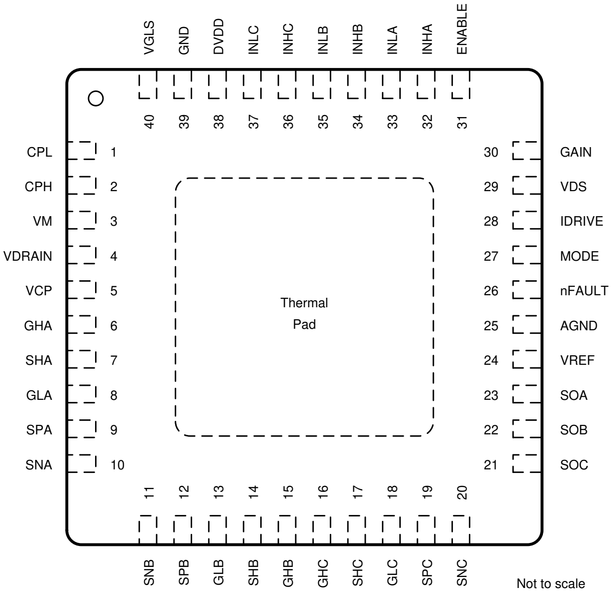
DATE	REVISION	NOTES
July 2020	*	Initial Release

5 Device Comparison Table

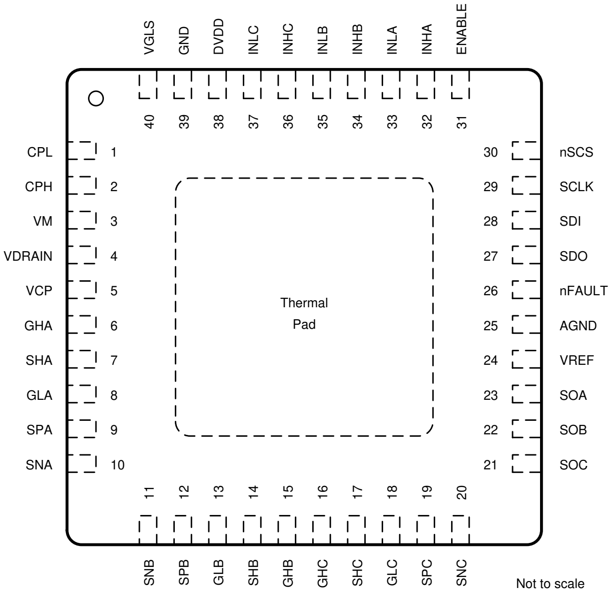
DEVICE	VARIANT	SHUNT AMPLIFIERS	INTERFACE
DRV8353M	DRV8353HM	3	Hardware (H)
	DRV8353SM		SPI (S)

6 Pin Configuration and Functions

Pin Functions—40-Pin DRV8353M Devices



DRV8353HM RTA Package 40-Pin VWQFN With Exposed Thermal Pad Top View



DRV8353SM RTA Package 40-Pin VWQFN With Exposed Thermal Pad Top View

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8353HM	DRV8353SM		
AGND	25	25	PWR	Device analog ground. Connect to system ground.
CPH	2	2	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, VDRAIN-rated ceramic capacitor between the CPH and CPL pins.
CPL	1	1	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, VDRAIN-rated ceramic capacitor between the CPH and CPL pins.
DVDD	38	38	PWR	5-V internal regulator output. Connect a X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the DVDD and GND pins. This regulator can source up to 10 mA externally.
ENABLE	31	31	I	Gate driver enable. When this pin is logic low the device goes to a low power sleep mode. An 8 to 40-µs low pulse can be used to reset fault conditions.
GAIN	30	—	I	Amplifier gain setting. The pin is a 4 level input pin set by an external resistor.
GND	39	39	PWR	Device power ground. Connect to system ground.
GHA	6	6	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	15	15	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	16	16	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	8	8	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8353HM	DRV8353SM		
GLB	13	13	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLC	18	18	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
IDRIVE	28	—	I	Gate drive output current setting. This pin is a 7 level input pin set by an external resistor.
INHA	32	32	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHB	34	34	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHC	36	36	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLA	33	33	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLB	35	35	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLC	37	37	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
MODE	27	—	I	PWM input mode setting. This pin is a 4 level input pin set by an external resistor.
nFAULT	26	26	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pullup resistor.
nSCS	—	30	I	Serial chip select. A logic low on this pin enables serial interface communication.
SCLK	—	29	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin.
SDI	—	28	I	Serial data input. Data is captured on the falling edge of the SCLK pin.
SDO	—	27	OD	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This pin requires an external pullup resistor.
SHA	7	7	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHB	14	14	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHC	17	17	I	High-side source sense input. Connect to the high-side power MOSFET source.
SNA	10	10	I	Shunt amplifier input. Connect to the low-side of the current shunt resistor.
SNB	11	11	I	Shunt amplifier input. Connect to the low-side of the current shunt resistor.
SNC	20	20	I	Shunt amplifier input. Connect to the low-side of the current shunt resistor.
SOA	23	23	O	Shunt amplifier output.
SOB	22	22	O	Shunt amplifier output.
SOC	21	21	O	Shunt amplifier output.
SPA	9	9	I	Low-side source sense and shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SPB	12	12	I	Low-side source sense and shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SPC	19	19	I	Low-side source sense and shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
VCP	5	5	PWR	Charge pump output. Connect a X5R or X7R, 1-µF, 16-V ceramic capacitor between the VCP and VDRAIN pins.
VDRAIN	4	4	I	High-side MOSFET drain sense input and charge pump reference. Connect to the common point of the MOSFET drains.
VDS	29	—	I	VDS monitor trip point setting. This pin is a 7 level input pin set by an external resistor.
VGLS	40	40	PWR	11-V internal regulator output. Connect a X5R or X7R, 1-µF, 16-V ceramic capacitor between the VGLS and GND pins.
VM	3	3	PWR	Gate driver power supply input. Connect to either VDRAIN or separate gate driver supply voltage. Connect a X5R or X7R, 0.1-µF, VM-rated ceramic and greater then or equal to 10-uF local capacitance between the VM and GND pins.
VREF	24	24	PWR	Shunt amplifier power supply input and reference. Connect a X5R or X7R, 0.1-µF, 6.3-V ceramic capacitor between the VREF and AGND pins.

(1) PWR = power, I = input, O = output, NC = no connection, OD = open-drain

7 Absolute Maximum Ratings

at T_A = –55°C to +125°C (unless otherwise noted)(1)

	MIN	MAX	UNIT
GATE DRIVER			
Power supply pin voltage (VM)	–0.3	80	V
Voltage differential between ground pins (AGND, BGND, DGND, PGND)	–0.3	0.3	V
MOSFET drain sense pin voltage (VDRAIN)	–0.3	102	V
MOSFET drain sense pin voltage slew rate (VDRAIN)	0	2	V/µs
Charge pump pin voltage (CPH, VCP)	–0.3	V_{VDRAIN} + 16	V
Charge-pump negative-switching pin voltage (CPL)	–0.3	V_{VDRAIN}	V
Low-side gate drive regulator pin voltage (VGLS)	–0.3	18	V
Internal logic regulator pin voltage (DVDD)	–0.3	5.75	V
Digital pin voltage (ENABLE, GAIN, IDRIVE, INHx, INLx, MODE, nFAULT, nSCS, SCLK, SDI, SDO, VDS)	–0.3	5.75	V
Continuous high-side gate drive pin voltage (GHx)	–5(2)	V_{VCP} + 0.3	V
Transient 200-ns high-side gate drive pin voltage (GHx)	–10	V_{VCP} + 0.3	V
High-side gate drive pin voltage with respect to SHx (GHx)	–0.3	16	V
Continuous high-side source sense pin voltage (SHx)	–5(2)	102	V
Continuous high-side source sense pin voltage (SHx)	–5(2)	V_{VDRAIN} + 5	V
Transient 200-ns high-side source sense pin voltage (SHx)	–10	V_{VDRAIN} + 10	V
Continuous low-side gate drive pin voltage (GLx)	–1.0	V_{VGLS} + 0.3	V
Transient 200-ns low-side gate drive pin voltage (GLx)	–5.0	V_{VGLS} + 0.3	V
Gate drive pin source current (GHx, GLx)	Internally limited	Internally limited	A
Gate drive pin sink current (GHx, GLx)	Internally limited	Internally limited	A
Continuous low-side source sense pin voltage (SLx)	–1	1	V
Transient 200-ns low-side source sense pin voltage (SLx)	–5	5	V
Continuous shunt amplifier input pin voltage (SNx, SPx)	–1	1	V
Transient 200-ns shunt amplifier input pin voltage (SNx, SPx)	–5	5	V
Reference input pin voltage (VREF)	–0.3	5.75	V
Shunt amplifier output pin voltage (SOx)	–0.3	V_{VREF} + 0.3	V
DRV8353M			
Ambient temperature, T_A	–55	125	°C
Junction temperature, T_J	–55	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) VDRAIN pin voltage with respect to high-side gate pin (GHx) and phase node pin voltage (SHx) should be limited to 102 V maximum. This will limit the GHx and SHx pin negative voltage capability when VDRAIN is greater than 92 V.

8 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

9 Recommended Operating Conditions

at T_A = –40°C to +125°C (unless otherwise noted)

		MIN	MAX	UNIT
GATE DRIVER				
V_{VM}	Gate driver power supply voltage (VM)	9	75	V
V_{VDRAIN}	Charge pump reference and drain voltage sense (VDRAIN)	7	100	V
V_I	Input voltage (ENABLE, GAIN, IDRIVE, INHx, INLx, MODE, nSCS, SCLK, SDI, VDS)	0	5.5	V
f_{PWM}	Applied PWM signal (INHx, INLx)	0	200(1)	kHz
t_{SH}	Switch-node slew rate range (SHx)	0	2	V/ns
I_{GATE_HS}	High-side average gate-drive current (GHx)	0	25(1)	mA
I_{GATE_LS}	Low-side average gate-drive current (GLx)	0	25(1)	mA
I_{DVDD}	External load current (DVDD)	0	10(1)	mA
V_{VREF}	Reference voltage input (VREF)	3	5.5	V
I_{SO}	Shunt amplifier output current (SOx)	0	5	mA
V_{OD}	Open drain pullup voltage (nFAULT, SDO)	0	5.5	V
I_{OD}	Open drain output current (nFAULT, SDO)	0	5	mA
DRV8353M				
T_A	Operating ambient temperature	–55	125	°C
T_J	Operating junction temperature	–55	150	°C

(1) Power dissipation and thermal limits must be observed.

10 Thermal Information

THERMAL METRIC[1]		DRV8353M
		RTA (WQFN)
		40 PINS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.1
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.1
$R_{\theta JB}$	Junction-to-board thermal resistance	8.4
Ψ_{JT}	Junction-to-top characterization parameter	0.1
Ψ_{JB}	Junction-to-board characterization parameter	8.4
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

11 Electrical Characteristics

at T_A = –55°C to +125°C, V_{VM} = 9 to 75 V, V_{VDRAIN} = 9 to 100 V, V_{VIN} = 48 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (DVDD, VCP, VGLS, VM)						
I_{VM}	VM operating supply current	V_{VM} = V_{VDRAIN} = 48 V, ENABLE = 3.3 V, INHx/INLx = 0 V		8.5	13	mA
I_{VDRAIN}	VDRAIN operating supply current	V_{VM} = V_{VDRAIN} = 48 V, ENABLE = 3.3 V, INHx/INLx = 0 V		1.9	4	mA
I_{SLEEP}	Sleep mode supply current	ENABLE = 0 V, V_{VM} = V_{VDRAIN} = 48 V, T_A = 25°C		20	40	µA
		ENABLE = 0 V, V_{VM} = V_{VDRAIN} = 48 V, T_A = 125°C			100	
t_{RST}	Reset pulse time	ENABLE = 0 V period to reset faults	5		40	us
t_{WAKE}	Turnon time	V_{VM} > V_{UVLO}, ENABLE = 3.3 V to outputs ready			1	ms
t_{SLEEP}	Turnoff time	ENABLE = 0 V to device sleep mode			1	ms
V_{DVDD}	DVDD regulator voltage	I_{DVDD} = 0 to 10 mA	4.75	5	5.25	V
V_{VCP}	VCP operating voltage with respect to VDRAIN	V_{VM} = 15 V, I_{VCP} = 0 to 25 mA	9	10.5	12	V
		V_{VM} = 12 V, I_{VCP} = 0 to 20 mA	7.5	10	11.5	
		V_{VM} = 10 V, I_{VCP} = 0 to 15 mA	6	8	9.5	
		V_{VM} = 9 V, I_{VCP} = 0 to 10 mA	5.5	7.5	8.5	
V_{VGLS}	VGLS operating voltage with respect to GND	V_{VM} = 15 V, I_{VGLS} = 0 to 25 mA	13	14.5	16	V
		V_{VM} = 12 V, I_{VGLS} = 0 to 20 mA	10	11.5	12.5	
		V_{VM} = 10 V, I_{VGLS} = 0 to 15 mA	8	9.5	10.5	
		V_{VM} = 9 V, I_{VGLS} = 0 to 10 mA	7	8.5	9.5	
LOGIC-LEVEL INPUTS (ENABLE, INHx, INLx, nSCS, SCLK, SDI)						
V_{IL}	Input logic low voltage		0		0.8	V
V_{IH}	Input logic high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			100		mV
I_{IL}	Input logic low current	V_{VIN} = 0 V	–5		5	µA
I_{IH}	Input logic high current	V_{VIN} = 5 V		50	70	µA
R_{PD}	Pulldown resistance	To GND		100		kΩ
t_{PD}	Propagation delay	INHx/INLx transition to GHx/GLx transition		200		ns
FOUR-LEVEL H/W INPUTS (GAIN, MODE)						
V_{I1}	Input mode 1 voltage	Tied to GND		0		V
V_{COMP1}	Quad-level voltage comparator 1	Voltage comparator between V_{I1} and V_{I2}	1.156	1.256	1.356	V
V_{I2}	Input mode 2 voltage	47 kΩ ± 5% to tied GND		1.9		V
V_{COMP2}	Quad-level voltage comparator 1	Voltage comparator between V_{I2} and V_{I3}	2.408	2.508	2.608	V
V_{I3}	Input mode 3 voltage	Hi-Z		3.1		V
V_{COMP3}	Quad-level voltage comparator 3	Voltage comparator between V_{I3} and V_{I4}	3.614	3.714	3.814	V
V_{I4}	Input mode 4 voltage	Tied to DVDD		5		V
R_{PU}	Pullup resistance	Internal pullup to DVDD		50		kΩ
R_{PD}	Pulldown resistance	Internal pulldown to GND		84		kΩ
SEVEN-LEVEL H/W INPUTS (IDRIVE, VDS)						
V_{I1}	Input mode 1 voltage	Tied to GND		0		V
V_{COMP1}	Seven-level voltage comparator 1	Voltage comparator between V_{I1} and V_{I2}	0.057	0.157	0.257	V
V_{I2}	Input mode 2 voltage	18 kΩ ± 5% tied to GND		0.8		V
V_{COMP2}	Seven-level voltage comparator 2	Voltage comparator between V_{I2} and V_{I3}	1.158	1.258	1.358	V
V_{I3}	Input mode 3 voltage	75 kΩ ± 5% tied to GND		1.7		V
V_{COMP3}	Seven-level voltage comparator 3	Voltage comparator between V_{I3} and V_{I4}	2.257	2.357	2.457	V
V_{I4}	Input mode 4 voltage	Hi-Z		2.5		V

at T_A = –55°C to +125°C, V_{VM} = 9 to 75 V, V_{VDRAIN} = 9 to 100 V, V_{VIN} = 48 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{COMP4}	Seven-level voltage comparator 4	Voltage comparator between V_{I4} and V_{I5}	2.561	2.661	2.761	V
V_{I5}	Input mode 5 voltage	75 kΩ ± 5% tied to DVDD		3.3		V
V_{COMP5}	Seven-level voltage comparator 5	Voltage comparator between V_{I5} and V_{I6}	3.615	3.715	3.815	V
V_{I6}	Input mode 6 voltage	18 kΩ ± 5% tied to DVDD		4.2		V
V_{COMP6}	Seven-level voltage comparator 6	Voltage comparator between V_{I6} and V_{I7}	4.74	4.85	4.95	V
V_{I7}	Input mode 7 voltage	Tied to DVDD		5		V
R_{PU}	Pullup resistance	Internal pullup to DVDD		73		kΩ
R_{PD}	Pulldown resistance	Internal pulldown to GND		73		kΩ
OPEN DRAIN OUTPUTS (nFAULT, SDO)						
V_{OL}	Output logic low voltage	I_O = 5 mA			0.125	V
I_{OZ}	Output high impedance leakage	V_O = 5 V	–2		2	μA

at T_A = –55°C to +125°C, V_{VM} = 9 to 75 V, V_{VDRAIN} = 9 to 100 V, V_{VIN} = 48 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE DRIVERS (GHx, GLx)							
V_{GSH}	High-side gate drive voltage with respect to SHx		V_{VM} = 15 V, I_{VCP} = 0 to 25 mA	9	10.5	12	V
			V_{VM} = 12 , I_{VCP} = 0 to 20 mA	7.5	10	11.5	
			V_{VM} = 10 V, I_{VCP} = 0 to 15 mA	6	8	9.5	
			V_{VM} = 9 V, I_{VCP} = 0 to 10 mA	5.5	7.5	8.5	
V_{GSL}	Low-side gate drive voltage with respect to PGND		V_{VM} = 15 V, I_{VGLS} = 0 to 25 mA	9.5	11	12.5	V
			V_{VM} = 12 V, I_{VGLS} = 0 to 20 mA	9	10.5	12	
			V_{VM} = 10 V, I_{VGLS} = 0 to 15 mA	7.5	9	10.5	
			V_{VM} = 9 V, I_{VGLS} = 0 to 10 mA	6.5	8	9.5	
t_{DEAD}	Gate drive dead time	SPI Device	DEAD_TIME = 00b		50		ns
			DEAD_TIME = 01b		100		
			DEAD_TIME = 10b		200		
			DEAD_TIME = 11b		400		
		H/W Device			100		
t_{DRIVE}	Peak current gate drive time	SPI Device	TDRIVE = 00b		500		ns
			TDRIVE = 01b		1000		
			TDRIVE = 10b		2000		
			TDRIVE = 11b		4000		
		H/W Device			4000		
I_{DRIVEP}	Peak source gate current	SPI Device	IDRIVEP_HS or IDRIVEP_LS = 0000b		50		mA
			IDRIVEP_HS or IDRIVEP_LS = 0001b		50		
			IDRIVEP_HS or IDRIVEP_LS = 0010b		100		
			IDRIVEP_HS or IDRIVEP_LS = 0011b		150		
			IDRIVEP_HS or IDRIVEP_LS = 0100b		300		
			IDRIVEP_HS or IDRIVEP_LS = 0101b		350		
			IDRIVEP_HS or IDRIVEP_LS = 0110b		400		
			IDRIVEP_HS or IDRIVEP_LS = 0111b		450		
			IDRIVEP_HS or IDRIVEP_LS = 1000b		550		
			IDRIVEP_HS or IDRIVEP_LS = 1001b		600		
			IDRIVEP_HS or IDRIVEP_LS = 1010b		650		
			IDRIVEP_HS or IDRIVEP_LS = 1011b		700		
			IDRIVEP_HS or IDRIVEP_LS = 1100b		850		
			IDRIVEP_HS or IDRIVEP_LS = 1101b		900		
			IDRIVEP_HS or IDRIVEP_LS = 1110b		950		
			IDRIVEP_HS or IDRIVEP_LS = 1111b		1000		
		H/W Device	IDRIVE = Tied to GND		50		
			IDRIVE = 18 kΩ ± 5% tied to GND		100		
			IDRIVE = 75 kΩ ± 5% tied to GND		150		
			IDRIVE = Hi-Z		300		
			IDRIVE = 75 kΩ ± 5% tied to DVDD		450		
			IDRIVE = 18 kΩ ± 5% tied to DVDD		700		
			IDRIVE = Tied to DVDD		1000		

at T_A = –55°C to +125°C, V_{VM} = 9 to 75 V, V_{VDRAIN} = 9 to 100 V, V_{VIN} = 48 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRIVEN}	Peak sink gate current	SPI Device	IDRIVEN_HS or IDRIVEN_LS = 0000b		100		mA
			IDRIVEN_HS or IDRIVEN_LS = 0001b		100		
			IDRIVEN_HS or IDRIVEN_LS = 0010b		200		
			IDRIVEN_HS or IDRIVEN_LS = 0011b		300		
			IDRIVEN_HS or IDRIVEN_LS = 0100b		600		
			IDRIVEN_HS or IDRIVEN_LS = 0101b		700		
			IDRIVEN_HS or IDRIVEN_LS = 0110b		800		
			IDRIVEN_HS or IDRIVEN_LS = 0111b		900		
			IDRIVEN_HS or IDRIVEN_LS = 1000b		1100		
			IDRIVEN_HS or IDRIVEN_LS = 1001b		1200		
			IDRIVEN_HS or IDRIVEN_LS = 1010b		1300		
			IDRIVEN_HS or IDRIVEN_LS = 1011b		1400		
			IDRIVEN_HS or IDRIVEN_LS = 1100b		1700		
			IDRIVEN_HS or IDRIVEN_LS = 1101b		1800		
			IDRIVEN_HS or IDRIVEN_LS = 1110b		1900		
			IDRIVEN_HS or IDRIVEN_LS = 1111b		2000		
		H/W Device	IDRIVE = Tied to GND		100		
			IDRIVE = 18 kΩ ± 5% tied to GND		200		
			IDRIVE = 75 kΩ ± 5% tied to GND		300		
			IDRIVE = Hi-Z		600		
			IDRIVE = 75 kΩ ± 5% tied to DVDD		900		
			IDRIVE = 18 kΩ ± 5% tied to DVDD		1400		
			IDRIVE = Tied to DVDD		2000		
I_{HOLD}	Gate holding current		Source current after t_{DRIVE}		50		mA
			Sink current after t_{DRIVE}		100		
I_{STRONG}	Gate strong pulldown current		GHx to SHx and GLx to SPx/SLx		2		A
R_{OFF}	Gate hold off resistor		GHx to SHx and GLx to SPx/SLx		150		kΩ
CURRENT SHUNT AMPLIFIER (SNx, SOx, SPx, VREF)							
G_{CSA}	Amplifier gain	SPI Device	CSA_GAIN = 00b	4.85	5	5.15	V/V
			CSA_GAIN = 01b	9.7	10	10.3	
			CSA_GAIN = 10b	19.4	20	20.6	
		SPI Device	CSA_GAIN = 11b	38.8	40	41.2	
		H/W Device	GAIN = Tied to GND	4.85	5	5.15	
		H/W Device	GAIN = 47 kΩ ± 5% tied to GND	9.7	10	10.3	
		H/W Device	GAIN = Hi-Z	19.4	20	20.6	
		H/W Device	GAIN = Tied to DVDD	38.8	40	41.2	
t_{SET}	Settling time to ±1%		V_{O_STEP} = 0.5 V, G_{CSA} = 5 V/V		250		ns
			V_{O_STEP} = 0.5 V, G_{CSA} = 10 V/V		500		
			V_{O_STEP} = 0.5 V, G_{VSA} = 20 V/V		1000		
			V_{O_STEP} = 0.5 V, G_{CSA} = 40 V/V		2000		
V_{COM}	Common mode input range			–0.15		0.15	V
V_{DIFF}	Differential mode input range			–0.3		0.3	V
V_{OFF}	Input offset error		V_{SP} = V_{SN} = 0 V	–3		3	mV
V_{DRIFT}	Drift offset		V_{SP} = V_{SN} = 0 V		10		µV/°C
V_{LINEAR}	SOx output voltage linear range			0.25		V_{VREF} – 0.25	V

at T_A = –55°C to +125°C, V_{VM} = 9 to 75 V, V_{VDRAIN} = 9 to 100 V, V_{VIN} = 48 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BIAS}	SOx output voltage bias	SPI Device	V_{SP} = V_{SN} = 0 V, VREF_DIV = 0b		V_{VREF} – 0.3		V
		SPI Device	V_{SP} = V_{SN} = 0 V, VREF_DIV = 1b		V_{VREF} / 2		
		H/W Device	V_{SP} = V_{SN} = 0 V		V_{VREF} / 2		
I_{BIAS}	SPx/SNx input bias current					250	µA
V_{SLEW}	SOx output slew rate		60-pF load		10		V/µs
I_{VREF}	VREF input current		V_{VREF} = 5 V		1.5	2.5	mA
UGB	Unity gain bandwidth		DRV835x: 60-pF load		10		MHz
PROTECTION CIRCUITS							
V_{VM_UV}	VM undervoltage lockout		DRV835x: VM falling, UVLO report	8.0	8.3	8.8	V
			DRV835x: VM rising, UVLO recovery	8.2	8.5	9.0	
V_{VM_UVH}	VM undervoltage hysteresis		Rising to falling threshold		200		mV
t_{VM_UVD}	VM undervoltage deglitch time		VM falling, UVLO report		10		us
V_{VDR_UV}	VDRAIN undervoltage lockout		DRV835x: VDRAIN falling, UVLO report	6.1	6.4	6.8	V
			DRV835x: VDRAIN rising, UVLO recovery	6.3	6.6	7.0	
V_{VDR_UVH}	VDRAIN undervoltage hysteresis		Rising to falling threshold		150		mV
t_{VDR_UVD}	VDRAIN undervoltage deglitch time		VDRAIN falling, UVLO report		10		us
V_{VCP_UV}	VCP charge pump undervoltage lockout		VCP falling, GDUV report		V_{DRAIN} + 5		V
V_{VGLS_UV}	VGLS low-side regulator undervoltage lockout		VGLS falling, GDUV report		4.25		V
V_{GS_CLAMP}	High-side gate clamp		Positive clamping voltage	12.5	13.5	16	V
			Negative clamping voltage		–0.7		
V_{VDS_OCP}	V_{DS} overcurrent trip voltage	SPI Device	VDS_LVL = 0000b	0.041	0.06	0.082	V
			VDS_LVL = 0001b	0.051	0.07	0.094	
			VDS_LVL = 0010b	0.061	0.08	0.106	
			VDS_LVL = 0011b	0.071	0.09	0.118	
			VDS_LVL = 0100b	0.081	0.1	0.125	
			VDS_LVL = 0101b	0.18	0.2	0.24	
			VDS_LVL = 0110b	0.27	0.3	0.345	
			VDS_LVL = 0111b	0.36	0.4	0.455	
			VDS_LVL = 1000b	0.45	0.5	0.565	
			VDS_LVL = 1001b	0.54	0.6	0.67	
			VDS_LVL = 1010b	0.63	0.7	0.78	
			VDS_LVL = 1011b	0.72	0.8	0.885	
			VDS_LVL = 1100b	0.81	0.9	1.0	
			VDS_LVL = 1101b	0.9	1.0	1.1	
			VDS_LVL = 1110b	1.35	1.5	1.65	
			VDS_LVL = 1111b	1.8	2	2.2	V
		H/W Device	VDS = 75 kΩ ± 5% tied to GND	0.18	0.2	0.24	V
			VDS = Hi-Z	0.36	0.4	0.455	
			VDS = 75 kΩ ± 5% tied to DVDD	0.63	0.7	0.78	
			VDS = 18 kΩ ± 5% tied to DVDD	0.9	1	1.1	
V_{VDS_OCP}	V_{DS} overcurrent trip voltage		VDS = Tied to DVDD		Disabled		

at T_A = –55°C to +125°C, V_{VM} = 9 to 75 V, V_{VDRAIN} = 9 to 100 V, V_{VIN} = 48 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OCP_DEG}	V_{DS} and V_{SENSE} overcurrent deglitch time	SPI Device	OCP_DEG = 00b		1		us
			OCP_DEG = 01b		2		
			OCP_DEG = 10b		4		
			OCP_DEG = 11b		8		
		H/W Device			4		
V_{SEN_OCP}	V_{SENSE} overcurrent trip voltage	SPI Device	SEN_LVL = 00b		0.25		V
			SEN_LVL = 01b		0.5		
			SEN_LVL = 10b		0.75		
			SEN_LVL = 11b		1		
		H/W Device			1		
t_{RETRY}	Overcurrent retry time	SPI Device	TRETRY = 0b		8		ms
			TRETRY = 1b		50		us
		H/W Device			8		ms
T_{OTW}	Thermal warning temperature		Die temperature, T_J	130	150	170	°C
T_{OTSD}	Thermal shutdown temperature		Die temperature, T_J	150	170	190	°C
T_{HYS}	Thermal hysteresis		Die temperature, T_J		20		°C

12 SPI Timing Requirements

at T_A = –40°C to +125°C, V_{VM} = 9 to 75 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{READY}	SPI ready after enable	VM > UVLO, ENABLE = 3.3 V			1	ms
t_{CLK}	SCLK minimum period		100			ns
t_{CLKH}	SCLK minimum high time		50			ns
t_{CLKL}	SCLK minimum low time		50			ns
t_{SU_SDI}	SDI input data setup time		20			ns
t_{H_SDI}	SDI input data hold time		30			ns
t_{D_SDO}	SDO output data delay time	SCLK high to SDO valid			30	ns
t_{SU_nSCS}	nSCS input setup time		50			ns
t_{H_nSCS}	nSCS input hold time		50			ns
t_{HI_nSCS}	nSCS minimum high time before active low		400			ns
t_{DIS_nSCS}	nSCS disable time	nSCS high to SDO high impedance		10		ns

13 Detailed Description

13.1 Overview

The DRV8353M family of devices are integrated 100-V gate drivers for three-phase motor drive applications. These devices decrease system component count, cost, and complexity by integrating three independent half-bridge gate drivers, charge pump and linear regulator for the high-side and low-side gate driver supply voltages, optional triple current shunt amplifiers, and an optional 350-mA buck regulator. A standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller. Alternatively, a hardware interface (H/W) option allows for configuring the most commonly used settings through fixed external resistors.

The gate drivers support external N-channel high-side and low-side power MOSFETs and can drive up to 1-A source, 2-A sink peak currents with a 25-mA average output current. The high-side gate drive supply voltage is generated using a doubler charge-pump architecture that regulates the VCP output to V_{VDRAIN} + 10.5-V. The low-side gate drive supply voltage is generated using a linear regulator from the VM power supply that regulates the VGLS output to 14.5-V. The VGLS supply is further regulated to 11-V on the GLx low-side gate driver outputs. A smart gate-drive architecture provides the ability to dynamically adjust the output gate-drive current strength allowing for the gate driver to control the power MOSFET V_{DS} switching speed. This allows for the removal of external gate drive resistors and diodes reducing BOM component count, cost, and PCB area. The architecture also uses an internal state machine to protect against gate-drive short-circuit events, control the half-bridge dead time, and protect against dV/dt parasitic turnon of the external power MOSFET.

The gate drivers can operate in either a single or dual supply architecture. In the single supply architecture, VM can be tied to VDRAIN and is regulated to the correct supply voltages internally. In the dual supply architecture, VM can be connected to a lower voltage supply from a more efficient switching regulator to improve the device efficiency. VDRAIN stays connected to the external MOSFETs to set the correct charge pump and overcurrent monitor reference.

The DRV8353 devices integrate three, bidirectional current-shunt amplifiers for monitoring the current level through each of the external half-bridges using a low-side shunt resistor. The gain setting of the shunt amplifier can be adjusted through the SPI or hardware interface with the SPI providing additional flexibility to adjust the output bias point.

In addition to the high level of device integration, the DRV8353M family of devices provides a wide range of integrated protection features. These features include power-supply undervoltage lockout (UVLO), gate drive undervoltage lockout (GDUV), V_{DS} overcurrent monitoring (OCP), gate-driver short-circuit detection (GDF), and overtemperature shutdown (OTW/OTSD). Fault events are indicated by the nFAULT pin with detailed information available in the SPI registers on the SPI device version.

The DRV8353M family of devices are available in 0.5-mm pin pitch, QFN surface-mount package. The QFN size is 6 × 6 mm for the 40-pin package.

13.2 Functional Block Diagram

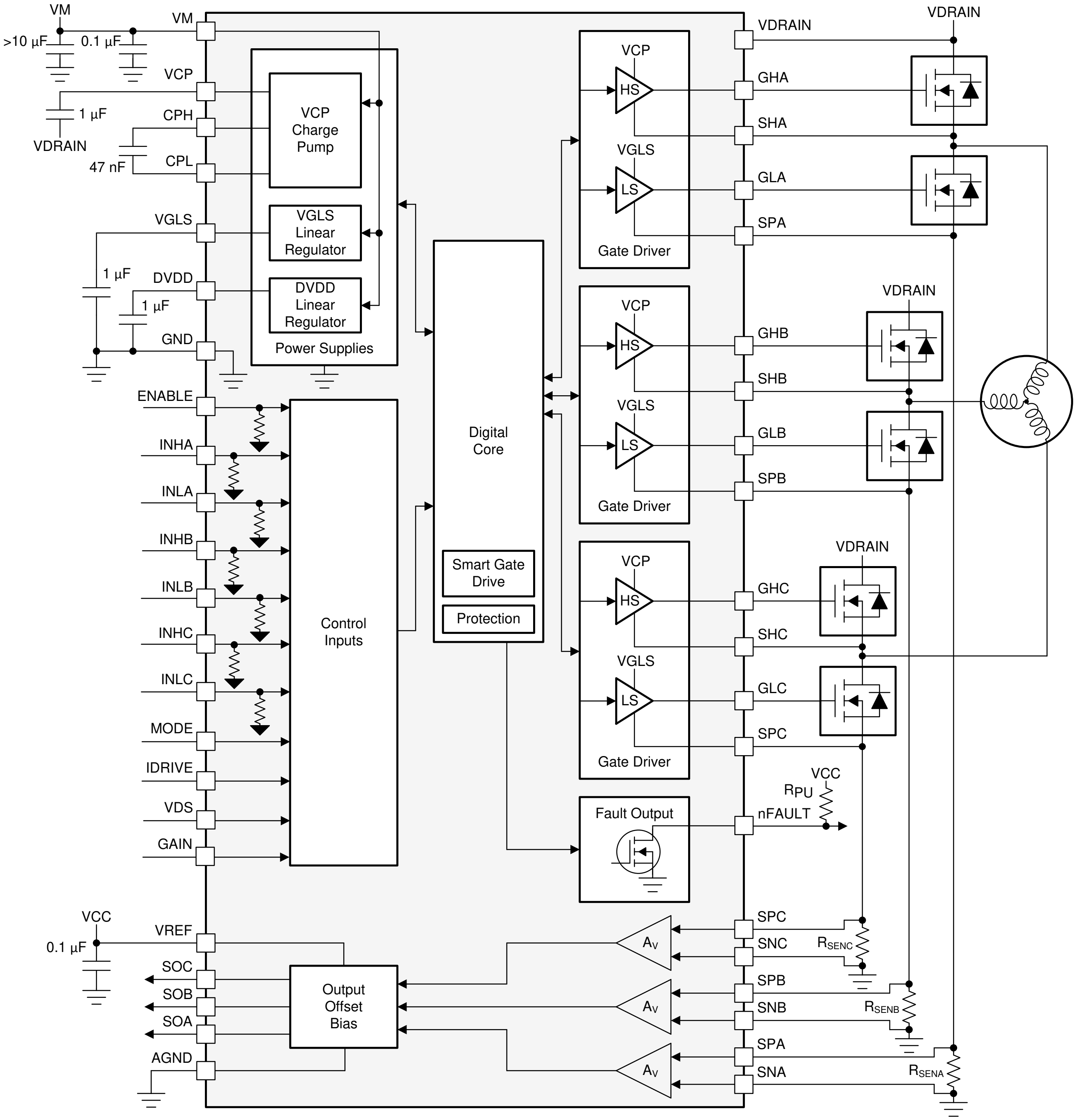


図 13-1. Block Diagram for DRV8353HM

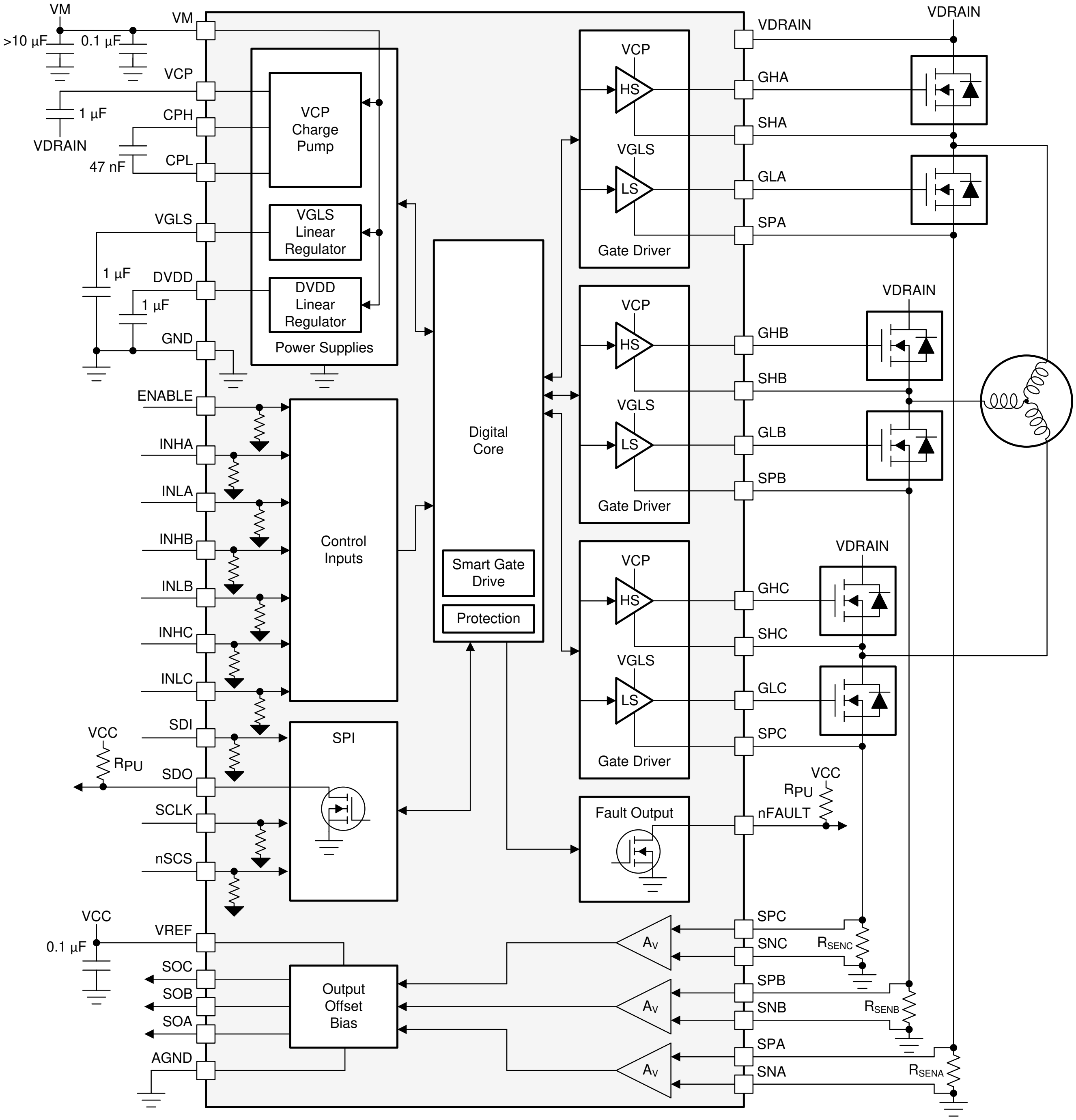


図 13-2. Block Diagram for DRV8353SM

13.3 Feature Description

13.3.1 Three Phase Smart Gate Drivers

The DRV8353M family of devices integrates three, half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. The VCP doubler charge pump provides the correct gate bias voltage to the high-side MOSFET across a wide operating voltage range in addition to providing 100% duty-cycle support. The internal VGLS linear regulator provides the gate-bias voltage for the low-side MOSFETs. The half-bridge gate drivers can be used in combination to drive a three-phase motor or separately to drive other types of loads.

The DRV8353M family of devices implement a smart gate-drive architecture which allows the user to dynamically adjust the gate drive current without requiring external gate current limiting resistors. Additionally, this architecture provides a variety of protection features for the external MOSFETs including automatic dead-time insertion, parasitic dV/dt gate turnon prevention, and gate-fault detection.

13.3.1.1 PWM Control Modes

The DRV8353M family of devices provides four different PWM control modes to support various commutation and control methods. Texas Instruments does not recommend changing the MODE pin or PWM_MODE register during operation of the power MOSFETs. Set all INHx and INLx pins to logic low before making a MODE or PWM_MODE change.

13.3.1.1.1 6x PWM Mode (PWM_MODE = 00b or MODE Pin Tied to AGND)

In this mode, each half-bridge supports three output states: low, high, or high-impedance (Hi-Z). The corresponding INHx and INLx signals control the output state as listed in 表 13-1.

表 13-1. 6x PWM Mode Truth Table

INLx	INHx	GLx	GHx	SHx
0	0	L	L	Hi-Z
0	1	L	H	H
1	0	H	L	L
1	1	L	L	Hi-Z

13.3.1.1.2 3x PWM Mode (PWM_MODE = 01b or MODE Pin = 47 kΩ to AGND)

In this mode, the INHx pin controls each half-bridge and supports two output states: low or high. The INLx pin is used to change the half-bridge to high impedance. If the high-impedance (Hi-Z) sate is not required, tie all INLx pins logic high. The corresponding INHx and INLx signals control the output state as listed in 表 13-2.

表 13-2. 3x PWM Mode Truth Table

INLx	INHx	GLx	GHx	SHx
0	X	L	L	Hi-Z
1	0	H	L	L
1	1	L	H	H

13.3.1.1.3 1x PWM Mode (PWM_MODE = 10b or MODE Pin = Hi-Z)

In this mode, the DRV8353M family of devices uses 6-step block commutation tables that are stored internally. This feature allows for a three-phase BLDC motor to be controlled using a single PWM sourced from a simple controller. The PWM is applied on the INHA pin and determines the output frequency and duty cycle of the half-bridges.

The half-bridge output states are managed by the INLA, INHB, and INLB pins which are used as state logic inputs. The state inputs can be controlled by an external controller or connected directly to hall sensor digital outputs from the motor (INLA = HALL_A, INHB = HALL_B, INLB = HALL_C). The 1x PWM mode usually operates with synchronous rectification, however it can be configured to use asynchronous diode freewheeling rectification on SPI devices. This configuration is set using the 1PWM_COM bit through the SPI registers.

The INHC input controls the direction through the 6-step commutation table which is used to change the direction of the motor when hall sensors are directly controlling the INLA, INHB, and INLB state inputs. Tie the INHC pin low if this feature is not required.

The INLC input brakes the motor by turning off all high-side MOSFETs and turning on all low-side MOSFETs when it is pulled low. This brake is independent of the states of the other input pins. Tie the INLC pin high if this feature is not required.

表 13-3. Synchronous 1x PWM Mode

LOGIC AND HALL INPUTS							GATE-DRIVE OUTPUTS						
STATE	INHC = 0			INHC = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	INLA	INHB	INLB	INLA	INHB	INLB	GHA	GLA	GHB	GLB	GHC	GLC	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	!PWM	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	!PWM	L	H	B → C
2	1	0	0	0	1	1	PWM	!PWM	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	!PWM	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	!PWM	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	!PWM	C → A
6	0	1	0	1	0	1	L	H	PWM	!PWM	L	L	B → A

表 13-4. Asynchronous 1x PWM Mode 1PWM_COM = 1 (SPI Only)

LOGIC AND HALL INPUTS							GATE-DRIVE OUTPUTS						
STATE	INHC = 0			INHC = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	INLA	INHB	INLB	INLA	INHB	INLB	GHA	GLA	GHB	GLB	GHC	GLC	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	L	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	L	L	H	B → C
2	1	0	0	0	1	1	PWM	L	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	L	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	L	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	L	C → A
6	0	1	0	1	0	1	L	H	PWM	L	L	L	B → A

図 13-3 and 図 13-4 show the different possible configurations in 1x PWM mode.

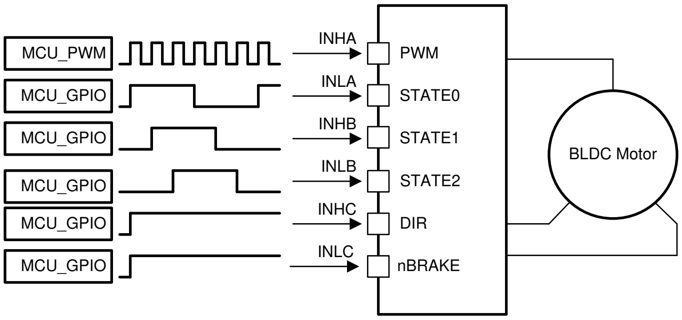


図 13-3. 1x PWM—Simple Controller

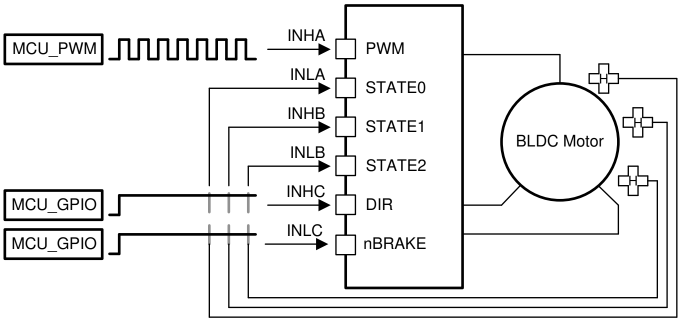


図 13-4. 1x PWM—Hall Sensor

13.3.1.1.4 Independent PWM Mode (PWM_MODE = 11b or MODE Pin Tied to DVDD)

In this mode, the corresponding input pin independently controls each high-side and low-side gate driver. This control mode allows for the external controller to bypass the internal dead-time handshake of the DRV8353M or to utilize the high-side and low-side drivers to drive separate high-side and low-side loads with each half-bridge. These types of loads include unidirectional brushed DC motors, solenoids, and low-side and high-side switches. In this mode, If the system is configured in a half-bridge configuration, shoot-through occurs when the high-side and low-side MOSFETs are turned on at the same time.

表 13-5. Independent PWM Mode Truth Table

INLx	INHx	GLx	GHx
0	0	L	L
0	1	L	H
1	0	H	L
1	1	H	H

Because the high-side and low-side V_{DS} overcurrent monitors share the SHx sense line, using both of the monitors is not possible if both the high-side and low-side gate drivers are being operated independently.

In this case, connect the SHx pin to the high-side driver and disable the V_{DS} overcurrent monitors as shown in 図 13-5.

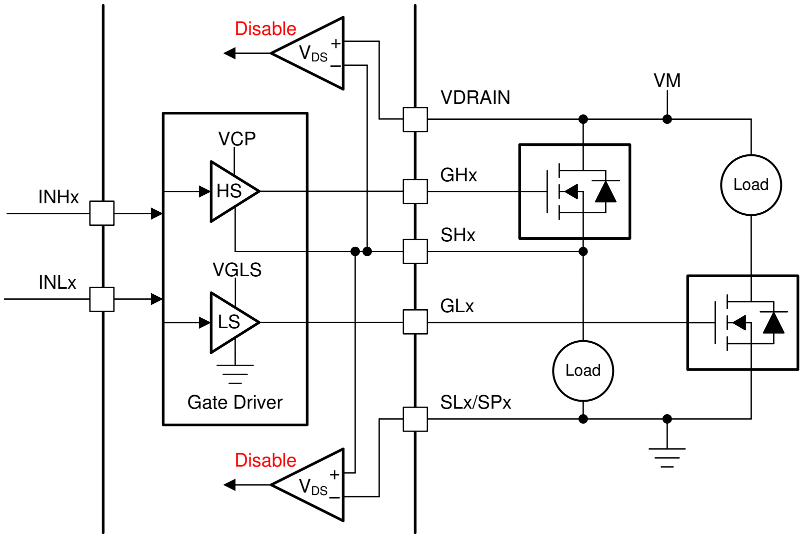


図 13-5. Independent PWM High-Side and Low-Side Drivers

If the half-bridge is used to implement only a high-side or low-side driver, using the V_{DS} overcurrent monitors is still possible. Connect the SHx pin as shown in 図 13-6 or 図 13-7. The unused gate driver and the corresponding input can be left disconnected.

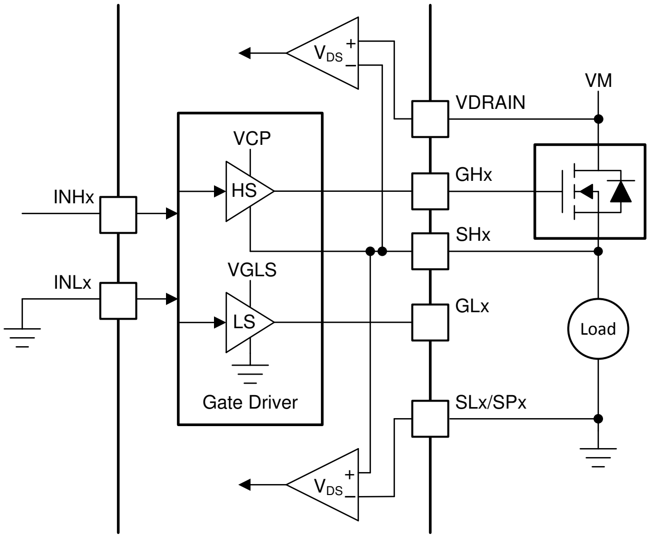


図 13-6. Single High-Side Driver

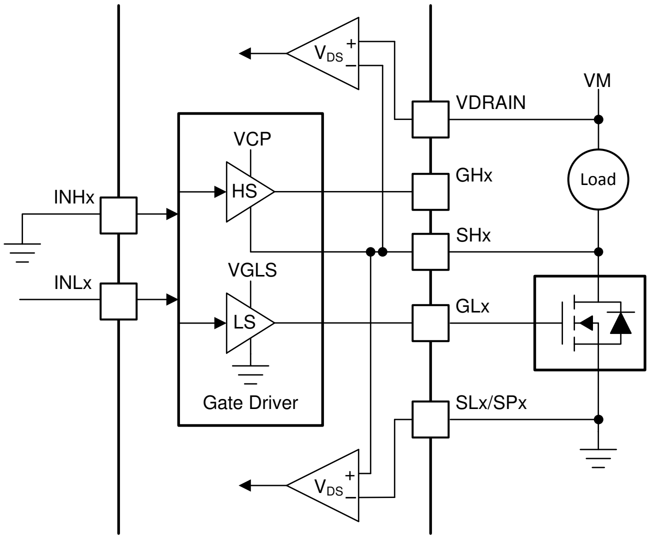


図 13-7. Single Low-Side Driver

13.3.1.2 Device Interface Modes

The DRV8353M family of devices support two different interface modes (SPI and hardware) to allow the end application to design for either flexibility or simplicity. The two interface modes share the same four pins, allowing the different versions to be pin to pin compatible. This allows for application designers to evaluate with one interface version and potentially switch to another with minimal modifications to their design.

13.3.1.2.1 Serial Peripheral Interface (SPI)

The SPI devices support a serial communication bus that allows for an external controller to send and receive data with the DRV835x. This allows for the external controller to configure device settings and read detailed fault information. The interface is a four wire interface utilizing the SCLK, SDI, SDO, and nSCS pins.

- The SCLK pin is an input which accepts a clock signal to determine when data is captured and propagated on SDI and SDO.
- The SDI pin is the data input.
- The SDO pin is the data output. The SDO pin uses an open-drain structure and requires an external pullup resistor.
- The nSCS pin is the chip select input. A logic low signal on this pin enables SPI communication with the DRV835x.

For more information on the SPI, see the *セクション 13.5.1* section.

13.3.1.2.2 Hardware Interface

Hardware interface devices convert the four SPI pins into four resistor configurable inputs, GAIN, IDRIVE, MODE, and VDS. This allows for the application designer to configure the most commonly used device settings by tying the pin logic high or logic low, or with a simple pullup or pulldown resistor. This removes the requirement for an SPI bus from the external controller. General fault information can still be obtained through the nFAULT pin.

- The GAIN pin configures the current shunt amplifier gain.
- The IDRIVE pin configures the gate drive current strength.
- The MODE pin configures the PWM control mode.
- The VDS pin configures the voltage threshold of the V_{DS} overcurrent monitors.

For more information on the hardware interface, see the *セクション 13.3.3* section.

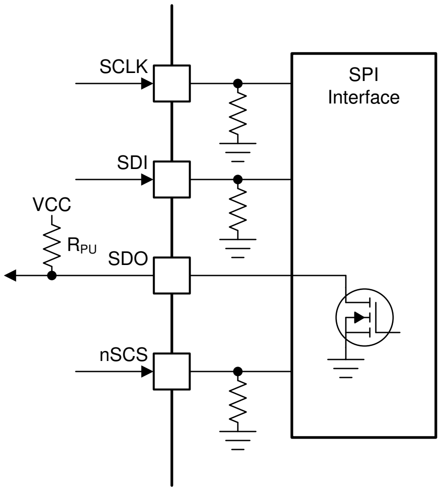


図 13-8. SPI

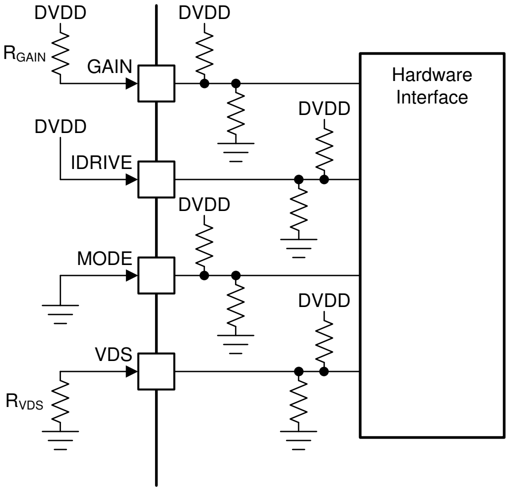


図 13-9. Hardware Interface

13.3.1.3 Gate Driver Voltage Supplies and Input Supply Configurations

The high-side gate-drive voltage supply is created using a doubler charge pump that operates from the VM and VDRAIN voltage supply inputs. The charge pump allows the gate driver to correctly bias the high-side MOSFET gate with respect to the source across a wide input supply voltage range. The charge pump is regulated to keep a fixed output voltage of V_{VDRAIN} + 10.5 V and supports an average output current of 25 mA. When V_{VM} is less than 12 V, the charge pump operates in full doubler mode and generates $V_{VCP} = 2 \times V_{VM} - 1.5$ V with respect to V_{VDRAIN} when unloaded. The charge pump is continuously monitored for undervoltage to prevent under-driven MOSFET conditions.

The charge pump requires a X5R or X7R, 1-µF, 16-V ceramic capacitor between the VDRAIN and VCP pins to act as the storage capacitor. Additionally, a X5R or X7R, 47-nF, VDRAIN-rated ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

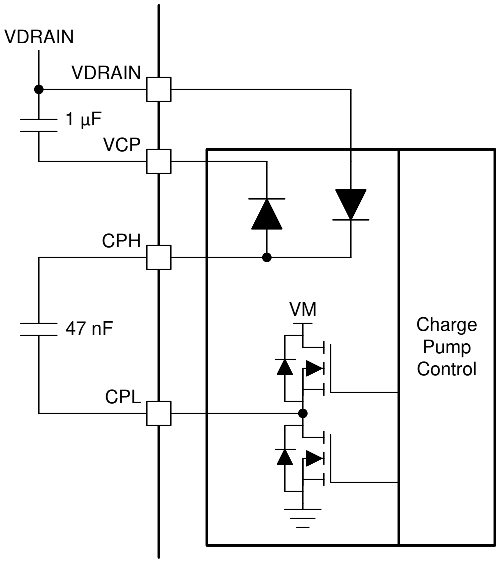


図 13-10. Charge Pump Architecture

The low-side gate drive voltage is created using a linear regulator that operates from the VM voltage supply input. The VGLS linear regulator allows the gate driver to correctly bias the low-side MOSFET gate with respect to ground. The VGLS linear regulator output is fixed at 14.5 V and further regulated to 11-V on the GLx outputs during operation. The VGLS regulator supports an output current of 25 mA. The VGLS linear regulator is monitored for undervoltage to prevent under driver MOSFET conditions. The VGLS linear regulator requires a X5R or X7R, 1-µF, 16-V ceramic capacitor between VGLS and GND.

Since the charge pump output is regulated to V_{VDRAIN} + 10.5 V this allows for VM to be supplied either directly from the high voltage motor supply (up to 75 V) to support a single supply system or from a low voltage gate driver power supply derived from a switching or linear regulator to improve the device efficiency or utilize an externally available power supply. 図 13-11 and 図 13-12 show examples of the DRV8353M configured in either single supply or dual supply configuration.

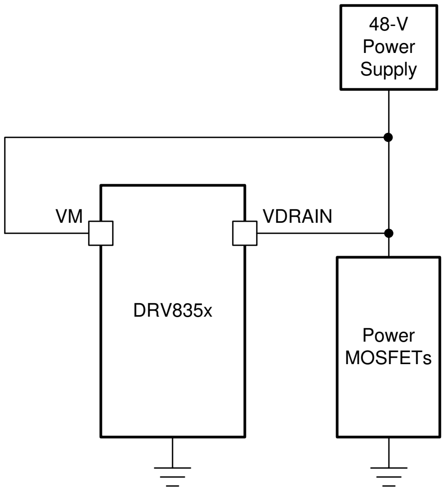


図 13-11. Single Supply Example

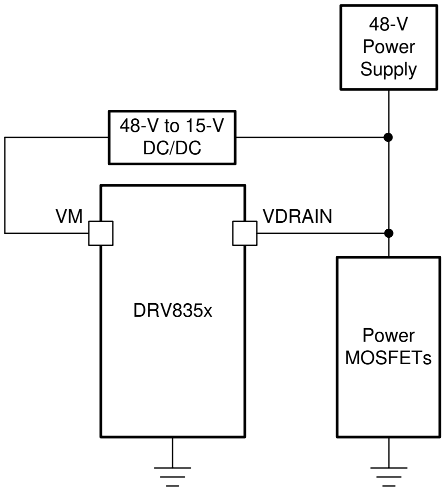


図 13-12. Dual Supply Example

13.3.1.4 Smart Gate Drive Architecture

The DRV8353M gate drivers use an adjustable, complimentary, push-pull topology for both the high-side and low-side drivers. This topology allows for both a strong pullup and pulldown of the external MOSFET gates.

Additionally, the gate drivers use a smart gate-drive architecture to provide additional control of the external power MOSFETs, take additional steps to protect the MOSFETs, and allow for optimal tradeoffs between efficiency and robustness. This architecture is implemented through two components called IDRIVE and TDRIVE which are detailed in the *セクション 13.3.1.4.1* section and *セクション 13.3.1.4.2* section. 図 13-13 shows the high-level functional block diagram of the gate driver.

The IDRIVE gate-drive current and TDRIVE gate-drive time should be initially selected based on the parameters of the external power MOSFET used in the system and the desired rise and fall times (see the *セクション 14* section).

The high-side gate driver also implements a Zener clamp diode to help protect the external MOSFET gate from overvoltage conditions in the case of external short-circuit events on the MOSFET.

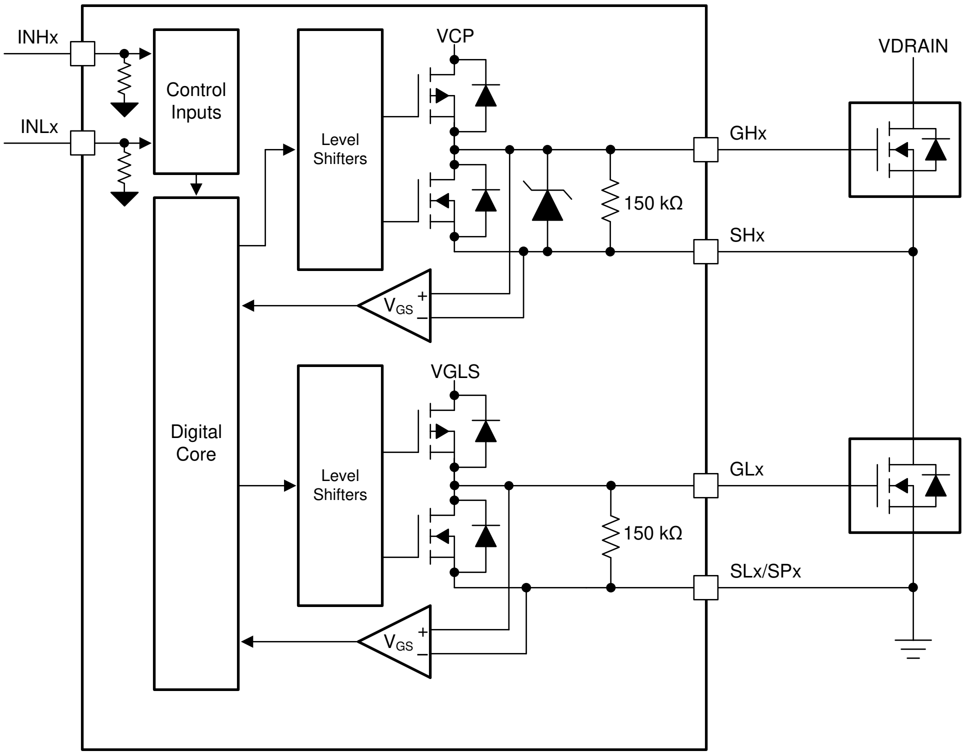


図 13-13. Gate Driver Block Diagram

13.3.1.4.1 IDRIVE: MOSFET Slew-Rate Control

The IDRIVE component implements adjustable gate-drive current to control the MOSFET V_{DS} slew rates. The MOSFET V_{DS} slew rates are a critical factor for optimizing radiated emissions, energy and duration of diode recovery spikes, dV/dt gate turnon leading to shoot-through, and switching voltage transients related to parasitics in the external half-bridge. IDRIVE operates on the principal that the MOSFET V_{DS} slew rates are predominately determined by the rate of gate charge (or gate current) delivered during the MOSFET Q_{GD} or Miller charging region. By allowing the gate driver to adjust the gate current, it can effectively control the slew rate of the external power MOSFETs.

IDRIVE allows the DRV8353M family of devices to dynamically switch between gate drive currents either through a register setting on SPI devices or the IDRIVE pin on hardware interface devices. The SPI devices provide 16 I_{DRIVE} settings ranging between 50-mA to 1-A source and 100-mA to 2-A sink. Hardware interface devices provides 7 I_{DRIVE} settings between the same ranges. The gate drive current setting is delivered to the gate during the turnon and turnoff of the external power MOSFET for the t_{DRIVE} duration. After the MOSFET turnon or turnoff, the gate driver switches to a smaller hold I_{HOLD} current to improve the gate driver efficiency. Additional details on the IDRIVE settings are described in the *セクション 13.6* section for the SPI devices and in the *セクション 13.3.3* section for the hardware interface devices.

13.3.1.4.2 TDRIVE: MOSFET Gate Drive Control

The TDRIVE component is an integrated gate-drive state machine that provides automatic dead time insertion through switching handshaking, parasitic dV/dt gate turnon prevention, and MOSFET gate-fault detection.

The first component of the TDRIVE state machine is automatic dead-time insertion. Dead time is period of time between the switching of the external high-side and low-side MOSFETs to make sure that they do not cross conduct and cause shoot-through. The DRV8353M family of devices use V_{GS} voltage monitors to measure the MOSFET gate-to-source voltage and determine the correct time to switch instead of relying on a fixed time value. This feature allows the gate-driver dead time to adjust for variation in the system such a temperature drift and variation in the MOSFET parameters. An additional digital dead time (t_{DEAD}) can be inserted and is adjustable through the registers on SPI devices.

The automatic dead-time insertion has a limitation when the gate driver is transitioning from high-side MOSFET on to low-side MOSFET on when the phase current is coming into the external half-bridge. In this case, the high-side diode will conduct during the dead-time and hold up the switch-node voltage to VDRAIN. In this case, an additional delay of approximately 100-200 ns is introduced into the dead-time handshake. This is introduced due to the need to discharge the voltage present on the internal V_{GS} detection circuit.

The second component focuses on parasitic dV/dt gate turnon prevention. To implement this, the TDRIVE state machine enables a strong pulldown I_{STRONG} current on the opposite MOSFET gate whenever a MOSFET is switching. The strong pulldown last for the TDRIVE duration. This feature helps remove parasitic charge that couples into the MOSFET gate when the half-bridge switch-node voltage slews rapidly.

The third component implements a gate-fault detection scheme to detect pin-to-pin solder defects, a MOSFET gate failure, or a MOSFET gate stuck-high or stuck-low voltage condition. This implementation is done with a pair of V_{GS} gate-to-source voltage monitors for each half-bridge gate driver. When the gate driver receives a command to change the state of the half-bridge it starts to monitor the gate voltage of the external MOSFET. If at the end of the t_{DRIVE} period the V_{GS} voltage has not reached the correct threshold the gate driver will report a fault. To make sure that a false fault is not detected, a t_{DRIVE} time should be selected that is longer than the time required to charge or discharge the MOSFET gate. The t_{DRIVE} time does not increase the PWM time and will terminate if another PWM command is received while active. Additional details on the TDRIVE settings are described in the *セクション 13.6* section for SPI devices and in the *セクション 13.3.3* section for hardware interface devices.

図 13-14 shows an example of the TDRIVE state machine in operation.

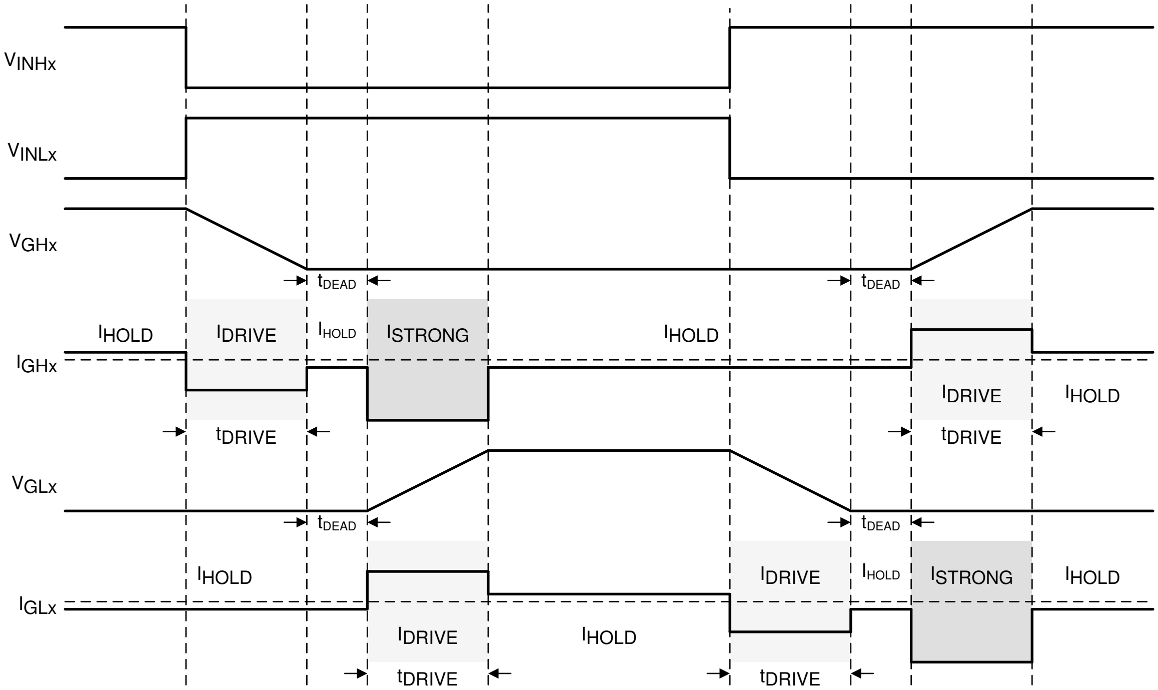


図 13-14. TDRIVE State Machine

13.3.1.4.3 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to a detected output change. This time has three parts consisting of the digital input deglitcher delay, the digital propagation delay, and the delay through the analog gate drivers.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. To support multiple control modes and dead time insertion, a small digital delay is added as the input command propagates through the device. Lastly, the analog gate drivers have a small delay that contributes to the overall propagation delay of the device.

13.3.1.4.4 MOSFET V_{DS} Monitors

The gate drivers implement adjustable V_{DS} voltage monitors to detect overcurrent or short-circuit conditions on the external power MOSFETs. When the monitored voltage is greater than the V_{DS} trip point (V_{VDS_OCP}) for longer than the deglitch time (t_{OCP}), an overcurrent condition is detected and action is taken according to the device V_{DS} fault mode.

The high-side V_{DS} monitors measure the voltage between the VDRAIN and SHx pins. The low-side V_{DS} monitors measure the voltage between the SHx and SPx pins. If the current shunt amplifier is unused, tie the SP pins to the common ground point of the external half-bridges.

For the SPI devices, the low-side V_{DS} monitor reference point can be changed between the SPx and SNx pins if desired with the LS_REF register setting. This is only for the low-side V_{DS} monitor. The high-side V_{DS} monitor stays between the VDRAIN and SHx pins.

The V_{VDS_OCP} threshold is programmable between 0.06 V and 2 V on SPI device and between 0.06 V and 1 V on hardware interface devices. Additional information on the V_{DS} monitor levels are described in the *セクション 13.6* section for SPI devices and in the *セクション 13.3.3* section hardware interface device.

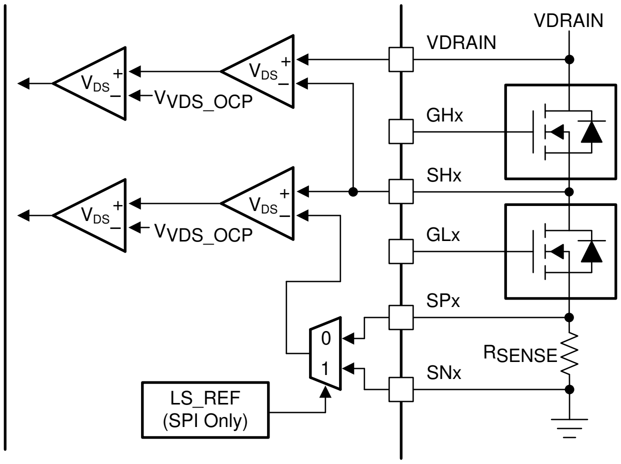


図 13-15. DRV8353M V_{DS} Monitors

13.3.1.4.5 VDRAIN Sense and Reference Pin

The DRV8353M family of devices provides a separate sense and reference pin for the common point of the high-side MOSFET drain. This pin is called VDRAIN. This pin allows the sense line for the overcurrent monitors (VDRAIN) and the power supply (VM) to stay separate and prevent noise on the VDRAIN sense line.

The VDRAIN pin serves as the reference point for the integrated charge pump. This makes sure that the charge pump reference stays with respect to the power MOSFET supply through voltage transient conditions.

Since the charge pump is referenced to VDRAIN, this also allows for VM to supplied either directed from the power MOSFET supply (VDRAIN) or from an independent supply. This allows for a configuration where VM can be supplied from an efficient low voltage supply to increase the device efficiency.

13.3.2 DVDD Linear Voltage Regulator

A 5-V, 10-mA linear regulator is integrated into the DRV8353M family of devices and is available for use by external circuitry. This regulator can provide the supply voltage for low-current supporting circuitry. The output of the DVDD regulator should be bypassed near the DVDD pin with a X5R or X7R, 1-μF, 6.3-V ceramic capacitor routed directly back to the adjacent DGND or GND ground pin.

The DVDD nominal, no-load output voltage is 5 V. When the DVDD load current exceeds 10 mA, the regulator functions like a constant-current source. The output voltage drops significantly with a current load greater than 10 mA.

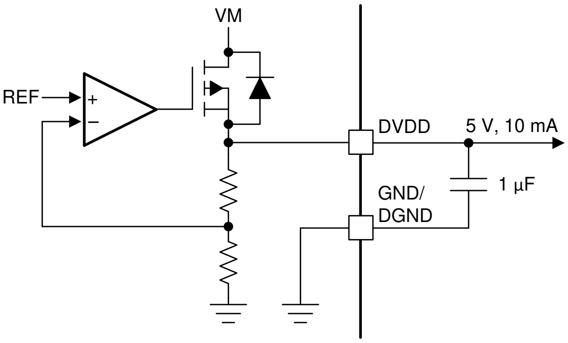


図 13-16. DVDD Linear Regulator Block Diagram

Use 式 1 to calculate the power dissipated in the device because of the DVDD linear regulator.

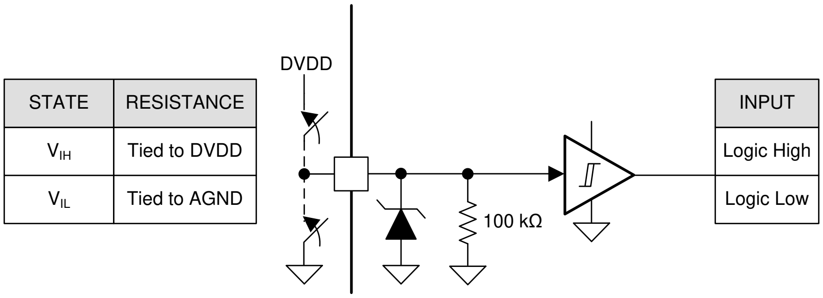
$$P = (V_{VM} - V_{DVDD}) \times I_{DVDD} \quad (1)$$

For example, at V_{VM} = 24 V, drawing 20 mA out of DVDD results in a power dissipation as shown in 式 2.

$$P = (24\ \text{V} - 3.3\ \text{V}) \times 20\ \text{mA} = 414\ \text{mW} \tag{2}$$

13.3.3 Pin Diagrams

図 13-17 shows the input structure for the logic-level pins, INHx, INLx, ENABLE, nSCS, SCLK, and SDI.

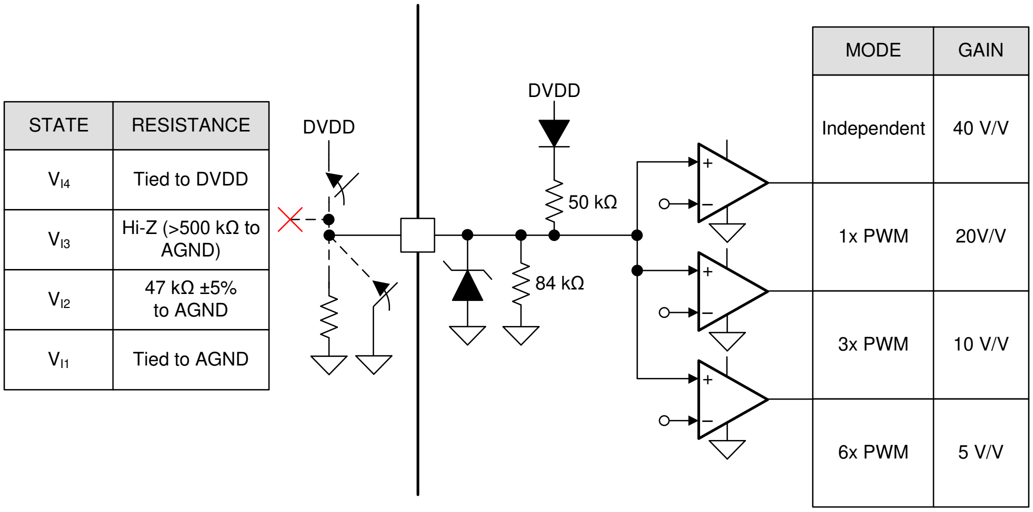


STATE	RESISTANCE
V_{IH}	Tied to DVDD
V_{IL}	Tied to AGND

INPUT
Logic High
Logic Low

図 13-17. Logic-Level Input Pin Structure

図 13-18 shows the structure of the four level input pins, MODE and GAIN, on hardware interface devices. The input can be set with an external resistor.

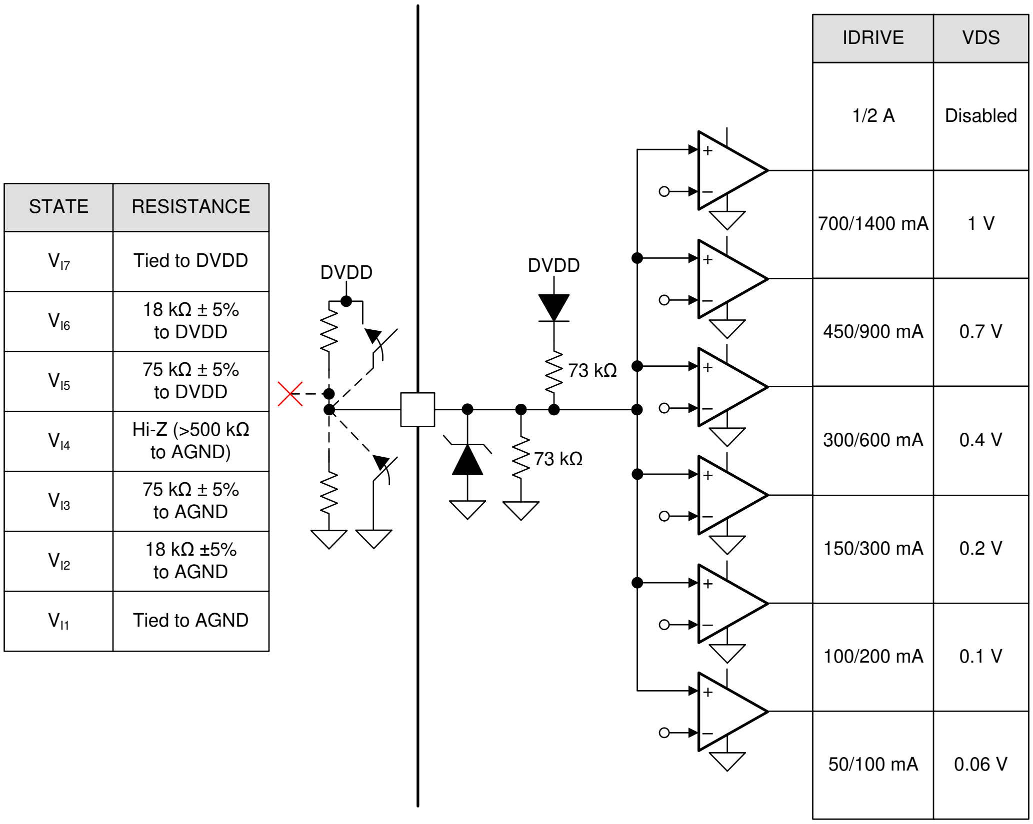


STATE	RESISTANCE
V_{I4}	Tied to DVDD
V_{I3}	Hi-Z (>500 kΩ to AGND)
V_{I2}	47 kΩ ±5% to AGND
V_{I1}	Tied to AGND

MODE	GAIN
Independent	40 V/V
1x PWM	20V/V
3x PWM	10 V/V
6x PWM	5 V/V

図 13-18. Four Level Input Pin Structure

図 13-19 shows the structure of the seven level input pins, IDRIVE and VDS, on hardware interface devices. The input can be set with an external resistor.



STATE	RESISTANCE
V_{I7}	Tied to DVDD
V_{I6}	18 kΩ ± 5% to DVDD
V_{I5}	75 kΩ ± 5% to DVDD
V_{I4}	Hi-Z (>500 kΩ to AGND)
V_{I3}	75 kΩ ± 5% to AGND
V_{I2}	18 kΩ ±5% to AGND
V_{I1}	Tied to AGND

IDRIVE	VDS
1/2 A	Disabled
700/1400 mA	1 V
450/900 mA	0.7 V
300/600 mA	0.4 V
150/300 mA	0.2 V
100/200 mA	0.1 V
50/100 mA	0.06 V

図 13-19. Seven Level Input Pin Structure

図 13-20 shows the structure of the open-drain output pins nFAULT and SDO. The open-drain output requires an external pullup resistor to function correctly.

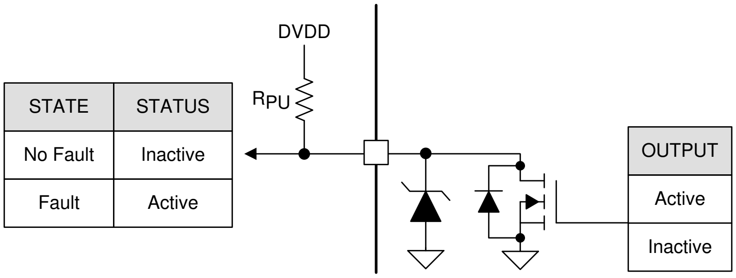


図 13-20. Open-Drain Output Pin Structure

13.3.4 Low-Side Current-Shunt Amplifiers

The DRV8353M integrate three, high-performance low-side current-shunt amplifiers for current measurements using low-side shunt resistors in the external half-bridges. Low-side current measurements are commonly used to implement overcurrent protection, external torque control, or brushless DC commutation with the external controller. All three amplifiers can be used to sense the current in each of the half-bridge legs or one amplifier can be used to sense the sum of the half-bridge legs. The current shunt amplifiers include features such as programmable gain, offset calibration, unidirectional and bidirectional support, and a voltage reference pin (VREF).

13.3.4.1 Bidirectional Current Sense Operation

The SOx pin on the DRV8353M outputs an analog voltage equal to the voltage across the SPx and SNx pins multiplied by the gain setting (G_{CSA}). The gain setting is adjustable between four different levels (5 V/V, 10 V/V, 20 V/V, and 40 V/V). Use 式 3 to calculate the current through the shunt resistor.

$$I = \frac{\frac{V_{VREF}}{2} - V_{SOx}}{G_{CSA} \times R_{SENSE}} \qquad (3)$$

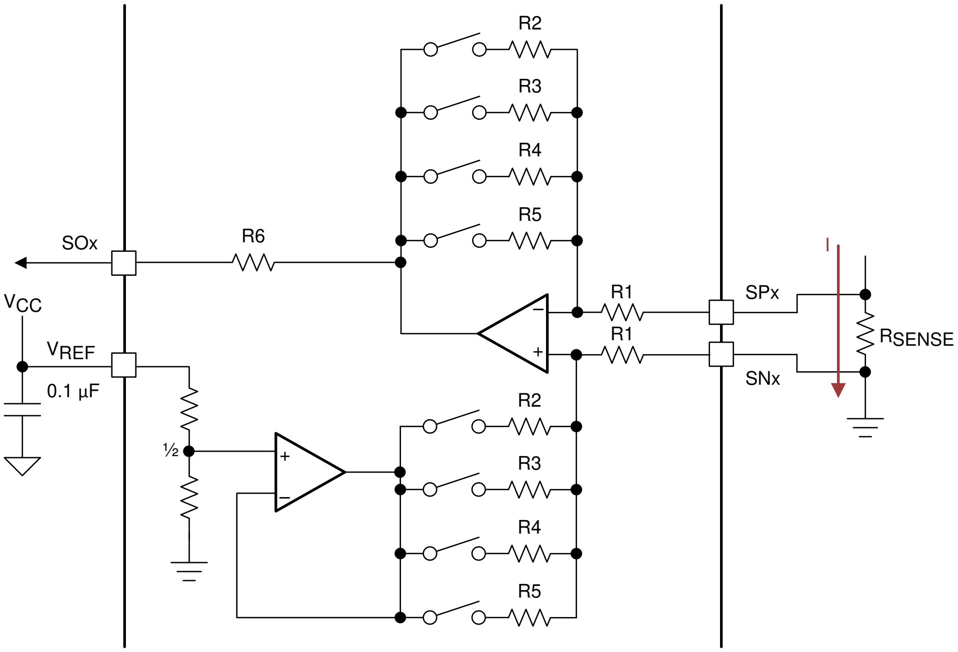


図 13-21. Bidirectional Current-Sense Configuration

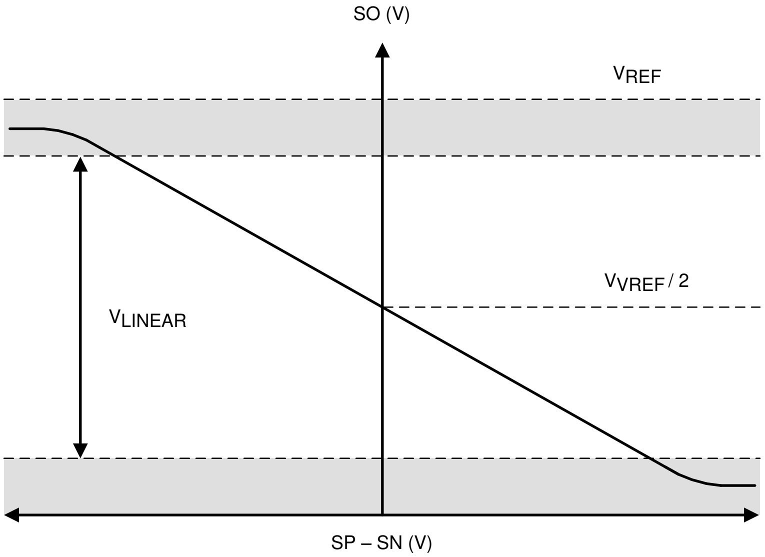


図 13-22. Bidirectional Current-Sense Output

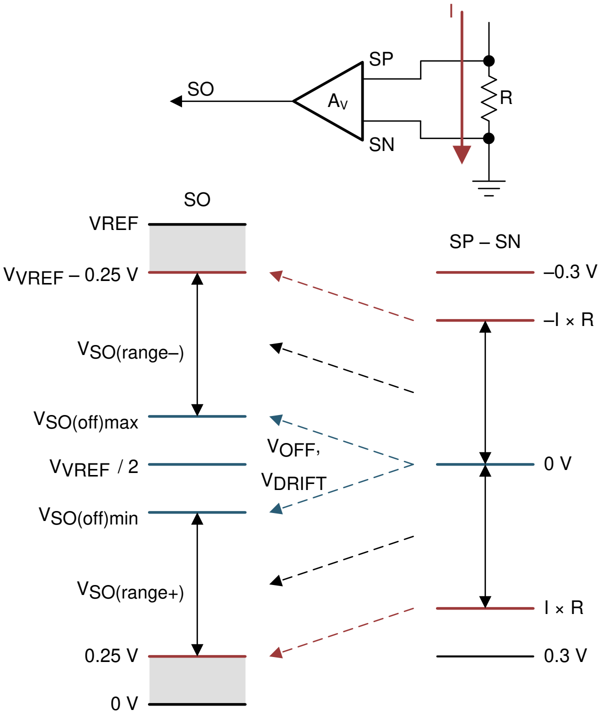


図 13-23. Bidirectional Current Sense Regions

13.3.4.2 Unidirectional Current Sense Operation (SPI only)

On the DRV8353M SPI devices, use the VREF_DIV bit to remove the VREF divider. In this case the shunt amplifier operates unidirectionally and SOx outputs an analog voltage equal to the voltage across the SPx and SNx pins multiplied by the gain setting (G_{CSA}). Use 式 4 to calculate the current through the shunt resistor.

$$I = \frac{V_{VREF} - V_{SOx}}{G_{CSA} \times R_{SENSE}} \tag{4}$$

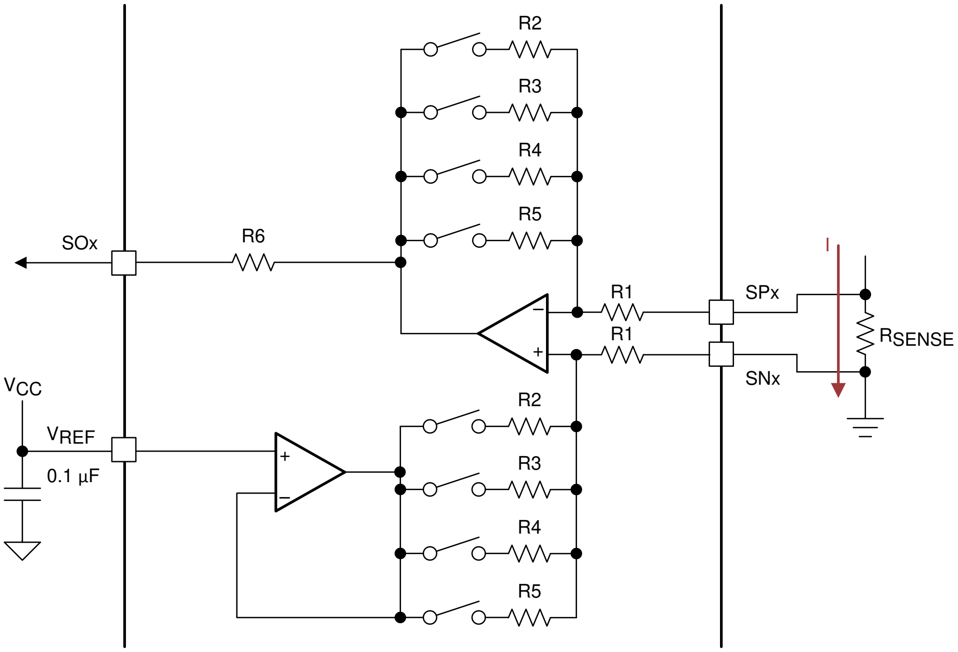


図 13-24. Unidirectional Current-Sense Configuration

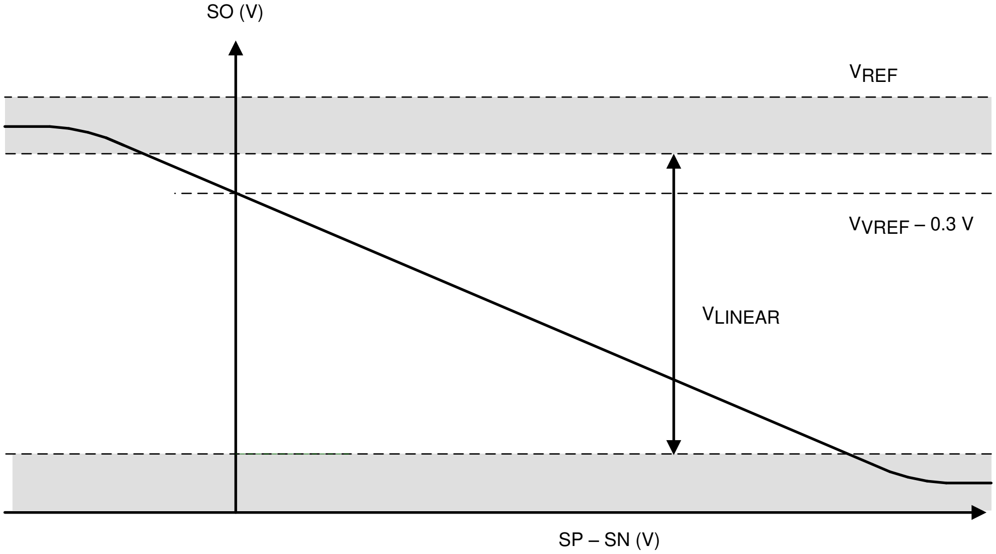


図 13-25. Unidirectional Current-Sense Output

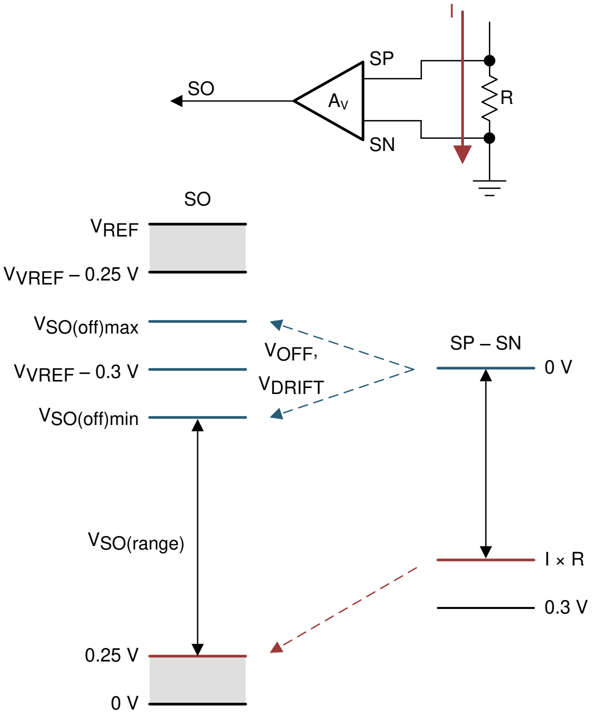


図 13-26. Unidirectional Current-Sense Regions

13.3.4.3 Amplifier Calibration Modes

To minimize DC offset and drift over temperature, a DC calibration mode is provided and enabled through the SPI register (CSA_CAL_X). This option is not available on hardware interface devices. When the calibration setting is enabled the inputs to the amplifier are shorted and the load is disconnected. DC calibration can be done at any time, even when the half-bridges are operating. For the best results, do the DC calibration during the switching OFF period to decrease the potential noise impact to the amplifier. A diagram of the calibration mode is shown below. When a CSA_CAL_X bit is enabled, the corresponding amplifier goes to the calibration mode.

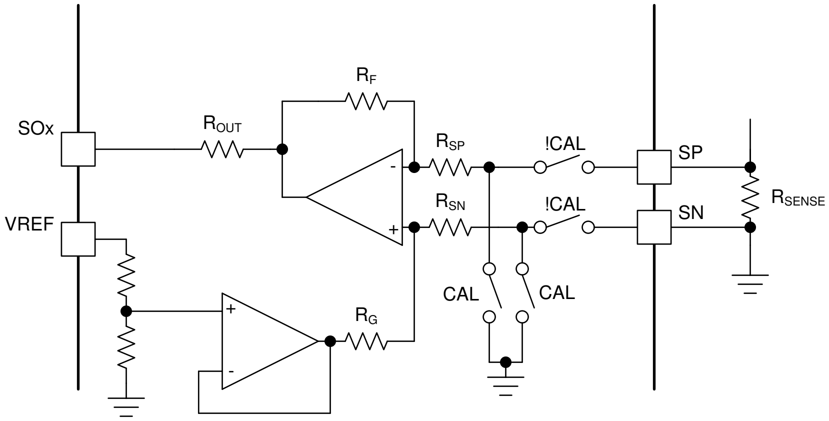


図 13-27. Amplifier Manual Calibration

In addition to the manual calibration method provided on the SPI devices versions, the DRV8353M family of devices provide an auto calibration feature on both the hardware and SPI device versions in order to minimize the amplifier input offset after power up and during run time to account for temperature and device variation.

Auto calibration occurs automatically on device power up for both the hardware and SPI device options. The power up auto calibration starts immediately after the VREF pin crosses the minimum operational VREF voltage.

50 us should be allowed for the power up auto calibration routine to complete after the VREF pin voltage crosses the minimum VREF operational voltage. The auto calibration functions by doing a trim routine of the amplifier to minimize the amplifier input offset. After this the amplifiers are ready for normal operation.

For the SPI device options, auto calibration can also be done again during run time by enabling the AUTO_CAL register setting. Auto calibration can then be commanded with the corresponding CSA_CAL_X register setting to rerun the auto calibration routine. During auto calibration all of the amplifiers will be configured for the max gain setting in order to improve the accuracy of the calibration routine.

13.3.4.4 MOSFET V_{DS} Sense Mode (SPI Only)

The current-sense amplifiers on the DRV8353M SPI devices can be configured to amplify the voltage across the external low-side MOSFET V_{DS}. This allows for the external controller to measure the voltage drop across the MOSFET $R_{DS(on)}$ without the shunt resistor and then calculate the half-bridge current level.

To enable this mode set the CSA_FET bit to 1. The positive input of the amplifier is then internally connected to the SHx pin with an internal clamp to prevent high voltage on the SHx pin from damaging the sense amplifier inputs. During this mode of operation, the SPx pins should stay connected to the source of the low-side MOSFET as it serves as the reference for the low-side gate driver. When the CSA_FET bit is set to 1, the negative reference for the low-side V_{DS} monitor is automatically set to SNx, regardless of the state of the LS_REF bit state. This setting is implemented to prevent disabling of the low-side V_{DS} monitor.

If the system operates in MOSFET V_{DS} sensing mode, route the SHx and SNx pins with Kelvin connections across the drain and source of the external low-side MOSFETs.

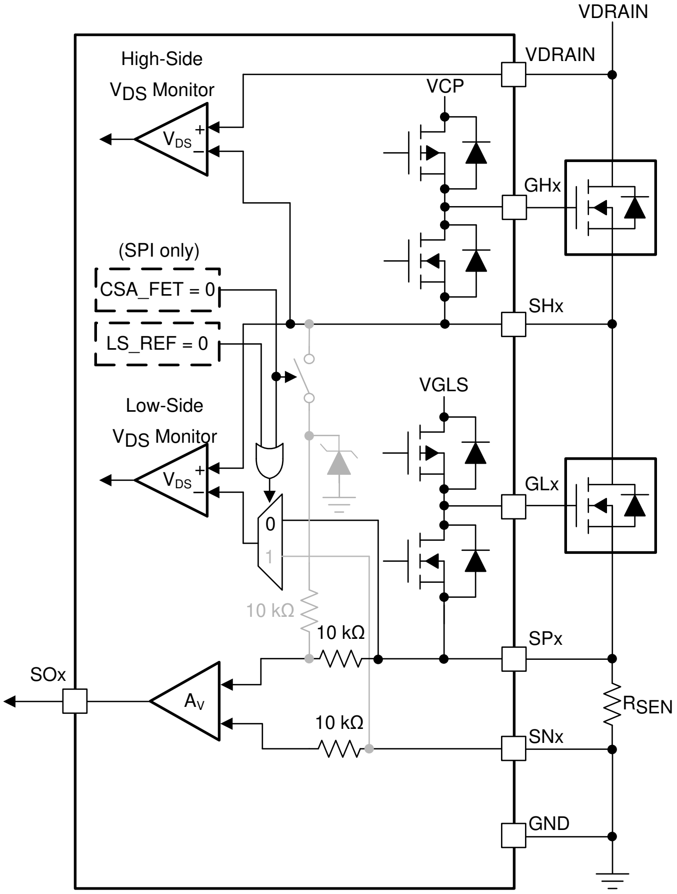


図 13-28. Resistor Sense Configuration

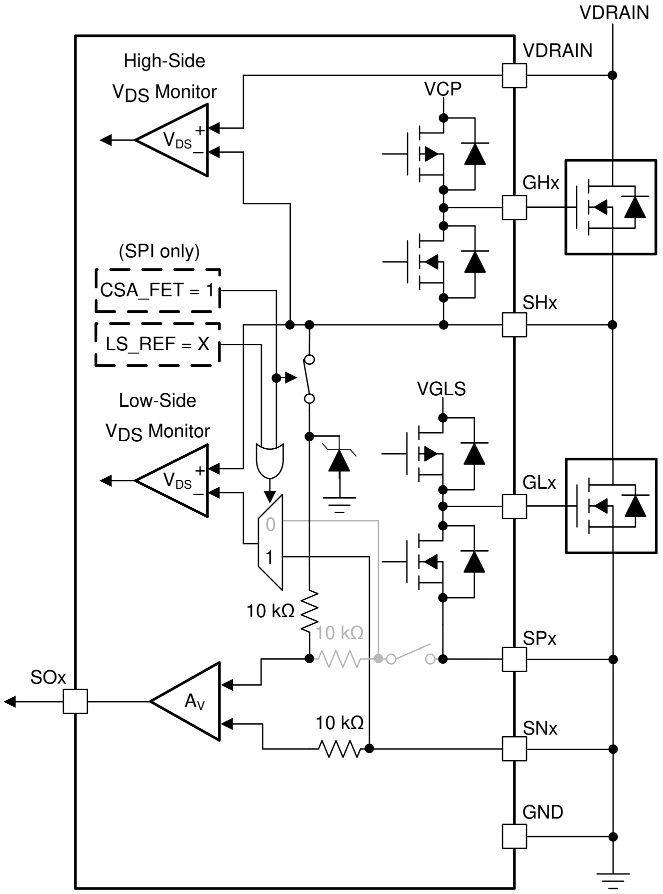


図 13-29. V_{DS} Sense Configuration

When operating in MOSFET V_{DS} sense mode, the amplifier is enabled at the end of the t_{DRIVE} time. At this time, the amplifier input is connected to the SHx pin, and the SOx output is valid. When the low-side MOSFET receives a signal to turn off, the amplifier inputs, SPx and SNx, are shorted together internally.

13.3.5 Gate Driver Protective Circuits

The DRV8353M family of devices are fully protected against VM undervoltage, charge pump and low-side regulator undervoltage, MOSFET V_{DS} overcurrent, gate driver shorts, and overtemperature events.

13.3.5.1 VM Supply and VDRAIN Undervoltage Lockout (UVLO)

If at any time the input supply voltage on the VM pin falls below the V_{VM_UV} threshold or voltage on VDRAIN pin falls below the V_{VDR_UV}, all of the external MOSFETs are disabled, the charge pump is disabled, and the nFAULT pin is driven low. The FAULT and UVLO bits are also latched high in the registers on SPI devices. Normal operation continues (gate driver operation and the nFAULT pin is released) when the undervoltage condition is removed. The UVLO bit stays set until cleared through the CLR_FLT bit or an ENABLE pin reset pulse (t_{RST}).

VM supply or VDRAIN undervoltage may also lead to VCP charge pump or VGLS regulator undervoltage conditions to report. This behavior is expected because the VCP and VGLS supply voltages are dependent on VM and VDRAIN pin voltages.

13.3.5.2 VCP Charge-Pump and VGLS Regulator Undervoltage Lockout (GDUV)

If at any time the voltage on the VCP pin (charge pump) falls below the V_{VCP_UV} threshold or voltage on the VGLS pin falls below the V_{VGLS_UV} threshold, all of the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT and GDUV bits are also latched high in the registers on SPI devices. Normal operation continues (gate-driver operation and the nFAULT pin is released) when the undervoltage condition is removed.

The GDUV bit stays set until cleared through the CLR_FLT bit or an ENABLE pin reset pulse (t_{RST}). Setting the DIS_GDUV bit high on the SPI devices disables this protection feature. On hardware interface devices, the GDUV protection is always enabled.

13.3.5.3 MOSFET V_{DS} Overcurrent Protection (VDS_OCP)

A MOSFET overcurrent event is sensed by monitoring the V_{DS} voltage drop across the external MOSFET $R_{DS(on)}$. If the voltage across an enabled MOSFET exceeds the V_{VDS_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a VDS_OCP event is recognized and action is done according to the OCP_MODE. On hardware interface devices, the V_{VDS_OCP} threshold is set with the VDS pin, the t_{OCP_DEG} is fixed at 4 µs, and the OCP_MODE is configured for 8-ms automatic retry but can be disabled by tying the VDS pin to DVDD. On SPI devices, the V_{VDS_OCP} threshold is set through the VDS_LVL SPI register, the t_{OCP_DEG} is set through the OCP_DEG SPI register, and the OCP_MODE bit can operate in four different modes: V_{DS} latched shutdown, V_{DS} automatic retry, V_{DS} report only, and V_{DS} disabled.

The MOSFET V_{DS} overcurrent protection operates in cycle-by-cycle (CBC) mode by default. This can be disabled on SPI device variants through the SPI registers. When in cycle-by-cycle (CBC) mode a new rising edge on the PWM inputs will clear an existing overcurrent fault.

Additionally, on SPI devices the OCP_ACT register setting can be set to change the VDS_OCP overcurrent response between linked and individual shutdown modes. When OCP_ACT is 0, a VDS_OCP fault will only effect the half-bridge in which it occurred. When OCP_ACT is 1, all three half-bridges will respond to a VDS_OCP fault on any of the other half-bridges. OCP_ACT defaults to 0, individual shutdown mode.

13.3.5.3.1 V_{DS} Latched Shutdown (OCP_MODE = 00b)

After a VDS_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, VDS_OCP, and corresponding MOSFET OCP bits are latched high in the SPI registers. Normal operation continues (gate driver operation and the nFAULT pin is released) when the VDS_OCP condition is removed and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

13.3.5.3.2 V_{DS} Automatic Retry (OCP_MODE = 01b)

After a VDS_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, VDS_OCP, and corresponding MOSFET OCP bits are latched high in the SPI registers. Normal operation continues automatically (gate driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. The FAULT, VDS_OCP, and MOSFET OCP bits stay latched until the t_{RETRY} period expires.

13.3.5.3.3 V_{DS} Report Only (OCP_MODE = 10b)

No protective action occurs after a VDS_OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT, VDS_OCP, and corresponding MOSFET OCP bits high in the SPI registers. The gate drivers continue to operate as normal. The external controller manages the overcurrent condition by acting appropriately. The reporting clears (nFAULT pin is released) when the VDS_OCP condition is removed and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

13.3.5.3.4 V_{DS} Disabled (OCP_MODE = 11b)

No action occurs after a VDS_OCP event in this mode.

13.3.5.4 V_{SENSE} Overcurrent Protection (SEN_OCP)

Half-bridge overcurrent is also monitored by sensing the voltage drop across the external current-sense resistor with the SP pin. If at any time, the voltage on the SP input of the current-sense amplifier exceeds the V_{SEN_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a SEN_OCP event is recognized and action is done according to the OCP_MODE. On hardware interface devices, the V_{SENSE} threshold is fixed at 1 V, t_{OCP_DEG} is fixed at 4 µs, and the OCP_MODE for V_{SENSE} is fixed for 8-ms automatic retry. On SPI devices, the V_{SENSE} threshold is set through the SEN_LVL SPI register, the t_{OCP_DEG} is set through the OCP_DEG SPI register, and the OCP_MODE bit can operate in four different modes: V_{SENSE} latched shutdown, V_{SENSE} automatic retry, V_{SENSE} report only, and V_{SENSE} disabled.

The V_{SENSE} overcurrent protection operates in cycle-by-cycle (CBC) mode by default. This can be disabled on SPI device variants through the SPI registers. When in cycle-by-cycle (CBC) mode a new rising edge on the PWM inputs will clear an existing overcurrent fault.

Additionally, on SPI devices the OCP_ACT register setting can be set to change the SEN_OCP overcurrent response between linked and individual shutdown modes. When OCP_ACT is 0, a SEN_OCP fault will only effect the half-bridge in which it occurred. When OCP_ACT is 1, all three half-bridges will respond to a SEN_OCP fault on any of the other half-bridges. OCP_ACT defaults to 0, individual shutdown mode.

13.3.5.4.1 V_{SENSE} Latched Shutdown (OCP_MODE = 00b)

After a SEN_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT and SEN_OCP bits are latched high in the SPI registers. Normal operation continues (gate driver operation and the nFAULT pin is released) when the SEN_OCP condition is removed and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

13.3.5.4.2 V_{SENSE} Automatic Retry (OCP_MODE = 01b)

After a SEN_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, SEN_OCP, and corresponding sense OCP bits are latched high in the SPI registers. Normal operation continues automatically (gate driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. The FAULT , SEN_OCP, and sense OCP bits stay latched until the t_{RETRY} period expires.

13.3.5.4.3 V_{SENSE} Report Only (OCP_MODE = 10b)

No protective action occurs after a SEN_OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT and SEN_OCP bits high in the SPI registers. The gate drivers continue to operate. The external controller manages the overcurrent condition by acting appropriately. The reporting clears (nFAULT released) when the SEN_OCP condition is removed and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

13.3.5.4.4 V_{SENSE} Disabled (OCP_MODE = 11b or DIS_SEN = 1b)

No action occurs after a SEN_OCP event in this mode. The SEN_OCP bit can be disabled independently of the VDS_OCP bit by using the DIS_SEN SPI register.

13.3.5.5 Gate Driver Fault (GDF)

The GHx and GLx pins are monitored such that if the voltage on the external MOSFET gate does not increase or decrease after the t_{DRIVE} time, a gate driver fault is detected. This fault may be encountered if the GHx or GLx pins are shorted to the PGND, SHx, or VM pins. Additionally, a gate driver fault may be encountered if the selected I_{DRIVE} setting is not sufficient to turn on the external MOSFET within the t_{DRIVE} period. After a gate drive fault is detected, all external MOSFETs are disabled and the nFAULT pin driven low. In addition, the FAULT, GDF, and corresponding VGS bits are latched high in the SPI registers. Normal operation continues (gate driver operation and the nFAULT pin is released) when the gate driver fault condition is removed and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}). On SPI devices, setting the DIS_GDF_UVLO bit high disables this protection feature.

Gate driver faults can indicate that the selected I_{DRIVE} or t_{DRIVE} settings are too low to slew the external MOSFET in the desired time. Increasing either the I_{DRIVE} or t_{DRIVE} setting can resolve gate driver faults in these cases. Alternatively, if a gate-to-source short occurs on the external MOSFET, a gate driver fault is reported because of the MOSFET gate not turning on.

13.3.5.6 Overcurrent Soft Shutdown (OCP Soft)

In the case of a MOSFET V_{DS} or V_{SENSE} overcurrent fault the driver uses a special shutdown sequence to protect the driver and MOSFETs from large voltage switching transients. These large voltage transients can be created when rapidly switching off the external MOSFETs when a large drain to source current is present, such as during an overcurrent event.

To mitigate this issue, the DRV8353M family of devices reduce the I_{DRIVEN} pull down current setting for both the high-side and low-side gate drivers during the MOSFET turn off in response to the fault event. If the programmed

I_{DRIVEN} value is less than 1100 mA, the IDRIVEN value is set to the minimum I_{DRIVEN} setting. If the programmed I_{DRIVEN} value is greater than or equal to 1100mA, the I_{DRIVEN} value is reduced by seven code settings.

13.3.5.7 Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OTW bit is set in the registers of SPI devices. The device does no additional action and continues to function. When the die temperature falls below the hysteresis point of the thermal warning, the OTW bit clears automatically. The OTW bit can also be configured to report on the nFAULT pin and FAULT bit by setting the OTW_REP bit to 1 through the SPI registers.

13.3.5.8 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}), all the external MOSFETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the FAULT and TSD bits are latched high. Normal operation continues (gate driver operation and the nFAULT pin is released) when the overtemperature condition is removed. The TSD bit stays latched high indicating that a thermal event occurred until a clear fault command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}). This protection feature cannot be disabled.

13.3.5.9 Fault Response Table

表 13-6. Fault Action and Response

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	RECOVERY
VM Undervoltage (VM_UV)	$V_{VM} < V_{VM\_UV}$	—	nFAULT	Hi-Z	Automatic: $V_{VM} > V_{VM\_UV}$
VDRAIN Undervoltage (VDR_UV)	$V_{VDRAIN} < V_{VDR\_UV}$	—	nFAULT	Hi-Z	Automatic: $V_{VM} > V_{VDR\_UV}$
Charge Pump Undervoltage (VCP_UV)	$V_{VCP} < V_{VCP\_UV}$	DIS_GDUV = 0b	nFAULT	Hi-Z	Automatic: $V_{VCP} > V_{VCP\_UV}$
		DIS_GDUV = 1b	None	Active	
VGLS Regulator Undervoltage (VGLS_UV)	$V_{VGLS} < V_{VGLS\_UV}$	DIS_GDUV = 0b	nFAULT	Hi-Z	Automatic: $V_{VGLS} > V_{VGLS\_UV}$
		DIS_GDUV = 1b	None	Active	
V_{DS} Overcurrent (VDS_OCP)	$V_{DS} > V_{VDS\_OCP}$	OCP_MODE = 00b	nFAULT	Hi-Z	Latched: CLR_FLT, ENABLE Pulse
		OCP_MODE = 01b	nFAULT	Hi-Z	Retry: t_{RETRY}
		OCP_MODE = 10b	nFAULT	Active	No action
		OCP_MODE = 11b	None	Active	No action
V_{SENSE} Overcurrent (SEN_OCP)	$V_{SP} > V_{SEN\_OCP}$	OCP_MODE = 00b	nFAULT	Hi-Z	Latched: CLR_FLT, ENABLE Pulse
		OCP_MODE = 01b	nFAULT	Hi-Z	Retry: t_{RETRY}
		OCP_MODE = 10b	nFAULT	Active	No action
		OCP_MODE = 11b or DIS_SEN = 1b	None	Active	No action
Gate Driver Fault (GDF)	V_{GS} Stuck > t_{DRIVE}	DIS_GDF = 0b	nFAULT	Hi-Z	Latched: CLR_FLT, ENABLE Pulse
		DIS_GDF = 1b	None	Active	No action
Thermal Warning (OTW)	$T_J > T_{OTW}$	OTW_REP = 1b	nFAULT	Active	Automatic: $T_J < T_{OTW} - T_{HYS}$
		OTW_REP = 0b	None	Active	No action
Thermal Shutdown (OTSD)	$T_J > T_{OTSD}$	—	nFAULT	Hi-Z	Automatic: $T_J < T_{OTSD} - T_{HYS}$

13.4 Device Functional Modes

13.4.1 Gate Driver Functional Modes

13.4.1.1 Sleep Mode

The ENABLE pin manages the state of the DRV8353M family of devices. When the ENABLE pin is low, the device goes to a low-power sleep mode. In sleep mode, all gate drivers are disabled, all external MOSFETs are disabled, the VCP charge pump and VGLS regulator are disabled, the DVDD regulator is disabled, the sense amplifiers are disabled, and the SPI bus is disabled. In sleep mode all the device registers will reset to their default values. The t_{SLEEP} time must elapse after a falling edge on the ENABLE pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the ENABLE pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

In sleep mode and when $V_{VM} < V_{UVLO}$, all external MOSFETs are disabled. The high-side gate pins, GHx, are pulled to the SHx pin by an internal resistor and the low-side gate pins, GLx, are pulled to the PGND pin by an internal resistor.

13.4.1.2 Operating Mode

When the ENABLE pin is high and $V_{VM} > V_{UVLO}$, the device goes to operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the charge pump, low-side gate regulator, DVDD regulator, and SPI bus are active

13.4.1.3 Fault Reset (CLR_FLT or ENABLE Reset Pulse)

In the case of device latched faults, the DRV8353M family of devices goes to a partial shutdown state to help protect the external power MOSFETs and system.

When the fault condition has been removed the device can reenter the operating state by either setting the CLR_FLT SPI bit on SPI devices or issuing a result pulse to the ENABLE pin on either interface variant. The ENABLE reset pulse (t_{RST}) consists of a high-to-low-to-high transition on the ENABLE pin. The low period of the sequence should fall with the t_{RST} time window or else the device will start the complete shutdown sequence. The reset pulse has no effect on any of the regulators, device settings, or other functional blocks

13.5 Programming

This section applies only to the DRV8353M SPI devices.

13.5.1 SPI Communication

13.5.1.1 SPI

On DRV8353M SPI devices, an SPI bus is used to set device configurations, operating parameters, and read out diagnostic information. The SPI operates in slave mode and connects to a master controller. The SPI input data (SDI) word consists of a 16 bit word, with a 5 bit command and 11 bits of data. The SPI output data (SDO) word consists of 11-bit register data. The first 5 bits are don’t care bits.

A valid frame must meet the following conditions:

- The SCLK pin should be low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin should be pulled high for at least 400 ns between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is set Hi-Z.
- Data is captured on the falling edge of SCLK and data is propagated on the rising edge of SCLK.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is not 16 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 5 bit command data.
- The SDO pin is an open-drain output and requires an external pullup resistor.

13.5.1.1.1 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit B15)
- 4 address bits, A (bits B14 through B11)
- 11 data bits, D (bits B11 through B0)

Set the read/write bit (W0, B15) to 0b for a write command. Set the read/write bit (W0, B15) to 1b for a read command.

The SDO output data word is 16 bits long and the first 5 bits are don't care bits. The response word is the data currently in the register being accessed.

表 13-7. SDI Input Data Word Format

R/W	ADDRESS				DATA										
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
W0	A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

表 13-8. SDO Output Data Word Format

DON'T CARE BITS					DATA										
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	X	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

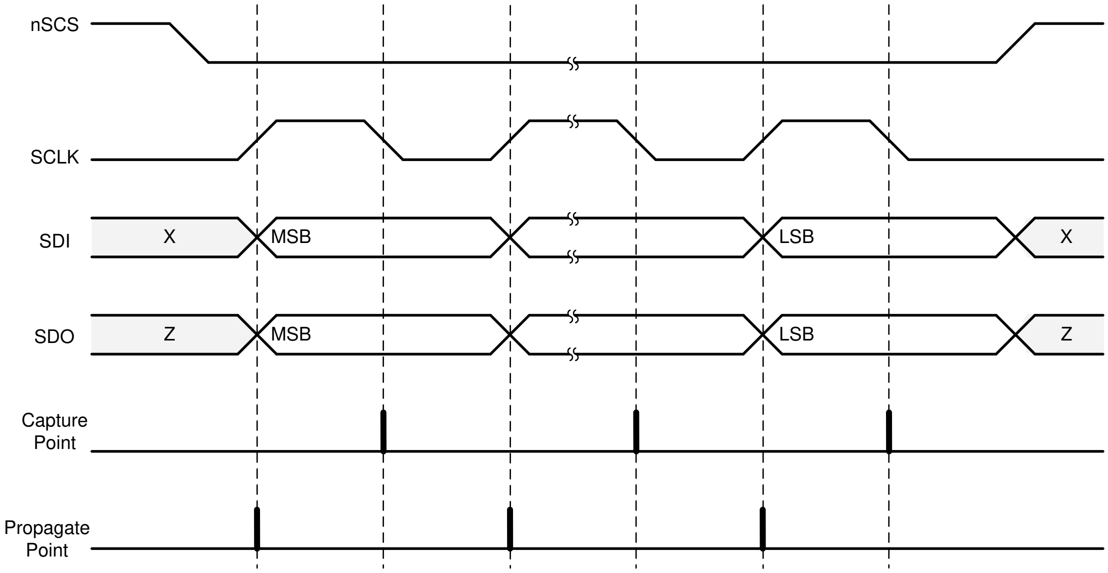


図 13-30. SPI Slave Timing Diagram

13.6 Register Maps

This section applies only to the DRV8353M SPI devices.

注

Do not modify reserved registers or addresses not listed in the register maps (). Writing to these registers may have unintended effects. For all reserved bits, the default value is 0. To help prevent erroneous SPI writes from the master controller, set the LOCK bits to lock the SPI registers.

表 13-9. Register Map

Name	10	9	8	7	6	5	4	3	2	1	0	Type	Address
Fault Status 1	FAULT	VDS_OCP	GDF	UVLO	OTSD	VDS_HA	VDS_LA	VDS_HB	VDS_LB	VDS_HC	VDS_LC	R	0h
VGS Status 2	SA_OC	SB_OC	SC_OC	OTW	GDUV	VGS_HA	VGS_LA	VGS_HB	VGS_LB	VGS_HC	VGS_LC	R	1h
Driver Control	OCP_ACT	DIS_GDUV	DIS_GDF	OTW_REP	PWM_MODE		1PWM_COM	1PWM_DIR	COAST	BRAKE	CLR_FLT	RW	2h
Gate Drive HS	LOCK			IDRIVEP_HS				IDRIVEN_HS				RW	3h
Gate Drive LS	CBC	TDRIVE		IDRIVEP_LS				IDRIVEN_LS				RW	4h
OCP Control	TRETRY	DEAD_TIME		OCP_MODE		OCP_DEG		VDS_LVL				RW	5h
CSA Control	CSA_FET	VREF_DIV	LS_REF	CSA_GAIN		DIS_SEN	CSA_CAL_A	CSA_CAL_B	CSA_CAL_C	SEN_LVL		RW	6h
Reserved	Reserved										CAL_MODE	RW	7h

13.6.1 Status Registers

The status registers are used to reporting warning and fault conditions. The status registers are read-only registers

Complex bit access types are encoded to fit into small table cells. 表 13-10 shows the codes that are used for access types in this section.

表 13-10. Status Registers Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-*n*		Value after reset or the default value

13.6.1.1 Fault Status Register 1 (address = 0x00h)

The fault status register 1 is shown in 図 13-31 and described in 表 13-11.

Register access type: Read only

図 13-31. Fault Status Register 1

10	9	8	7	6	5	4	3	2	1	0
FAULT	VDS_OCP	GDF	UVLO	OTSD	VDS_HA	VDS_LA	VDS_HB	VDS_LB	VDS_HC	VDS_LC
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 13-11. Fault Status Register 1 Field Descriptions

Bit	Field	Type	Default	Description
10	FAULT	R	0b	Logic OR of FAULT status registers. Mirrors nFAULT pin.
9	VDS_OCP	R	0b	Indicates VDS monitor overcurrent fault condition
8	GDF	R	0b	Indicates gate drive fault condition
7	UVLO	R	0b	Indicates undervoltage lockout fault condition
6	OTSD	R	0b	Indicates overtemperature shutdown
5	VDS_HA	R	0b	Indicates VDS overcurrent fault on the A high-side MOSFET
4	VDS_LA	R	0b	Indicates VDS overcurrent fault on the A low-side MOSFET
3	VDS_HB	R	0b	Indicates VDS overcurrent fault on the B high-side MOSFET
2	VDS_LB	R	0b	Indicates VDS overcurrent fault on the B low-side MOSFET
1	VDS_HC	R	0b	Indicates VDS overcurrent fault on the C high-side MOSFET
0	VDS_LC	R	0b	Indicates VDS overcurrent fault on the C low-side MOSFET

13.6.1.2 Fault Status Register 2 (address = 0x01h)

The fault status register 2 is shown in 図 13-32 and described in 表 13-12.

Register access type: Read only

図 13-32. Fault Status Register 2

10	9	8	7	6	5	4	3	2	1	0
SA_OC	SB_OC	SC_OC	OTW	GDUV	VGS_HA	VGS_LA	VGS_HB	VGS_LB	VGS_HC	VGS_LC
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 13-12. Fault Status Register 2 Field Descriptions

Bit	Field	Type	Default	Description
10	SA_OC	R	0b	Indicates overcurrent on phase A sense amplifier
9	SB_OC	R	0b	Indicates overcurrent on phase B sense amplifier
8	SC_OC	R	0b	Indicates overcurrent on phase C sense amplifier
7	OTW	R	0b	Indicates overtemperature warning
6	GDUV	R	0b	Indicates VCP charge pump and/or VGLS undervoltage fault condition
5	VGS_HA	R	0b	Indicates gate drive fault on the A high-side MOSFET
4	VGS_LA	R	0b	Indicates gate drive fault on the A low-side MOSFET
3	VGS_HB	R	0b	Indicates gate drive fault on the B high-side MOSFET
2	VGS_LB	R	0b	Indicates gate drive fault on the B low-side MOSFET
1	VGS_HC	R	0b	Indicates gate drive fault on the C high-side MOSFET
0	VGS_LC	R	0b	Indicates gate drive fault on the C low-side MOSFET

13.6.2 Control Registers

The control registers are used to configure the device. The control registers are read and write capable

Complex bit access types are encoded to fit into small table cells. 表 13-13 shows the codes that are used for access types in this section.

表 13-13. Control Registers Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

13.6.2.1 Driver Control Register (address = 0x02h)

The driver control register is shown in 図 13-33 and described in 表 13-14.

Register access type: Read/Write

図 13-33. Driver Control Register

10	9	8	7	6	5	4	3	2	1	0
OCP _ACT	DIS _GDUV	DIS _GDF	OTW _REP	PWM_MODE		1PWM _COM	1PWM _DIR	COAST	BRAKE	CLR _FLT
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 13-14. Driver Control Field Descriptions

Bit	Field	Type	Default	Description
10	OCP_ACT	R/W	0b	**0b = Associated half-bridge is shutdown in response to VDS_OCP and SEN_OCP** 1b = All three half-bridges are shutdown in response to VDS_OCP and SEN_OCP
9	DIS_GDUV	R/W	0b	**0b =VCP and VGLS undervoltage lockout fault is enabled** 1b = VCP and VGLS undervoltage lockout fault is disabled
8	DIS_GDF	R/W	0b	**0b = Gate drive fault is enabled** 1b = Gate drive fault is disabled
7	OTW_REP	R/W	0b	**0b = OTW is not reported on nFAULT or the FAULT bit** 1b = OTW is reported on nFAULT and the FAULT bit
6-5	PWM_MODE	R/W	00b	**00b = 6x PWM Mode** 01b = 3x PWM mode 10b = 1x PWM mode 11b = Independent PWM mode
4	1PWM_COM	R/W	0b	**0b = 1x PWM mode uses synchronous rectification** 1b = 1x PWM mode uses asynchronous rectification
3	1PWM_DIR	R/W	0b	In 1x PWM mode this bit is ORed with the INHC (DIR) input
2	COAST	R/W	0b	Write a 1 to this bit to put all MOSFETs in the Hi-Z state
1	BRAKE	R/W	0b	Write a 1 to this bit to turn on all three low-side MOSFETs This bit is ORed with the INLC (BRAKE) input in 1x PWM mode.
0	CLR_FLT	R/W	0b	Write a 1 to this bit to clear latched fault bits. This bit automatically resets after being writen.

13.6.2.2 Gate Drive HS Register (address = 0x03h)

The gate drive HS register is shown in 図 13-34 and described in 表 13-15.

Register access type: Read/Write

図 13-34. Gate Drive HS Register

10	9	8	7	6	5	4	3	2	1	0
LOCK			IDRIVEP_HS				IDRIVEn_HS			
R/W-011b			R/W-1111b				R/W-1111b			

表 13-15. Gate Drive HS Field Descriptions

Bit	Field	Type	Default	Description
10-8	LOCK	R/W	011b	Write 110b to lock the settings by ignoring further register writes except to these bits and address 0x02h bits 0-2. Writing any sequence other than 110b has no effect when unlocked. Write 011b to this register to unlock all registers. Writing any sequence other than 011b has no effect when locked.
7-4	IDRIVEP_HS	R/W	1111b	0000b = 50 mA 0001b = 50 mA 0010b = 100 mA 0011b = 150 mA 0100b = 300 mA 0101b = 350 mA 0110b = 400 mA 0111b = 450 mA 1000b = 550 mA 1001b = 600 mA 1010b = 650 mA 1011b = 700 mA 1100b = 850 mA 1101b = 900 mA 1110b = 950 mA **1111b = 1000 mA**
3-0	IDRIVEN_HS	R/W	1111b	0000b = 100 mA 0001b = 100 mA 0010b = 200 mA 0011b = 300 mA 0100b = 600 mA 0101b = 700 mA 0110b = 800 mA 0111b = 900 mA 1000b = 1100 mA 1001b = 1200 mA 1010b = 1300 mA 1011b = 1400 mA 1100b = 1700 mA 1101b = 1800 mA 1110b = 1900 mA **1111b = 2000 mA**

13.6.2.3 Gate Drive LS Register (address = 0x04h)

The gate drive LS register is shown in 図 13-35 and described in 表 13-16.

Register access type: Read/Write

図 13-35. Gate Drive LS Register

10	9	8	7	6	5	4	3	2	1	0
CBC	TDRIVE		IDRIVEP_LS				IDRIVEN_LS			
R/W-1b	R/W-11b		R/W-1111b				R/W-1111b			

表 13-16. Gate Drive LS Register Field Descriptions

Bit	Field	Type	Default	Description
10	CBC	R/W	1b	Active only when OCP_MODE = 01b 0b = For VDS_OCP and SEN_OCP, the fault is cleared after t_{RETRY} **1b = For VDS_OCP and SEN_OCP, the fault is cleared when a new PWM input is given or after t_{RETRY}**
9-8	TDRIVE	R/W	11b	00b = 500-ns peak gate-current drive time 01b = 1000-ns peak gate-current drive time 10b = 2000-ns peak gate-current drive time **11b = 4000-ns peak gate-current drive time**
7-4	IDRIVEP_LS	R/W	1111b	0000b = 50 mA 0001b = 50 mA 0010b = 100 mA 0011b = 150 mA 0100b = 300 mA 0101b = 350 mA 0110b = 400 mA 0111b = 450 mA 1000b = 550 mA 1001b = 600 mA 1010b = 650 mA 1011b = 700 mA 1100b = 850 mA 1101b = 900 mA 1110b = 950 mA **1111b = 1000 mA**
3-0	IDRIVEN_LS	R/W	1111b	0000b = 100 mA 0001b = 100 mA 0010b = 200 mA 0011b = 300 mA 0100b = 600 mA 0101b = 700 mA 0110b = 800 mA 0111b = 900 mA 1000b = 1100 mA 1001b = 1200 mA 1010b = 1300 mA 1011b = 1400 mA 1100b = 1700 mA 1101b = 1800 mA 1110b = 1900 mA **1111b = 2000 mA**

13.6.2.4 OCP Control Register (address = 0x05h)

The OCP control register is shown in 図 13-36 and described in 表 13-17.

Register access type: Read/Write

図 13-36. OCP Control Register

10	9	8	7	6	5	4	3	2	1	0
TRETRY	DEAD_TIME		OCP_MODE		OCP_DEG		VDS_LVL			
R/W-0b	R/W-01b		R/W-01b		R/W-01b		R/W-1101b			

表 13-17. OCP Control Field Descriptions

Bit	Field	Type	Default	Description
10	TRETRY	R/W	0b	**0b = VDS_OCP and SEN_OCP retry time is 8 ms** 1b = VDS_OCP and SEN_OCP retry time is 50 µs
9-8	DEAD_TIME	R/W	01b	00b = 50-ns dead time **01b = 100-ns dead time** 10b = 200-ns dead time 11b = 400-ns dead time
7-6	OCP_MODE	R/W	01b	00b = Overcurrent causes a latched fault **01b = Overcurrent causes an automatic retrying fault** 10b = Overcurrent is report only but no action is taken 11b = Overcurrent is not reported and no action is taken
5-4	OCP_DEG	R/W	10b	00b = Overcurrent deglitch of 1 µs 01b = Overcurrent deglitch of 2 µs **10b = Overcurrent deglitch of 4 µs** 11b = Overcurrent deglitch of 8 µs
3-0	VDS_LVL	R/W	1001b	0000b = 0.06 V 0001b = 0.07 V 0010b = 0.08 V 0011b = 0.09 V 0100b = 0.1 V 0101b = 0.2 V 0110b = 0.3 V 0111b = 0.4 V 1000b = 0.5 V 1001b = 0.6 V 1010b = 0.7 V 1011b = 0.8 V 1100b = 0.9 V **1101b = 1 V** 1110b = 1.5 V 1111b = 2 V

13.6.2.5 CSA Control Register (address = 0x06h)

The CSA control register is shown in 図 13-37 and described in 表 13-18.

Register access type: Read/Write.

図 13-37. CSA Control Register

10	9	8	7	6	5	4	3	2	1	0
CSA _FET	VREF _DIV	LS _REF	CSA _GAIN		DIS _SEN	CSA _CAL_A	CSA _CAL_B	CSA _CAL_C	SEN _LVL	
R/W-0b	R/W-1b	R/W-0b	R/W-10b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-11b	

表 13-18. CSA Control Field Descriptions

Bit	Field	Type	Default	Description
10	CSA_FET	R/W	0b	**0b = Sense amplifier positive input is SPx** 1b = Sense amplifier positive input is SHx (also automatically sets the LS_REF bit to 1)
9	VREF_DIV	R/W	1b	0b = Sense amplifier reference voltage is VREF (unidirectional mode) **1b = Sense amplifier reference voltage is VREF divided by 2**
8	LS_REF	R/W	0b	**0b = VDS_OCP for the low-side MOSFET is measured across SHx to SPx** 1b = VDS_OCP for the low-side MOSFET is measured across SHx to SNx
7-6	CSA_GAIN	R/W	10b	00b = 5-V/V shunt amplifier gain 01b = 10-V/V shunt amplifier gain **10b = 20-V/V shunt amplifier gain** 11b = 40-V/V shunt amplifier gain
5	DIS_SEN	R/W	0b	**0b = Sense overcurrent fault is enabled** 1b = Sense overcurrent fault is disabled
4	CSA_CAL_A	R/W	0b	**0b = Normal sense amplifier A operation** 1b = Short inputs to sense amplifier A for offset calibration
3	CSA_CAL_B	R/W	0b	**0b = Normal sense amplifier B operation** 1b = Short inputs to sense amplifier B for offset calibration
2	CSA_CAL_C	R/W	0b	**0b = Normal sense amplifier C operation** 1b = Short inputs to sense amplifier C for offset calibration
1-0	SEN_LVL	R/W	11b	00b = Sense OCP 0.25 V 01b = Sense OCP 0.5 V 10b = Sense OCP 0.75 V **11b = Sense OCP 1 V**

13.6.2.6 Driver Configuration Register (address = 0x07h)

The driver configuration register is shown in 図 13-38 and described in 表 13-19.

Register access type: Read/Write

図 13-38. Driver Configuration Register

10	9	8	7	6	5	4	3	2	1	0
Reserved										CAL _MODE
R/W-000 0000 000b										R/W-0b

表 13-19. Driver Configuration Field Descriptions

Bit	Field	Type	Default	Description
10-1	Reserved	R/W	000 0000 000b	Reserved
0	CAL_MODE	R/W	0b	**0b = Amplifier calibration operates in manual mode** 1b = Amplifier calibration uses internal auto calibration routine

14 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

14.1 Application Information

The DRV8353M family of devices are primarily used in three-phase brushless DC motor control applications. The design procedures in the *セクション 14.2* section highlight how to use and configure the DRV8353M family of devices.

14.2 Typical Application

14.2.1 Primary Application

The DRV8353M is shown being used for a single supply, three-phase BLDC motor drive with individual half-bridge current sense in this application example.

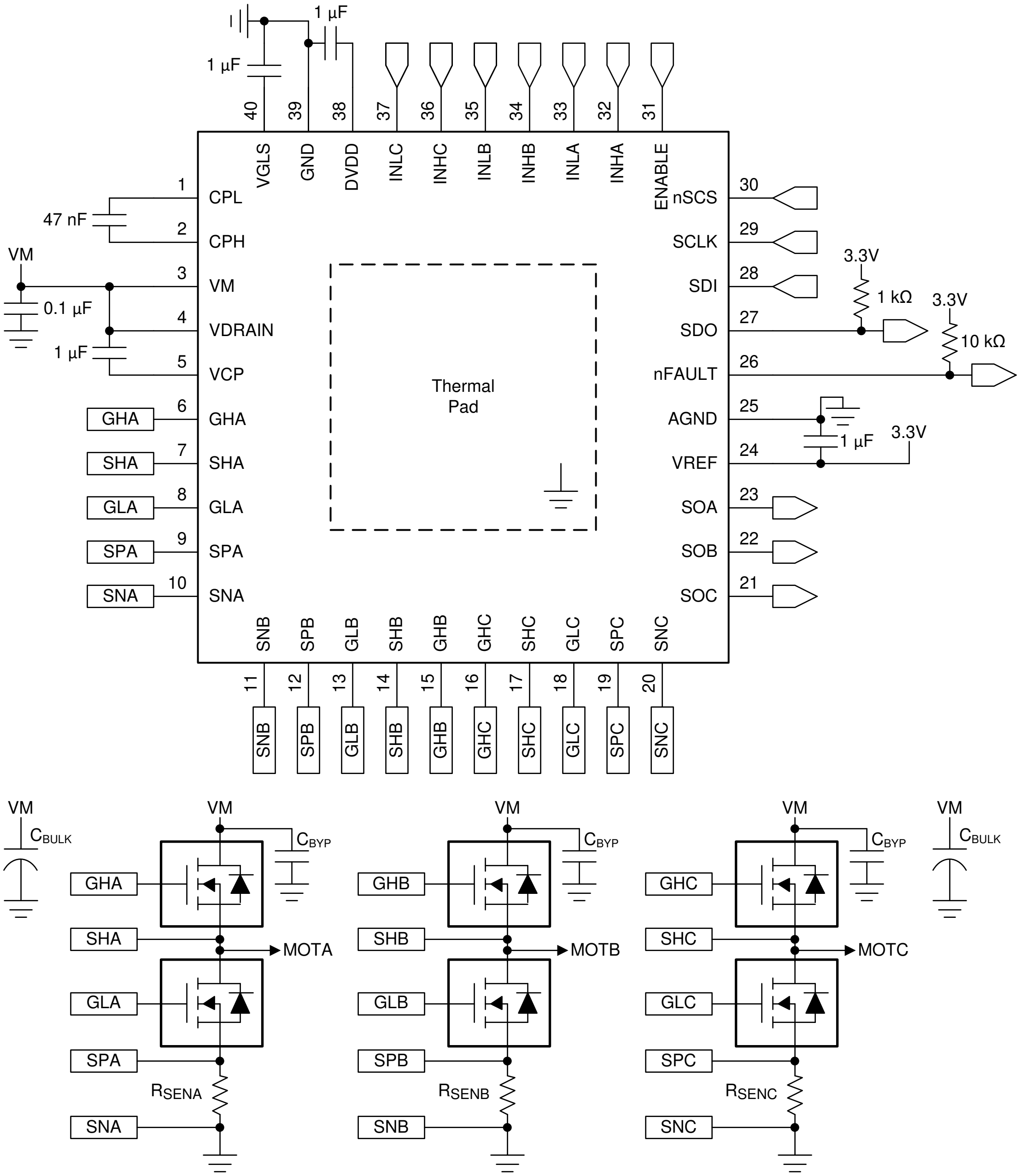


図 14-1. Primary Application Schematic

14.2.1.1 Design Requirements

表 14-1 lists the example input parameters for the system design.

表 14-1. Design Parameters

EXAMPLE DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Power supply voltage	V_{VM}, V_{VDRAIN}, V_{VIN}	48 V
MOSFET part number	MOSFET	CSD19535KCS
MOSFET total gate charge	Q_g	78 nC (typical) at V_{VGS} = 10 V
MOSFET gate to drain charge	Q_{gd}	13 nC (typical)
Target output rise time	t_r	100 to 300 ns
Target output fall time	t_f	50 to 150 ns
PWM frequency	f_{PWM}	45 kHz
Buck regulator output voltage	V_{VCC}	3.3 V
Buck regulator output current	I_{VCC}	100 mA
Maximum motor current	I_{max}	100 A
ADC reference voltage	V_{VREF}	3.3 V
Winding sense current range	I_{SENSE}	–40 A to +40 A
Motor RMS current	I_{RMS}	28.3 A
Sense resistor power rating	P_{SENSE}	3 W
System ambient temperature	T_A	–20°C to +60°C

14.2.1.2 Detailed Design Procedure

表 14-2 lists the recommended values of the external components for the gate driver.

表 14-2. DRV8353M Gate-Driver External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	X5R or X7R, 0.1-µF, VM-rated capacitor
C_{VM2}	VM	GND	≥ 10 µF, VM-rated capacitor
C_{VCP}	VCP	VM	X5R or X7R, 1-µF, 16-V capacitor
C_{VGLS}	VGLS	GND	X5R or X7R, 1-µF, 16-V capacitor
C_{SW}	CPH	CPL	X5R or X7R, 47-nF, VDRAIN-rated capacitor
C_{DVDD}	DVDD	DGND	X5R or X7R, 1-µF, 6.3-V capacitor
R_{nFAULT}	VCC(1)	nFAULT	Pullup resistor
R_{SDO}	VCC(1)	SDO	Pullup resistor
R_{IDRIVE}	IDRIVE	GND or DVDD	DRV8353M hardware interface
R_{VDS}	VDS	GND or DVDD	DRV8353M hardware interface
R_{MODE}	MODE	GND or DVDD	DRV8353M hardware interface
R_{GAIN}	GAIN	GND or DVDD	DRV8353M hardware interface
C_{VREF}	VREF	GND or DGND	Optional capacitor rated for VREF
R_{ASENSE}	SPA	SNA and GND	Sense shunt resistor
R_{BSENSE}	SPB	SNB and GND	Sense shunt resistor
R_{CSENSE}	SPC	SNC and GND	Sense shunt resistor

(1) VCC is not a pin on the DRV8353M family of devices, but a VCC supply voltage pullup is required for the open-drain output nFAULT and SDO. These pins can also be pulled up to DVDD.

14.2.1.2.1 External MOSFET Support

The DRV833M family of devices MOSFET support is based on the MOSFET gate charge, VCP charge-pump capacity, VGLS regulator capacity, and output PWM switching frequency. For a quick calculation of MOSFET driving capacity, use Equation 5 and Equation 6 for three phase BLDC motor applications.

Trapezoidal 120° Commutation: $I_{VCP/VGLS} > Q_g \times f_{PWM}$ (5)

Sinusoidal 180° Commutation: $I_{VCP/VGLS} > 3 \times Q_g \times f_{PWM}$ (6)

where

- f_{PWM} is the maximum desired PWM switching frequency.
- Q_g is the MOSFET total gate charge
- $I_{VCP/VGLS}$ is the charge pump or low-side regulator capacity, dependent on the VM pin voltage.
- The MOSFET multiplier based on the commutation control method, may vary based on implementation.

14.2.1.2.1.1 MOSFET Example

If a system is using V_{VM} = 48 V (I_{VCP} = 25 mA) and a maximum PWM switching frequency of 45 kHz, then the VCP charge-pump and VGLS regulator can support MOSFETs using trapezoidal commutation with a Q_g < 556 nC, and MOSFETs using sinusoidal commutation with a Q_g < 185 nC.

14.2.1.2.2 IDRIVE Configuration

The gate drive current strength, I_{DRIVE}, is selected based on the gate-to-drain charge of the external MOSFETs and the target rise and fall times at the outputs. If I_{DRIVE} is selected to be too low for a given MOSFET, then the MOSFET may not turn on completely within the t_{DRIVE} time and a gate drive fault may be asserted. Additionally, slow rise and fall times will lead to higher switching power losses. TI recommends adjusting these values in system with the required external MOSFETs and motor to determine the best possible setting for any application.

The I_{DRIVEP} and I_{DRIVEN} current for both the low-side and high-side MOSFETs are independently adjustable on SPI devices through the SPI registers. On hardware interface devices, both source and sink settings are selected at the same time on the IDRIVE pin.

For MOSFETs with a known gate-to-drain charge Q_{gd}, desired rise time (t_r), and a desired fall time (t_f), use Equation 7 and Equation 8 to calculate the value of I_{DRIVEP} and I_{DRIVEN} (respectively).

$$I_{DRIVEP} > \frac{Q_{gd}}{t_r} \tag{7}$$

$$I_{DRIVEN} > \frac{Q_{gd}}{t_f} \tag{8}$$

14.2.1.2.2.1 IDRIVE Example

Use Equation 9 and Equation 10 to calculate the value of $I_{DRIVEP1}$ and $I_{DRIVEP2}$ (respectively) for a gate to drain charge of 13 nC and a rise time from 100 to 300 ns.

$$I_{DRIVEP1} = \frac{13\ \text{nC}}{100\ \text{ns}} = 130\ \text{mA} \tag{9}$$

$$I_{DRIVEP2} = \frac{13\ \text{nC}}{300\ \text{ns}} = 43\ \text{mA} \tag{10}$$

Select a value for I_{DRIVEP} that is between 43 mA and 130 mA. For this example, the value of I_{DRIVEP} was selected as 100-mA source.

Use Equation 11 and Equation 12 to calculate the value of $I_{DRIVEN1}$ and $I_{DRIVEN2}$ (respectively) for a gate to drain charge of 13 nC and a fall time from 50 to 150 ns.

$$I_{DRIVEN1} = \frac{13\ \text{nC}}{50\ \text{ns}} = 260\ \text{mA} \tag{11}$$

$$I_{DRIVEN2} = \frac{13\ \text{nC}}{150\ \text{ns}} = 87\ \text{mA} \tag{12}$$

Select a value for I_{DRIVEN} that is between 87 mA and 260 mA. For this example, the value of I_{DRIVEN} was selected as 200-mA sink.

14.2.1.2.3 V_{DS} Overcurrent Monitor Configuration

The V_{DS} monitors are configured based on the worst-case motor current and the $R_{DS(on)}$ of the external MOSFETs as shown in Equation 13.

$$V_{DS\_OCP} > I_{max} \times R_{DS(on)max} \tag{13}$$

14.2.1.2.3.1 V_{DS} Overcurrent Example

The goal of this example is to set the V_{DS} monitor to trip at a current greater than 75 A. According to the *CSD19535KCS 100 V N-Channel NexFET™ Power MOSFET* data sheet, the $R_{DS(on)}$ value is 2.2 times higher at 175°C, and the maximum $R_{DS(on)}$ value at a V_{GS} of 10 V is 3.6 mΩ at T_A = 25°C. From these values, the approximate worst-case value of $R_{DS(on)}$ is 2.2 × 3.6 mΩ = 7.92 mΩ.

Using Equation 14 with a value of 7.92 mΩ for $R_{DS(on)}$ and a worst-case motor current of 75 A, Equation 14 shows the calculated desired value of the V_{DS} overcurrent monitors.

$$V_{DS\_OCP} > 75\ \text{A} \times 7.92\ \text{m}\Omega$$
$$V_{DS\_OCP} > 0.594\ \text{V} \tag{14}$$

For this example, the value of V_{DS_OCP} was selected as 0.6 V.

The SPI devices allow for adjustment of the deglitch time for the V_{DS} overcurrent monitor. The deglitch time can be set to 1 µs, 2 µs, 4 µs, or 8 µs.

14.2.1.2.4 Sense-Amplifier Bidirectional Configuration

The sense amplifier gain on the DRV8353M and sense resistor value are selected based on the target current range, VREF reference voltage, sense-resistor power rating, and operating temperature range. In bidirectional operation of the sense amplifier, the dynamic range at the output is approximately calculated as shown in Equation 15.

$$V_O = \left(V_{VREF} - 0.25\ \text{V}\right) - \frac{V_{VREF}}{2} \tag{15}$$

Use Equation 16 to calculate the approximate value of the selected sense resistor with V_O calculated using Equation 15.

$$R = \frac{V_O}{A_V \times I} \qquad P_{SENSE} > I_{RMS}{}^2 \times R \tag{16}$$

From Equation 15 and Equation 16, select a target gain setting based on the power rating of the target sense resistor.

14.2.1.2.4.1 Sense-Amplifier Example

In this system example, the value of VREF voltage is 3.3 V with a sense current from –40 to +40 A. The linear range of the SOx output is 0.25 V to V_{VREF} – 0.25 V (from the V_{LINEAR} specification). The differential range of the sense amplifier input is –0.3 to +0.3 V (V_{DIFF}).

$$V_O = \left(3.3\ \text{V} - 0.25\ \text{V}\right) - \frac{3.3\ \text{V}}{2} = 1.4\ \text{V} \tag{17}$$

$$R = \frac{1.4\ \text{V}}{A_V \times 40\ \text{A}} \qquad 2\ \text{W} > 28.3^2 \times R \rightarrow R < 2.5\ \text{m}\Omega \tag{18}$$

$$2.5\ \text{m}\Omega > \frac{1.4\ \text{V}}{A_V \times 40\ \text{A}} \rightarrow A_V > 14 \tag{19}$$

Therefore, the gain setting must be selected as 20 V/V or 40 V/V and the value of the sense resistor must be less than 2.5 mΩ to meet the power requirement for the sense resistor. For this example, the gain setting was selected as 20 V/V. The value of the resistor and worst case current can be verified that R < 2.5 mΩ and I_{max} = 40 A does not violate the differential range specification of the sense amplifier input (V_{SPxD}).

14.2.1.2.5 Single Supply Power Dissipation

Design care must be taken to make sure that the thermal ratings of the DRV8353M are not violated during normal operation of the device. The is especially critical in higher voltage and higher ambient operation applications where power dissipation or the device ambient temperature are increased.

To determine the temperature of the device in single supply operation, first the power internal power dissipation must be calculated. The internal power dissipation has four primary components:

- VCP charge pump power dissipation (P_{VCP})
- VGLS low-side regulator power dissipation (P_{VGLS})
- VM device nominal power dissipation (P_{VM})
- VIN buck regulator power dissipation (P_{BUCK})

The values of P_{VCP} and P_{VGLS} can be approximated by referring to *セクション 14.2.1.2.1* to first determine I_{VCP} and I_{VGLS} and then referring to Equation 20 and Equation 21.

$$P_{VCP} = I_{VCP} \times (V_{VM} + V_{VDRAIN}) \tag{20}$$

$$P_{VGLS} = I_{VGLS} \times V_{VM} \tag{21}$$

The value of P_{VM} can be calculated by referring to the data sheet parameter for I_{VM} current and Equation 22.

$$P_{VM} = I_{VM} \times V_{VM} \tag{22}$$

$$P_{BUCK} = (P_O / \eta) - P_O \tag{23}$$

where

- $P_O = V_{VCC} \times I_{VCC}$

The value of P_{BUCK} can be calculated with the buck output voltage (V_{VCC}), buck output current (I_{VCC}), and by referring to the typical characteristic curve for efficiency (η) in the LM5008A data sheet.

The total power dissipation is then calculated by summing the four components as shown in Equation 24.

$$P_{tot} = P_{VCP} + P_{VGLS} + P_{VM} + P_{BUCK} \tag{24}$$

Lastly, the device junction temperature can be estimate by referring to *セクション 10* and Equation 25.

$$T_J\text{max} = T_A\text{max} + (R_{\theta JA} \times P_{tot}) \tag{25}$$

The information in *セクション 10* is based off of a standardized test metric for package and PCB thermal dissipation. The actual values may vary based on the actual PCB design used in the application.

14.2.1.2.6 Single Supply Power Dissipation Example

In this application example the device is configured for single supply operation. This configuration requires only one power supply for the DRV8353M but comes at the tradeoff of increased internal power dissipation. The junction temperature is estimated in the example below.

Use Equation 26 to calculate the value of I_{VCP} and I_{VGLS} for a MOSFET gate charge of 78 nC, all 3 high-side and 3 low-side MOSFETs switching, and a switching frequency of 45 kHz.

$$I_{VCP/VGLS} = 78\text{ nC} \times 3 \times 45\text{ kHz} = 10.5\text{ mA} \tag{26}$$

Use Equation 27, Equation 28, Equation 29, Equation 30, and Equation 31 to calculate the value of P_{tot} for V_{VM} = V_{VDRAIN} = V_{VIN} = 48 V, I_{VM} = 9.5 mA, I_{VCP} = 10.5 mA, I_{VGLS} = 10.5 mA, V_{VCC} = 3.3 V, I_{VCC} = 100 mA, and η = 86 %.

$$P_{VCP} = 10.5\text{ mA} \times (48\text{ V} + 48\text{ V}) = 1\text{ W} \tag{27}$$

$$P_{VGLS} = 10.5\text{ mA} \times 48\text{ V} = 0.5\text{ W} \tag{28}$$

$$P_{VM} = 9.5\text{ mA} \times 48\text{ V} = 0.5\text{ W} \tag{29}$$

$$P_{BUCK} = [(3.3\text{ V} \times 100\text{ mA}) / 0.86] - (3.3\text{ V} \times 100\text{ mA}) = 0.054\text{ W} \tag{30}$$

$$P_{tot} = 1\text{ W} + 0.5\text{ W} + 0.5\text{ W} + 0.054 = 2.054\text{ W} \tag{31}$$

Lastly, to estimate the device junction temperature during operation, use Equation 32 to calculate the value of $T_J$max for $T_A$max = 60°C, $R_{θJA}$ = 26.6°C/W for the RGZ package, and P_{tot} = 2.054 W. Again, please note that the $R_{θJA}$ is highly dependent on the PCB design used in the actual application and should be verified. For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

$$T_J\text{max} = 60°\text{C} + (26.6°\text{C/W} \times 2.054\text{ W}) = 115°\text{C} \tag{32}$$

As shown in this example, the device is within its operational limits, but is operating almost to its maximum operational junction temperature. Design care should be taken in the single supply configuration to correctly manage the power dissipation of the device.

14.2.1.3 Application Curves

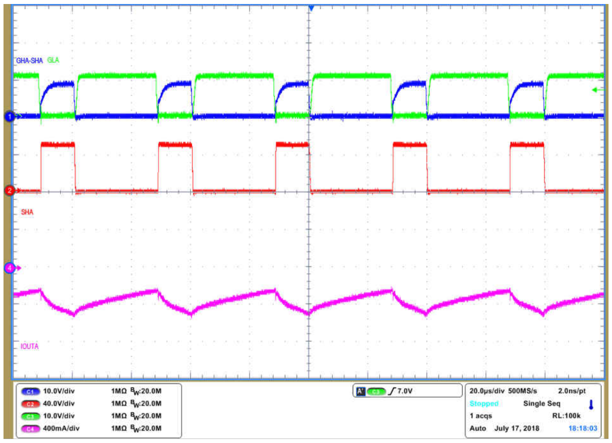


図 14-2. Gate Driver Operation 30% Duty Cycle

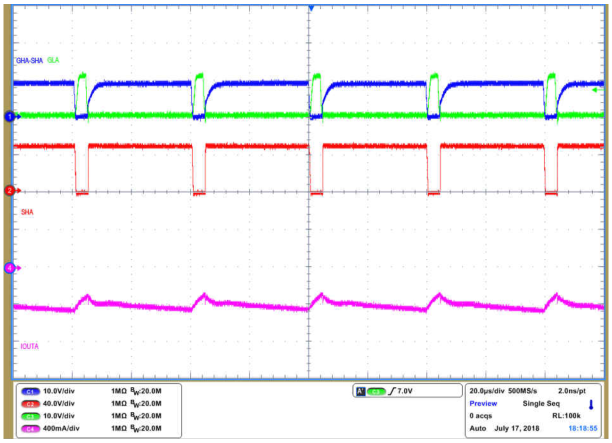


図 14-3. Gate Driver Operation 90% Duty Cycle

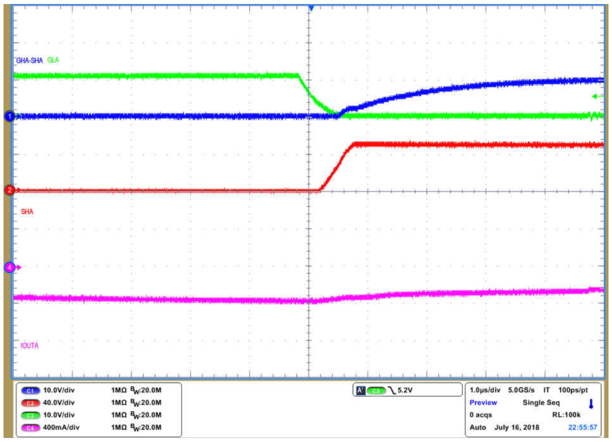


図 14-4. IDRIVE Minimum Setting Positive Current

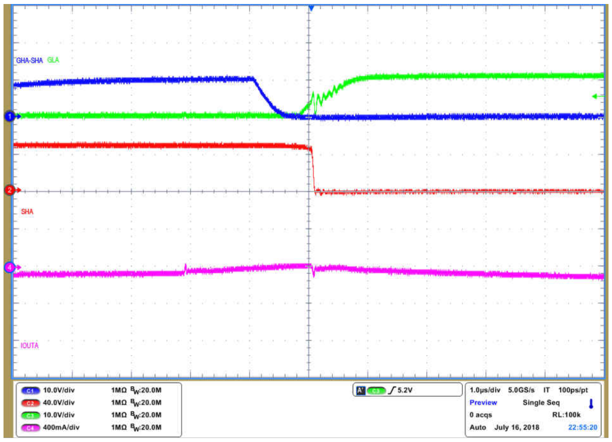


図 14-5. IDRIVE Minimum Setting Negative Current

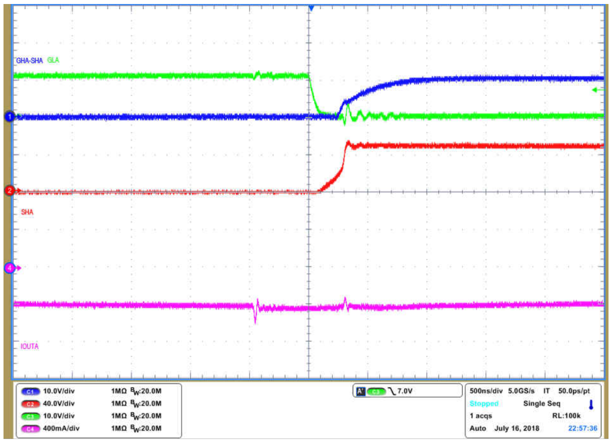


図 14-6. IDRIVE 300-mA and 600-mA Setting Positive Current

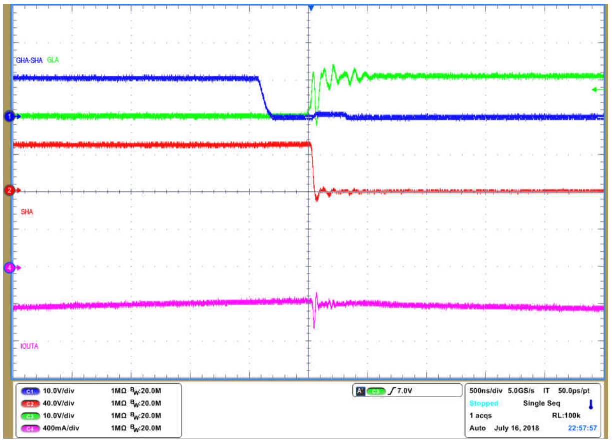


図 14-7. IDRIVE 300-mA and 600-mA Setting Negative Current

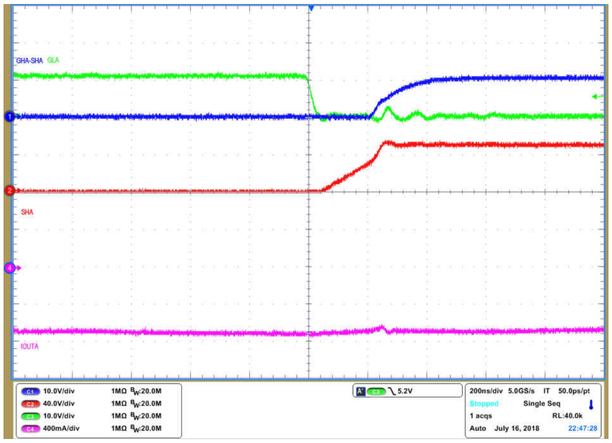


図 14-8. IDRIVE Maximum Setting Positive Current

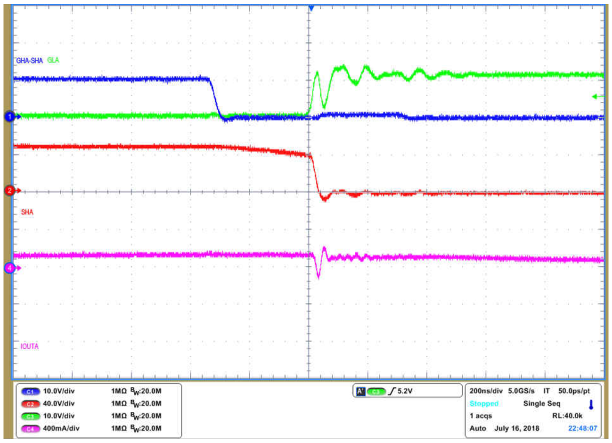


図 14-9. IDRIVE Maximum Setting Negative Current

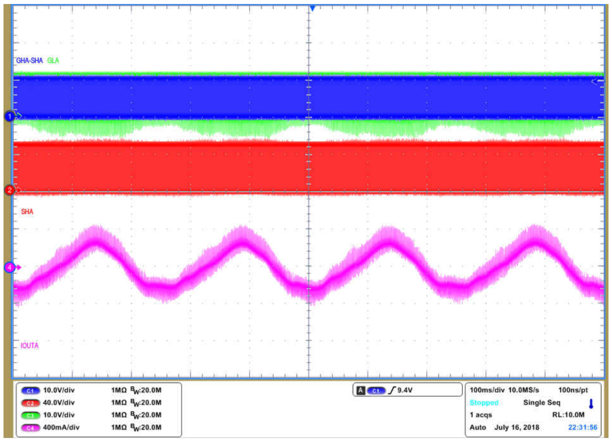


図 14-10. FOC Motor Commutation

15 Power Supply Recommendations

The DRV8353M family of devices are designed to operate from an input voltage supply (VM) range between 9 V and 75 V. A 0.1-µF ceramic capacitor rated for VM must be placed as near to the device as possible. In addition, a bulk capacitor must be included on the VM pin but can be shared with the bulk bypass capacitance for the external power MOSFETs. Additional bulk capacitance is required to bypass the external half-bridge MOSFETs and should be sized according to the application requirements.

15.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is usually beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size. The amount of local capacitance depends on a variety of factors including:

- The highest current required by the motor system
- The power supply's type, capacitance, and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable supply voltage ripple
- Type of motor (brushed DC, brushless DC, stepper)
- The motor startup and braking methods

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage stays stable and high current can be quickly supplied.

The data sheet provides a recommended minimum value, but system level testing is required to determine the appropriate sized bulk capacitor.

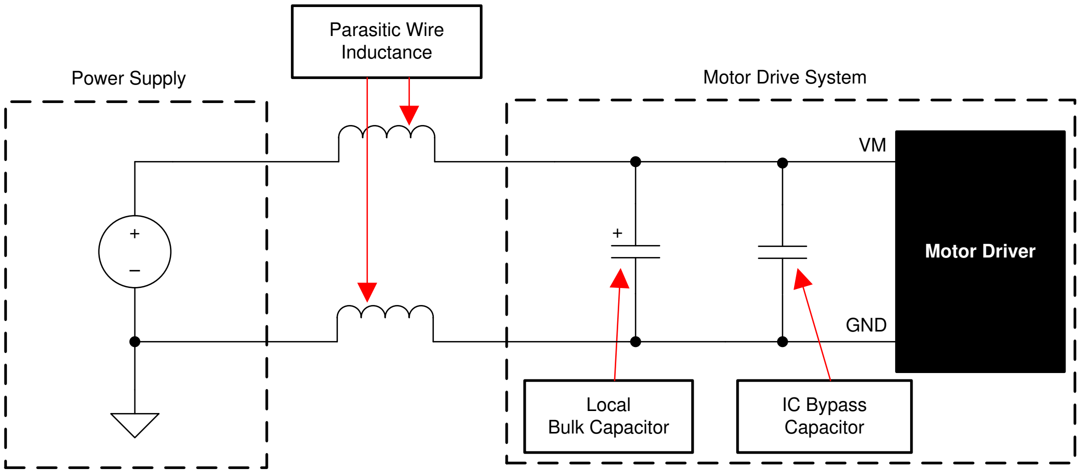


図 15-1. Motor Drive Supply Parasitics Example

16 Layout

16.1 Layout Guidelines

Bypass the VM pin to the GND pin using a low-ESR ceramic bypass capacitor with a recommended value of 0.1 μF. Place this capacitor as near to the VM pin as possible with a thick trace or ground plane connected to the GND pin. Additionally, bypass the VM pin using a bulk capacitor rated for VM. This component can be electrolytic. This capacitance must be at least 10 μF.

Additional bulk capacitance is required to bypass the high current path on the external MOSFETs. This bulk capacitance should be placed such that it minimizes the length of any high current paths through the external MOSFETs. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Place a low-ESR ceramic capacitor between the CPL and CPH pins. This capacitor should be 47 nF, rated for VDRAIN, and be of type X5R or X7R. Additionally, place a low-ESR ceramic capacitor between the VCP and VDRAIN pins and VGLS and GNDs. These capacitors should be 1 μF, rated for 16 V, and be of type X5R or X7R.

Bypass the DVDD pin to the GND/DGND pin with a 1-μF low-ESR ceramic capacitor rated for 6.3 V and of type X5R or X7R. Place this capacitor as near to the pin as possible and minimize the path from the capacitor to the GND/DGND pin.

The VDRAIN pin can be shorted directly to the VM pin for single supply application configurations. However, if a significant distance is between the device and the external MOSFETs, use a dedicated trace to connect to the common point of the drains of the high-side external MOSFETs. Do not connect the SLx pins directly to GND. Instead, use dedicated traces to connect these pins to the sources of the low-side external MOSFETs. These recommendations allow for more accurate V_{DS} sensing of the external MOSFETs for overcurrent detection.

Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the GHx pin of the device to the high-side power MOSFET gate, then follows the high-side MOSFET source back to the SHx pin. The low-side loop is from the GLx pin of the device to the low-side power MOSFET gate, then follows the low-side MOSFET source back to the SPx/SLx pins.

16.2 Layout Example

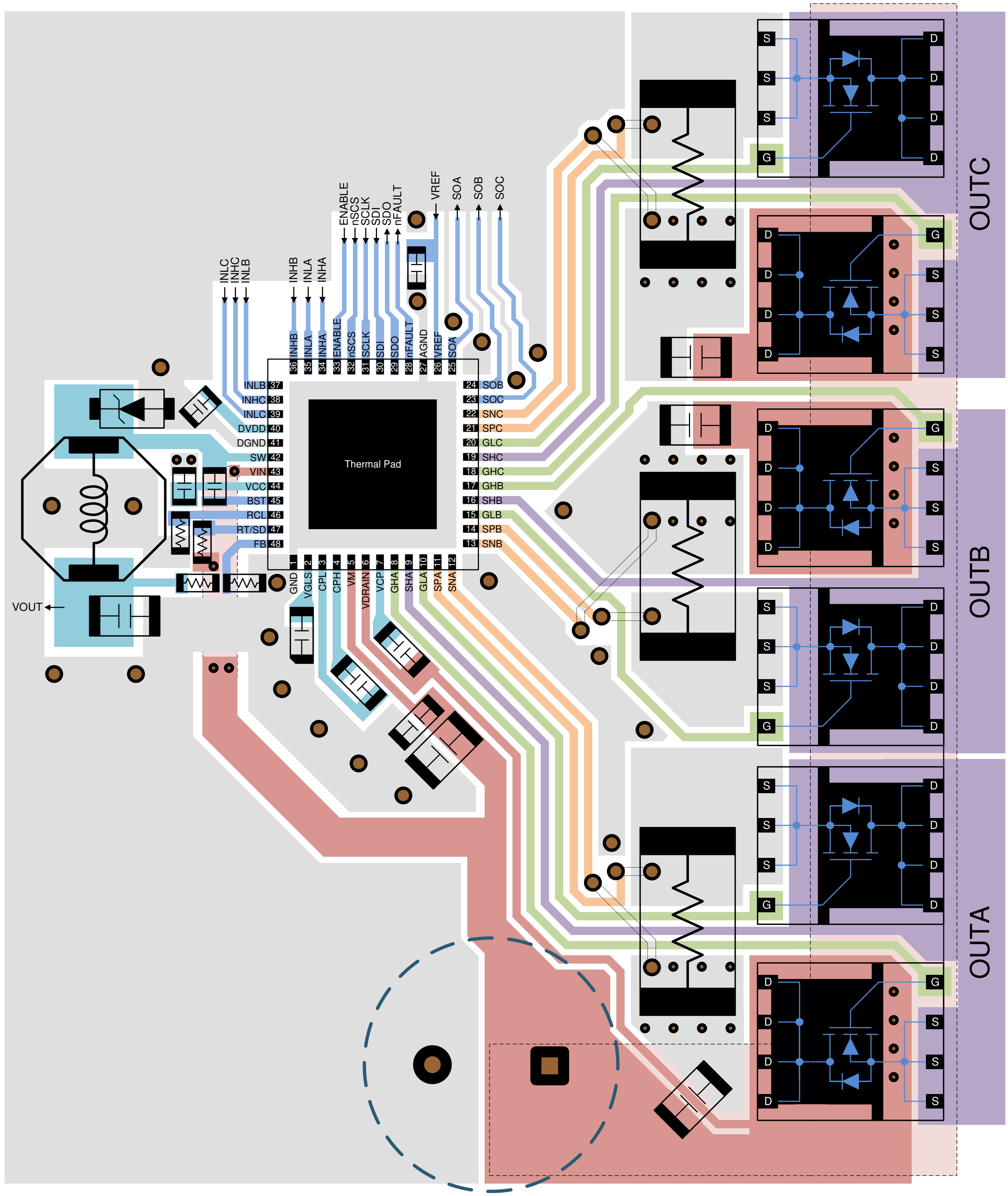


図 16-1. Layout Example

17 Device and Documentation Support

17.1 Device Support

17.1.1 Device Nomenclature

17.2 Documentation Support

17.2.1 Related Documentation

For related documentation, refer to:

- Texas Instruments, *DRV8353Rx-EVM User’s Guide* user's guide
- Texas Instruments, *DRV8353Rx-EVM GUI User’s Guide*
- Texas Instruments, *DRV8353Rx-EVM InstaSPIN™ Software Quick Start Guide*
- Texas Instruments, *DRV8350x-EVM User’s Guide* user's guide
- Texas Instruments, *DRV8350x-EVM GUI User’s Guide* user's guide
- Texas Instruments, *DRV8350x-EVM Sensorless Software User's Guide* user's guide
- Texas Instruments, *DRV8350x-EVM Sensored Software User's Guide* user's guide
- Texas Instruments, *LM5008A 100-V 350-mA Constant On-Time Buck Switching Regulator* data sheet
- Texas Instruments, *CSD19535KCS 100 V N-Channel NexFET™ Power MOSFET* data sheet
- Texas Instruments, *Understanding IDRIVE and TDRIVE In TI Motor Gate Drivers* application report
- Texas Instruments, *Motor Drive Protection with TI Smart Gate Drive* TI TechNote
- Texas Instruments, *Reduce Motor Drive BOM and PCB Area with TI Smart Gate Drive* TI TechNote
- Texas Instruments, *Reducing EMI Radiated Emissions with TI Smart Gate Drive* TI TechNote
- Texas Instruments, *Hardware Design Considerations for an Efficient Vacuum Cleaner using BLDC Motor*
- Texas Instruments, *Hardware Design Considerations for an Electric Bicycle using BLDC Motor*
- Texas Instruments, *Industrial Motor Drive Solution Guide*
- Texas Instruments, *Layout Guidelines for Switching Power Supplies* application report
- Texas Instruments, *QFN/SON PCB Attachment* application report
- Texas Instruments, *Sensored 3-Phase BLDC Motor Control Using MSP430™ application report*
- Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies* application report

17.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報の 1 週間分のダイジェストを受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

17.4 サポート・リソース

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この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

17.7 用語集

TI 用語集	この用語集には、用語や略語の一覧および定義が記載されています。

18 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8353HMRTAT	Active	Production	WQFN (RTA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	DRV 8353HM
DRV8353HMRTAT.A	Active	Production	WQFN (RTA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	DRV 8353HM
DRV8353HMRTATG4	Active	Production	WQFN (RTA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	DRV 8353HM
DRV8353HMRTATG4.A	Active	Production	WQFN (RTA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	DRV 8353HM
DRV8353SMRTAT	Active	Production	WQFN (RTA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	DRV 8353SM
DRV8353SMRTAT.A	Active	Production	WQFN (RTA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	DRV 8353SM
DRV8353SMRTATG4	Active	Production	WQFN (RTA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	DRV 8353SM
DRV8353SMRTATG4.A	Active	Production	WQFN (RTA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	DRV 8353SM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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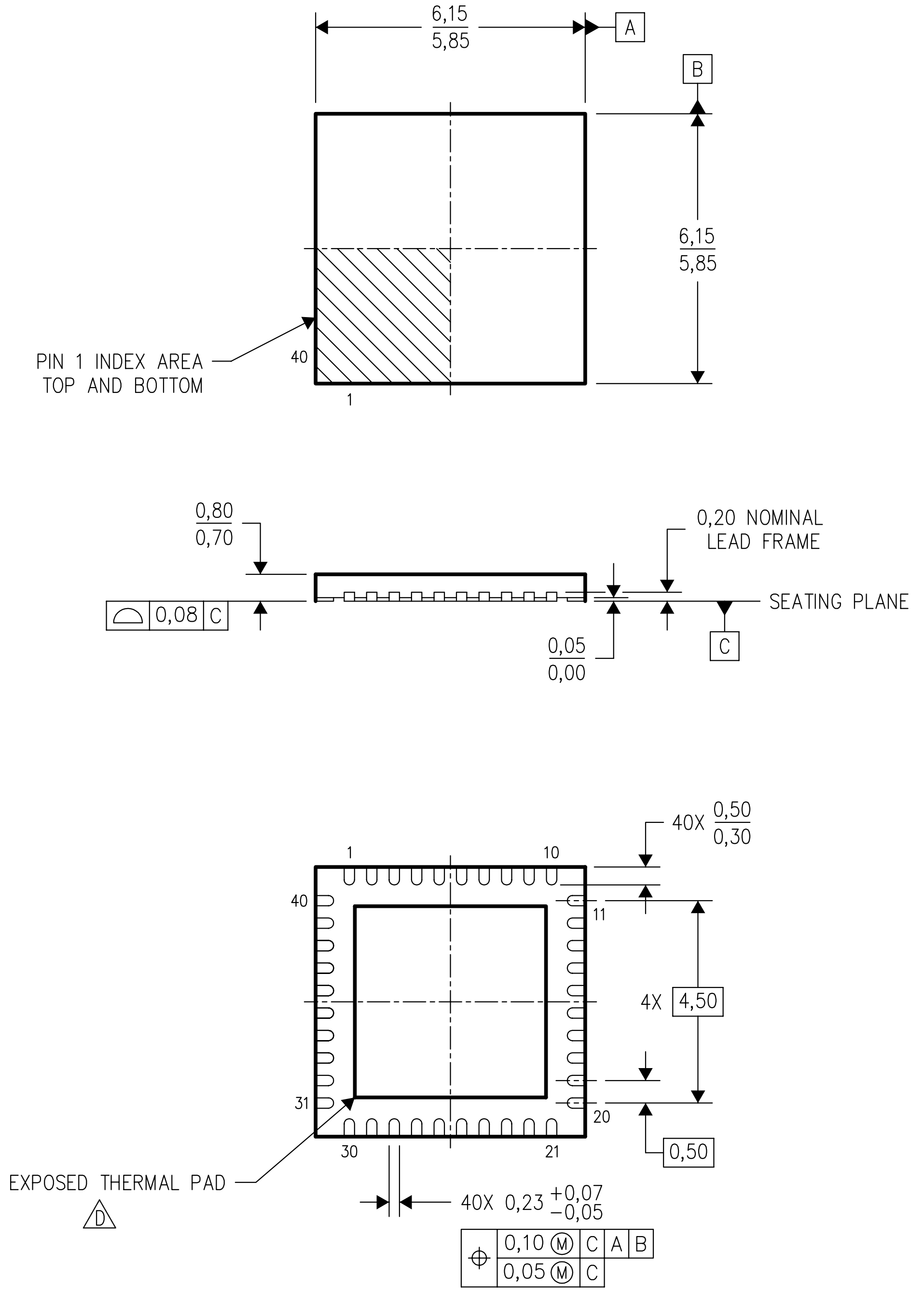
RTA (S–PQFP–N40) PLASTIC QUAD FLATPACK



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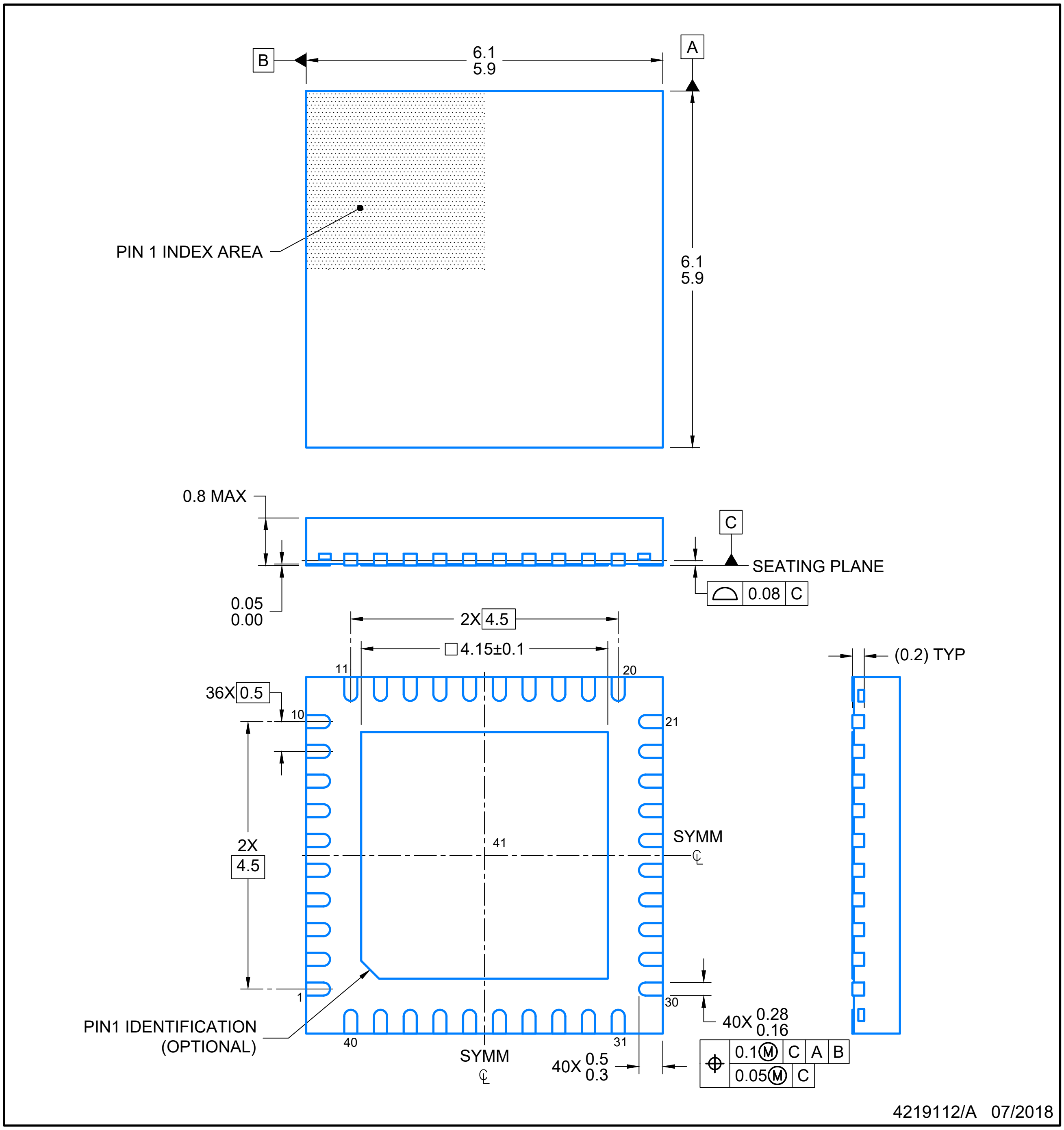
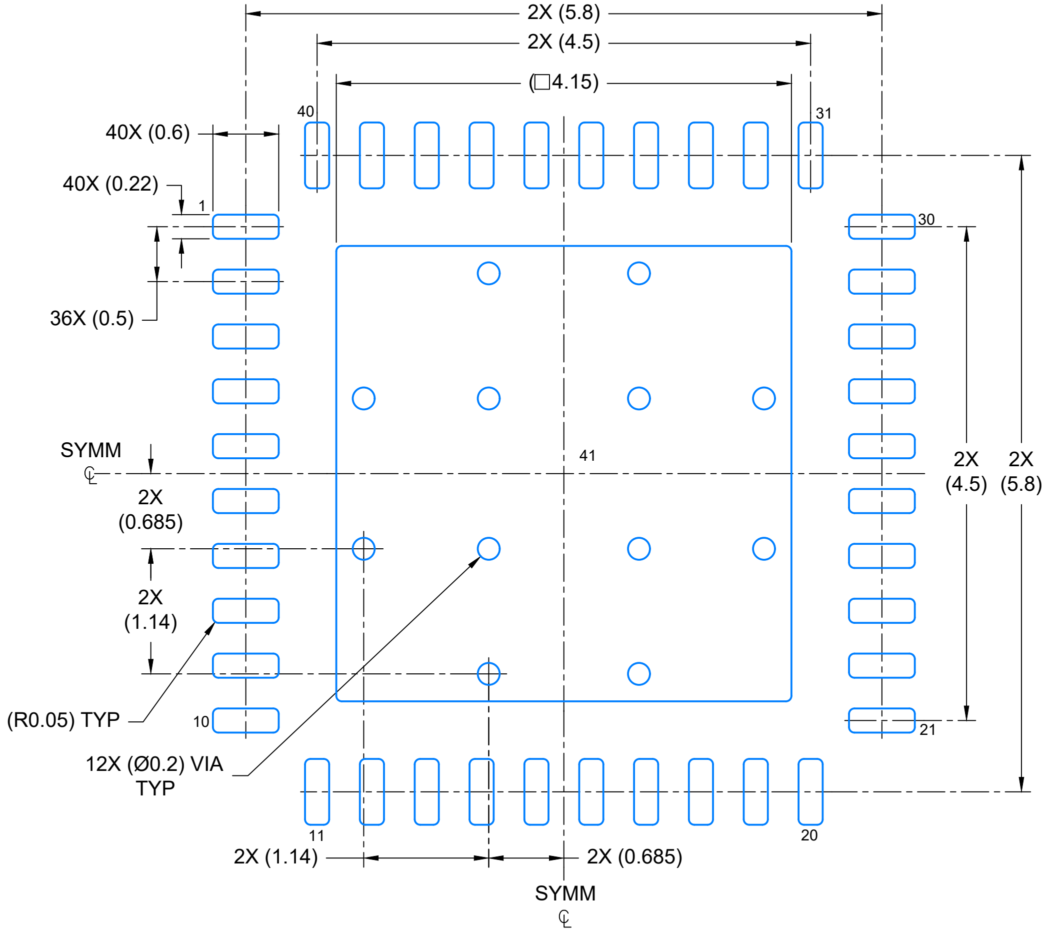
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

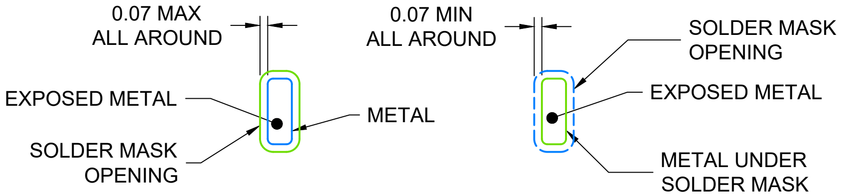


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 15X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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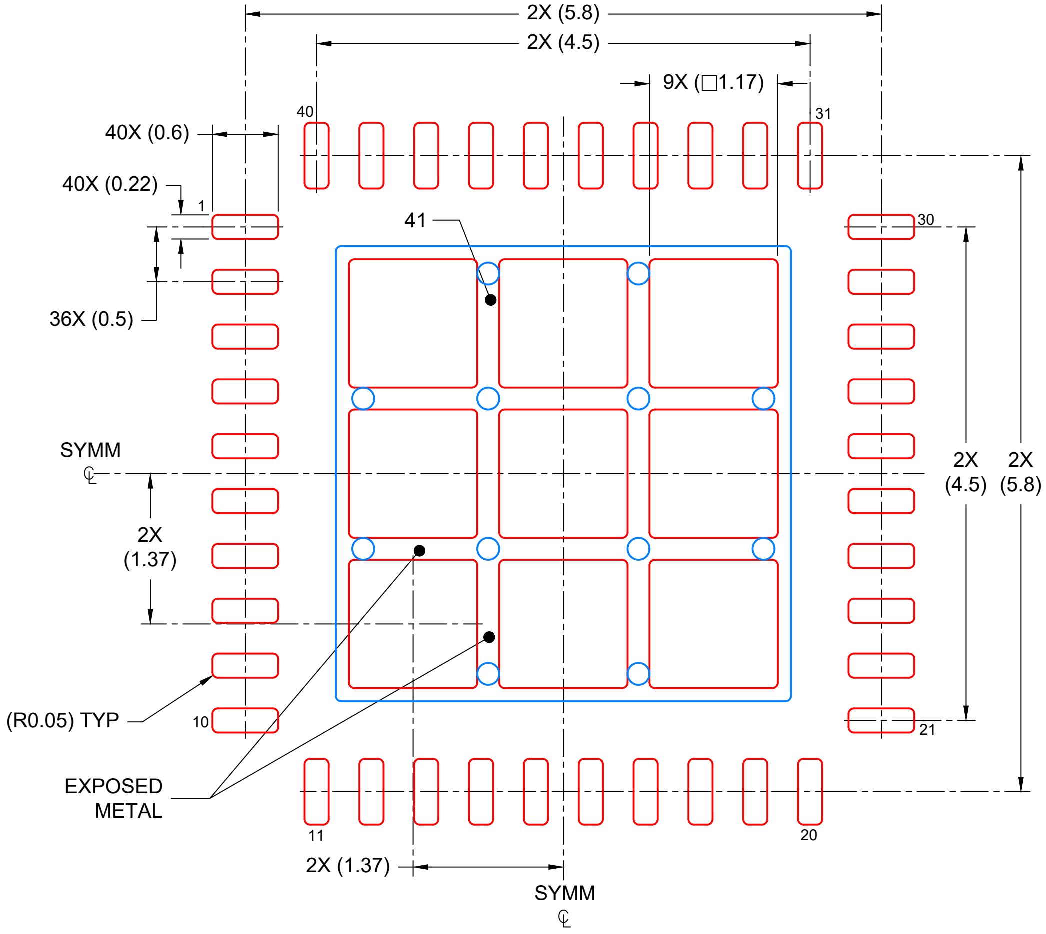
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
71% PRINTED COVERAGE BY AREA
SCALE: 15X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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