DRV8306 38VブラシレスDCモータ・コントローラ

1 特長

- **6V～38V、トリプル・ハーフブリッジ、3xホール・コンパレータ搭載のゲート・ドライバ**
  - 絶対最大定格40V
  - 12Vおよび24V DCレールに完全最適化
  - ハイサイドとローサイドのNチャネルMOSFETを駆動
  - 100%のPWMデューティ・サイクルをサポート
- **スマート・ゲート・ドライブ・アーキテクチャ**
  - 可変スルーレート制御によりEMI/EMC性能が向上
  - V_{GS}ハンドシェークおよび最小限のデッドタイム挿入により貫通電流を回避
  - 15mA～150mAのピーク・ソース電流
  - 30mA～300mAのピーク・シンク電流
- **ホール・センサからの整流機能を内蔵**
  - 120°台形電流制御
  - 低コストのホール素子をサポート
  - タコ出力信号(FGOUT)による閉ループの速度制御
- **ゲート・ドライバ電源を内蔵**
  - ハイサイドのチャージ・ポンプ
  - ローサイドのリニア・レギュレータ
- **サイクルごとの電流制限**
- **1.8V、3.3V、5Vのロジック入力電圧をサポート**
- **低電力スリープ・モード**
- **リニア電圧レギュレータ、3.3V、30mA**
- **小型で占有面積の小さいVQFNパッケージ**
- **保護機能を内蔵**
  - VM低電圧誤動作防止（UVLO）
  - チャージ・ポンプ低電圧（CPUV）
  - MOSFET過電流保護（OCP）
  - ゲート・ドライバ障害（GDF）
  - サーマル・シャットダウン(OTSD)
  - 障害状況インジケータ（nFAULT）

2 アプリケーション

- **BLDCモータ・モジュール**
- **サービス・ロボットやサービス・ロボティクス**
- **掃除機**
- **ドローン、ロボティクス、ラジコン玩具**
- **白物家電**
- **ATMおよび貨幣計数機**

3 概要

DRV8306デバイスは、3相ブラシレスDC (BLDC)モータ・アプリケーション用の統合ゲート・ドライバです。このデバイスには、3つのハーフ・ブリッジ・ゲート・ドライバがあり、それぞれがハイサイドとローサイドのNチャネル・パワーMOSFETを駆動できます。DRV8306デバイスは、内蔵のチャージ・ポンプを使用してハイサイドMOSFET用の、リニア・レギュレータを使用してローサイドMOSFET用の、適切なゲート駆動電圧を生成します。スマート・ゲート駆動アーキテクチャは、最大150mAのソースおよび300mAのシンク・ピーク・ゲート駆動電流と、15mAのrmsゲート駆動電流をサポートします。

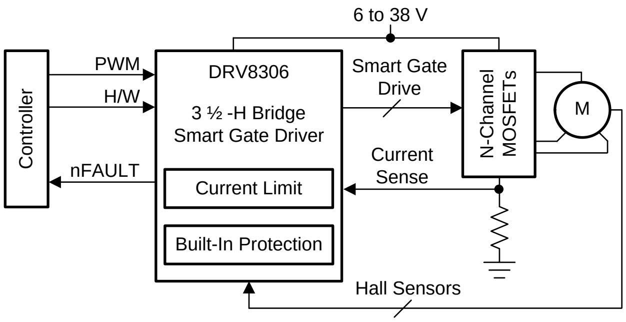
このデバイスには、台形BLDCモータ用に120°整流機能が内蔵されています。DRV8306デバイスには3つのホール・コンパレータがあり、ホール素子からの入力を使用して内部整流を行います。モータの位相電圧のデューティ・サイクル比は、PWMピンで変更できます。ブレーキ(nBRAKE)および方向(DIR)ピンが用意されており、BLDCモータのブレーキおよび方向設定に使用できます。3.3V、30mAの低ドロップアウト(LDO)レギュレータにより、外部のコントローラとホール素子に給電できます。追加のFGOUT信号が用意されており、整流周波数の測定値を示します。この信号を使用して、BLDCモータの閉ループ制御を実装できます。

製品情報[1]

型番	パッケージ	本体サイズ（公称）
DRV8306	VQFN (32)	4.00mm×4.00mm

[1] 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年4月発行のものから更新 **Page**

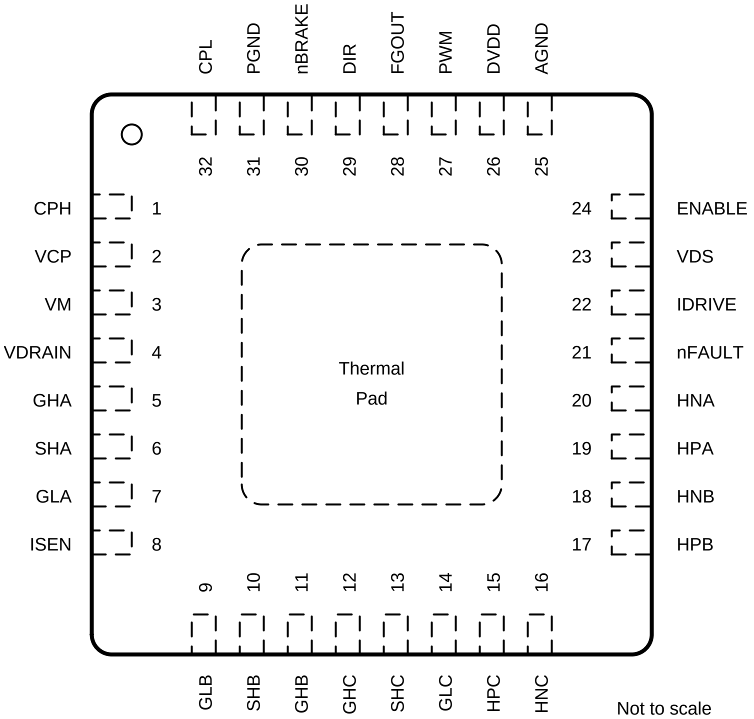
- データシートのステータスを「事前情報」から「量産データ」に 変更 1

5 概要（続き）

低消費電力のスリープ・モードがあり、内部回路のほとんどをシャットダウンして、静止電流を低減できます。低電圧誤動作防止、チャージ・ポンプ障害、MOSFET過電流、MOSFET短絡、ゲート・ドライバ障害、過熱に対する保護機能が内蔵されています。障害状況は、nFAULTピンにより示されます。

6 Pin Configuration and Functions

RSM Package
32-Pin VQFN With Exposed Thermal Pad
Top View



Not to scale

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AGND	25	PWR	Device analog ground. Connect to system ground.
CPH	1	PWR	Charge-pump switching node. Connect a X5R or X7R, 22-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
CPL	32	PWR	Charge-pump switching node. Connect a X5R or X7R, 22-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
DIR	29	I	Direction pin for setting the direction of the motor rotation to clockwise or counterclockwise. Internal pulldown resistor.
DVDD	26	PWR	3.3-V internal regulator output. Connect a X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the DVDD and AGND pins. This regulator can source up to 30 mA externally.
ENABLE	24	I	Gate driver enable. When this pin is logic low the device enters a low-power sleep mode. A 15 to 40-µs low pulse can be used to reset fault conditions.
FGOUT	28	OD	Outputs a commutation zero crossing signal generated from Hall sensors.
GHA	5	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	11	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	12	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	7	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	9	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLC	14	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
HNA	20	I	Hall element negative input. Noise filter capacitors may be desirable, connected between the positive and negative Hall inputs.
HNB	18	I	Hall element negative input. Noise filter capacitors may be desirable, connected between the positive and negative Hall inputs.
HNC	16	I	Hall element negative input. Noise filter capacitors may be desirable, connected between the positive and negative Hall inputs.
HPA	19	I	Hall element positive input. Noise filter capacitors may be desirable, connected between the positive and negative Hall inputs.
HPB	17	I	Hall element positive input. Noise filter capacitors may be desirable, connected between the positive and negative Hall inputs.
HPC	15	I	Hall element positive input. Noise filter capacitors may be desirable, connected between the positive and negative Hall inputs.
IDRIVE	22	I	Gate drive output current setting. This pin is a 7 level input pin set by an external resistor.
ISEN	8	I	Current sense for pulse-by-pulse current limit. Connect to low-side current sense resistor.
PGND	31	PWR	Device power ground. Connect to system ground.

(1) PWR = power, I = input, O = output, OD = open-drain

Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
PWM	27	I	PWM input for motor control. Set the output voltage and switching frequency of the phase voltage of the motor.
SHA	6	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHB	10	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHC	13	I	High-side source sense input. Connect to the high-side power MOSFET source.
VCP	2	PWR	Charge pump output. Connect a X5R or X7R, 1-µF, 16-V ceramic capacitor between the VCP and VM pins.
VDRAIN	4	I	High-side MOSFET drain sense input. Connect to the common point of the MOSFET drains.
VDS	23	I	VDS monitor trip point setting. This pin is a 7 level input pin set by an external resistor.
VM	3	PWR	Gate driver power supply input. Connect to the bridge power supply. Connect a X5R or X7R, 0.1-µF, VM-rated ceramic and greater then or equal to 10-uF local capacitance between the VM and PGND pins.
nBRAKE	30	I	Causes motor to brake. Internal pulldown resistor.
nFAULT	21	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pullup resistor.

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	40	V
Voltage differential between any ground pin (AGND, DGND, PGND)	–0.5	0.5	V
Internal logic regulator voltage (DVDD)	–0.3	3.8	V
MOSFET voltage sense (VDRAIN)	–0.3	40	V
Charge pump voltage (VCP, CPH)	–0.3	VM + 13.5	V
Charge pump negative switching pin voltage (CPL)	–0.3	VM	V
Digital pin voltage (PWM, DIR, nBRAKE, nFAULT, ENABLE, VDS, IDRIVE, FGOUT)	–0.3	5.75	V
Open drain output current range (nFAULT, FGOUT)	0	5	mA
Continuous high-side gate pin voltage (GHX)	–2	VCP + 0.5	V
Pulsed 200 ns high-side gate pin voltage (GHX)	-5	VCP + 0.5	V
High-side gate voltage with respect to SHX (GHX)	–0.3	13.5	V
Continuous phase node pin voltage (SHX)	–2	VM + 2	V
Pulsed 200 ns phase node pin voltage (SHX)	-5	VM + 2	V
Continuous low-side gate pin voltage (GLX)	–1	13.5	V
Pulsed 200 ns low-side gate pin voltage (GLX)	-5	13.5	V
Gate pin source current (GHX, GLX)	Internally limited		A
Gate pin sink current (GHX, GLX)	Internally limited		A
Hall sensor input terminal voltage (HPA, HPB, HPC, HNA, HNB, HNC)	0	DVDD	V
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 [2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Power supply voltage range	6	38	V
V_I	Logic level input voltage range	0	5.5	V
f_{PWM}	Applied PWM signal (PWM)		200 (1)	kHz
I_{GATE_HS}	High-side average gate drive current (GHX)		15 (1)	mA
I_{GATE_LS}	Low-side average gate drive current (GLX)		15 (1)	mA
I_{DVDD}	DVDD external load current		30 (1)	mA
f_{HALL}	Hall sensor input frequency	0	30	kHz
V_{OD}	Open drain pull up voltage (nFAULT, FGOUT)	0	5.5	V
I_{OD}	Open drain output current (nFAULT, FGOUT)	0	5	mA
T_A	Operating ambient temperature	–40	125	°C

(1) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC (1)		DRV8306 RSM (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at V_{VM} = 6 to 38 V over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	V_{VM} = 24 V; ENABLE = 1; PWM = 0 V		5	8	mA
I_{VMQ}	VM sleep mode supply current	ENABLE = 0; V_{VM} = 24 V, T_A = 25°C		20	40	µA
		ENABLE = 0, V_{VM} = 24 V, T_A = 125°C			100	
t_{RST}	Reset pulse time	ENABLE = 0 V period to reset faults	15		40	µs
t_{SLEEP}	Sleep time	ENABLE = 0 V to driver tri-stated			200	µs
t_{WAKE}	Wake-up time	$V_{VM} > V_{UVLO}$; ENABLE = 3.3 V to output transition			1	ms
V_{DVDD}	Internal logic regulator voltage	I_{DVDD} = 0 to 30 mA	2.9	3.3	3.6	V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage with respect to VM	V_M = 12 to 38 V; I_{VCP} = 0 to 15 mA	7	10	11.5	V
		V_M = 10 V; I_{VCP} = 0 to 10 mA	6.5	7.5	9.5	
		V_M = 8 V; I_{VCP} = 0 to 5 mA	5	6	7.5	
		V_M = 6 V; I_{VCP} = 0 to 1 mA	3.8	4.3	6.5	
LOGIC-LEVEL INPUTS (PWM, DIR, nBRAKE)						
V_{IL}	Input logic low voltage		0		0.8	V
V_{IH}	Input logic high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis		100			mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V	–1		1	µA

Electrical Characteristics (continued)

at V_{VM} = 6 to 38 V over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	Input logic high current	V_{PIN} (Pin Voltage) = 5 V			100	µA
R_{PD}	Pulldown resistance (PWM, DIR, nBRAKE)	Internal pulldown to AGND		100		kΩ
LOGIC-LEVEL INPUTS (ENABLE)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis		100			mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V	–10		10	µA
I_{IH}	Input logic high current	V_{PIN} (Pin Voltage) = 5 V	–5		5	µA
SEVEN-LEVEL INPUTS (IDRIVE, VDS)						
V_{I1}	Input mode 1 voltage	Tied to AGND		0		V
V_{I2}	Input mode 2 voltage	18 kΩ ± 5% to AGND		0.5		V
V_{I3}	Input mode 3 voltage	75 kΩ ± 5% to AGND		1.1		V
V_{I4}	Input mode 4 voltage	Hi-Z		1.65		V
V_{I5}	Input mode 5 voltage	75 kΩ ± 5% to DVDD		2.2		V
V_{I6}	Input mode 6 voltage	18 kΩ ± 5% to DVDD		2.8		V
V_{I7}	Input mode 7 voltage	Tied to DVDD		3.3		V
OPEN-DRAIN OUTPUTS (nFAULT, FGOUT)						
V_{OL}	Output logic low voltage	I_{OD} = 2 mA			0.1	V
I_{OZ}	Output logic high current	V_{OD} = 5 V	–1		1	µA
GATE DRIVERS (GHX, SHX, GLX)						
V_{GHS}	High-side V_{GS} gate drive (gate-to-source)	V_{VM} = 12 to 38 V; I_{HS_GATE} = 0 to 15 mA	7	10	11.5	V
		V_{VM} = 10 V; I_{HS_GATE} = 0 to 10 mA	6.5	7.5	8.5	
		V_{VM} = 8 V; I_{HS_GATE} = 0 to 5 mA	5	6	7	
		V_{VM} = 6 V; I_{HS_GATE} = 0 to 1 mA	3.8	4.3	6.5	
V_{GSL}	Low-side V_{GS} gate drive (gate-to-source)	V_{VM} = 12 to 38 V; I_{LS_GATE} = 0 to 15 mA	7.5	10	12.5	V
		V_{VM} = 10 V; I_{LS_GATE} = 0 to 10 mA	5.5	7.5	9.5	
		V_{VM} = 8 V; I_{LS_GATE} = 0 to 5 mA	3.5	6	8.5	
		V_{VM} = 6 V; I_{LS_GATE} = 0 to 1 mA	3	4.3	6.5	
t_{DEAD}	Output dead time			120		ns
t_{DRIVE}	Peak gate drive time			4000		ns
I_{DRIVEP}	Peak source gate current (high-side and low-side)	IDRIVE tied to AGND		15		mA
		IDRIVE 18 kΩ (±5%) to AGND		45		
		IDRIVE 75 kΩ (±5%) to AGND		60		
		IDRIVE Hi-Z (> 500 kΩ to AGND)		90		
		IDRIVE 75 kΩ (±5%) to DVDD		105		
		IDRIVE 18 kΩ (±5%) to DVDD		135		
		IDRIVE tied to DVDD		150		
I_{DRIVEN}	Peak sink gate current (high-side and low-side)	IDRIVE tied to AGND		30		mA
		IDRIVE 18 kΩ (±5%) to AGND		90		
		IDRIVE 75 kΩ (±5%) to AGND		120		
		IDRIVE Hi-Z (> 500 kΩ to AGND)		180		
		IDRIVE 75 kΩ (±5%) to DVDD		210		
		IDRIVE 18 kΩ (±5%) to DVDD		270		
		IDRIVE tied to DVDD		300		

Electrical Characteristics (continued)

at V_{VM} = 6 to 38 V over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{HOLD}	FET holding current	Source current after t_{DRIVE}		15		mA
		Sink current after t_{DRIVE}		30		
I_{STRONG}	FET hold-off strong pulldown	GHX and GLX		300		mA
R_{OFF}	FET gate hold-off resistor	GHX to SHX and GLX to PGND		150		kΩ
t_{PD}	Propagation delay	PWM transition to GHX/GLX transition		180	250	ns
HALL SENSOR INPUTS (HPX, HNX)						
V_{HYS}	Hall comparator hysteresis voltage		20	30	40	mV
ΔV_{HYS}	Hall comparator hysteresis difference	Between A, B and C	-5		5	mV
V_{ID}	Hall comparator input differential		50			mV
V_{CM}	Hall comparator input common mode voltage CM range		1.5		3.5	V
I_I	Input leakage current	HPX = HNX = 0 V	–1		1	µA
t_{HDEG}	Hall deglitch time			5		µs
CYCLE-BY-CYCLE CURRENT LIMIT (ISEN)						
V_{LIMIT}	Voltage limit across R_{SENSE} for the current limiter		0.225	0.25	0.275	V
t_{BLANK}	Time that V_{LIMIT} is ignored from the start of the PWM cycle			5		µs
PROTECTION CIRCUITS						
V_{UVLO}	VM undervoltage lockout	VM falling, UVLO report	5.4		5.8	V
		VM rising, UVLO recovery	5.6		6	
V_{UVLO_HYS}	VM undervoltage hysteresis	Rising to falling threshold		200		mV
t_{UVLO_DEG}	VM undervoltage deglitch time	VM falling, UVLO report		10		µs
V_{CPUV}	Charge pump undervoltage	With respect to VM		2.4		V
V_{GS_CLAMP}	Gate drive clamping voltage	Positive clamping voltage	10.5		15	V
		Negative clamping voltage		–0.6		
V_{DS_OCP}	V_{DS} overcurrent trip voltage	VDS tied to AGND		0.15		V
		VDS 18 kΩ (±5%) to AGND		0.24		
		VDS 75 kΩ (±5%) to AGND		0.4		
		VDS Hi-Z (> 500 kΩ to AGND)		0.6		
		VDS 75 kΩ (±5%) to DVDD		0.9		
		VDS 18 kΩ (±5%) to DVDD		1.8		
		VDS tied to DVDD		Disabled		
V_{SEN_OCP}	V_{SENSE} overcurrent trip voltage		1.7	1.8	1.9	V
t_{OCP_DEG}	V_{DS} and V_{SENSE} overcurrent deglitch time			4.5		µs
t_{RETRY}	Overcurrent retry time			4		ms
T_{OTSD}	Thermal shutdown temperature	Die temperature T_j	150	170		°C
T_{HYS}	Thermal hysteresis	Die temperature T_j		20		°C

7.6 Typical Characteristics

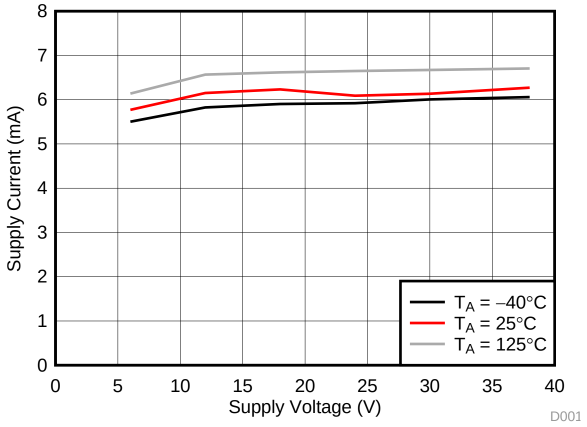


図 1. Supply Current Over Supply Voltage

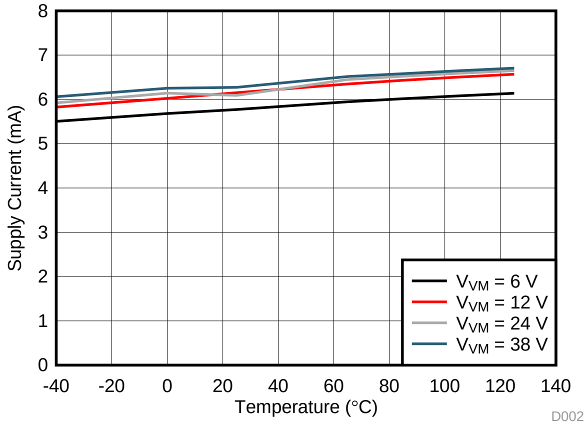


図 2. Supply Current Over Temperature

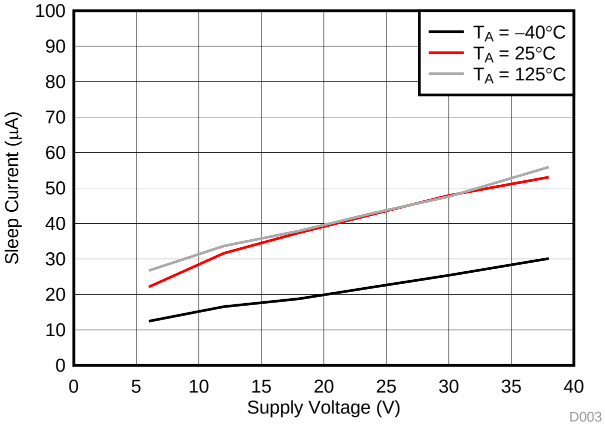


図 3. Sleep Current Over Supply Voltage

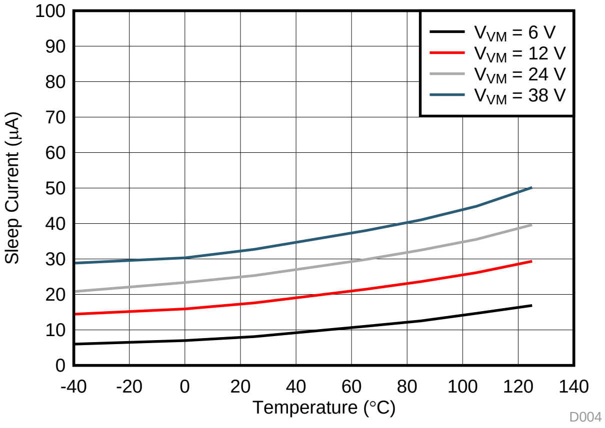
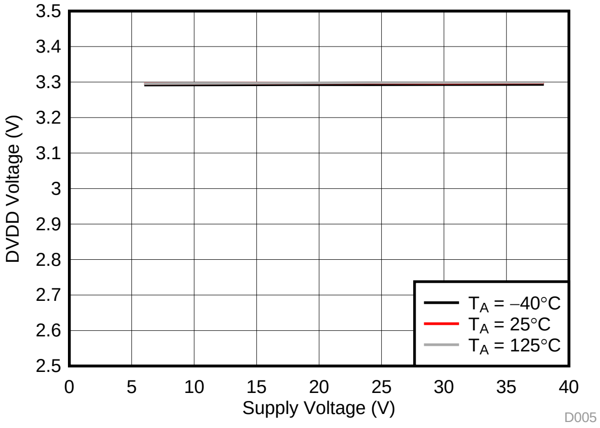
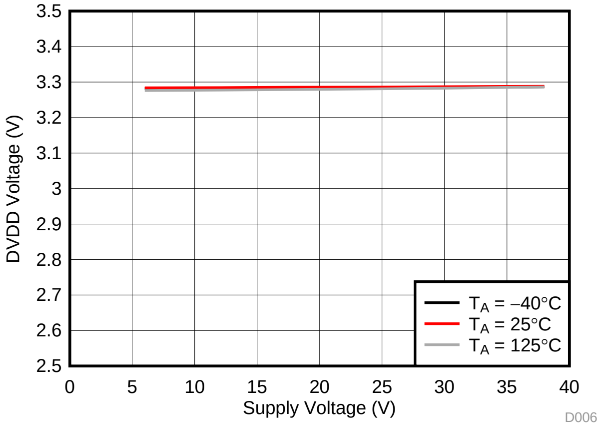


図 4. Sleep Current Over Temperature



I_{DVDD} = 0 mA

図 5. DVDD Voltage Over Supply Voltage



I_{DVDD} = 30 mA

図 6. DVDD Voltage Over Supply Voltage

Typical Characteristics (continued)

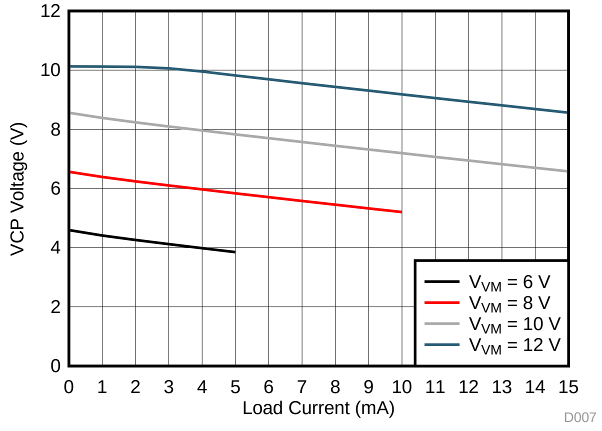


図 7. VCP Voltage Over Load

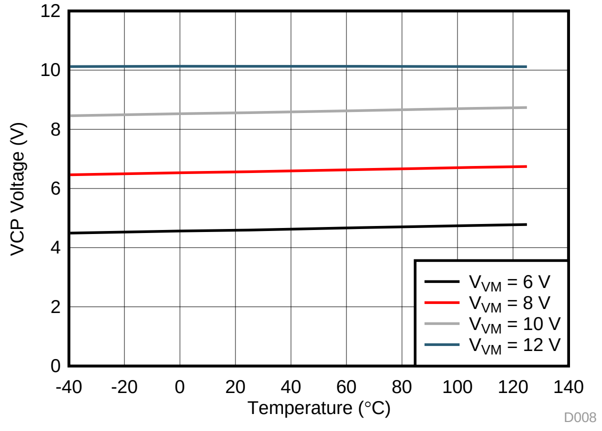


図 8. VCP Voltage Over Temperature

8 Detailed Description

8.1 Overview

The DRV8306 device is an integrated 6-V to 38-V gate driver for three-phase motor-drive applications. The device reduces system component count, cost, and complexity by integrating three independent half-bridge gate drivers, charge pump, and linear low-dropout (LDO) regulator for the high-side and low-side gate-driver supply voltages. A hardware interface (H/W) option allows for configuring the most commonly used settings through fixed external resistors.

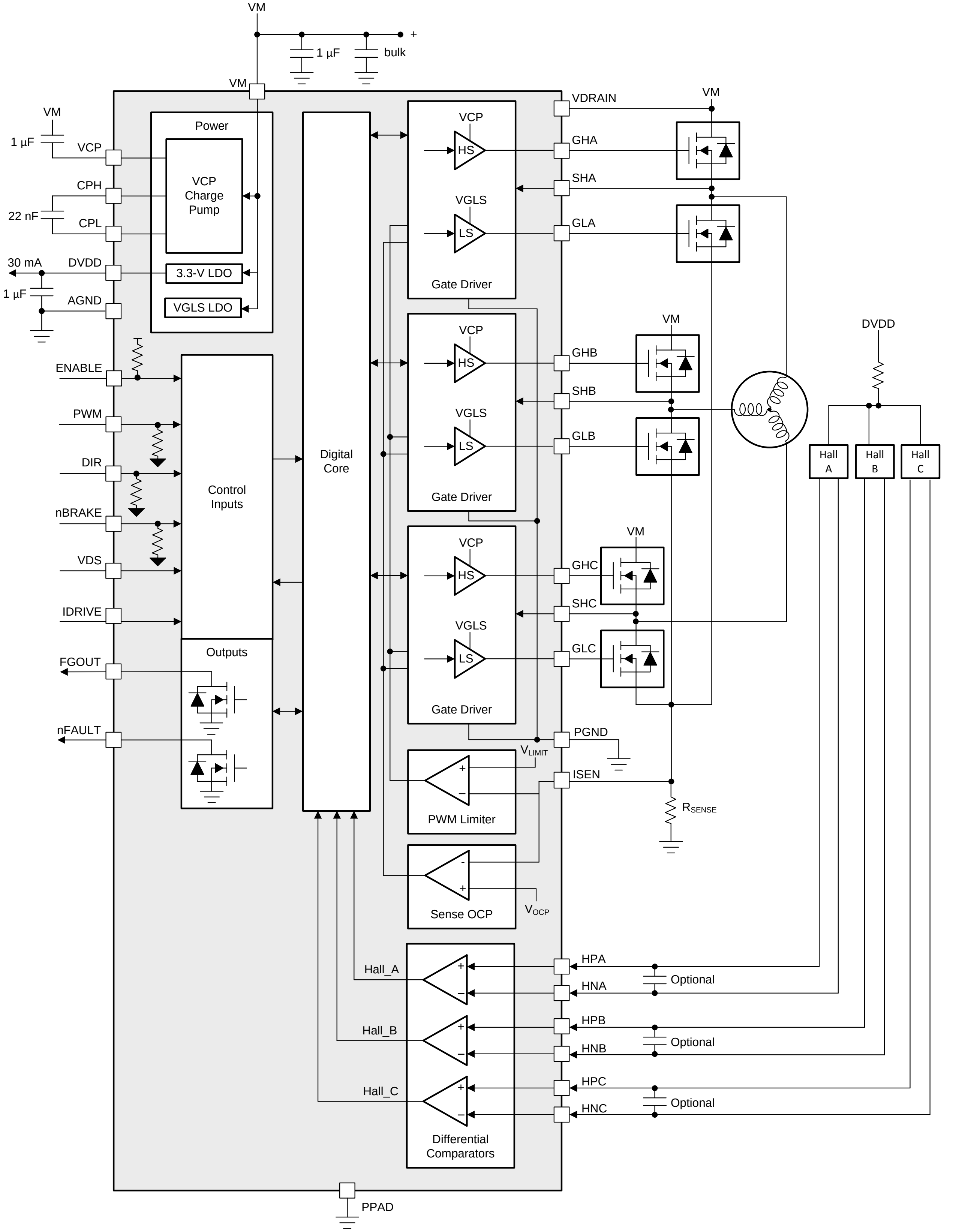
The gate drivers support external N-channel high-side and low-side power MOSFETs and can drive up to 150-mA source and 300-mA sink peak currents with a 15-mA average output current. The high-side gate drive supply voltage is generated using a doubler charge-pump architecture that regulates the VCP output to V_{VM} + 10 V. The low-side gate drive supply voltage is generated using a linear regulator from the VM power supply that regulates to 10 V. A smart gate-drive architecture provides the ability to adjust the output gate-drive current strength allowing for the gate driver to control the power MOSFET V_{DS} switching speed. This allows for the removal of external gate drive resistors and diodes reducing BOM component count, cost, and PCB area. The architecture also uses an internal state machine to protect against gate-drive short-circuit events, control the half-bridge dead time, and protect against dV/dt parasitic turnon of the external power MOSFET.

The DRV8306 device also integrates three Hall comparators for rotor position sensing using the Hall elements. This input is used for electronically commutating the BLDC motor in trapezoidal mode. This device also has a 3.3-V LDO regulator which can be powered up to loads up to 30 mA.

In addition to the high level of device integration, the DRV8306 device provides a wide range of integrated protection features. These features include power-supply undervoltage lockout (UVLO), charge-pump undervoltage lockout (CPUV), V_{DS} and V_{SENSE} overcurrent monitoring (OCP), gate-driver short-circuit detection (GDF), and overtemperature shutdown (OTSD). Fault events are indicated by the nFAULT pin.

The DRV8306 device is available in a 0.4-mm pin pitch, VQFN surface-mount package. The VQFN package size is 4-mm × 4-mm.

8.2 Functional Block Diagram



8.3 Feature Description

表 1 lists the recommended values of the external components for the gate driver.

表 1. DRV8306 Gate-Driver External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	X5R or X7R, 0.1-µF, VM-rated capacitor
C_{VM2}	VM	PGND	≥ 10-µF, VM-rated capacitor
C_{VCP}	VCP	VM	X5R or X7R, 16-V, 1-µF capacitor
C_{SW}	CPH	CPL	X5R or X7R, VM-rated capacitor, 22-nF capacitor
C_{DVDD}	DVDD	AGND	X5R or X7R, 1-µF, 6.3-V capacitor
R_{nFAULT}	VCC(1)	nFAULT	Pullup resistor
R_{PWM}	PWM	AGND or DVDD	DRV8306 hardware interface
R_{BRK}	nBRAKE	AGND or DVDD	DRV8306 hardware interface
R_{DIR}	DIR	AGND or DVDD	DRV8306 hardware interface
R_{IDRIVE}	IDRIVE	AGND or DVDD	DRV8306 hardware interface
R_{VDS}	VDS	AGND or DVDD	DRV8306 hardware interface

(1) The VCC pin is not a pin on the DRV8306 device, but a VCC supply-voltage pullup is required for the open-drain output nFAULT and SDO. These pins can also be pulled up to DVDD.

8.3.1 Three Phase Smart Gate Drivers

The DRV8306 device integrates three, half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. A doubler charge pump provides the proper gate bias voltage to the high-side MOSFET across a wide operating voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs.

The DRV8306 device implements a smart gate-drive architecture which lets the user dynamically adjust the gate drive current (through the IDRIVE pin) without requiring external gate current limiting resistors. Additionally, this architecture provides a variety of protection features for the external MOSFETs including automatic dead-time insertion, parasitic dV/dt gate turnon prevention, and gate-fault detection.

8.3.1.1 PWM Control Mode (1x PWM Mode)

The DRV8306 device provides a 1x PWM control mode for driving the BLDC motor into trapezoidal current-control mode. The DRV8306 device uses 6-step block commutation tables that are stored internally. This feature lets a three-phase BLDC motor be controlled using a single PWM sourced from a simple controller. The PWM is applied on the PWM pin and determines the output frequency and duty cycle of the half-bridges.

The half-bridge output states are managed by the HPA, HNA, HPB, HNB, HPC and HNC pins which are used as state logic inputs. The state inputs are the position feedback of the BLDC motor. The device always operates with synchronous rectification.

The DIR pin controls the direction of BLDC motor in either clockwise or counter-clockwise direction. Tie the DIR pin low if this feature is not required.

The nBRAKE input halts the motor by turning off all high-side MOSFETs and turning on all low-side MOSFETs when it is pulled low. This brake is independent of the states of the other input pins. Tie the nBRAKE pin high if this feature is not required.

表 2. Synchronous 1x PWM Mode

STATE	HALL INPUTS						GATE-DRIVE OUTPUTS						DESCRIPTION
	DIR = 0			DIR = 1			PHASE A		PHASE B		PHASE C		
	HALL_A	HALL_B	HALL_C	HALL_A	HALL_B	HALL_C	GHA	GLA	GHB	GLB	GHC	GLC	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	!PWM	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	!PWM	L	H	B → C
2	1	0	0	0	1	1	PWM	!PWM	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	!PWM	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	!PWM	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	!PWM	C → A
6	0	1	0	1	0	1	L	H	PWM	!PWM	L	L	B → A

図 9 shows the configuration in 1x PWM mode.

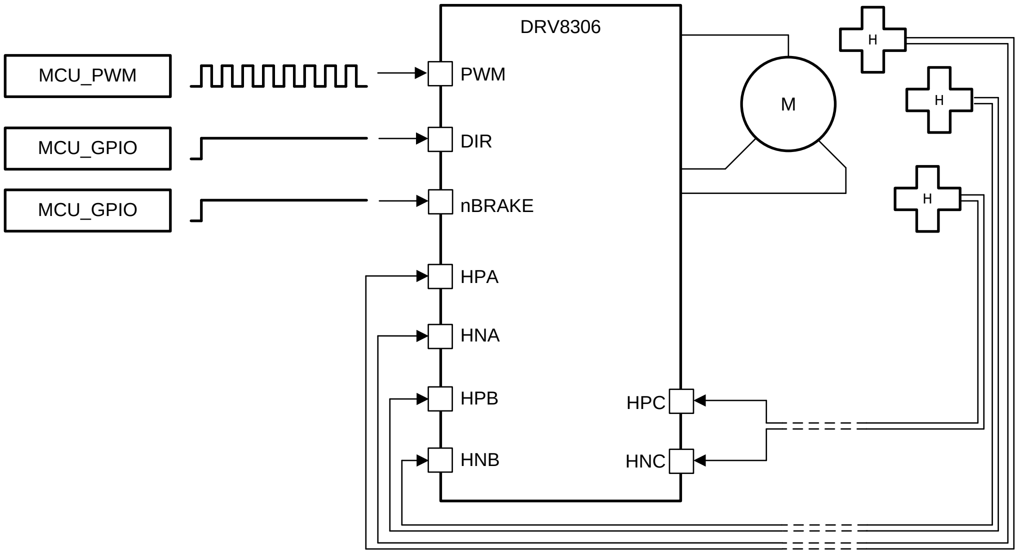


図 9. 1x PWM Mode

8.3.1.2 Hardware Interface Mode

The DRV8306 device supports a hardware interface mode for simple end-application design. In this hardware interface device, the V_{DS} overcurrent limit and the gate drive current levels can be configured through the resistor-configurable inputs, IDRIVE and VDS. This feature lets the application designer configure the most commonly used device settings by tying the pin logic high or logic low, or with a simple pullup or pulldown resistor.

The IDRIVE pin configures the gate drive current strength. The VDS pin configures the voltage threshold of the V_{DS} overcurrent monitors.

For more information on the hardware interface, see the *Pin Diagrams* section.

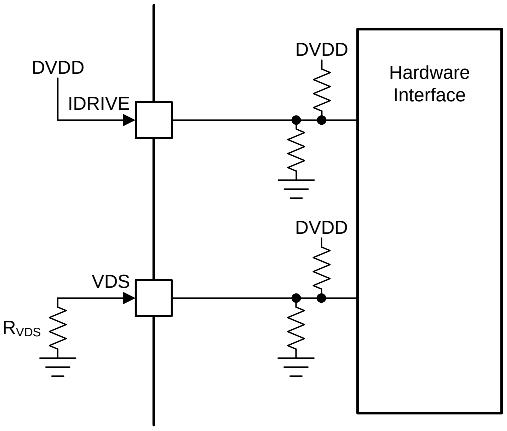


図 10. Sample Configuration of Hardware Interface

8.3.1.3 Gate Driver Voltage Supplies

The high-side gate-drive voltage supply is created using a doubler charge pump that operates from the VM voltage supply input. The charge pump lets the gate driver correctly bias the high-side MOSFET gate with respect to its source across a wide input supply voltage range. The charge pump is regulated to maintain a fixed output voltage of V_{VM} + 10 V and supports an average output current of 15 mA. When the V_{VM} voltage is less than 12 V, the charge pump operates in full doubler mode and generates $V_{VCP} = 2 \times V_{VM} - 1.5$ V when unloaded. The charge pump is continuously monitored for undervoltage to prevent under-driven MOSFET conditions. The charge pump requires a X5R or X7R, 1-µF, 16-V ceramic capacitor between the VM and VCP pins to act as the storage capacitor. Additionally, a X5R or X7R, 22-nF, VM-rated ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

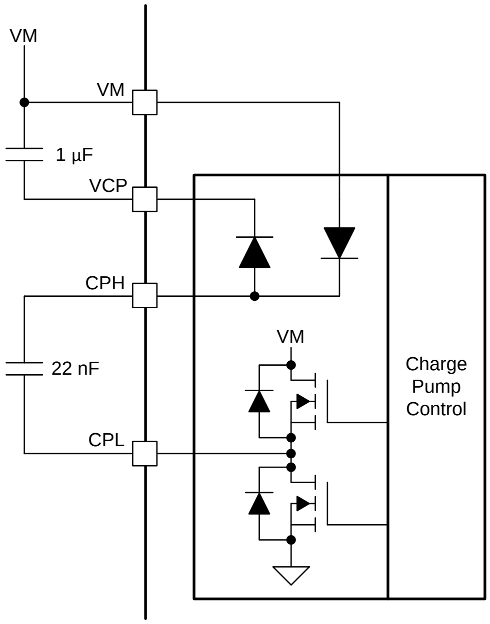


図 11. Charge Pump Architecture

The low-side gate drive voltage is created using a linear low-dropout (LDO) regulator that operates from the VM voltage supply input. The LDO regulator allows the gate driver to properly bias the low-side MOSFET gate with respect to ground. The LDO regulator output is fixed at 10 V and supports an output current of 15 mA. The LDO regulator is monitored for undervoltage to prevent under-driven MOSFET conditions.

8.3.1.4 Smart Gate Drive Architecture

The DRV8306 gate drivers use an adjustable, complimentary, push-pull topology for both the high-side and low-side drivers. This topology allows for both a strong pullup and pulldown of the external MOSFET gates.

Additionally, the gate drivers use a smart gate-drive architecture to provide additional control of the external power MOSFETs, take additional steps to protect the MOSFETs, and allow for optimal tradeoffs between efficiency and robustness. This architecture is implemented through two components called IDRIVE and TDRIVE which are detailed in the *IDRIVE: MOSFET Slew-Rate Control* section and *TDRIVE: MOSFET Gate Drive Control* section. 図 12 shows the high-level functional block diagram of the gate driver.

The IDRIVE gate-drive current and TDRIVE gate-drive time should be initially selected based on the parameters of the external power MOSFET used in the system and the desired rise and fall times (see the *Application and Implementation* section).

The high-side gate driver also implements a Zener clamp diode to help protect the external MOSFET gate from overvoltage conditions in the case of external short-circuit events on the MOSFET.

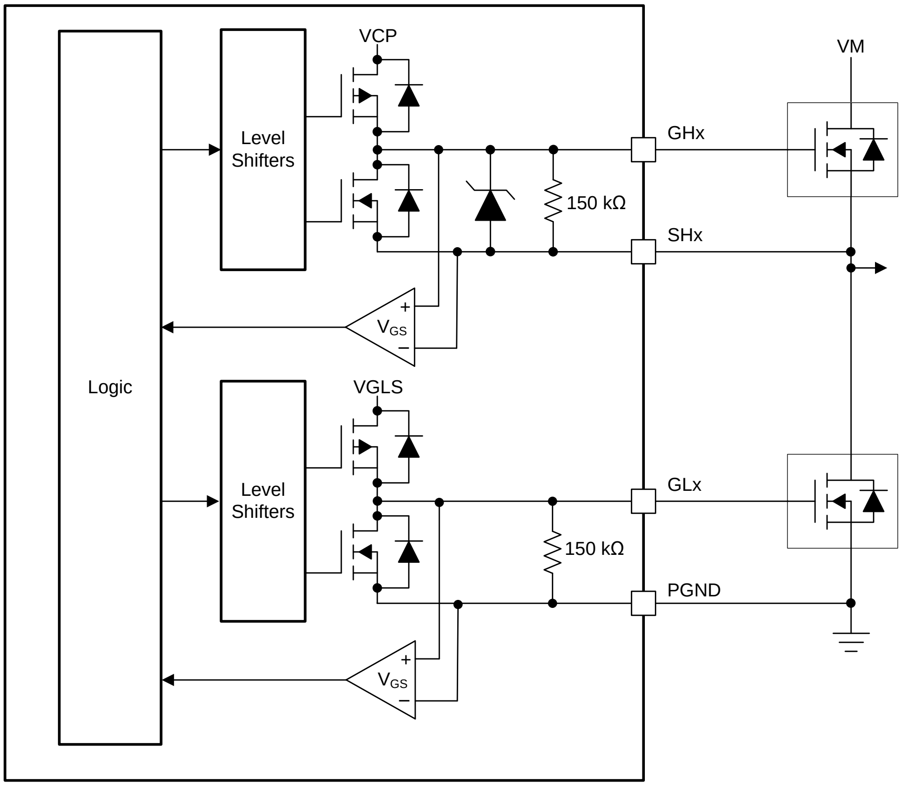


図 12. Gate Driver Block Diagram

8.3.1.4.1 IDRIVE: MOSFET Slew-Rate Control

The IDRIVE component implements adjustable gate-drive current to control the MOSFET V_{DS} slew rates. The MOSFET V_{DS} slew rates are a critical factor for optimizing radiated emissions, energy and duration of diode recovery spikes, dV/dt gate turnon leading to shoot-through, and switching voltage transients related to parasitics in the external half-bridge. The IDRIVE component operates on the principal that the MOSFET V_{DS} slew rates are predominately determined by the rate of gate charge (or gate current) delivered during the MOSFET Q_{GD} or Miller charging region. By allowing the gate driver to adjust the gate current, it can effectively control the slew rate of the external power MOSFETs.

The IDRIVE component allows the DRV8306 device to dynamically switch between gate drive currents through an IDRIVE pin. This hardware interface devices provides seven I_{DRIVE} settings from 15-mA to 150-mA (source) and 30-mA to 300-mA (sink). The gate drive current setting is delivered to the gate during the turnon and turnoff of the external power MOSFET for the t_{DRIVE} duration. After the MOSFET turnon or turnoff, the gate driver switches to a smaller hold current (I_{HOLD}) to improve the gate driver efficiency. Additional details on the IDRIVE settings are described in the *Pin Diagrams* section.

8.3.1.4.2 TDRIVE: MOSFET Gate Drive Control

The TDRIVE component is an integrated gate-drive state machine that provides automatic dead time insertion through switching handshaking, parasitic dV/dt gate turnon prevention, and MOSFET gate-fault detection.

The first component of the TDRIVE state machine is automatic dead-time insertion. Dead time is period of time between the switching of the external high-side and low-side MOSFETs to ensure that they do not cross conduct and cause shoot-through. The DRV8306 device uses V_{GS} voltage monitors to measure the MOSFET gate-to-source voltage and determine the proper time to switch instead of relying on a fixed time value. This feature allows the gate-driver dead time to adjust for variation in the system such as temperature drift and variation in the MOSFET parameters. An additional digital dead time (t_{DEAD}) is inserted on top of the gate-driver dead time and is fixed for the DRV8306 device.

The second component focuses on prevention of parasitic dV/dt gate turnon. To implement this feature, the TDRIVE state machine enables a strong pulldown current (I_{STRONG}) on the opposite MOSFET gate whenever a MOSFET is switching. The strong pulldown last for the TDRIVE duration. This feature helps remove parasitic charge that couples into the MOSFET gate when the half-bridge switch-node voltage slews rapidly.

The third component implements a gate-fault detection scheme to detect pin-to-pin solder defects, a MOSFET gate failure, or a MOSFET gate stuck-high or stuck-low voltage condition. This implementation is done with a pair of V_{GS} gate-to-source voltage monitors for each half-bridge gate driver. When the gate driver receives a command to change the state of the half-bridge it begins to monitor the gate voltage of the external MOSFET. If the V_{GS} voltage has not reached the proper threshold at the end of the t_{DRIVE} period, the gate driver reports a fault. To ensure that a false fault is not detected, the user must ensure that the t_{DRIVE} time is longer than the time required to charge or discharge the MOSFET gate (this setting can be configured indirectly using the IDRIVE pin). The t_{DRIVE} time does not increase the PWM time and will terminate if another PWM command is received while active. Additional details on the TDRIVE settings are described in the *Pin Diagrams* section for hardware interface devices.

図 13 shows an example of the TDRIVE state machine in operation.

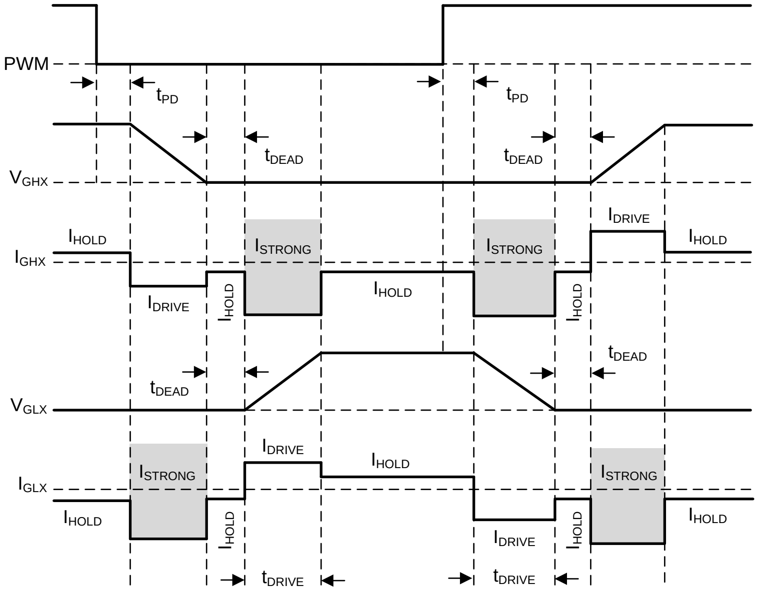


図 13. TDRIVE State Machine

8.3.1.4.3 Gate Drive Clamp

A clamping structure limits the gate drive output voltage to the $V_{GS,CLAMP}$ voltage to help protect the external high-side MOSFETs from gate overvoltage damage. The positive voltage clamp is realized using a series of diodes. The negative voltage clamp uses the body diodes of the internal pulldown gate driver as shown in 図 14.

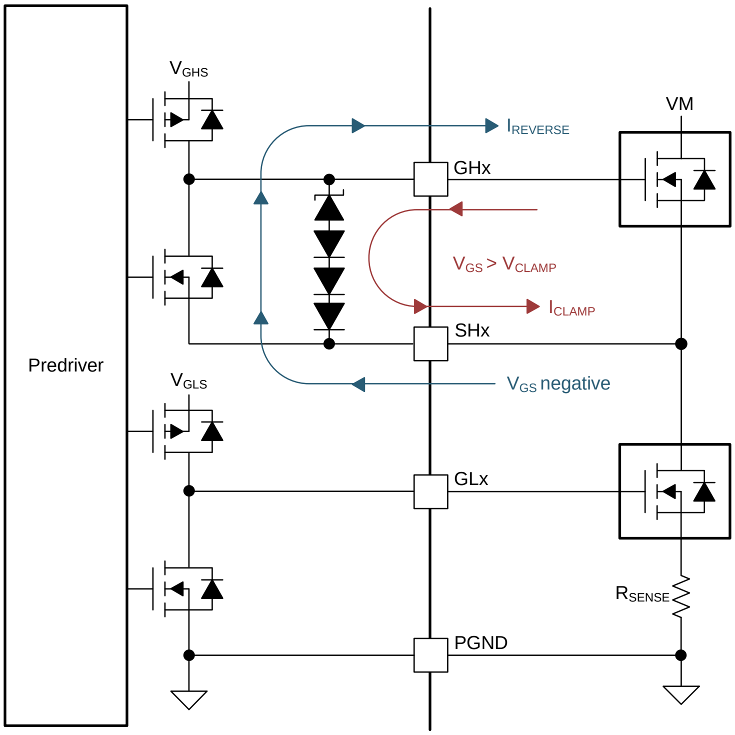


図 14. Gate Drive Clamp

8.3.1.4.4 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an PWM logic edge detected to the GHX / GLX transition as shown in 図 13. This time comprises three parts consisting of the digital input deglitcher delay, the digital propagation delay, and the delay through the analog gate drivers.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. To support multiple control modes and dead time insertion, a small digital delay is added as the input command propagates through the device. Lastly, the analog gate drivers have a small delay that contributes to the overall propagation delay of the device.

In order for the output to change state during normal operation, one MOSFET must first be turned off. The MOSFET gate is ramped down according to the IDRIVE setting, and the observed propagation delay ends when the MOSFET gate falls below the threshold voltage.

8.3.1.4.5 MOSFET V_{DS} Monitors

The gate drivers implement adjustable V_{DS} voltage monitors to detect overcurrent or short-circuit conditions on the external power MOSFETs. When the monitored voltage is greater than the V_{DS} trip point (V_{VDS_OCP}) for longer than the deglitch time (t_{OCP}), an overcurrent condition is detected and the driver enters into the V_{DS} automatic-retry mode.

The high-side V_{DS} monitors measure the voltage between the VDRAIN and SHx pins and the low side V_{DS} monitors measure the voltage between the SHx and ISEN pins. The V_{VDS_OCP} threshold is programmable from 0.15 V to 1.8 V. Additional information on the V_{DS} monitor levels are described in the *Pin Diagrams* section.

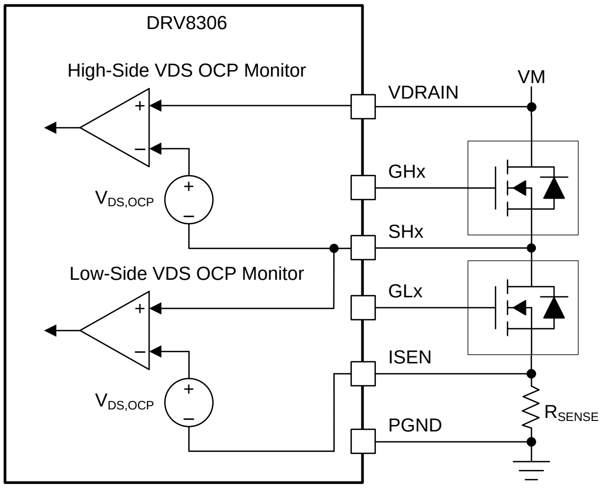


図 15. DRV8306 V_{DS} Monitors

8.3.1.4.6 VDRAIN Sense Pin

The DRV8306 device provides a separate sense pin for the common point of the high-side MOSFET drain. This pin is called VDRAIN. This pin allows the sense line for the overcurrent monitors (VDRAIN) and the power supply (VM) to remain separate and prevent noise on the VDRAIN sense line. This separation also allows for a small filter to be implemented on the gate driver supply (VM) or to insert a boost converter to support lower voltage operation if desired. Care must still be taken when the filter or separate supply is designed because VM is still the reference point for the VCP charge pump that supplies the high-side gate drive voltage (V_{GSH}). The VM supply must not drift too far from the VDRAIN supply to avoid violating the V_{GS} voltage specification of the external power MOSFETs.

8.3.2 DVDD Linear Voltage Regulator

A 3.3-V, 30-mA linear regulator is integrated into the DRV8306 device and is available for use by external circuitry. This regulator can provide the supply voltage for a low-power microcontroller or other low-current supporting circuitry. The output of the DVDD regulator should be bypassed near the DVDD pin with a X5R or X7R, 1-µF, 6.3-V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The DVDD nominal, no-load output voltage is 3.3 V. When the DVDD load current exceeds 30 mA, the regulator functions like a constant-current source. The output voltage drops significantly with a current load greater than 30 mA.

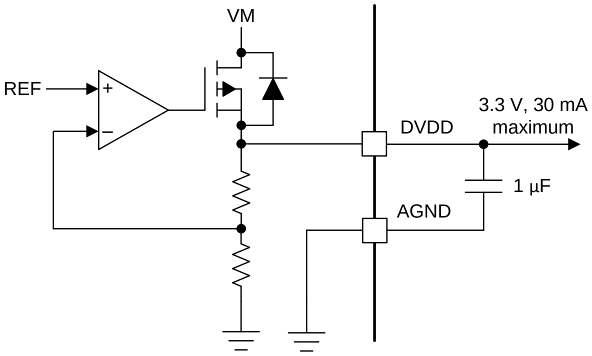


図 16. DVDD Linear Regulator Block Diagram

Use 式 1 to calculate the power dissipated in the device because of the DVDD linear regulator.

$$P = \left(V_{VM} - V_{DVDD}\right) \times I_{DVDD} \quad (1)$$

For example, at V_{VM} = 24 V, drawing 20 mA out of DVDD results in a power dissipation as shown in 式 2.

$$P = \left(24\ \text{V} - 3.3\ \text{V}\right) \times 20\ \text{mA} = 414\ \text{mW} \tag{2}$$

8.3.3 Pulse-by-Pulse Current Limit

The current-limit circuit activates if the voltage detected across the low-side sense resistor (ISEN pin) exceeds the V_{LIMIT} voltage. This feature restricts motor current to less than the V_{LIMIT} voltage divided by the R_{SENSE} resistance.

注

The current-limit circuit is ignored immediately after the PWM signal goes active for a short blanking time to prevent false trips of the current-limit circuit.

If the current limit activates, the high-side FET is disabled until the beginning of the next PWM cycle. Because the synchronous rectification is always enabled, when the current limit activates, the low-side FET is activated while the high-side FET is disabled.

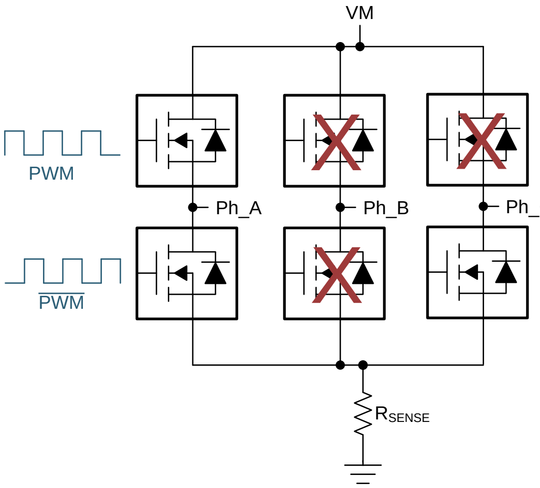


図 17. Bridge Operation in Normal Mode (Current Limit Not Active)

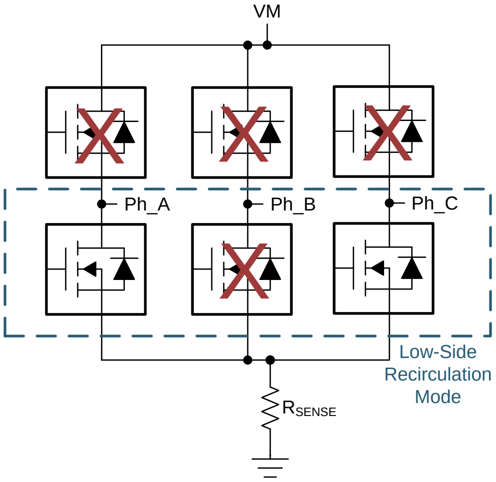


図 18. Bridge Operation in Current Limit Mode (Current Limit Active)

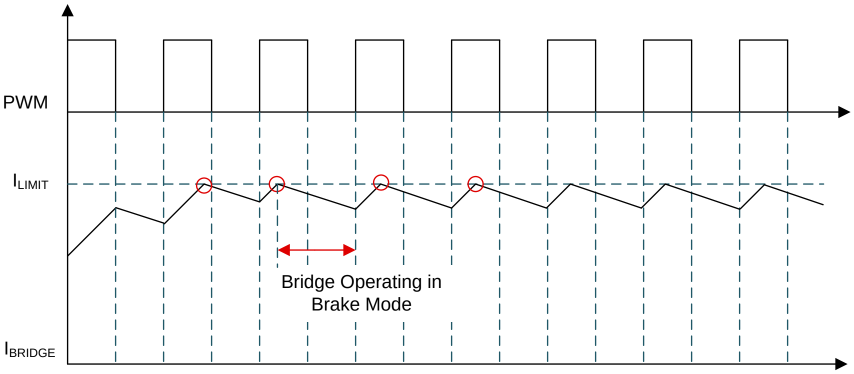


図 19. Pulse-by-Pulse Current-Limit Operation

8.3.4 Hall Comparators

Three comparators are provided to process the raw signals from the Hall effect transducers to commutate the motor. The Hall comparators sense zero crossings of the differential inputs and pass the information to digital logic. The Hall comparators have hysteresis, and their detect threshold is centered at 0. The hysteresis is defined as shown in 図 20.

In addition to the hysteresis, the Hall inputs are deglitched with a circuit that ignores any extra Hall transitions for a period of t_{HDEG} after sensing a valid transition. Ignoring these transitions for the t_{HDEG} time prevents PWM noise from being coupled into the Hall inputs, which can result in erroneous commutation.

If excessive noise is still coupled into the Hall comparator inputs, adding capacitors between the positive and negative inputs of the Hall comparators may be required. The ESD protection circuitry on the Hall inputs implements a diode to the DVDD pin. Because of this diode, the voltage on the Hall inputs should not exceed the DVDD voltage.

Because the DVDD pin is disabled in standby mode (ENABLE inactive), the Hall inputs should not be driven by external voltages in standby mode. If the Hall sensors are powered externally, the supply to the Hall sensors should be disabled if the DRV8306 device is put into standby mode. In addition, the Hall sensor power supply should be powered up after enabling the motor otherwise an invalid Hall state may cause a delay in motor operation.

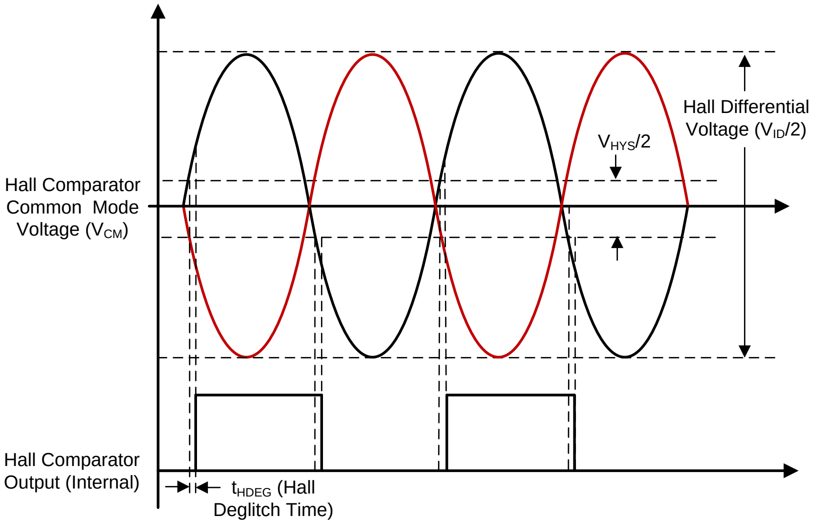


図 20. Hall Comparators

8.3.5 FGOUT Signal

The DRV8306 device also has an open-drain FGOUT signal that can be used for the closed-loop speed control of BLDC motor. This signal includes the information of all three Hall-elements inputs as shown in 図 21.

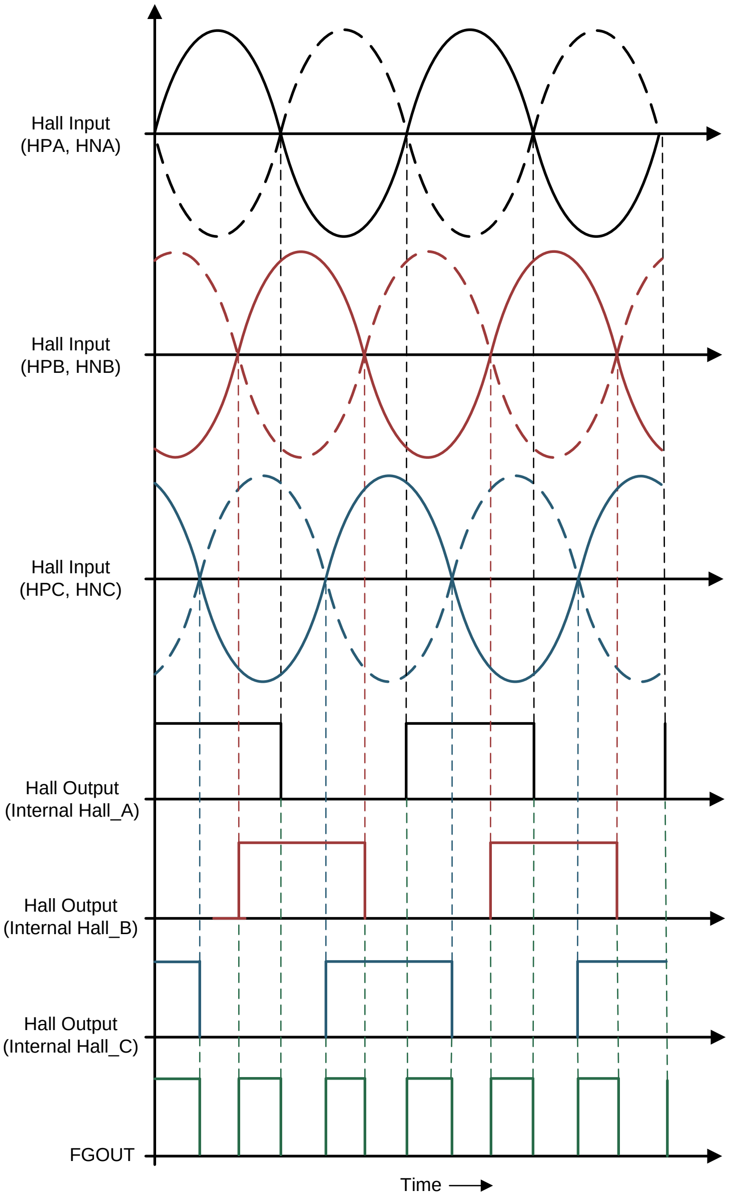
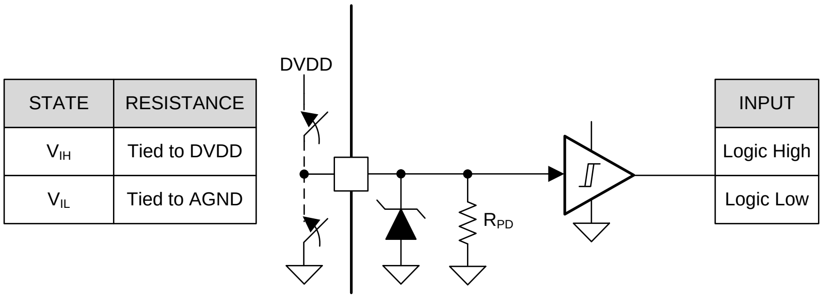


図 21. FGOUT Signal

8.3.6 Pin Diagrams

図 22 shows the input structure for the logic-level pins, PWM, DIR and nBRAKE. The input can be driven with a voltage or external resistor.

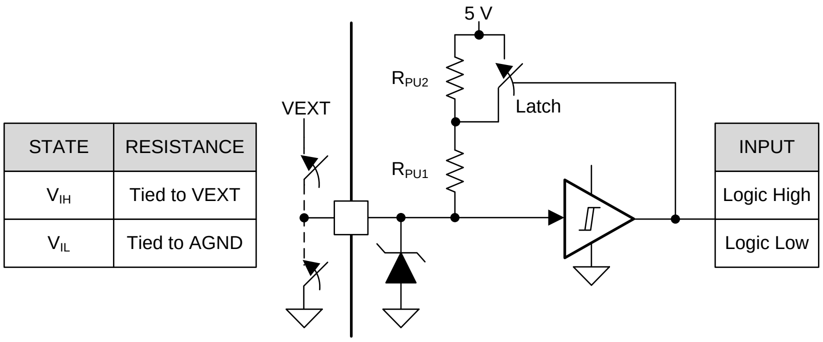


STATE	RESISTANCE
V_{IH}	Tied to DVDD
V_{IL}	Tied to AGND

INPUT
Logic High
Logic Low

図 22. Logic-Level Input Pin Structure (PWM, DIR, and nBRAKE)

図 23 shows the input structure for the logic-level pin, ENABLE pin. The input can be driven with a voltage or external resistor. The VEXT represents the external voltage.

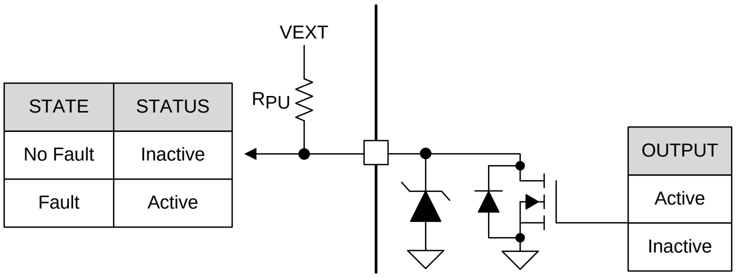


STATE	RESISTANCE
V_{IH}	Tied to VEXT
V_{IL}	Tied to AGND

INPUT
Logic High
Logic Low

図 23. Logic-Level Input Pin Structure (ENABLE)

図 24 shows the structure of the open-drain output pin, nFAULT. The open-drain output requires an external pullup resistor to function properly.

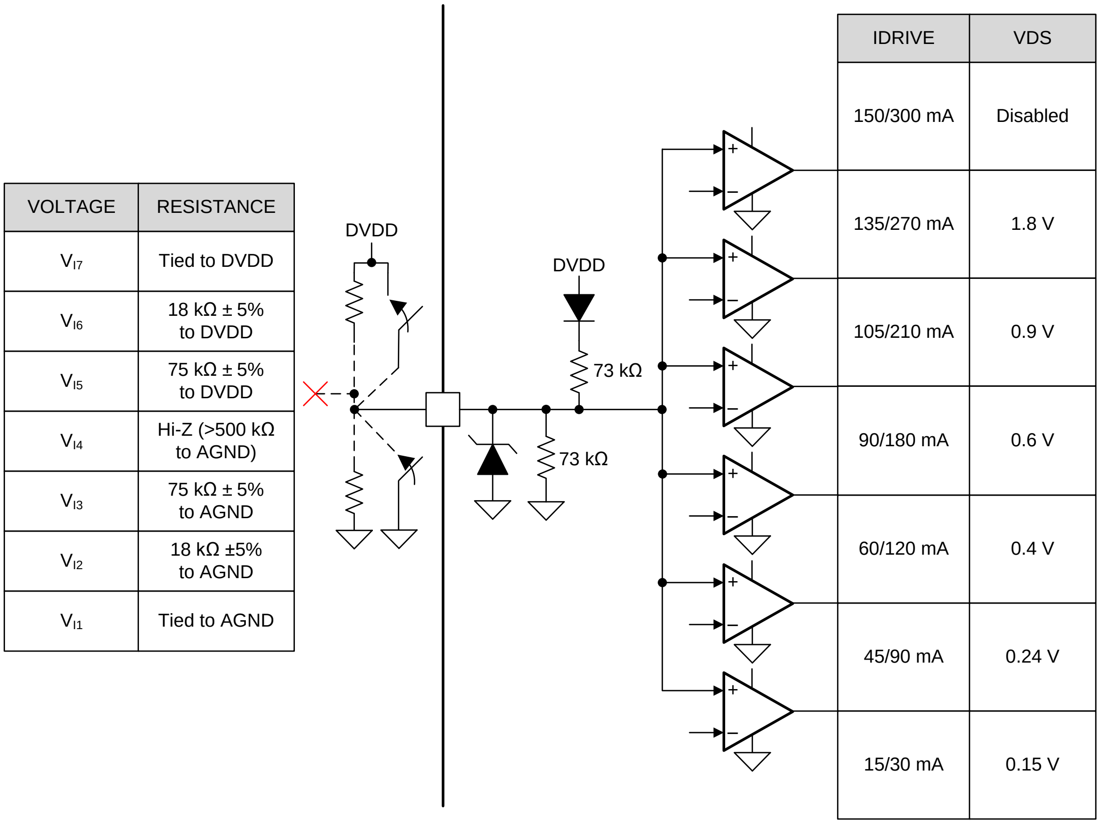


STATE	STATUS
No Fault	Inactive
Fault	Active

OUTPUT
Active
Inactive

図 24. Open-Drain Output Pin Structure

図 25 shows the structure of the seven level input pins, IDRIVE and VDS. The input can be set with an external resistor.



VOLTAGE	RESISTANCE
V_{I7}	Tied to DVDD
V_{I6}	18 kΩ ± 5% to DVDD
V_{I5}	75 kΩ ± 5% to DVDD
V_{I4}	Hi-Z (>500 kΩ to AGND)
V_{I3}	75 kΩ ± 5% to AGND
V_{I2}	18 kΩ ±5% to AGND
V_{I1}	Tied to AGND

IDRIVE	VDS
150/300 mA	Disabled
135/270 mA	1.8 V
105/210 mA	0.9 V
90/180 mA	0.6 V
60/120 mA	0.4 V
45/90 mA	0.24 V
15/30 mA	0.15 V

図 25. Seven Level Input Pin Structure

8.3.7 Gate-Driver Protective Circuits

The DRV8306 device is fully protected against VM undervoltage, charge pump undervoltage, MOSFET V_{DS} overcurrent, gate driver shorts, and overtemperature events.

表 3. Fault Action and Response

FAULT	CONDITION	REPORT	GATE DRIVER	LOGIC	RECOVERY
VM undervoltage (UVLO)	$V_{VM} < V_{UVLO}$	nFAULT	Hi-Z	Disabled	Automatic: $V_{VM} > V_{UVLO}$
Charge pump undervoltage (CPUV)	$V_{VCP} < V_{CPUV}$	nFAULT	Hi-Z	Active	Automatic: $V_{VCP} > V_{CPUV}$
V_{DS} overcurrent (VDS_OCP)	$V_{DS} > V_{VDS\_OCP}$	nFAULT	Hi-Z	Active	Retry: t_{RETRY}
V_{SENSE} overcurrent (SEN_OCP)	$V_{SP} > V_{SEN\_OCP}$	nFAULT	Hi-Z	Active	Retry: t_{RETRY}
Gate driver fault (GDF)	Gate voltage stuck > t_{DRIVE}	nFAULT	Hi-Z	Active	Latched: ENABLE Pulse
Thermal shutdown (OTSD)	$T_J > T_{OTSD}$	nFAULT	Hi-Z	Active	Automatic: $T_J < T_{OTSD} – T_{HYS}$

8.3.7.1 VM Supply Undervoltage Lockout (UVLO)

If at any time the input supply voltage on the VM pin falls below the V_{UVLO} threshold, all of the external MOSFETs are disabled, the charge pump is disabled, and the nFAULT pin is driven low. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the VM undervoltage condition is removed.

8.3.7.2 VCP Charge-Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls below the V_{CPUV} threshold voltage of the charge pump, all of the external MOSFETs are disabled and the nFAULT pin is driven low. Normal operation resumes (gate-driver operation and the nFAULT pin is released) when the VCP undervoltage condition is removed.

8.3.7.3 MOSFET V_{DS} Overcurrent Protection (VDS_OCP)

A MOSFET overcurrent event is sensed by monitoring the V_{DS} voltage drop across the external MOSFET $R_{DS(on)}$. If the voltage across an enabled MOSFET exceeds the V_{VDS_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a VDS_OCP event is recognized. The V_{VDS_OCP} threshold is set with the VDS pin, the t_{OCP_DEG} is fixed at 4.5 µs, and the driver operates with fixed for 4-ms automatic retry in an OCP event, but can be disabled by tying the VDS pin to DVDD.

8.3.7.4 V_{SENSE} Overcurrent Protection (SEN_OCP)

Three-phase bridge overcurrent is also monitored by sensing the voltage drop across the external current-sense resistor with the ISEN pin. If at any time the voltage on the ISEN input of the current-sense amplifier exceeds the V_{SEN_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a SEN_OCP event is recognized. The $V_{SEN,OCP}$ threshold is fixed at 1.8 V, t_{OCP_DEG} is fixed at 4 µs, and, during the OCP event, the driver operates with fixed t_{RETRY} for 4-ms automatic retry.

8.3.7.5 Gate Driver Fault (GDF)

The GHx and GLx pins are monitored such that if the voltage on the external MOSFET gate does not increase or decrease after the t_{DRIVE} time, a gate driver fault is detected. This fault may be encountered if the GHx or GLx pins are shorted to the PGND, SHx, or VM pins. Additionally, a gate driver fault may be encountered if the selected I_{DRIVE} setting is not sufficient to turn on the external MOSFET within the t_{DRIVE} period. After a gate drive fault is detected, all external MOSFETs are disabled and the nFAULT pin is driven low. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the gate driver fault condition is removed.

Gate driver faults can indicate that the selected I_{DRIVE} or t_{DRIVE} settings are too low to slew the external MOSFET in the desired time. Increasing either the I_{DRIVE} or t_{DRIVE} setting can resolve gate driver faults in these cases. Alternatively, if a gate-to-source short occurs on the external MOSFET, a gate driver fault is reported because of the MOSFET gate not turning on.

8.3.7.6 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}), all the external MOSFETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the overtemperature condition is removed. This protection feature cannot be disabled.

8.4 Device Functional Modes

8.4.1 Gate Driver Functional Modes

8.4.1.1 Sleep Mode

The ENABLE pin manages the state of the DRV8306 device. When the ENABLE pin is low, the device goes to a low-power sleep mode. In sleep mode, all gate drivers are disabled, all external MOSFETs are disabled, the charge pump is disabled, and the DVDD regulator is disabled. The t_{SLEEP} time must elapse after a falling edge on the ENABLE pin before the device goes to the sleep mode. The device goes from the sleep mode automatically if the ENABLE pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

In sleep mode and when $V_{VM} < V_{UVLO}$, all external MOSFETs are disabled. The high-side gate pins, GHx, are pulled to the SHx pin by an internal resistor and the low-side gate pins, GLx, are pulled to the PGND pin by an internal resistor.

注

During power up and power down of the device through the ENABLE pin, the nFAULT pin is held low as the internal regulators are enabled or disabled. After the regulators have enabled or disabled, the nFAULT pin is automatically released. The duration that the nFAULT pin is low does not exceed the t_{SLEEP} or t_{WAKE} time.

8.4.1.2 Operating Mode

When the ENABLE pin is high or left floating and $V_{VM} > V_{UVLO}$, the device goes to the operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the charge pump, low-side gate regulator, and DVDD regulator are active. The hardware inputs (IDRIVE and VDS) are latched during the wake-up time (t_{WAKE}). Any further change to these pins is ignored unless a power-up cycle or an ENABLE pin transition after sleep mode occurs.

8.4.1.3 Fault Reset (ENABLE Reset Pulse)

In the case of device-latched faults, the DRV8306 device goes to driver Hi-Z state to help protect the external power MOSFETs and system.

When the fault condition is removed the device can go back to the operating state by issuing a result pulse to the ENABLE pin on either interface variant. The ENABLE reset pulse (t_{RST}) consists of a high-to-low-to-high transition on the ENABLE pin. The low period of the sequence should fall with the t_{RST} time window or else the device will begin the complete shutdown sequence. The reset pulse has no effect on any of the regulators, device settings, or other functional blocks

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8306 device is primarily used in three-phase brushless DC motor-control applications. The design procedures in the *Typical Application* section highlight how to use and configure the DRV8306 device.

9.1.1 Hall Sensor Configuration and Connection

The combinations of Hall sensor connections in this section are common connections.

9.1.1.1 Typical Configuration

The Hall sensor inputs on the DRV8306 device can interface with a variety of Hall sensors. Typically, a Hall element is used, which outputs a differential signal on the order of 100 mV. To use this type of sensor, the DVDD regulator can be used to power the Hall sensor. 図 26 shows the connections.

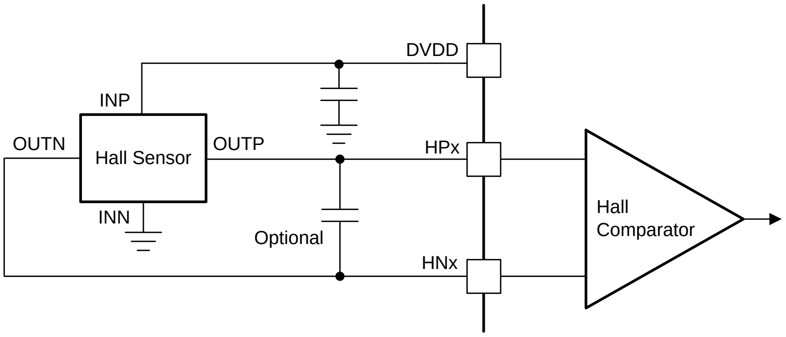


図 26. Typical Hall Sensor Configuration

Because the amplitude of the Hall-sensor output signal is very low, capacitors are often placed across the Hall inputs to help reject noise coupled from the motor. Capacitors with a value of 1 nF to 100 nF are typically used.

9.1.1.2 Open Drain Configuration

Some motors use digital Hall sensors with open-drain outputs. These sensors can also be used with the DRV8306 device, with the addition of a few resistors as shown in 図 27.

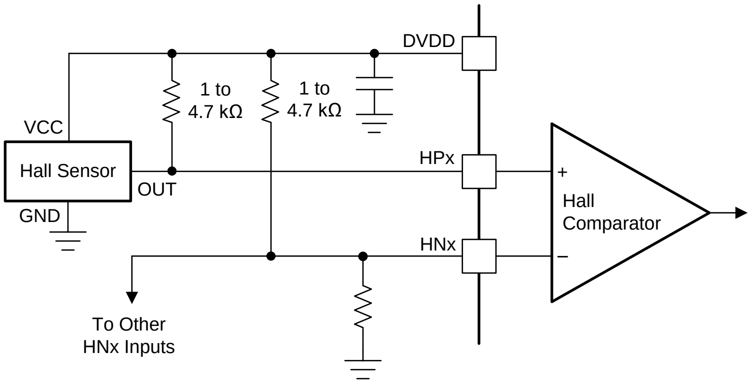


図 27. Open-Drain Hall Sensor Configuration

Application Information (continued)

The negative (HNx) inputs are biased to DVDD / 2 by a pair of resistors between the DVDD pin and ground. For open-collector Hall sensors, an additional pullup resistor to the VREG pin is required on the positive (HPx) input. Again, the DVDD output can usually be used to supply power to the Hall sensors.

9.1.1.3 Series Configuration

Hall elements are also connected in series or parallel depending upon the Hall sensor current/voltage requirement. 図 28 shows the series connection of Hall sensors powered via the DRV8306 internal LDO (DVDD). This configuration is used if the current requirement per Hall sensor is high (>10 mA)

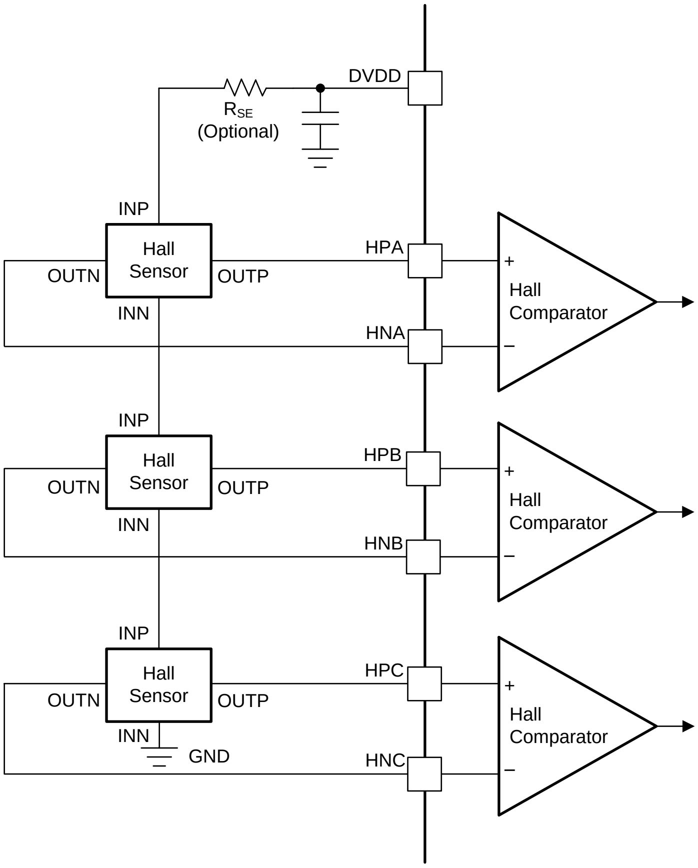


図 28. Hall Sensor Connected in Series Configuration

Application Information (continued)

9.1.1.4 Parallel Configuration

図 29 shows the parallel connection of Hall sensors which is powered by the DVDD. This configuration can be used if the current requirement per Hall sensor is low (<10 mA).

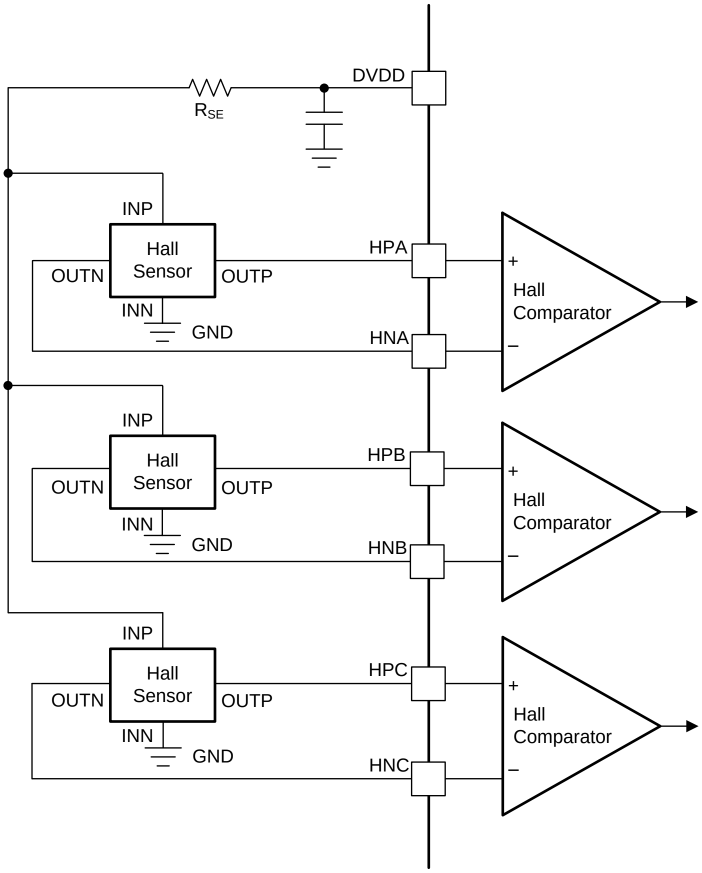


図 29. Hall Sensors Connected in Parallel Configuration

9.2 Typical Application

9.2.1 Primary Application

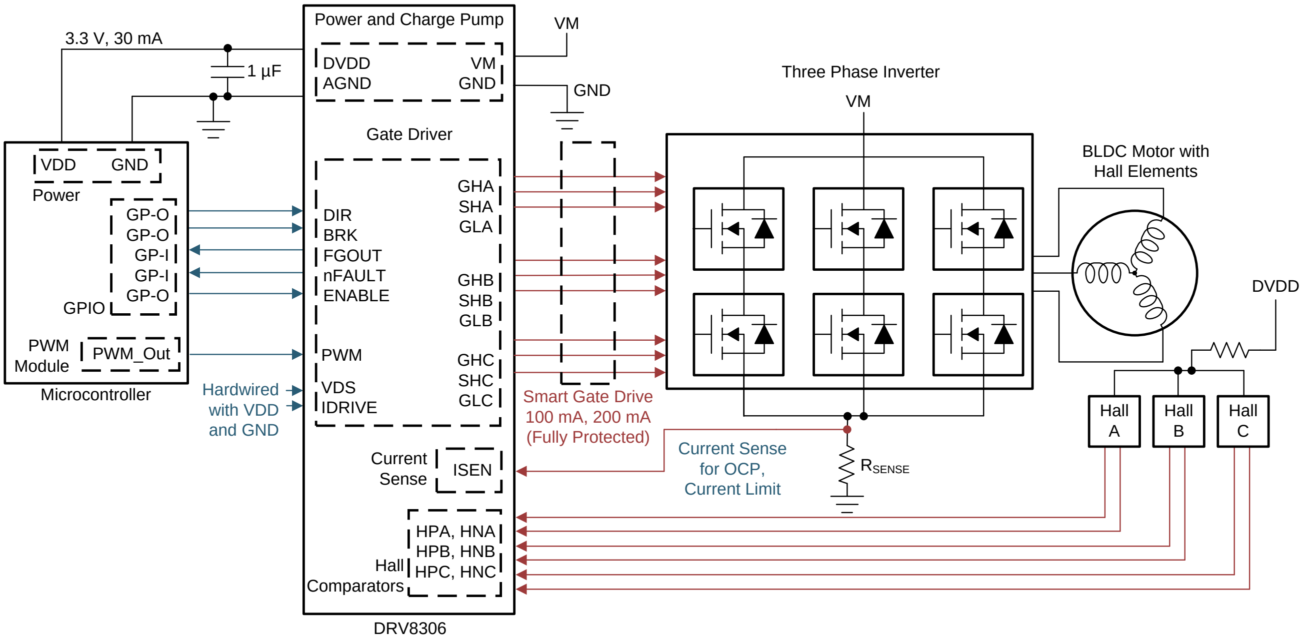


図 30. Primary Application Schematic

9.2.1.1 Design Requirements

表 4 lists the example input parameters for the system design.

表 4. Design Parameters

EXAMPLE DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Nominal supply voltage	V_{VM}	24 V
Supply voltage range		8 V to 38 V
MOSFET part number		CSD18514Q5A
MOSFET total gate charge	Q_g	29 nC (typical) at V_{VGS} = 10 V
MOSFET gate to drain charge	Q_{gd}	5 nC (typical)
Target output rise time	t_r	100 to 300 ns
Target output fall time	t_f	50 to 150 ns
PWM frequency	f_{PWM}	45 kHz
Maximum motor current	I_{max}	50 A
Winding sense current range	I_{SENSE}	–20 A to +20 A
Motor RMS current	I_{RMS}	14.14 A
Sense resistor power rating	P_{SENSE}	2 W
System ambient temperature	T_A	–20°C to +105°C

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 External MOSFET Support

The DRV8306 MOSFET support is based on the charge-pump capacity and output PWM switching frequency. For a quick calculation of MOSFET driving capacity, use 式 3 for three-phase BLDC motor applications.

Trapezoidal 120° Commutation: $I_{VCP} > Q_g \times f_{PWM}$

where

- f_{PWM} is the maximum desired PWM switching frequency.
- I_{VCP} is the charge pump capacity, which depends on the VM pin voltage.
- The multiplier based on the commutation control method, may vary based on implementation. (3)

9.2.1.2.1.1 Example

If a system at V_{VM} = 8 V (I_{VCP} = 15 mA) uses a maximum PWM switching frequency of 45 kHz, then the charge-pump can support MOSFETs using trapezoidal commutation with a Q_g < 333 nC. When the VM voltage (V_{VM}) is 8 V, the maximum DRV8306 gate drive voltage (V_{GSH}) is 7.3 V. Therefore, at 7.3-V gate drive, the target FET (part number CSD18514Q5A) only has a gate charge of approximately 22 nC. Therefore, with this FET, the system can have an adequate margin.

9.2.1.2.2 IDRIVE Configuration

The gate drive current strength, I_{DRIVE}, is selected based on the gate-to-drain charge of the external MOSFETs and the target rise and fall times at the outputs. If I_{DRIVE} is selected to be too low for a given MOSFET, then the MOSFET may not turn on completely within the t_{DRIVE} time and a gate drive fault may be asserted. Additionally, slow rise and fall times will lead to higher switching power losses. TI recommends adjusting these values in the system with the required external MOSFETs and motor to determine the best possible setting for any application.

The I_{DRIVEP} and I_{DRIVEN} current for both the low-side and high-side MOSFETs are selected simultaneously on the IDRIVE pin.

For MOSFETs with a known gate-to-drain charge Q_{gd}, desired rise time (t_r), and a desired fall time (t_f), use 式 4 and 式 5 to calculate the value of I_{DRIVEP} and I_{DRIVEN} (respectively).

$$I_{DRIVEP} = \frac{Q_{gd}}{t_r} \tag{4}$$

$$I_{DRIVEN} = \frac{Q_{gd}}{t_f} \tag{5}$$

9.2.1.2.2.1 Example

Use 式 6 and 式 7 to calculate the value of $I_{DRIVEP1}$ and $I_{DRIVEP2}$ (respectively) for a gate to drain charge of 5 nC and a rise time from 100 to 300 ns.

$$I_{DRIVEP1} = \frac{5\ \text{nC}}{100\ \text{ns}} = 50\ \text{mA} \tag{6}$$

$$I_{DRIVEP2} = \frac{5\ \text{nC}}{300\ \text{ns}} = 16.67\ \text{mA} \tag{7}$$

Select a value for I_{DRIVEP} that is between 16.67 mA and 50 mA. For this example, the value of I_{DRIVEP} was selected as 45-mA source.

Use 式 8 and 式 9 to calculate the value of $I_{DRIVEN1}$ and $I_{DRIVEN2}$ (respectively) for a gate to drain charge of 5 nC and a fall time from 50 to 150 ns.

$$I_{DRIVEN1} = \frac{5\ \text{nC}}{50\ \text{ns}} = 100\ \text{mA} \tag{8}$$

$$I_{DRIVEN2} = \frac{5\ \text{nC}}{150\ \text{ns}} = 33.33\ \text{mA} \tag{9}$$

Select a value for I_{DRIVEN} that is between 33.33 mA and 100 mA. For this example, the value of I_{DRIVEN} was selected as 90-mA sink.

9.2.1.2.3 V_{DS} Overcurrent Monitor Configuration

The V_{DS} monitors are configured based on the worst-case motor current and the $R_{DS(on)}$ of the external MOSFETs as shown in 式 10.

$$V_{DS\_OCP} > I_{max} \times R_{DS(on)max} \tag{10}$$

9.2.1.2.3.1 Example

The goal of this example is to set the V_{DS} monitor to trip at a current greater than 50 A. According to the *CSD18514Q5A 40 V N-Channel NexFET™ Power MOSFET* data sheet, the $R_{DS(on)}$ value is 1.8 times higher at 175°C, and the maximum $R_{DS(on)}$ value at a V_{GS} of 10 V is 4.9 mΩ. From these values, the approximate worst-case value of $R_{DS(on)}$ is 1.8 × 4.9 mΩ = 8.82 mΩ.

Using 式 10 with a value of 8.82 mΩ for $R_{DS(on)}$ and a worst-case motor current of 50 A, 式 11 shows the calculated the value of the V_{DS} monitors.

$$V_{DS\_OCP} > 50\ \text{A} \times 8.82\ \text{m}\Omega$$

$$V_{DS\_OCP} > 0.441\ \text{V} \tag{11}$$

For this example, the value of V_{DS_OCP} was selected as 0.51 V.

The deglitch time for the V_{DS} overcurrent monitor is fixed at 4 µs.

9.2.1.3 Application Curves

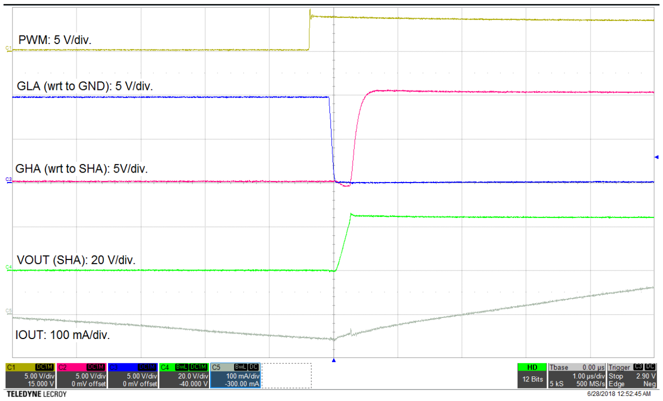


図 31. IDRIVE Maximum Setting

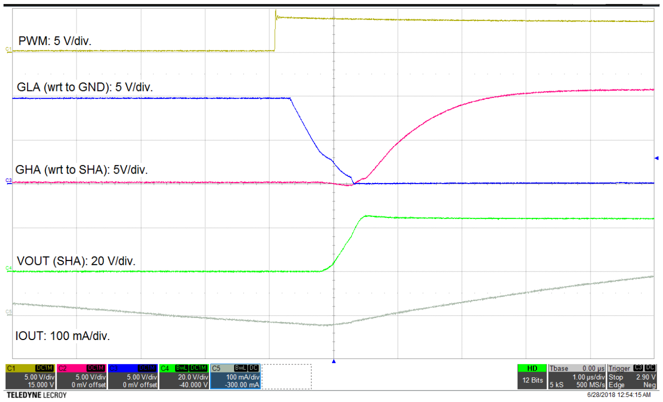


図 32. IDRIVE Minimum Setting

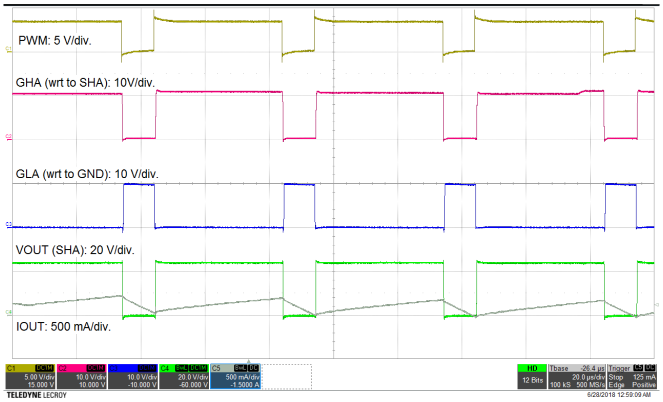


図 33. Gate Drive 80% Duty Cycle

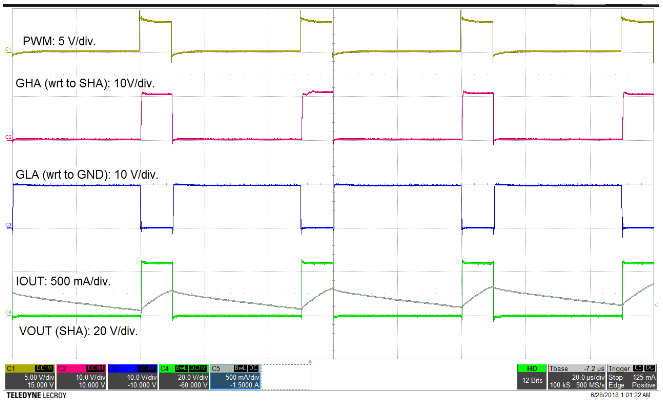


図 34. Gate Drive 20% Duty Cycle

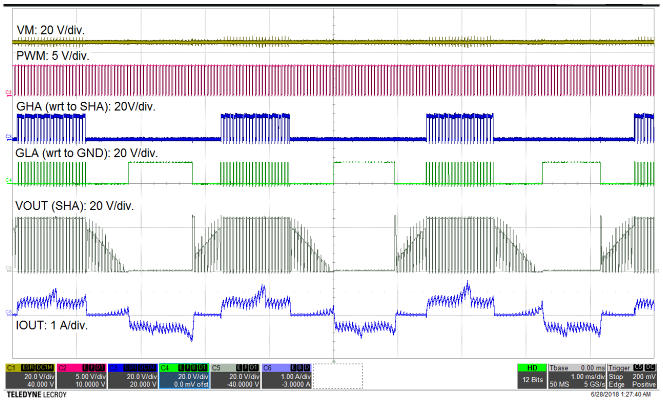


図 35. Motor Operation at 80% PWM Duty

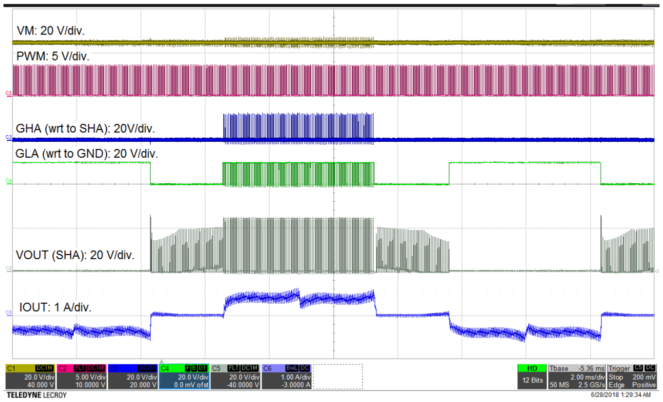


図 36. Motor Operation at 20% PWM Duty

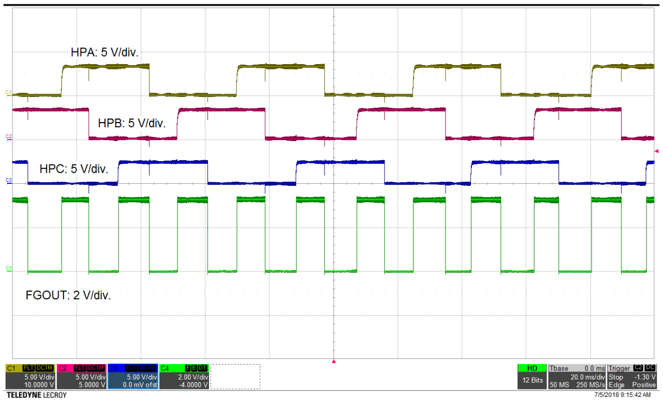


図 37. Hall Operation (Digital Hall Sensors Connected)

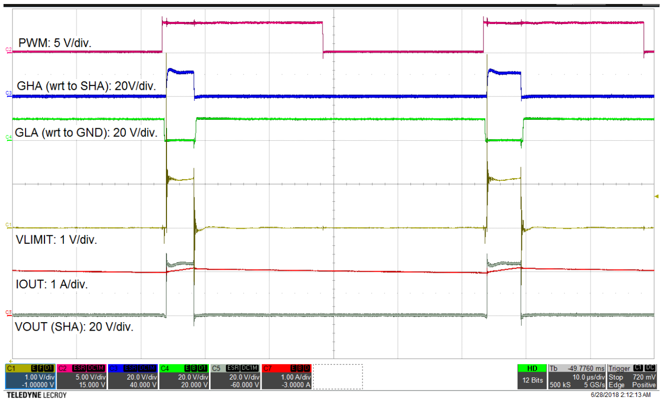


図 38. VLIMIT Operation

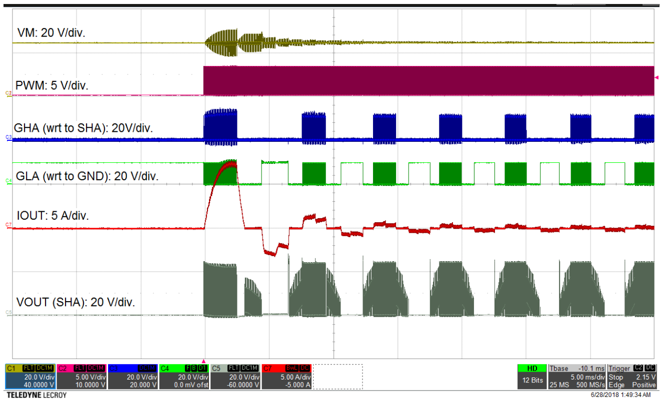


図 39. Motor Starting With PWM Duty Change

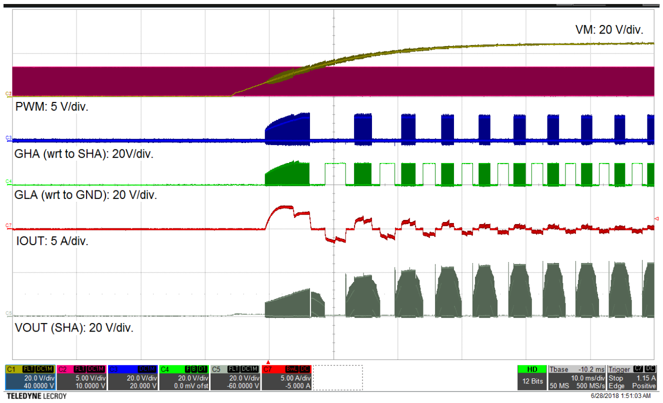


図 40. Motor Starting With Supply Voltage Change

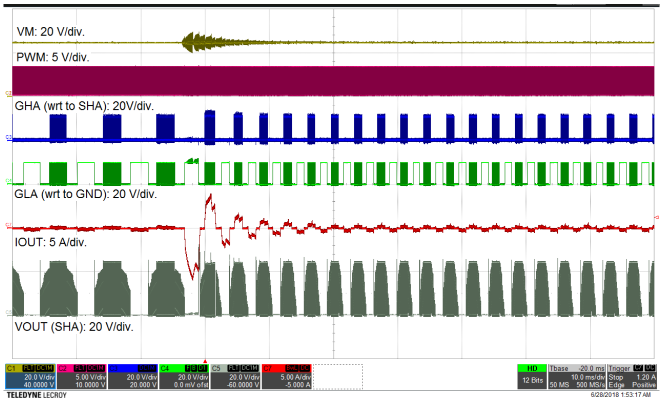


図 41. Motor Performance at Speed Change

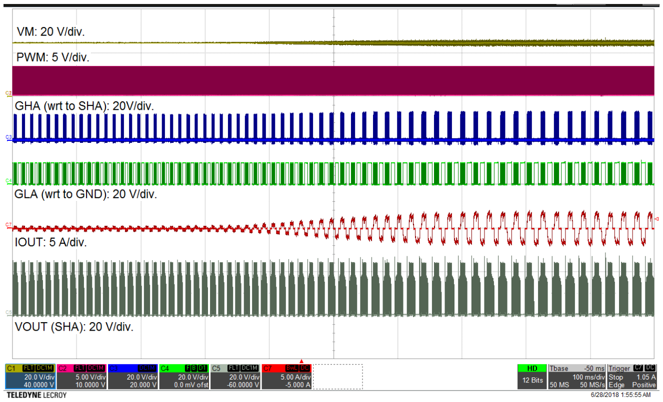


図 42. Motor Performance at Load Change

10 Power Supply Recommendations

The DRV8306 device is designed to operate from an input voltage supply (VM) range from 6 V to 38 V. A 0.1-µF ceramic capacitor rated for VM must be placed as close to the device as possible. In addition, a bulk capacitor must be included on the VM pin but can be shared with the bulk bypass capacitance for the external power MOSFETs. Additional bulk capacitance is required to bypass the external half-bridge MOSFETs and should be sized according to the application requirements.

10.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size. The amount of local capacitance depends on a variety of factors including:

- The highest current required by the motor system
- The power supply's type, capacitance, and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable supply voltage ripple
- Type of motor (brushed DC, brushless DC, stepper)
- The motor startup and braking methods

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet provides a recommended minimum value, but system level testing is required to determine the appropriate sized bulk capacitor.

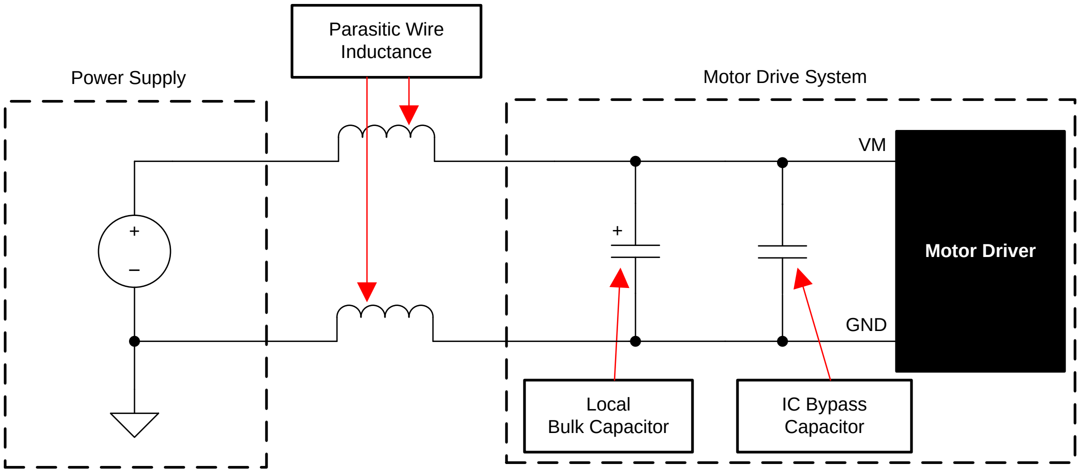


図 43. Motor Drive Supply Parasitics Example

11 Layout

11.1 Layout Guidelines

Bypass the VM pin to the PGND pin using a low-ESR ceramic bypass capacitor with a recommended value of 0.1 µF. Place this capacitor as close to the VM pin as possible with a thick trace or ground plane connected to the PGND pin. Additionally, bypass the VM pin using a bulk capacitor rated for VM. This component can be electrolytic. This capacitance must be at least 10 µF.

Additional bulk capacitance is required to bypass the high current path on the external MOSFETs. This bulk capacitance should be placed such that it minimizes the length of any high current paths through the external MOSFETs. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and let the bulk capacitor deliver high current.

Place a low-ESR ceramic capacitor between the CPL and CPH pins. This capacitor should be 47 nF, rated for VM, and be of type X5R or X7R. Additionally, place a low-ESR ceramic capacitor between the VCP and VM pins. This capacitor should be 1 µF, rated for 16 V, and be of type X5R or X7R.

Bypass the DVDD pin to the AGND pin with a 1-µF low-ESR ceramic capacitor rated for 6.3 V and of type X5R or X7R. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the AGND pin.

The VDRAIN pin can be shorted directly to the VM pin. However, if a significant distance is between the device and the external MOSFETs, use a dedicated trace to connect to the common point of the drains of the high-side external MOSFETs. Do not connect the SLx pins directly to PGND. Instead, use dedicated traces to connect these pins to the sources of the low-side external MOSFETs. These recommendations offer more accurate V_{DS} sensing of the external MOSFETs for overcurrent detection.

Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the GHx pin of the device to the high-side power MOSFET gate, then follows the high-side MOSFET source back to the SHx pin. The low-side loop is from the GLx pin of the device to the low-side power MOSFET gate, then follows the low-side MOSFET source back to the PGND pin.

11.2 Layout Example

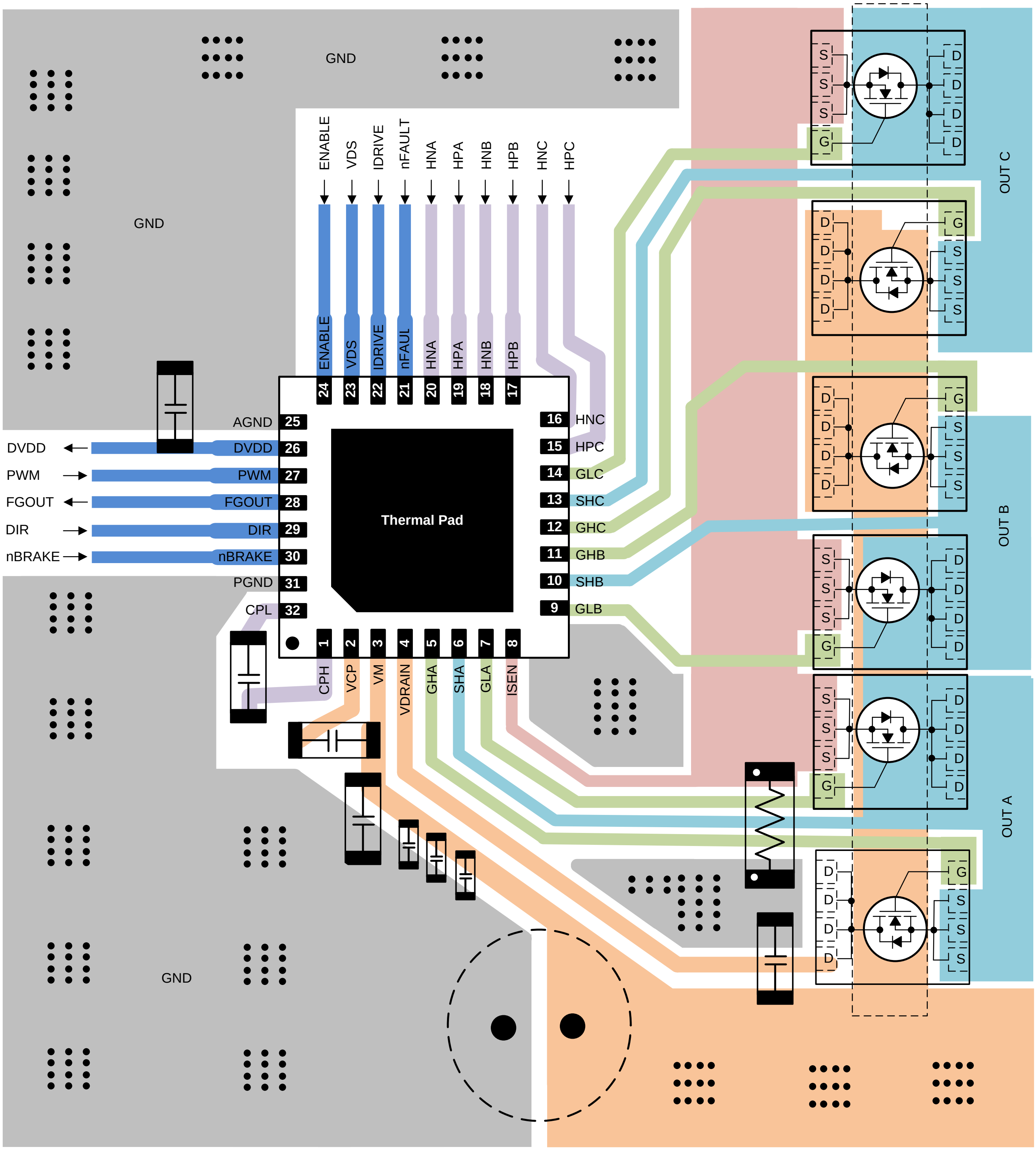


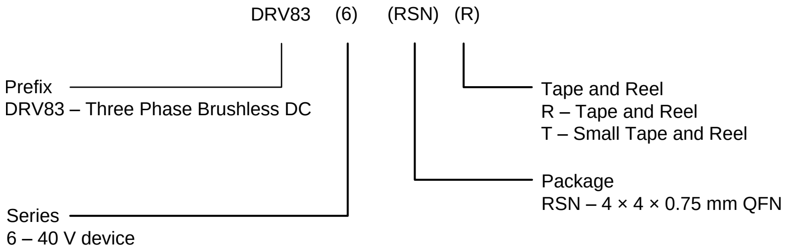
図 44. Layout Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの項目表記

次の図は、完全なデバイス名を解釈するための凡例を示したものです。



12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『AN-1149 スイッチング電源のレイアウトのガイドライン』*アプリケーション・レポート
- テキサス・インスツルメンツ、*『DRV8306EVMユーザー・ガイド』*
- テキサス・インスツルメンツ、*『BLDCモータを使用する効率的な掃除機のハードウェア設計の考慮事項』*アプリケーション・レポート
- テキサス・インスツルメンツ、*『BLDCモータを使用する電動自転車のハードウェア設計の考慮事項』*アプリケーション・レポート
- テキサス・インスツルメンツ、*『産業用モーター・ドライブ・ソリューション・ガイド』*
- テキサス・インスツルメンツ、*『スイッチング電源のレイアウトのガイドライン』*アプリケーション・レポート
- テキサス・インスツルメンツ、*『TIスマート・ゲート・ドライブによるモータ・ドライブの保護』*TI TechNote
- テキサス・インスツルメンツ、*『QFN/SONのPCB実装』*アプリケーション・レポート
- テキサス・インスツルメンツ、*『TIスマート・ゲート・ドライブによるモータ・ドライブのBOMとPCB面積の削減』*TI TechNote
- テキサス・インスツルメンツ、*『MSP430™を使用するセンサ付き3相BLDCモーター制御』*アプリケーション・レポート
- テキサス・インスツルメンツ、*『TI製モーター・ゲート・ドライバでのIDRIVEおよびTDRIVEについて』*アプリケーション・レポート

12.3 ドキュメントの更新通知を受け取る方法

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12.4 コミュニティ・リソース

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12.5 商標

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12.6 静電気放電に関する注意事項

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8306HRSMR	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8306H
DRV8306HRSMR.A	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8306H
DRV8306HRSMT	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8306H
DRV8306HRSMT.A	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8306H

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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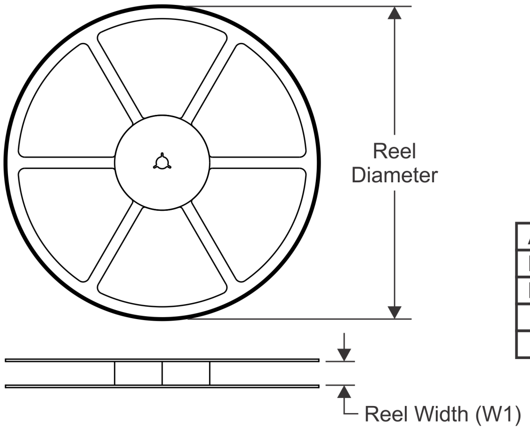
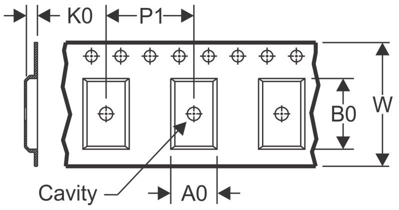
TAPE AND REEL INFORMATION

REEL DIMENSIONS

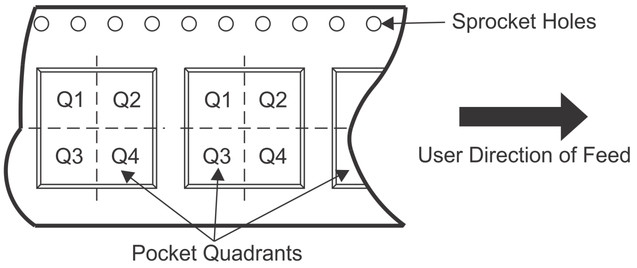


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

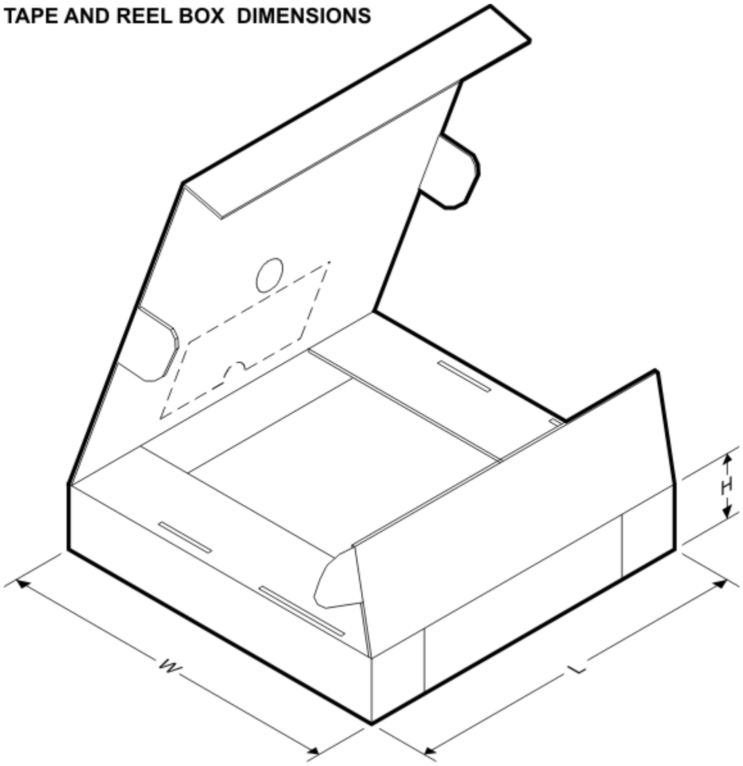
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8306HRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV8306HRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8306HRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
DRV8306HRSMT	VQFN	RSM	32	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

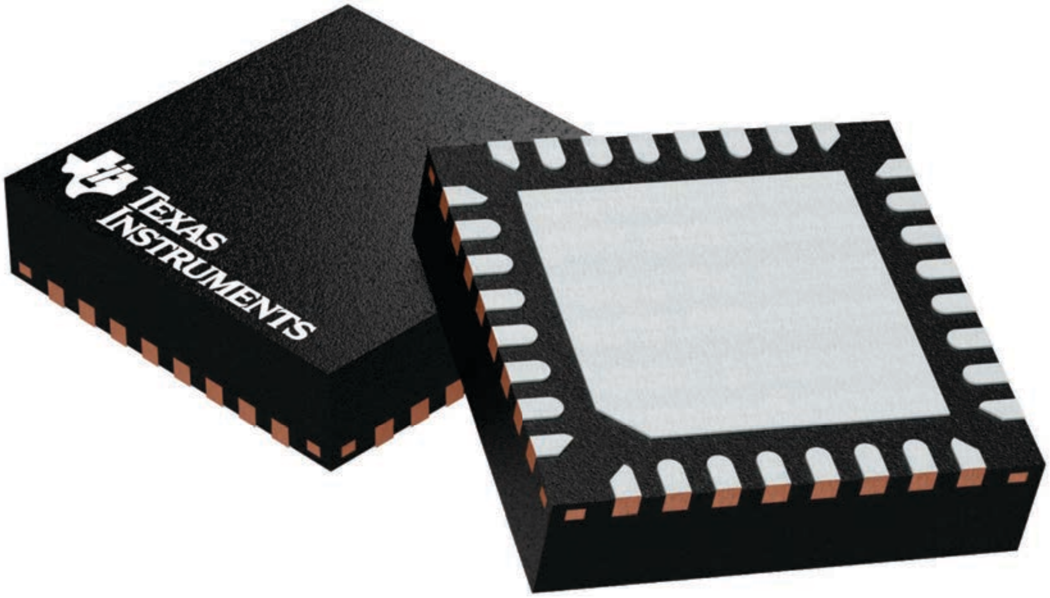
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

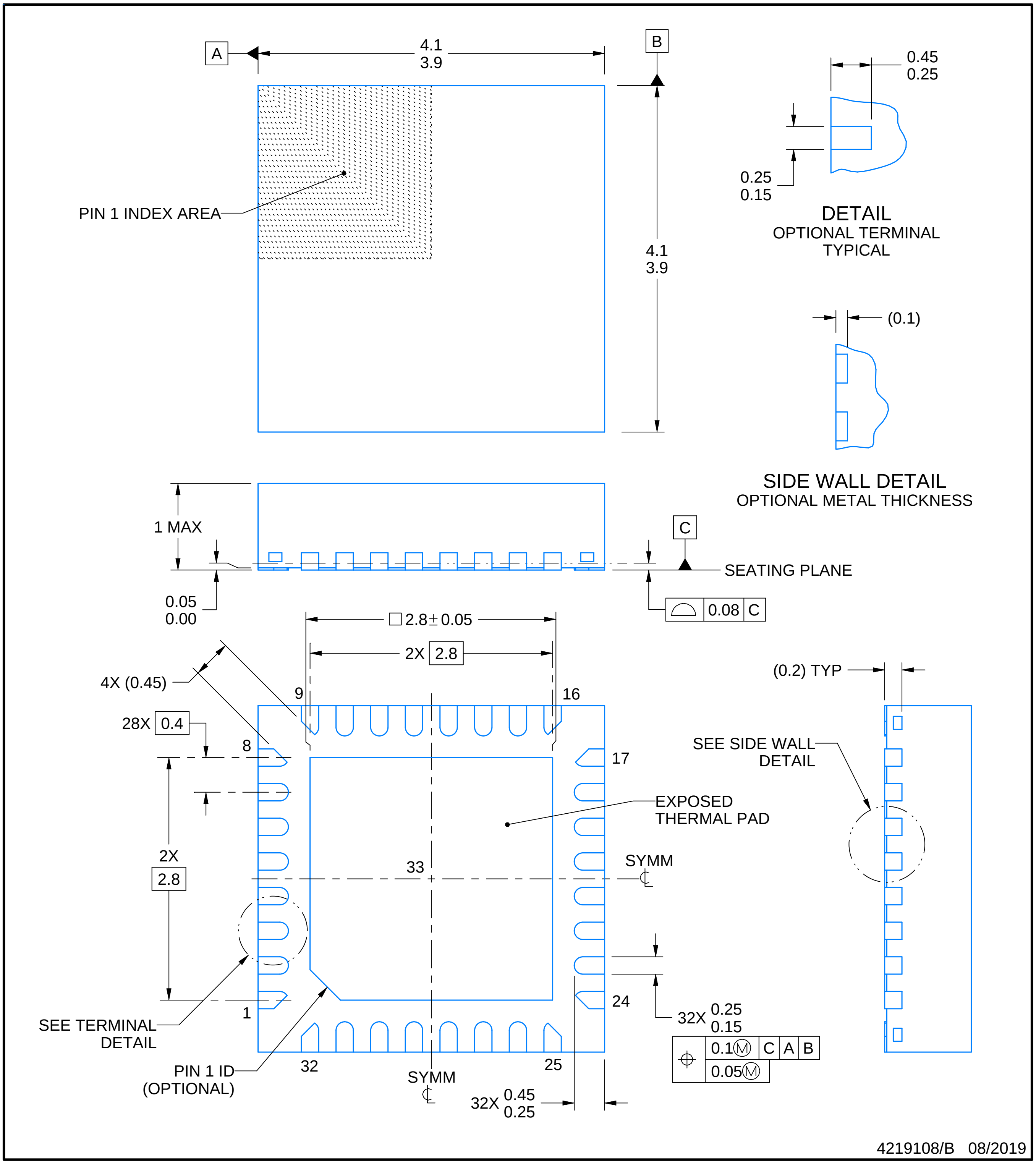


4224982/A

PACKAGE OUTLINE

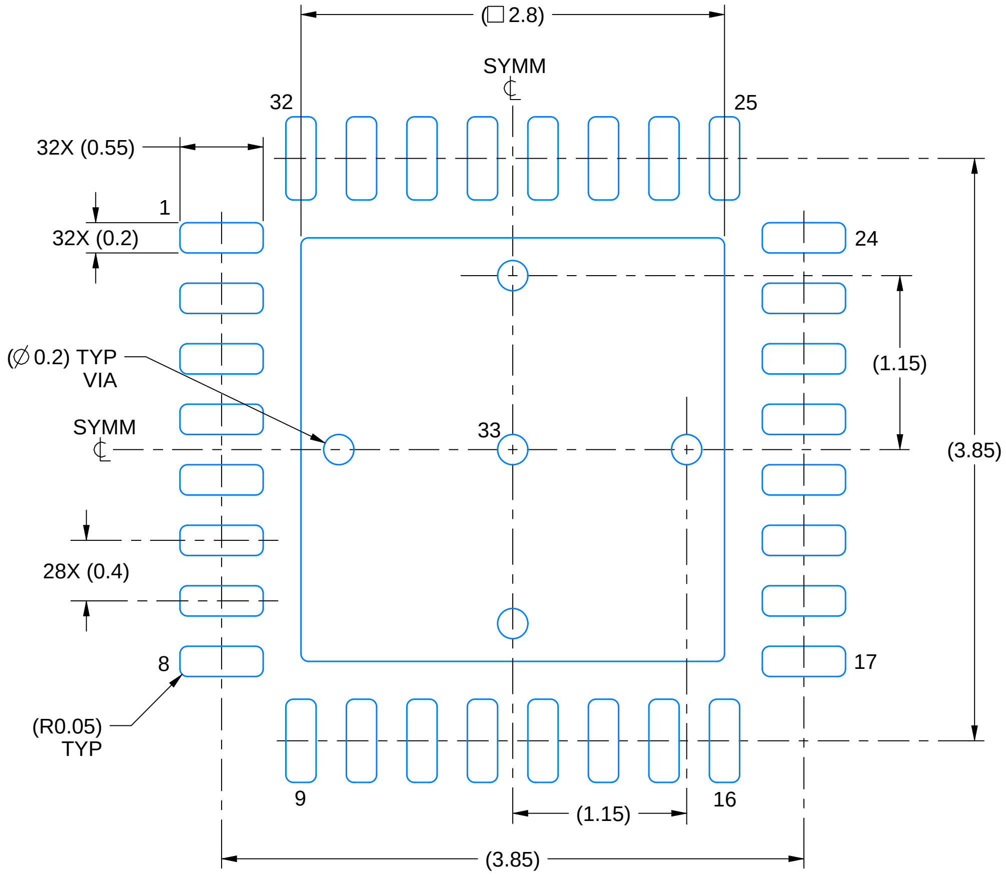
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

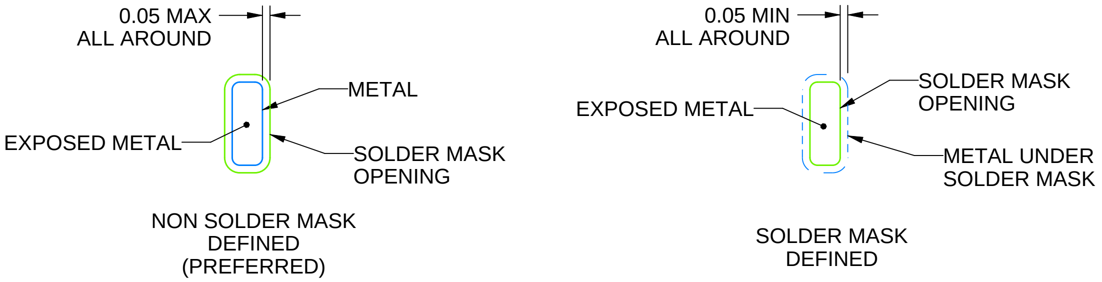


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



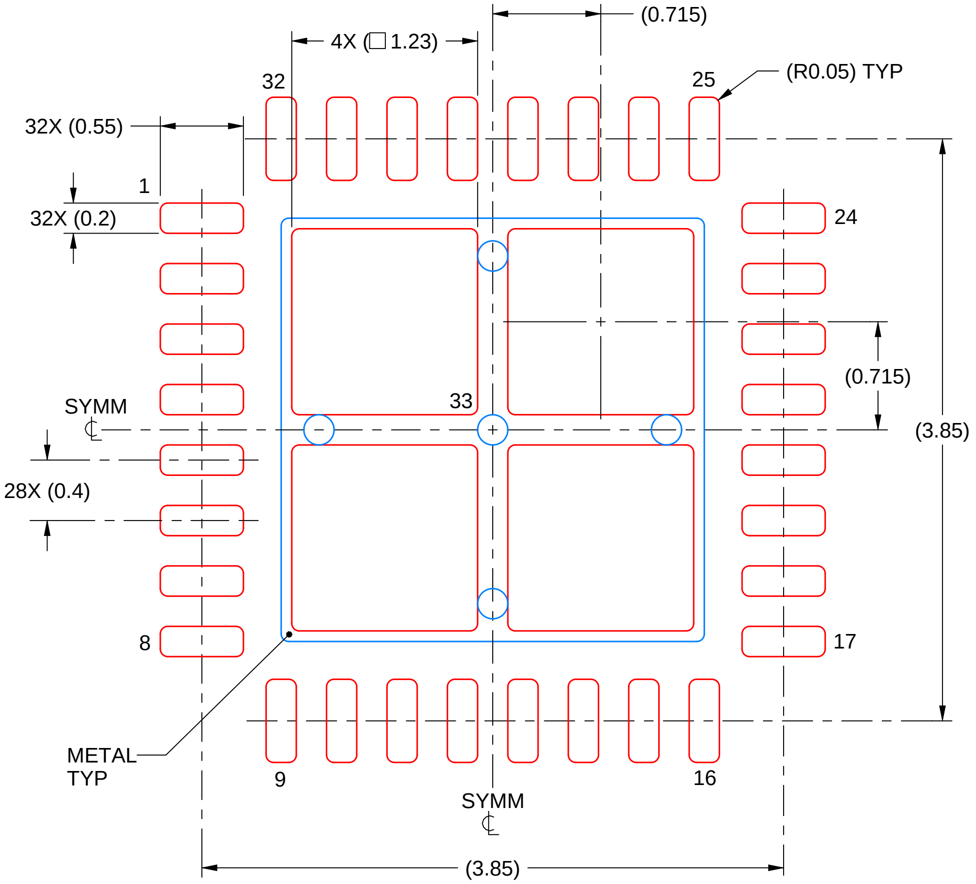
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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