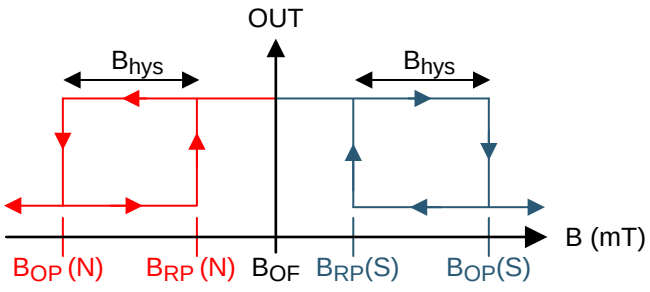
TEXAS INSTRUMENTS
DRV5033-Q1
JAJSC70E – DECEMBER 2014 – REVISED SEPTEMBER 2016

DRV5033-Q1 車載用デジタル・オムニポーラ・スイッチ・ホール効果センサ

1 特長

- デジタル・オムニポーラ・スイッチ・ホール・センサ
- 車載アプリケーション用にAEC-Q100認定済み
  - グレード 1: T_A = –40℃～125℃ (Q、図 23を参照)
  - グレード0: T_A = –40℃～150℃ (E、図 23を参照)
- 優れた温度安定性
  - 温度範囲全体にわたってB_{OP}±10%
- 複数の感度オプション(B_{OP} / B_{RP})
  - ±3.5 / ±2 mT (FA、図 23を参照)
  - ±6.9 / ±3.5 mT (AJ、図 23を参照)
- N極とS極の磁場を検出
- 広い範囲の電圧をサポート
  - 2.7V～38V
  - 外部レギュレータ不要
- オープン・ドレイン出力(30mAシンク)
- 高速な電源オン時間: 35µs
- 小さなパッケージと占有面積
  - 表面実装の3ピンSOT-23 (DBZ)
    - 2.92mm×2.37mm
  - スルーホールの3ピンTO-92 (LPG)
    - 4.00mm×3.15mm
- 保護機能
  - 逆電圧保護(最大-22V)
  - 40Vまでの負荷ダンプをサポート
  - 出力短絡保護
  - 出力電流制限
  - OUTからバッテリへの短絡保護

出力状態



2 アプリケーション

- ドッキング検出
- ドアの開閉検出
- 近接感知
- バルブの位置決め
- パルスのカウント

3 概要

DRV5033-Q1デバイスはチョッパ安定化されたホール効果センサで、温度範囲全体にわたって優れた感度の安定性を持つ磁気感知ソリューションを提供し、保護機能が内蔵されています。

DRV5033-Q1は磁場方向の検出において、両方の極に対して同じように反応します。周囲の磁束密度がB_{OP}スレッショルドを超えると、DRV5033-Q1のオープン・ドレイン出力がLOWに変化します。磁場がB_{RP}未満に低下するまで出力はLOWに維持され、その後で出力がHIGHインピーダンスになります。出力電流シンクの容量は30mAです。2.7V～38Vまでの広い範囲の電圧で動作し、-22Vまでは逆極性保護されるため、広範な車載用アプリケーションに適したデバイスです。

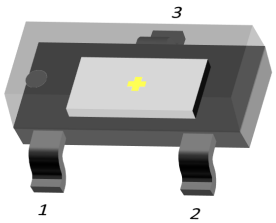
逆電圧の状態、負荷ダンプ、および出力短絡や過電流に対して、内部的な保護機能が搭載されています。

製品情報(1)

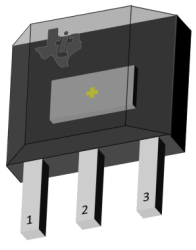
型番	パッケージ	本体サイズ(公称)
DRV5033-Q1	SOT-23 (3)	2.92mm×1.30mm
	TO-92 (3)	4.00mm×3.15mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

SOT-23



TO-92



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (May 2016) から **Revision E** に変更 **Page**

- Made changes to the Power-on time in the *Electrical Characteristics* table ... 5

Revision C (February 2016) から **Revision D** に変更 **Page**

- Revised preliminary limits for the FA version ... 5

Revision B (December 2015) から **Revision C** に変更 **Page**

- FAデバイス・オプション 追加 ... 1
- Added the typical bandwidth value to the *Magnetic Characteristics* table ... 5

Revision A (May 2015) から **Revision B** に変更 **Page**

- SOT-23パッケージの本体サイズを訂正し、SIPパッケージ名をTO-92に訂正 ... 1
- Added B_{MAX} to *Absolute Maximum Ratings* ... 4
- Removed table notes regarding testing for the operating junction temperature in *Absolute Maximum Ratings* ... 4
- パッケージのテープ&リールに関するMとブランクのオプションを更新 ... 18
- コミュニティ・リソースを追加 ... 19

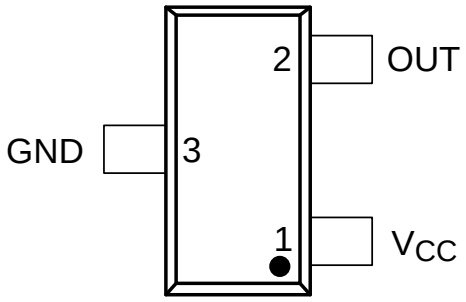
2014年12月 発行のものから更新 **Page**

- デバイスのステータスを量産データへ更新 ... 1

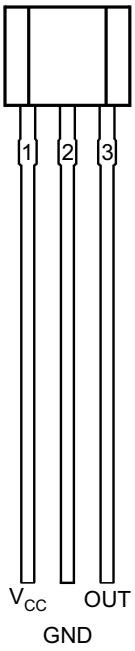
5 Pin Configuration and Functions

For additional configuration information, see デバイスのマーキング and メカニカル、パッケージ、および注文情報.

DBZ Package
3-Pin SOT-23
Top View



LPG Package
3-Pin TO-92
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DBZ	LPG		
GND	3	2	GND	Ground pin
OUT	2	3	Output	Hall sensor open-drain output. The open drain requires a resistor pullup.
V_{CC}	1	1	PWR	2.7 to 38 V power supply. Bypass this pin to the GND pin with a 0.01-µF (minimum) ceramic capacitor rated for V_{CC}.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Power supply voltage	V_{CC}	–22 (2)	40	V
	Voltage ramp rate (V_{CC}), V_{CC} < 5 V	Unlimited		V/µs
	Voltage ramp rate (V_{CC}), V_{CC} > 5 V	0	2	
Output pin voltage		–0.5	40	V
Output pin reverse current during reverse supply condition		0	100	mA
Magnetic flux density, B_{MAX}		Unlimited		
Operating junction temperature, T_J	Q, see 図 23	–40	150	°C
	E, see 図 23	–40	17	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Ensured by design. Only tested to –20 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Power supply voltage		2.7	38	V
V_O	Output pin voltage (OUT)		0	38	V
I_{SINK}	Output pin current sink (OUT) (1)		0	30	mA
T_A	Operating ambient temperature	Q, see 図 23	–40	125	°C
		E, see 図 23	–40	150	

(1) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC (1)		DRV5033-Q1		UNIT
		DBZ (SOT-23)	LPG (TO-92)	
		3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	333.2	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.9	98.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.9	154.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.9	40	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.2	154.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (V_{CC})						
V_{CC}	V_{CC} operating voltage		2.7		38	V
I_{CC}	Operating supply current	V_{CC} = 2.7 to 38 V, T_A = 25°C		2.7		mA
		V_{CC} = 2.7 to 38 V, T_A = $T_{A, MAX}$ (1)		3	3.6	
t_{on}	Power-on time	AJ version		35	50	µs
		FA version		35	70	
OPEN DRAIN OUTPUT (OUT)						
$r_{DS(on)}$	FET on-resistance	V_{CC} = 3.3 V, I_O = 10 mA, T_A = 25°C		22		Ω
		V_{CC} = 3.3 V, I_O = 10 mA, T_A = 125°C		36	50	
$I_{lkg(off)}$	Off-state leakage current	Output Hi-Z			1	µA
PROTECTION CIRCUITS						
V_{CCR}	Reverse supply voltage		–22			V
I_{OCP}	Overcurrent protection level	OUT shorted V_{CC}	15	30	45	mA

(1) $T_{A, MAX}$ is 125°C for Q Grade 1 devices and 150°C for E Grade 0 devices (see 図 23)

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN DRAIN OUTPUT (OUT)						
t_d	Output delay time	B = B_{RP} – 10 mT to B_{OP} + 10 mT in 1 µs		13	25	µs
t_r	Output rise time (10% to 90%)	R1 = 1 kΩ, C_O = 50 pF, V_{CC} = 3.3 V		200		ns
t_f	Output fall time (90% to 10%)	R1 = 1 kΩ, C_O = 50 pF, V_{CC} = 3.3 V		31		ns

6.7 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT (1)
f_{BW}	Bandwidth (2)		20	30		kHz
DRV5033FA: ±3.5 / ±2 mT						
B_{OP}	Operate point; see Figure 12		±1.8	±3.5	±6.8	mT
B_{RP}	Release point; see Figure 12		±0.5	±2	±4.2	mT
B_{hys}	Hysteresis; B_{hys} = (B_{OP} – B_{RP}) (3)			±1.5		mT
B_O	Magnetic offset; B_O = (B_{OP} + B_{RP}) / 2			±2.8		mT
DRV5033AJ: ±6.9 / ±3.5 mT						
B_{OP}	Operate point; see Figure 12		±3	±6.9	±12	mT
B_{RP}	Release point; see Figure 12		±1	±3.5	±5	mT
B_{hys}	Hysteresis; B_{hys} = (B_{OP} – B_{RP}) (3)			3.4		mT
B_O	Magnetic offset; B_O = (B_{OP} + B_{RP}) / 2			5.2		mT

(1) 1 mT = 10 Gauss
(2) Bandwidth describes the fastest changing magnetic field that can be detected and translated to the output.
(3) $|B_{OP}|$ is always greater than $|B_{RP}|$.

6.8 Typical Characteristics

T_A > 125°C data is valid for Grade 0 devices only (E, see 図 23)

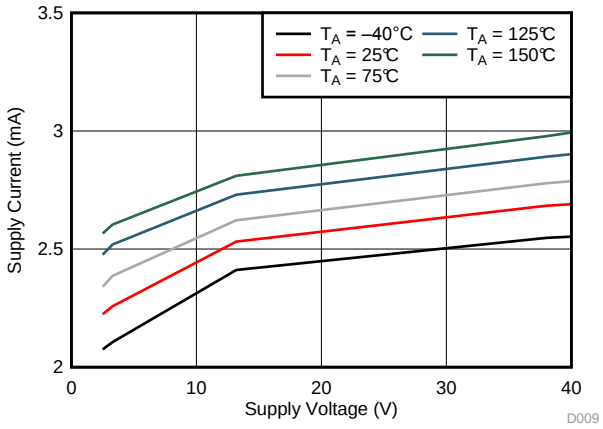


Figure 1. I_{CC} vs V_{CC}

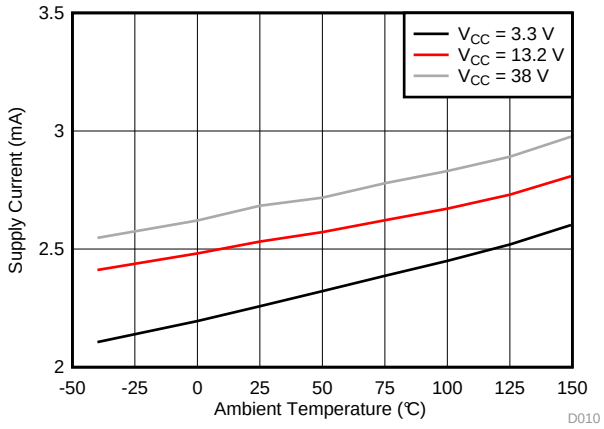
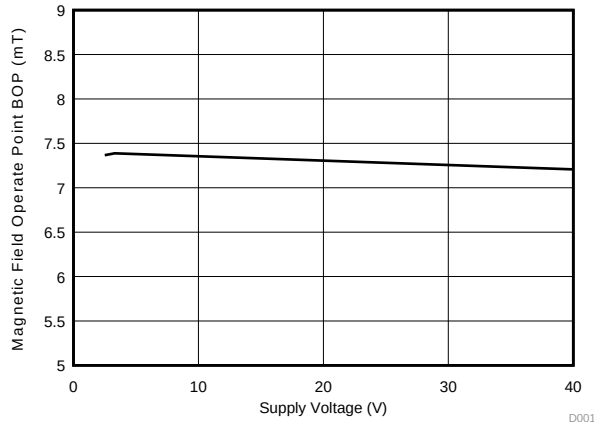
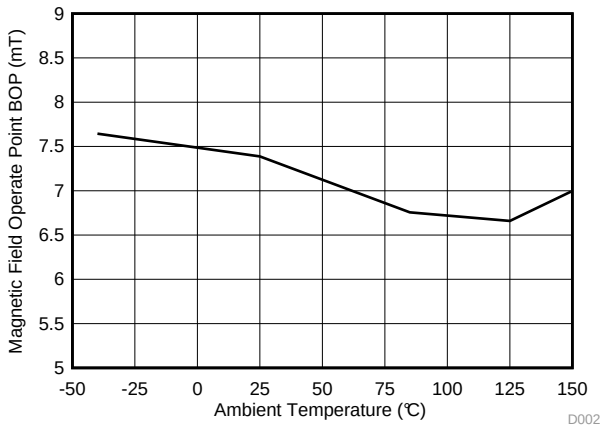


Figure 2. I_{CC} vs Temperature



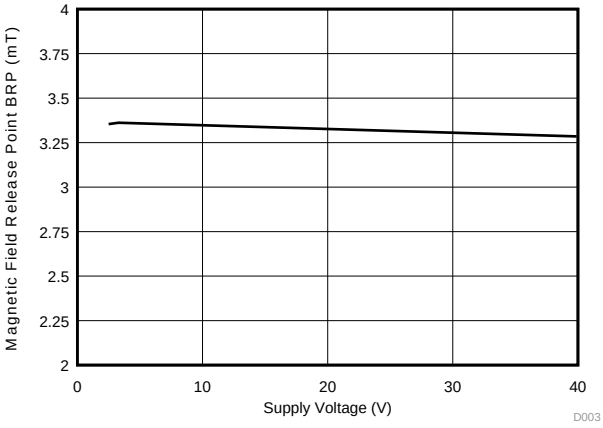
T_A = 25°C

Figure 3. DRV5033-Q1AJ, B_{OP} vs V_{CC}



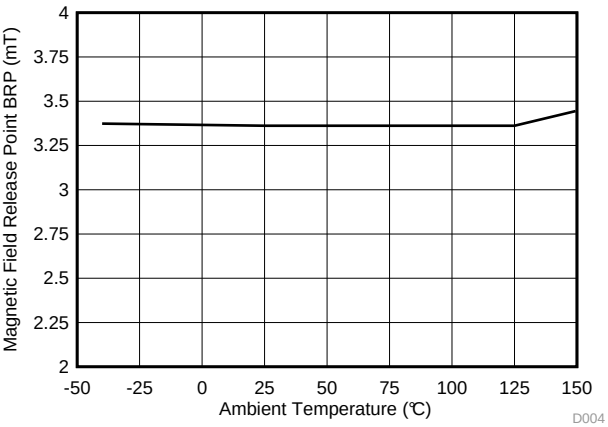
V_{CC} = 3.3 V

Figure 4. DRV5033-Q1AJ, B_{OP} vs Temperature



T_A = 25°C

Figure 5. DRV5033-Q1AJ, B_{RP} vs V_{CC}

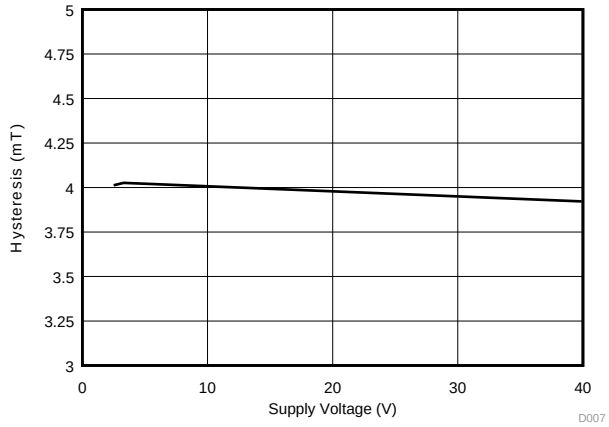


V_{CC} = 3.3 V

Figure 6. DRV5033-Q1AJ, B_{RP} vs Temperature

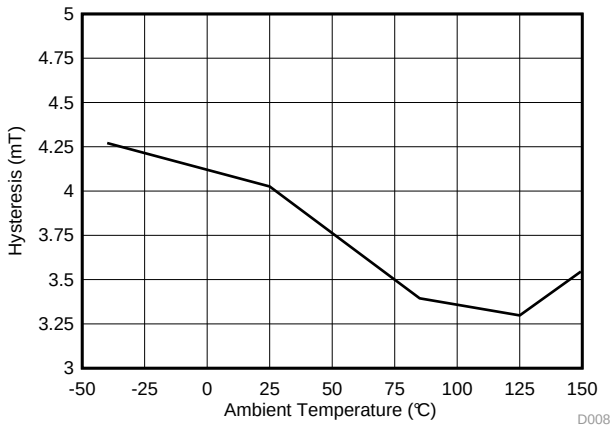
Typical Characteristics (continued)

T_A > 125°C data is valid for Grade 0 devices only (E, see 図 23)



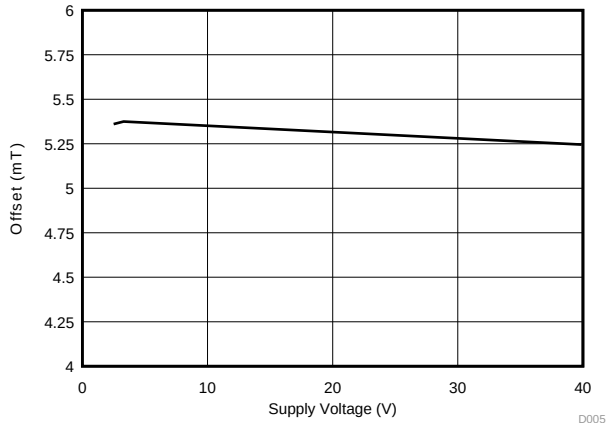
T_A = 25°C

Figure 7. DRV5033-Q1AJ, Hysteresis vs V_{CC}



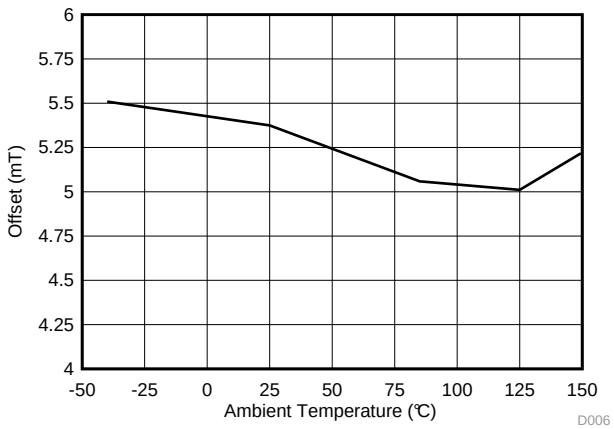
V_{CC} = 3.3 V

Figure 8. DRV5033-Q1AJ, Hysteresis vs Temperature



T_A = 25°C

Figure 9. DRV5033-Q1AJ, Offset vs V_{CC}



V_{CC} = 3.3 V

Figure 10. DRV5033-Q1AJ, Offset vs Temperature

7 Detailed Description

7.1 Overview

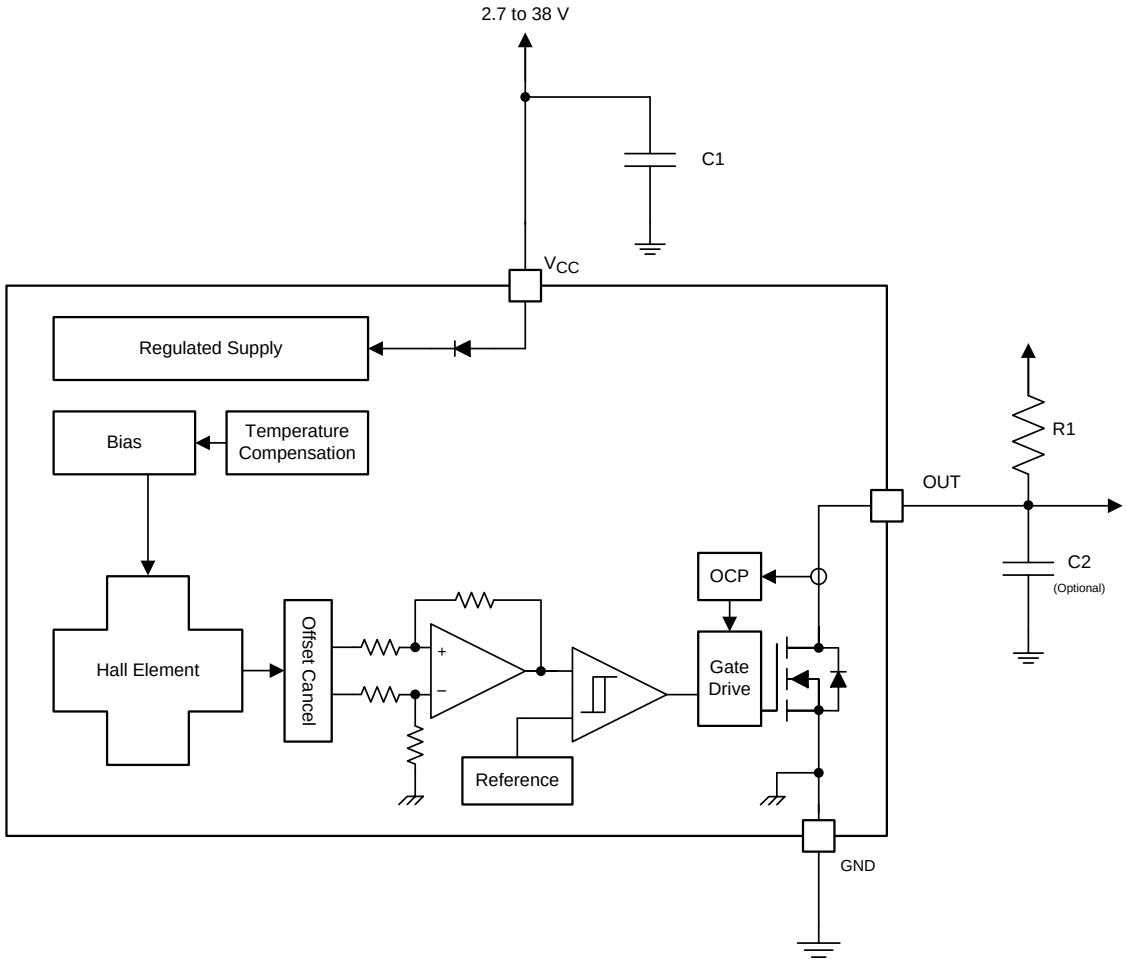
The DRV5033-Q1 device is a chopper-stabilized hall sensor with a digital omnipolar switch output for magnetic sensing applications. The DRV5033-Q1 device can be powered with a supply voltage between 2.7 and 38 V, and will survive –22 V reverse battery conditions continuously. Note that the DRV5033-Q1 device will not be operating when about –22 to 2.4 V is applied to V_{CC} (with respect to GND). In addition, the device can withstand voltages up to 40 V for transient durations.

The field polarity is defined as follows: a south pole near the marked side of the package is a positive magnetic field. A north pole near the marked side of the package is a negative magnetic field.

The omnipolar configuration allows the hall sensor to respond to either a south or north pole. A strong magnetic field of either polarity will cause the output to pull low (operate point, B_{OP}), and a weaker magnetic field will cause the output to release (release point, B_{RP}). Hysteresis is included in between the operate and release points, so magnetic field noise will not trip the output accidentally.

An external pullup resistor is required on the OUT pin. The OUT pin can be pulled up to V_{CC}, or to a different voltage supply. This allows for easier interfacing with controller circuits.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Field Direction Definition

A positive magnetic field is defined as a south pole near the marked side of the package as shown in Figure 11.

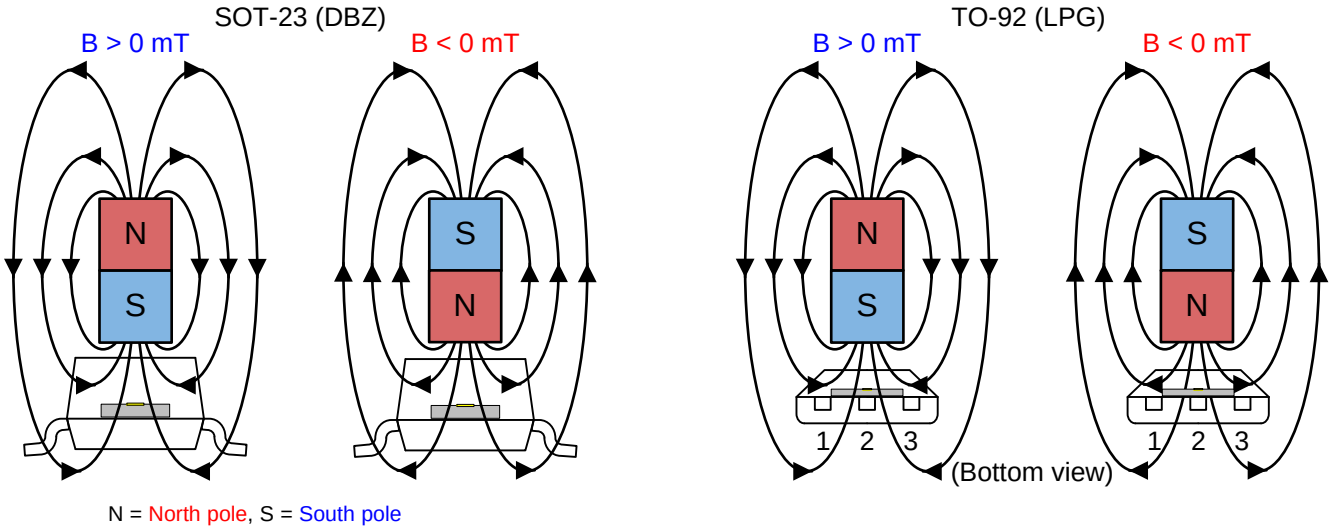


Figure 11. Field Direction Definition

7.3.2 Device Output

If the device is powered on with a magnetic field strength between B_{RP} and B_{OP}, then the device output is indeterminate and can either be Hi-Z or Low. If the field strength is greater than B_{OP}, then the output is pulled low. If the field strength is less than B_{RP}, then the output is released.

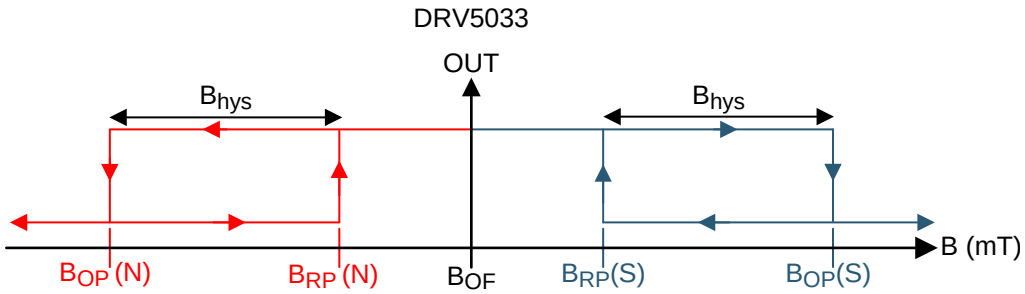


Figure 12. DRV5033-Q1—B_{OP} > 0

Feature Description (continued)

7.3.3 Power-On Time

After applying V_{CC} to the DRV5033-Q1 device, t_{on} must elapse before the OUT pin is valid. During the power-up sequence, the output is Hi-Z. A pulse as shown in Figure 13 and Figure 14 occurs at the end of t_{on}. This pulse can allow the host processor to determine when the DRV5033-Q1 output is valid after startup. In Case 1 (Figure 13) and Case 2 (Figure 14), the output is defined assuming a constant magnetic field B > B_{OP} and B < B_{RP}.

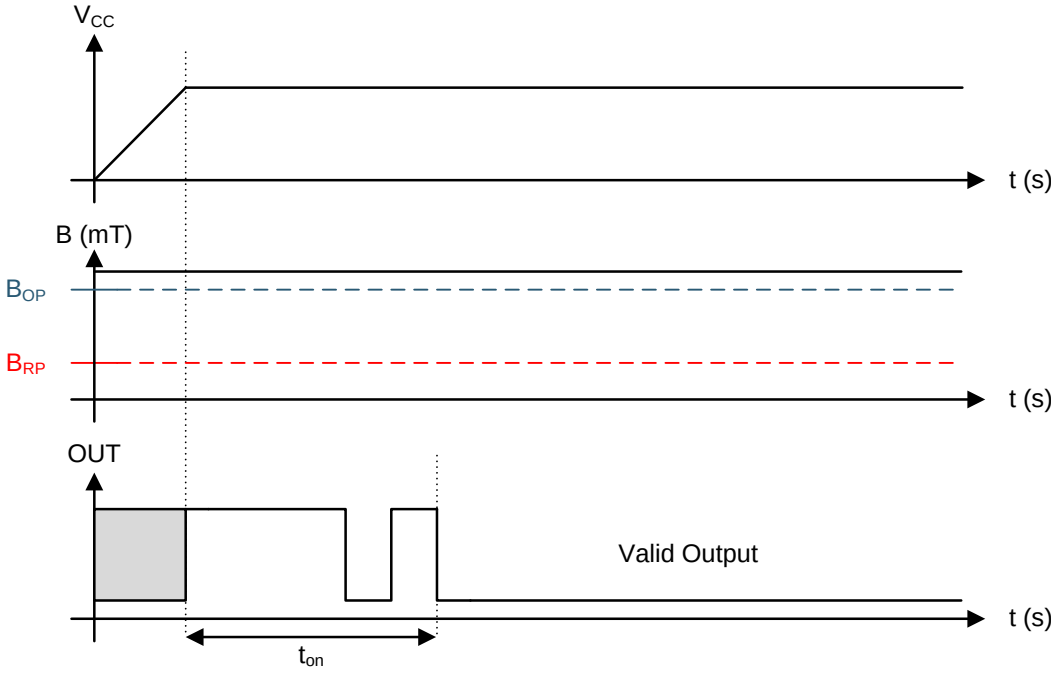


Figure 13. Case 1: Power On When B > B_{OP}

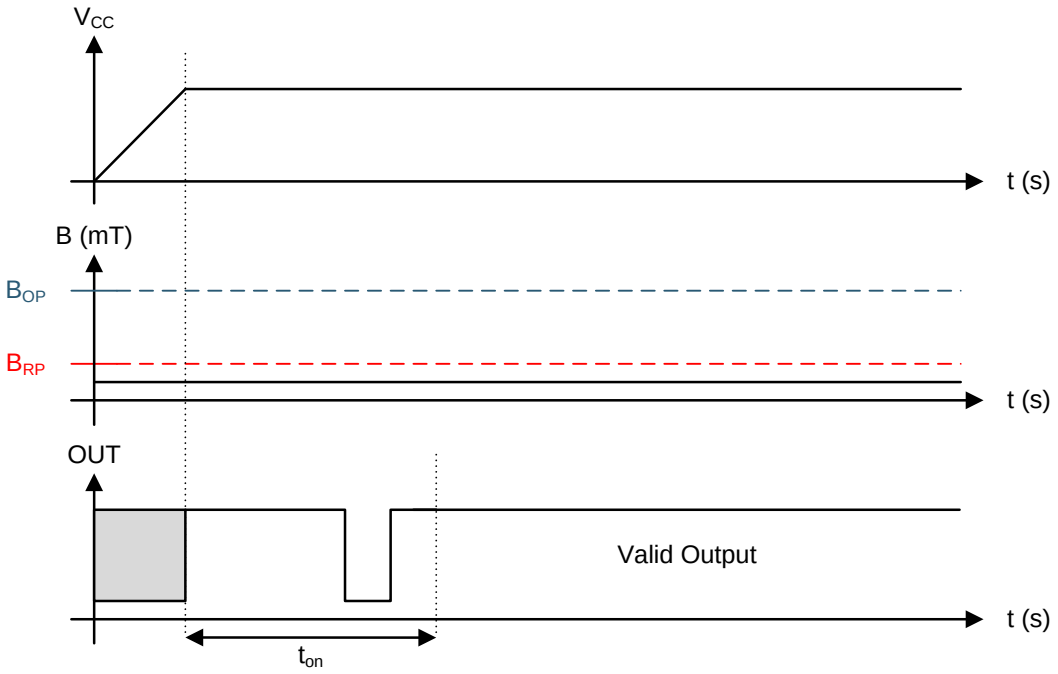


Figure 14. Case 2: Power On When B < B_{RP}

Feature Description (continued)

If the device is powered on with the magnetic field strength B_{RP} < B < B_{OP}, then the device output is indeterminate and can either be Hi-Z or pulled low. During the power-up sequence, the output is held Hi-Z until t_{on} has elapsed. At the end of t_{on}, a pulse is given on the OUT pin to indicate that t_{on} has elapsed. After t_{on}, if the magnetic field changes such that B_{OP} < B, the output is released. Case 3 (Figure 15) and Case 4 (Figure 16) show examples of this behavior.

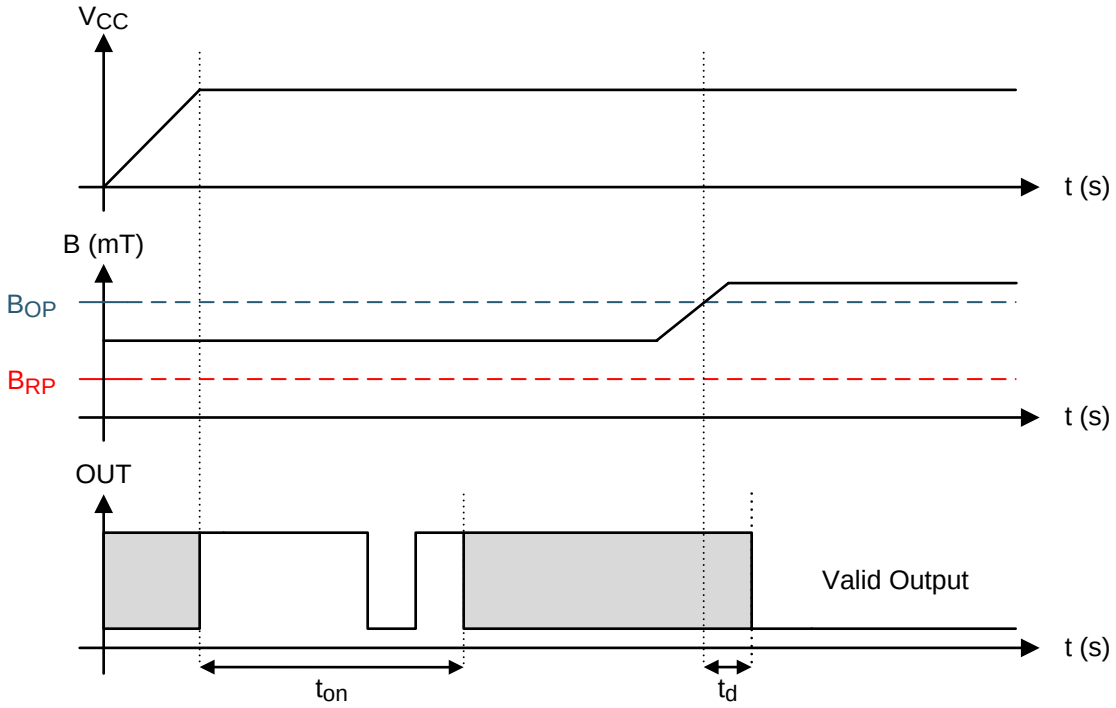


Figure 15. Case 3: Power On When B_{RP} < B < B_{OP}, Followed by B > B_{OP}

Feature Description (continued)

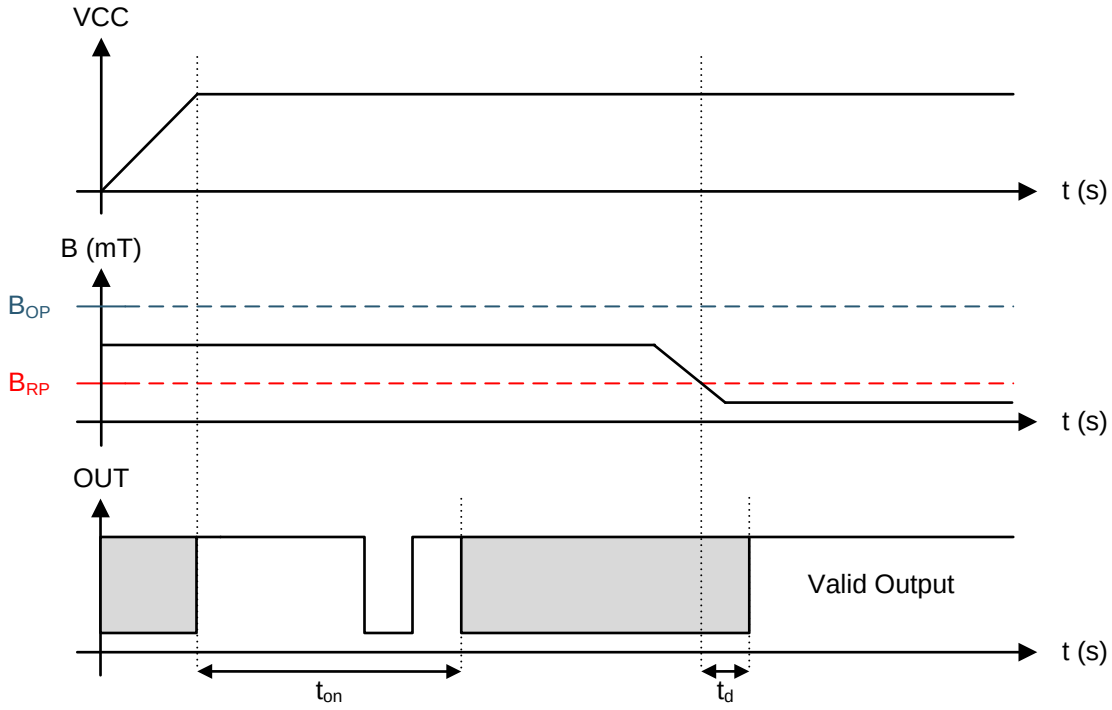


Figure 16. Case 4: Power On When B_{RP} < B < B_{OP}, Followed by B < B_{RP}

7.3.4 Output Stage

The DRV5033-Q1 output stage uses an open-drain NMOS, and it is rated to sink up to 30 mA of current. For proper operation, calculate the value of the pullup resistor R1 using Equation 1.

$$\frac{V_{ref}\,max}{30\ mA} \le R1 \le \frac{V_{ref}\,min}{100\ \mu A} \quad (1)$$

The size of R1 is a tradeoff between the OUT rise time and the current when OUT is pulled low. A lower current is generally better, however faster transitions and bandwidth require a smaller resistor for faster switching.

In addition, ensure that the value of R1 > 500 Ω to ensure the output driver can pull the OUT pin close to GND.

NOTE

V_{ref} is not restricted to V_{CC}. The allowable voltage range of this pin is specified in the *Absolute Maximum Ratings*.

Feature Description (continued)

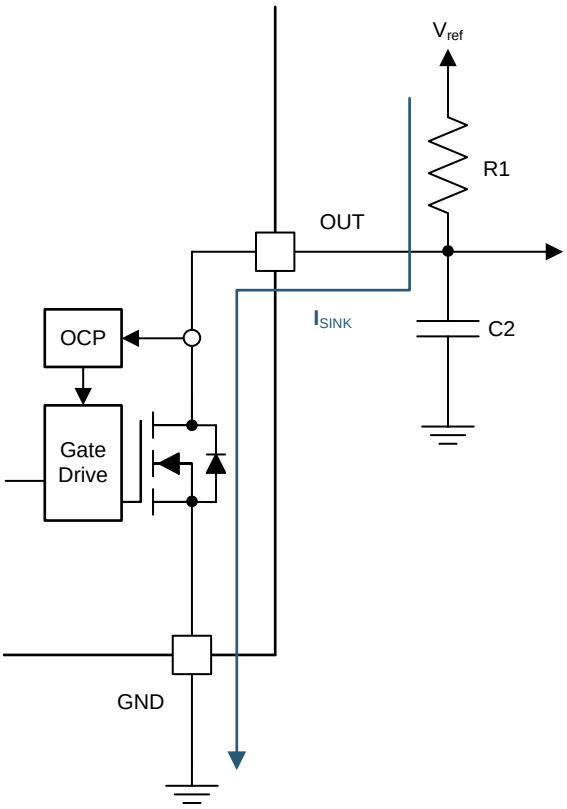


Figure 17.

Select a value for C2 based on the system bandwidth specifications as shown in Equation 2.

$$2 \times f_{BW}\ (\text{Hz}) < \frac{1}{2\pi \times R1 \times C2} \tag{2}$$

Most applications do no require this C2 filtering capacitor.

Feature Description (continued)

7.3.5 Protection Circuits

The DRV5033-Q1 device is fully protected against overcurrent and reverse-supply conditions.

7.3.5.1 Overcurrent Protection (OCP)

An analog current-limit circuit limits the current through the FET. The driver current is clamped to I_{OCP}. During this clamping, the $r_{DS(on)}$ of the output FET is increased from the nominal value.

7.3.5.2 Load Dump Protection

The DRV5033-Q1 device operates at DC V_{CC} conditions up to 38 V nominally, and can additionally withstand V_{CC} = 40 V. No current-limiting series resistor is required for this protection.

7.3.5.3 Reverse Supply Protection

The DRV5033-Q1 device is protected in the event that the V_{CC} pin and the GND pin are reversed (up to –22 V).

NOTE

In a reverse supply condition, the OUT pin reverse-current must not exceed the ratings specified in the *Absolute Maximum Ratings*.

Table 1.

FAULT	CONDITION	DEVICE	DESCRIPTION	RECOVERY
FET overload (OCP)	$I_{SINK} \geq I_{OCP}$	Operating	Output current is clamped to I_{OCP}	$I_O < I_{OCP}$
Load dump	38 V < V_{CC} < 40 V	Operating	Device will operate for a transient duration	$V_{CC} \leq$ 38 V
Reverse supply	–22 V < V_{CC} < 0 V	Disabled	Device will survive this condition	$V_{CC} \geq$ 2.7 V

7.4 Device Functional Modes

The DRV5033-Q1 device is active only when V_{CC} is between 2.7 and 38 V.

When a reverse supply condition exists, the device is inactive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV5033-Q1 device is used in magnetic-field sensing applications.

8.2 Typical Applications

8.2.1 Standard Circuit

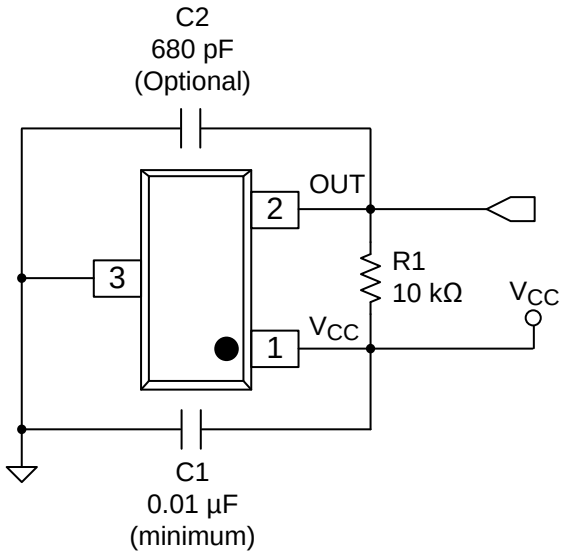


Figure 18. Typical Application Circuit

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	3.2 to 3.4 V
System bandwidth	f_{BW}	10 kHz

8.2.1.2 Detailed Design Procedure

Table 3. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C1	V_{CC}	GND	A 0.01-µF (minimum) ceramic capacitor rated for V_{CC}
C2	OUT	GND	**Optional**: Place a ceramic capacitor to GND
R1	OUT	REF(1)	Requires a resistor pullup

(1) REF is not a pin on the DRV5033-Q1 device, but a REF supply-voltage pullup is required for the OUT pin; the OUT pin may be pulled up to V_{CC}.

8.2.1.2.1 Configuration Example

In a 3.3-V system, 3.2 V ≤ V_{ref} ≤ 3.4 V. Use Equation 3 to calculate the allowable range for R1.

$$\frac{V_{ref}\,max}{30\ mA} \le R1 \le \frac{V_{ref}\,min}{100\ \mu A} \tag{3}$$

For this design example, use Equation 4 to calculate the allowable range of R1.

$$\frac{3.4\ V}{30\ mA} \le R1 \le \frac{3.2\ V}{100\ \mu A} \tag{4}$$

Therefore:

$$113\ \Omega \le R1 \le 32\ k\Omega \tag{5}$$

After finding the allowable range of R1 (Equation 5), select a value between 500 Ω and 32 kΩ for R1.

Assuming a system bandwidth of 10 kHz, use Equation 6 to calculate the value of C2.

$$2 \times f_{BW}\ (Hz) < \frac{1}{2\pi \times R1 \times C2} \tag{6}$$

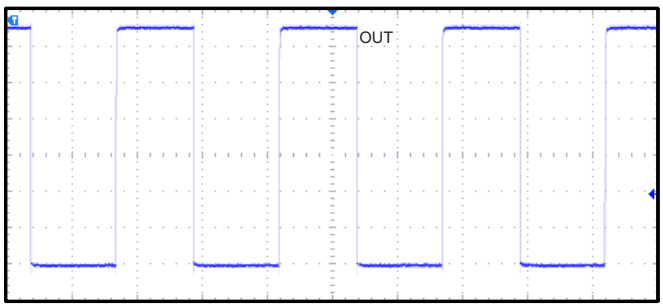
For this design example, use Equation 7 to calculate the value of C2.

$$2 \times 10\ kHz < \frac{1}{2\pi \times R1 \times C2} \tag{7}$$

An R1 value of 10 kΩ and a C2 value less than 820 pF satisfy the requirement for a 10-kHz system bandwidth.

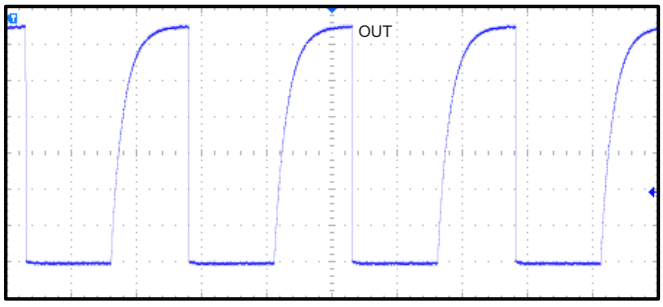
A selection of R1 = 10 kΩ and C2 = 680 pF would cause a low-pass filter with a corner frequency of 23.4 kHz.

8.2.1.3 Application Curves



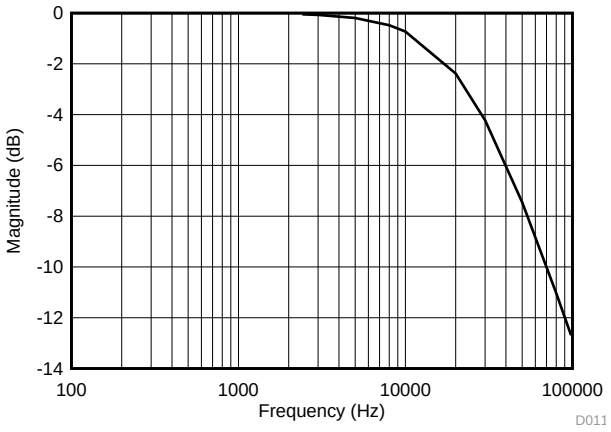
R1 = 10 kΩ pullup No C2

Figure 19. 10-kHz Switching Magnetic Field



R1 = 10-kΩ pullup C2 = 680 pF

Figure 20. 10-kHz Switching Magnetic Field



R1 = 10-kΩ pullup C2 = 680 pF

Figure 21. Low-Pass Filtering

8.2.2 Alternative Two-Wire Application

For systems that require minimal wire count, the device output can be connected to V_{CC} through a resistor, and the total supplied current can be sensed near the controller.

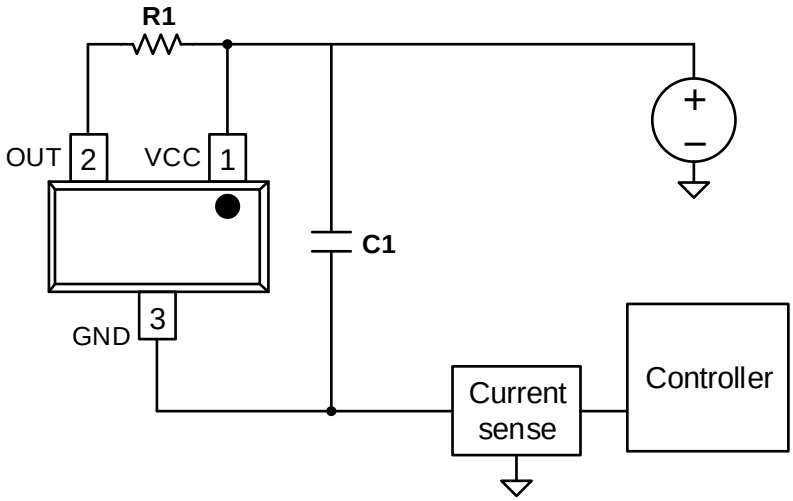


Figure 22. 2-Wire Application

Current can be sensed using a shunt resistor or other circuitry.

8.2.2.1 Design Requirements

Table 4 lists the related design parameters.

Table 4. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	12 V
OUT resistor	R1	1 kΩ
Bypass capacitor	C1	0.1 µF
Current when B < B_{RP}	$I_{RELEASE}$	About 3 mA
Current when B > B_{OP}	$I_{OPERATE}$	About 15 mA

8.2.2.2 Detailed Design Procedure

When the open-drain output of the device is high-impedance, current through the path equals the I_{CC} of the device (approximately 3 mA).

When the output pulls low, a parallel current path is added, equal to V_{CC} / (R1 + $r_{DS(on)}$). Using 12 V and 1 kΩ, the parallel current is approximately 12 mA, making the total current approximately 15 mA.

The local bypass capacitor C1 should be at least 0.1 µF, and a larger value if there is high inductance in the power line interconnect.

9 Power Supply Recommendations

The DRV5033-Q1 device is designed to operate from an input voltage supply (VM) range between 2.7 and 38 V. A 0.01-µF (minimum) ceramic capacitor rated for V_{CC} must be placed as close to the DRV5033-Q1 device as possible.

10 デバイスおよびドキュメントのサポート

10.1 デバイス・サポート

10.1.1 デバイスの項目表記

DRV5033-Q1のデバイス名の各部の読み方を図 23に示します。

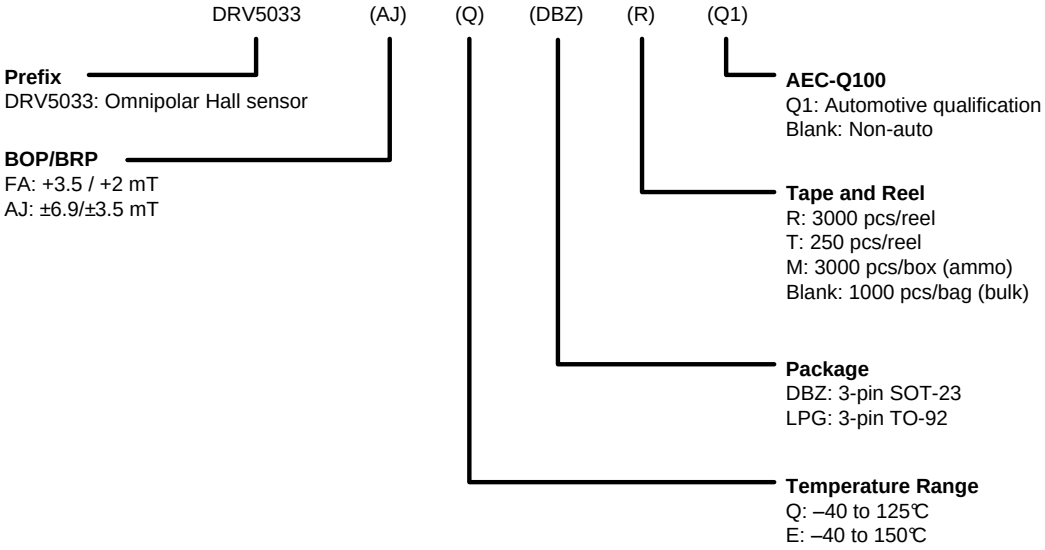


図 23. デバイスの項目表記

10.1.2 デバイスのマーキング

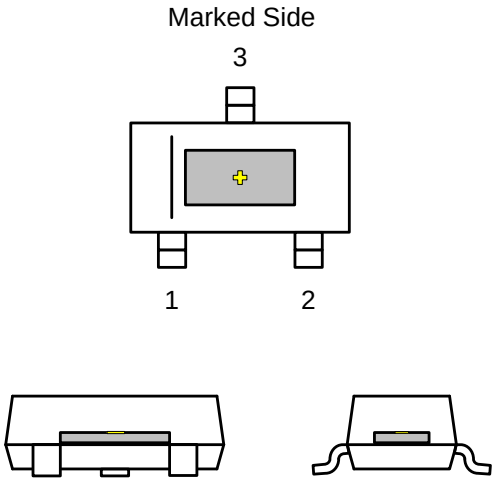


図 **24. SOT-23 (DBZ)**パッケージ

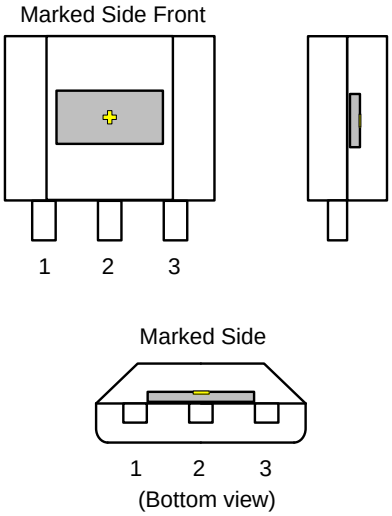


図 **25. TO-92 (LPG)**パッケージ

✚はホール効果センサを示します(実際の大きさに比例してはいません)。ホール素子はパッケージの中心に、許容誤差±100µmで配置されています。ホール素子の高さは、パッケージの底面から計測して、DBZパッケージでは0.7mm±50µm、LPGパッケージでは0.987mm±50µmです。

10.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.3 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

10.4 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

10.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV5033AJEDBZRQ1	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	+QJAJ
DRV5033AJEDBZRQ1.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	+QJAJ
DRV5033AJEDBZTQ1	Obsolete	Production	SOT-23 (DBZ) | 3	-	-	Call TI	Call TI	-40 to 150	+QJAJ
DRV5033AJELPGMQ1	Active	Production	TO-92 (LPG) | 3	3000 | AMMO	Yes	SN	N/A for Pkg Type	-40 to 150	+QJAJ
DRV5033AJELPGMQ1.A	Active	Production	TO-92 (LPG) | 3	3000 | AMMO	Yes	SN	N/A for Pkg Type	-40 to 150	+QJAJ
DRV5033AJELPGQ1	Active	Production	TO-92 (LPG) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	-40 to 150	+QJAJ
DRV5033AJELPGQ1.A	Active	Production	TO-92 (LPG) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	-40 to 150	+QJAJ
DRV5033AJQDBZRQ1	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	+QKAJ
DRV5033AJQDBZRQ1.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	+QKAJ
DRV5033AJQDBZTQ1	Obsolete	Production	SOT-23 (DBZ) | 3	-	-	Call TI	Call TI	-40 to 125	+QKAJ
DRV5033AJQLPGMQ1	Active	Production	TO-92 (LPG) | 3	3000 | AMMO	Yes	SN	N/A for Pkg Type	-40 to 125	+QKAJ
DRV5033AJQLPGMQ1.A	Active	Production	TO-92 (LPG) | 3	3000 | AMMO	Yes	SN	N/A for Pkg Type	-40 to 125	+QKAJ
DRV5033AJQLPGQ1	Active	Production	TO-92 (LPG) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	-40 to 125	+QKAJ
DRV5033AJQLPGQ1.A	Active	Production	TO-92 (LPG) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	-40 to 125	+QKAJ
DRV5033FAEDBZRQ1	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	+QJFA
DRV5033FAEDBZRQ1.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	+QJFA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF DRV5033-Q1 :

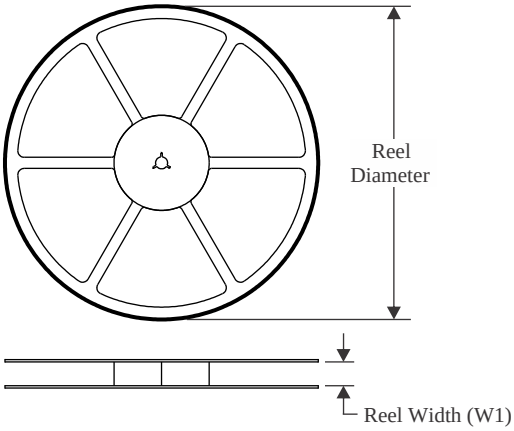
- Catalog : DRV5033

NOTE: Qualified Version Definitions:

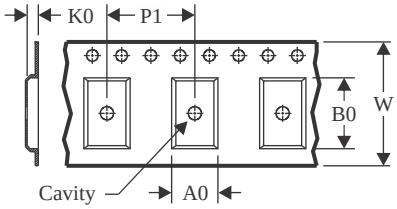
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

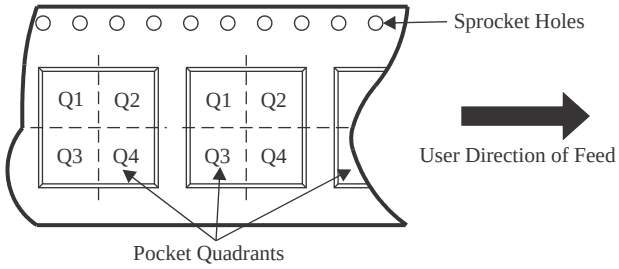


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

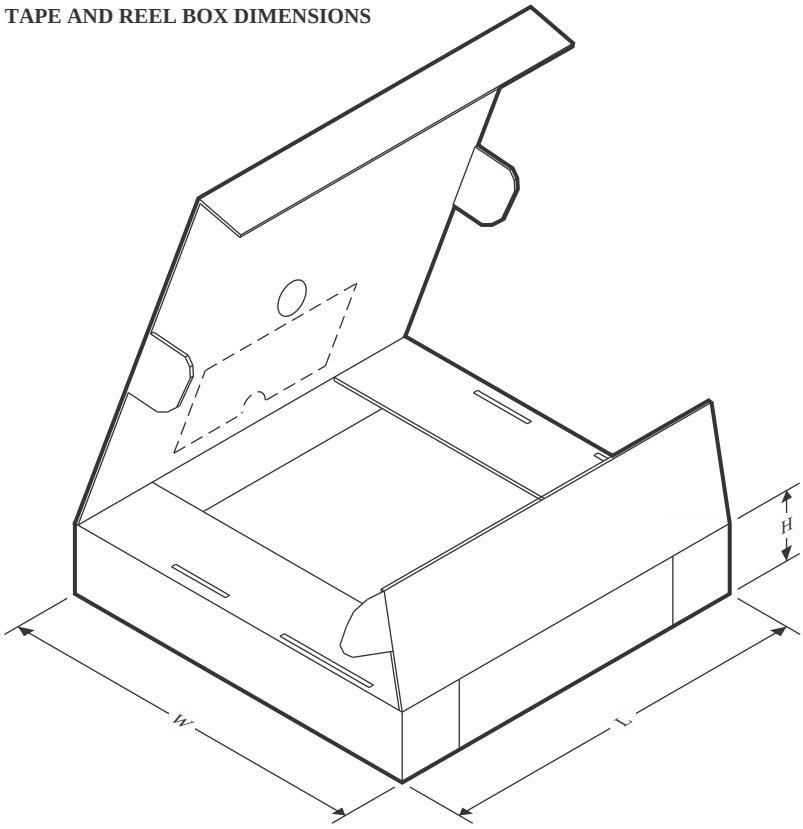
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV5033AJEDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5033AJQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5033FAEDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

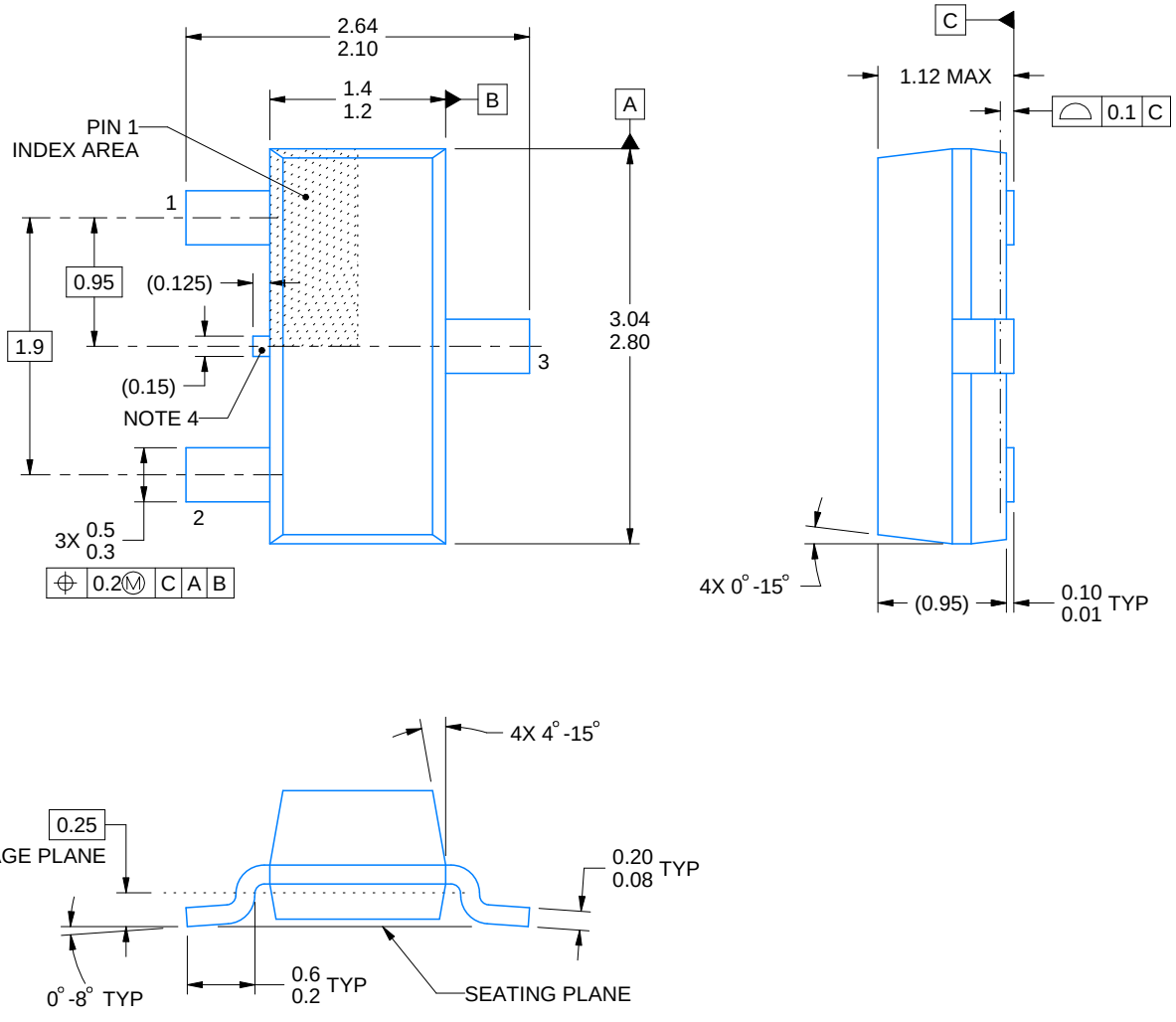
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV5033AJEDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5033AJQDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5033FAEDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

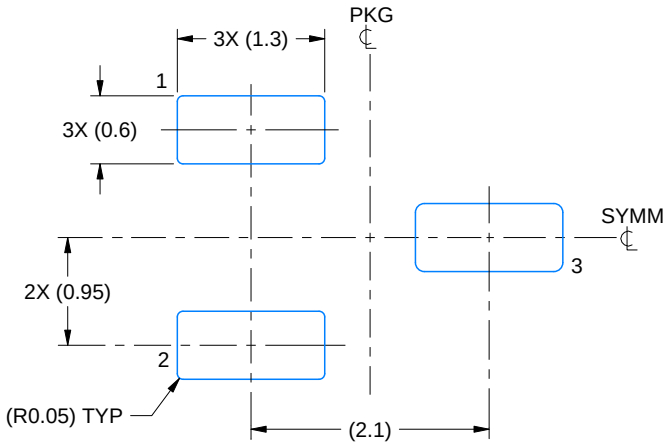
SMALL OUTLINE TRANSISTOR



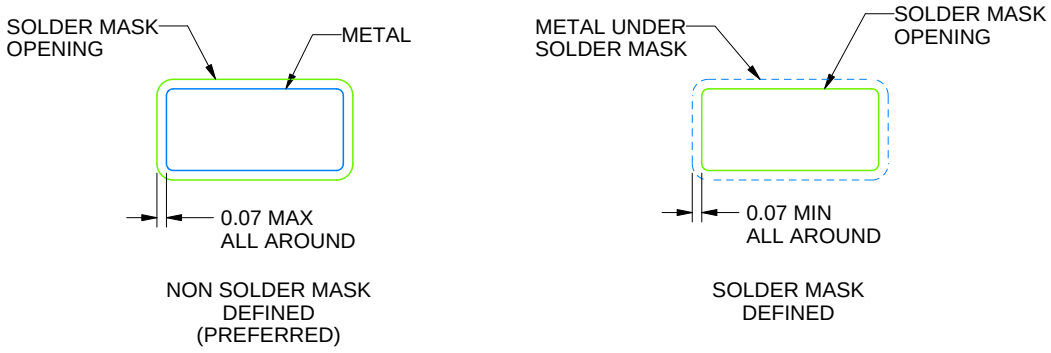
4214838/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X

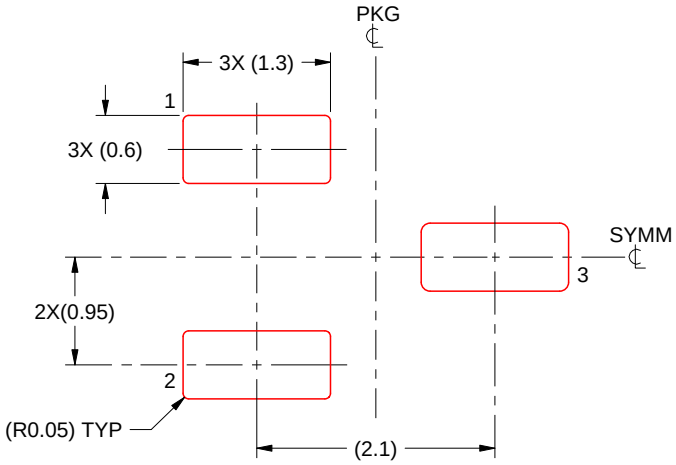


SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

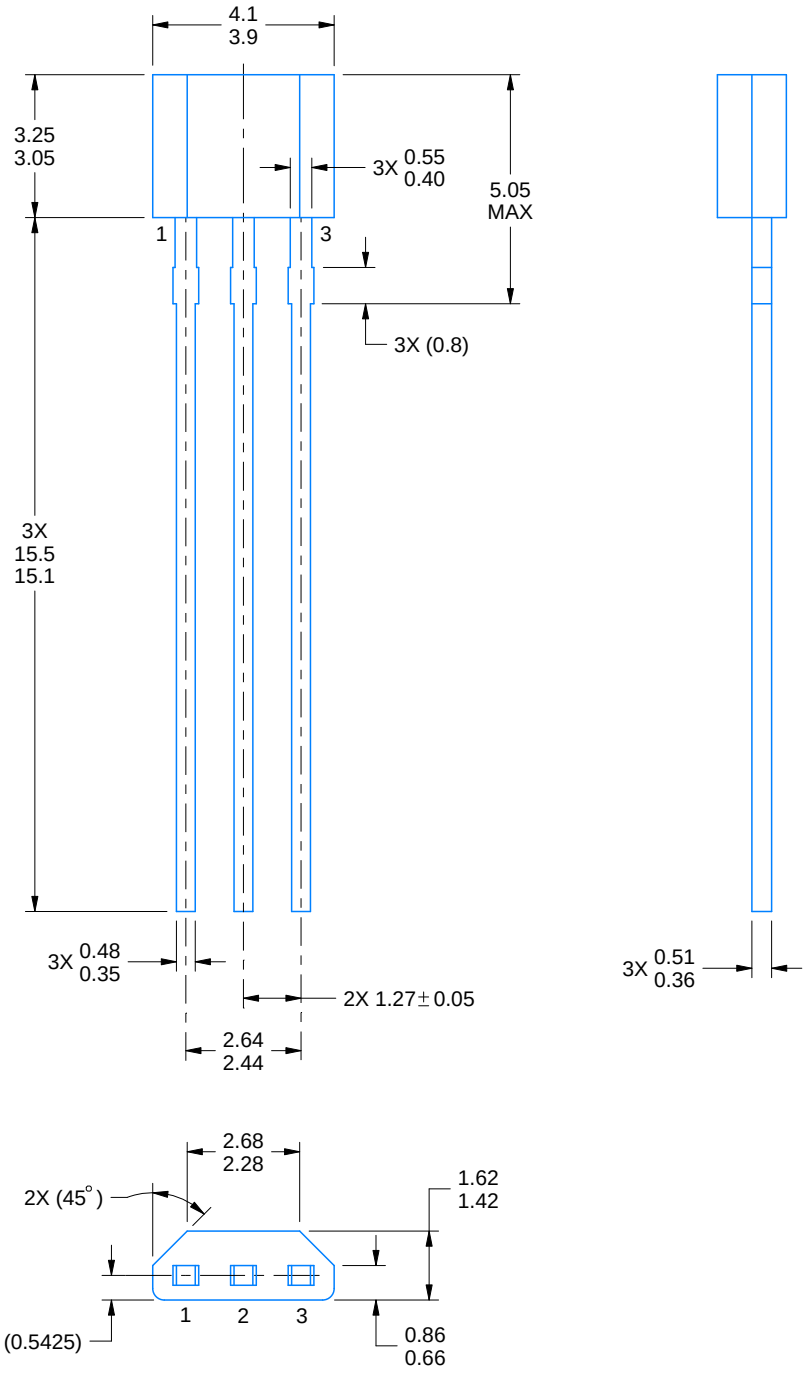
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

LPG0003A

TO-92 - 5.05 mm max height

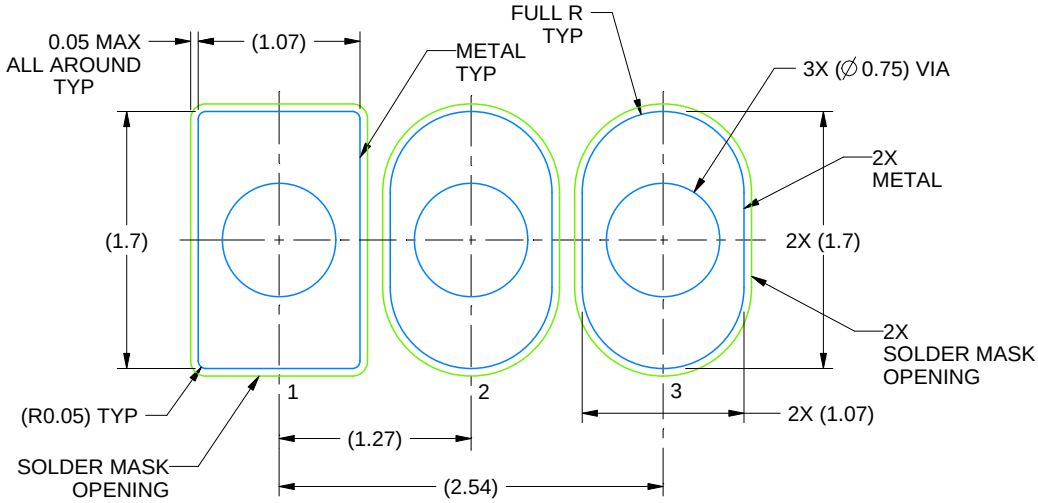
TRANSISTOR OUTLINE



4221343/C 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X

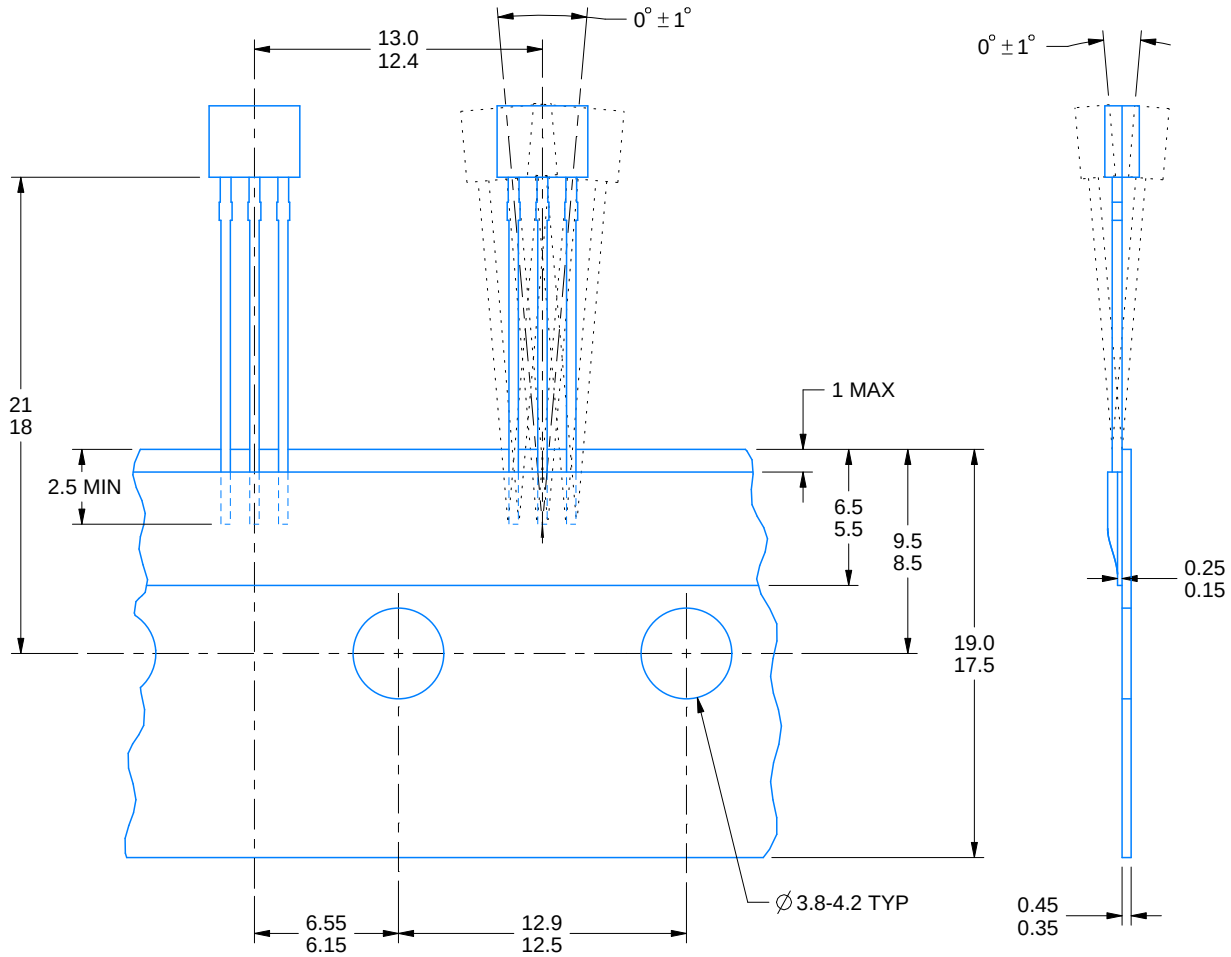
4221343/C 01/2018

TAPE SPECIFICATIONS

LPG0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



4221343/C 01/2018

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