TEXAS INSTRUMENTS
DRV3205-Q1
JAJSC41E – SEPTEMBER 2015 – REVISED FEBRUARY 2017

DRV3205-Q1 車載、三相ゲート・ドライバ、3個の電流シャント・アンプ内蔵、保護、診断、監視機能を強化

1 特長

- 車載アプリケーション用にAEC-Q100認定済み:
  - デバイス温度グレード1: 動作時周囲温度–40℃～+125℃
- モーター制御用の三相ブリッジ・ドライバ
- 12Vおよび24Vアプリケーション向け
- 3個の高精度電流センス・アンプを内蔵
- 昇圧コンバータ内蔵、最小4.75Vでのゲート駆動
- 6個の独立したNチャネル・パワーMOSFETを駆動
- 大電流FET向けの強力な1Aゲート・ドライバ
- プログラム可能なデッド・タイム
- PWM周波数：最大20kHz
- 100%デューティ・サイクルでの動作をサポート
- 短絡保護付き
  - VDS監視（検出レベルを調整可能）
  - シャント電流制限（検出レベルを調整可能）
- 過電圧および低電圧保護
- 過熱警告およびシャットダウン
- SPIによる高度な障害検出および処理
- システム監視
  - Q&Aウォッチドッグ
  - I/O電源の監視
  - ADREFの監視
- 内部的なフォルト診断をプログラム可能
- スリープ・モード機能
- 熱特性が強化された48ピンHTQFP PowerPAD™ICパッケージ(7-mm × 7-mm本体)

2 アプリケーション

- 車載用モーター制御アプリケーション
  - 電動パワー・ステアリング（EPS、EHPS）
  - 電気式ブレーキおよびブレーキ・アシスト
  - トランスミッション
  - ポンプ
- 産業用モーター制御アプリケーション

3 概要

DRV3205-Q1ブリッジ・ドライバは、車載用の三相ブラシレスDCモータの制御アプリケーションに特化した設計です。このデバイスには、標準レベルのNチャネルMOSFETトランジスタ専用のドライバが6つ搭載されています。FETが内蔵された昇圧コンバータにより、オーバードライブ電圧が供給され、最低4.75Vの低いバッテリ電圧でも、電源段の完全な制御が可能です。ドライバが強力なことから、大電流のアプリケーションに適しており、ピーク出力電流を制限するようプログラム可能です。

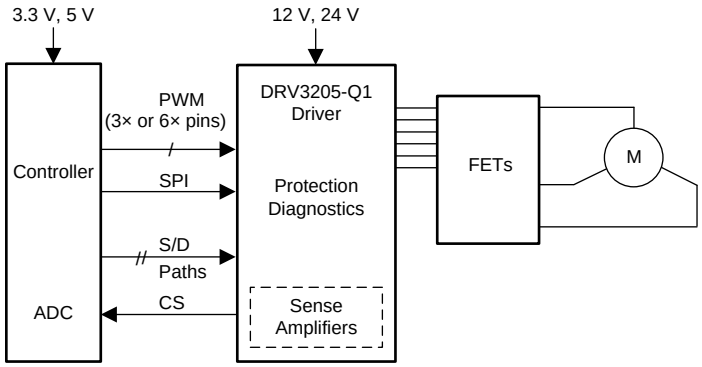
このデバイスには強固なFET保護と、Q&Aウォッチドッグや、I/O電源およびADC基準電圧の電圧監視などのシステム監視機能が組み込まれています。内蔵の内部診断機能は、SPIインターフェイスによりアクセスやプログラムが可能です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
DRV3205-Q1	HTQFP（48）	7.00mm×7.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

代表的なアプリケーションの図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (November 2016) から **Revision E** に変更 **Page**

- Added the propagation delay graphs to the *Typical Characteristics* section ... 15
- Changed the note on the *Single 8-Bit SPI Frame/Transfer* figure ... 17
- Updated the *Typical Application Diagram* figure ... 22

Revision C (October 2016) から **Revision D** に変更 **Page**

- Changed the maximum value for the RVSET resistor error detection parameter (4.4.31) from 1.5 to 1.4 kΩ in the *Electrical Characteristics* table ... 10
- Changed the units and symbol for the RVSET output voltage parameter (4.4.32–4.4.34), and fixed duplicate position number for T_J = 25°C and 125°C in the *Electrical Characteristics* table ... 10
- Added characterization note to parameters 5.7 and 5.29 through 5.30e in the *Electrical Characteristics* table ... 11
- Deleted the VS voltage range test condition from the boost output voltage parameter (6.1) in the *Electrical Characteristics* table ... 12
- Added new test condition to the switching frequency parameter (6.3) and add new values for switching frequency at V_S < 6 (6.31) in the *Electrical Characteristics* table ... 12
- Changed the maximum value for the input pulldown resistor at EN pin parameter (7.4) from 300 to 360 kΩ in the *Electrical Characteristics* table ... 12
- Changed the position number for the output high and low voltage 2 parameters in the *Electrical Characteristics* table ... 12
- Added characterization note to parameters 13.2 through 13.11 in the *Serial Peripheral Interface Timing Requirements* table ... 14

Revision B (October 2016) から **Revision C** に変更 **Page**

- Clarified the temperature for the BOOST pin quiescent current parameters (3.6B and 3.6C) and added new temperature condition (3.62B and 3.61C) in the *Recommended Operating Conditions* table ... 7
- Deleted the maximum value for the input hysteresis parameters (7.3 and 7.3A) in the *Electrical Characteristics* table ... 12
- Changed the values for the input pullup resistance parameter (7.5) in the *Electrical Characteristics* table ... 12

Revision A (October 2016) から Revision B に変更 **Page**

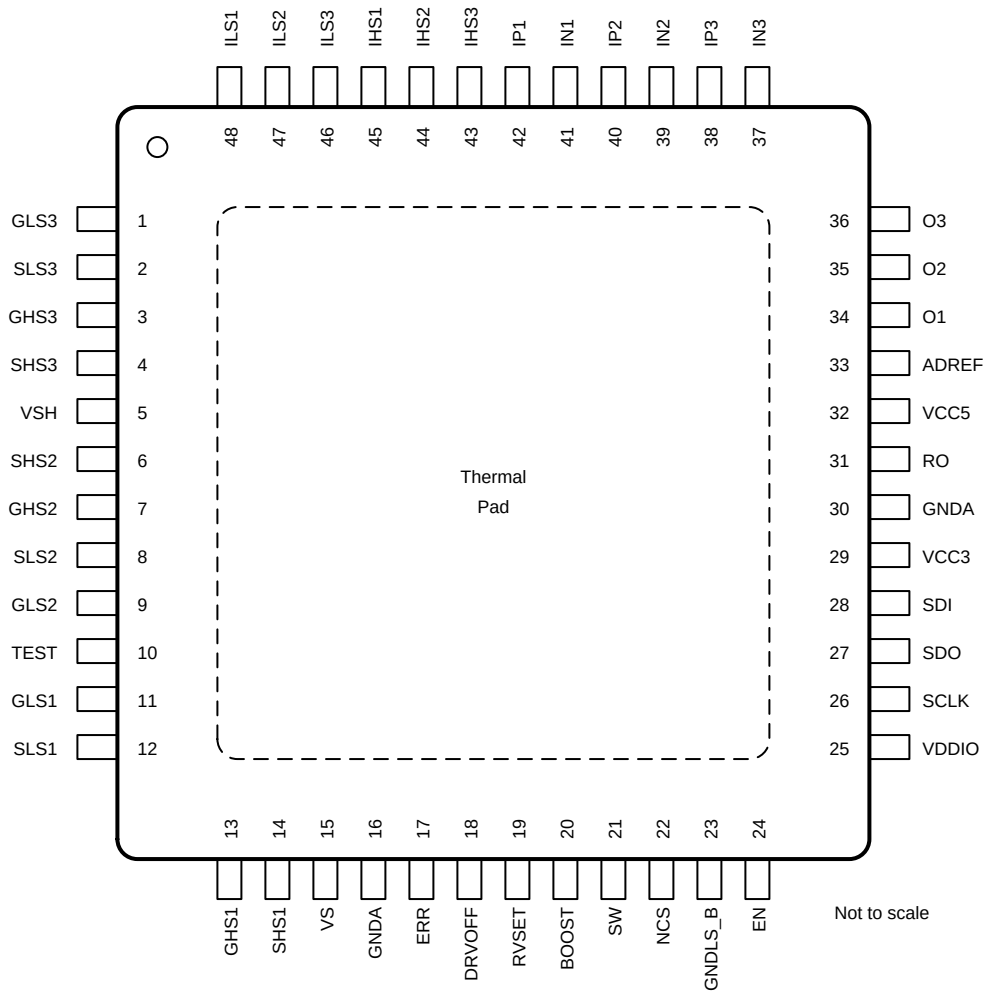
- *「特長」セクション*でAEC-Q1100をAEC-Q100へ 変更 1
- Changed the maximum value for the VCC5 and VCC3 short-to-ground current from 70 to 80 mA in the *Absolute Maximum Ratings* table 6
- Changed the minimum value for the high-side/low-side driver shutdown current parameter from 7 to 2 mA in the *Electrical Characteristics* table 11

2016年9月発行のものから更新 **Page**

- *デバイスのステータスを製品プレビューから量産データへ* 変更..... 1

5 Pin Configuration and Functions

PHP PowerPAD™ Package
48-Pin HTQFP
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	GLS3	PWR	Gate low-side 3, connected to gate of external power MOSFET.
2	SLS3	PWR	Source low-side 3, connected to external power MOSFET for gate discharge and VDS monitoring.
3	GHS3	PWR	Gate high-side 3, connected to gate of external power MOSFET.
4	SHS3	PWR	Source high-side 3, connected to external power MOSFET for gate discharge and VDS monitoring.
5	VSH	HVI_A	Sense high-side, sensing VS connection of the external power MOSFETs for VDS monitoring.
6	SHS2	PWR	Source high-side 2, connected to external power MOSFET gate discharge and VDS monitoring.
7	GHS2	PWR	Gate high-side 2, connected to gate of external power MOSFET.
8	SLS2	PWR	Source low-side 2, connected to external power MOSFET for gate discharge and VDS monitoring.
9	GLS2	PWR	Gate low-side 2, connected to gate of external power MOSFET.
10	TEST	HVI_A	Test mode input, during normal application connected to ground.

(1) Description of pin type: GND = Ground; HVI_A = High-voltage input analog; HVI_D = High-voltage input digital; LVI_A = Low-voltage input analog; LVO_A = Low-voltage output analog; LVO_D = Low-voltage output digital; NC = No connect; PWR = Power output; Supply = Supply input

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
11	GLS1	PWR	Gate low-side 1, connected to gate of external power MOSFET.
12	SLS1	PWR	Source low-side 1, connected to external power MOSFET for gate discharge and VDS monitoring.
13	GHS1	PWR	Gate high-side 1, connected to gate of external power MOS transistor.
14	SHS1	PWR	Source high-side 1, connected to external power MOS transistor for gate discharge and VDS.
15	VS	Supply	Power-supply voltage (externally protected against reverse battery connection).
16	GNDA	GND	Analog ground.
17	ERR	LVO_D	Error (low active), Error pin to indicate detected error.
18	DRVOFF	HVI_D	Driver OFF (high active), secondary bridge driver disable.
19	RVSET	HVI_A	VDDIO / ADREF OV/UV configuration resister.
20	BOOST	Supply	Boost output voltage, used as supply for the gate drivers.
21	SW	PWR	Boost converter switching node connected to external coil and external diode.
22	NCS	HVI_D	SPI chip select.
23	GNDLS_B	GND	Boost GND to set current limit. Boost switching current goes through this pin through external resistor to ground.
24	EN	HVI_D	Enable (high active) of the device.
25	VDDIO	Supply	I/O supply voltage, defines the interface voltage of digital I/O, for example, SPI.
26	SCLK	HVI_D	SPI clock.
27	SDO	LVO_D	SPI data output.
28	SDI	HVI_D	SPI data input.
29	VCC3	LVO_A	VCC3 regulator, for internal use only. TI recommends an external decoupling capacitor of 0.1 µF. External load < 100 µA.
30	GNDA	GND	Analog ground.
31	RO	LVO_A	Analog output.
32	VCC5	LVO_A	VCC5 regulator, for internal use only. Recommended external decoupling capacitor 1 µF. External load < 100 µA.
33	ADREF	LVI_A	ADC reference of MCU, used as maximum voltage clamp for O1 to O3.
34	O1	LVO_A	Output current sense amplifier 1.
35	O2	LVO_A	Output current sense amplifier 2.
36	O3	LVO_A	Output current sense amplifier 3.
37	IN3	LVI_A	Current sense negative input 3.
38	IP3	LVI_A	Current sense positive input 3.
39	IN2	LVI_A	Current sense input N 2.
40	IP2	LVI_A	Current sense input P 2.
41	IN1	LVI_A	Current sense input N 1.
42	IP1	LVI_A	Current sense input P 1.
43	IHS3	HVI_D	High-side input 3, digital input to drive the HS3.
44	IHS2	HVI_D	Input HS 2, digital input to drive the HS2.
45	IHS1	HVI_D	Input HS 1, digital input to drive the HS1.
46	ILS3	HVI_D	Low-side input 3, digital input to drive the LS3.
47	ILS2	HVI_D	Input LS 2, digital input to drive the LS2.
48	ILS1	HVI_D	Input LS 1, digital input to drive the LS1.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

POS				MIN	MAX	UNIT
2.1	VS, VSH	DC voltage		–0.3	60	V
2.1a	VS	DC voltage	Negative voltages with minimum serial resistor 5 Ω, T_A = 25°C	–5		V
2.1b	VSH	DC voltage	Negative voltages with minimum serial resistor 10 Ω, T_A = 25°C	–5		V
2.1c	VS	DC voltage	Negative voltages with minimum serial resistor 5 Ω, T_A = 105°C	–2.5		V
2.1d	VSH	DC voltage	Negative voltages with minimum serial resistor 10 Ω, T_A = 105°C	–2.5		V
2.2A	GHSx	Gate high-side voltage		–9	70	V
2.2B	SHSx	Source high-side voltage		–9	70	V
2.3	GHSx-SHSx	Gate-source high-side voltage difference	Externally driven, internal limited, see position 5.4 in *Electrical Characteristics*	–0.3	15	V
2.4	GLSx	Gate low-side voltage		–9	20	V
2.5	SLSx	Source low-side voltage		–9	7	V
2.6	GLSx-SLSx	Gate-source low-side voltage difference	Externally driven, internal limited, see position 5.5 in *Electrical Characteristics*	–0.3	15	V
2.7	BOOST, SW	Boost converter		–0.3	70	V
2.8	INx, IPx	Current sense input voltage		–9	7	V
2.8A	INx, IPx	Current sense input current	Clamping current	–5	5	mA
2.8C	Ox	Current sense output voltage		–0.3	ADREF +0.3	V
2.8D	Ox	Forced input current		–10	10	mA
2.9	VDDIO	Analog input voltage		–0.3	60	V
2.9a	ADREF	Analog input voltage		–0.3	60	V
2.10	ILSx,IHSx, EN, DRVOFF, SCLK, NCS, SDI	Digital input voltage		–0.3	60	V
2.11	RVSET	Analog input voltage		–0.3	60	V
2.13	GNDA, GNDLS_B	Difference between GNDA and GNDLS_B		–0.3	0.3	V
2.20		Maximum slew rate of SHSx pins, SR_{SHS}		–250	250	V/µs
2.21	ERR, SDO, RO	Analog and digital output voltages		–0.3	6	V
2.21 A	ERR, SDO, RO	Forced input/output current		–10	10	mA
2.22	TEST	Unused pins. Connect to GND.		–0.3	0.3	V
2.24	VCC5	Internal supply voltage		–0.3	6	V
2.24 A		Short-to-ground current, I_{VCC5}(3)	Internal current limit		80	mA
2.25	VCC3	Internal supply voltage		–0.3	3.6	V
2.26		Short-to-ground current, I_{VCC3}	Limited by VCC5		80	mA
2.27		Driver FET total gate charge (per FET), Q_{gmax}	VS = 12 V, f_{PWM} = 20 kHz, 6 FETs ON/OFF per PWM cycle		200(4)	nC
2.28			VS = 24 V, f_{PWM} = 20 kHz, 6 FETs ON/OFF per PWM cycle		100(4)	nC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal, unless specified otherwise.
(3) I_{VCC5} is not specifying VCC5 output current capability for external load. The allowed external load on VCC5 is specified at position 3.18 in *Recommended Operating Conditions*.
(4) The maximum value also depends on PCB thermal design, modulation scheme, and motor operation time.

Absolute Maximum Ratings (continued)

over operating free-air temperature range (unless otherwise noted)(1)(2)

POS			MIN	MAX	UNIT
2.14		Operating virtual junction temperature, T_J	–40	150	°C
2.15		Storage temperature, T_{stg}	–55	165	°C

6.2 ESD Ratings

POS				VALUE	UNIT
2.17	$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
			Pins 4, 6, and 14	±4000	
2.18		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
2.19			Corner pins (1, 12, 13, 24, 25, 36, 37, and 48)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

POS				MIN	NOM	MAX	UNIT
3.1	VS	Supply voltage, normal voltage operation	Full device functionality. Operation at VS = 4.75 V only when coming from higher VS. Minimum VS for startup = 4.85 V	4.75		40	V
3.2	VSLO	Supply voltage, logic operation	Logic functional (during battery cranking after coming from full device functionality)	4		40	V
3.3	VDDIO	Supply voltage for digital I/Os		2.97		5.5	V
3.4	D	Duty cycle of bridge drivers		0%		100%	
3.5	f_{PWM}	PWM switching frequency		0		22(1)	kHz
3.6A	I_{VSn}	VS quiescent current normal operation (boost converter enabled, drivers not switching)	Boost converter enabled, see and for SHSx/SLSx connections. EN_GDBIAS = 1			22	mA
3.61A	I_{VSn}	VS quiescent current normal operation (boost converter enabled, drivers not switching)	Boost converter enabled, see and for SHSx/SLSx connections. EN_GDBIAS = 0			22.3	mA
3.6B	I_{BOOSTn}	BOOST pin quiescent current normal operation (drivers not switching)	4.75 V < VS < 20 V, T_A = 25°C to 125°C			9	mA
3.62B			4.75 V < VS < 20 V, T_A = –40°C			10	mA
3.61B	I_{VSn}	VS quiescent additional current normal operation because of RVSET thermal voltage output enabled (boost converter enabled, drivers not switching)	THERMAL_RVSET_EN = 1			0.6	
3.6C	I_{BOOSTn}	BOOST pin quiescent current normal operation (drivers not switching)	20 < VS < 40 V, T_A = 25°C to 125°C			9.5	mA
3.61C			20 < VS < 40 V, T_A = –40°C			10.5	
3.6D	$I_{BOOST,sw}$	BOOST pin additional load current because of switching gate drivers	Excluding FET gate charge current. 20-kHz all gate drivers switching at the same time. EN_GDBIAS = 1			4	mA
3.61D	$I_{BOOST,sw}$	BOOST pin additional load current because of switching gate drivers	Excluding FET gate charge current. 20-kHz all gate drivers switching at the same time. EN_GDBIAS = 0			5.4	mA
3.75	I_{VSq_1}	VS quiescent current shutdown (sleep mode) 1	VS = 14 V, no operation, T_J < 25°C, EN = Low, total leakage current on all supply connected pins			20	µA
3.75a	I_{VSq_2}	VS quiescent current shutdown (sleep mode) 2	VS = 14 V, no operation, T_J < 85°C, EN = Low, total leakage current on all supply connected pins			30	µA
3.8	T_J	Junction temperature		–40		150	°C
3.9	T_A	Operating ambient free-air temperature	With proper thermal connection	–40		125	°C
3.11	V_{INx},V_{IPx}	Current sense input voltage	V_{IPx} – V_{Inx}, RO = 2.5 V GAIN = 12	–0.15		0.15	V
3.13	ADREF	Clamping voltage for current sense amplifier outputs O1/2/3		2.97		5.5	V
3.13a		Reserved					V

(1) Maximum PWM allowed also depends on maximum operating temperature, FET gate charge current, VS supply voltage, modulation scheme, and PCB thermal design.

Recommended Operating Conditions (continued)

POS				MIN	NOM	MAX	UNIT
3.13b		Reserved					V
3.14	VCC3	Internal supply voltage	VS > 4 V, external load current <100 µA, decoupling capacitor typical 0.1 µF	3(1)		3.3	V
3.15	I_{VCC3}	VCC3 output current	Intended for MCU ADC input	0		100	µA
3.16	C_{VCC3}	VCC3 decoupling capacitance		0.075	0.1	0.2	µF
3.17	VCC5	Internal supply voltage	VS > 6 V, external load current < 100 µA, decoupling capacitor typical 1 µF	5.15		5.45	V
3.18	I_{VCC5}	VCC5 output current	Intended for MCU ADC input	0		100	µA
3.19	C_{VCC5}	VCC5 decoupling capacitance		0.5	1	1.5	µF

6.4 Thermal Information

THERMAL METRIC(1)		DRV3205-Q1 PHP (HTQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over operating temperature T_J = –40°C to 150°C and recommended operating conditions, VS = 4.75 V to 40 V(1), f_{PWM} < 20 kHz (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.1	**CURRENT SENSE AMPLIFIER**						
4.2.1	V_{off1a}	Initial input offset of amplifiers	T_J = 25°C, ADREF = 5 V, RO_CFG [4:0] = 5'b11000: ADREF × 25 / 50		±1		mV
4.2.1a	V_{off1a}	Initial input offset of amplifiers	T_J = 25°C, ADREF = 3.3 V, RO_CFG [4:0] = 5'b11000: ADREF × 25 / 50		±1		mV
4.2.2	V_{off1b}	Temperature and aging offset(2)	ADREF = 5 V, RO_CFG [4:0] = 5'b11000: ADREF × 25 / 50		±1		mV
4.2.2a	V_{off1b}	Temperature and aging offset(2)	ADREF = 3.3 V, RO_CFG [4:0] = 5'b11000: ADREF × 25 / 50		±1		mV
4.2.3	V_{com1}(3)	Input common voltage range		–3		3	V
4.2.4	V_{Oa}	Nominal output voltage level, positive ox swing	Normal voltage operation, VS ≥ 5.75 V; 0.5-mA load current	ADREF – 0.5 + V_{oxm}			V
4.2.4a	V_{Oa}	Nominal output voltage level, negative ox swing	Normal voltage operation, VS ≥ 5.75 V; 0.5-mA load current			0.5	V
4.2.4b	V_{Oa}	Nominal output voltage level 2, positive ox swing	Normal voltage operation, VS ≥ 5.75 V; 10-µA load current	ADREF – 0.06 + V_{oxm}			V
4.2.4c	V_{Oa}	Nominal output voltage level 2, negative ox swing	Normal voltage operation, VS ≥ 5.75 V; 10-µA load current			0.09	V
4.2.5	V_{Ob}	Output voltage level during low voltage operation, positive ox swing	Low voltage operation, 4.75 V ≤ VS < 5.75 V; 0.5-mA load current	VS – 1.25; ADREF – 0.5 + V_{oxm}			V
4.2.5a	V_{Ob}	Output voltage level during low voltage operation, negative ox swing	Low voltage operation, 4.75 V ≤ VS < 5.75 V; 0.5-mA load current			0.5	V

(1) Product life time depends on VS voltage, PCB thermal design, modulation scheme, and motor operation time. The product is designed for 12-V and 24-V battery system.
(2) Ensured by characterization.
(3) ADREF / VDDIO overvoltage and undervoltage is set by RVSET.

Electrical Characteristics (continued)

over operating temperature T_J = –40°C to 150°C and recommended operating conditions, VS = 4.75 V to 40 V[1], f_{PWM} < 20 kHz (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.2.5b	V_{Ob}	Output voltage level during low voltage operation 2, positive ox swing	Low voltage operation, 4.75 V ≤ VS < 5.75 V; 10-µA load current	VS – 0.75; ADREF – 0.06 + V_{oxm}			V
4.2.5c	V_{Ob}	Output voltage level during low voltage operation 2, negative ox swing	Low voltage operation, 4.75 V ≤ VS < 5.75 V; 10-µA load current			0.09	V
4.2.6	GBP	Gain bandwidth product GBP	0.5 V ≤ O1/2/3 ≤ 4.5 V, capacitor load = 25 pF, specified by design.	5			MHz
4.2.8	G1	Gain 1	SPI configurable, Normal voltage operation, VS ≥ 5.75 V; 0.5-mA load current	7.896	8	8.096	V/V
4.2.9	G2	Gain 2	SPI configurable, Normal voltage operation, VS ≥ 5.75 V; 0.5-mA load current	11.856	12	12.144	V/V
4.2.10	G3	Gain 3	SPI configurable, Normal voltage operation, VS ≥ 5.75 V; 0.5-mA load current	15.808	16	16.192	V/V
4.2.11	G4	Gain 4	SPI configurable, Normal voltage operation, VS ≥ 5.75 V; 0.5-mA load current	31.616	32	32.384	V/V
4.2.12	$PSRR_{o123}$	Power supply rejection ratio at DC	VS to O1/2/3 decoupling capacitor typical 1 µF on VCC5 / 0.1-µF VCC3 at DC Specified by design, capacitor load = 25 pF RO = 2.5 V, ADREF = 5 V, gain = 16, dVS / dOx dVCC5 / dOx	60	80		dB
4.2.12a	$CMRR_{o123}$	Common mode rejection ratio at DC	Specified by design, capacitor load = 25 pF RO = 2.5 V, ADREF = 5 V, gain = 1, VS = 12 V	70	80		dB
4.2.12b	CMG_{o123}	Common mode gain at 500 kHz	Specified by design, capacitor load = 25 pF RO = 2.5 V, ADREF = 5 V, gain = 16			–29	dB
4.2.12c	CMG_{o123}	Common mode gain peak	Specified by design, capacitor load = 25 pF RO = 2.5 V, ADREF = 5 V, gain = 16			–15	dB
4.2.13	Iinamp	Inx, IPx input bias current	VCM (input common mode voltage) = ±3 V, RSHUNT_MODE[1:0] = 11		50	90	µA
4.2.13	Iinamp2	Inx, IPx input bias current	VCM (input common mode voltage) = ±3 V, RSHUNT_MODE[1:0] = 2'b000110		60	90	µA
4.2.14	$Tsettle_{O123}$	Ox settling time to withing ±2% of final value	Specified by design, capacitor load = 25 pF, RO = 2.5 V, ADREF = 5 V, gain = 16, 0.5 V ≤ O1/2/3 ≤ 4.5 V			0.8	µs
4.2.15	Iinampd	Inx, IPx Input bias differential current	VCM = ±3 V $I_{IPx-INx}$, IPx-INx = 0 V, RSHUNT_MODE[1:0] = 11	–1.2		1.2	µA
4.2.16	Rinam	Inx, IPx Input resistance	VCM = ±3 V	9	12	15	kΩ
4.2.12d	$PSRR3_{o123}$	Power supply rejection ratio at DC	VS to O1/2/3 decoupling capacitor typical 1 µF on VCC5 / 0.1-µF VCC3 at DC specified by design, capacitor load = 25 pF RO = 1.65 V ADREF = 3.3 V, gain = 16, dVS / dOx dVCC5 / dOx	70	80		dB
4.2.12e	$CMRR_{3o123}$	Common mode rejection ratio at DC	Specified by design, capacitor load = 25 pF RO = 1.65 V ADREF = 3.3 V, gain = 16 VS = 12 V	70	80		dB
4.2.12f	$CMG3_{o123}$	Common mode gain at 500 kHz	Specified by design, capacitor load = 25 pF RO = 1.65 V ADREF = 3.3 V, gain = 16			–29	dB
4.2.12g	$CMG3_{o123}$	Common mode gain peak	Specified by design, capacitor load = 25 pF RO = 1.65 V ADREF = 3.3 V, gain = 16			–15	dB

Electrical Characteristics (continued)

over operating temperature T_J = –40°C to 150°C and recommended operating conditions, VS = 4.75 V to 40 V(1), f_{PWM} < 20 kHz (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.3	**SHIFT BUFFER**						
4.3.2	VRO	Shift output voltage range	ADREF = 5 V	0.1 × ADREF		0.5 × ADREF	V
4.3.3	VR_{offset}	Shift voltage offset (with respect to RO)	ADREF = 5 V, RO_CFG [4:0] = 5'b11000: ADREF × 25 / 50, I_{load} = internal load		±1.7		mV
4.3.3a			RO_CFG [4:0] = 5'b00100: ADREF × 5 / 50-5'b10111: ADREF × 24 / 50		±4		mV
4.3.3b	VR_{offset}	Shift voltage offset (with respect to ADREF (3.3 V) × 25 / 50 (RO_CFG [4:0] = 5'b11000))	ADREF = 3.3 V, RO_CFG [4:0] = 5'b11000: ADREF × 25 / 50, I_{load} = internal load		±1.7		mV
4.3.4	C_{RO}	RO output load capacitance range		0		150	pF
4.3.5	I_{RO}	Shift output current capability	ADREF = 5 V, RO_CFG [4:0] = 5'b11000: ADREF × 25 / 50	–5		5	mA
4.3.6			RO_CFG [4:0] = 5'b00100: ADREF × 5 / 50-5'b10111: ADREF × 24 / 50	–1		1	mA
4.3.7	$T_{dgadref}$	ADREF UV/ OV detection deglitch time		3	5	7	µs
4.3.8	$PSRR_{RO}$	Power supply rejection ratio at DC	Decoupling capacitor typical 1 µF on VCC5 / 0.1 µF VCC3 at DC. Specified by design, capacitor load = 25 pF RO = 2.5 V ADREF = 5 V, Gain = 16, dVS / d_{RO} dVCC5 / d_{RO}	70	80		dB
4.4.9	$t_{dgadref}$	ADREF UV/OV detection deglitch time		3	5	7	µs
4.4	**ADREF / VDDIO**						
4.4.1	V_{oxm}	Tolerance of ADREF voltage clamp	Relative to ADREF 5.75 V ≤ VS	–0.1	0.03	0.25	V
4.4.2	V_{oxos}	Overshoot of O1/2/3 over ADREF	Ox-ADREF; for <1 µs; specified by design			1.2	V
4.4.3	I_{ADREF}	Bias current for voltage clamping circuit	ADREF = 3.3 V, pin to ground			300	µA
4.4.4	$V_{ovadref}$	Overvoltage threshold	ADREF: 3.3-V setting by RVSET resistor	3.696	3.795	3.894	V
4.4.4a			ADREF: 5-V setting by RVSET resistor	5.6	5.75	5.9	V
4.4.5	$V_{uvadref}$	Undervoltage threshold	ADREF: 3.3-V setting by RVSET resistor	2.706	2.805	2.904	V
4.4.5a			ADREF: 5-V setting by RVSET resistor	4.1	4.25	4.4	V
4.4.7	$V_{ovvddio}$	Overvoltage threshold	VDDIO: 3.3-V setting by RVSET resistor	3.696	3.795	3.894	V
4.4.7a			VDDIO: 5-V setting by RVSET resistor	5.6	5.75	5.9	V
4.4.8	$V_{uvvddio}$	Undervoltage threshold	VDDIO: 3.3-V setting by RVSET resistor	2.706	2.805	2.904	V
4.4.8a			VDDIO: 5-V setting by RVSET resistor	4.1	4.25	4.4	V
4.4.10	R_{vset33}	VDDIO = 3.3 V / ADREF = 3.3-V mode	STAT6 bit[3:0] = 4'b0001	135	150	165	kΩ
4.4.11	R_{vset53}	VDDIO = 5 V / ADREF = 3.3-V mode	STAT6 bit[3:0] = 4'b0100	46	51	56.5	kΩ
4.4.12	R_{vset35}	VDDIO = 3.3 V / ADREF = 5-V mode	STAT6 bit[3:0] = 4'b1000	13.5	15	16.5	kΩ
4.4.13	R_{vset55}	VDDIO = 5 V / ADREF = 5-V mode	STAT6 bit[3:0] = 4'b0010	4.6	5.1	5.65	kΩ
4.4.30	$R_{vsetopen}$	RVSET resistor error detection		650			kΩ
4.4.31	$R_{vsetshort}$	RVSET resistor error detection				1.4	kΩ
4.4.32	$V_{rvsettjn40}$	RVSET output voltage	–40°C T_J, THERMAL_RVSET_EN = 1	1.67	1.745	1.82	V
4.4.33	$V_{rvsettj25}$		25°C T_J, THERMAL_RVSET_EN = 1	1.445	1.535	1.625	
4.4.34	$V_{rvsettj125}$		125°C T_J, THERMAL_RVSET_EN = 1	1.085	1.195	1.305	

Electrical Characteristics (continued)

over operating temperature T_J = –40°C to 150°C and recommended operating conditions, VS = 4.75 V to 40 V(1), f_{PWM} < 20 kHz (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	VCC3 / VCC5 REGULATORS						
4.4.14	VCC3	VCC3 regulator output voltage	VS > 4 V	3	3.15	3.3	V
4.4.15	$VCC3_{UV}$	VCC3 regulator undervoltage threshold	VS > 4 V	2.7	2.85	3	V
4.4.16	$VCC3_{OV}$(3)	VCC3 regulator overvoltage threshold	VS > 4 V	3.3	3.45	3.6	V
4.4.17	VCC5_1	VCC5 regulator output voltage 1	VS > 6 V	5.15	5.3	5.45	V
4.4.18	VCC5_2	VCC5 regulator output voltage 2	6 V > VS > 4.75 V	4.6		5.45	V
4.4.19	$VCC5_{UV}$	VCC5 regulator undervoltage threshold	VS > 4.75 V	4.3		4.6	V
4.4.20	$VCC5_{OV}$	VCC5 regulator overvoltage threshold	VS > 4.75 V	5.45	5.6	5.75	V
5.	**GATE DRIVER**						
5.1	$V_{GS,low}$	Gate-source voltage low, high-side/low-side driver	Active pulldown, I_{load} = –2 mA	0		0.2	V
5.2	R_{GSp}	Passive gate-source resistance	Vgs ≤ 200 mV	110	220	330	kΩ
5.3	R_{GSsa}	Semi-active gate-source resistance	In sleep mode, V_{GS} > 2 V		2	4	kΩ
5.3b	I_{GSL01}	Low-side driver pullup/pulldown current	Gate driven low by gate driver, CURR1, 3 = 01, SPI configurable	TYP × 0.65	0.65	TYP × 1.35	A
5.3c	I_{GSL00}		Gate driven low by gate driver(3), CURR1, 3 = 00, SPI configurable	TYP × 0.1	0.15	TYP × 1.9	A
5.3d	I_{GSL10}		Gate driven low by gate driver, CURR1, 3 = 11, SPI configurable	TYP × 0.65	1.1	TYP × 1.35	A
5.3f	I_{GSH01}	High-side driver pullup/pulldown current	Gate driven low by gate driver, CURR0, 2 = 01, SPI configurable	TYP × 0.65	0.65	TYP × 1.35	A
5.3g	I_{GSH00}		Gate driven low by gate driver(3), CURR0, 2 = 00, SPI configurable	TYP × 0.1	0.15	TYP × 1.9	A
5.3h	I_{GSH11}		Gate driven low by gate driver, CURR0, 2 = 11, SPI configurable	TYP × 0.65	1.1	TYP × 1.35	A
5.3i	I_{GSHsd}	High-side/low-side driver shutdown current		2	30	70	mA
5.4	$V_{GS,HS,high}$	High-side output voltage	I_{load} = –2 mA; 4.75 V < VS < 40 V	9		13.4	V
5.5	$V_{GS,LS,high}$	Low-side output voltage	I_{load} = –2 mA	9		13.4	V
5.27	t_{Don}	Propagation on delay time(2)	After ILx/IHx rising edge, Cload = 10 nF, CURR1, 3 = 10, VGS = 1 V	100	200	350	ns
5.31	A_{dt}	Accuracy of dead time	If not disabled in CFG1	–15%		15%	
5.32	IHSxlk_1	Source leak current, total leakage current of source pins	EN = L, SHSx = 1.5 V, T_J < 125°C	–5		5	µA
5.32a	IHSxlk_2		EN = L, SHSx = 1.5 V, 125°C < T_J < 150°C	–40		40	µA
5.29	t_{Doff}	Propagation off delay time(2)	ILx/IHx falling edge to $V_{GS,LS,high}$($V_{GS,HS,high}$) – 1 V Ciss = 10 nF, CURR1,3 = 10,	100	200	350	ns
5.30	$t_{Doffdiff}$	Propagation off delay time difference(2)	LSx to LSy and HSx to HSy Cload = 10 nF, CURR1,3 = 10, $V_{GS,LS,high}$($V_{GS,HS,high}$) – 1 V			50	ns
5.30a	$t_{Don\_Doff\_diff}$	Difference between propagation on delay time and propagation off delay time(2)	For each gate driver in each channel: Cload = 10 nF, CURR1, 3 = 10, VGS = 1 V (rising), $V_{GS,LS,high}$($V_{GS,HS,high}$) – 1 V (falling)			150	ns
5.30c	t_{ENoff}	Propagation off (EN) deglitching time(2)	After falling edge on EN	2.5	6	12	µs
5.30d	t_{SD}	Time until gate drivers initiate shutdown(2)	After falling edge on EN		12	24	µs
5.30e	t_{SDDRV}	Time until gate drivers initiate shutdown(2)	After rising edge on DRVOFF			10	µs

Electrical Characteristics (continued)

over operating temperature T_J = –40°C to 150°C and recommended operating conditions, VS = 4.75 V to 40 V(1), f_{PWM} < 20 kHz (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
6.	**BOOST CONVERTER**						
6.1	V_{BOOST}	Boost output voltage excluding switching ripple and response delay.	BOOST-VS voltage	14	15	16.5	V
6.1b	$V_{BOOSTOV}$	Boost output voltage overvoltage with respect GND		64	67.5	70	V
6.2	I_{BOOST}	Output current capability	External load current including external MOSFET gate charge current BOOST – VS > $V_{BOOSTUV}$	40			mA
6.3	f_{BOOST}	Switching frequency	BOOST – VS > $V_{BOOSTUV}$; ensured by characterization(4)	1.8	2.5	3	MHz
6.31			BOOST – VS > $V_{BOOSTUV}$; V_S < 6 V; ensured by characterization(4)	1.1		3	
6.4	$V_{BOOSTUV}$	Undervoltage shutdown level	BOOST-VS voltage	7		8	V
6.4a	$V_{BOOSTUV2}$	Undervoltage condition that device may enter RESET state	BOOST-GND voltage			10	V
6.5	t_{BCSD}	Filter time for undervoltage detection		5		6	µs
6.7	$V_{GNDLS\_B,off}$	Voltage at GNDLS_B pin at which boost FET switches off because of current limit		110	150	200	mV
6.7a	$t_{SW,off}$	Delay of the GNDLS_B current limit comparator	Specified by design			100	ns
6.8	$I_{SW,fail}$	Internal second-level current limit	GNDLS_B = 0 V	840		1600	mA
6.9	R_{dson_BSTfet}	R_{dson} resistance boost FET	VS ≥ 6 I_{SW} = $V_{GNDLS\_B,off}$ / 0.33 Ω	0.25		1.5	Ω
6.9a			VS < 6 I_{SW}= $V_{GNDLS\_B,off}$ / 0.33 Ω			2	Ω
7.	**DIGITAL INPUTS**						
7.1	INL	Input low threshold	All digital inputs NCS, DRVOFF, ILSx, IHSx, SDI			VDDIO × 0.3	V
7.1a	ENH	EN input high threshold	VS > 4 V	2.7			V
7.1b	ENL	EN input low threshold	VS > 4 V			0.7	V
7.2	INH	Input high threshold	All digital inputs NCS, DRVOFF, ILSx, IHSx, SDI	VDDIO × 0.7			V
7.3	Inhys	Input hysteresis	All digital inputs EN, NCS, DRVOFF, ILSx, IHSx, SDI, VDDIO = 5 V	0.3	0.4		V
7.3a	Inhys	Input hysteresis	All digital inputs EN, NCS, DRVOFF, ILSx, IHSx, SDI, VDDIO = 3.3 V	0.2	0.3		V
7.4	$R_{pd,EN}$	Input pulldown resistor at EN pin	EN	140	200	360	kΩ
7.4a	$t_{deg,ENon}$	Power-up time after EN pin high from sleep mode to active mode	ERR = L → H			5	ms
7.5	R_{pullup}	Input pullup resistance	NCS, DRVOFF	200	280	400	kΩ
7.6	$R_{pulldown}$	Input pulldown resistance	ILSx, IHSx, SDI , SCLK Input voltage = 0.1 V	100	140	200	kΩ
7.6a	$R_{pulldown}$	Input pulldown current	ILSx, IHSx, SDI, SCLK Input voltage = VDDIO	4		50	µA
8.	**DIGITAL OUTPUTS**						
8.1	OH1	Output high voltage 1	All digital outputs: SDO, I = ±2 mA; VDDIO in functional range(5)	VDDIO × 0.9			V
8.2	OL1	Output low voltage 1	All digital outputs: SDO, I = ±2 mA; VDDIO in functional range			VDDIO × 0.1	V
8.3	OH2	Output high voltage 2	ERR I = –0.2 mA; VDDIO in functional range	VDDIO × 0.9			V
8.4	OL2	Output low voltage 2	ERR I = +0.2 mA; VDDIO in functional range			VDDIO × 0.1	V
9.	**VDS / VGS / R_{SHUNT} MONITORING**						
9.1	V_{SCTH}	VDS short-circuit threshold range	If not disabled in CFG1	0.1		2	V

(4) During startup when BOOST-VS < VBOOSTUV , f_{BOOST} is typically 1.25 MHz.
(5) All digital outputs have a push-pull output stage between VDDIO and ground.

Electrical Characteristics (continued)

over operating temperature T_J = –40°C to 150°C and recommended operating conditions, VS = 4.75 V to 40 V(1), f_{PWM} < 20 kHz (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
9.2	A_{vds}	Accuracy of VDS monitoring	0.1-V to 0.5-V threshold setting	–50		50	mV
			0.6-V to 2-V threshold setting	–10%		10%	
9.3	t_{VDS}	Detection filter time	Only rising edge of VDS comparators are filtered		5		µs
9.4	V_{gserr+_1}	VGS error detection 1	STAT7, IHSx (ILSx) = H	7		8.5	V
9.5	V_{gserr-}	VGS error detection	STAT7, IHSx (ILSx) = L			2	V
9.6	t_{VGS}	Detection filter time	CFG6[5:4]		1.0		µs
9.6a	t_{VGSm}	Detection mask time	CFG6[2:0]		2.5		µs
9.7	V_{SHUNT}	R_{SHUNT} shutdown threshold range	SPI configurable	75		540	mV
9.8	A_{VSHUNT}	Accuracy of R_{SHUNT} shutdown	75-mV to 165-mV setting	–18		18	mV
			180-mV to 540-mV setting	–10%		10%	
9.9	t_{VSHUNT}	Detection filter time			5		µs
10.	**THERMAL SHUTDOWN**						
10.1	T_{msd0}	Thermal recovery	Specified by characterization	130	153	178	°C
10.2	T_{msd1}	Thermal warning	Specified by characterization	140	165	190	°C
10.3	T_{msd2}	Thermal global reset	Specified by characterization	170	195	220	°C
10.4	T_{hmsd}	Thermal shutdown×2 hysteresis	Specified by characterization		40		°C
10.5	t_{TSD1}	Thermal warning filter time	Specified by characterization	40	45	50	µs
10.6	t_{TSD2}	Thermal shutdown×2 filter time	Specified by characterization	2.5	6	12	µs
12.	**VS MONITORING**						
12.1	$V_{VS,OVoff0}$	Overvoltage shutdown level range(6)	Programmable CFG5 mode1, 12-V/24-V mode	29		38	V
12.1a	$V_{VS,OVoff1}$	Overvoltage shutdown level(6)	29-V threshold setting	27.5	29	30.5	V
12.1b	$V_{VS,\ OVon1}$	Recovery level form overvoltage shutdown(6)	29-V threshold setting	26.5	28	29.5	V
12.1c	$V_{VS,OVoff2}$	Overvoltage shutdown level(6)	33-V threshold setting	32	33.5	35	V
12.1d	$V_{VS,\ OVon2}$	Recovery level form overvoltage shutdown(6)	33-V threshold setting	31	32.5	34	V
12.1e	$V_{VS,OVoff3}$	Overvoltage shutdown level(6)	38-V threshold setting	36.5	38	39.5	V
12.1f	$V_{VS,\ OVon3}$	Recovery level form overvoltage shutdown(6)	38-V threshold setting	35.5	37	38.5	V
12.2	$V_{VS,UVoff}$	Undervoltage shutdown level(6)	VS is falling from higher voltage than 4.75 V	4.5		4.75	V
12.2a	$V_{VS,UVon}$	Recovery level form undervoltage shutdown(6)	Minimum VS for device startup	4.6		4.85	V
12.3	$t_{VS,SHD}$	Filter time for overvoltage/undervoltage shutdown		5		6	µs

(6) *Shutdown* signifies *predriver shutdown*, not VCC3/VCC5 regulator shutdown.

6.6 Serial Peripheral Interface Timing Requirements

POS 13			MIN	NOM	MAX	UNIT
13.1	f_{SPI}	SPI clock (SCLK) frequency			4 (1)	MHz
13.2	t_{SPI}	SPI clock period (2)	250			ns
13.3	t_{high}	High time: SCLK logic high duration (2)	90			ns
13.4	t_{low}	Low time: SCLK logic low duration (2)	90			ns
13.5	t_{sucs}	Setup time NCS: time between falling edge of NCS and rising edge of SCLK (2)	t_{SPI} / 2			ns
13.6	t_{d1}	Delay time: time delay from falling edge of NCS to data valid at SDO (2)			60	ns
13.7	t_{susi}	Setup time at SDI: setup time of SDI before the rising edge of SCLK (2)	30			ns
13.8	t_{d2}	Delay time: time delay from falling edge of SCLK to data valid at SDO (2)	0		60	ns
13.9	t_{hcs}	Hold time: time between the falling edge of SCLK and rising edge of NCS (2)	45			ns
13.10	t_{hlcs}	SPI transfer inactive time (time between two transfers) (2)	250			ns
13.11	t_{tri}	Tri-state delay time: time between rising edge of NCS and SDO in tri-state (2)			30	ns

(1) The maximum SPI clock tolerance is ±10%.
(2) Ensured by characterization.

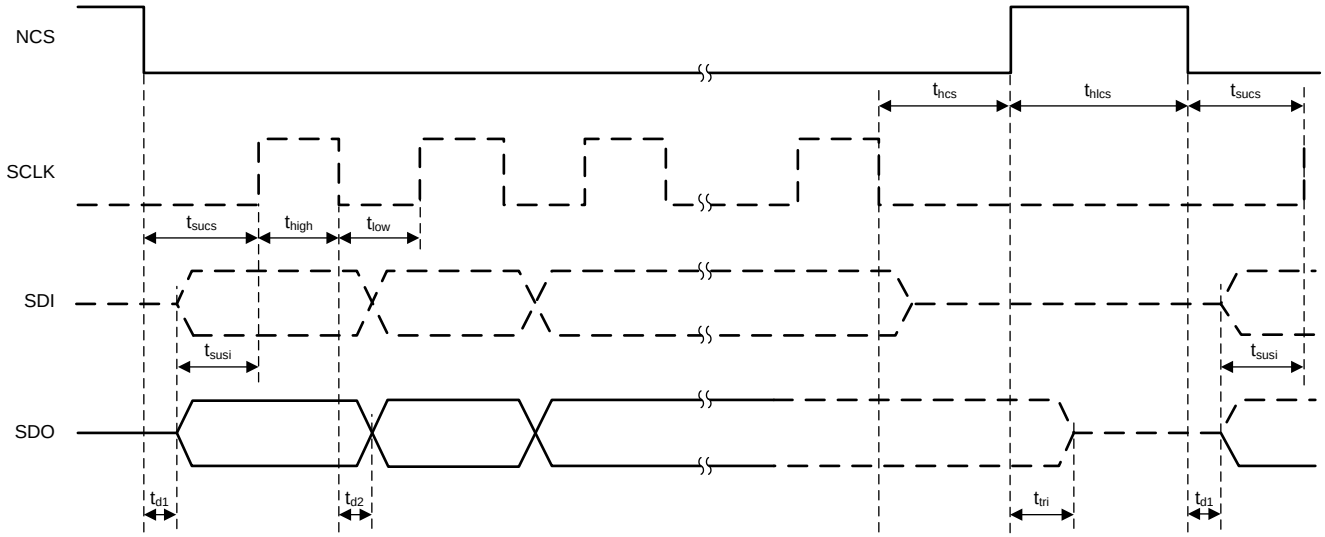


Figure 1. SPI Timing Parameters

6.7 Typical Characteristics

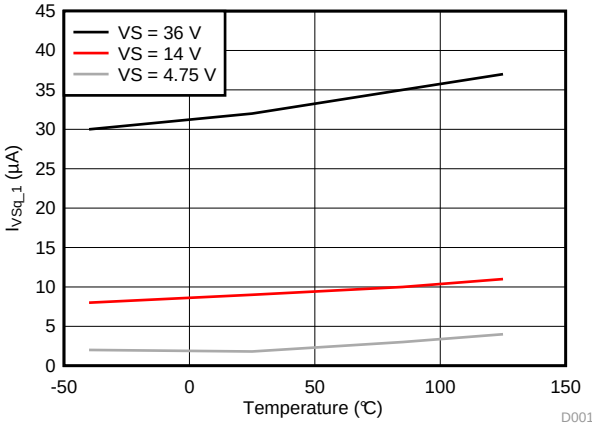


Figure 2. VS Quiescent Current Shutdown

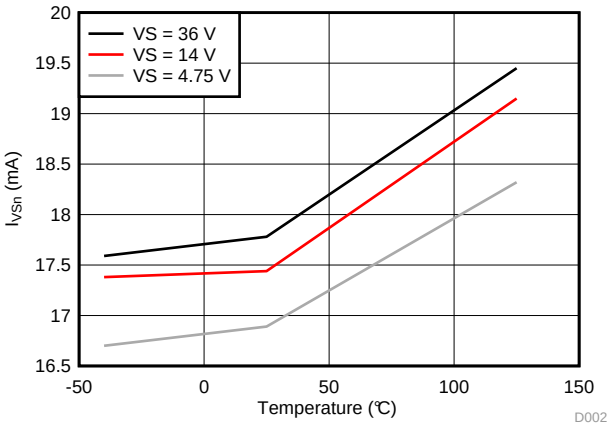


Figure 3. VS Quiescent Current Shutdown

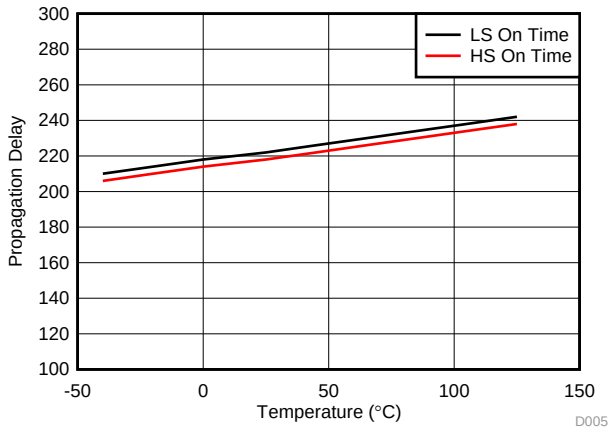


Figure 4. Propagation Delay On Time vs Temperature

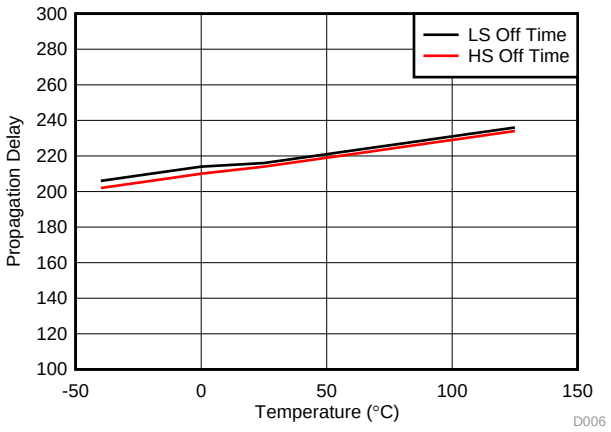


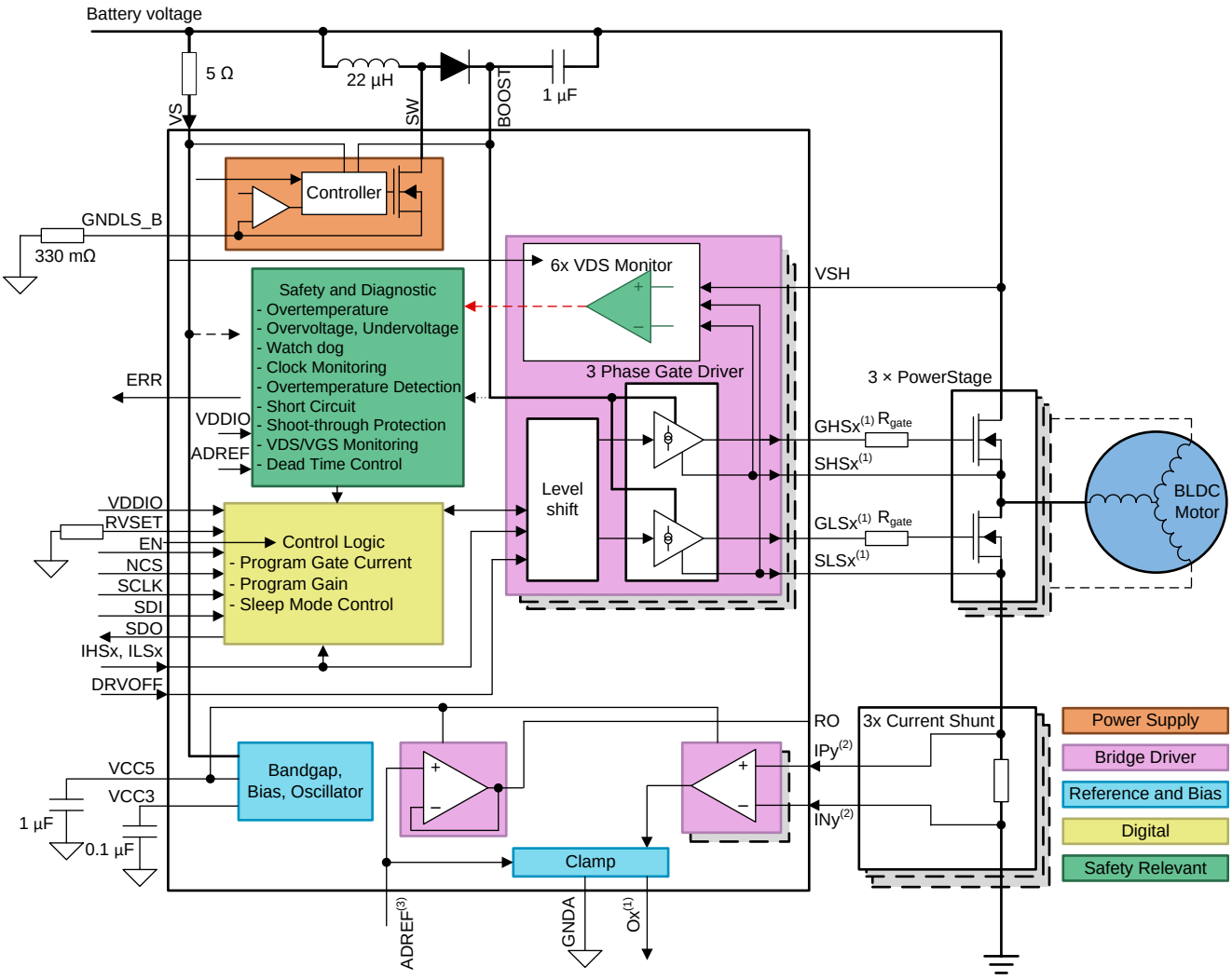
Figure 5. Propagation Delay Off Time vs Temperature

7 Detailed Description

7.1 Overview

The DRV3205-Q1 is designed to control 3-phase brushless DC motors in automotive applications using pulse-width modulation. Three high-side and three low-side gate drivers can be switched individually with low propagation delay. The input logic prevents simultaneous activation of the high-side and low-side driver of the same channel. A configuration and status register can be accessed through a SPI communication interface.

7.2 Functional Block Diagram



(1) x = 1, 2, 3

(2) y = 1, 2, 3

(3) An external reference voltage (VCC5 or VCC3) cannot be used for ADREF voltage.

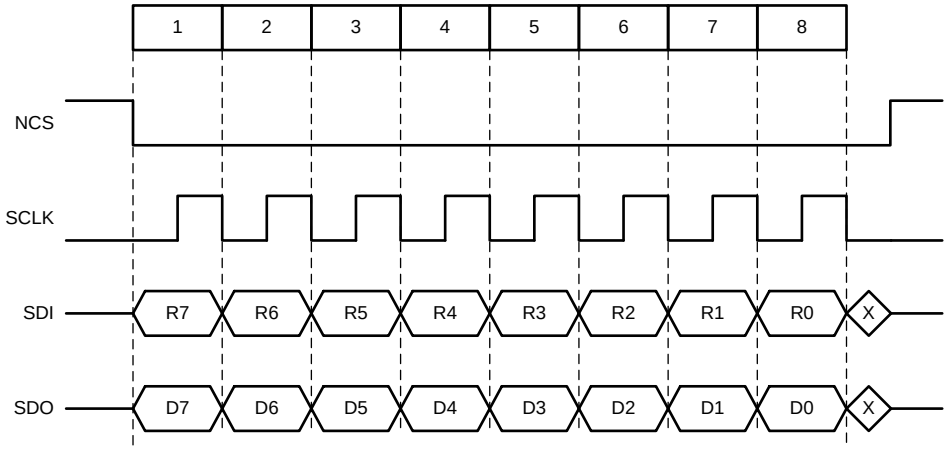
7.3 Programming

7.3.1 SPI

The SPI slave interface is used for serial communication with the external SPI master (external MCU). The SPI communication starts with the NCS falling edge and ends with NCS rising edge. The NCS high level keeps the SPI slave interface in reset state, and the SDO output in tri-state.

7.3.1.1 Address Mode Transfer

The address mode transfer is an 8-bit protocol. Both SPI slave and SPI master transmit the MSB first.



NOTE: SPI master (MCU) and SPI slave (DRV3205-Q1) sample received data on the ~~!– falling~~!~rising SCLK edge and transmit on the ~~!– rising~~!~falling SCLK edge.

Figure 6. Single 8-Bit SPI Frame/Transfer

After the NCS falling edge, the first word of 7 bits are address bits followed by the RW bit. During first address transfer, the device returns the STAT1 register on SDO.

Each complete 8-bit frame will be processed. If NCS goes high before a multiple of 8 bits is transferred, the bits are ignored.

7.3.1.1.1 SPI Address Transfer Phase

Figure 7. SPI Address Transfer Phase Bits

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	RW

ADDR [6:0] Register address

RW Read and write access

RW = 0: Read access. The SPI master performs a read access to selected register. During following SPI transfer, the device returns the requested register read value on SDO, and device interprets SDI bits as a next address transfer.

RW = 1: Write access. The master performs a write access on the selected register. The slave updates the register value during next SPI transfer (if followed immediately) and returns the current register value on SDO.

7.3.1.2 SPI Data Transfer Phase

Figure 8. SPI Data Transfer Phase Bits

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	DATA7	DATA6	DATA5	DATA4	ADDR3	DATA2	DATA1	DATA0

DATA [7:0] Data value for write access (8-Bit).

Figure 8 shows data value encoding scheme during a write access. Mixing the two access modes (write and read access) during one SPI communication sequence (NCS = 0) is possible. The SPI communication can be terminated after single 8-bit SPI transfer by asserting NCS = 1. Device returns STAT1 register (for the very first SPI transfer after power-up) or current register value that was addressed during SPI Transfer Address Phase.

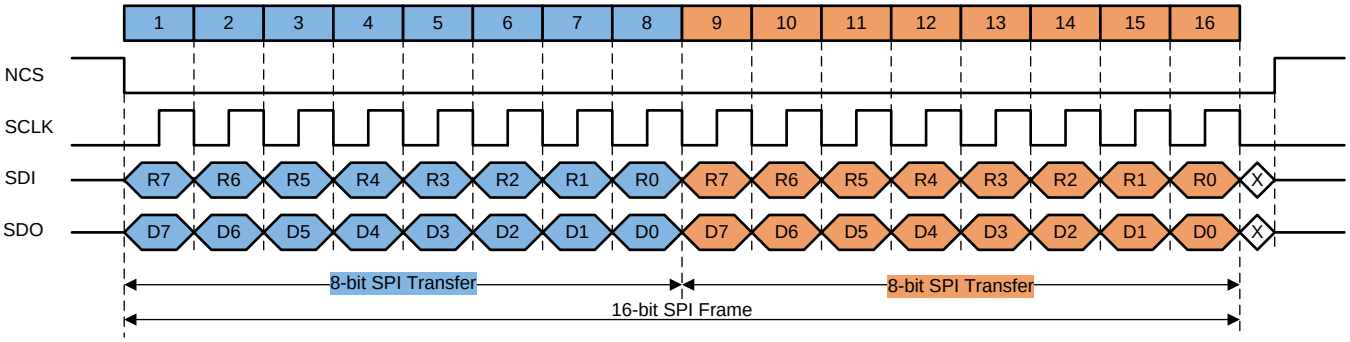
7.3.1.3 Device Data Response

Figure 9. Device Data Response Bits

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0

REG [7:0] Internal register value. All unused bits are set to 0.

Figure 10 shows a complete 16-bit SPI frame. Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, and Figure 16 show the frame examples.



SPI Master (MCU) and SPI slave (DRV32~~!~ 20~~!~05-Q1) sample received data on the rising SCLK edge, and transmit data on the falling SCLK edge

Figure 10. 16-Bit SPI Frame

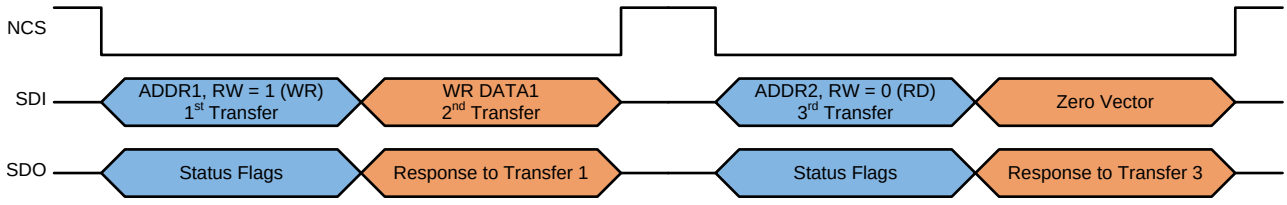


Figure 11. Write Access Followed by Read Access

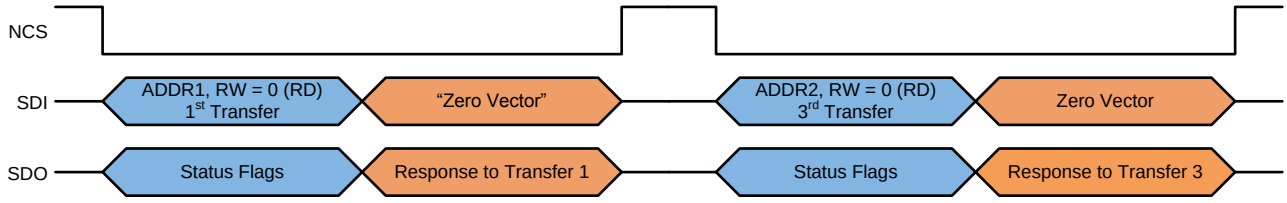


Figure 12. Read Access Followed by Read Access

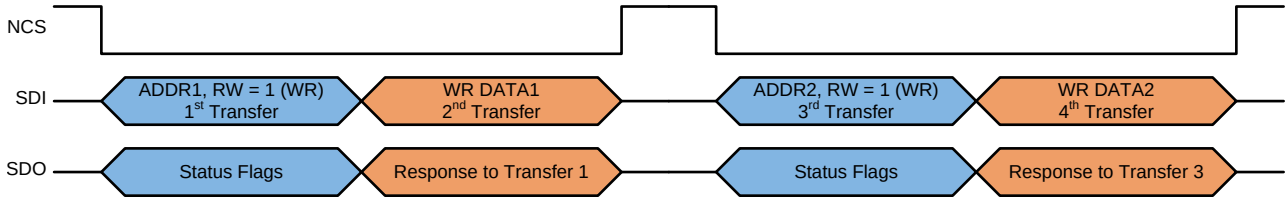


Figure 13. Write Access Followed by Write Access

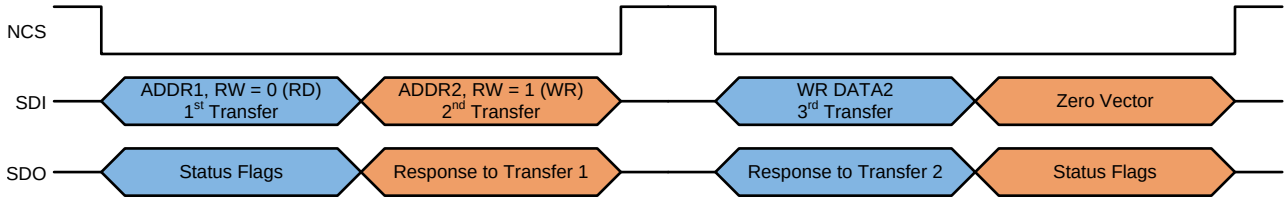


Figure 14. Read Access Followed by Write Access

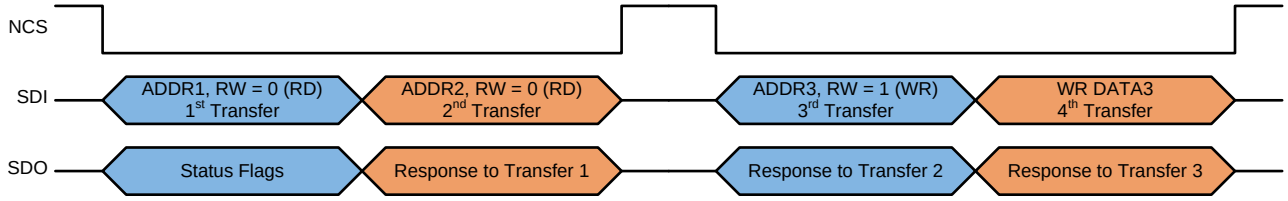


Figure 15. Read Access Followed by Read Access Followed by Write Access

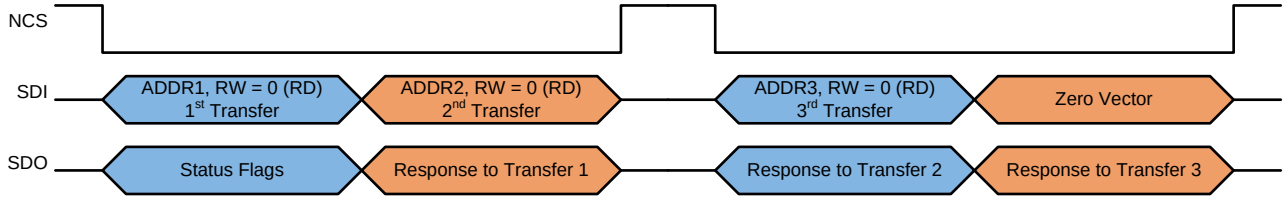


Figure 16. Read Access Followed by Read Access Followed by Read Access

7.4 Register Maps

Table 1. Register Address Map

Address	Name	Reset Value	CRC Check	Access State(1)	Reset Event(2) (bit wide exception)
0×01	Configuration register 0 (CFG0)	8'h3F	Yes	W/R : D, A([6:3]) R : A(7,[2:0], SF	RST1-4
0×02	Configuration register 1 (CFG1)	8'h3F	Yes	W/R: D R: A, SF	RST1-4
0×03	Configuration register 2 (CFG2)	8'h00	Yes	W/R: D R: A, SF	RST1-4
0×04	HS 1/2/3 drive register (CURR0) ON	8'h00	Yes	W/R: D R: A, SF	RST1-4
0×05	LS 1/2/3 drive register (CURR1) ON	8'h00	Yes	W/R: D R: A, SF	RST1-4
0×06	HS 1/2/3 drive register (CURR2) OFF	8'h00	Yes	W/R: D R: A, SF	RST1-4
0×07	LS 1/2/3 drive register (CURR3) OFF	8'h00	Yes	W/R: D R: A, SF	RST1-4
0×08	Safety/error configuration register (SECR1)	8'hC0	Yes	W/R: D R: A, SF	RST1
0×09	Safety function configuration register (SFCR1)	8'h80	Yes	W/R: D R: A, SF	RST1-3
0×0A	Status register 0 (STAT0)	8'h00	No	R: D, A, SF	RST1-4
0×0B	Status register 1 (STAT1)	8'h80	No	R: D, A, SF	RST1-3
0×0C	Status register 2 (STAT2)	8'h00	No	R: D, A, SF	RST1-3
0×0D	Status register 3 (STAT3)	8'h03	No	R: D, A, SF	RST1-3
0×0E	Status register 4 (STAT4)	8'h00	No	R: D, A, SF	RST1-3
0×0F	Status register 5 (STAT5)	8'h03	No	R: D, A, SF	RST1-3 (Bit[4]:RST1)
0×10	Status register 6 (STAT6)	8'h00	No	R: D, A, SF	RST1-3
0×11	Status register 7 (STAT7)	8'h00	No	R: D, A, SF	RST1-4
0×12	Status register 8 (STAT8)	8'h00	No	R: D, A, SF	RST1-4 (Bit[0]:RST1)
0×13	Safety error status (SAFETY_ERR_STAT)	8'h00	No	R: D, A, SF	RST1-3 (Bit[3:1]:RST1)
0×14	Status register 9 (STAT9)	8'h00	No	R: D, A, SF	RST1-3
0×15	Reserved1	8'h00	No	W/R: D, A, SF	RST1-3
0×16	Reserved2	8'h00	No	W/R: D, A, SF	RST1-3
0×1E	SPI transfer write CRC register (SPIWR_CRC)	8'h00	No	W/R: D, A, SF	RST1-3
0×1F	SPI transfer read CRC register (SPIRD_CRC)	8'hFF	No	R: D, A, SF	RST1-3
0×20	SAFETY_CHECK_CTRL register (SFCC1)	8'h01	No	W/R: D R: A, SF	RST1-3
0×21	CRC control register (CRCCTL)	8'h00	No	W/R: D, A R: SF	RST1-3
0×22	CRC calculated (CRCCALC)	N/A	No	W/R: D R: A, SF	RST1-3
0×23	Reserved 3	8'h00	No	W/R: D, A, SF	RST1-3
0×24	HS/LS read back (RB0)	8'h00	No	R: D, A, SF	RST1-3
0×25	HS/LS count control (RB1)	8'h00	No	W/R: D, A R: SF	RST1-4

(1) W/R: Write and Read access possible, W: Write access possible, R: Read access possible
D: DIAGNOSITC STATE, A: ACTIVE STATE, SF: SAFE STATE, SY: STANDBY STATE, R: RESET
(2) RST1: Power up, RST2: System clock error detected by clock monitor RST3: VCC3 UV/OV or from other state to RESET, RST4: LBIST

Register Maps (continued)

Table 1. Register Address Map (continued)

Address	Name	Reset Value	CRC Check	Access State(1)	Reset Event(2) (bit wide exception)
0×26	HS/LS count (RB2)	8'h00	No	R: D, A, SF	RST1-4
0×27	Configuration register 3 (CFG3)	8'hAB	Yes	W/R: D R: A, SF	RST1-4
0×28	Configuration register 4 (CFG4)	8'h00	Yes	W/R: D R: A, SF	RST1-4
0×29	Configuration register 5 (CFG5)	8'hAB	Yes	W/R: D R: A, SF	RST1-3
0×2A	CSM unlock (CSM_UNLOCK1)	8'h00	No	W/R: D R: A, SF	RST1-4
0×2B	CSM unlock (CSM_UNLOCK2)	8'h3F	No	W/R: D R: A, SF	RST1-4
0×2C	RO configuration register 2 (RO_CFG)	8'h00	Yes	W/R: D R: A, SF	RST1-4
0×2D	Safety BIST control register 1 (SAFETY_BIST_CTL1)	8'h00	Yes	W/R: D R: SF, A	RST1-3
0×2E	SPI test register (SPI_TEST)	8'h00	No	W/R: D, A, SF	RST1-4
0×2F	Reserved4	8'h00	No	W/R: D, A, SF	RST1-3
0×30	Safety BIST control register 2 (SAFETY_BIST_CTL2)	8'h00	Yes	W/R: D R: SF, A	RST1-3 (Bit[5]:RST1)
0×31	Watch dog timer configuration register (WDT_WIN1_CFG)	8'h02	Yes	W/R: D R: SF, A	RST1-4
0×32	Watch dog timer configuration register (WDT_WIN2_CFG)	8'h08	Yes	W/R: D R: SF, A	RST1-4
0×33	Watch dog timer TOKEN register (WDT_TOKEN_FDBCK)	8'h04	Yes	W/R: D R: SF, A	RST1
0×34	Watch dog timer TOKEN register (WDT_TOKEN_VALUE)	8'h40	No	R: D, SF, A	RST1-4
0×35	Watch dog timer ANSWER register (WDT_ANSWER)	8'h00	No	W/R: D, A, SF	RST1-4
0×36	Watch dog timer status register (WDT_STATUS)	8'hC0	No	R: D, A, SG	RST1-4
0×37	Watch dog failure detection configuration register (WD_FAIL_CFG)	8'hEC	Yes	W/R: D R: SF, A	RST1-4
0×38	Configuration register 6 (CFG6)	8'h10	Yes	W/R: D R: A, SF	RST1-4
0×39	Configuration register 7 (CFG7)	8'h13	Yes	W/R : D R : A, SF	RST1-4
0×3A	Configuration register 8 (CFG8)	8'h20	Yes	W/R : D R : A, SF	RST1-4
0×3B	Configuration register 9 (CFG9)	8'hFE	Yes	W/R : D R : A, SF	RST1-4

8 Application and Implementation

NOTE

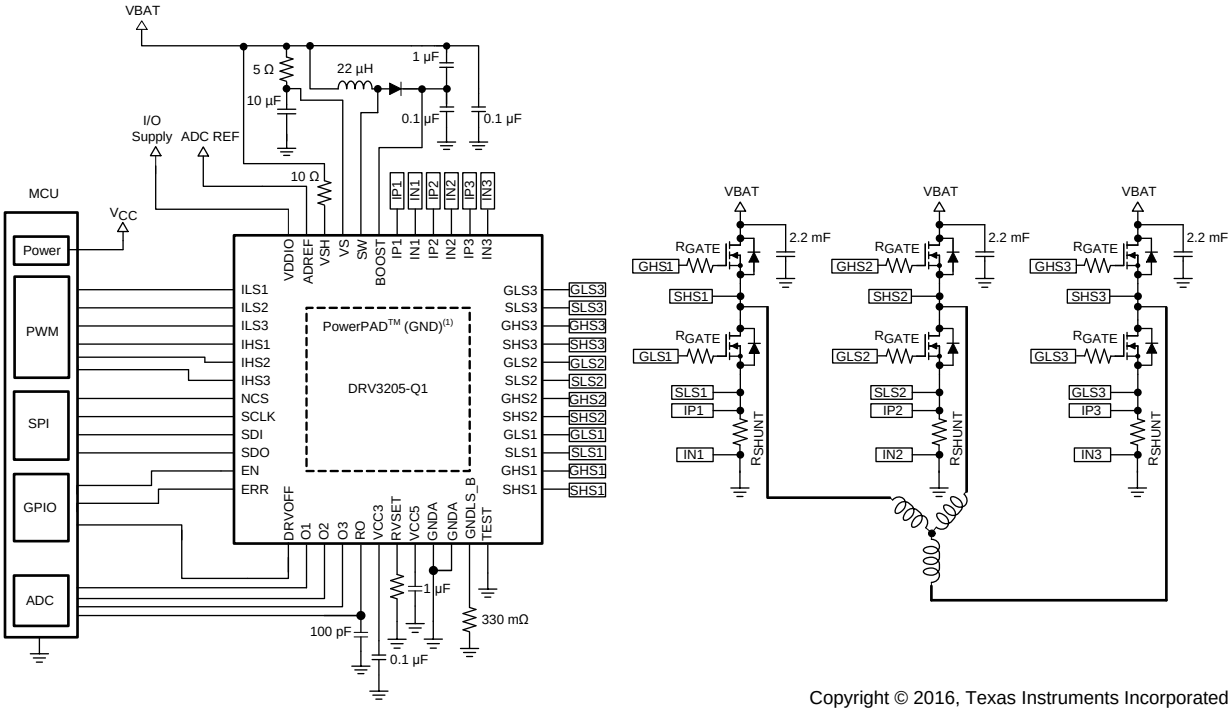
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV3205-Q1 is a predriver for automotive applications featuring three-phase brushless DC-motor control. Because this device has a boost regulator for charging high-side gates, it can handle gate charges of 250 nC. A boost converter allows full control on the power-stages even for a low battery voltage down to 4.75 V.

8.2 Typical Application

8.2.1 Three-Phase Motor Drive-Device for Automotive Application



(1) This schematic of the DRV3205-Q1 48-pin HTQFP does not provide a true representation of physical pin locations.

(2) Use same supply from the TPS6538x as the supply used for the MCU IO.

(3) Resistor not required for reverse protected battery.

(4) L1 = B82442A1223K000 INDUCTOR, SMT, 22 uH, 10%, 480 mA). The maximum inductor current must be more than VGNDLS_B / 330 mΩ.

(5) D1 = SS28 (DIODE, SMT, SCHOTTKY, 80 V, 2 A). A fast recovery diode is recommended.

(6) QxHS, QxLS = IRFS3004PBF (HEXFET, N-CHANNEL, POWER MOSFET, D2PACK)

(7) R_{shunt1} and R_{shunt2} = BVR-Z-R0005 (RES, SMT, 4026, PRECISION POWER, 0.0005 Ω, 1%, 5 W)

(8) R_{gate} = Must be adjust based on system requirement such as EMI, Slew rate, and power

Figure 17. Typical Application Diagram

8.3 System Example

Figure 18 shows a typical system example for an electric power-steering system.

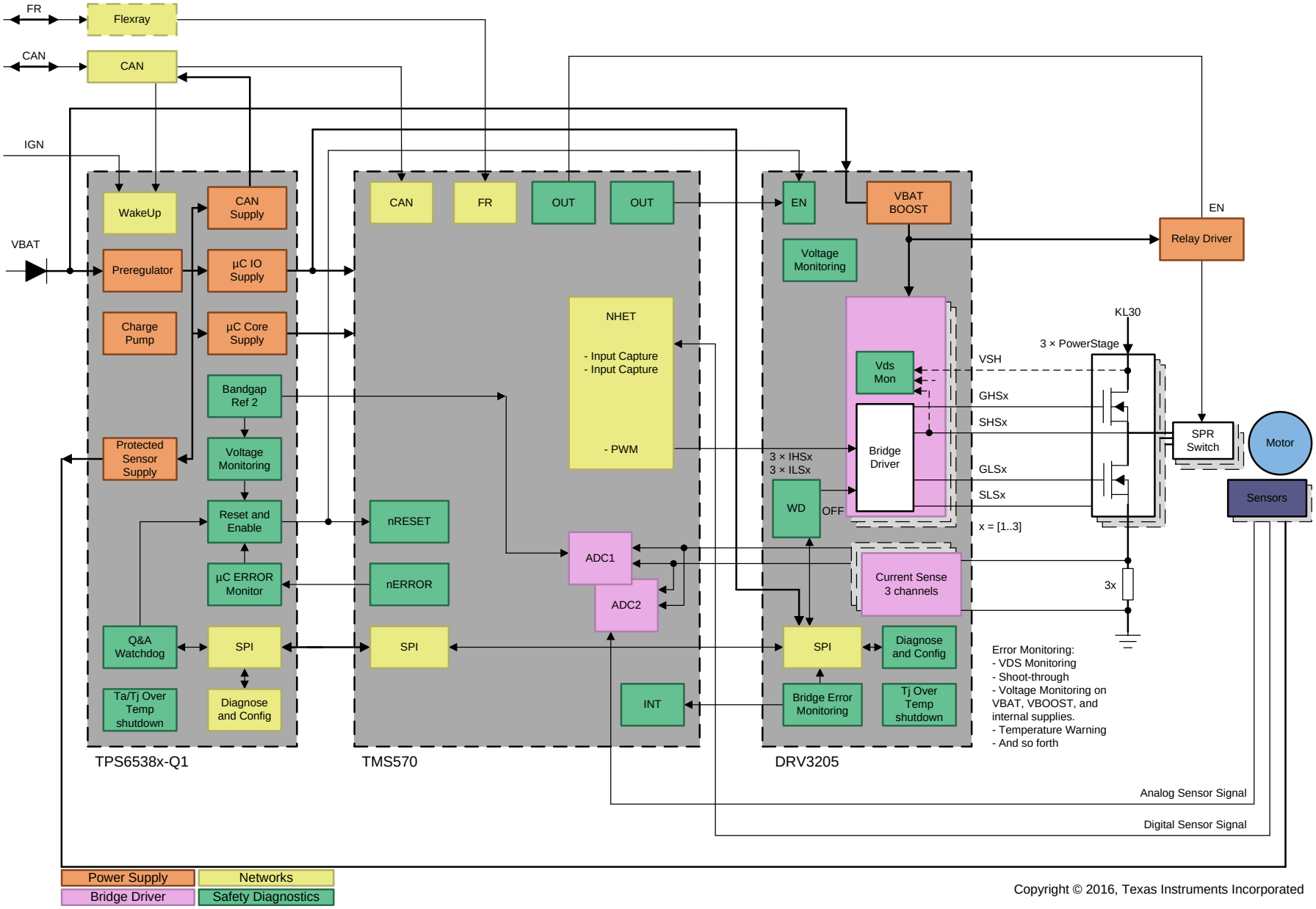


Figure 18. Typical System – Electrical Power Steering Example

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range of 4.75 V to 40 V. The protection circuit must be placed for protection against reverse supply connection.

10 Layout

10.1 Layout Guidelines

Use the following guidelines when designing a PCB for the DRV3205-Q1:

- In addition to the GND pins, the DRV3205-Q1 makes an electrical connection to GND through the PowerPAD. Always check that the PowerPAD has been properly soldered (see *PowerPAD™ Thermally Enhanced Package* [SLMA002]).
- The VS bypass capacitors should be placed close to the power supply terminals. See the VS box in Figure 19
- Place the VCC5 and VCC5 bypass capacitors close to the corresponding pins with a low impedance path to the ground plane pin (pin 16). See the VCC3 VCC5 bypass box in Figure 19.
- AGND should all be tied to the ground plane through a low impedance trace or copper fill.
- Add stitching vias to reduce the impedance of the GND path from the top to bottom side.
- Try to clear the space around and below the DRV3205-Q1 to allow for better heat spreading from the PowerPAD.
- Route the sense lines, IPx and INx, each with a unique trace, directly to either side of the sense resistor. See the SENSE box in Figure 19.
- Keep the BOOST components close to the device and current loops small. See the BOOST boxes in Figure 19.
- Place the current sense resistors close to the respective low-side FET. See the SENSE box in Figure 19.
- Place the GNDLS_B resistor close to the device pin. See the GNDLS_B box in Figure 19.

10.2 Layout Example

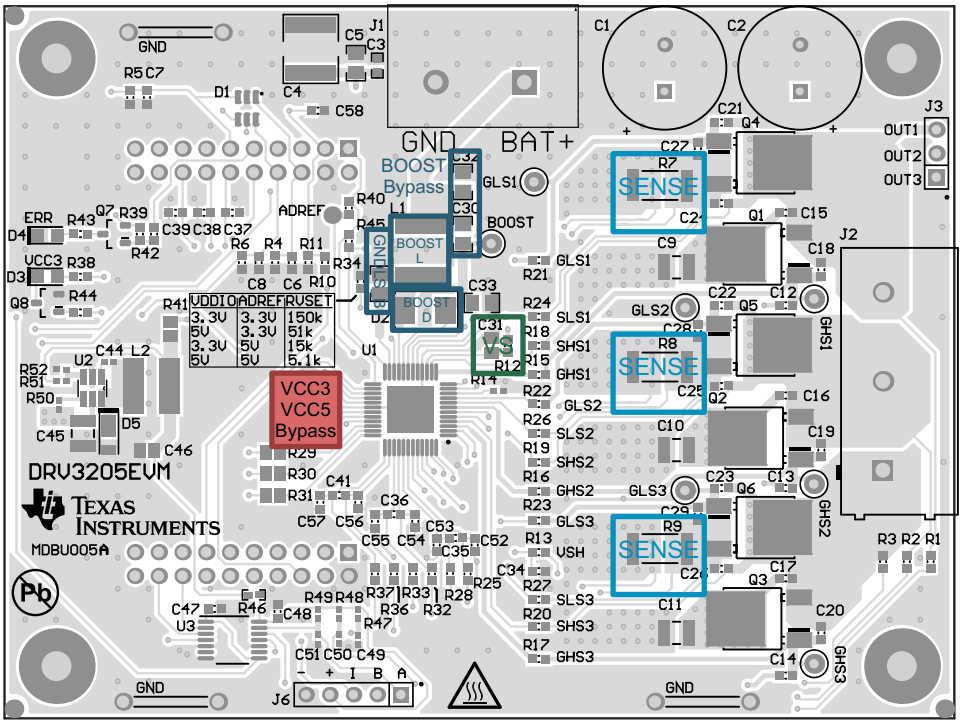


Figure 19. Layout Schematic

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください：

- 『DRV3205-Q1 24V車載システムのアプリケーション』
- 『DRV3205-Q1 評価モジュール ユーザー・ガイド』
- 『DRV3205-Q1 ソース・ピンの負の電圧ストレス』
- 『DRV3205-Q1 安全性マニュアル』
- 『DRV3205-Q1での電動パワー・ステアリング設計ガイド』
- 『放熱特性の優れたPowerPAD™パッケージ』
- 『車載モータ・ドライブ・システムの逆極性保護』
- 『DRV3205-Q1用のQ&Aウォッチドッグ・タイマ構成』
- 『TPS653850-Q1 安全関連アプリケーションのマイクロコントローラ用のマルチレール電源』
- 『TPS653853-Q1 安全関連アプリケーションのマイクロコントローラ用のマルチレール電源』

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*** **エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。**

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

11.4 商標

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV3205QPHPRQ1	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV32205Q
DRV3205QPHPRQ1.A	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV32205Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

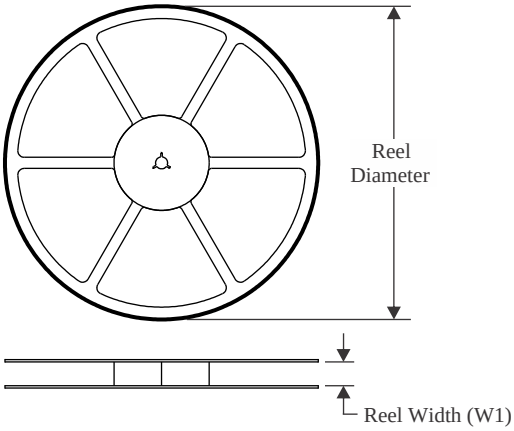
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

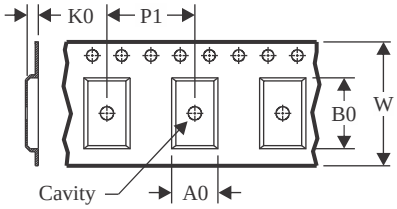
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

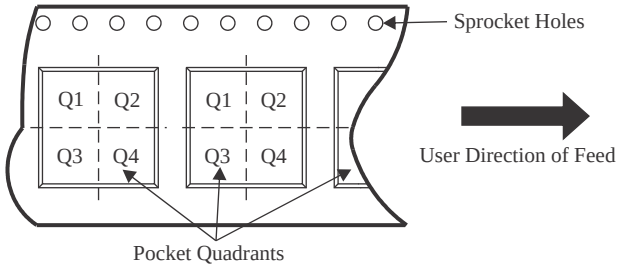


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

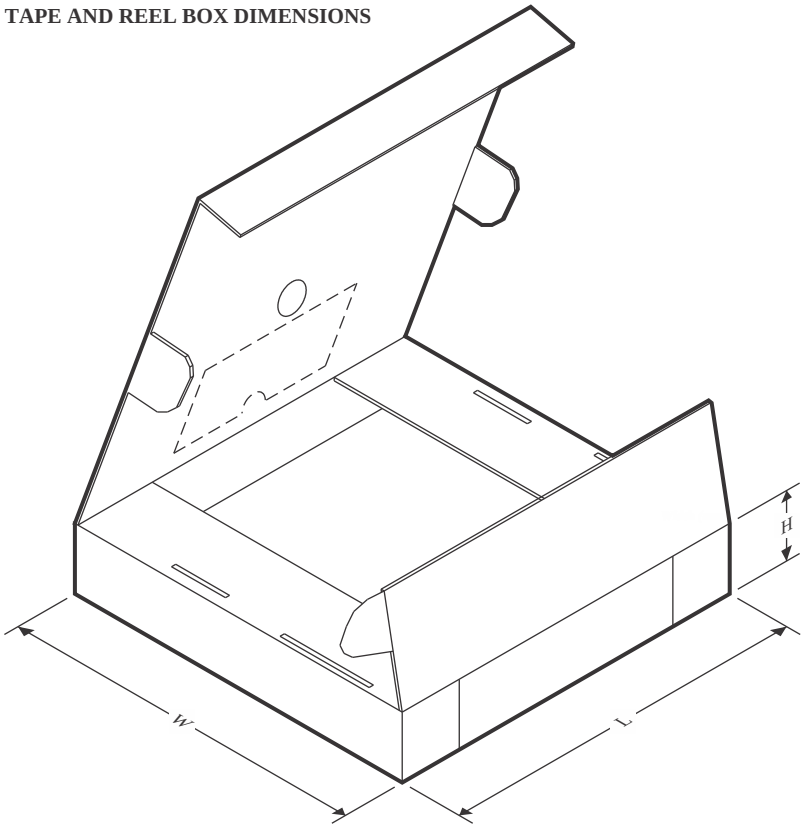
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV3205QPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV3205QPHPRQ1	HTQFP	PHP	48	1000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

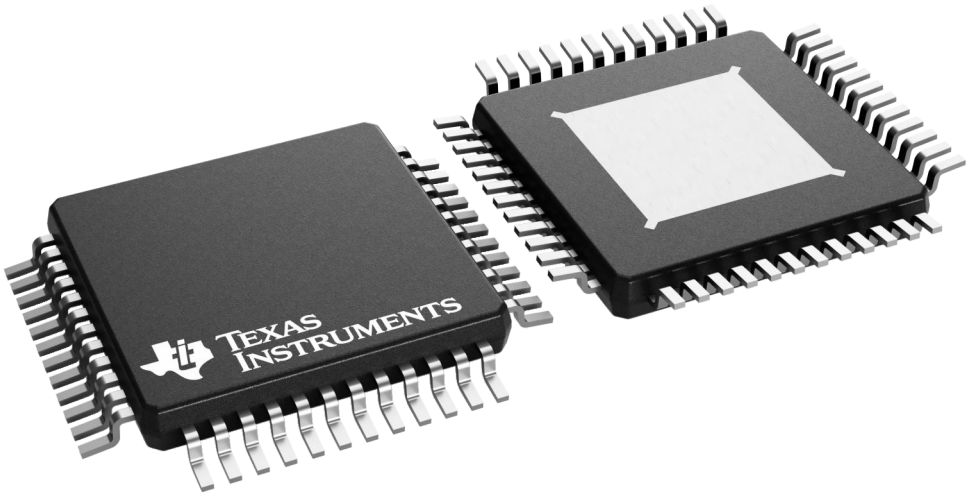
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



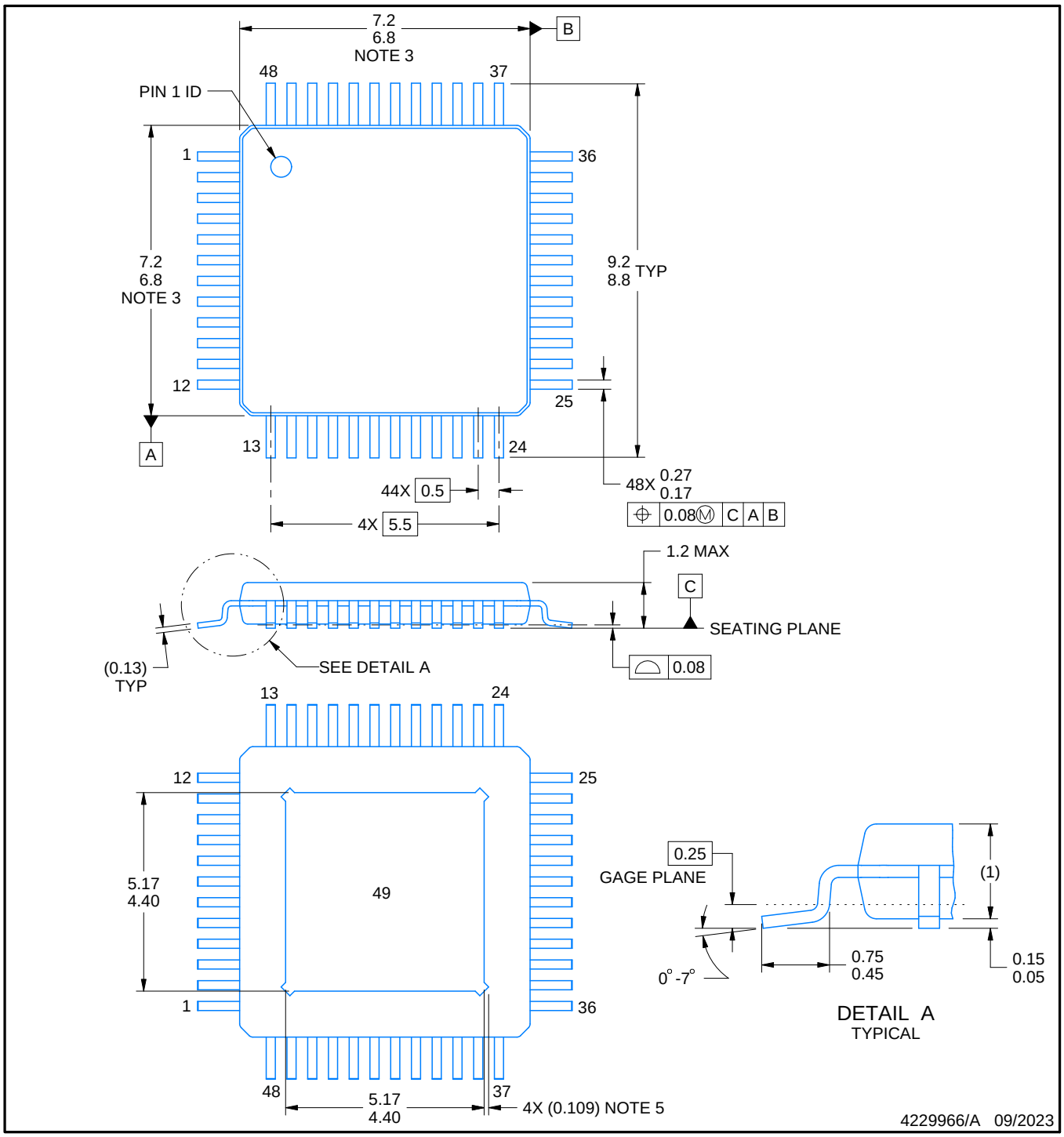
4226443/A

PACKAGE OUTLINE

PHP0048N

PowerPAD™ HTQFP - 1.2 mm max height

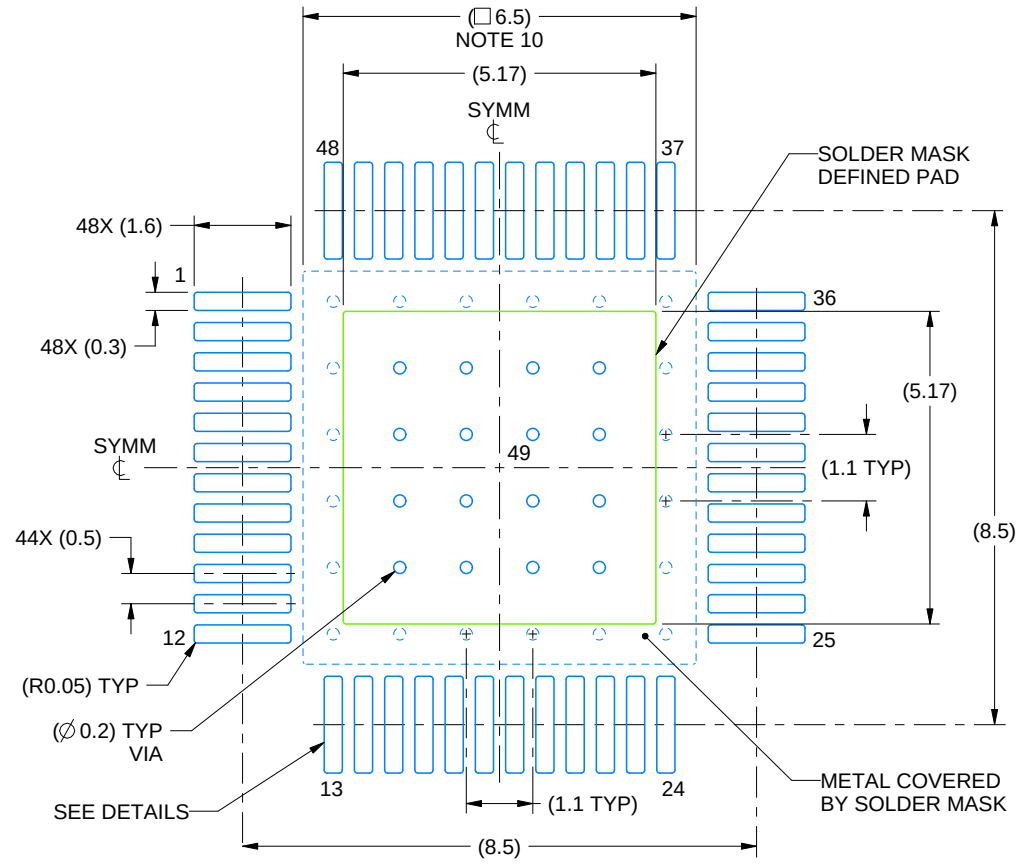
PLASTIC QUAD FLATPACK



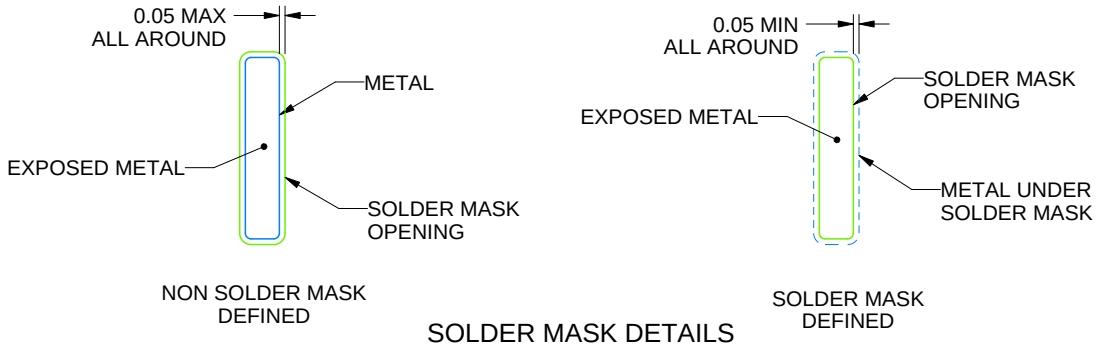
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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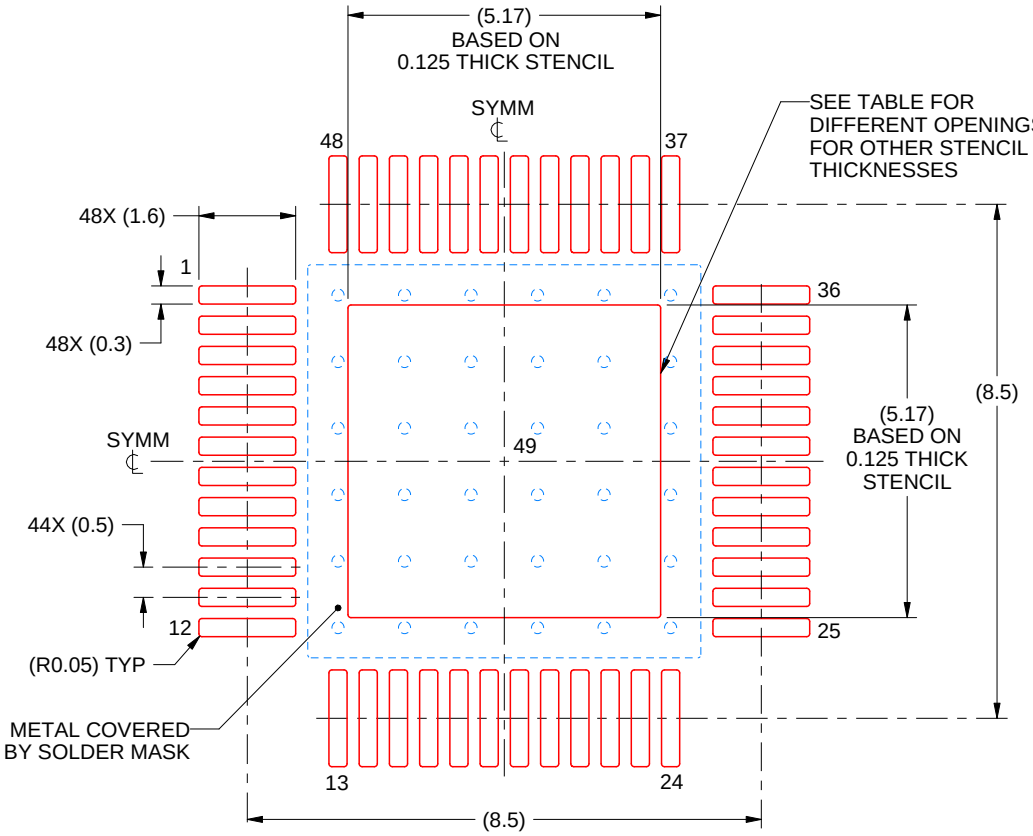
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.78 X 5.78
0.125	5.17 X 5.17 (SHOWN)
0.150	4.72 X 4.72
0.175	4.37 X 4.37

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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