DRV2667 ピエゾ・ハプティクス・ドライバ 昇圧、デジタル・フロント・エンド、内部波形メモリ付き

1 特長

- 統合型デジタル・フロント・エンド
  - 最高 400kHz の I^2C バス制御
  - 先進の波形シンセサイザ
  - 2kB の内部波形メモリ
  - 100 バイトの内部 FIFO インターフェイス
  - Immersion TS5000 準拠
  - オプションのアナログ入力
- 高電圧ピエゾ・ハプティクス・ドライバ
  - $200V_{PP}$、300Hz で最大 100nF を駆動
  - $150V_{PP}$、300Hz で最大 150nF を駆動
  - $100V_{PP}$、300Hz で最大 330nF を駆動
  - $50V_{PP}$、300Hz で最大 680nF を駆動
  - 差動出力
- 105V の内蔵昇圧コンバータ
  - 可変昇圧電圧
  - 可変昇圧電流制限
  - プログラム可能な昇圧電流制限機能
  - パワー FET およびダイオードを内蔵
  - 変圧器不要
- 2ms の短いスタートアップ時間
- 3.3～5.5V の広い電源電圧範囲
- 1.8V 互換、V_{DD} 許容のデジタル・ピン

2 アプリケーション

- 携帯電話およびタブレット
- 携帯型コンピュータ
- キーボードとマウス
- 電子ゲーム機
- タッチ対応デバイス

3 概要

DRV2667 デバイスは、105V 昇圧スイッチ、パワー・ダイオード、完全差動アンプ、デジタル・フロント・エンドを内蔵したピエゾ・ハプティクス・ドライバであり、高電圧と低電圧の両方のピエゾ・ハプティクス・アクチュエータを駆動可能です。この多用途デバイスは、I^2C ポートまたはアナログ入力により、HD ハプティクスをサポートします。

DRV2667 デバイスのデジタル・インターフェイスは、I^2C 互換バスを介して利用できます。デジタル・インターフェイスを採用すると、PWM 生成によるコストのかかるプロセッサの負担や、ホスト・システムでの追加のアナログ・チャネル要件を緩和できます。内部 FIFO への書き込みが行われるたびに、本デバイスは自動的に復帰し、2ms の内部スタートアップ手順の後で波形の再生を開始します。データ・フローが停止するか、FIFO がアンダーランすると、本デバイスは自動的にポップなしのシャットダウン手順に移行します。

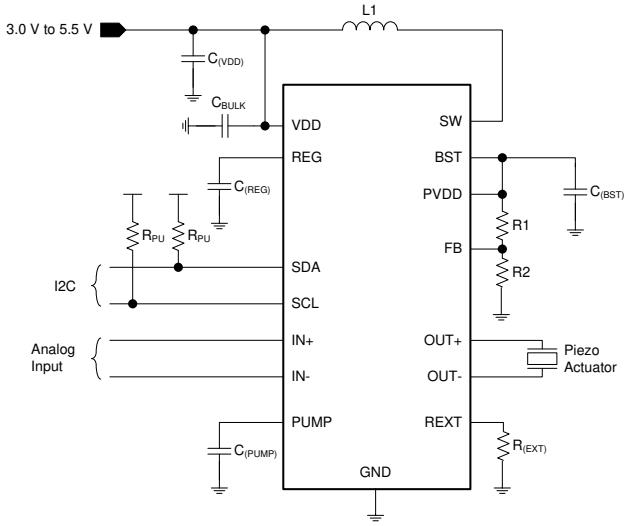
DRV2667 デバイスは、波形を保存して最低限のレイテンシで呼び出せる波形メモリ、最小限のメモリを使って複雑なハプティクス波形を構築できる先進の波形シンセサイザも備えています。これにより、ハードウェア・アクセラレーションが可能となり、ホスト・プロセッサはハプティクス生成の役目から解放され、ハプティクス・インターフェイス上のバス・トラフィックも最小限になります。

昇圧電圧は 2 つの外付け抵抗によって設定され、昇圧電流制限は R_{EXT} 抵抗によりプログラム可能です。標準のスタートアップ時間が 2ms である DRV2667 は、高速のハプティクス応答に理想的なピエゾ・ドライバです。熱過負荷保護機能により、過駆動時の損傷からデバイスを保護しています。

製品情報(1)

部品番号	パッケージ	本体サイズ (最大)
DRV2667	QFN (20)	4.00mm × 4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



簡略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (November 2018) to Revision E (January 2023)	Page
• Changed V_{DD} MIN spec from 3.0 to 3.3	4

Changes from Revision C (December 2017) to Revision D (November 2018)	Page
• Changed the first sentence of the second paragraph in the *FIFO Mode* section	14

Changes from Revision B (September 2015) to Revision C (December 2017)	Page
• Changed Bit 6-3 in *Address: 0x01*	27
• Changed 3.3 µF to 22 µF To: 3.3 µH to 22 µH in the *Inductor Selection* section	33

Changes from Revision A (January 2014) to Revision B (September 2015)	Page
• 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。	1
• Added Exception description to *セクション 7.3.11.3* section	13

Changes from Revision * (March 2013) to Revision A (January 2014)	Page
• 製品フォルダの 1 ページのデータシートを完全なデータシートに変更	1

5 Pin Configuration and Functions

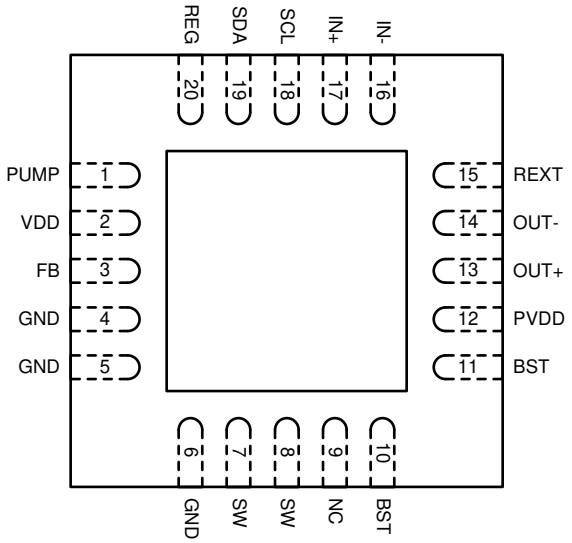


図 5-1. RGP Package 20-Pin QFN With Exposed Thermal Pad Top View

表 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
PUMP	1	P	Internal charge pump voltage
VDD	2	P	3- to 5.5-V supply input. A 1 µF-capacitor is required.
FB	3	I	Boost feedback
GND	4, 5, 6	P	Supply ground
SW	7, 8	P	Internal boost switch pin
NC	9	—	No connect
BST	10, 11	P	Boost output voltage. A 0.1-µF capacitor is required.
PVDD	12	P	High-voltage amplifier input voltage
OUT+	13	O	Positive haptic driver differential output
OUT-	14	O	Negative haptic driver differential output
REXT	15	I	Sets boost current limit. Resistor to ground.
IN-	16	I	Negative analog input
IN+	17	I	Positive analog input
SCL	18	I	I^2C clock
SDA	19	I/O	I^2C data
REG	20	O	1.8-V regulator output. A 0.1-µF capacitor is required.

1. I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage, V_{DD}		–0.3	6	V
Input voltage, V_I	SDA, SCL, IN+, IN–, FB	–0.3	V_{DD} + 0.3	V
Boost voltage	BST, SW, OUT+, OUT–, PVDD	–0.3	120	V
Operating free-air temperature, T_A		–40	70	°C
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		3.3		5.5	V
V_{BST}	Boost voltage		15		105	V
V_{IN}	Differential input voltage			1.8		V
C_L	Load capacitance	V_{BST} = 105 V, Frequency = 500 Hz, V_{OUT} = 200 V_{PP}			50	nF
		V_{BST} = 105 V, Frequency = 300 Hz, V_{OUT} = 200 V_{PP}			100	
		V_{BST} = 80 V, Frequency = 300 Hz, V_{OUT} = 150 V_{PP}			150	
		V_{BST} = 55 V, Frequency = 300 Hz, V_{OUT} = 100 V_{PP}			330	
		V_{BST} = 30 V, Frequency = 300 Hz, V_{OUT} = 50 V_{PP}			680	
		V_{BST} = 25 V, Frequency = 300 Hz, V_{OUT} = 40 V_{PP}			1000	
		V_{BST} = 15 V, Frequency = 300 Hz, V_{OUT} = 20 V_{PP}			3000	
R_{EXT}	Current limit control resistor		6		35	kΩ
L	Inductance for boost converter		3.3			µH

6.4 Thermal Information

THERMAL METRIC(1)		DRV2667 RGP (QFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.1	°C/W

THERMAL METRIC(1)		DRV2667 RGP (QFN) 20 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = 25 °C, V_{DD} = 3.6 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG}	Voltage at the REG pin			1.6	1.75	1.9	V
I_{IL}	Digital low-level input current		SDA, SCL V_{DD} = 3.6 V, V_I = 0 V			1	µA
I_{IH}	Digital high-level input current		SDA, SCL V_{DD} = 3.6 V, V_I = V_{DD}			1	uA
V_{IL}	Digital low-level input voltage		SDA, SCL V_{DD} = 3.6 V			0.5	V
V_{IH}	Digital high-level input voltage		SDA, SCL V_{DD} = 3.6 V	1.4			V
V_{OL}	Digital low-level output voltage		SDA 3-mA sink current			0.4	V
I_{SD}	Shutdown current		V_{DD} = 3.6 V, STANDBY = 1		10		µA
I_Q	Quiescent current	Digital mode	V_{DD} = 3.6 V, STANDBY = 0		130	175	µA
		Analog mode	V_{DD} = 3.6 V, analog input mode, V_{BST} = 105 V		24		mA
			V_{DD} = 3.6 V, analog input mode, V_{BST} = 80 V		13		
			V_{DD} = 3.6 V, analog input mode, V_{BST} = 50 V		9		
			V_{DD} = 3.6 V, analog input mode, V_{BST} = 30 V		5		
R_{IN}	Input impedance		IN+, IN–; All gains		100		kΩ
$V_{OUT(FS)}$	Full-scale output voltage (digital mode)		GAIN[1:0] = 00	49	50	51	V_{PP}
			GAIN[1:0] = 01	98	100	102	
			GAIN[1:0] = 10	147	150	153	
			GAIN[1:0] = 01	196	200	204	
$V_{OUT(OS)}$	Output offset		All gains	–0.25		0.25	V
BW	Amplifier bandwidth		GAIN[1:0] = 00, V_{OUT} = 50 V_{PP}, no load		20		kHz
			GAIN[1:0] = 01, V_{OUT} = 100 V_{PP}, no load		10		
			GAIN[1:0] = 10, V_{OUT} = 150 V_{PP}, no load		7.5		
			GAIN[1:0] = 11, V_{OUT} = 200 V_{PP}, no load		5		

T_A = 25 °C, V_{DD} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{BAT, AVG}$	Average battery current during operation	C_L = 220 nF, f = 200 Hz, V_{BST} = 30 V, GAIN[1:0] = 00, V_{OUT} = 50 V_{PP}		69		mA
		C_L = 680 nF, f = 150 Hz, V_{BST} = 30 V, GAIN[1:0] = 00, V_{OUT} = 50 V_{PP}		75		
		C_L = 680 nF, f = 300 Hz, V_{BST} = 30 V, GAIN[1:0] = 00, V_{OUT} = 50 V_{PP}		115		
		C_L = 22 nF, f = 200 Hz, V_{BST} = 80 V, GAIN[1:0] = 10, V_{OUT} = 150 V_{PP}		67		
		C_L = 47 nF, f = 150 Hz, V_{BST} = 105 V, GAIN[1:0] = 11, V_{OUT} = 200 V_{PP}		210		
		C_L = 47 nF, f = 300 Hz, V_{BST} = 105 V, GAIN[1:0] = 11, V_{OUT} = 200 V_{PP}		400		
THD+N	Total harmonic distortion plus noise	f = 300 Hz, V_{OUT} = 200 V_{PP}		1%		
f_S	Output sample rate	Digital playback engine sample rate	7.8	8	8.05	kHz

6.6 Timing Requirements

T_A = 25 °C, V_{DD} = 3.6 V (unless otherwise noted). For timing diagrams, see 図 6-1 and 図 6-2.

		MIN	NOM	MAX	UNIT
f_{SCL}	Frequency at the SCL pin with no wait states			400	kHz
$t_{w(H)}$	Pulse duration, SCL high	0.6			µs
$t_{w(L)}$	Pulse duration, SCL low	1.3			µs
$t_{su(1)}$	Setup time, SDA to SCL	100			ns
$t_{h(1)}$	Hold time, SCL to SDA	10			ns
t_{BUF}	Bus free time between stop and start condition	1.3			µs
$t_{su(2)}$	Setup time, SCL to start condition	0.6			µs
$t_{h(2)}$	Hold time, start condition to SCL	0.6			µs
$t_{su(3)}$	Setup time, SCL to stop condition	0.6			µs

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{start}	Start-up time	Time from I^2C write until boost and amplifier are fully enabled		2		ms

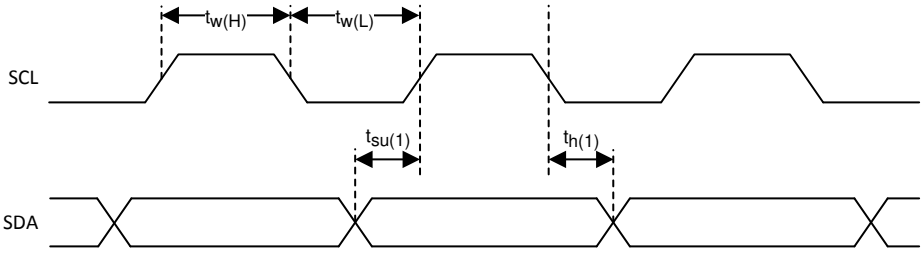


図 6-1. SCL and SDA Timing

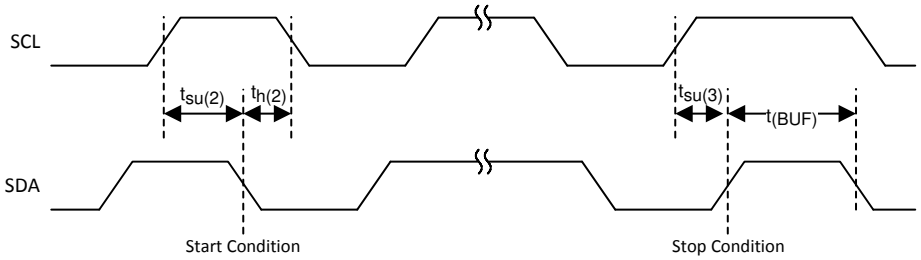
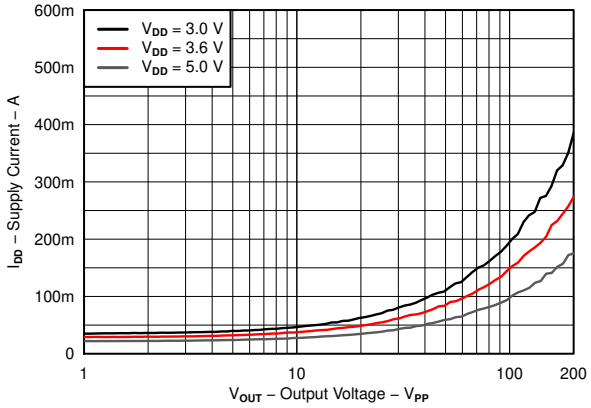


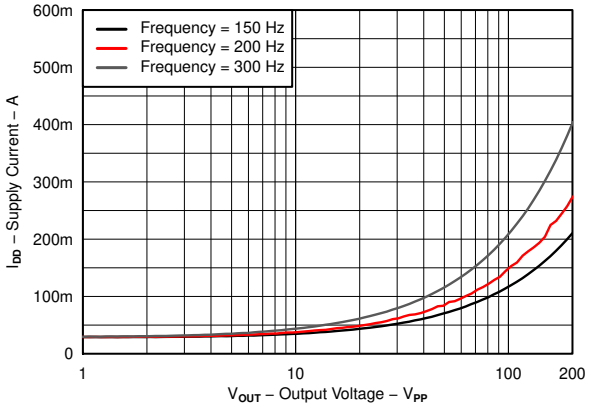
図 6-2. Timing for Start and Stop Conditions

6.8 Typical Characteristics



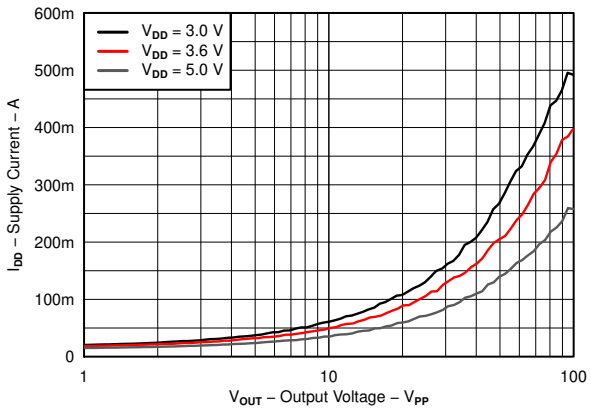
f = 200 Hz　　PVDD = 105 V
C_{LOAD} = 47 nF　　Gain = 40 dB

図 6-3. Supply Current vs Output Voltage



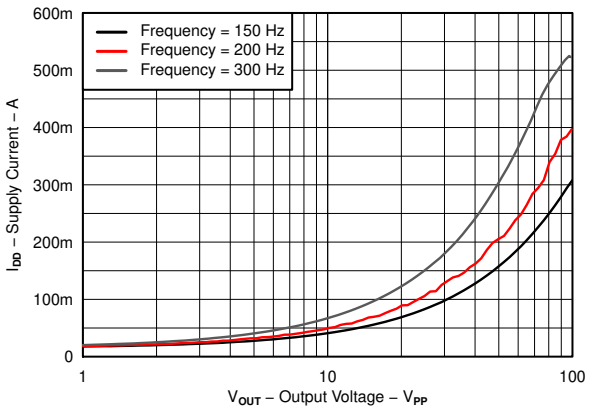
V_{DD} = 3.6 V　　PVDD = 105 V
C_{LOAD} = 47 nF　　Gain = 40 dB

図 6-4. Supply Current vs Output Voltage



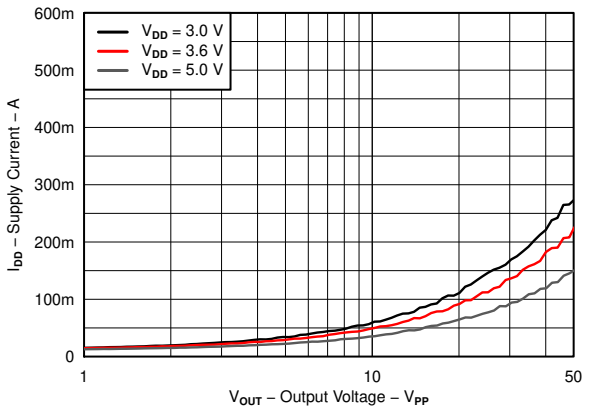
f = 200 Hz　　PVDD = 55 V
C_{LOAD} = 330 nF　　Gain = 34 dB

図 6-5. Supply Current vs Output Voltage



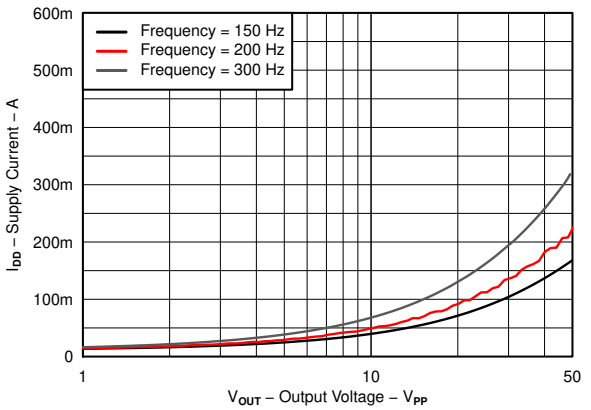
V_{DD} = 3.6 V　　PVDD = 55 V
C_{LOAD} = 330 nF　　Gain = 34 dB

図 6-6. Supply Current vs Output Voltage



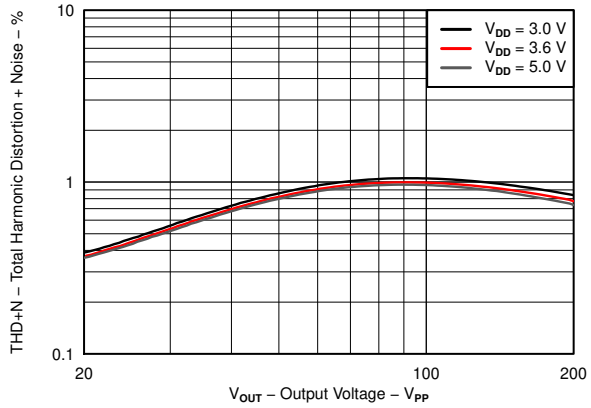
f = 200 Hz　　PVDD = 30 V
C_{LOAD} = 680 nF　　Gain = 28 dB

図 6-7. Supply Current vs Output Voltage



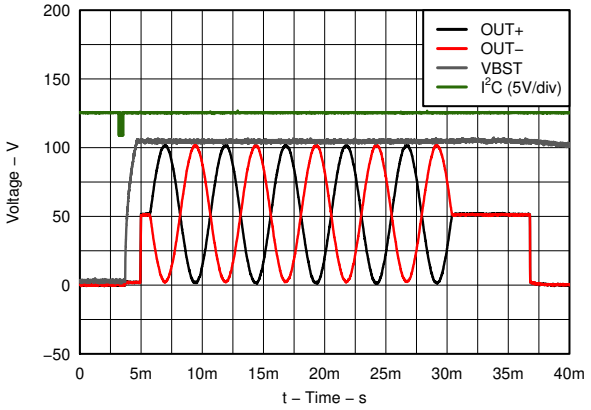
V_{DD} = 3.6 V　　PVDD = 30 V
C_{LOAD} = 680 nF　　Gain = 28 dB

図 6-8. Supply Current vs Output Voltage



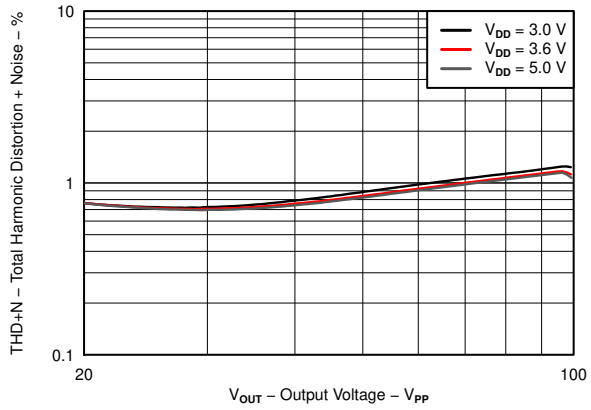
f = 200 Hz
C_{LOAD} = 47 nF
PVDD = 105 V
Gain = 40 dB

図 6-9. Total Harmonic Distortion + Noise vs Output Voltage



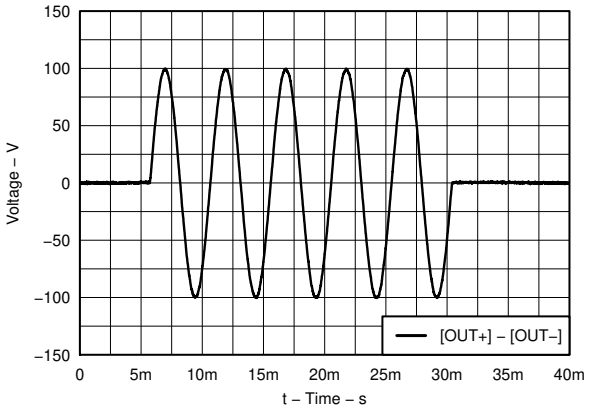
V_{DD} = 3.6 V
C_{LOAD} = 47 nF
PVDD = 105 V
Gain = 40 dB

図 6-10. Typical Waveform



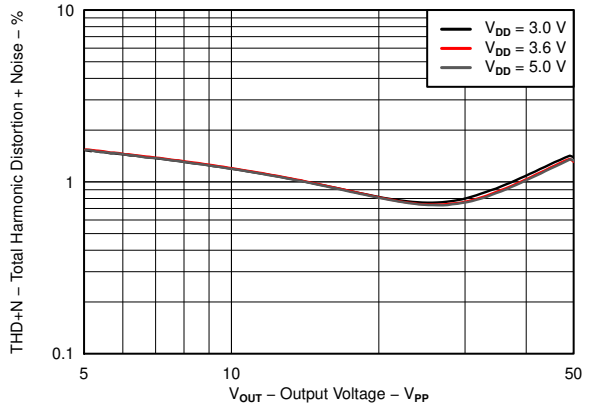
f = 200 Hz
C_{LOAD} = 330 nF
PVDD = 55 V
Gain = 34 dB

図 6-11. Total Harmonic Distortion + Noise vs Output Voltage



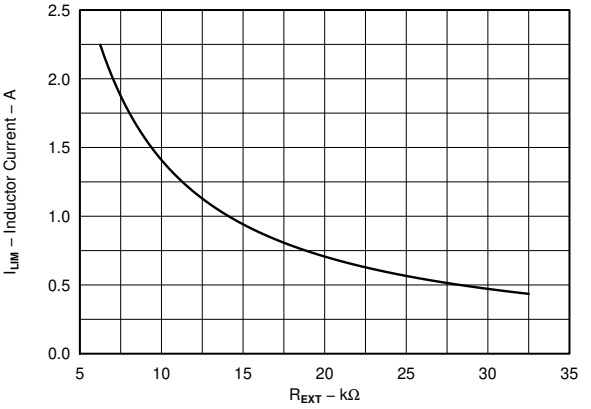
V_{DD} = 3.6 V
C_{LOAD} = 330 nF
PVDD = 55 V
Gain = 34 dB

図 6-12. Typical Waveform - Differential



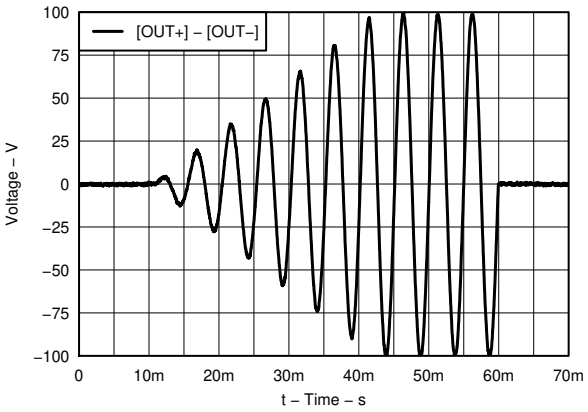
f = 200 Hz
C_{LOAD} = 680 nF
PVDD = 30 V
Gain = 28 dB

図 6-13. Total Harmonic Distortion + Noise vs Output Voltage



V_{DD} = 3.6 V
C_{LOAD} = 680 nF
PVDD = 30 V
Gain = 28 dB

図 6-14. I_{LIM} vs $R_{(EXT)}$



f = 200 Hz
C_{LOAD} = 47 nF
PVDD = 105 V
Gain = 40 dB

図 6-15. Example Waveform – Envelope Up

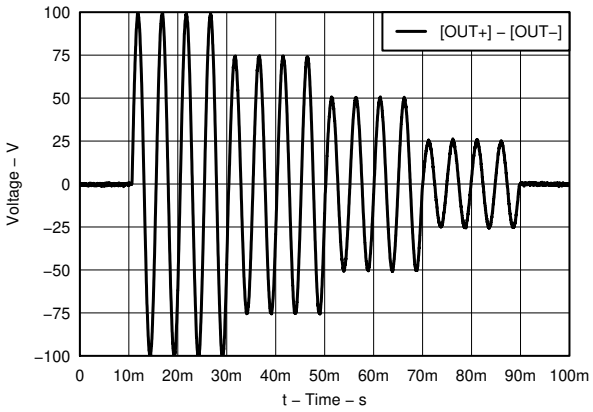


図 6-16. Example Waveform – Amplitude

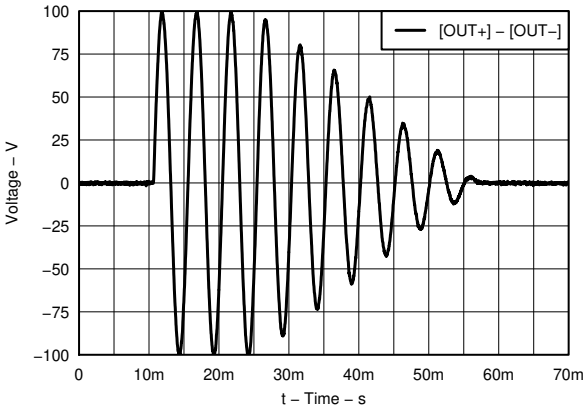


図 6-17. Example Waveform – Envelope Down

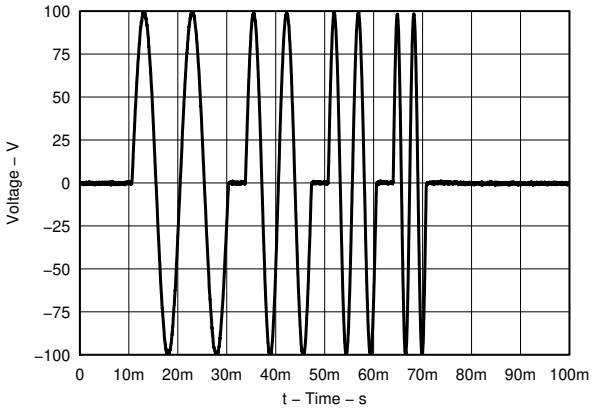


図 6-18. Example Waveform – Frequency

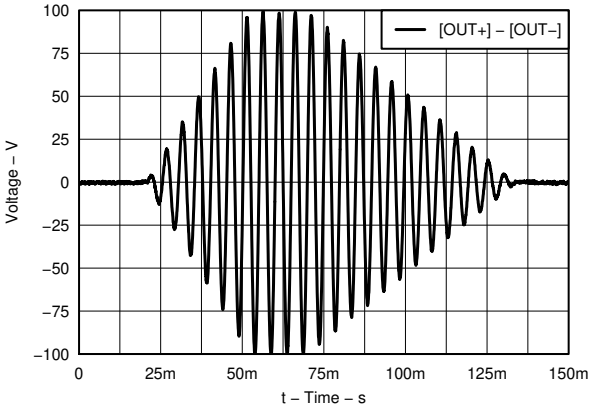


図 6-19. Example Waveform – Envelope Up and Down

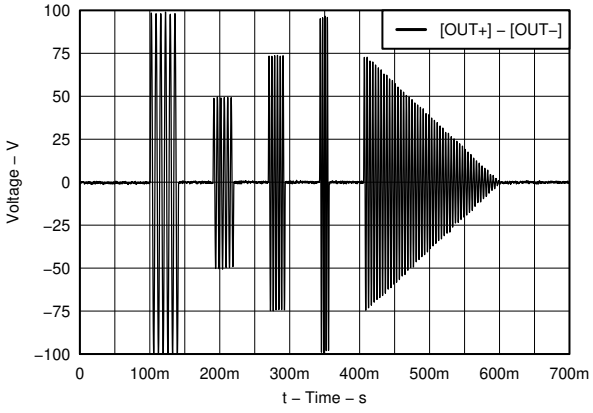


図 6-20. Example Waveform – Pinball Effect

7 Detailed Description

7.1 Overview

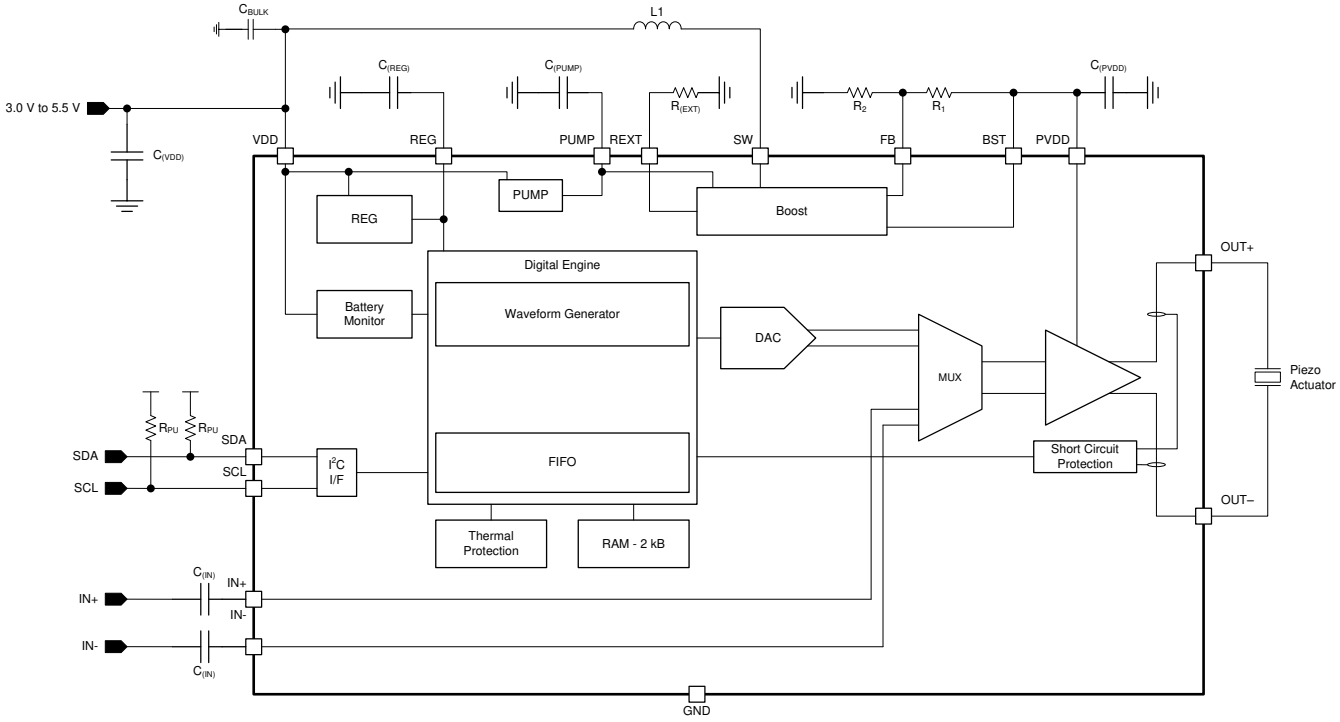
The DRV2667 device is a piezo haptic driver with integrated boost switch, integrated power diode, integrated fully-differential amplifier, and integrated digital front end. This versatile device is capable of driving both high-voltage and low-voltage piezo haptic actuators. The input signal can be driven over the I^2C port or the analog inputs.

The digital interface of the DRV2667 device is available through an I^2C compatible bus. A digital interface relieves the costly processor burden of PWM generation or additional analog channel requirements in the host system. Any writes to the internal FIFO automatically wakes up the device and begin playing the waveform after the 2 ms internal startup procedure. When the data flow stops or the FIFO under runs, the device automatically enters a pop-less shutdown procedure.

The DRV2667 device also includes waveform memory to store and recall waveforms with minimal latency as well as an advanced waveform synthesizer to construct complex haptic waveforms with minimal memory usage. This provide a means of hardware acceleration, relieving the host processor of haptic generation duties as well as minimizing bus traffic over the haptic interface.

The boost voltage is set using two external resistors, and the boost current limit is programmable through the R_{EXT} resistor. A typical start-up time of 2 ms makes the DRV2667 an ideal piezo driver for fast haptic responses. Thermal overload protection prevents the device from being damaged when overdriven.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Support for Haptic Piezo Actuators

The DRV2667 device supports haptic piezo actuators of up to 200 V_{PP}.

7.3.2 Flexible Front End Interface

The DRV2667 device supports multiple approaches to launch and control haptic effects, that are detailed in セクション 7.4.

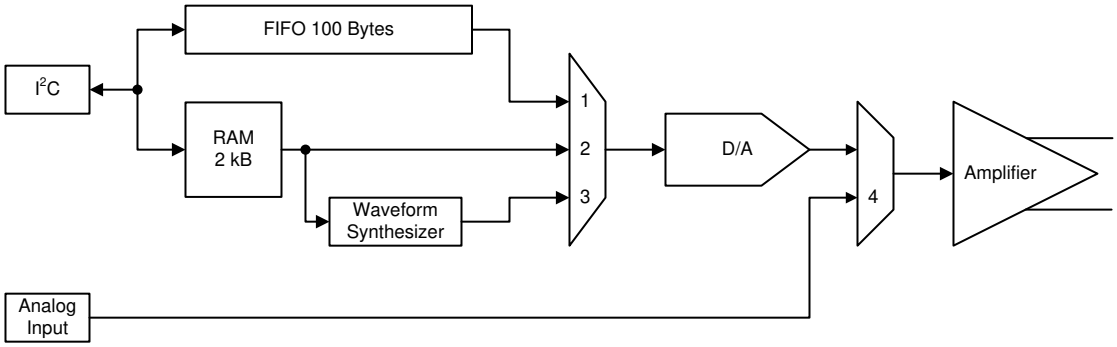


図 7-1. Front-End Interface

7.3.3 Ramp Down Behavior

If the user leaves the state of the DAC at any level other than mid-scale (0x00), the DAC automatically ramps down at a safe rate after the timeout period has expired. If the DRV2667 device is properly programmed, the ramp down sequence will never be used. This is a failsafe for any unavoidable interruptions to the playback process. Any writes to the FIFO during the ramp down period are discarded.

7.3.4 Low Latency Startup

The DRV2667 device features a fast startup time, that is essential for achieving low latency in haptic applications. When the STANDBY bit is transitioned from high to low, the device is ready for operation. The device logic automatically controls the internal boost converter and amplifier enable signals. The boost converter and amplifier are enabled only when needed and otherwise remain in a lower power idle state. When the device received a data byte through the FIFO interface, or the GO bit is asserted (in Direct Playback from RAM or Waveform Synthesis Playback modes), the boost converter and amplifier wake up and the internal logic sends the first sample through the internal DAC after the wake-up is completed. In the system application, the entire system latency must be kept to less than 30 ms total to be imperceptible to the end user. At a 2-ms wake-up time, the device is a small percentage of the total system latency.

If the EN_OVERRIDE bit is set, the device immediately enters the startup procedure and the boost converter and amplifier remain enabled, bypassing the internal controls. Subsequent transactions occur immediately with no wake-up overhead, but the boost converter and amplifier draw a quiescent current until the EN_OVERRIDE bit is cleared by the user.

7.3.5 Low Power Standby Mode

The DRV2667 device has a low-power standby mode through the I^2C interface that puts the device in its lowest power state. This mode is entered when the standby bit (STANDBY) is set from low to high. When the STANDBY bit is set high, no other mode of operation is enabled. When the STANDBY bit transitions from high to low, the device is readied for operation and may receive data.

7.3.6 Device Reset

The DRV2667 device has software-based reset functionality. When the DEV_RST bit is set, the device immediately stops any transaction in process, resets all of its internal registers to the default values, and enters standby mode.

7.3.7 Amplifier Gain

The amplifier gain determines the gain from IN+/IN– to OUT+/OUT– when using the analog playback mode. For digital playback, the gain is optimized for achieving approximately 50 V_{PP}, 100 V_{PP}, 150 V_{PP}, 200 V_{PP} without clipping. Note that clipping of the amplifier occurs if the expected peak voltage is greater than the boost converter output voltage (VBST)

The DRV2667 device gain is programmable according to 表 7-1.

表 7-1. Amplifier Gain Table

GAIN[1]	GAIN[0]	FULL SCALE PEAK VOLTAGE (V)	GAIN (dB) ANALOG MODE
0	0	25	28.8
0	1	50	34.8
1	0	75	38.4
1	1	100	40.7

7.3.8 Adjustable Boost Voltage

The output voltage of the integrated boost converter may be adjusted by a resistive feedback divider between the boost output voltage (VBST) and the feedback pin (FB). The boost voltage must be programmed to a value greater than the maximum peak signal voltage that the user expects to create with the device amplifier. Lower boost voltages achieve better system efficiency when lower amplitude signals are applied, thus the user must take care not to use a higher boost voltage than necessary. The maximum allowed boost voltage is 105 V.

7.3.9 Adjustable Current Limit

The current limit of the boost switch can be adjusted through a resistor to ground placed on the REXT pin. To avoid damage to both the inductor and the DRV2667 device, the programmed current limit must be less than the rated saturation limit of the inductor selected by the user. If the combination of the programmed limit and inductor saturation is not high enough, then the output current of the boost converter will not be high enough to regulate the boost output voltage under heavy load conditions. This then causes the boosted rail to sag, possibly causing distortion of the output waveform.

7.3.10 Internal Charge Pump

The DRV2667 device has an integrated charge pump to provide adequate gate drive for internal nodes. The output of this charge pump is placed on the PUMP pin. An X5R or X7R storage capacitor of 0.1 µF with a voltage rating of 10 V or greater must be placed at this pin.

7.3.11 Device Protection

7.3.11.1 Thermal Protection

The DRV2667 device contains an internal temperature sensor that shuts down both the boost converter and the high-voltage amplifier when the temperature threshold is exceeded. When the device temperature falls below the threshold, the device will restart operation automatically. Continuous operation of the device is not recommended. Most haptic use models only operate the device in short bursts. The thermal shutdown function protects the device from damage when overdriven, but usage models which drive the device into thermal shutdown must always be avoided.

7.3.11.2 Overcurrent Protection

If the load demands more current than what the DRV2667 device can supply, the device automatically clamps the output voltage to avoid damage.

7.3.11.3 Brownout Protection

The DRV2667 device has on-chip brownout protection. When activated, a reset signal is issued that returns the DRV2667 device to the initial default state. If the voltage regulator V_{REG} goes below the brownout protection threshold (V_{BOT}) the DRV2667 device automatically shuts down. When V_{REG} returns to the typical output voltage (1.75 V), the DRV2667 device returns to the initial device state. The brownout protection threshold, V_{BOT}, is typically at 0.84 V.

There is one exception to this behavior. The brownout circuit is designed to tolerate fast brownout conditions as shown by Case 1 in 図 7-2. If the V_{DD} ramp-up rate is slower than 3.6 kV/s, then the device can fall into an unknown state. In such a situation, to return to the initial default state the device must be power-cycled with a V_{DD} ramp-up rate that is faster than 3.6 kV/s.

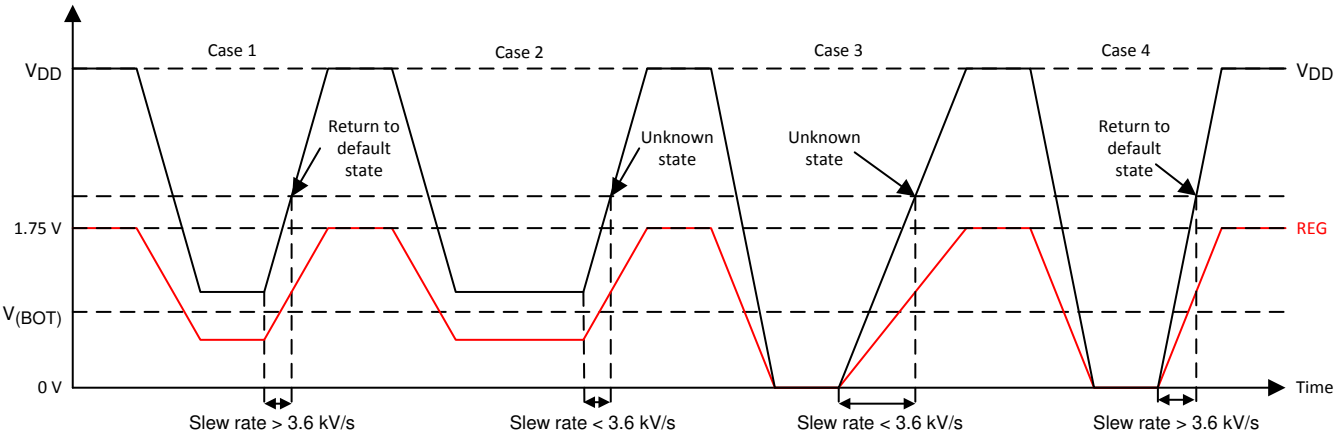


図 7-2. Brownout Behavior

7.4 Device Functional Modes

7.4.1 FIFO Mode

The DRV2667 device includes a 100-byte FIFO for real-time haptic waveform playback. The FIFO mode accepts 8-bit digital haptic waveform data over an I^2C compatible bus and writes it into an on-chip FIFO. The data is read out of the FIFO automatically at an 8-kHz sampling rate and fed into a digital-to-analog converter (DAC). The DAC then drives the high-voltage amplifier. This mode is utilized when the user writes directly to the I^2C FIFO entry address (0x0B). When the first data byte is written to the FIFO, the device goes through the proper start-up sequence and begins outputting the waveform automatically. An internal timing sequence waits approximately 2 ms before the first data is sent through the DAC and output by the device. It is important that the data values start and end at or near the mid-scale code (0x00) to avoid large steps at the beginning and end of the waveform. When the FIFO is empty, the device waits for the timeout period (see *セクション 7.4.1.1*), and then enters into an idle state.

Because the speed of the serial interface could be faster than the read-out rate of the FIFO, the device issues a "not acknowledge" or "NAK" if the FIFO is full during a FIFO write transaction. If at any time the FIFO becomes completely full, the FIFO_FULL bit is set. When in this condition, the FIFO cannot accept more data without overwriting previous data that has not yet been played. If this occurs, the user must wait until data has had a chance to empty from the FIFO before sending more data. The data must be re-sent starting at the byte that received a NAK.

Any multi-byte I^2C write to the FIFO register is treated as a continuous write to the FIFO. Multi-byte writes are preferred for optimum performance. The FIFO interprets the incoming data as twos complement. This means the maximum full-scale code is 0x7F, the maximum negative voltage is 0x80, and the mid-scale is 0x00.

7.4.1.1 Waveform Timeout

The DRV2667 device has a timeout period after the FIFO has emptied. This timeout period allows the user time to send a subsequent waveform before the device logic puts the device into idle mode, that then allows the host processor time to cue up an adjoining waveform from memory. After the timeout expires, the DRV2667 device must re-enter the 2 ms startup sequence before the next waveform plays. The timeout period is register-selectable to be 5, 10, 15 or 20 ms.

7.4.2 Direct Playback from RAM Mode

The Direct Playback from RAM mode makes use of the on-chip 2 kB of RAM for internal waveform storage. This mode allows for immediate, low-latency recall of arbitrary haptic waveforms with very little intervention from the host processor. Haptic waveforms, be they simple or complex, may be stored in this memory at opportune times when immediate processor response is not critical. Examples of this are when the end-user product is being powered up and initialized or when an application is being launched.

The waveforms are stored as 8-bit twos-complement, Nyquist-rate data points, and are played from RAM at an 8-kHz data rate. Up to 250 ms of total waveform playback time may be stored in the Direct Playback From RAM mode format in the 2-kB memory. The waveform sizes are completely customizable, so many small waveforms may be stored or fewer long ones. The sum of the waveform lengths must not be greater than the 2-kB RAM size.

7.4.3 Waveform Synthesis Playback Mode

The Waveform Synthesis Playback mode is a very powerful and an efficient way of utilizing the on-chip RAM while retaining all of the low-latency and low-processor overhead benefits of the Direct Playback From RAM mode. In this mode, the actual playback data is not explicitly stored, it is synthesized based on simple sinusoidal waveform "chunks". Each sinusoidal chunk consists of the following bytes:

- Amplitude
- Frequency
- Number of Cycles (Duration)
- Envelope

Using this method, multiple chunks may be cascaded together to form a wide variety of haptic effects. In addition to programming frequency, amplitude and duration bytes, the envelope byte allows individual amplitude ramps of various rates to be applied to the beginning and end of each chunk. The Waveform Synthesis Playback mode equips the user with powerful tools to store a virtually infinite tapestry of effects in device memory.

7.4.4 Waveform Sequencer

For the Direct Playback from RAM and the Waveform Synthesis Playback modes, waveform identifiers are stored sequentially into a waveform header at the beginning of the waveform memory. Each waveform may be called out from memory during playback by its individual waveform identifier using the waveform sequencer. The waveform sequencer allows the user to cascade up to eight waveforms together, that can be played either as a direct waveform or a synthesized waveform using the Direct Playback from RAM and Waveform Synthesis Playback methods. When the waveform memory and the waveform sequencer are populated, this powerful feature allows the host processor to fire a chain of up to eight cascaded effects with a single I^2C register write.

7.4.5 Analog Playback Mode

In analog playback mode the signal in the IN+/IN– inputs is amplified and played through the high-voltage amplifier. When the INPUT_MUX bit is set, the DRV2667 device switches the analog inputs (IN+/IN–) to the high-voltage amplifier. While in the analog mode, the gain is still register-selectable. Also, the high-voltage amplifier enable is controlled directly through the EN_OVERRIDE bit, so the EN_OVERRIDE bit must be set for the boost and amplifier to be active.

7.4.6 Low Voltage Operation Mode

The lowest gain setting is optimized for 50 V_{PP} with a boost voltage of 30 V. Some applications may not need 50 V_{PP}, so the user may elect to program the boost converter as low as 15 V to improve efficiency. When using boost voltages lower than 30 V, consider the following: First, to reduce boost ripple to an acceptable level, a 50-V rater, 0.22-µF boost capacitor is recommended. Second, the maximum code range of the digital interface is limited. For example, the user may elect to program the boost voltage to 25 V, and plan for a maximum drive signal of 40 V_{PP} at the actuator. Any digital code given to the FIFO that is greater than 20 V_P / 25 V_P x 127 = ±102 may induce clipping, so the user must only send digital codes between –102 and 102. Use of codes outside this range, for this example, may clip or drive the actuator beyond its rating.

7.5 Programming

7.5.1 Programming the Boost Voltage

The boost output voltage is programmed through two external resistors as shown in 図 7-3. The boost output voltage is given by 式 1.

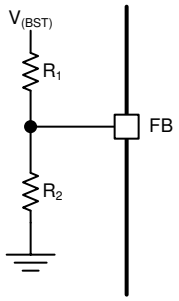


図 7-3. FB Network

$$V_{(BST)} = V_{(FB)} \cdot \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where

- $V_{(FB)}$ = 1.32 V

$V_{(BST)}$ must be programmed to a value of 5.0 V greater than the largest peak voltage expected in the system to allow adequate amplifier headroom. Because the programming range for the boost voltage extends to 105 V, the leakage current through the resistor divider can become significant. It is recommended that the sum of the resistances R_1 + R_2 be greater than 400 kΩ. When resistor values greater than 1 MΩ are used, PCB contamination may cause boost voltage inaccuracy. Exercise caution when soldering large resistances, and clean the area when finished for best results. 表 7-2 shows examples on how to configure the device for different output voltages.

表 7-2. Boost Voltage Table

R_1	R_2	GAIN[1:0]	$V_{(BST)}$	FULL SCALE PEAK VOLTAGE (V)
402 kΩ	18.2 kΩ	00	30	25
392 kΩ	9.76 kΩ	01	55	50
768 kΩ	13 kΩ	10	80	75
768 kΩ	9.76 kΩ	11	105	100

7.5.2 Programming the Boost Current Limit

The peak current drawn from the supply through the inductor is set solely by the $R_{(EXT)}$ resistor. This peak current limit is independent of the inductance value chosen, but the inductor must be capable of handling this programmed limit. The relationship of $R_{(EXT)}$ and I_{LIM} is approximated by 式 2.

$$R_{(EXT)} = \left(K \cdot \frac{V_{REF}}{I_{LIM}}\right) - R_{INT} \quad (2)$$

where

- K = 10500, , and
- V_{REF} = 1.35 V
- R_{INT} = 60 Ω
- I_{LIM} is the desired peak current limit through the inductor.

7.5.3 Programming the RAM

7.5.3.1 Accessing the RAM

To maintain compatibility with the majority of standard I^2C controllers, the DRV2667 device uses 8-bit addressing. To access 2 kB of RAM, a paging system is employed. The page register is located at address 0xFF.

There are 8 memory pages that make up the 2048 bytes with 256 bytes on each page. Note that page 0 is reserved for register control space, as shown in 図 7-4.

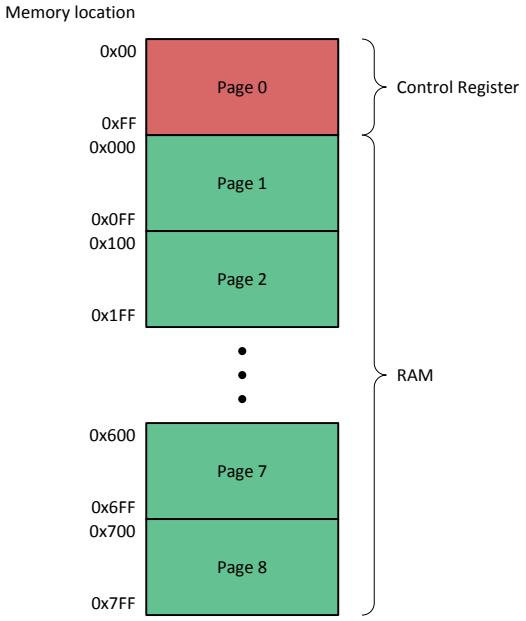


図 7-4. Page Structure

Because the device addresses are only 8-bits, a special exception exists to distinguish whether the user is trying to write the page register at address 0xFF or the memory location at 0xPFF, where P represents the page number. In order to access the page register, the programmer must use a Single-Byte I^2C protocol to perform a single-byte write to memory location 0xFF (see *セクション 7.5.4.3*). To access the memory location in RAM at register 0xFF, the user must use the Incremental Multiple-Byte protocol (see *セクション 7.5.4.4*), and the beginning address must be less than 0xFF.

The page register automatically increments for multiple-byte writes that cross the page boundaries, as a convenience for filling memory across multiple pages. Multiple-byte reads across page boundaries are not supported. All memory is retained in the device until the device power is cycled.

7.5.3.2 RAM Format

The RAM is structured into 3 main blocks as shown in 図 7-5:

- Header size block; 1 byte
- Header block; *N* x 5 bytes, where *N* is the number of effects stored
- Waveform data block

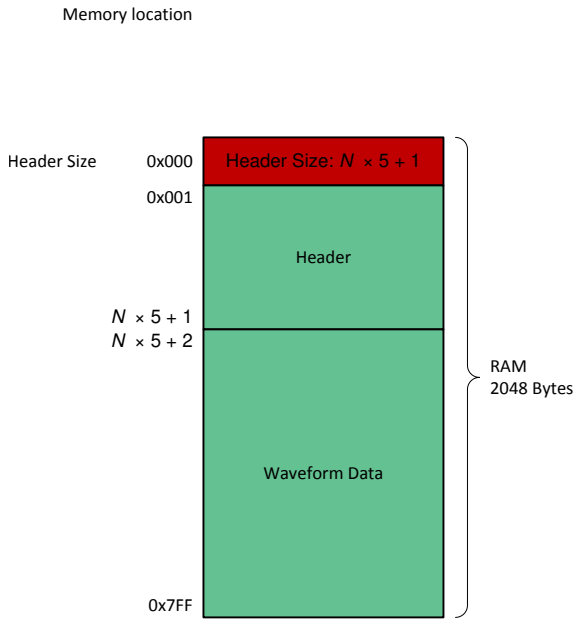


図 7-5. RAM Structure

The first byte of the RAM (at memory location 0x00 on Page 1) must contain the header size. The header size refers to the last byte in the header, so the value stored must be *N* x 5 + 1, as shown in 図 7-5.

The header block describes the location of the waveform data content. The structure of the header consists of 5-byte blocks containing the following information (see 図 7-6):

- Start address, upper byte
- Start address, lower byte
- Stop address, upper byte
- Stop address, lower byte
- Repeat count

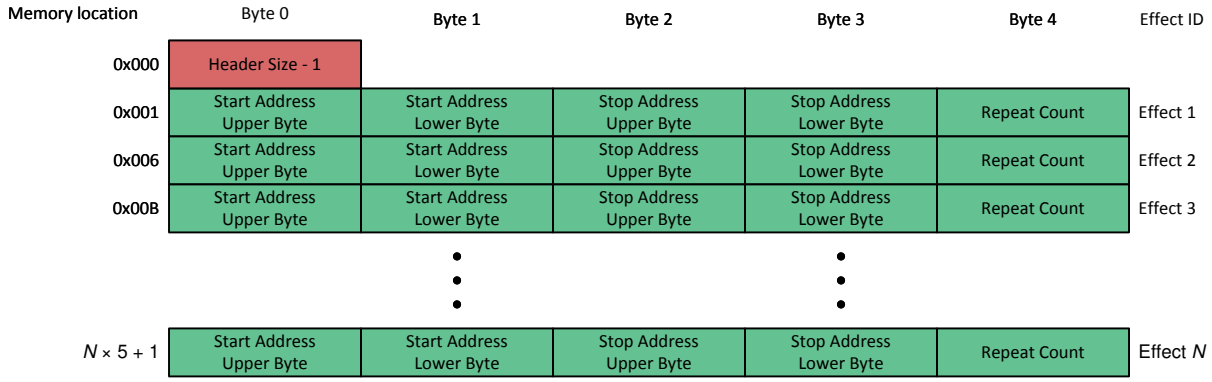


図 7-6. Header Format

Because more than 8-bits are required to address the 2 kB of memory, each start and stop address consists of two bytes. The start address contains the location of the first byte in the waveform and the stop byte contains the locations of the last byte in the waveform. Within the address byte, the upper byte contains the page address, and the lower byte refers to the specified address within the page (see 図 7-7). The upper byte interprets a 0 as Page 1, and a 7 as Page 8 because the waveform processing engine cannot access the control space in Page 0.

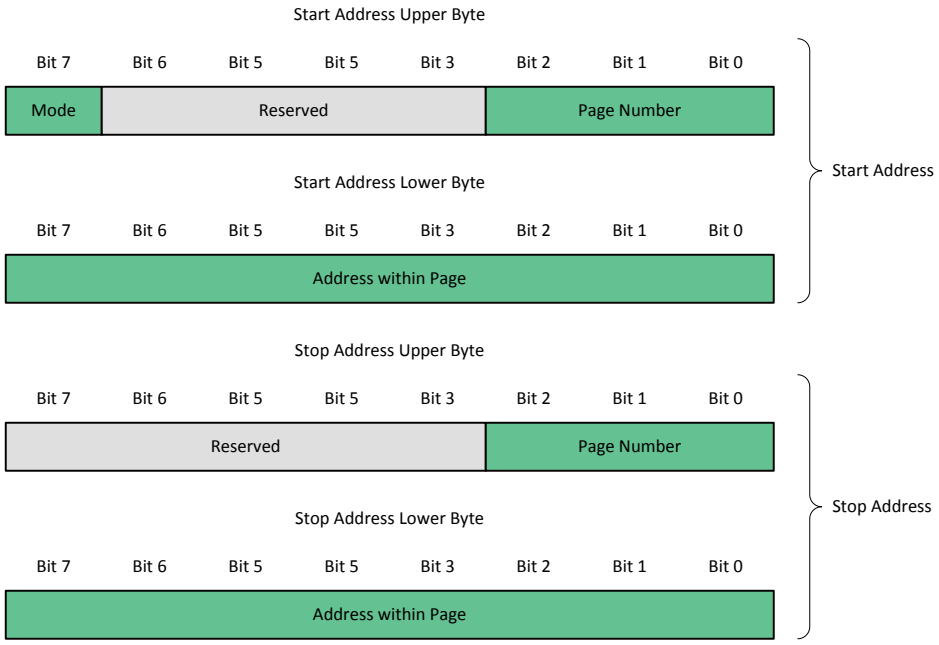


図 7-7. Header Address Byte Format

The repeat count byte contains the number of times this waveform identifier (which starts at the start address and ends at the stop address) is to be repeated when it is called during playback. A 0 in this byte is interpreted as an infinite loop and the waveform is played indefinitely until the GO bit is cleared by the user. Otherwise, the repeat count is simply the number of times that the waveform is repeated.

The waveform data can be interpreted in two ways:

- Direct Playback from RAM mode
- Waveform Synthesis Playback mode

Note that both modes can be stored in the RAM, and the device interprets the waveform data according to the mode specified. To signal the device which mode is desired, the MSB of the start address, upper byte is used (see 図 7-7). A 0 indicates Direct Playback from RAM Mode, and a 1 indicates a Waveform Synthesis Playback Mode.

The Direct Playback from RAM mode requires no special handling: the waveform starts at the start-address location and plays each sub-sequent byte at the Nyquist-rate. The data is stored in twos complement, where 0xFF is interpreted as full-scale, 0x00 is no signal, and 0x80 is negative full-scale. The waveform is played at an 8-kHz data rate.

The Waveform Synthesis Playback Mode stores data in sinusoidal chunks, where each chunk consists of four bytes as shown in 図 7-8:

- Amplitude
- Frequency
- Number of Cycles (Duration)
- Envelope

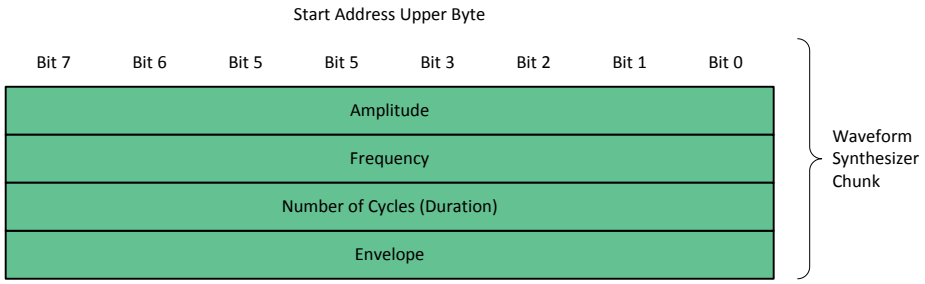


図 7-8. Waveform Synthesizer Format

The interpretation of each of these four bytes is outlined in 表 7-3.

表 7-3. Waveform Chunk Bytes for Synthesizer

BYTE	NAME	DESCRIPTION
1	Amplitude	The amplitude byte refers to the magnitude of the synthesized sinusoid. 0xFF produces a full-scale sinusoid, 0x80 produces a half-scale sinusoid, and 0x00 does not produce any signal. An amplitude of 0x00 can be useful for producing timed waits or delays within the effect. To calculate the absolute peak voltage, use the following equation, where *amplitude* is a single-byte integer: Peak voltage = amplitude / 255 x full-scale peak voltage
2	Frequency	The frequency byte adjusts the frequency of the synthesized sinusoid. The minimum frequency is 7.8125 Hz. A value of zero is not allowed. The sinusoidal frequency is determined with the following equation, where *frequency* is a single-byte integer: Sinusoid frequency (Hz) = 7.8125 x frequency
3	Number of Cycles (Duration)	The number of sinusoidal cycles to be played by the synthesizer. A convenient way to specify the duration of a coherent sinusoid is by inputting the number of cycles. This method ensures that the waveform chunk will always begin and end at zero amplitude, thus avoiding discontinuities. The actual duration in time given by this value may be calculated through the following equation, where *# of cycles* and *frequency* are both single-byte integers. Duration (ms) = 1000 x # of cycles / (7.8125 x frequency)

表 7-3. Waveform Chunk Bytes for Synthesizer (continued)

BYTE	NAME	DESCRIPTION	
4	Envelope	The envelope byte is divided into two nibbles. The upper nibble, bits [7:4], sets the ramp-up rate at the beginning of the synthesized sinusoid, and the lower nibble, bits [3:0], sets the ramp-down rate at the end of the synthesized sinusoid. The user must note that the ramp-up time is included in the duration parameter of the waveform, and the ramp-down time is appended to the duration parameter of the waveform. As such, if a ramp-up time is used, the ramp-up time must be less than the duration time as programmed in byte 3. Also note that the *Total Ramp Time* is for a ramp to full-scale amplitude (amplitude = 0xFF). Ramps to a fraction of full-scale have the same fraction of the *Total Ramp Time*.	
		Nibble Value	Total Ramp Time
		0	No Envelope
		1	32 ms
		2	64 ms
		3	96 ms
		4	128 ms
		5	160 ms
		6	192 ms
		7	224 ms
		8	256 ms
		9	512 ms
		10	768 ms
		11	1024 ms
		12	1280 ms
		13	1536 ms
		14	1792 ms
		15	2048 ms

7.5.3.2.1 Programming the Waveform Sequencer

To play the effects stored in memory, the effects must be loaded into the waveform sequencer. The effects can then be launched by the use of the GO bit.

The waveform sequencer queues up to eight waveform identifiers for playback. A waveform identifier is an integer value referring to the index position of a waveform in the Header Block (see 図 7-6). Upon assertion of the GO bit, playback begins at register 0x03. When playback of that waveform ends, the waveform sequencer plays the next waveform identifier in register 0x04 if the identifier stored in register 0x04 is non-zero. Th waveform sequencer continues in this way until the sequencer reaches an identifier value of zero or until all eight identifiers are played as shown in 図 7-9.

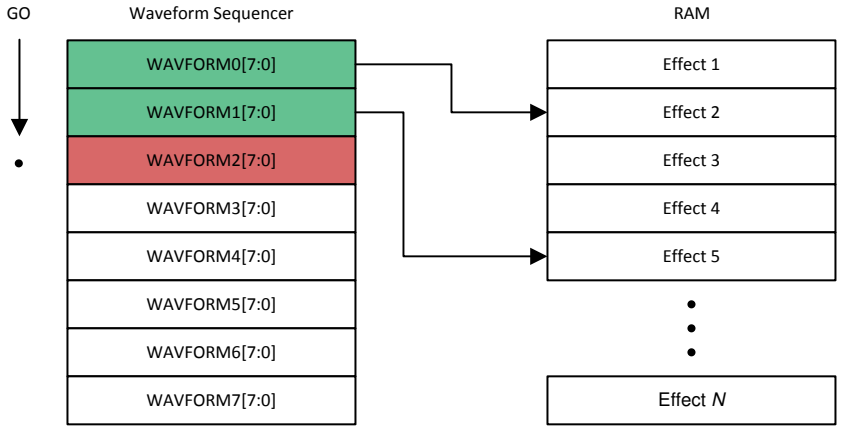


図 7-9. Waveform Sequencer

7.5.4 I²C Interface

7.5.4.1 General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The bus transfers data serially, one bit at a time. The 8-bit address and data bytes are transferred with the most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on the SDA signal indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. 図 7-10 shows a typical sequence. The master device generates the 7-bit slave address and the read-write (R/W) bit to start communication with a slave device. The master device then waits for an acknowledge condition. The slave device holds the SDA signal low during the acknowledge clock period to indicate acknowledgment. When this acknowledgment occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus a R/W bit (1 byte). All compatible devices share the same signals through a bidirectional bus using a wired-AND connection.

The number of bytes that can be transmitted between start and stop conditions is not limited. When the last word transfers, the master generates a stop condition to release the bus. 図 7-10 shows a generic data-transfer sequence.

Use external pullup resistors for the SDA and SCL signals to set the logic-high level for the bus. Pullup resistors with values between 660 Ω and 4.7 kΩ are recommended. Do not allow the SDA and SCL voltages to exceed the DRV2667 supply voltage, V_{DD}.

The DRV2667 device operates as an I²C-slave with 1.8-V logic thresholds, but can operate up to the V_{DD} voltage.

注

The slave address for the DRV2667 device is 0x59 (7-bit), or 1011001 in binary, which is equivalent to 0xB2 (8-bit) for writing and 0xB3 (8-bit) for reading.

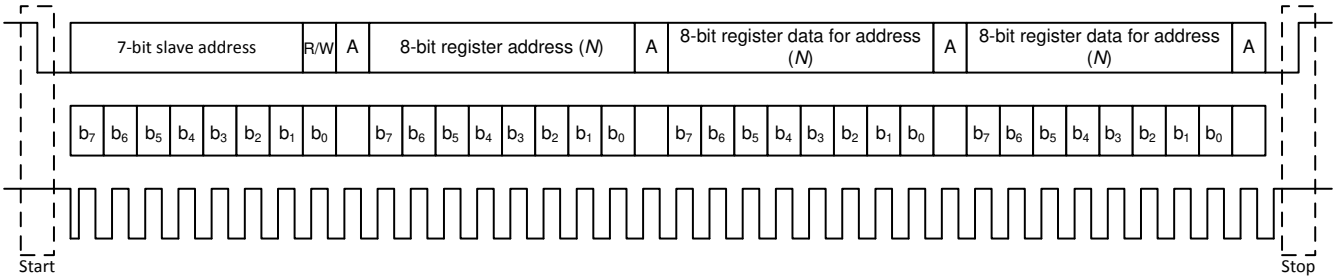


図 7-10. Typical I²C Sequence

7.5.4.2 Single-Byte and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read-write operations for all registers.

During multi-byte transactions, the register address provided serves as the starting address. Subsequent data transfers automatically increment the register address accessed until a stop condition is reached.

7.5.4.3 Single-Byte Write

As shown in 図 7-11, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read-write bit. The read-write bit determines the direction of the data transfer. For a write-data transfer, the read-write bit must be set to 0. After receiving the correct I²C device address and the read-write bit, the DRV2667 device responds with an acknowledge bit. Next, the master

transmits the register byte corresponding to the DRV2667 internal-memory address that is accessed. After receiving the register byte, the device responds again with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

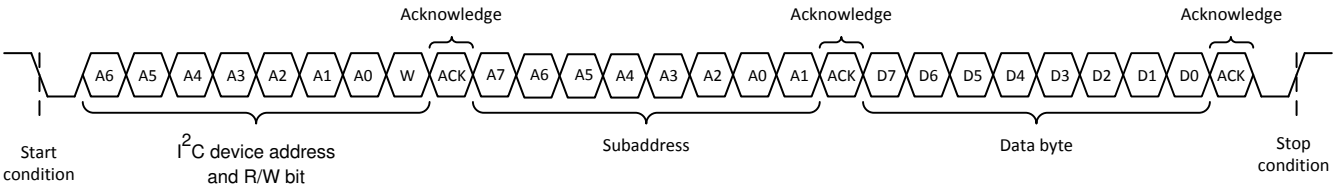


図 7-11. Single-Byte Write Transfer

7.5.4.4 Multiple-Byte Write and Incremental Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DRV2667 device. After receiving each data byte, the DRV2667 device responds with an acknowledge bit as shown in 図 7-12.

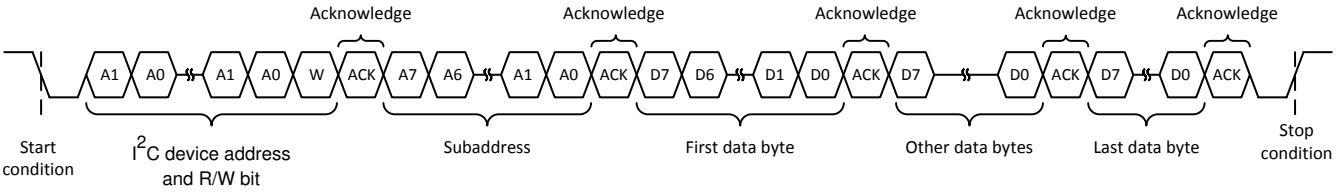


図 7-12. Multiple-Byte Write Transfer

7.5.4.5 Single-Byte Read

図 7-13 shows that a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read-write bit. For the data-read transfer, both a write followed by a read actually occur. Initially, a write occurs to transfer the address byte of the internal memory address to be read. As a result, the read-write bit is set to 0.

After receiving the DRV2667 address and the read-write bit, the DRV2667 device responds with an acknowledge bit. The master then sends the internal memory address byte, after which the device issues an acknowledge bit. The master device transmits another start condition followed by the DRV2667 address and the read-write bit again. This time, the read-write bit is set to 1, indicating a read transfer. Next, the DRV2667 device transmits the data byte from the memory address that is read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer. See the note in the *セクション 7.5.4.1* section for the device address.

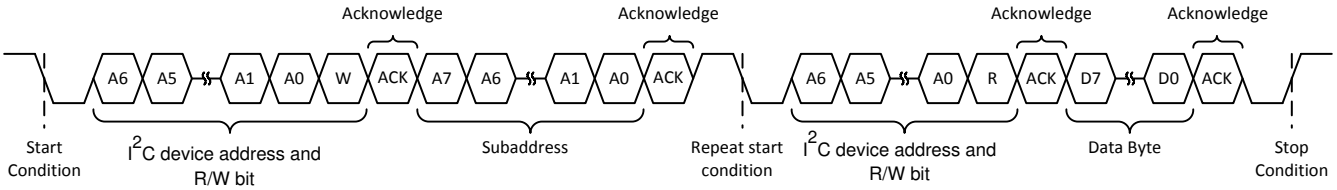


図 7-13. Single-Byte Read Transfer

7.5.4.6 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the DRV2667 device to the master device as shown in 図 7-14. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

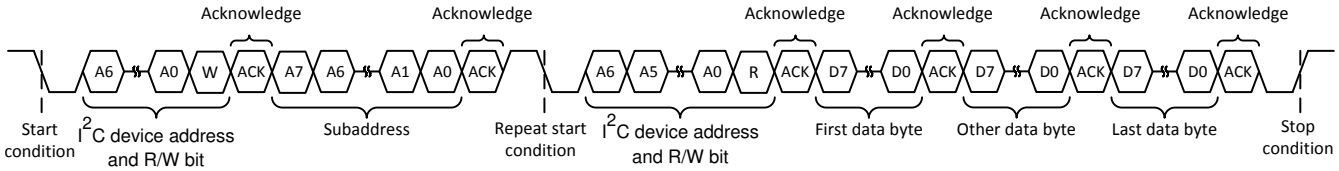


図 7-14. Multiple-Byte Read Transfer

7.6 Register Map

表 7-4. Register Map Overview

REG NO.	DEFAULT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x00	0x02	Reserved					ILLEGAL_ADDR	FIFO_EMPTY	FIFO_FULL
0x01	0x38	Reserved	CHIPID[3:0]				INPUT_MUX	GAIN[1:0]	
0x02	0x40	DEV_RST	STANDBY	Reserved		TIMEOUT[1:0]		EN_OVERRIDE	GO
0x03	0x00	WAVFORM0[7:0]							
0x04	0x00	WAVFORM1[7:0]							
0x05	0x00	WAVFORM2[7:0]							
0x06	0x00	WAVFORM3[7:0]							
0x07	0x00	WAVFORM4[7:0]							
0x08	0x00	WAVFORM5[7:0]							
0x09	0x00	WAVFORM6[7:0]							
0x0A	0x00	WAVFORM7[7:0]							
0x0B	0x00	FIFO[7:0]							
0xFF	0x00	PAGE[7:0]							

表 7-5. EEPROM Map Overview

REG NO.	DEFAULT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x01	0x38	Reserved	CHIPID[3:0]						

7.6.1 Address: 0x00

図 7-15. 0x00

7	6	5	4	3	2	1	0
Reserved					ILLEGAL_ADDR[0]	FIFO_EMPTY[0]	FIFO_FULL[0]
					RO-0	RO-1	RO-0

表 7-6. Address: 0x00

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7-3	Reserved			
2	ILLEGAL_ADDR	RO	0	Indicates that the waveform generator attempted to perform an illegal operation. This usually means that the user entered improper header information in the waveform memory. 0 Normal operation 1 Illegal address attempted
1	FIFO_EMPTY	RO	1	Indicates that the internal 100-byte FIFO is empty. 0 FIFO is not empty 1 FIFO is empty
0	FIFO_FULL	RO	0	Indicates that the internal 100-byte FIFO is full and cannot accept data until another byte has played through the internal DAC. 0 FIFO not full 1 FIFO is full

7.6.2 Address: 0x01

図 7-16. 0x01

7	6	5	4	3	2	1	0
Reserved	CHIPID[3:0]				INPUT_MUX[0]	GAIN[1:0]	
	RW-0	RW-1	RW-1	RW-1	R/W-0	R/W-0	R/W-0

表 7-7. Address: 0x01

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	Reserved			
6-3	CHIPID[3:0]	RW	7	Identifies the device. 5 DRV2665 7 DRV2667
2	INPUT_MUX	R/W	0	Selects the source to be played. 0 Digital input source 1 Analog input source
1-0	GAIN[1:0]	R/W	0	Selects the gain for the amplifier. 0 25 V (Digital) - 28.8 dB (Analog) 1 50 V (Digital) - 34.8 dB (Analog) 2 75 V (Digital) - 38.4 dB (Analog) 3 100 V (Digital) - 40.7 dB (Analog)

7.6.3 Address: 0x02

図 7-17. 0x02

7	6	5	4	3	2	1	0
DEV_RST[0]	STANDBY[0]	Reserved		TIMEOUT[1:0]		EN_OVERRIDE[0]	GO[0]

図 7-17. 0x02 (continued)

R/W-0	R/W-1			R/W-0	R/W-0	R/W-0	R/W-0

表 7-8. Address: 0x02

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	DEV_RST	R/W	0	When asserted, the device will immediately stop any transaction in process, reset all of its internal register to their default values, and enters standby mode. 0 Normal operation 1 Reset device
6	STANDBY	R/W	1	Low-power standby 0 Device is active and ready to receive a signal. 1 Device is in low-power standby mode
5-4	Reserved			
3-2	TIMEOUT[1:0]	R/W	0	Time period when the FIFO runs empty and the device goes into idle mode, powering down the boost converter and amplifier. 0 5 ms 1 10 ms 2 15 ms 3 20 ms
1	EN_OVERRIDE	R/W	0	Override bit for the boost converter and amplifier enables. 0 Boost converter and amplifier enables are controlled by device logic. 1 Boost converter and amplifier are enabled indefinitely.
0	GO	R/W	0	Starts waveform playback, as indicated by the sequence registers 0x03 through 0x0A. This bit remains high during the execution of waveform playback, and self-clears upon completion of playback. The user may optionally clear this bit to cancel waveform playback. 0 No waveform playing 1 Play (playing) waveform

7.6.4 Address: 0x03

図 7-18. 0x03

7	6	5	4	3	2	1	0
WAVFORM0[7:0]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-9. Address: 0x03

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7-0	WAVFORM0[7:0]	R/W	0	When the GO bit is asserted, the waveform processing engine will go to register address 0x03 and play the waveform ID that is indicated there. After completion of that waveform, the engine proceeds to register address 0x04 to play that waveform ID. If the ID value is zero, the playback process terminates. Otherwise this process repeats until it finds a waveform ID of zero, or all 8 waveforms are played.

7.6.5 Address: 0x04

図 7-19. 0x04

7	6	5	4	3	2	1	0
WAVFORM1[7:0]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-10. Address: 0x04

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7-0	WAVFORM1[7:0]	R/W	0	When the GO bit is asserted, the waveform processing engine will go to register address 0x03 and play the waveform ID that is indicated there. After completion of that waveform, the engine proceeds to register address 0x04 to play that waveform ID. If the ID value is zero, the playback process terminates. Otherwise this process repeats until it finds a waveform ID of zero, or all 8 waveforms are played.

7.6.6 Address: 0x05

図 7-20. 0x05

7	6	5	4	3	2	1	0
WAVFORM2[7:0]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-11. Address: 0x05

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7-0	WAVFORM2[7:0]	R/W	0	When the GO bit is asserted, the waveform processing engine will go to register address 0x03 and play the waveform ID that is indicated there. After completion of that waveform, the engine proceeds to register address 0x04 to play that waveform ID. If the ID value is zero, the playback process terminates. Otherwise this process repeats until it finds a waveform ID of zero, or all 8 waveforms are played.

7.6.7 Address: 0x06

図 7-21. 0x06

7	6	5	4	3	2	1	0
WAVFORM3[7:0]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-12. Address: 0x06

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7-0	WAVFORM3[7:0]	R/W	0	When the GO bit is asserted, the waveform processing engine will go to register address 0x03 and play the waveform ID that is indicated there. After completion of that waveform, the engine proceeds to register address 0x04 to play that waveform ID. If the ID value is zero, the playback process terminates. Otherwise this process repeats until it finds a waveform ID of zero, or all 8 waveforms are played.

7.6.8 Address: 0x07

図 7-22. 0x07

7	6	5	4	3	2	1	0
WAVFORM4[7:0]							

図 7-22. 0x07 (continued)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-13. Address: 0x07

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7-0	WAVFORM4[7:0]	R/W	0	When the GO bit is asserted, the waveform processing engine will go to register address 0x03 and play the waveform ID that is indicated there. After completion of that waveform, the engine proceeds to register address 0x04 to play that waveform ID. If the ID value is zero, the playback process terminates. Otherwise this process repeats until it finds a waveform ID of zero, or all 8 waveforms are played.

7.6.9 Address: 0x08

図 7-23. 0x08

7	6	5	4	3	2	1	0
WAVFORM5[7:0]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-14. Address: 0x08

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7-0	WAVFORM5[7:0]	R/W	0	When the GO bit is asserted, the waveform processing engine will go to register address 0x03 and play the waveform ID that is indicated there. After completion of that waveform, the engine proceeds to register address 0x04 to play that waveform ID. If the ID value is zero, the playback process terminates. Otherwise this process repeats until it finds a waveform ID of zero, or all 8 waveforms are played.

7.6.10 Address: 0x09

図 7-24. 0x09

7	6	5	4	3	2	1	0
WAVFORM6[7:0]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-15. Address: 0x09

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7-0	WAVFORM6[7:0]	R/W	0	When the GO bit is asserted, the waveform processing engine will go to register address 0x03 and play the waveform ID that is indicated there. After completion of that waveform, the engine proceeds to register address 0x04 to play that waveform ID. If the ID value is zero, the playback process terminates. Otherwise this process repeats until it finds a waveform ID of zero, or all 8 waveforms are played.

7.6.11 Address: 0x0A

図 7-25. 0x0A

7	6	5	4	3	2	1	0
WAVFORM7[7:0]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-16. Address: 0x0A

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7-0	WAVFORM7[7:0]	R/W	0	When the GO bit is asserted, the waveform processing engine will go to register address 0x03 and play the waveform ID that is indicated there. After completion of that waveform, the engine proceeds to register address 0x04 to play that waveform ID. If the ID value is zero, the playback process terminates. Otherwise this process repeats until it finds a waveform ID of zero, or all 8 waveforms are played.

7.6.12 Address: 0x0B

図 7-26. 0x0B

7	6	5	4	3	2	1	0
FIFO[7:0]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-17. Address: 0x0B

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7-0	FIFO[7:0]	R/W	0	Entry point for FIFO data. The user repeatedly writes this register with continuous haptic waveform data.

7.6.13 Address: 0xFF

図 7-27. 0xFF

7	6	5	4	3	2	1	0
PAGE[7:0]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-18. Address: 0xFF

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7-0	PAGE[7:0]	R/W	0	Page register for memory interface. Write this register with the memory page to be accessed.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

8.1 Application Information

The typical application for a haptic driver is in a touch-enabled system that already has an application processor that makes the decision on when to execute haptic effects.

The DRV2667 device is configured and can be used fully with I^2C communication to stream or launch haptic effects. Additionally, the system designer may decide to use the analog input to stream the desired haptic effects.

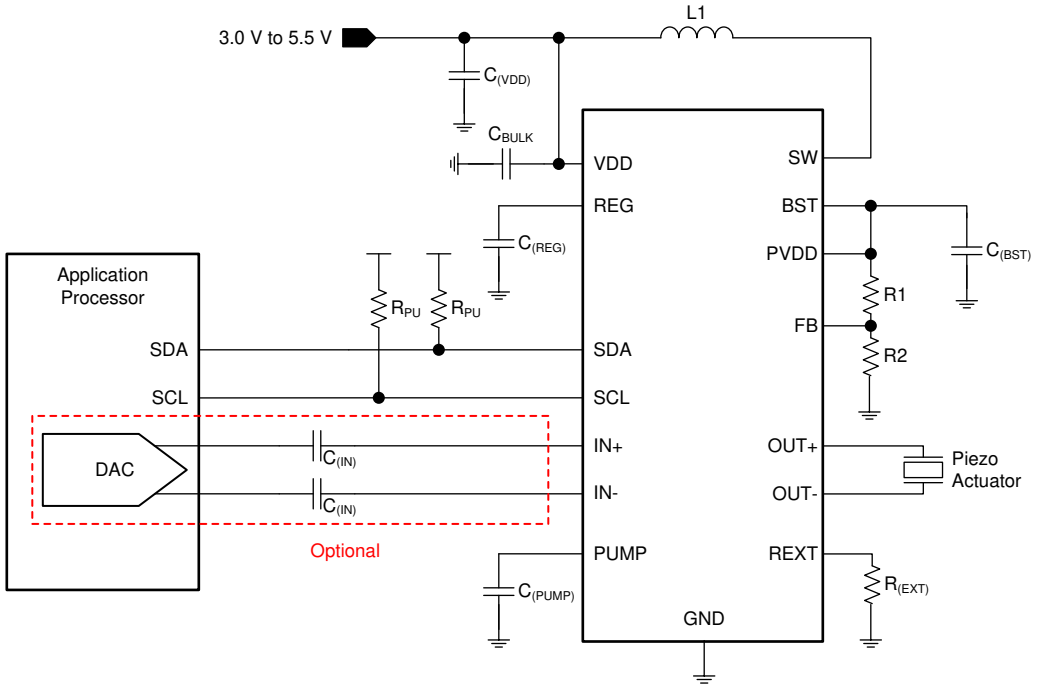


図 8-1. Typical Application Configuration

表 8-1. Recommended External Components

COMPONENT	DESCRIPTION	SPECIFICATION	TYPICAL VALUE
$C_{(VDD)}$	Input capacitor	Capacitance	1 µF
$C_{(REG)}$	Regulator capacitor	Capacitance	0.1 µF
$C_{(BST)}$	Boost capacitor	Capacitance	0.1 µF
C_{BULK}	Bulk capacitor	Capacitance	10 µF
$C_{(PUMP)}$	Internal charge pump capacitor	Capacitance	0.1 µF
$C_{(IN)}$	AC coupling capacitor (optional)	Capacitance	1 µF
R_1	Boost feedback resistor (see セクション 7.5.1)	Resistance	768 kΩ
R_2	Boost feedback resistor (see セクション 7.5.1)	Resistance	9.76 kΩ

表 8-1. Recommended External Components (continued)

COMPONENT	DESCRIPTION	SPECIFICATION	TYPICAL VALUE
R_2	Current limit resistor (see セクション 7.5.2)	Resistance	13 kΩ
$R_{(PU)}$	Pullup resistor	Resistance	2.2 kΩ
L_1	Boost inductor	Inductance	3.3 µH

8.2 Typical Application

A typical application of the DRV2667 device is in a system that has external buttons which fire different haptic effects when pressed. 図 8-2 shows a typical schematic of such a system. The buttons can be physical buttons, capacitive-touch buttons, or GPIO signals coming from the touch-screen system.

Effects in this type of system are programmable.

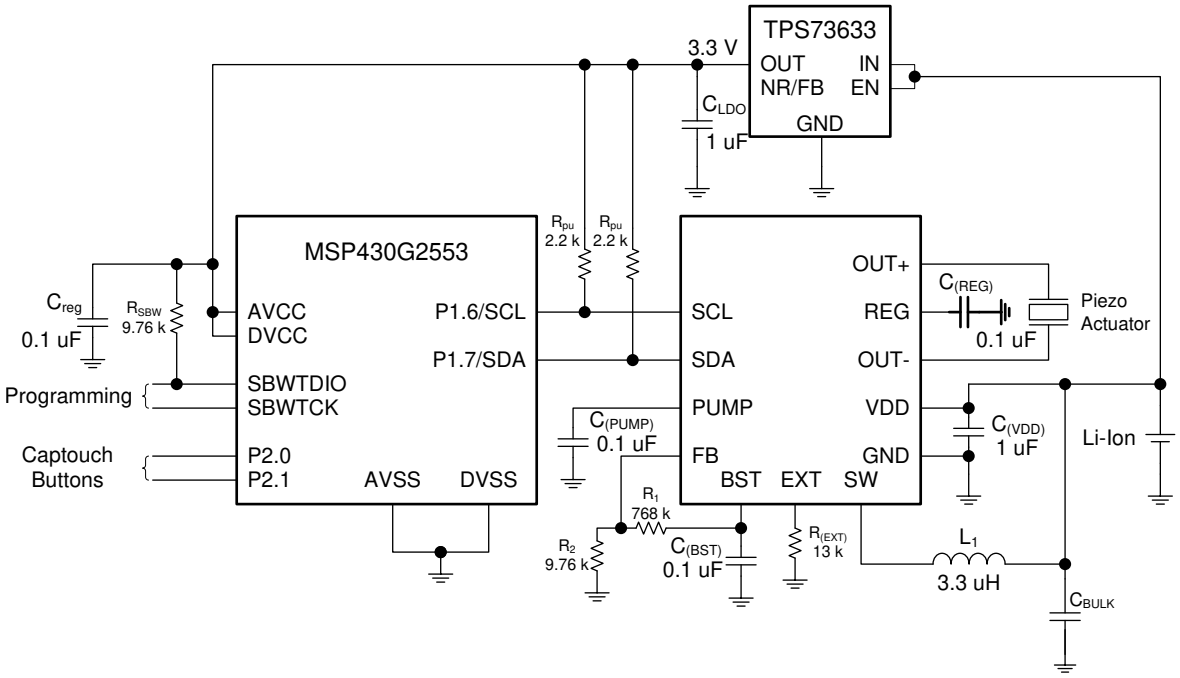


図 8-2. Example Application Schematic

8.2.1 Design Requirements

For this design example, use the values listed in 表 8-2 as the input parameters.

表 8-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Actuator type	120 V_{PP} 50 V_{PP}
Input power source	Li-ion / Li-polymer

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection

Inductor selection plays a critical role in the performance of the DRV2667 device. The range of recommended inductances is from 3.3 µH to 22 µH. In general, higher inductances within an inductor series of a given manufacturer have lower saturation current limits, and vice-versa. When a larger inductance is chosen, the device boost converter automatically runs at a lower switching frequency and incurs less switching losses; however, larger values of inductance may have higher equivalent series resistance (ESR), that increases the parasitic inductor losses. Because lower values of inductance generally have higher saturation currents, they are

a better choice when attempting to maximize the output current of the boost converter. Ensure that the saturation current of the inductor selected is higher than the programmed current limit for the device.

8.2.2.2 Piezo Actuator Selection

There are several key specifications to consider when choosing a piezo actuator for haptics, such as dimensions, blocking force, and displacement. However, the key electrical specifications from the driver perspective are voltage rating and capacitance.

At the maximum frequency of 500 Hz, the device is optimized to drive up to 50 nF at 200 V_{PP}, that is the highest voltage swing capability. It drives larger capacitances if the programmed boost voltage is lowered and/or the user limits the input frequency range to lower frequencies (e.g. 300 Hz).

8.2.2.3 Boost Capacitor Selection

The boost output voltage may be programmed as high as 105-V. A capacitor with a voltage rating of at least the boost output voltage must be selected. A 250-V rated 100-nF capacitor of the X5R or X7R type is recommended for the 105 V case because ceramic capacitors tend to come in ratings of 100 V or 250 V. The selected boost capacitor must have a minimum working capacitance of at least 50 nF. For boost voltages from 30 V to 80 V, a 100-V rated or 250-V rated, 100-nF capacitor is acceptable. For boost voltages less than 30 V, a 50-V, 0.22-µF capacitor is recommended.

8.2.2.4 Bulk Capacitor Selection

The use of a bulk capacitor placed next to the inductor is recommended due to the switch pin current requirements. A ceramic capacitors of the X5R or X7R type with capacitance of at least 1 µF is recommended.

8.2.3 Application Curves

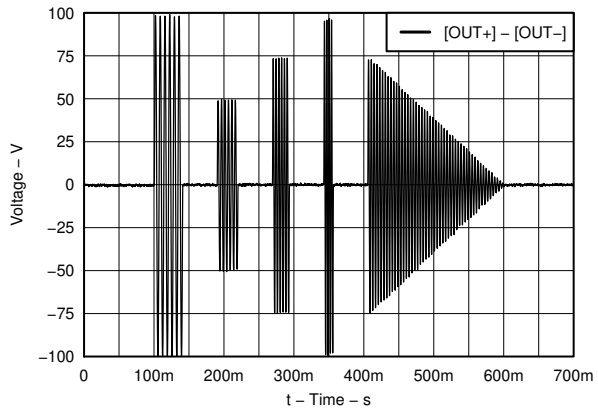


図 8-3. Example Waveform – Pinball Effect

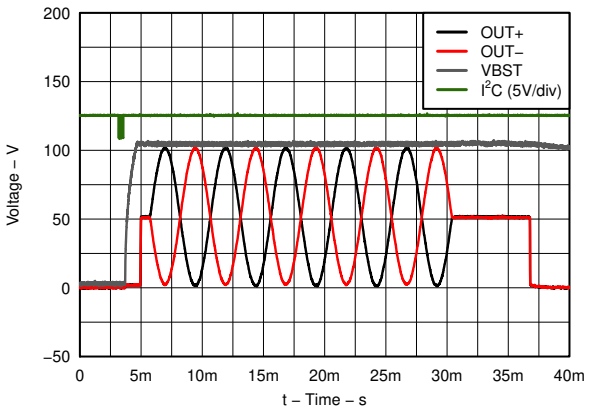


図 8-4. Typical Waveform

8.3 Initialization Setup

The DRV2667 device features a simple initialization procedure:

8.3.1 Initialization Procedure

1. Apply power to the DRV2667 device.
2. Wait for 1 ms for the DRV2667 device to power-up before attempting an I^2C write.
3. Exit low-power standby mode by clearing the STANDBY bit in register 0x02, bit 6.
4. Choose the interface mode as analog or digital in register 0x01, bit 2.
5. Select the gain setting for your application in register 0x01, bits [1:0].
6. Choose the desired timeout period if using the digital interface mode (FIFO), in register 0x02, bits[3:2].
7. If using the digital interface mode, the device is now ready to receive data. If using the analog input mode, set the EN_OVERRIDE bit in register 0x02, bit 1 to enable the boost and high-voltage amplifier and begin sourcing the waveform to the analog input.

8.3.2 Typical Usage Examples

8.3.2.1 Single Click or Alert Example

The following programming example shows how to initialize the device and send a simple Mode 3 (Waveform Synthesis Playback mode) transaction. If the number of cycles is short (< 10), the effect is a click, and if the number of cycles is long (> 10) the effect is a buzz alert.

I^2C ADDRESS	I^2C DATA	DESCRIPTION
Control		
0x02	0x00	Take device out of standby mode
0x01	0x00	Set to lowest gain, 50 V_{PP} maximum
0x03	0x01	Set sequencer to play waveform ID #1
0x04	0x00	End of sequence
Header		
0xFF	0x01	Set memory to page 1
0x00	0x05	Header size –1
0x01	0x80	Start address upper byte, also indicates Mode 3
0x02	0x06	Start address lower byte
0x03	0x00	Stop address upper byte
0x04	0x09	Stop address lower byte
0x05	0x01	Repeat count, play waveform once
Data		
0x06	0xFF	Amplitude for waveform ID #1, full-scale, 50 V_{PP} at gain = 0
0x07	0x19	Frequency for waveform ID #1, 195 Hz
0x08	0x05	Duration for waveform ID #1, play 5 cycles
0x09	0x00	Envelope for waveform ID #1, ramp up = no envelope, ramp down = no envelope
Control		
0xFF	0x00	Set page register to control space
0x02	0x01	Set GO bit (execute waveform sequence)

8.3.2.2 Library Storage Example

This example loads and plays the six effects shown in 図 6-15 through 図 6-20 into the waveform RAM. This is a simple example of how to put multiple waveforms in memory for subsequent low-latency recall. It is generally good practice to put the waveform header in page 1, and the waveform data in the following pages. When new waveforms are added later, the waveform data does not need to be shifted when this practice is used. Although this sequence seems long with the verbose descriptions, this example only takes 121 bytes of the waveform RAM, that is 6% of the available on-chip memory.

I²C ADDRESS	I²C DATA	DESCRIPTION
Control		
0x02	0x00	Take device out of standby mode
0x01	0x03	Set to highest gain, 200 V_{PP} maximum
0x03	0x02	Set sequencer to play waveform ID #2 (図 6-15)
0x04	0x01	Set sequencer to play waveform ID #1 (図 6-16)
0x05	0x03	Set sequencer to play waveform ID #3 (図 6-17)
0x06	0x04	Set sequencer to play waveform ID #4 (図 6-18)
0x07	0x05	Set sequencer to play waveform ID #5 (図 6-19)
0x08	0x06	Set sequencer to play waveform ID #6 (図 6-20)
0x09	0x00	End of sequence
Header		
0xFF	0x01	Set memory to page 1
0x00	0x1E	Header size –1
0x01	0x81	Start address upper byte #1, also indicates Mode 3
0x02	0x00	Start address lower byte #1
0x03	0x01	Stop address upper byte #1
0x04	0x03	Stop address lower byte #1
0x05	0x01	Repeat count, play waveform #1 once
0x06	0x81	Start address upper byte #2, also indicates Mode 3
0x07	0x04	Start address lower byte #2
0x08	0x01	Stop address upper byte #2
0x09	0x07	Stop address lower byte #2
0x0A	0x01	Repeat count, play waveform #2 once
0x0B	0x81	Start address upper byte #3, also indicates Mode 3
0x0C	0x08	Start address lower byte #3
0x0D	0x01	Stop address upper byte #3
0x0E	0x0B	Stop address lower byte #3
0x0F	0x01	Repeat count, play waveform #3 once
0x10	0x81	Start address upper byte #4, also indicates Mode 3
0x11	0x0C	Start address lower byte #4
0x12	0x01	Stop address upper byte #4
0x13	0x1B	Stop address lower byte #4
0x14	0x01	Repeat count, play waveform #4 once
0x15	0x81	Start address upper byte #5, also indicates Mode 3
0x16	0x1C	Start address lower byte #5
0x17	0x01	Stop address upper byte #5
0x18	0x37	Stop address lower byte #5
0x19	0x01	Repeat count, play waveform #5 once
0x1A	0x81	Start address upper byte #6, also indicates Mode 3

I²C ADDRESS	I²C DATA	DESCRIPTION
0x1B	0x38	Start address lower byte #6
0x1C	0x01	Stop address upper byte #6
0x1D	0x5B	Stop address lower byte #6
0x1E	0x01	Repeat count, play waveform #6 once
Data		
0xFF	0x02	Set memory to page 2
0x00	0xFF	Amplitude for waveform ID #1, full-scale, 200 V_{PP} at gain = 3
0x01	0x1A	Frequency for waveform ID #1, 203 Hz
0x02	0x0A	Duration for waveform ID #1, play 10 cycles
0x03	0x10	Envelope for waveform ID #1, ramp up = 32 ms, ramp down = no envelope
0x04	0xFF	Amplitude for waveform ID #2, full-scale, 200 V_{PP} at gain = 3
0x05	0x1A	Frequency for waveform ID #2, 203 Hz
0x06	0x03	Duration for waveform ID #2, play 3 cycles
0x07	0x01	Envelope for waveform ID #2, ramp up = no envelope, ramp down = 32 ms
0x08	0xFF	Amplitude for waveform ID #3, full-scale, 200 V_{PP} at gain = 3
0x09	0x1A	Frequency for waveform ID #3, 203 Hz
0x0A	0x0A	Duration for waveform ID #3, play 10 cycles
0x0B	0x12	Envelope for waveform ID #3, ramp up = 32 ms, ramp down = 64 ms
0x0C	0xFF	Amplitude for waveform ID #4, full-scale, 200 V_{PP} at gain = 3
0x0D	0x1A	Frequency for waveform ID #4, 203 Hz
0x0E	0x04	Duration for waveform ID #4, play 4 cycles
0x0F	0x00	Envelope for waveform ID #4, ramp up = no envelope, ramp down = no envelope
0x10	0xBF	Amplitude for waveform ID #4, 150 V_{PP} at gain = 3
0x11	0x1A	Frequency for waveform ID #4, 203 Hz
0x12	0x04	Duration for waveform ID #4, play 4 cycles
0x13	0x00	Envelope for waveform ID #4, ramp up = no envelope, ramp down = no envelope
0x14	0x80	Amplitude for waveform ID #4,100 V_{PP} at gain = 3
0x15	0x1A	Frequency for waveform ID #4, 203 Hz
0x16	0x04	Duration for waveform ID #4, play 4 cycles
0x17	0x00	Envelope for waveform ID #4, ramp up = no envelope, ramp down = no envelope
0x18	0x40	Amplitude for waveform ID #4, full-scale, 50 V_{PP} at gain = 3
0x19	0x1A	Frequency for waveform ID #4, 203 Hz
0x1A	0x04	Duration for waveform ID #4, play 4 cycles
0x1B	0x00	Envelope for waveform ID #4, ramp up = no envelope, ramp down = no envelope
0x1C	0xFF	Amplitude for waveform ID #5, full-scale, 200 V_{PP} at gain = 3
0x1D	0x0D	Frequency for waveform ID #5, 102 Hz
0x1E	0x02	Duration for waveform ID #5, play 2 cycles
0x1F	0x00	Envelope for waveform ID #5, ramp up = no envelope, ramp down = no envelope
0x20	0x00	Amplitude for waveform ID #5, 0 V for delay
0x21	0x26	Frequency for waveform ID #5, 297 Hz
0x22	0x01	Duration for waveform ID #5, play 1 cycle (3.4 ms delay)
0x23	0x00	Envelope for waveform ID #5, ramp up = no envelope, ramp down = no envelope
0x24	0xFF	Amplitude for waveform ID #5, full-scale, 200 V_{PP} at gain = 3
0x25	0x13	Frequency for waveform ID #5, 148 Hz
0x26	0x02	Duration for waveform ID #5, play 2 cycles
0x27	0x00	Envelope for waveform ID #5, ramp up = no envelope, ramp down = no envelope

I²C ADDRESS	I²C DATA	DESCRIPTION
0x28	0x00	Amplitude for waveform ID #5, 0 V for delay
0x29	0x26	Frequency for waveform ID #5, 297 Hz
0x2A	0x01	Duration for waveform ID #5, play 1 cycle (3.4 ms delay)
0x2B	0x00	Envelope for waveform ID #5, ramp up = no envelope, ramp down = no envelope
0x2C	0xFF	Amplitude for waveform ID #5, full-scale, 200 V_{PP} at gain = 3
0x2D	0x1A	Frequency for waveform ID #5, 203 Hz
0x2E	0x02	Duration for waveform ID #5, play 2 cycles
0x2F	0x00	Envelope for waveform ID #5, ramp up = no envelope, ramp down = no envelope
0x30	0x00	Amplitude for waveform ID #5, 0 V for delay
0x31	0x26	Frequency for waveform ID #5, 297 Hz
0x32	0x01	Duration for waveform ID #5, play 1 cycle (3.4 ms delay)
0x33	0x00	Envelope for waveform ID #5, ramp up = no envelope, ramp down = no envelope
0x34	0xFF	Amplitude for waveform ID #5, full-scale, 200 V_{PP} at gain = 3
0x35	0x26	Frequency for waveform ID #5, 297 Hz
0x36	0x02	Duration for waveform ID #5, play 2 cycles
0x37	0x00	Envelope for waveform ID #5, ramp up = no envelope, ramp down = no envelope
0x38	0xFF	Amplitude for waveform ID #6, full-scale, 200 V_{PP} at gain = 3
0x39	0x13	Frequency for waveform ID #6, 148 Hz
0x3A	0x06	Duration for waveform ID #6, play 6 cycles
0x3B	0x00	Envelope for waveform ID #6, ramp up = no envelope, ramp down = no envelope
0x3C	0x00	Amplitude for waveform ID #6, 0 V for delay
0x3D	0x0D	Frequency for waveform ID #6, 102 Hz
0x3E	0x05	Duration for waveform ID #6, play 5 cycles (50 ms delay)
0x3F	0x00	Envelope for waveform ID #6, ramp up = no envelope, ramp down = no envelope
0x40	0x80	Amplitude for waveform ID #6, 100 V_{PP} at gain = 3
0x41	0x1A	Frequency for waveform ID #6, 203 Hz
0x42	0x06	Duration for waveform ID #6, play 6 cycles
0x43	0x00	Envelope for waveform ID #6, ramp up = no envelope, ramp down = no envelope
0x44	0x00	Amplitude for waveform ID #6, 0 V for delay
0x45	0x0D	Frequency for waveform ID #6, 102 Hz
0x46	0x05	Duration for waveform ID #6, play 5 cycles (50 ms delay)
0x47	0x00	Envelope for waveform ID #6, ramp up = no envelope, ramp down = no envelope
0x48	0xBF	Amplitude for waveform ID #6, 150 V_{PP} at gain = 3
0x49	0x20	Frequency for waveform ID #6, 250 Hz
0x4A	0x06	Duration for waveform ID #6, play 6 cycles
0x4B	0x00	Envelope for waveform ID #6, ramp up = no envelope, ramp down = no envelope
0x4C	0x00	Amplitude for waveform ID #6, 0 V for delay
0x4D	0x0D	Frequency for waveform ID #6, 102 Hz
0x4E	0x05	Duration for waveform ID #6, play 5 cycles (50 ms delay)
0x4F	0x00	Envelope for waveform ID #6, ramp up = no envelope, ramp down = no envelope
0x50	0xFF	Amplitude for waveform ID #6, full-scale, 200 V_{PP} at gain = 3
0x51	0x26	Frequency for waveform ID #6, 297 Hz
0x52	0x04	Duration for waveform ID #6, play 4 cycles
0x53	0x00	Envelope for waveform ID #6, ramp up = no envelope, ramp down = no envelope
0x54	0x00	Amplitude for waveform ID #6, 0 V for delay
0x55	0x0D	Frequency for waveform ID #6, 102 Hz

I²C ADDRESS	I²C DATA	DESCRIPTION
0x56	0x05	Duration for waveform ID #6, play 5 cycles (50 ms delay)
0x57	0x00	Envelope for waveform ID #6, ramp up = no envelope, ramp down = no envelope
0x58	0xBF	Amplitude for waveform ID #6,150 V_{PP} at gain = 3
0x59	0x20	Frequency for waveform ID #6, 250 Hz
0x5A	0x01	Duration for waveform ID #6, play 1 cycle
0x5B	0x08	Envelope for waveform ID #6, ramp up = no envelope, ramp down = 256 ms

I²C ADDRESS	I²C DATA	DESCRIPTION
Control		
0xFF	0x00	Set page register to control space
0x02	0x01	Set GO bit (execute waveform sequence)

9 Power Supply Recommendations

The DRV2667 device is designed to operate from an input-voltage supply range between 3 V and 5.5 V. The decoupling capacitor for the power supply must be placed as close to the device pin as possible.

10 Layout

10.1 Layout Guidelines

Use the following guidelines for the DRV2667 device layout:

- The decoupling capacitor for the power supply (V_{DD}) must be placed close to the device pin.
- The filtering capacitor for the regulator (REG) must be placed close to the device pin.
- The boost inductor must be placed as close as possible to the SW pin.
- The bulk capacitor for the boost must be placed as close as possible to the inductor.
- The charge pump capacitor (PUMP) must be placed close to the device pin.

Use of the thermal footprint outlined by this datasheet is recommended to achieve optimum device performance. See land pattern diagram for exact dimensions.

The DRV2667 device power pad must be soldered directly to the thermal pad on the printed circuit board. The printed circuit board thermal pad must be connected to the ground net and thermal vias to any existing backside/ internal copper ground planes. Connection to a ground plane on the top layer near the corners of the device is also recommended. Another key layout consideration is to keep the boost programming resistors (R1 and R2) as close as possible to the FB pin of the device. Care must be taken to avoid getting the FB trace near the SW trace.

10.2 Layout Example

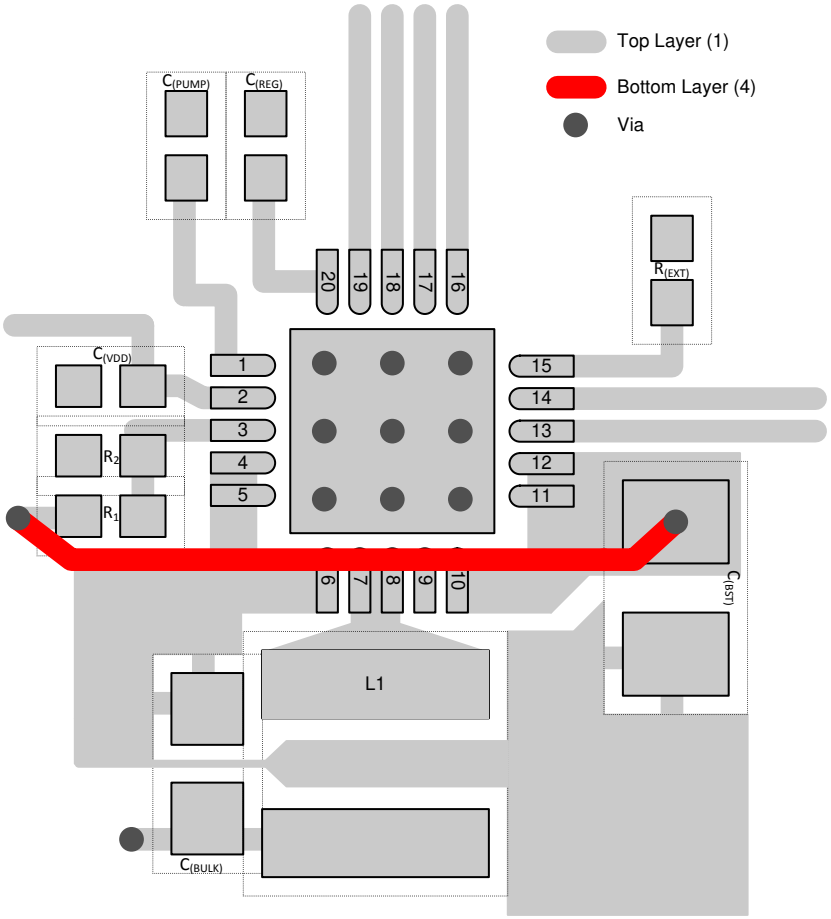


図 10-1. Layout Example with a 4-Layer Board

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

11.3 Trademarks

すべての商標は、それぞれの所有者に帰属します。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV2667RGPR	Active	Production	QFN (RGP) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	2667
DRV2667RGPR.A	Active	Production	QFN (RGP) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	2667
DRV2667RGPR.B	Active	Production	QFN (RGP) | 20	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
DRV2667RGPRG4	Active	Production	QFN (RGP) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	2667
DRV2667RGPRG4.A	Active	Production	QFN (RGP) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	2667
DRV2667RGPRG4.B	Active	Production	QFN (RGP) | 20	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
DRV2667RGPT	Active	Production	QFN (RGP) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	2667
DRV2667RGPT.A	Active	Production	QFN (RGP) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	2667
DRV2667RGPT.B	Active	Production	QFN (RGP) | 20	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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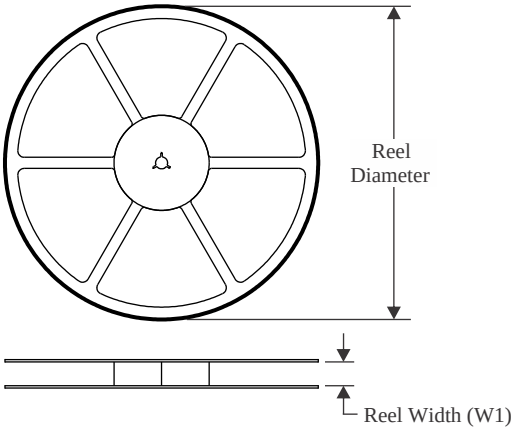
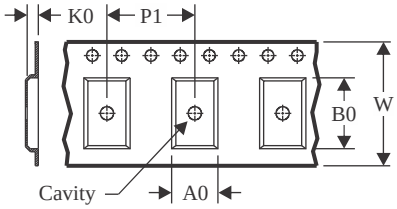
TAPE AND REEL INFORMATION

REEL DIMENSIONS

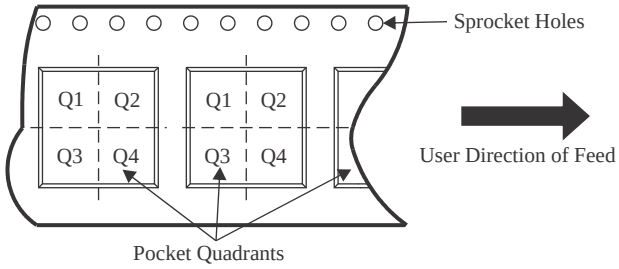


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

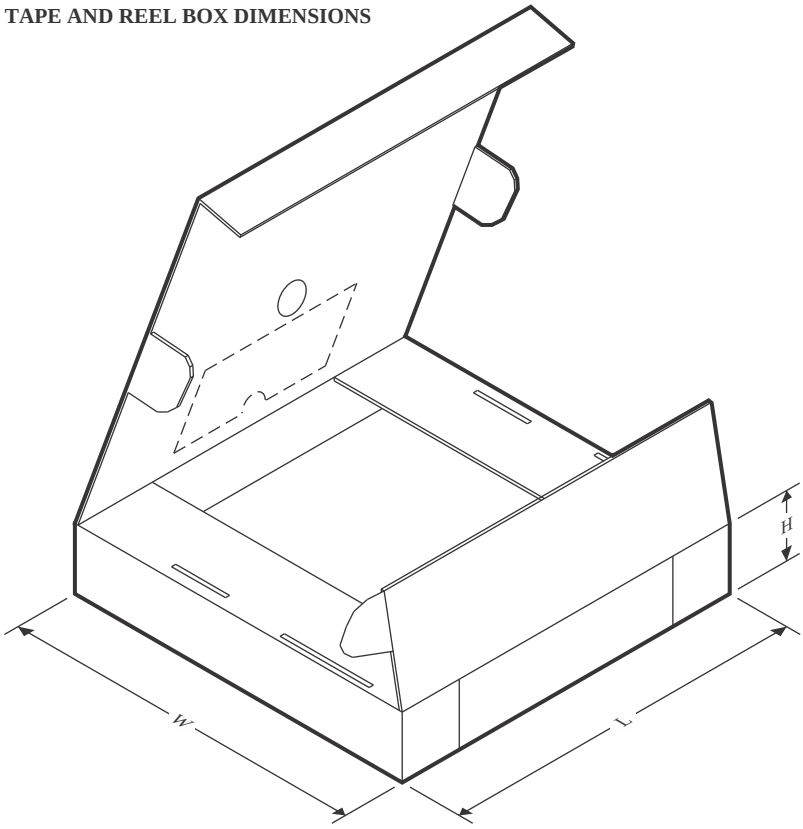
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV2667RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV2667RGPRG4	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV2667RGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV2667RGPR	QFN	RGP	20	3000	346.0	346.0	33.0
DRV2667RGPRG4	QFN	RGP	20	3000	346.0	346.0	33.0
DRV2667RGPT	QFN	RGP	20	250	210.0	185.0	35.0

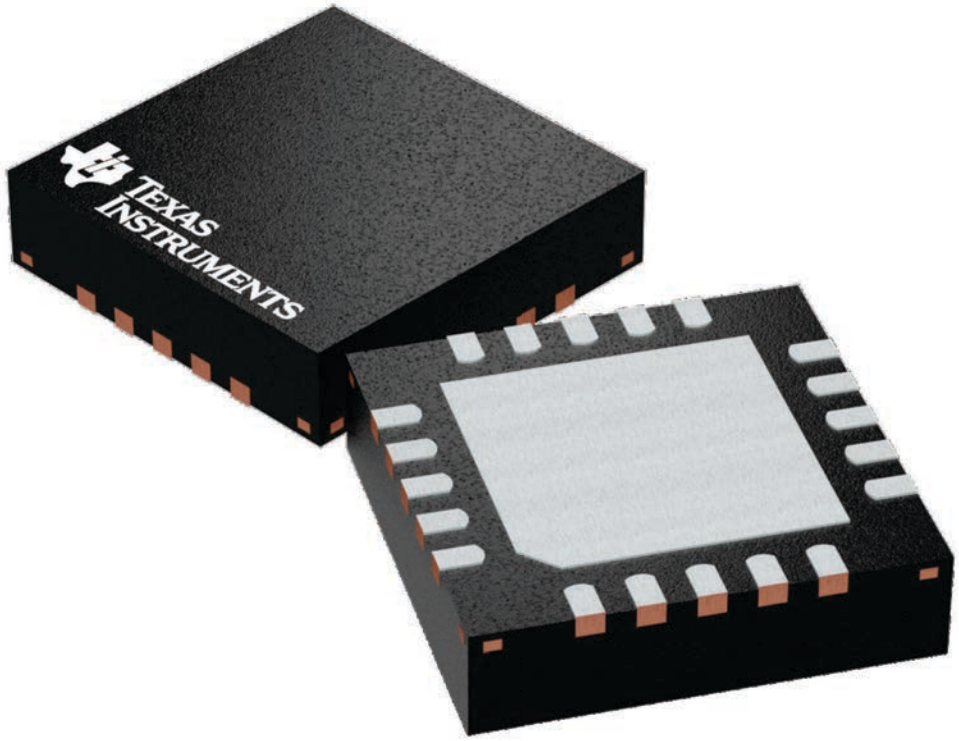
GENERIC PACKAGE VIEW

RGP 20

VQFN - 1 mm max height

4 x 4, 0.5 mm pitch

VERY THIN QUAD FLATPACK



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

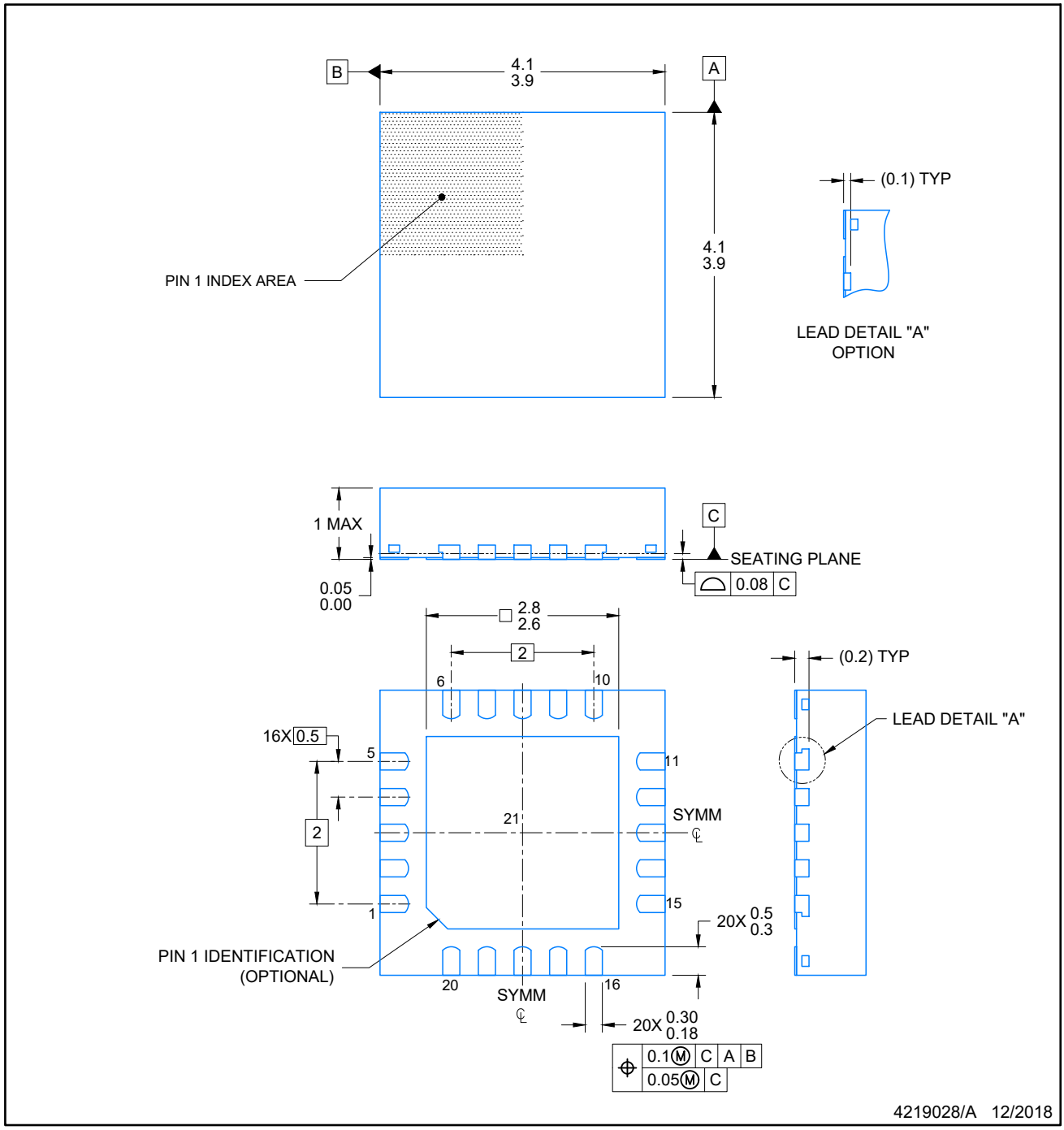
4224735/A

PACKAGE OUTLINE

RGP0020D

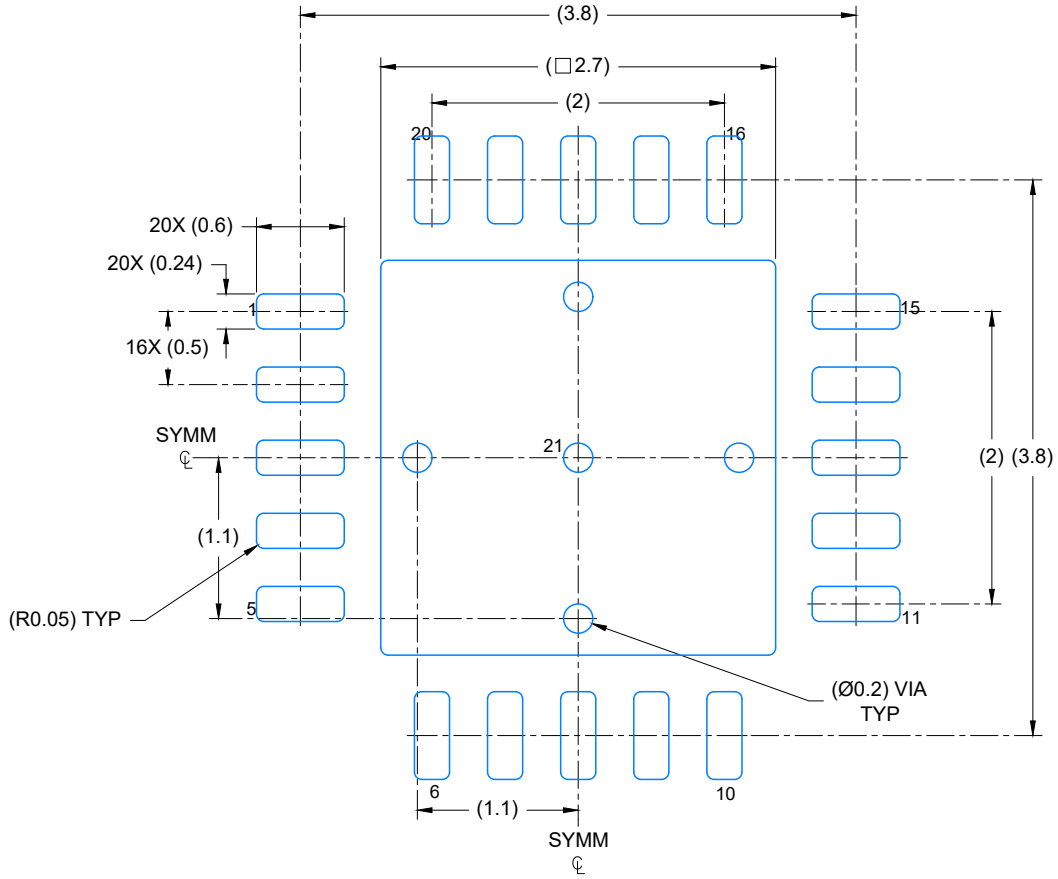
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

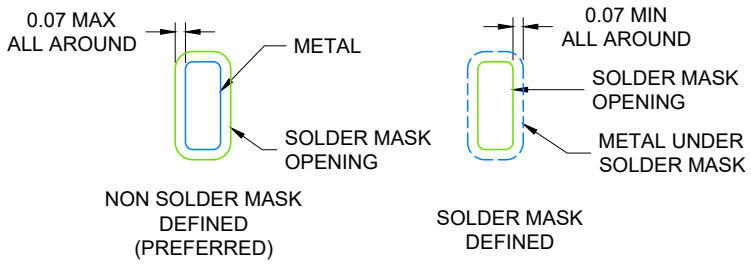


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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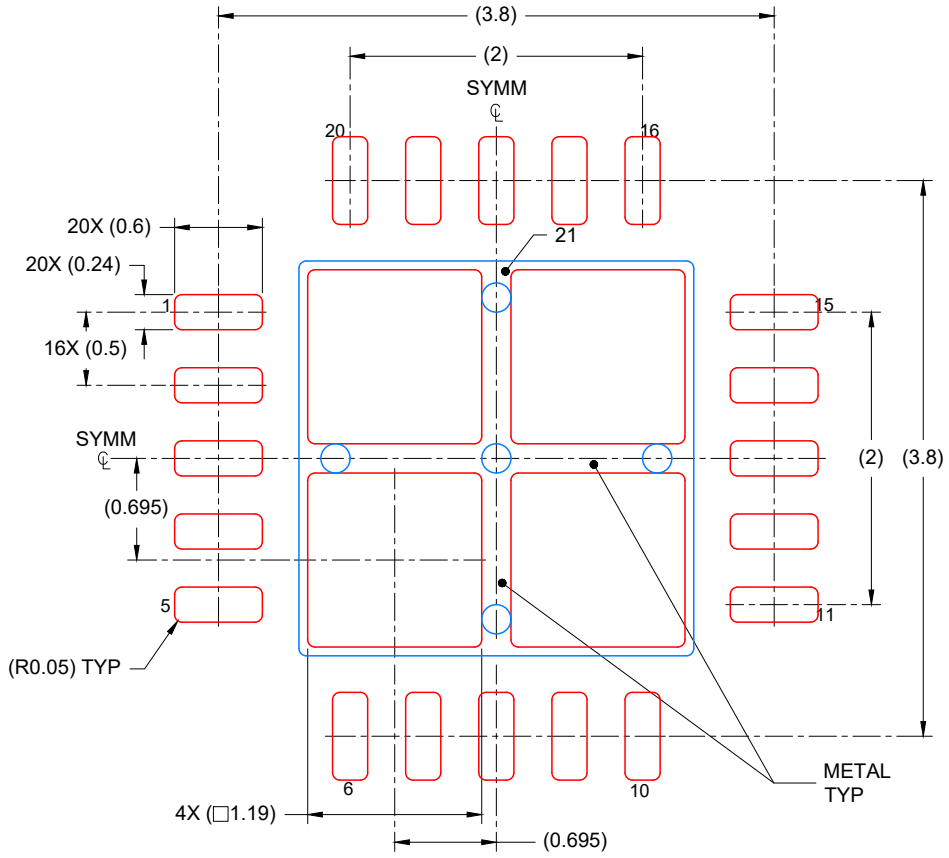
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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