TEXAS INSTRUMENTS

DRV2510-Q1
JAJSCC7D – JUNE 2016 – REVISED NOVEMBER 2023

DRV2510-Q1 3A 車載用、ソレノイドおよび音声コイル用ハプティック ドライバ、診断機能内蔵

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:-40℃〜125℃、T_A
- 広い動作電圧範囲 (4.5V〜18V)
- 負荷ダンプ保護を内蔵 (40V)
- 高い電流ドライブ (3A ピーク)
- 低い $R_{DS(on)}$、完全な H ブリッジ出力
- 診断機能内蔵
- フォルト保護機能内蔵
  - ISO-7637-2 準拠の 40V 負荷ダンプ保護
  - 短絡保護
  - 過熱保護機能
  - 過電圧および低電圧保護
  - 障害通知
- アナログ入力
- I²C 通信
- 専用の割り込みピン
- ISO9000: 2002 TS16949 認定済み

2 アプリケーション

- 電磁気アクチュエータドライバ
  - 音声コイル
  - ソレノイド
- 機械式ボタンの置き換え
- 車載用ハプティック アプリケーション
  - インフォテインメント
  - 中央コンソール
  - ステアリング ホイール
  - ドア パネル
  - シート

3 概要

DRV2510-Q1 デバイスは、大電流のハプティック ドライバで、ソレノイドや音声コイルなど誘導性の負荷に特化して設計されています。

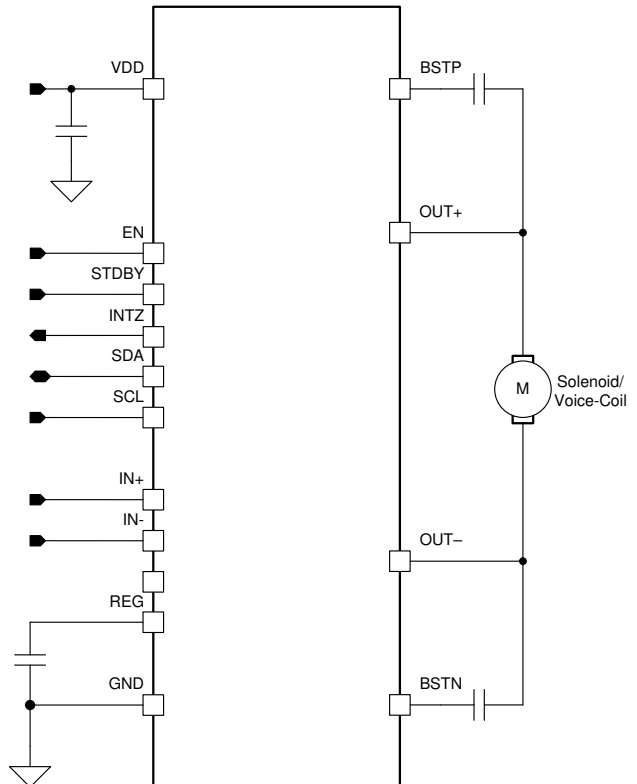出力段は、完全な H ブリッジで構成され、3A のピーク電流を供給できます。

DRV2510-Q1 デバイスは、低電圧誤動作防止、過電流保護、過熱保護などの保護機能を備えています。

DRV2510-Q1 デバイスは車載用に認定済みです。負荷ダンプ保護が搭載されているため、外付け電圧クランプのコストとサイズを減らすことができ、オンボードの負荷診断機能によりデジタル インターフェイス経由でアクチュエータの状態が報告されます。

製品情報

部品番号	パッケージ [(1)]	本体サイズ (公称)
DRV2510-Q1	HTSSOP (16)	5.00 mm x 4.40 mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

概略回路図

English Data Sheet: SLOS919

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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• ドキュメント全体にわたって表、図、相互参照の採番方法を更新...1	

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• 車載用の「特長」を「特長」リストの先頭に移動 1	
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• Changed the *ESD Ratings* table...5	
• Added INTZ Report to the *Electrical Characteristics* table..6	
• Changed 図 7-1 10	
• Changed From: "The load diagnostic function runs on de-assertion" To: "The load diagnostic function runs on assertion" in the *Load Diagnostics* section..11	
• Added the *Protection and Monitoring* section...12	
• Changed From: "NRST pin..." To: "EN pin..." in the *Operation in Shutdown Mode* section..............13	
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• Deleted register 0x00 from the *Register Map* section..17	
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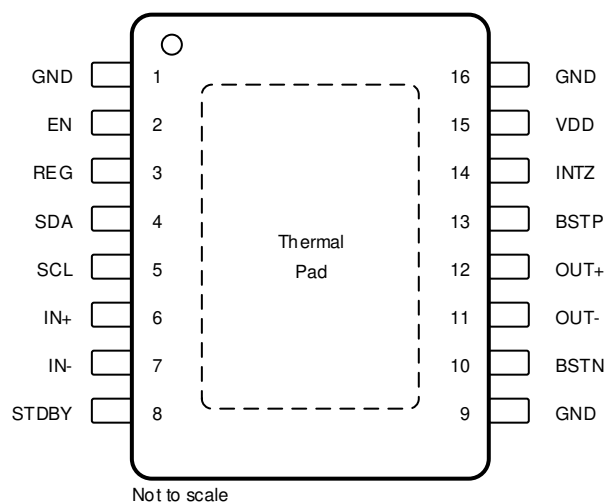
図 5-1. TWP Package HTSSOP 16-Pin With Thermal Pad Top View

表 5-1. Pin Functions

PIN NAME	PIN NO.	TYPE	DESCRIPTION
GND	1, 9, 16	P	Ground.
EN	2	I	Device enable pin.
REG	3	P	Internally generated gate voltage supply. Not to be used as a supply or connected to any component other than a 1 µF X7R ceramic decoupling capacitor and the MODE resistor divider.
SDA	4	I	I2C data.
SCL	5	I	I2C clock.
IN+	6	I	Positive differential input.
IN-	7	I	Negative differential input.
STDBY	8	I	Standby pin.
BSTN	10	P	Boot strap for negative output, connect to 220 nF X5R, or better ceramic cap to OUT-.
OUT-	11	O	Negative output.
OUT+	12	O	Positive output.
BSTP	13	P	Boot strap for positive output, connect to 220 nF X5R, or better ceramic cap to OUT+.
INTZ	14	O	General fault reporting. Open drain. INTZ = High, normal operation INTZ = Low, fault condition
VDD	15	P	Power supply.
Thermal Pad		G	Connect to GND for best system performance. If not connected to GND, leave floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage	VDD DC supply voltage range	−0.3	30	V
	VDD pulsed supply voltage range. t < 400 ms exposure	−1	40	
	VDD supply voltage ramp rate		15	V/ms
Input voltage, V_I	SCL, SDA, EN	−0.3	5	V
	IN+, IN-, STDBY	−0.3	6.5	
Current	DC current on VDD, GND, OUT+, OUT-	−4	4	A
	Maximum current in all input pins	−1	1	mA
	Maximum sink current for open-drain pins		7	
Operating free-air temperature, T_A		−40	125	°C
Junction temperature, T_J		−40	150	
Storage temperature range, T_{stg}		−55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1] HBM ESD Classification Level H2	±3500	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage. VDD.	4.5		18	V
V_{IH}	High-level input voltage. SDA, SCL, STDBY, EN.	2.1			V
V_{IL}	Low-level input voltage. SDA, SCL, STDBY, EN.			0.7	V
V_{OL}	Low-level output voltage			0.4	V
V_{OH}	High-level output voltage	2.4			V
I_{IH}	High-level input current. SDA, SCL, STDBY, EN.			50	µA
R_L	Minimum load Impedance		1.5		Ω
C_B	Load capacitance for each bus line (SDA/SCL)			400	pF

6.4 Thermal Information

THERMAL METRIC[1]	DRV2510-Q1 PWP (HTSSOP) {16} PINS	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	39.4	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	24.9	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	20	°C/W
ψ_{JT} Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB} Junction-to-board characterization parameter	19.8	°C/W

THERMAL METRIC[1]		DRV2510-Q1	UNIT
		PWP (HTSSOP)	
		{16} PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = 25°C, AVCC = VDD = 12 V, R_L = 5 Ω (unless otherwise noted)

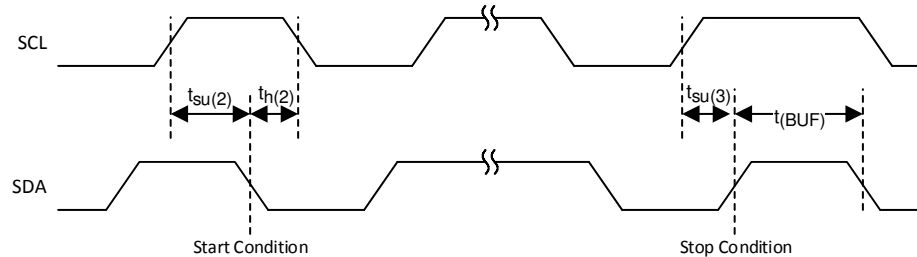|	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$|V_{OS}|$	Output offset voltage (measured differentially)	V_I = 0 V, Gain = 20 dB	–25		25	mV
I_{VDD}	Quiescent supply current	No load or filter		16		mA
$I_{VDD(SD)}$	Quiescent supply current in shutdown mode	No load or filter		5	20	µA
$I_{VDD(STDBY)}$	Quiescent supply current in standby mode	No load or filter		7		mA
$r_{DS(on)}$	Drain-source on-state resistance, measured pin to pin	T_J = 25°C		180		mΩ
G	Gain	$P_{(o)}$ = 1 W	19	20	21	dB
			25	26	27	
			31	32	33	dB
			35	36	37	
V_{REG}	Regulator voltage		6.4	6.9	7.4	V
V_O	Output voltage (measured differentially)			20		V
PSRR	Power supply ripple rejection	VDD = 12 V + 1 Vrms at 1 kHz		75		dB
V_{ICMIN}	Input common-mode min			0.3		V
V_{ICMAX}	Input common-mode max			4.4		
CMRR	Common-mode rejection ratio	f = 1 kHz, 100 mVrms referenced to GND. Gain = 20 dB		63		dB
f_{OSC}	Oscillator frequency (with PWM duty cycle < 96%)			400		kHz
				500		
	Output resistance in shutdown			10		MΩ
	Resistance to detect a short from OUT pin(s) to VDD or GND				200	Ω
	Open-circuit detection threshold		75	95	120	Ω
	Short-circuit detection threshold		0.9	1.2	1.5	Ω
	Power-on threshold			4.1		V
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C
	Over-current trip point			3.5		A
	Over-voltage trip point			21		V
	Over-voltage hysteresis			0.6		V
	Under-voltage trip point			4		V
	Under-voltage hysteresis			0.25		V
INTZ Report						
	INTZ pin output voltage for logic-level high (open-drain logic output)	External 47-kΩ pullup resistor to 3.3 V	2.4			V
	INTZ pin output voltage for logic-level low (open-drain logic output)	External 47-kΩ pullup resistor to 3.3 V			0.5	V

Product Folder Links: *DRV2510-Q1*

English Data Sheet: SLOS919

6.6 Timing Requirements

T_A = 25 °C, V_{DD} = 3.6 V (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$f_{(SCL)}$	Frequency at the SCL pin with no wait states			400	kHz
$t_{w(H)}$	Pulse duration, SCL high	0.6			µs
$t_{w(L)}$	Pulse duration, SCL low	1.3			µs
$t_{su(1)}$	Setup time, SDA to SCL	100			ns
$t_{h(1)}$	Hold time, SCL to SDA	300			ns
$t_{(BUF)}$	Bus free time between stop and start condition	1.3			µs
$t_{su(2)}$	Setup time, SCL to start condition	0.6			µs
$t_{h(2)}$	Hold time, start condition to SCL	0.6			µs
$t_{su(3)}$	Setup time, SCL to stop condition	0.6			µs
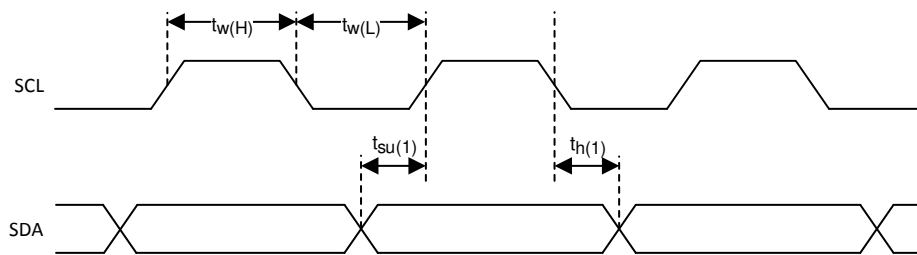
図 **6-1. SCL and SDA Timing**

図 **6-2. Timing for Start and Stop Conditions**

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{on-sd}	Turn-on time from shutdown to waveform	EN = Low to High, STBY = Low		229			ms
t_{OFF-sd}	Turn-off time	EN = High to Low		47		µs	
$t_{on-stdby}$	Turn-on time from standby to waveform	EN = High, STBY = High to Low		32		µs	

6.8 Typical Characteristics
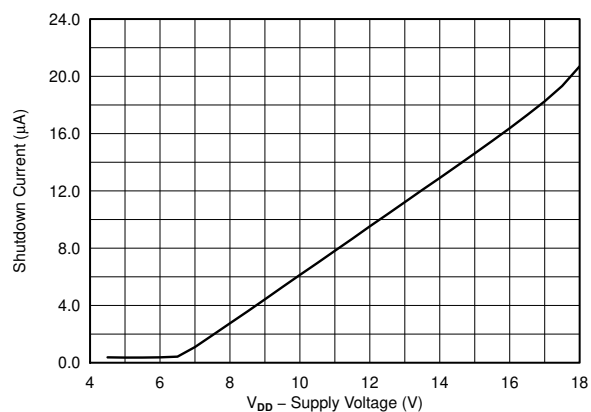
図 6-3. Shutdown Current vs VDD Voltage
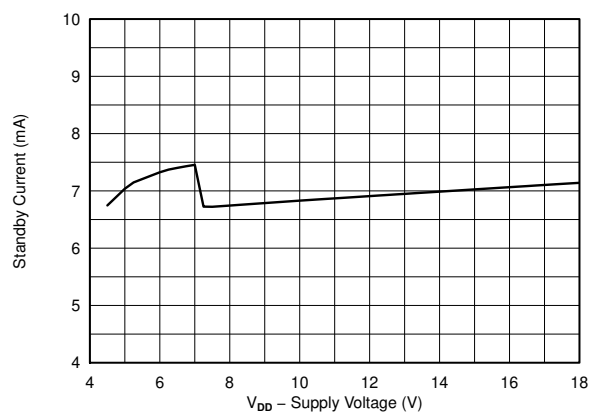
図 6-4. Standby Current vs VDD Voltage

資料に関するフィードバック (ご意見やお問い合わせ) を送信

Product Folder Links: *DRV2510-Q1*

English Data Sheet: SLOS919

7 Detailed Description

## 7.1 Overview

The DRV2510-Q1 device is a high current haptic driver specifically designed for inductive loads, such as solenoids and voice coils.

The output stage consists of a full H-bridge capable of delivering 3 A of peak current.

The design uses an ultra-efficient switching output technology developed by Texas Instruments, but with features added for the automotive industry. The DRV2510-Q1 device provides protection functions such as undervoltage lockout, over-current protection and over-temperature protection. This technology allows for reduced power consumption, reduced heat, and reduced peak currents in the electrical system.

The DRV2510-Q1 device is automotive qualified. The integrated load-dump protection reduces external voltage clamp cost and size, and the onboard load diagnostics report the status of the actuator through the digital interface.

7.2 Functional Block Diagram
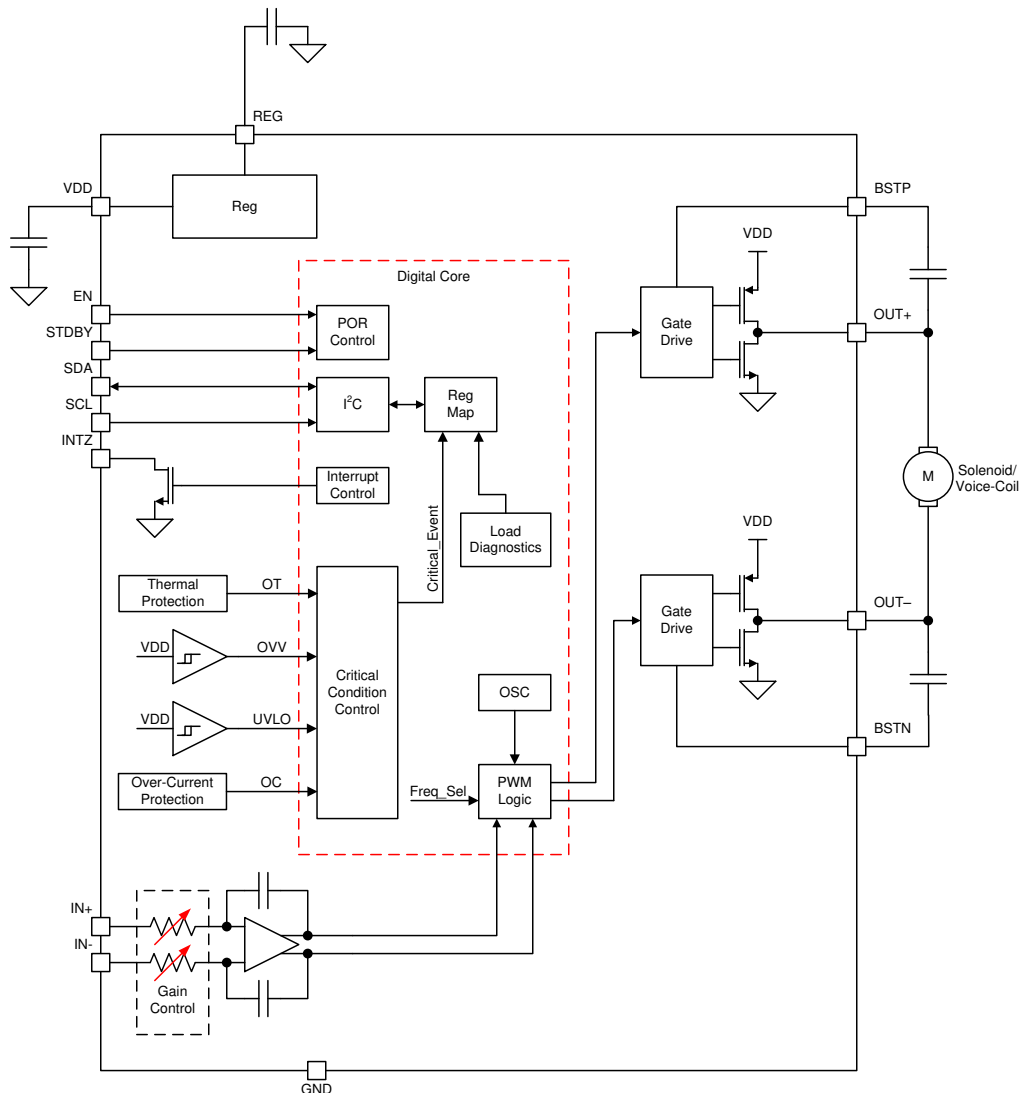
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7.3 Feature Description

7.3.1 Analog Input and Configurable Pre-amplifier

The DRV2510-Q1 device features a differential input stage that cancels common-mode noise that appears on the inputs. The DRV2510-Q1 device also features four gain settings that are configurable via I^{2}C. Please see the Programming Sections for register locations.

表 7-1. Gain Configuration Table

GAIN	INPUT IMPEDANCE
20 dB	60 kΩ
26 dB	30 kΩ
32 dB	15 kΩ
36 dB	9 kΩ

7.3.2 Pulse-Width Modulator (PWM)

The DRV2510-Q1 device features BD modulation scheme with high bandwidth, low noise, low distortion, and excellent stability.

The BD modulation scheme allows for smaller ripple currents through the load. Each output switches from 0 V to the supply voltage. With no input, the OUT+ and OUT- pins are in phase with each other so that there is little or no current in the load. For positive differential inputs, the duty cycle of OUT+ is greater than 50% and the duty cycle of OUT- is lower than 50% for a positive differential output voltage. The opposite is true for negative differential inputs. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces the I^{2}R losses in the load.
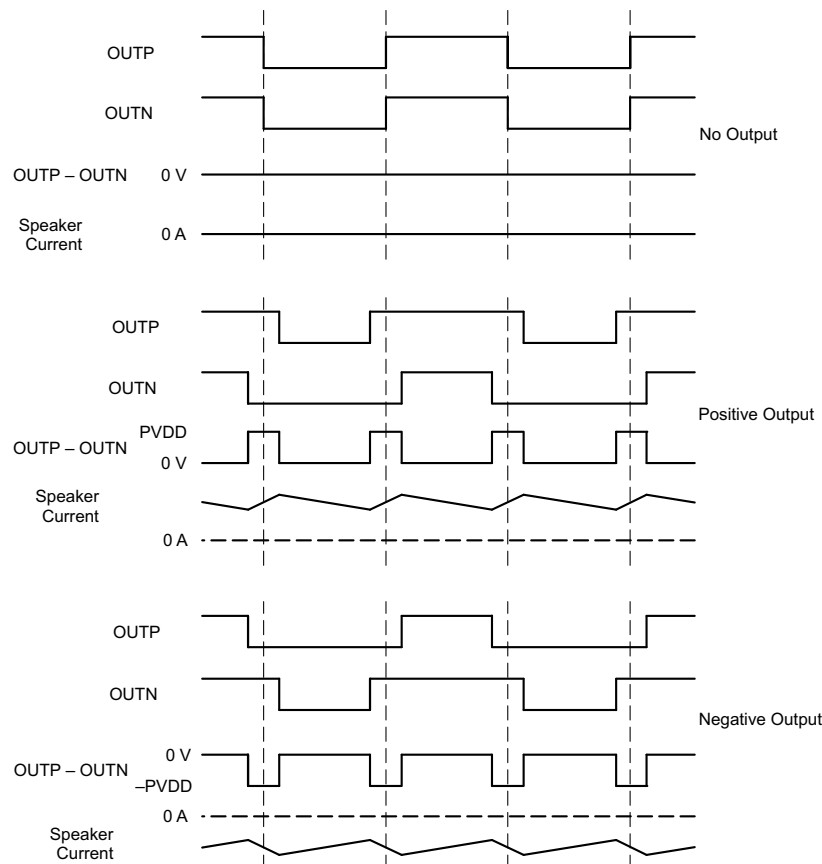
図 7-1. BD Mode Modulation

7.3.3 Designed for low EMI

The DRV2510-Q1 device design has minimal parasitic inductances due to the short leads on the package. This dramatically reduces EMI that results from current passing from the die to the system PCB. The design incorporates circuitry that optimizes output transitions that causes EMI. Follow the recommended design requirements in the *セクション 8.2.1.1* section.

7.3.4 Device Protection Systems

The DRV2510-Q1 device features a complete set of protection circuits carefully designed to protect the device against permanent failures due to shorts, over-temperature, over-voltage, and under-voltage scenarios. The INTZ pin signals if an error is detected.

Additionally, the DRV2510-Q1 device is not damaged by adjacent pin to pin shorts.

表 7-2. Fault Reporting Table

FAULT	TRIGGERING CONDITION	INTZ	ACTION
Over-current	Output short or short to VDD or GND	pulled low	output in high impedance. I^2 updated.
Over-temperature	T_j > 150 °C	pulled low	output in high impedance. Recovery is automatic once the temperature returns to a safe level.
Under-voltage	VDD < 4 V	pulled low	output in high impedance. I^2 reset.
Over-voltage	VDD > 21 V	pulled low	output in high impedance. I^2 updated.

7.3.4.1 Diagnostics

The device incorporates load diagnostic circuitry designed for detecting and determining the status of output connections. The device supports the following diagnostics:

- Short to GND
- Short to VDD
- Short across load
- Open load

The device reports the presence of any of the short or open conditions to the system via I^2C register read.

7.3.4.1.1 Load Diagnostics

The load diagnostic function runs on assertion of EN or when the device is in a fault state (dc detect, overcurrent, overvoltage, undervoltage, and overtemperature). During this test, the outputs are in a Hi-Z state. The device determines whether the output is a short to GND, short to VDD, open load, or shorted load. The load diagnostic biases the output, which therefore requires limiting the capacitance value for proper functioning. The load diagnostic test takes approximately 229 ms to run. Note that the *check* phase repeats up to five times if a fault is present or a large capacitor to GND is present on the output. On detection of an open load, the output still operates. On detection of any other fault condition, the output goes into a Hi-Z state, and the device checks the load continuously until removal of the fault condition. After detection of a normal output condition, the output starts. The load diagnostics run after every other overvoltage (OV) event. The load diagnostic for open load only has I^2C reporting. All other faults have I^2C and INTZ pin assertion.

The device performs load diagnostic tests as shown in 図 7-2.
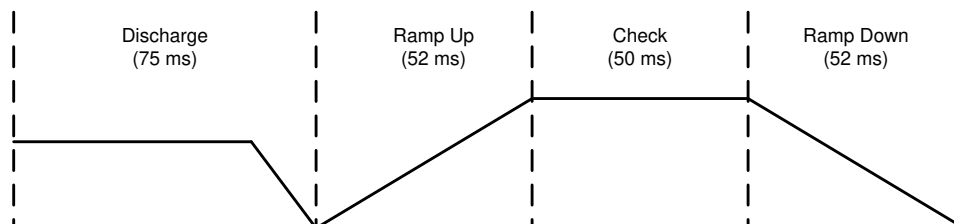
図 7-2. Load Diagnostics Sequence of Events

図 7-3 illustrates how the diagnostics determine the load based on output conditions.

図 7-3. Load Diagnostic Reporting Thresholds

7.3.4.2 Faults During Load Diagnostics

If the device detects a fault (overtemperature, overvoltage, undervoltage) during the load diagnostics test, the device exits the load diagnostics, which may result in a small transient on the output.

7.3.4.3 Protection and Monitoring

- **Overcurrent Shutdown (OCSD)**—The overcurrent shutdown forces the output into Hi-Z. The device asserts the INTZ pin and updates the I^{2}C register.
- **DC Detect**—This circuit checks for a dc offset continuously during normal operation at the output of the amplifier. If a dc offset occurs, the device asserts the INTZ pin and updates the I^{2}C register. Note that the dc detection threshold follows VDD changes.
- **Overtemperature Shutdown (OTSD)**—The device shuts down when the die junction temperature reaches the overtemperature threshold. The device asserts the INTZ pin and updates I^{2}C register. Recovery is automatic when the temperature returns to a safe level.
- **Undervoltage (UV)**—The undervoltage (UV) protection detects low voltages on VDD. In the event of an undervoltage condition, the device asserts the INTZ pin and resets the I^{2}C register.
- **Power-On Reset (POR)**—Power-on reset (POR) occurs when VDD drops below the POR threshold. A POR event causes the I^{2}C bus to go into a high-impedance state. After recovery from the POR event, the device restarts automatically with default I^{2}C register settings. The I^{2}C is active as long as the device is not in POR.
- **Overvoltage (OV) and Load Dump**—OV protection detects high voltages on VDD. If VDD reaches the overvoltage threshold, the device asserts the INTZ pin and updates the I^{2}C register. The device can withstand 40-V load-dump voltage spikes.
- **SpeakerGuard™**—This protection circuitry limits the output voltage to the value selected in I^{2}C register 0x03. This value determines both the positive and negative limits. The user can use the SpeakerGuard feature to improve battery life or protect the actuator from exceeding its excursion limits.
- **Adjacent-Pin Shorts**—The device design is such that shorts between adjacent pins do not cause damage.

7.4 Device Functional Modes

The DRV2510-Q1 device has multiple power states to optimize power consumption.

7.4.1 Operation in Shutdown Mode

The EN pin of the DRV2510-Q1 device puts the device in a shutdown mode. When EN is de-asserted (logic low), all internal blocks of the device are off to achieve ultra low power. I^{2}C is not operational in this mode and the output is in Hi-Z state.

7.4.2 Operation in Standby Mode

The STDBY pin of the DRV2510-Q1 device puts the device in a standby mode. When STDBY is asserted (logic high), some internal blocks of the device are off to achieve low power while preserving the ability to wake up quickly to achieve low latency waveform playback.

7.4.3 Operation in Active Mode

The DRV2510-Q1 device is in active mode when it has a valid supply, and it is not in either shutdown or standby modes. In this mode the DRV2510-Q1 device is fully on and reproducing at the output the input times the gain.

7.5 Programming

7.5.1 General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The bus transfers data serially, one bit at a time. The 8-bit address and data bytes are transferred with the most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on the SDA signal indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. 図 7-4 shows a typical sequence. The master device generates the 7-bit slave address and the read-write (R/W) bit to start communication with a slave device. The master device then waits for an acknowledge condition. The slave device holds the SDA signal low during the acknowledge clock period to indicate acknowledgment. When the acknowledgment occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus a R/W bit (1 byte). All compatible devices share the same signals through a bidirectional bus using a wired-AND connection.

The number of bytes that can be transmitted between start and stop conditions is not limited. When the last word transfers, the master generates a stop condition to release the bus. 図 7-4 shows a generic data-transfer sequence.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus. Pull-up resistors between 660 Ω and 4.7 kΩ are recommended. Do not allow the SDA and SCL voltages to exceed the DRV2510-Q1 supply voltage, V_{DD}.

注

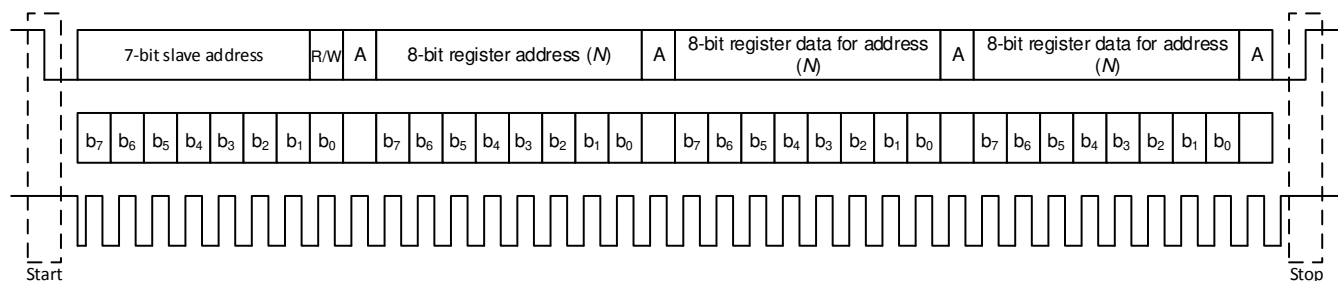The DRV2510-Q1 slave address is 0x6C (7-bit), or 1101100 in binary.

図 7-4. Typical I²C Sequence

The DRV2510-Q1 device operates as an I²C-slave 1.8-V logic thresholds, but can operate up to the V_{DD} voltage. The device address is 0x5A (7-bit), or 1011010 in binary which is equivalent to 0xB4 (8-bit) for writing and 0xB5 (8-bit) for reading.

7.5.2 Single-Byte and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte R/W operations for all registers.

During multiple-byte read operations, the DRV2510-Q1 device responds with data one byte at a time and begins at the signed register. The device responds as long as the master device continues to respond with acknowledges.

The DRV2510-Q1 supports sequential I²C addressing. For write transactions, a sequential I²C write transaction has taken place if a register is issued followed by data for that register as well as the remaining registers that follow. For I²C sequential-write transactions, the register issued then serves as the starting point and the amount of data transmitted subsequently before a stop or start is transmitted determines how many registers are written.

7.5.3 Single-Byte Write

As shown in 図 7-5, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I^{2}C device address and the read-write bit. The read-write bit determines the direction of the data transfer. For a write-data transfer, the read-write bit must be set to 0. After receiving the correct I^{2}C device address and the read-write bit, the DRV2510-Q1 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the DRV2510-Q1 internal-memory address that is accessed. After receiving the register byte, the device responds again with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.
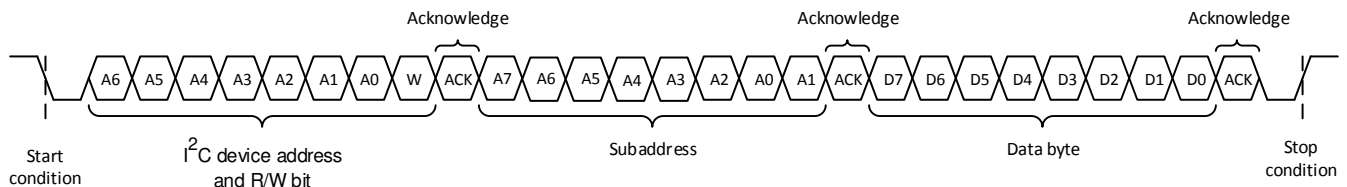
図 7-5. Single-Byte Write Transfer

7.5.4 Multiple-Byte Write and Incremental Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DRV2510-Q1 device as shown in 図 7-6. After receiving each data byte, the DRV2510-Q1 device responds with an acknowledge bit.
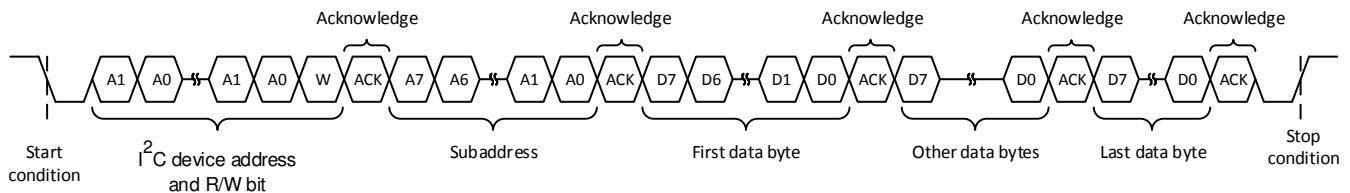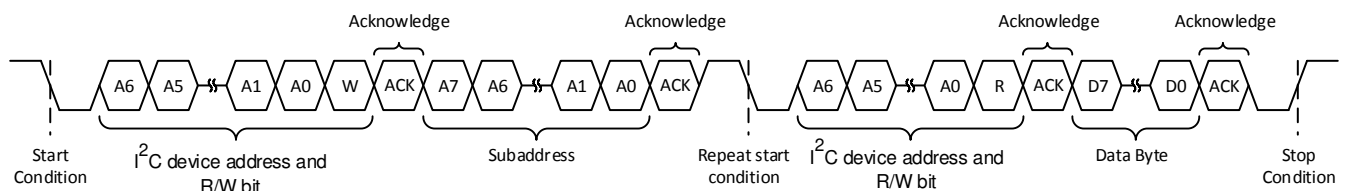

図 7-6. Multiple-Byte Write Transfer

7.5.5 Single-Byte Read

図 7-7 shows that a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I^{2}C device address and the read-write bit. For the data-read transfer, both a write followed by a read actually occur. Initially, a write occurs to transfer the address byte of the internal memory address to be read. As a result, the read-write bit is set to 0.

After receiving the DRV2510-Q1 address and the read-write bit, the DRV2510-Q1 device responds with an acknowledge bit. The master then sends the internal memory address byte, after which the device issues an acknowledge bit. The master device transmits another start condition followed by the DRV2510-Q1 address and the read-write bit again. On this occasion, the read-write bit is set to 1, indicating a read transfer. Next, the DRV2510-Q1 device transmits the data byte from the memory address that is read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer. See the note in the セクション 7.5.1 section.

図 7-7. Single-Byte Read Transfer

Product Folder Links: *DRV2510-Q1*

English Data Sheet: SLOS919

7.5.6 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the DRV2510-Q1 device to the master device as shown in 図 7-8. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.
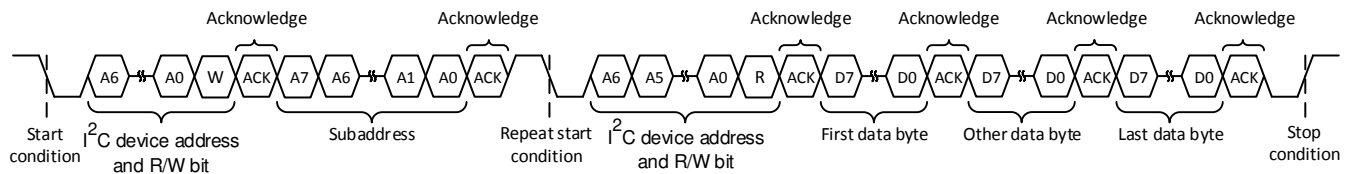
図 7-8. Multiple-Byte Read Transfer

Product Folder Links: *DRV2510-Q1*

English Data Sheet: SLOS919

7.6 Register Map

表 7-3. Register Map Overview

REG NO.	DEFAULT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x01	0x00	OVER_TEMP	DC_OFFSET	OVER_VOLT	UNDER_VOLT	OVER_CURR	LOAD_DIAG	Reserved	
0x02	0x00	DEV_ACTIVE	STDBY	DIAG_ACTIVE	FAULT	LOAD_SHORT	LOAD_OPEN	LOAD_SHORT_GND	LOAD_SHORT_VDD
0x03	0x00	GAIN[1:0]		PEAK_PROTECTION[1:2]			Reserved		FREQ_SEL

7.6.1 Address: 0x01

図 7-9. 0x01

7	6	5	4	3	2	1	0
OVER_TEMP[0]	DC_OFFSET[0]	OVER_VOLT[0]	UNDER_VOLT[0]	OVER_CURR[0]	LOAD_DIAG[0]	Reserved	
RO-0	RO-0	RO-0	RO-0	RO-0	RO-0		

表 7-4. Address: 0x01

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION	
7	OVER_TEMP	RO	0	Shows the current statuts of the thermal protection	
				0	Temperature is below the over-temperature threshold.
				1	Temperature is above the over-temperature threshold.
6	DC_OFFSET	RO	0	Shows the status of DC offset protection	
				0	DC offset protection has not occurred.
				1	DC offset protection has occurred.
5	OVER_VOLT	RO	0	Shows the status of the over-voltage protection.	
				0	VDD voltage is below the over-voltage threshold.
				1	VDD voltage is above the over-voltage threshold.
4	UNDER_VOLT	RO	0	Shows the status of the under-voltage protection.	
				0	VDD voltage is above the under-voltage threshold.
				1	VDD voltage is below the under-voltage threshold.
3	OVER_CURR	RO	0	Shows the status of the over-current protection.	
				0	An over-current event has not occurred.
				1	Device shutdown due to over-current.
2	LOAD_DIAG	RO	0	Shows the status of the load diagnostics.	
				0	An open or short has not been detected.
				1	An open or short was detected.
1:0	Reserved				

7.6.2 Address: 0x02

図 7-10. 0x02

7	6	5	4	3	2	1	0
DEV_ACTIVE [0]	STDBY [0]	DIAG_ACTIVE [0]	FAULT [0]	LOAD_SHORT [0]	LOAD_OPEN [0]	LOAD_SHORT_GND [0]	LOAD_SHORT_VDD [0]
RO-0	RO-0	RO-0	RO-0	RO-0	RO-0	RO-0	RO-0

表 7-5. Address: 0x02

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION	
7	DEV_ACTIVE	RO	0	Shows the device status (active or shutdown).	
				0	Device is shutdown.
				1	Device is active.
6	STDBY	RO	0	Shows the device standby status.	
				0	Device is not on standby.
				1	Device is on standby.
5	DIAG_ACTIVE	RO	0	Shows the status of the diagnositcs engine.	
				0	Not performing load diagnostics.
				1	Performing load diagnostics.
4	FAULT	RO	0	Shows if a fault has occurred on the system. Either over-voltage, under-voltage, over-current, over-temperature.	
				0	No fault has occurred.
				1	A fault has occurred.
3	LOAD_SHORT	RO	0	Shows whether the output is shorted.	
				0	OUT+ is not shorted to OUT-.
				1	OUT+ is shorted to OUT-.
2	LOAD_OPEN	RO	0	Shows whether the output has a proper load connected.	
				0	A proper load is connected between OUT+ and OUT-.
				1	There is an open connection between OUT+ and OUT-.
1	LOAD_SHORT_GND	RO	0	Shows whether the output is shorted to GND.	
				0	Output is not shorted to GND.
				1	Either OUT+ or OUT- is shorted to GND.
0	LOAD_SHORT_VDD	RO	0	Shows whether the output is shorted to VDD.	
				0	Output is not shorted to VDD.
				1	Either OUT+ or OUT- is shorted to VDD.

Product Folder Links: *DRV2510-Q1*

English Data Sheet: *SLOS919*

7.6.3 Address: 0x03

図 7-11. 0x03

7	6	5	4	3	2	1	0
GAIN[1:0]		PEAK_PROTECTION[2:0]			Reserved		FREQ_SEL[0]
R/W-0		R/W-0			R/W-0		R/W-0

表 7-6. Address: 0x03

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION	
7:6	GAIN[1:0]	R/W	01	Sets the gain.	
				0	20 dB.
				1	26 dB.
				2	32 dB.
				3	36 dB.
5:3	PEAK_PROTECTION[2:0]	R/W	111	Sets the peak output protection.	
				0	5V pk
				1	5.9 Vpk
				2	7 Vpk
				3	8.4 Vpk
				4	9.8 Vpk
				5	11.8 Vpk
				6	14 Vpk
				7	Protection disabled
2:1	Reserved		00	Always write default values	
0	FREQ_SEL	R/W	0	Sets the output frequency.	
				0	400 kHz.
				1	500 kHz.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The DRV2510-Q1 device is a high-efficiency driver for inductive loads, such as solenoids and voice-coils. The typical use of the device is on haptic applications where short, strong waveforms are desired to create a haptic event that will be coming from the application processor.

8.2 Typical Applications

8.2.1 Single-Ended Source

To use the DRV2510-Q1 with a single-ended source, apply either a voltage divider to bias IN- to 3 V, or use a 0.1-µF cap from IN- to GND to have the device self bias. Apply the single-ended signal to the IN+ pin through an AC coupling capacitor.
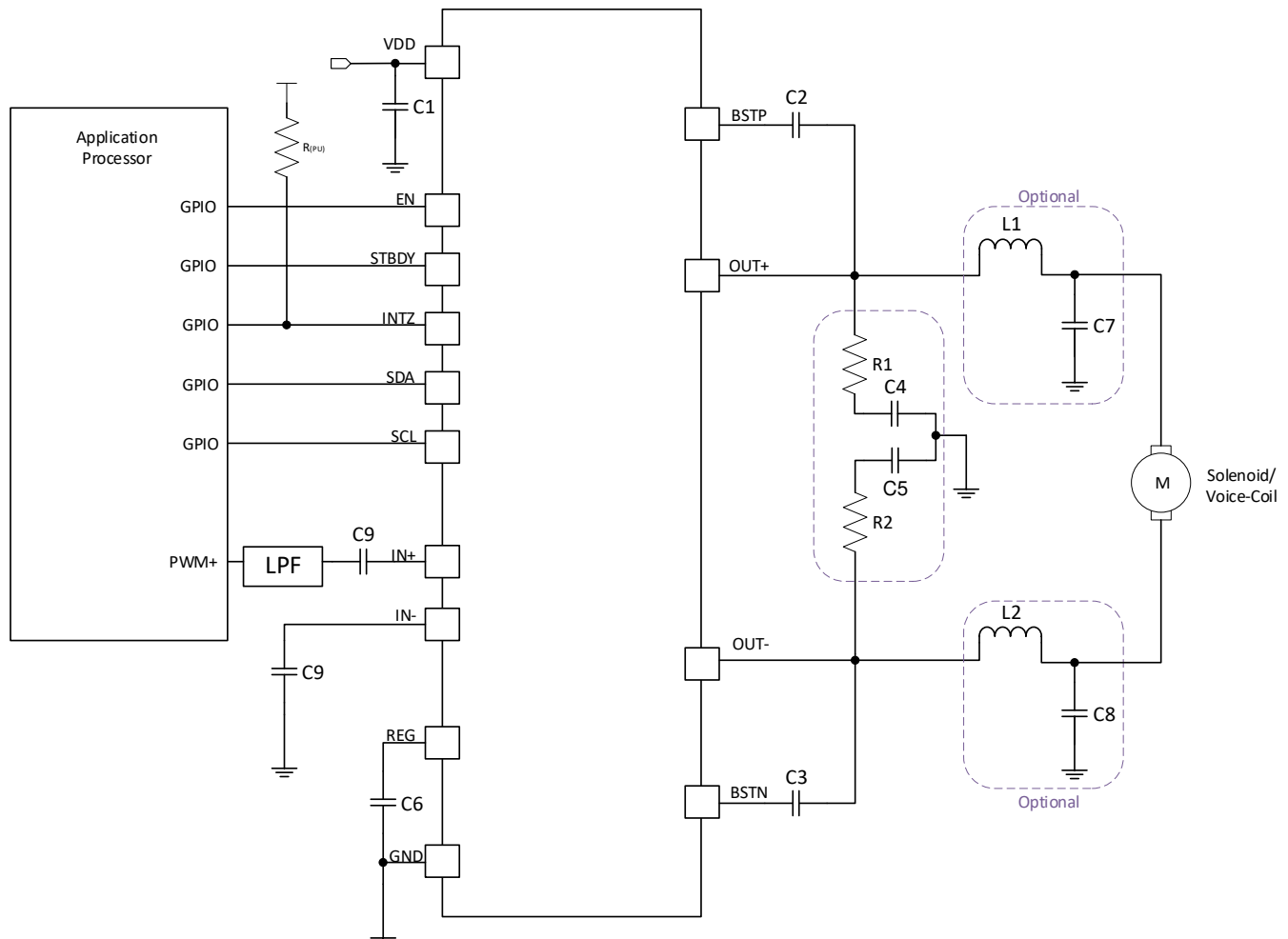

図 8-1. Typical Application Schematic

8.2.1.1 Design Requirements

For most applications the following component values found in 表 8-1 below can be used.

表 8-1. Component Requirements Table

COMPONENT	DESCRIPTION	SPECIFICATION	TYPICAL VALUE
C1	Supply capacitor	Capacitance	22 µF, 10 µF, and 0.1 µF
C2/C3	Boost capacitor	Capacitance	0.22 µF
C4/C5	Output snubber capacitor	Capacitance	470 pF
C6	Regulator capacitor	Capacitance	1 µF
C9	Input decoupling capacitor	Capacitance	0.1 µF
R1/R2	Output snubber resistor	Resistance	3.3 Ω
$R_{(PU)}$	Pull-up resistor	Resistance	100 kΩ

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Optional Components

Note that in the diagrams, there are a few optional external components. These optional external components may be needed in the application to meet EMI/EMC standards and specifications by filters necessary frequency spectrums.

8.2.1.2.2 Capacitor Selection

A bulk bypass capacitor should be mounted between VBAT and GND. The capacitance needs to be >22 uF with a X5R or better rating on the power pins to GND. Also include two ceramic capacitors in the ranges of 220 pF to 1 uF and 100 nF to 1 uF. The bootstrap capacitors, BSTP and BSTN, should be 220-nF ceramic capacitors of quality X5R or better rated for at least the maximum rating of the pin.

8.2.1.2.3 Solenoid Selection

The DRV2510-Q1 solenoid driver can accommodate a variety of solenoids. Solenoids should have an equivalent resistance of 1.6 Ω or greater. Solenoids with lower resistances are prone to driving high currents. A maximum peak current of 3-A should not be exceeded.

8.2.1.2.4 Output Filter Considerations

The output filter is optional and is mainly for limiting peak currents. A second-order Butterworth low-pass filter with the cut-off frequency set to a few kilohertz should be sufficient. See Equation 1, through Equation 4, for example filter design.

$$H(s) = \frac{1}{s^2 + \sqrt{2}s + 1} \tag{1}$$

$$L_x = \frac{\sqrt{2} \times R_L}{2\omega_o} \tag{2}$$
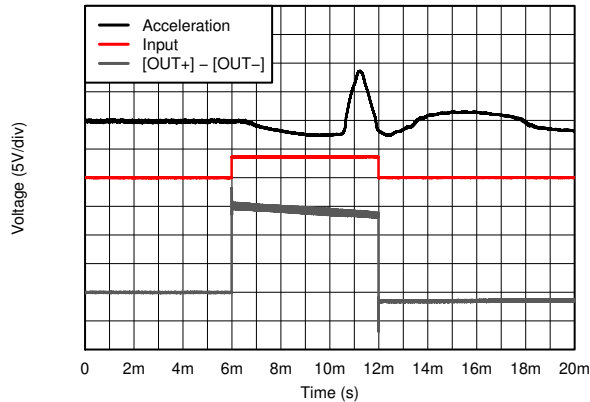
$$2 \times C_F = \frac{\sqrt{2}}{2 \times \frac{R_L}{2} \times \omega_0} \tag{3}$$

$$\omega_0 = 2\pi \times f \tag{4}$$

8.2.1.3 Application Curves

These application curves were taken using an HA200 solenoid with a 100-g mass, and the acceleration was measured using the DRV-AAC16-EVM accelerometer. The following scales apply to the graphs:
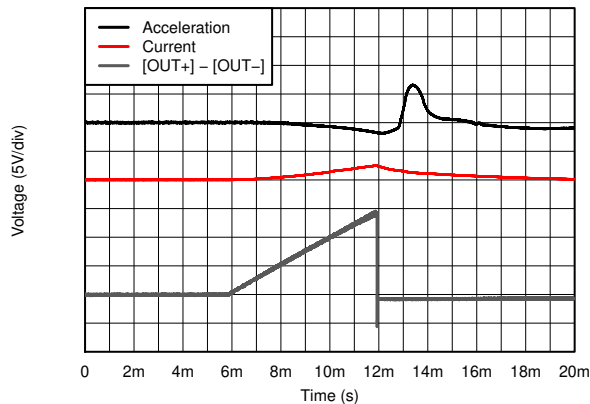
- Output Differential Voltage scale is shown on the plots at 5-V/div
- Acceleration scale is 5.85-G/div
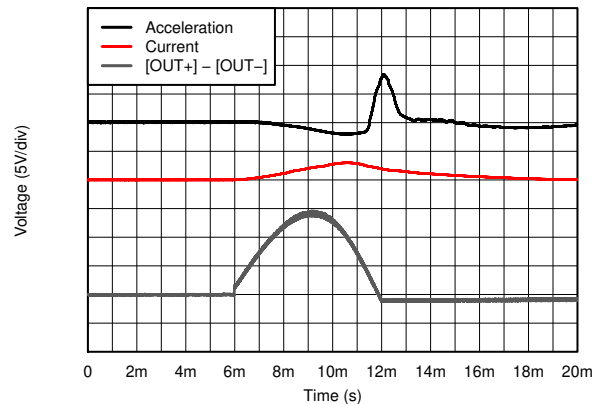- Current scale is 2-A/div

図 8-2. Voltage and Acceleration vs Time (Input Square Wave)
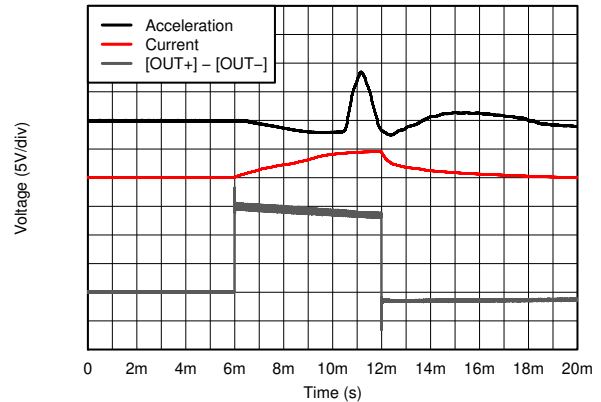
図 8-3. Voltage and Acceleration vs Time (Square Wave)

図 8-4. Voltage and Acceleration vs Time (Ramp Wave)

図 8-5. Voltage and Acceleration vs Time (1/2 Sine Wave)

Product Folder Links: *DRV2510-Q1*

8.2.1.4 Differential Input Diagram

To use the DRV2510-Q1 with a differential input source, apply both inputs differentially through AC coupling capacitors from a control source (GPIO, DAC, etc...).
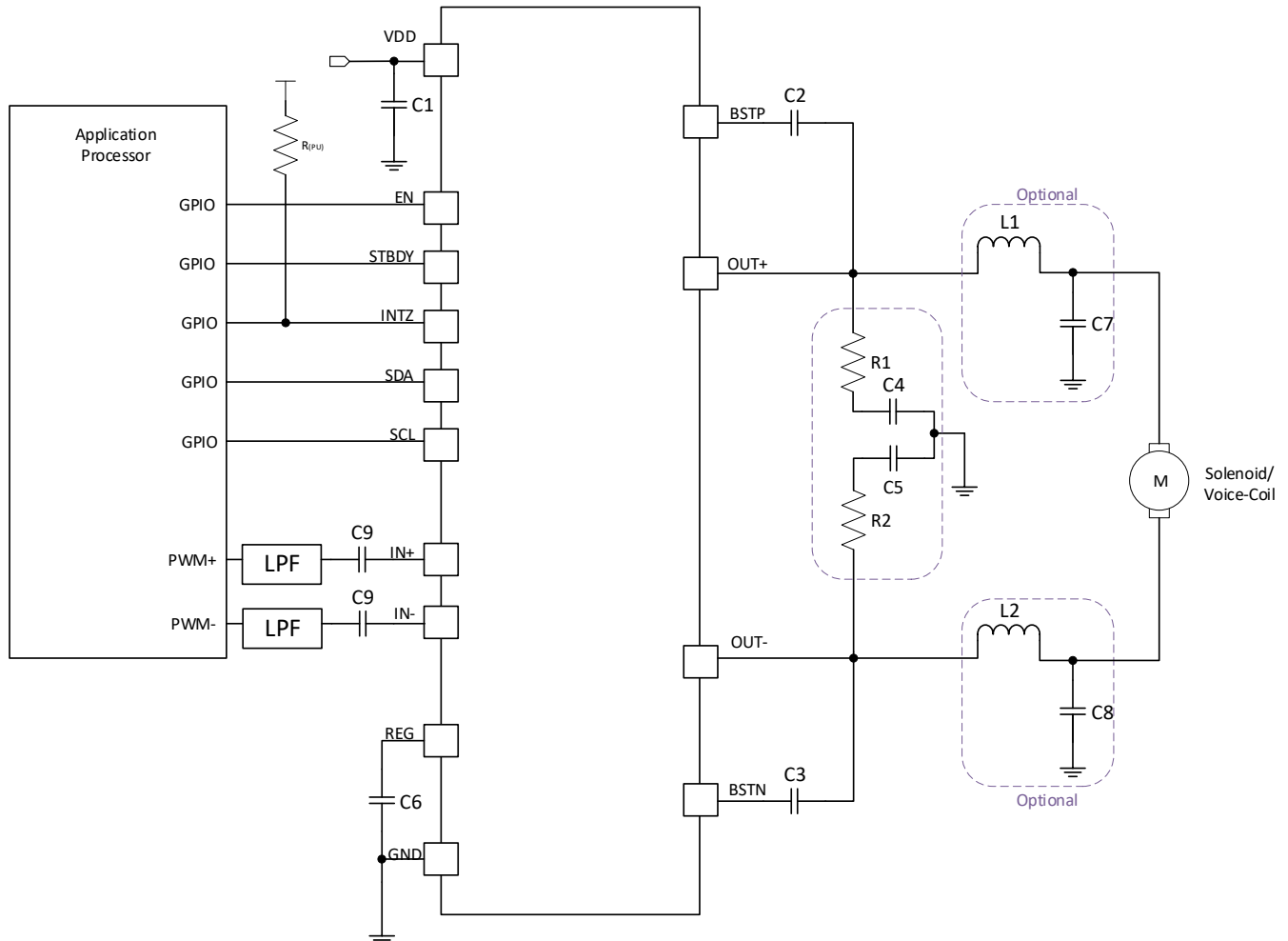

図 8-6. Typical Application Schematic

9 Power Supply Recommendations

The DRV2510-Q1 device operates from 4.5 V - 18 V and this supply should be able to handle high surge currents in order to meet the high currrent draws for haptics effects. Additionally the DRV2510-Q1 should have 22-µF, 10-µF and 0.1-µF ceramic capacitors near the VDD pin for additional decoupling from trace routing.

10 Layout

10.1 Layout Guidelines

The EVM layout optimizes for thermal dissipation and EMC performance. The DRV2510-Q1 device has a thermal pad down, and good thermal conduction and dissipation require adequate copper area. Layout also affects EMC performance. It is best practice to use the same/similiar layout as shown below in the DRV2510Q1EVM.
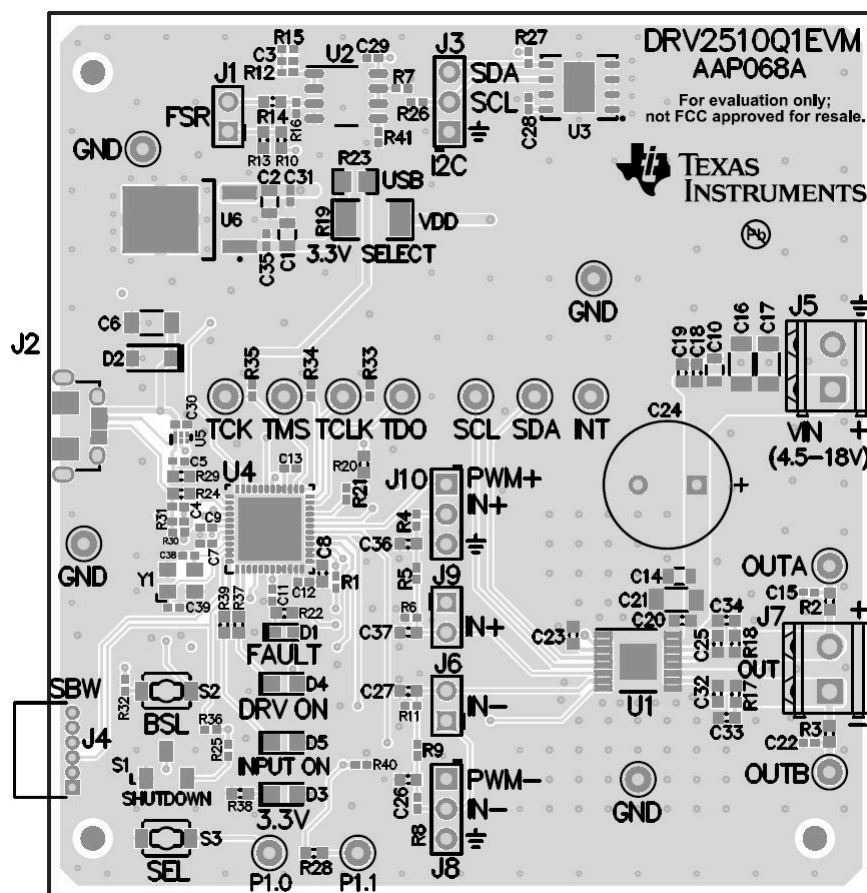
10.2 Layout Example

図 **10-1. DRV2510-Q1 EVM**

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Product Folder Links: *DRV2510-Q1*

English Data Sheet: *SLOS919*

11 Device and Documentation Support

11.1 Device Support

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11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV2510QPWPRQ1	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV2510
DRV2510QPWPRQ1.B	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV2510

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV2510QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV2510QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0

PWP 16

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE
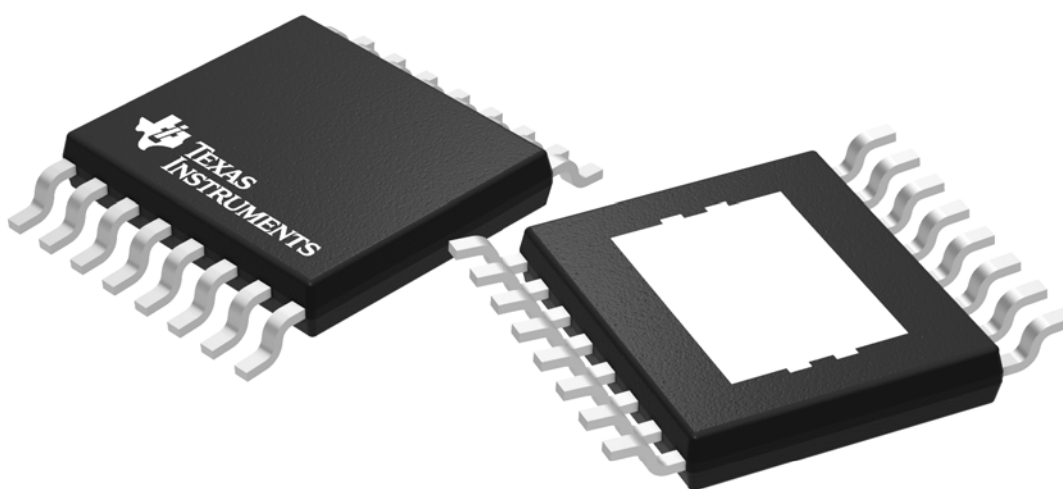
Images above are just a representation of the package family, actual package may vary.
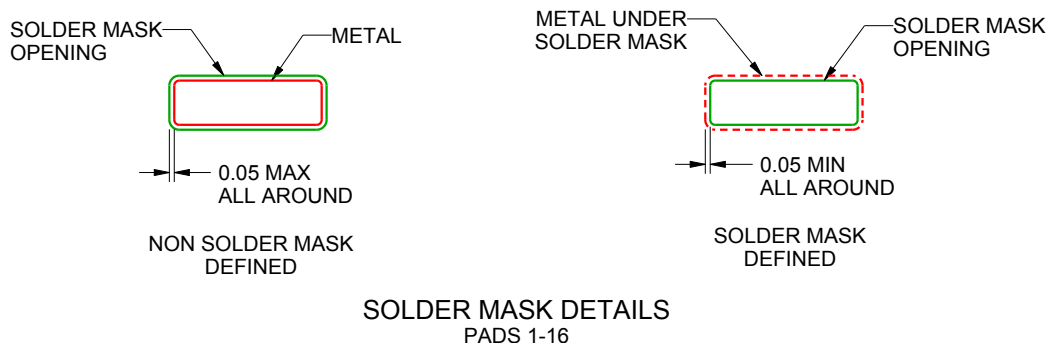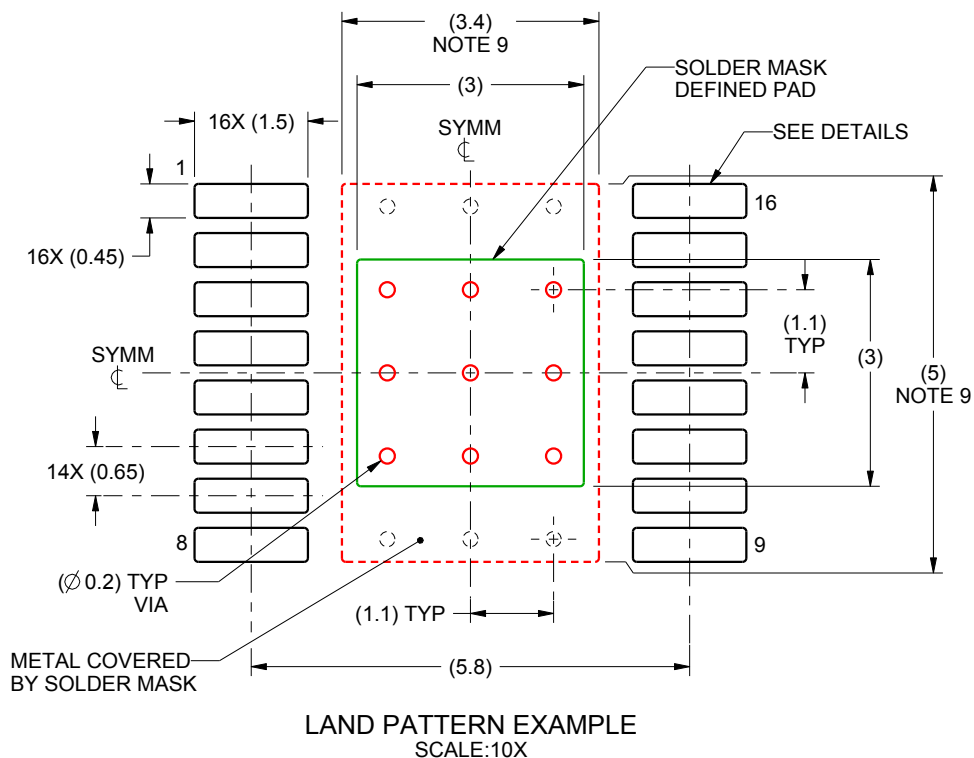Refer to the product data sheet for package details.

4073225-3/J

TEXAS
INSTRUMENTS

6.6 / 6.2 TYP

PIN 1 ID AREA

14X 0.65

A

1

16

5.1 / 4.9 NOTE 3

2X 4.55

8

9

B

4.5 / 4.3

16X 0.30 / 0.19

⊕ | 0.1 Ⓜ | C | A Ⓢ | B Ⓢ

C

SEATING PLANE

⌒ | 0.1 | C

SEE DETAIL A

(0.15) TYP

2X 0.95 MAX NOTE 5

4X 0.15 MAX NOTE 5

THERMAL PAD

3.0 / 2.4

3.0 / 2.4

0.25

GAGE PLANE

0° - 8°

0.75 / 0.50

(1)

1.2 MAX

0.15 / 0.05

DETAIL A
TYPICAL

4218971/A   01/2016

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.

(3.4)
NOTE 9

(3)

16X (1.5)

SOLDER MASK
DEFINED PAD

SEE DETAILS

SYMM

1

16

16X (0.45)

(1.1)
TYP

(3)

(5)
NOTE 9

SYMM

14X (0.65)

8

9

(Ø 0.2) TYP
VIA

(1.1) TYP

METAL COVERED
BY SOLDER MASK

(5.8)

LAND PATTERN EXAMPLE
SCALE:10X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
PADS 1-16

4218971/A   01/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

PWP0016B

PowerPAD™ TSSOP - 1.2 mm max height

(3)
BASED ON
0.125 THICK
STENCIL

16X (1.5)

1

16X (0.45)

(R0.05) TYP

16

SYMM
₵

(3)
BASED ON
0.125 THICK
STENCIL

14X (0.65)

8

9

METAL COVERED
BY SOLDER MASK

SYMM
₵

(5.8)

SEE TABLE FOR
DIFFERENT OPENINGS
FOR OTHER STENCIL
THICKNESSES
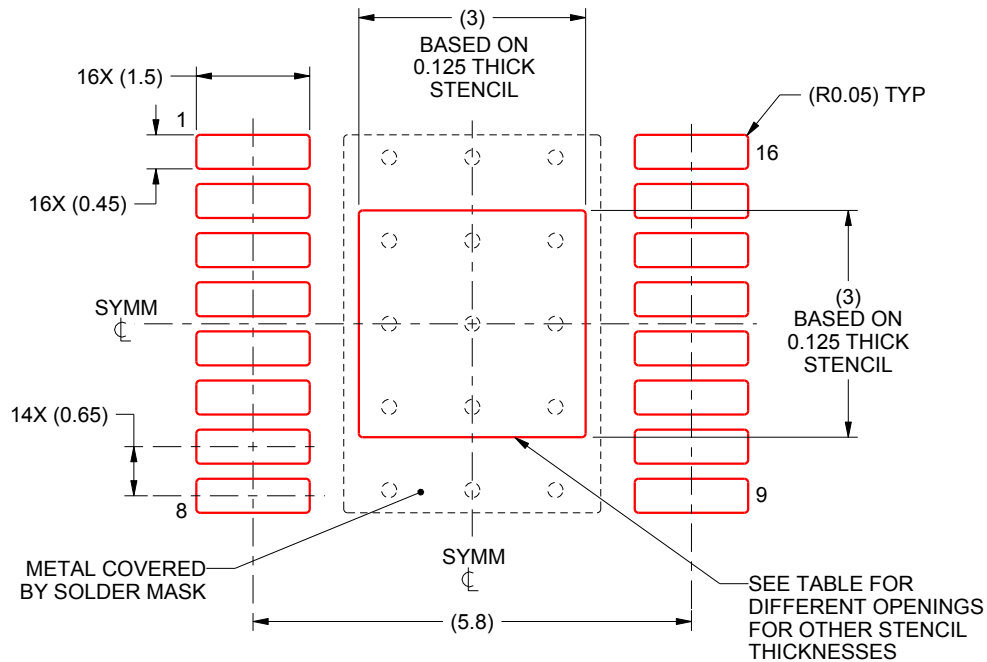
SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.35 X 3.35
0.125	3 X 3 (SHOWN)
0.15	2.74 X 2.74
0.175	2.54 X 2.54

4218971/A   01/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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