



DRV120 Single-Channel Relay, Solenoid, Valve Low-Side Driver With Current Regulation

1 Features

- Integrated MOSFET With PWM to Control Solenoid Current
 - Integrated Sense Resistor for Regulating Solenoid Current
- Fast Ramp-Up of Solenoid Current to Guarantee Activation
- Solenoid Current is Reduced in Hold Mode for Lower Power and Thermal Dissipation
- Peak Current, Keep Time at Peak Current, Hold Current, and PWM Clock Frequency Can Be Set Externally. They Can Also Be Operated at Nominal Values Without External Components.
- Internal Supply Voltage Regulation
 - Up to 28-V External Supply
- Protection
 - Thermal Shutdown
 - Undervoltage Lockout (UVLO)
 - Maximum Ramp Time
 - Optional STATUS Output
- Operating Temperature Range: -40°C to 105°C
- 8-Pin and 14-Pin TSSOP Package Options

2 Applications

- Electromechanical Drivers: Solenoids, Valves, Relays
- White Goods, Solar, Transportation

3 Description

The DRV120 device is a PWM current driver for solenoids. The device is designed to regulate the current with a well-controlled waveform to guarantee activation and to reduce power dissipation at the same time. The solenoid current is ramped up fast to ensure opening of the valve or relay. After the initial ramping, solenoid current is kept at peak value to ensure the correct operation, after which it is reduced to a lower hold level in order to avoid thermal problems and reduce power dissipation.

The peak current duration is set with an external capacitor. The current ramp peak and hold levels, as well as PWM frequency, can independently be set with external resistors. External setting resistors can also be omitted, if the default values for the corresponding parameters are suitable for the application.

The DRV120 can operate from an external 6-V to 28-V supply.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV120	TSSOP (14)	5.00 mm × 4.40 mm
	TSSOP (8)	3.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

I_{SOLENOID} vs Time

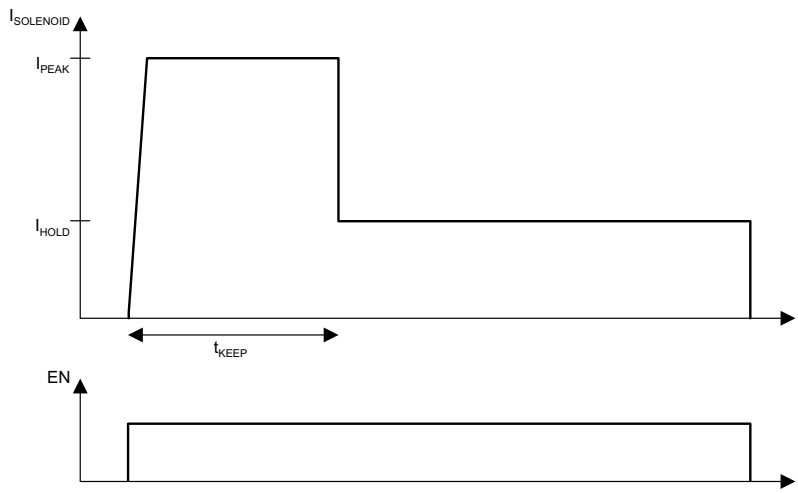


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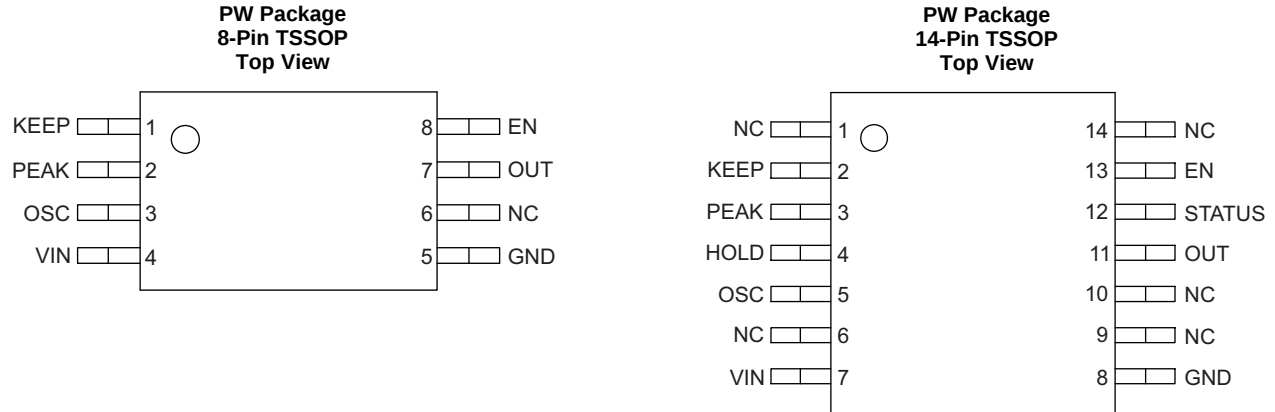
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2015) to Revision C	Page
• Changed the title of the data sheet	1
• Changed the minimum R_{OSC} value in the f_{PWM} equation from 66.67 k Ω to 160 k Ω	9
• Changed the <i>PWM Clock Frequency Setting</i> graph.....	9
• Added the <i>Receiving Notification of Documentation Updates</i> section	13

Changes from Revision A (August 2012) to Revision B	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

5 Pin Configuration and Functions



Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	8-PIN PW ⁽¹⁾	14-PIN PW		
EN	8	13	I	Enable
GND	5	8	—	Ground
HOLD	-	4	I	Hold current set
KEEP	1	2	I	Keep time set
NC	6	1, 6, 9, 10, 14	—	No connect
OSC	3	5	I	PWM frequency set
OUT	7	11	O	Controlled current sink
PEAK	2	3	I	Peak current set
STATUS	-	12	O	Open-drain fault indicator
VIN	4	7	I	6-V to 28-V supply

(1) In the 8-pin package, the HOLD pin is not bonded out. For this package, the HOLD mode is configured to default (internal) settings.

6 Specifications

6.1 Absolute Maximum Ratings

See ⁽¹⁾ and ⁽²⁾

	MIN	MAX	UNIT
VIN Input voltage	−0.3	28	V
Voltage on EN, STATUS, PEAK, HOLD, OSC, SENSE, RAMP	−0.3	7	V
Voltage on OUT	−0.3	28	V
T _J Operating virtual junction temperature	−40	125	°C
T _{stg} Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
I _{OUT} Average solenoid DC current			125	mA
V _{IN} Supply voltage	6	12	26	V
C _{IN} Input capacitor	1	4.7		μF
L Solenoid inductance		1		H
T _A Operating ambient temperature	–40		105	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DRV120		UNIT
		PW [TSSOP]		
		8 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	183.8	122.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	69.2	51.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	112.6	64.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	10.4	6.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	110.9	63.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

 $V_{IN} = 14\text{ V}$, $T_A = -40^{\circ}\text{C}$ to 105°C , over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I _Q	Standby current	EN = 0, V _{IN} = 14 V		100	150	μA
	Quiescent current	EN = 1, V _{IN} = 14 V		300	400	
CURRENT DRIVER						
R _{OUT}	OUT to GND resistance	I _{OUT} = 200 mA		1.7	2.5	Ω
f _{PWM}	PWM frequency	OSC = GND	15	20	25	kHz
D _{MAX}	Maximum PWM duty cycle			100		%
D _{MIN}	Minimum PWM duty cycle			9		%
t _D	Start-up delay	Delay between EN going high until driver enabled ⁽¹⁾ , f _{PWM} = 20 kHz		25	50	μs
CURRENT CONTROLLER, INTERNAL SETTINGS						
I _{PEAK}	Peak current	PEAK = GND	160	200	240	mA
I _{HOLD}	Hold current	HOLD = GND	40	50	60	mA
CURRENT CONTROLLER, EXTERNAL SETTINGS						
t _{KEEP} ⁽²⁾	Externally set keep time at peak current	C _{KEEP} = 1 μF		75		ms
I _{PEAK}	Externally set peak current	R _{PEAK} = 50 kΩ		250		mA
		R _{PEAK} = 200 kΩ		83		
I _{HOLD}	Externally set hold current	R _{HOLD} = 50 kΩ		100		mA
		R _{HOLD} = 200 kΩ		33		
f _{PWM}	Externally set PWM frequency	R _{OSC} = 50 kΩ		60		kHz
		R _{OSC} = 200 kΩ		20		
LOGIC INPUT LEVELS (EN)						
V _{IL}	Input low level				1.3	V
V _{IH}	Input high level		1.65			V
R _{EN}	Input pullup resistance		350	500		kΩ
LOGIC OUTPUT LEVELS (STATUS)						
V _{OL}	Output low level	Pulldown activated, I _{STATUS} = 2 mA			0.3	V
I _{IL}	Output leakage current	Pulldown deactivated, V(STATUS) = 5 V			1	μA
UNDERVOLTAGE LOCKOUT						
V _{UVLO}	Undervoltage lockout threshold			4.6		V
THERMAL SHUTDOWN						
T _{TSD}	Junction temperature shutdown threshold			160		°C
T _{TSU}	Junction temperature start-up threshold			140		°C

(1) Logic HIGH between 4 V and 7 V. Note: absolute maximum voltage rating is 7 V.

(2) Either internal or external t_{KEEP} time setting is selected to be activated during manufacturing of production version of DRV120.

6.6 Typical Characteristics

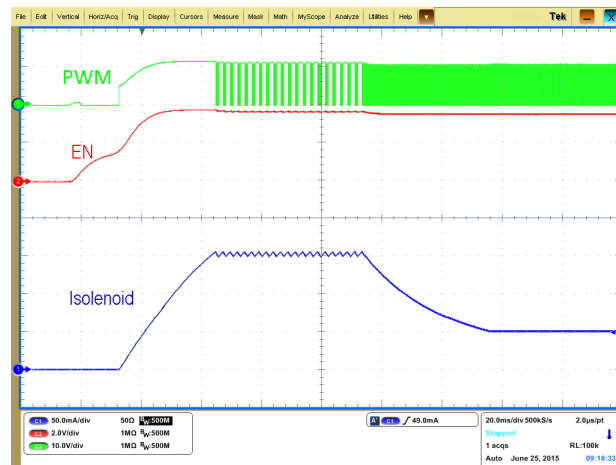


Figure 1. Solenoid Current, EN, and PWM vs Time

Feature Description (continued)

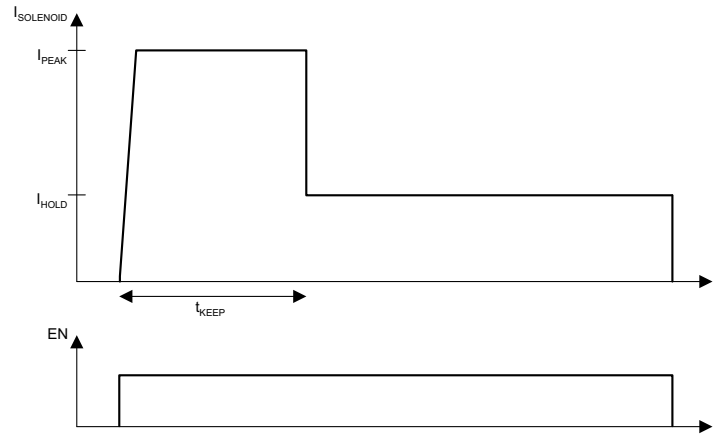


Figure 2. Typical Current Waveform Through the Solenoid

t_{KEEP} is set externally by connecting a capacitor to the KEEP pin. A constant current is sourced from the KEEP pin that is driven into an external capacitor resulting in a linear voltage ramp. When the KEEP pin voltage reaches 75 mV, the current regulation reference voltage, V_{REF} , is switched from V_{PEAK} to V_{HOLD} . Dependency of t_{KEEP} from the external capacitor size can be calculated with [Equation 1](#).

$$t_{KEEP} [s] = C_{KEEP} [F] \cdot 75 \cdot 10^3 \left[\frac{s}{F} \right] \quad (1)$$

The current control loop regulates, cycle-by-cycle, the solenoid current by using an internal current-sensing resistor and MOSFET switch. During the ON-cycle, current flows from OUT pin to GND pin through the internal switch as long as voltage across the current-sensing resistor is less than V_{REF} . As soon as the current sensing voltage is above V_{REF} , the internal switch is immediately turned off until the next ON-cycle is triggered by the internal PWM clock signal. In the beginning of each ON-cycle, the internal switch is turned on and stays on for at least the time determined by the minimum PWM signal duty cycle, D_{MIN} .

I_{PEAK} and I_{HOLD} depend on fixed resistance values R_{PEAK} and R_{HOLD} approximately as shown in [Figure 3](#). If the PEAK pin is connected to ground or if R_{PEAK} or R_{HOLD} is below 33.33 k Ω (typical value), then I_{PEAK} is at its default value (internal setting) of 200 mA for I_{PEAK} and 50 mA for I_{HOLD} . The I_{PEAK} value can alternatively be set by connecting an external resistor to ground from the PEAK pin. For example, if a 50-k Ω ($= R_{PEAK}$) resistor is connected between PEAK and GND, then the externally set I_{PEAK} level will be 250 mA. If $R_{PEAK} = 200$ k Ω is, then the externally set I_{PEAK} level will be 83 mA. In the 8-pin package, I_{HOLD} is set to 50 mA by default. In the 14-pin package, external settings of I_{HOLD} works in the same way as I_{PEAK} . External settings for I_{PEAK} and I_{HOLD} are independent of each other. Approximate I_{PEAK} and I_{HOLD} values can be calculated by using [Equation 2](#) and [Equation 3](#).

$$I_{PEAK} = \frac{250mA}{R_{PEAK}} \cdot 66.67k\Omega; 66.67k\Omega < R_{PEAK} < 550k\Omega \quad (2)$$

$$I_{HOLD} = \frac{100mA}{R_{HOLD}} \cdot 66.67k\Omega; 66.67k\Omega < R_{HOLD} < 250k\Omega \quad (3)$$

Feature Description (continued)

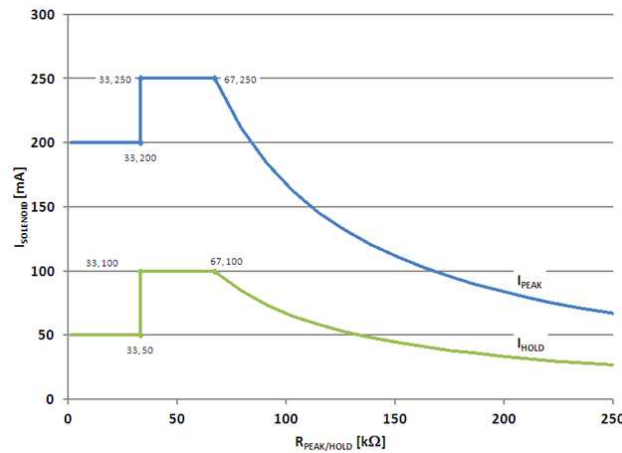


Figure 3. PEAK and HOLD Mode Current Settings

Frequency of the internal PWM clock signal, PWM_{CLK} , that triggers each ON-cycle can be adjusted by external resistor, R_{OSC} , connected between OSC and GND. Frequency as a function of resistor value is shown in Figure 4. Default frequency is used when OSC is connected to GND directly. Use Equation 4 to calculate the PWM frequency as a function of the external fixed adjustment resistor value (greater than 160 kΩ).

$$f_{PWM} = \frac{60 \text{ kHz}}{R_{OSC}} \times 66.67 \text{ k}\Omega; 160 \text{ k}\Omega < R_{OSC} < 2 \text{ M}\Omega \quad (4)$$

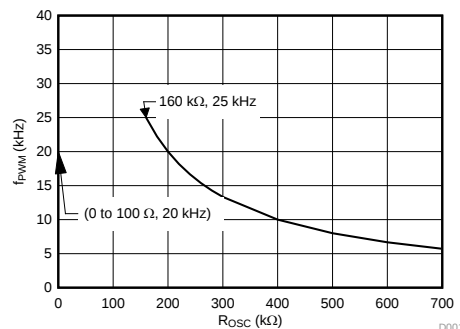


Figure 4. PWM Clock Frequency Setting

Open-drain STATUS output is deactivated if either undervoltage lockout or thermal shutdown blocks have triggered.

7.4 Device Functional Modes

The DRV120 transitions through three different states. The first is the OFF state, where the EN pin is low and the PWM output is off. The second is the PEAK state, which begins when the EN pin is pulled high by an external controller or internal pullup, and ends once t_{KEEP} has been reached. During this state, the PWM operates in order to reach the I_{PEAK} set by the R_{PEAK} . Finally, once t_{KEEP} has been reached, the PWM continues to operate, but at the I_{HOLD} level. This continues until the EN pin is forced low again and the PWM turns off.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV120 device is designed to operate a solenoid valve or relay. A typical DC input design will be outlined in [Typical Application](#). Approximate resistor and capacitor values for the peak current, hold current, and keep time will be derived for a sample application.

8.2 Typical Application

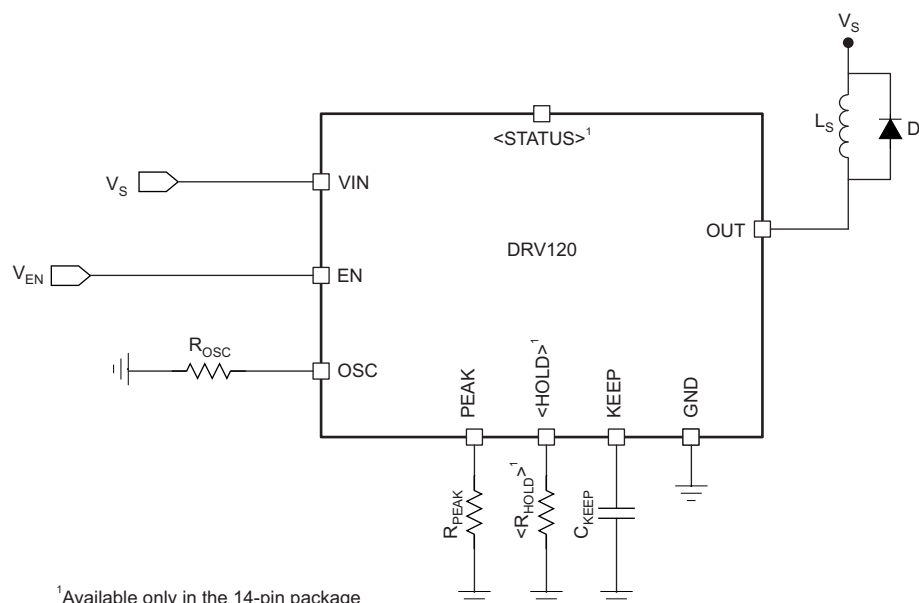


Figure 5. Default Configuration

8.2.1 Design Requirements

The key elements to identify here are the system input voltage, peak current, hold current, and peak keep time values required for the solenoid or relay being used. With these values, approximate R_S , R_{PEAK} , R_{HOLD} (for 14-pin package), and C_{KEEP} values can be determined and the proper FET and diode can be identified. R_{OSC} can be varied in order to tune the circuit to the chosen solenoid or relay.

8.2.2 Detailed Design Procedure

First, with the known peak current, hold current, and peak keep time values known, the R_{PEAK} , R_{HOLD} (for 14-pin package), and C_{KEEP} values can be determined. Calculation will proceed based on example values shown in [Table 1](#).

Table 1. Sample Application Values

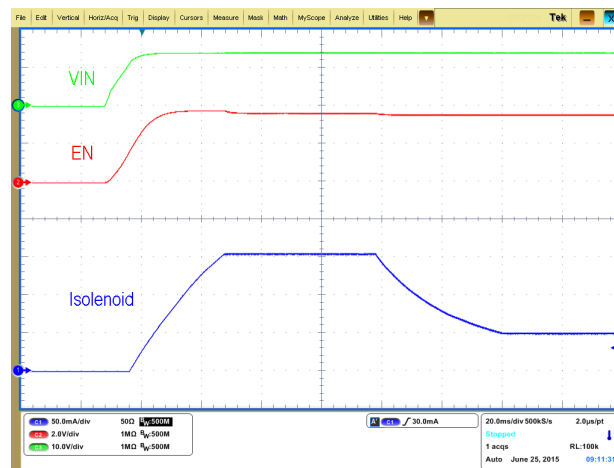
VARIABLE	VALUE
Peak current	150 mA
Hold current	50 mA
Keep time	100 ms

R_{PEAK} and R_{HOLD} (if applicable) can be determined using [Equation 2](#) and [Equation 3](#). For the sample values, R_{PEAK} is set to 111 k Ω and R_{HOLD} can be shorted to GND. TI recommends that a 0- Ω resistor is used for prototyping in case changes to this value are desired.

Next, C_{KEEP} can be set based on [Equation 1](#), 1.33 μ F for the sample values. R_{OSC} can initially be shorted to GND, but again a 0- Ω resistor is recommended for prototyping. Additionally, a filter on the SENSE line may be added if it will be in a high-noise environment and is recommended for prototyping. Typical values for this are 1 k Ω and 100 pF.

Finally, a current recirculation diode must be chosen based on the current values defined in [Table 1](#). The current recirculation diode should be a fast recovery diode.

8.2.3 Application Curves



$$L_{ind} = 1 \text{ H}$$

$$R_{ind} = 50 \text{ } \Omega$$

Figure 6. $I_{SOLENOID}$, EN, and V_{IN} vs Time

9 Power Supply Recommendations

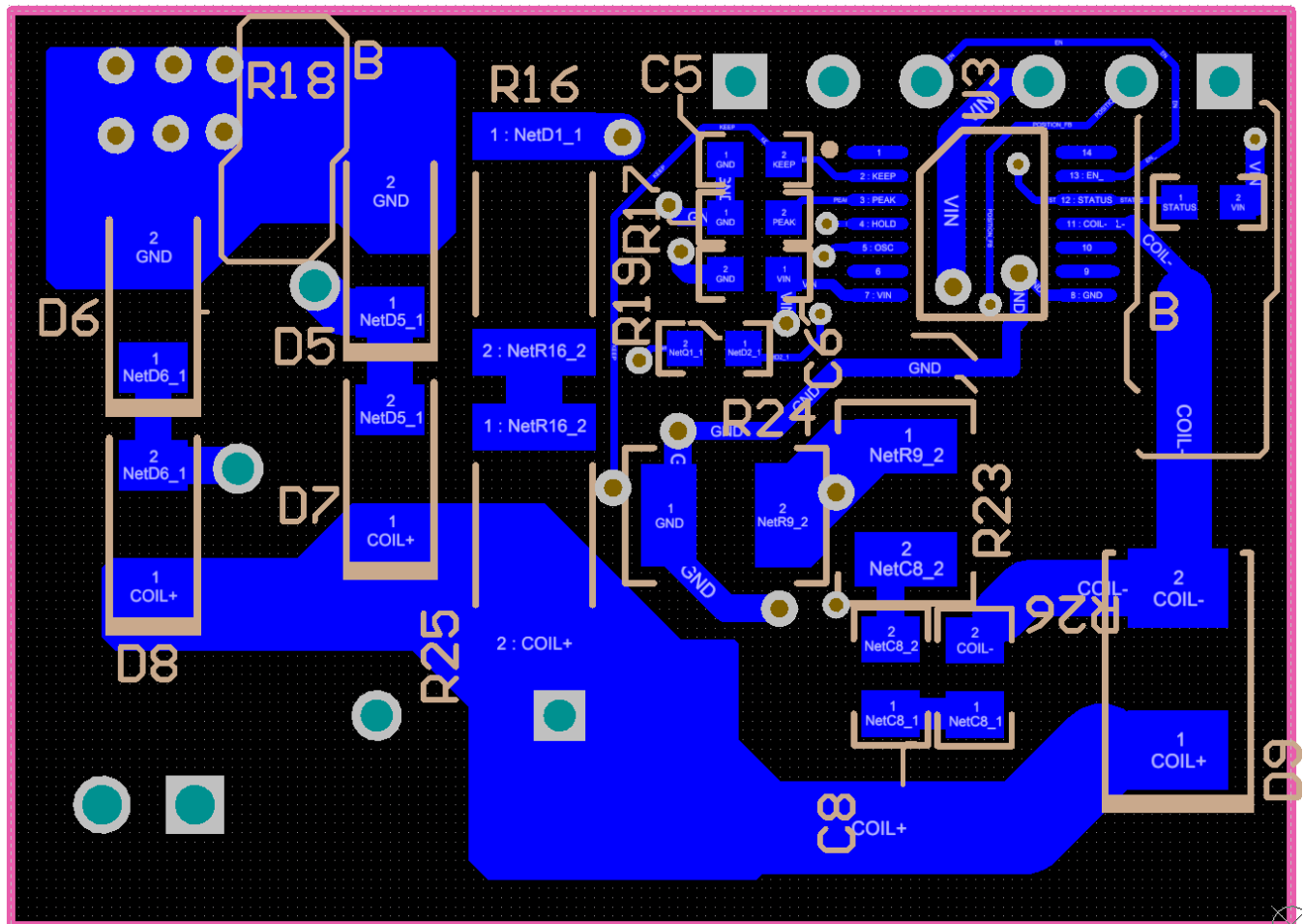
The input supply range must be at least 6 V and should be below 26 V. An input capacitor of 4.7 μF (typical) is required as well. Current requirements will be set by the required current from the solenoid.

10 Layout

10.1 Layout Guidelines

The trace for the solenoid or relay current should be wide in order to prevent any unexpected voltage drop. Diode placement should not be far from the inductor and both should be placed close to the output.

10.2 Layout Example



11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

[Current Controlled Driver for 230V AC Solenoids Reference Design
DRV110 and DRV120 Evaluation Modules \(EVM\)](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV120APWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	120A
DRV120APWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	120A
DRV120APWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	120A
DRV120APWRG4.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	120A
DRV120PWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	120
DRV120PWR.B	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	120

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

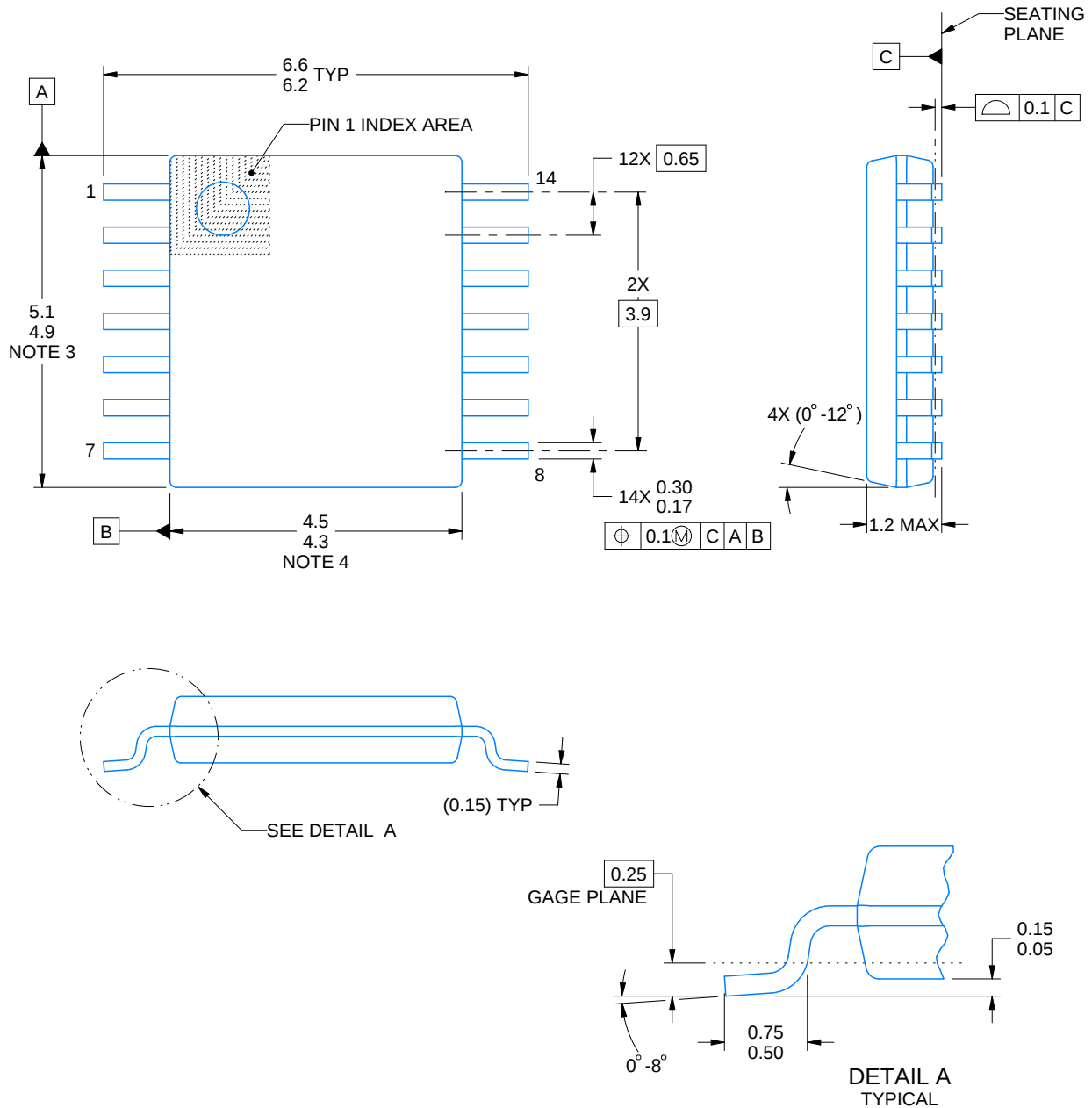
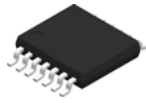
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV120APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV120APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV120PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV120APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
DRV120APWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
DRV120PWR	TSSOP	PW	8	2000	353.0	353.0	32.0



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NOTES:

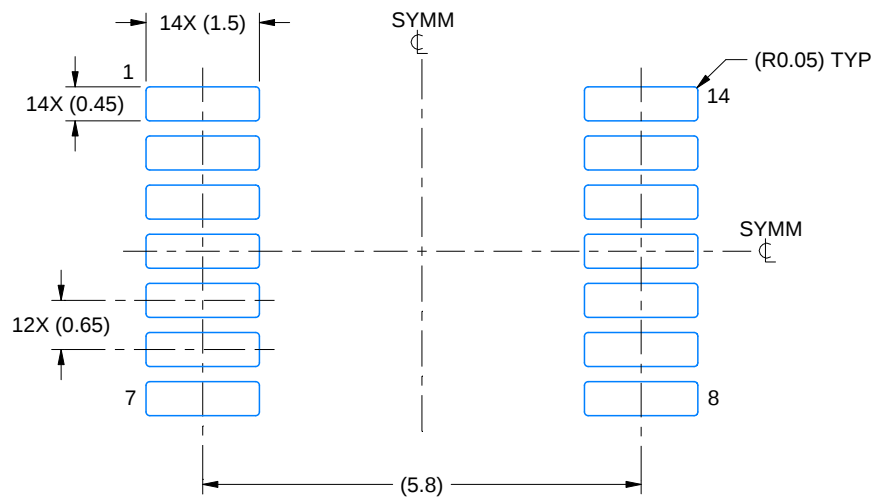
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

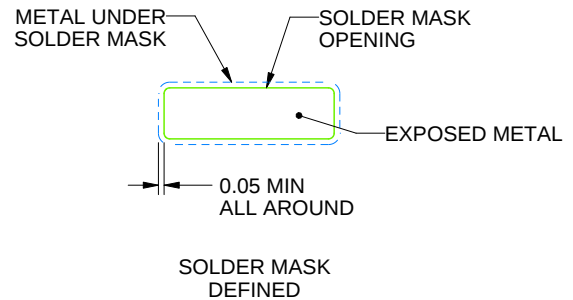
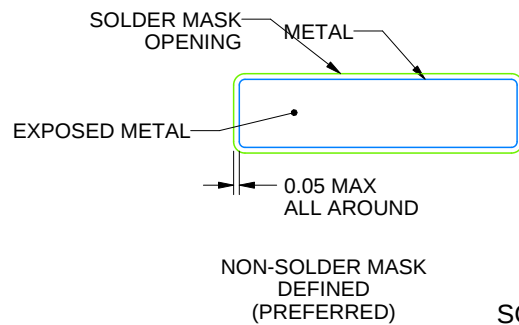
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

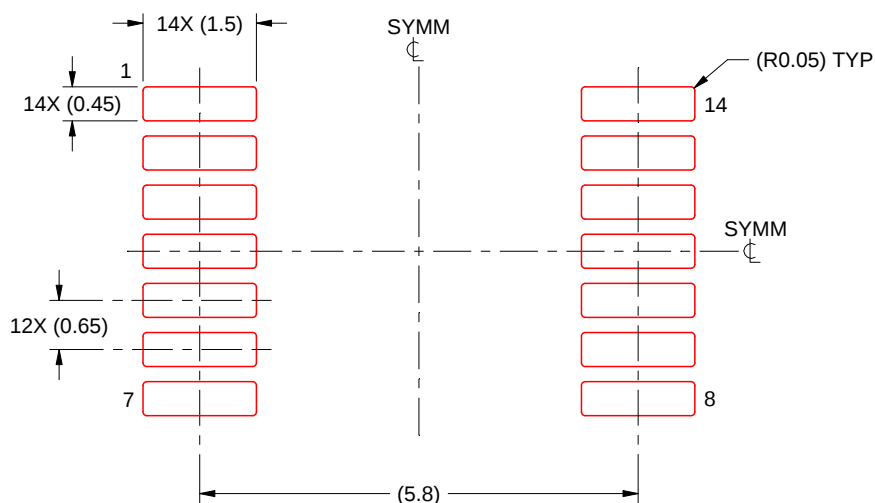
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

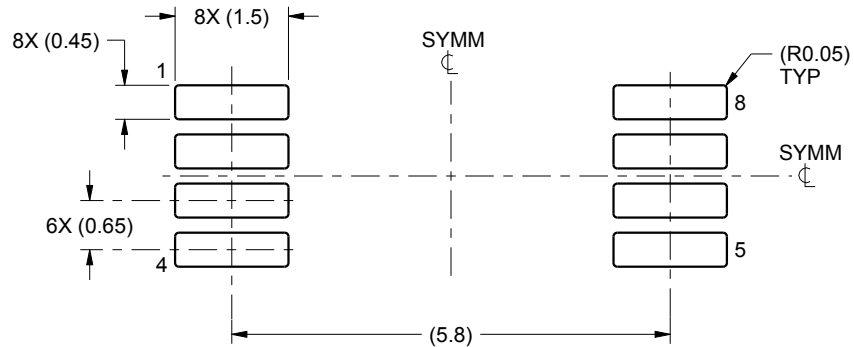
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

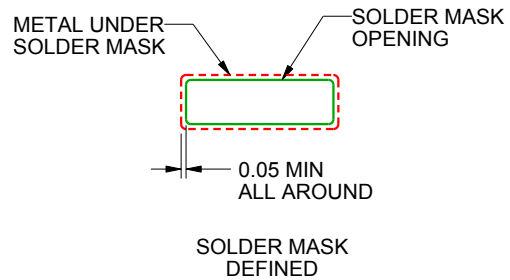
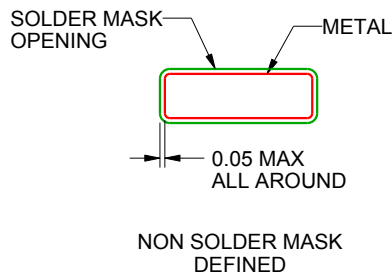
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

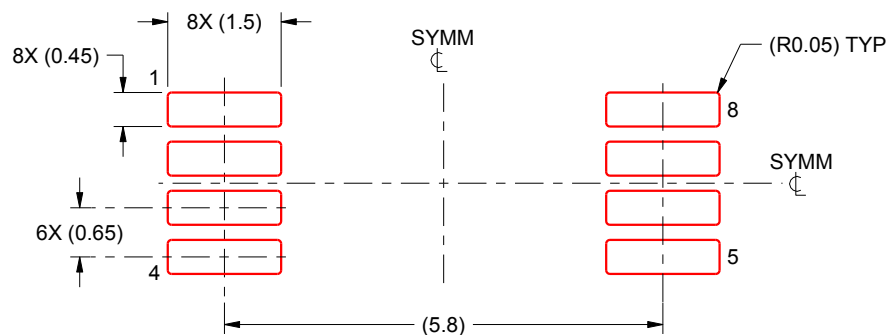
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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