



# DRA78x インフォテインメント・アプリケーション・プロセッサ

## 1 デバイスの概要

### 1.1 特長

- インフォテインメント・アプリケーション用に設計されたアーキテクチャ
- 最大2つのC66x浮動小数点VLIW DSP
  - C67xおよびC64x+と完全にオブジェクト・コード互換
  - サイクルごとに最高32回の16×16ビット固定小数点乗算
- 最大512KBのオンチップL3 RAM
- レベル3 (L3)とレベル4 (L4)の相互接続
- メモリ・インターフェイス(EMIF)モジュール
  - DDR-1066までのDDR3/DDR3Lをサポート
  - DDR-800までのDDR2をサポート
  - 最大2GBをサポート
- デュアル Arm® Cortex®-M4 (IPU)
- Vision AccelerationPac
  - 組み込みのビジョン・エンジン(EVE)
- ディスプレイ・サブシステム
  - DMAエンジン搭載のディスプレイ・コントローラ
  - CVIDEO/SD-DAC TVのアナログ・コンポジット出力
- オンチップの温度センサ、温度アラートも生成可能
- 汎用メモリ・コントローラ(GPMC)
- 拡張ダイレクト・メモリ・アクセス(EDMA)コントローラ
- 3ポート(外部2)のギガビット・イーサネット(GMAC)スイッチ
- コントローラ・エリア・ネットワーク(DCAN)モジュール
  - CAN 2.0Bプロトコル
- モジュラー・コントローラ・エリア・ネットワーク(MCAN)モジュール
  - CAN 2.0Bプロトコル
- 8つの32ビット汎用タイマ
- 3つの構成可能なUARTモジュール
- 4つのマルチチャネル・シリアル・ペリフェラル・インターフェイス(McSPI)
- クワッドSPIインターフェイス
- 2つのI<sup>2</sup>C (Inter-Integrated Circuit)ポート
- 3つのマルチチャネル・オーディオ・シリアル・ポート(McASP)モジュール
- マルチメディア・カード/セキュア・デジタル/セキュア・デジタル出力インターフェイス(MMC™/ SD®/SDIO)
- 最大126の汎用I/O (GPIO)ピン
- 電源、リセット、クロック管理
- CToolsテクノロジーによるオンチップ・デバッグ
- 車載用にAEC-Q100認定済み
- 15×15mm、0.65mmピッチ、367ピンPBGA (ABF)
- リアルタイム割り込み(RTI)モジュールのインスタンスが5つ内蔵され、ウォッチドッグ・タイマとして使用可能
- 8チャンネル、10ビットのADC
- PWMSS
- ビデオおよび画像処理のサポート
  - フルHDビデオ(1920×1080p、60fps)
  - ビデオ入力とビデオ出力
  - ビデオを使用しないときはGPIO
- ビデオ入力ポート(VIP)モジュール
  - 最大4つの多重化された入力ポートをサポート



## 1.2 アプリケーション

- デジタルおよびアナログ・ラジオ
- ハイブリッド・ラジオ
- DSPオーディオ・アンプ
- 車両コネクティビティ用コプロセッサ

## 1.3 概要

DRA78x プロセッサは、367 ボール、15×15mm、0.65mm ボール・ピッチ (信号には 0.8mm 間隔のルールを使用できます) で、Via Channel™ Array (VCA) テクノロジーのボール・グリッド・アレイ (FCBGA) パッケージで供給されます。

このアーキテクチャは、コスト効率が重要なソリューションにおける車載用コプロセッサ、ハイブリッドのラジオ、およびアンプの高性能の同時動作用に設計されており、DRA75x (「Jacinto 6 EP」および「Jacinto 6 Ex」)、DRA74x「Jacinto 6」、DRA72x「Jacinto 6 Eco」、およびDRA71x「Jacinto 6 Entry」ファミリのインフォテインメント・プロセッサからの完全な拡張性があります。

さらに、テキサス・インスツルメンツ (TI) は Arm および DSP 用に完全な開発ツールのセットを提供しており、C コンパイラのほか、デバッグ・インターフェイスによってソースコードの実行を見通すことができます。

DRA78x Jacinto 6 RSP (ラジオ・サウンド・プロセッサ) デバイス・ファミリは、AEC-Q100標準に従って認定済みです。

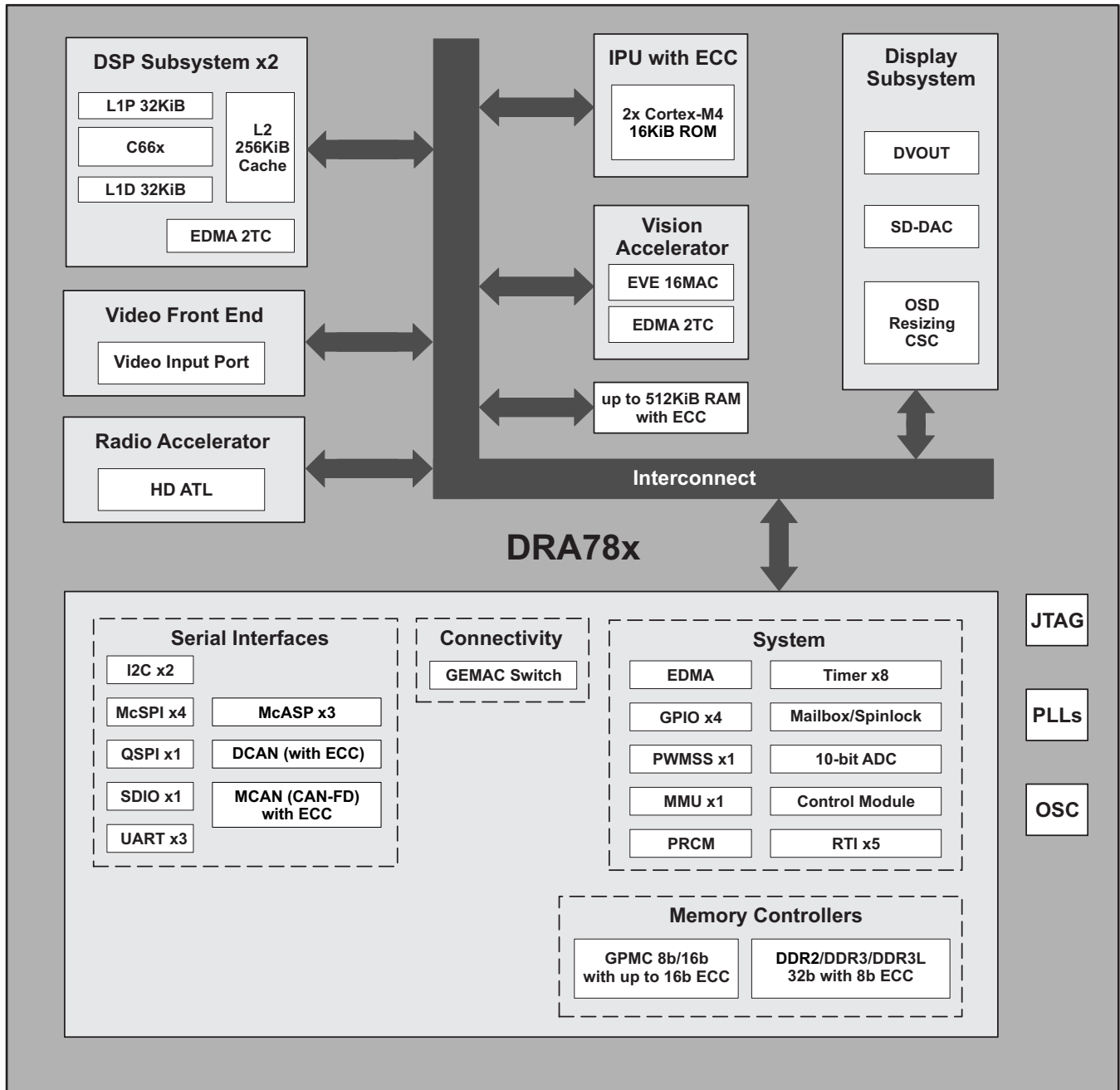
このデバイスは電源レール・マッピングが単純化されているため、PMICソリューションのコストを低減できます。

### 製品情報

| 型番     | パッケージ       | 本体サイズ         |
|--------|-------------|---------------|
| DRA780 | FCBGA (367) | 15.0mm×15.0mm |
| DRA781 | FCBGA (367) | 15.0mm×15.0mm |
| DRA782 | FCBGA (367) | 15.0mm×15.0mm |
| DRA783 | FCBGA (367) | 15.0mm×15.0mm |
| DRA784 | FCBGA (367) | 15.0mm×15.0mm |
| DRA785 | FCBGA (367) | 15.0mm×15.0mm |
| DRA786 | FCBGA (367) | 15.0mm×15.0mm |
| DRA787 | FCBGA (367) | 15.0mm×15.0mm |
| DRA788 | FCBGA (367) | 15.0mm×15.0mm |

## 1.4 機能ブロック図

スーパーセットの機能ブロック図を、図 1-1 に示します。



func\_spr968-001

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図 1-1. DRA78xのブロック図

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## 2 改訂履歴

| 2018年9月19日発行分から2019年03月31日発行分への変更 (from F Revision (September 2018) to G Revision)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Page |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| <ul style="list-style-type: none"> <li>「製品情報」表を更新し、各デバイス用の行を追加 ..... <a href="#">1</a></li> <li>Added clarification notes regarding XTDA3SX part number to <a href="#">表 3-1, Device Comparison</a> ..... <a href="#">8</a></li> <li>Added Related Products section ..... <a href="#">9</a></li> <li>Removed Internal pulldown for OSC0 and OSC1 oscillators from <a href="#">表 4-1, Pin Attributes</a> ..... <a href="#">12</a></li> <li>Added clarification notes for EMU[1:0] connections in <a href="#">表 4-20, GPIOs Signal Descriptions</a> and <a href="#">表 4-23, Debug Signal Descriptions</a> ..... <a href="#">59</a></li> <li>Added clarification note regarding TSHUT feature in <a href="#">Section 5.4, Recommended Operating Conditions</a> ..... <a href="#">81</a></li> <li>Updated VD_CORE max value in <a href="#">表 5-3, Voltage Domains Operating Performance Points</a> ..... <a href="#">81</a></li> <li>Updated FUNC_32K_CLK source name in <a href="#">表 5-5, Maximum Supported Frequency</a> ..... <a href="#">82</a></li> <li>Updated paragraphs as per datasheet standard in <a href="#">Section 5.9.1.1.2, 1.8 V and 3.3 V Signal Transition Rates</a> and <a href="#">5.9.5, Recommended Clock and Control Signal Transition Behavior</a> ..... <a href="#">99</a></li> <li>Added missing "hsync" and "fld" signals to <a href="#">表 5-28, VIN1 IOSETs</a> ..... <a href="#">118</a></li> <li>Fixed muxmode value for vin2a_hsync0 in <a href="#">表 5-29, VIN2 IOSETs</a> ..... <a href="#">119</a></li> <li>Updated <a href="#">8.1, Device Nomenclature</a>, <a href="#">8.2 Tools and Software</a>, and <a href="#">8.3, Documentation Support</a>; Removed section 9.3.1 FCC Warning, section 9.3.2 Information About Cautions and Warnings, and section 9.4 Receiving Notification of Documentation Updates; Fixed Arm trademark in section 9.7 Trademarks ..... <a href="#">274</a></li> <li>Updated note for cosmetic marks on package ..... <a href="#">274</a></li> <li>Added clarification notes regarding XTDA3SX part number in <a href="#">表 8-1, Nomenclature Description</a> ..... <a href="#">274</a></li> <li>Updated <a href="#">9, Mechanical, Packaging, and Orderable Information</a> as per datasheet standard ..... <a href="#">279</a></li> </ul> |      |

### 3 Device Comparison

表 3-1 shows a comparison between devices, highlighting the differences.

**表 3-1. Device Comparison<sup>(4)</sup>**

| FEATURES                                                                              |                               | DEVICE     |            |            |            |            |            |            |            |            |
|---------------------------------------------------------------------------------------|-------------------------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|
|                                                                                       |                               | DRA780     | DRA781     | DRA784     | DRA782     | DRA783     | DRA785     | DRA786     | DRA787     | DRA788     |
| Features                                                                              |                               |            |            |            |            |            |            |            |            |            |
| CTRL_WKUP_STD_FUSE_DIE_ID_2 [31:24] Base PN register bitfield value <sup>(3)(4)</sup> |                               | 112 (0x70) | 113 (0x71) | 116 (0x74) | 114 (0x72) | 115 (0x73) | 117 (0x75) | 118 (0x76) | 119 (0x77) | 120 (0x78) |
| Processors/ Accelerators                                                              |                               |            |            |            |            |            |            |            |            |            |
| Speed Grades                                                                          |                               | D          | R          | S          | D          | R          | S          | D          | R          | S          |
| C66x VLIW DSP                                                                         | DSP1                          | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        |
|                                                                                       | DSP2                          | No         | No         | No         | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        |
| Display Subsystem                                                                     | VOUT1                         | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        |
|                                                                                       | SD_DAC                        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        |
| Embedded Vision Engine (EVE)                                                          | EVE1                          | No         | No         | No         | No         | No         | No         | Yes        | Yes        | Yes        |
| Dual Arm Cortex-M4 Image Processing Unit (IPU)                                        | IPU1                          | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        |
| Imaging Subsystem Processor (ISS) with MIPI CSI-2 and CPI ports                       | ISP                           | No         | No         | No         | No         | No         | No         | No         | No         | No         |
|                                                                                       | WDR & Mesh LDC <sup>(1)</sup> | No         | No         | No         | No         | No         | No         | No         | No         | No         |
|                                                                                       | CAL_A                         | No         | No         | No         | No         | No         | No         | No         | No         | No         |
|                                                                                       | CAL_B                         | No         | No         | No         | No         | No         | No         | No         | No         | No         |
|                                                                                       | LVDS-RX                       | No         | No         | No         | No         | No         | No         | No         | No         | No         |
|                                                                                       | CPI                           | No         | No         | No         | No         | No         | No         | No         | No         | No         |
| Video Input Port (VIP)                                                                | VIP1                          | vin1a      | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        |
|                                                                                       |                               | vin1b      | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        |
|                                                                                       |                               | vin2a      | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        |
|                                                                                       |                               | vin2b      | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        |
| Program/Data Storage                                                                  |                               |            |            |            |            |            |            |            |            |            |
| On-Chip Shared Memory (RAM)                                                           | OCMC_RAM1                     | 512kB      | 512kB      | 512kB      | 512kB      | 512kB      | 512kB      | 512kB      | 512kB      | 512kB      |
| General-Purpose Memory Controller (GPMC)                                              | GPMC                          | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        |
| DDR2/DDR3/DDR3L Memory Controller                                                     | EMIF1 (optional with SECCDED) | up to 2GB  | up to 2GB  | up to 2GB  | up to 2GB  | up to 2GB  | up to 2GB  | up to 2GB  | up to 2GB  | up to 2GB  |
| Radio Support                                                                         |                               |            |            |            |            |            |            |            |            |            |
| Audio Tracking Logic (ATL)                                                            | ATL                           | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        |
| Peripherals                                                                           |                               |            |            |            |            |            |            |            |            |            |
| Controller Area Network Interface (CAN)                                               | DCAN1                         | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        |

表 3-1. Device Comparison<sup>(4)</sup> (continued)

| FEATURES                                                                           |             | DEVICE            |                   |                   |                   |                   |                   |                   |                   |                   |
|------------------------------------------------------------------------------------|-------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
|                                                                                    |             | DRA780            | DRA781            | DRA784            | DRA782            | DRA783            | DRA785            | DRA786            | DRA787            | DRA788            |
|                                                                                    | MCAN        | FD <sup>(2)</sup> | FD <sup>(2)</sup> | FD <sup>(2)</sup> | FD <sup>(2)</sup> | FD <sup>(2)</sup> | FD <sup>(2)</sup> | FD <sup>(2)</sup> | FD <sup>(2)</sup> | FD <sup>(2)</sup> |
| Enhanced DMA (EDMA)                                                                | EDMA        | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               |
| Embedded 8 channel ADC                                                             | ADC         | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               |
| Ethernet Subsystem (Ethernet SS)                                                   | GMAC_SW[0]  | RGMII Only        | RGMII Only        | RGMII Only        | RGMII Only        | RGMII Only        | RGMII Only        | RGMII Only        | RGMII Only        | RGMII Only        |
|                                                                                    | GMAC_SW[1]  | RGMII Only        | RGMII Only        | RGMII Only        | RGMII Only        | RGMII Only        | RGMII Only        | RGMII Only        | RGMII Only        | RGMII Only        |
| General-Purpose IO (GPIO)                                                          | GPIO        | Up to 126         | Up to 126         | Up to 126         | Up to 126         | Up to 126         | Up to 126         | Up to 126         | Up to 126         | Up to 126         |
| Inter-Integrated Circuit Interface (I2C)                                           | I2C         | 2                 | 2                 | 2                 | 2                 | 2                 | 2                 | 2                 | 2                 | 2                 |
| System Mailbox Module                                                              | MAILBOX     | 2                 | 2                 | 2                 | 2                 | 2                 | 2                 | 2                 | 2                 | 2                 |
| Multichannel Audio Serial Port (McASP)                                             | McASP1      | 16 serializers    | 16 serializers    | 16 serializers    | 16 serializers    | 16 serializers    | 16 serializers    | 16 serializers    | 16 serializers    | 16 serializers    |
|                                                                                    | McASP2      | 6 serializers     | 6 serializers     | 6 serializers     | 6 serializers     | 6 serializers     | 6 serializers     | 6 serializers     | 6 serializers     | 6 serializers     |
|                                                                                    | McASP3      | 6 serializers     | 6 serializers     | 6 serializers     | 6 serializers     | 6 serializers     | 6 serializers     | 6 serializers     | 6 serializers     | 6 serializers     |
| MultiMedia Card/Secure Digital/Secure Digital Input Output Interface (MMC/SD/SDIO) | MMC         | 1x SDIO 4b        | 1x SDIO 4b        | 1x SDIO 4b        | 1x SDIO 4b        | 1x SDIO 4b        | 1x SDIO 4b        | 1x SDIO 4b        | 1x SDIO 4b        | 1x SDIO 4b        |
| Multichannel Serial Peripheral Interface (McSPI)                                   | McSPI       | 4                 | 4                 | 4                 | 4                 | 4                 | 4                 | 4                 | 4                 | 4                 |
| Quad SPI ( QSPI™)                                                                  | QSPI        | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               |
| Spinlock Module                                                                    | SPINLOCK    | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               |
| Timers, General-Purpose                                                            | TIMER       | 8                 | 8                 | 8                 | 8                 | 8                 | 8                 | 8                 | 8                 | 8                 |
| Dual Clock Comparators (DCC)                                                       | DCC         | No                | No                | No                | No                | No                | No                | No                | No                | No                |
| Pulse-Width Modulation Subsystem (PWMSS)                                           | PWMSS1      | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               | Yes               |
| Universal Asynchronous Receiver/Transmitter (UART)                                 | UART        | 3                 | 3                 | 3                 | 3                 | 3                 | 3                 | 3                 | 3                 | 3                 |
| Memory Cyclic Redundancy Check (CRC)                                               | CRC         | No                | No                | No                | No                | No                | No                | No                | No                | No                |
| TESOC (LBIST/PBIST)                                                                | LBIST/PBIST | No                | No                | No                | No                | No                | No                | No                | No                | No                |
| Error Signaling Module (ESM)                                                       | ESM         | No                | No                | No                | No                | No                | No                | No                | No                | No                |
| Real Time Interrupt (RTI)                                                          | RTI         | 5                 | 5                 | 5                 | 5                 | 5                 | 5                 | 5                 | 5                 | 5                 |

(1) Wide Dynamic Range and Lens Distortion Correction.

(2) MCAN with available FD (Flexible Data Rate) functionality. Devices that show MCAN = Yes do not support the Flexible Data Rate (FD) feature.

(3) For more details about the CTRL\_WKUP\_STD\_FUSE\_DIE\_ID\_2 register and Base PN bitfield, see the [DRA78x SoC for Automotive Infotainment Silicon Revision 2.0](#).

(4) XTDA3SX is the base part number for the superset device. Software should constrain the features used to match the intended production device. The Base PN register bitfield value is 0x98.

### 3.1 Related Products

**Companion Products for DRA78x** Review products that are frequently purchased or used in conjunction with this product.

**Reference Designs for DRA78x** TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs and design files to speed your time to market. Search and download designs at [ti.com/tidesigns](https://www.ti.com/tidesigns).

## 4 Terminal Configuration and Functions

### 4.1 Pin Diagram

图 4-1 shows the ball locations for the 367 plastic ball grid array (PBGA) package and are used in conjunction with 表 4-1 through 表 4-28 to locate signal names and ball grid numbers.

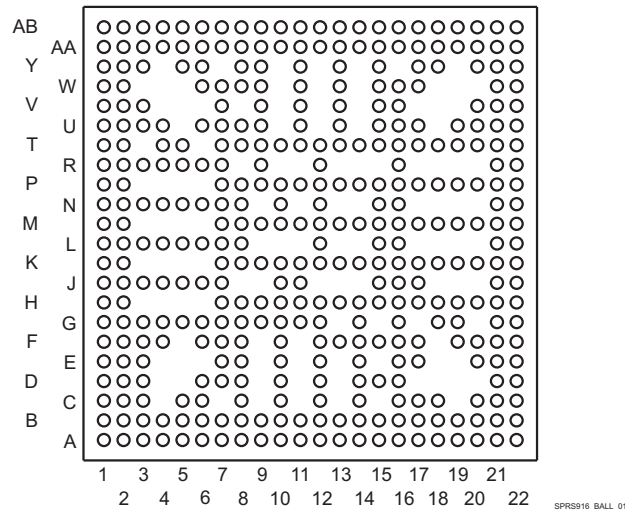


图 4-1. ABF FCBGA-N367 Package (Bottom View)

注: The following bottom balls are not connected: C4 / C7 / C9 / C11 / C13 / C15 / C19 / D4 / D5 / D9 / D11 / D13 / D17 / D18 / D19 / D20 / E4 / E5 / E6 / E9 / E11 / E13 / E15 / E18 / E19 / F5 / F9 / F11 / F18 / G13 / G15 / G17 / G20 / H3 / H4 / H5 / H6 / J8 / J9 / J12 / J13 / J14 / J18 / J19 / J20 / K3 / K4 / K5 / K6 / L9 / L10 / L11 / L13 / L14 / L17 / L18 / L19 / L20 / M3 / M4 / M5 / M6 / N9 / N11 / N13 / N14 / N17 / N18 / N19 / N20 / P3 / P4 / P5 / P6 / R8 / R10 / R11 / R13 / R14 / R15 / R17 / R18 / R19 / R20 / T3 / T6 / U5 / U10 / U12 / U14 / U18 / V4 / V5 / V6 / V8 / V10 / V12 / V14 / V17 / V18 / V19 / W3 / W4 / W5 / W10 / W12 / W14 / W18 / W19 / W20 / Y4 / Y7 / Y10 / Y12 / Y14 / Y16 / Y19.

These balls do not exist on the package.

### 4.2 Pin Attributes

表 4-1 describes the terminal characteristics and the signals multiplexed on each ball. The following list describes the table column headers:

1. **BALL NUMBER:** Ball number(s) on the bottom side associated with each signal on the bottom.
2. **BALL NAME:** Mechanical name from package device (name is taken from muxmode 0).
3. **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).

注: 表 4-1 does not take into account the subsystem multiplexing signals. Subsystem multiplexing signals are described in 4.3, *Signal Descriptions*.

注: In the Driver off mode, the buffer is configured in high-impedance.

4. **MUXMODE:** Multiplexing mode number:

- a. MUXMODE 0 is the primary mode; this means that when MUXMODE=0 is set, the function mapped on the pin corresponds to the name of the pin. The primary muxmode is not necessarily

the default muxmode.

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注: The default mode is the mode at the release of the reset; also see the RESET REL. MUXMODE column.

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- b. MUXMODE 1 through 15 are possible muxmodes for alternate functions. On each pin, some muxmodes are effectively used for alternate functions, while some muxmodes are not used. Only MUXMODE values which correspond to defined functions should be used.
    - c. An empty box means Not Applicable.
  5. **TYPE:** Signal type and direction:
    - I = Input
    - O = Output
    - IO = Input or Output
    - D = Open drain
    - DS = Differential Signaling
    - A = Analog
    - PWR = Power
    - GND = Ground
    - CAP = LDO Capacitor
  6. **BALL RESET STATE:** The state of the terminal at power-on reset:
    - drive 0 (OFF): The buffer drives  $V_{OL}$  (pulldown or pullup resistor not activated).
    - drive 1 (OFF): The buffer drives  $V_{OH}$  (pulldown or pullup resistor not activated).
    - OFF: High-impedance
    - PD: High-impedance with an active pulldown resistor
    - PU: High-impedance with an active pullup resistor
    - An empty box means Not Applicable
  7. **BALL RESET REL. STATE:** The state of the terminal at the deactivation of the rstoutn signal (also mapped to the PRCM SYS\_WARM\_OUT\_RST signal).
    - drive 0 (OFF): The buffer drives  $V_{OL}$  (pulldown or pullup resistor not activated).
    - drive clk (OFF): The buffer drives a toggling clock (pulldown or pullup resistor not activated).
    - drive 1 (OFF): The buffer drives  $V_{OH}$  (pulldown or pullup resistor not activated).
    - OFF: High-impedance
    - PD: High-impedance with an active pulldown resistor
    - PU: High-impedance with an active pullup resistor
    - An empty box means Not Applicable
- 
- 注: For more information on the CORE\_PWRON\_RET\_RST reset signal and its reset sources, see the Power, Reset, and Clock Management / Reset Management Functional Description section of the Device TRM.
- 
8. **BALL RESET REL. MUXMODE:** This muxmode is automatically configured at the release of the rstoutn signal (also mapped to the PRCM SYS\_WARM\_OUT\_RST signal).  
An empty box means Not Applicable.
  9. **IO VOLTAGE VALUE:** This column describes the IO voltage value (the corresponding power supply).  
An empty box means Not Applicable.
  10. **POWER:** The voltage supply that powers the terminal IO buffers.  
An empty box means Not Applicable.
  11. **HYS:** Indicates if the input buffer is with hysteresis:
    - Yes: With hysteresis
    - No: Without hysteresis

- An empty box: Not Applicable

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注: For more information, see the hysteresis values in [5.7, DC Electrical Characteristics](#).

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12. **BUFFER TYPE:** Drive strength of the associated output buffer.

An empty box means Not Applicable.

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注: For programmable buffer strength:

- The default value is given in [表 4-1](#).
  - A note describes all possible values according to the selected muxmode.
- 

13. **PULL UP / DOWN TYPE:** Denotes the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.

- PU: Internal pullup
- PD: Internal pulldown
- PU/PD: Internal pullup and pulldown
- PUx/PDy: Programmable internal pullup and pulldown
- PDy: Programmable internal pulldown
- An empty box means No pull

14. **DSIS:** The deselected input state (DSIS) indicates the state driven on the peripheral input (logic "0" or logic "1") when the peripheral pin function is not selected by any of the CTRL\_CORE\_PADx registers.

- 0: Logic 0 driven on the peripheral's input signal port.
- 1: Logic 1 driven on the peripheral's input signal port.
- blank: Pin state driven on the peripheral's input signal port.

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注: Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration (Hi-Z mode is not an input signal).

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注: When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This should be avoided.

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表 4-1. Pin Attributes<sup>(1)</sup>

| BALL NUMBER<br>[1] | BALL NAME [2]     | SIGNAL NAME [3]   | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]     | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|-------------------|-------------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|-------------------------|------------------------------|-----------|
| M19                | adc_in0           | adc_in0           | 0              | A        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_adc   |          | GPADC                   |                              |           |
| M20                | adc_in1           | adc_in1           | 0              | A        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_adc   |          | GPADC                   |                              |           |
| M21                | adc_in2           | adc_in2           | 0              | A        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_adc   |          | GPADC                   |                              |           |
| M22                | adc_in3           | adc_in3           | 0              | A        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_adc   |          | GPADC                   |                              |           |
| N22                | adc_in4           | adc_in4           | 0              | A        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_adc   |          | GPADC                   |                              |           |
| N21                | adc_in5           | adc_in5           | 0              | A        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_adc   |          | GPADC                   |                              |           |
| P19                | adc_in6           | adc_in6           | 0              | A        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_adc   |          | GPADC                   |                              |           |
| P18                | adc_in7           | adc_in7           | 0              | A        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_adc   |          | GPADC                   |                              |           |
| P20                | adc_vrefp         | adc_vrefp         | 0              | A        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_adc   |          | GPADC                   |                              |           |
| N15                | cap_vddram_core1  | cap_vddram_core1  |                | CAP      |                            |                                 |                                      |                             |            |          |                         |                              |           |
| M15                | cap_vddram_core2  | cap_vddram_core2  |                | CAP      |                            |                                 |                                      |                             |            |          |                         |                              |           |
| M14                | cap_vddram_dspeve | cap_vddram_dspeve |                | CAP      |                            |                                 |                                      |                             |            |          |                         |                              |           |
| A11                | csi2_0_dx0        | csi2_0_dx0        | 0              | I        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_csi   | Yes      | LVC MOS<br>CSI2         | PU/PD                        |           |
| A12                | csi2_0_dx1        | csi2_0_dx1        | 0              | I        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_csi   | Yes      | LVC MOS<br>CSI2         | PU/PD                        |           |
| A13                | csi2_0_dx2        | csi2_0_dx2        | 0              | I        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_csi   | Yes      | LVC MOS<br>CSI2         | PU/PD                        |           |
| A15                | csi2_0_dx3        | csi2_0_dx3        | 0              | I        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_csi   | Yes      | LVC MOS<br>CSI2         | PU/PD                        |           |
| A16                | csi2_0_dx4        | csi2_0_dx4        | 0              | I        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_csi   | Yes      | LVC MOS<br>CSI2         | PU/PD                        |           |
| B11                | csi2_0_dy0        | csi2_0_dy0        | 0              | I        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_csi   | Yes      | LVC MOS<br>CSI2         | PU/PD                        |           |
| B12                | csi2_0_dy1        | csi2_0_dy1        | 0              | I        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_csi   | Yes      | LVC MOS<br>CSI2         | PU/PD                        |           |
| B13                | csi2_0_dy2        | csi2_0_dy2        | 0              | I        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_csi   | Yes      | LVC MOS<br>CSI2         | PU/PD                        |           |
| B15                | csi2_0_dy3        | csi2_0_dy3        | 0              | I        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_csi   | Yes      | LVC MOS<br>CSI2         | PU/PD                        |           |
| B16                | csi2_0_dy4        | csi2_0_dy4        | 0              | I        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_csi   | Yes      | LVC MOS<br>CSI2         | PU/PD                        |           |
| T18                | cvideo_rset       | cvideo_rset       | 0              | A        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_dac   |          | AVDAC                   |                              |           |
| T17                | cvideo_tvout      | cvideo_tvout      | 0              | A        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_dac   |          | AVDAC                   |                              |           |
| P17                | cvideo_vfb        | cvideo_vfb        | 0              | A        | OFF                        | OFF                             | 0                                    | 1.8                         | vdda_dac   |          | AVDAC                   |                              |           |
| N6                 | dcan1_rx          | dcan1_rx          | 0              | IO       | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVC MOS | PU/PD                        |           |
|                    |                   | gpio4_10          | 14             | IO       |                            |                                 |                                      |                             |            |          |                         |                              |           |
|                    |                   | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                         |                              |           |
| N5                 | dcan1_tx          | dcan1_tx          | 0              | IO       | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVC MOS | PU/PD                        |           |
|                    |                   | gpio4_9           | 14             | IO       |                            |                                 |                                      |                             |            |          |                         |                              |           |
|                    |                   | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                         |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12] | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|-----------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|---------------------|------------------------------|-----------|
| F2                 | ddr1_casn     | ddr1_casn       | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr2  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| G1                 | ddr1_ck       | ddr1_ck         | 0              | O        | PD                         | drive clk<br>(OFF)              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr2  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AB13               | ddr1_dqm_ecc  | ddr1_dqm_ecc    | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AB10               | ddr1_dqsn_ecc | ddr1_dqsn_ecc   | 0              | IO       | PU                         | PU                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AA10               | ddr1_dqs_ecc  | ddr1_dqs_ecc    | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| G2                 | ddr1_nck      | ddr1_nck        | 0              | O        | PD                         | drive clk<br>(OFF)              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr2  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| F1                 | ddr1_rasn     | ddr1_rasn       | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr2  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| N1                 | ddr1_rst      | ddr1_rst        | 0              | O        | PD                         | drive 0 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| E3                 | ddr1_wen      | ddr1_wen        | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr2  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| U4                 | ddr1_a0       | ddr1_a0         | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| C1                 | ddr1_a1       | ddr1_a1         | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr2  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| D3                 | ddr1_a2       | ddr1_a2         | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr2  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| R4                 | ddr1_a3       | ddr1_a3         | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| T4                 | ddr1_a4       | ddr1_a4         | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| N3                 | ddr1_a5       | ddr1_a5         | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| T2                 | ddr1_a6       | ddr1_a6         | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| N2                 | ddr1_a7       | ddr1_a7         | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| T1                 | ddr1_a8       | ddr1_a8         | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| U1                 | ddr1_a9       | ddr1_a9         | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| D1                 | ddr1_a10      | ddr1_a10        | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr2  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| R3                 | ddr1_a11      | ddr1_a11        | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| U2                 | ddr1_a12      | ddr1_a12        | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| C3                 | ddr1_a13      | ddr1_a13        | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr2  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |

**表 4-1. Pin Attributes<sup>(1)</sup> (continued)**

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12] | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|-----------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|---------------------|------------------------------|-----------|
| R2                 | ddr1_a14      | ddr1_a14        | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| V1                 | ddr1_a15      | ddr1_a15        | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| B3                 | ddr1_ba0      | ddr1_ba0        | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr2  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| A3                 | ddr1_ba1      | ddr1_ba1        | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr2  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| D2                 | ddr1_ba2      | ddr1_ba2        | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr2  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| F3                 | ddr1_cke0     | ddr1_cke0       | 0              | O        | PD                         | drive 0 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr2  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| B2                 | ddr1_csn0     | ddr1_csn0       | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr2  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AA6                | ddr1_d0       | ddr1_d0         | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AA8                | ddr1_d1       | ddr1_d1         | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| Y8                 | ddr1_d2       | ddr1_d2         | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AA7                | ddr1_d3       | ddr1_d3         | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AB4                | ddr1_d4       | ddr1_d4         | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| Y5                 | ddr1_d5       | ddr1_d5         | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AA4                | ddr1_d6       | ddr1_d6         | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| Y6                 | ddr1_d7       | ddr1_d7         | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AA18               | ddr1_d8       | ddr1_d8         | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| Y21                | ddr1_d9       | ddr1_d9         | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AA21               | ddr1_d10      | ddr1_d10        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| Y22                | ddr1_d11      | ddr1_d11        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AA19               | ddr1_d12      | ddr1_d12        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AB20               | ddr1_d13      | ddr1_d13        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| Y17                | ddr1_d14      | ddr1_d14        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AB18               | ddr1_d15      | ddr1_d15        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12] | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|-----------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|---------------------|------------------------------|-----------|
| AA3                | ddr1_d16      | ddr1_d16        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AA2                | ddr1_d17      | ddr1_d17        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| Y3                 | ddr1_d18      | ddr1_d18        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| V2                 | ddr1_d19      | ddr1_d19        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| U3                 | ddr1_d20      | ddr1_d20        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| V3                 | ddr1_d21      | ddr1_d21        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| Y2                 | ddr1_d22      | ddr1_d22        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| Y1                 | ddr1_d23      | ddr1_d23        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| U21                | ddr1_d24      | ddr1_d24        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| T20                | ddr1_d25      | ddr1_d25        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| R21                | ddr1_d26      | ddr1_d26        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| U20                | ddr1_d27      | ddr1_d27        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| R22                | ddr1_d28      | ddr1_d28        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| V20                | ddr1_d29      | ddr1_d29        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| W22                | ddr1_d30      | ddr1_d30        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| U22                | ddr1_d31      | ddr1_d31        | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AB8                | ddr1_dqm0     | ddr1_dqm0       | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| Y18                | ddr1_dqm1     | ddr1_dqm1       | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AB3                | ddr1_dqm2     | ddr1_dqm2       | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| W21                | ddr1_dqm3     | ddr1_dqm3       | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AA5                | ddr1_dqs0     | ddr1_dqs0       | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| AA20               | ddr1_dqs1     | ddr1_dqs1       | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |
| W1                 | ddr1_dqs2     | ddr1_dqs2       | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR      | PuX/PDy                      |           |

**表 4-1. Pin Attributes<sup>(1)</sup> (continued)**

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]     | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|-----------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|-------------------------|------------------------------|-----------|
| T21                | ddr1_dqs3     | ddr1_dqs3       | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR          | PuX/PDy                      |           |
| AB5                | ddr1_dqsn0    | ddr1_dqsn0      | 0              | IO       | PU                         | PU                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR          | PuX/PDy                      |           |
| Y20                | ddr1_dqsn1    | ddr1_dqsn1      | 0              | IO       | PU                         | PU                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR          | PuX/PDy                      |           |
| W2                 | ddr1_dqsn2    | ddr1_dqsn2      | 0              | IO       | PU                         | PU                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR          | PuX/PDy                      |           |
| T22                | ddr1_dqsn3    | ddr1_dqsn3      | 0              | IO       | PU                         | PU                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr3  |          | LVC MOS<br>DDR          | PuX/PDy                      |           |
| Y11                | ddr1_ecc_d0   | ddr1_ecc_d0     | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR          | PuX/PDy                      |           |
| AA12               | ddr1_ecc_d1   | ddr1_ecc_d1     | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR          | PuX/PDy                      |           |
| AA11               | ddr1_ecc_d2   | ddr1_ecc_d2     | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR          | PuX/PDy                      |           |
| Y9                 | ddr1_ecc_d3   | ddr1_ecc_d3     | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR          | PuX/PDy                      |           |
| AA13               | ddr1_ecc_d4   | ddr1_ecc_d4     | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR          | PuX/PDy                      |           |
| AB11               | ddr1_ecc_d5   | ddr1_ecc_d5     | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR          | PuX/PDy                      |           |
| AA9                | ddr1_ecc_d6   | ddr1_ecc_d6     | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR          | PuX/PDy                      |           |
| AB9                | ddr1_ecc_d7   | ddr1_ecc_d7     | 0              | IO       | PD                         | PD                              | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR          | PuX/PDy                      |           |
| P2                 | ddr1_odt0     | ddr1_odt0       | 0              | O        | PD                         | drive 0 (OFF)                   | 0                                    | 1.2/1.35/1.5/1.8            | vdds_ddr1  |          | LVC MOS<br>DDR          | PuX/PDy                      |           |
| H1                 | emu0          | emu0            | 0              | IO       | PU                         | PU                              | 0                                    | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVC MOS | PU/PD                        |           |
|                    |               | gpio4_28        | 14             | IO       |                            |                                 |                                      |                             |            |          |                         |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                         |                              |           |
| H2                 | emu1          | emu1            | 0              | IO       | PU                         | PU                              | 0                                    | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVC MOS | PU/PD                        |           |
|                    |               | gpio4_29        | 14             | IO       |                            |                                 |                                      |                             |            |          |                         |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                         |                              |           |
| E8                 | gpmc_ad0      | gpmc_ad0        | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVC MOS | PU/PD                        | 0         |
|                    |               | rgmii1_rxd2     | 1              | I        |                            |                                 |                                      |                             |            |          |                         |                              | 0         |
|                    |               | gpio1_14        | 14             | IO       |                            |                                 |                                      |                             |            |          |                         |                              |           |
|                    |               | sysboot0        | 15             | I        |                            |                                 |                                      |                             |            |          |                         |                              |           |
| A7                 | gpmc_ad1      | gpmc_ad1        | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVC MOS | PU/PD                        | 0         |
|                    |               | rgmii1_rxd1     | 1              | I        |                            |                                 |                                      |                             |            |          |                         |                              | 0         |
|                    |               | gpio1_15        | 14             | IO       |                            |                                 |                                      |                             |            |          |                         |                              |           |
|                    |               | sysboot1        | 15             | I        |                            |                                 |                                      |                             |            |          |                         |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3]             | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|-----------------------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| F8                 | gpmc_ad2      | gpmc_ad2                    | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | rgmii1_rxd0                 | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio1_16                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sysboot2                    | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| B7                 | gpmc_ad3      | gpmc_ad3                    | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | qspi1_rtclk                 | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio1_17                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sysboot3                    | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| A6                 | gpmc_ad4      | gpmc_ad4                    | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cam_strobe                  | 1              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio1_18                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sysboot4                    | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| F7                 | gpmc_ad5      | gpmc_ad5                    | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | uart2_txd                   | 2              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | timer6                      | 3              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | spi3_d1                     | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio1_19                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sysboot5<br>mcasp2_aclck    | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| E7                 | gpmc_ad6      | gpmc_ad6                    | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | uart2_rxd                   | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | timer5                      | 3              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | spi3_d0                     | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio1_20                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sysboot6<br>mcasp2_fsx      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| C6                 | gpmc_ad7      | gpmc_ad7                    | 0              | IO       | OFF                        | OFF                             | 0                                    | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cam_shutter                 | 1              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | timer4                      | 3              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | spi3_sclk                   | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio1_21                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp2_ahclkx | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| B6                 | gpmc_ad8      | gpmc_ad8                    | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | timer7                      | 3              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | spi3_cs0                    | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio1_22                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sysboot8<br>mcasp2_aclkr    | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3]          | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|--------------------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| A5                 | gpmc_ad9      | gpmc_ad9                 | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | eCAP1_in_PWM1_out        | 3              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | spi3_cs1                 | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio1_23                 | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sysboot9<br>mcasp2_fsr   | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| D6                 | gpmc_ad10     | gpmc_ad10                | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | timer2                   | 3              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio1_24                 | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sysboot10<br>mcasp2_axr0 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| C5                 | gpmc_ad11     | gpmc_ad11                | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | timer3                   | 3              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio1_25                 | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sysboot11<br>mcasp2_axr1 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| B5                 | gpmc_ad12     | gpmc_ad12                | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | gpio1_26                 | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sysboot12<br>mcasp2_axr2 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| D7                 | gpmc_ad13     | gpmc_ad13                | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | rgmii1_rxc               | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio1_27                 | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sysboot13<br>mcasp2_axr3 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| B4                 | gpmc_ad14     | gpmc_ad14                | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | spi2_cs1                 | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio1_28                 | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sysboot14<br>mcasp2_axr4 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| A4                 | gpmc_ad15     | gpmc_ad15                | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | spi2_cs0                 | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio1_29                 | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sysboot15<br>mcasp2_axr5 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2]  | SIGNAL NAME [3]        | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|----------------|------------------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| F12                | gpmc_adv_n_ale | gpmc_adv_n_ale         | 0              | O        | PD                         | PD                              | 0                                    | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |                | rgmii1_txd2            | 1              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | ehrpwm1_tripzone_input | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |                | clkout1                | 5              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | dma_evt4               | 6              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | gpio1_3                | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| D12                | gpmc_ben0      | gpmc_ben0              | 0              | O        | PD                         | PD                              | 0                                    | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |                | rgmii1_txc1            | 1              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | ehrpwm1A               | 4              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | dma_evt2               | 6              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | gpio1_1                | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                |                        |                |          |                            |                                 |                                      |                             |            |          |                        |                              |           |
| E12                | gpmc_ben1      | gpmc_ben1              | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |                | rgmii1_txd3            | 1              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | ehrpwm1B               | 4              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | dma_evt3               | 6              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | gpio1_2                | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                |                        |                |          |                            |                                 |                                      |                             |            |          |                        |                              |           |
| C12                | gpmc_clk       | gpmc_clk               | 0              | IO       | PD                         | PD                              | 0                                    | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |                | rgmii1_txc             | 1              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | clkout0                | 5              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | dma_evt1               | 6              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | gpio1_0                | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                |                        |                |          |                            |                                 |                                      |                             |            |          |                        |                              |           |
| C10                | gpmc_cs0       | gpmc_cs0               | 0              | O        | PU                         | PU                              | 0                                    | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |                | rgmii1_rxctl           | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |                | gpio1_6                | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| E10                | gpmc_cs1       | gpmc_cs1               | 0              | O        | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |                | qspl1_cs0              | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |                | gpio1_7                | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| D10                | gpmc_cs2       | gpmc_cs2               | 0              | O        | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |                | qspl1_d3               | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |                | gpio1_8                | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |                | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]        | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|-----------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|----------------------------|------------------------------|-----------|
| A9                 | gpmc_cs3      | gpmc_cs3        | 0              | O        | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS     | PU/PD                        |           |
|                    |               | qspi1_d2        | 1              | IO       |                            |                                 |                                      |                             |            |          |                            |                              | 0         |
|                    |               | gpio1_9         | 14             | IO       |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                            |                              |           |
| B9                 | gpmc_cs4      | gpmc_cs4        | 0              | O        | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS     | PU/PD                        |           |
|                    |               | qspi1_d0        | 1              | IO       |                            |                                 |                                      |                             |            |          |                            |                              | 0         |
|                    |               | gpio1_10        | 14             | IO       |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                            |                              |           |
| F10                | gpmc_cs5      | gpmc_cs5        | 0              | O        | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS     | PU/PD                        |           |
|                    |               | qspi1_d1        | 1              | IO       |                            |                                 |                                      |                             |            |          |                            |                              | 0         |
|                    |               | gpio1_11        | 14             | IO       |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                            |                              |           |
| C8                 | gpmc_cs6      | gpmc_cs6        | 0              | O        | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS     | PU/PD                        |           |
|                    |               | qspi1_sclk      | 1              | O        |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | gpio1_12        | 14             | IO       |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                            |                              |           |
| A10                | gpmc_oen_ren  | gpmc_oen_ren    | 0              | O        | PD                         | PD                              | 0                                    | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS     | PU/PD                        |           |
|                    |               | rgmii1_txd1     | 1              | O        |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | ehrpwm1_synci   | 4              | I        |                            |                                 |                                      |                             |            |          |                            |                              | 0         |
|                    |               | clkout2         | 5              | O        |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | gpio1_4         | 14             | IO       |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                            |                              |           |
| D8                 | gpmc_wait0    | gpmc_wait0      | 0              | I        | PU                         | PU                              | 0                                    | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS     | PU/PD                        | 1         |
|                    |               | rgmii1_rxd3     | 1              | I        |                            |                                 |                                      |                             |            |          |                            |                              | 0         |
|                    |               | qspi1_rtclk     | 2              | I        |                            |                                 |                                      |                             |            |          |                            |                              | 0         |
|                    |               | dma_evt4        | 6              | I        |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | gpio1_13        | 14             | IO       |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                            |                              |           |
| B10                | gpmc_wen      | gpmc_wen        | 0              | O        | PD                         | PD                              | 0                                    | 1.8/3.3                     | vddshv2    | Yes      | Dual Voltage<br>LVCMOS     | PU/PD                        |           |
|                    |               | rgmii1_txd0     | 1              | O        |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | ehrpwm1_synco   | 4              | O        |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | gpio1_5         | 14             | IO       |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                            |                              |           |
| L3                 | i2c1_scl      | i2c1_scl        | 0              | IO       | OFF                        | OFF                             | 0                                    | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS I2C | PU                           |           |
| L4                 | i2c1_sda      | i2c1_sda        | 0              | IO       | OFF                        | OFF                             | 0                                    | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS I2C | PU                           |           |
| L6                 | i2c2_scl      | i2c2_scl        | 0              | IO       | OFF                        | OFF                             | 0                                    | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS I2C | PU                           |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]        | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|-----------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|----------------------------|------------------------------|-----------|
| L5                 | i2c2_sda      | i2c2_sda        | 0              | IO       | OFF                        | OFF                             | 0                                    | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS I2C | PU                           |           |
| W6                 | mcan_rx       | mcan_rx         | 0              | IO       | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS     | PU/PD                        | 1         |
|                    |               | cam_nreset      | 1              | IO       |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | vin2a_vsync0    | 2              | I        |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | spi1_cs3        | 3              | IO       |                            |                                 |                                      |                             |            |          |                            |                              | 1         |
|                    |               | uart3_txd       | 4              | O        |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | gpmc_cs7        | 5              | O        |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | vin1b_vsync1    | 7              | I        |                            |                                 |                                      |                             |            |          |                            |                              | 0         |
|                    |               | gpio4_12        | 14             | IO       |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                            |                              |           |
| W7                 | mcan_tx       | mcan_tx         | 0              | IO       | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS     | PU/PD                        | 1         |
|                    |               | vin2a_de0       | 1              | I        |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | vin2a_hsync0    | 2              | I        |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | spi1_cs2        | 3              | IO       |                            |                                 |                                      |                             |            |          |                            |                              | 1         |
|                    |               | uart3_rxd       | 4              | I        |                            |                                 |                                      |                             |            |          |                            |                              | 1         |
|                    |               | gpmc_wait1      | 6              | I        |                            |                                 |                                      |                             |            |          |                            |                              | 1         |
|                    |               | vin1b_hsync1    | 7              | I        |                            |                                 |                                      |                             |            |          |                            |                              | 0         |
|                    |               | vin1b_de1       | 8              | I        |                            |                                 |                                      |                             |            |          |                            |                              | 0         |
|                    |               | gpio4_11        | 14             | IO       |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                            |                              |           |
| B17                | mdio_d        | mdio_d          | 0              | IO       | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv4    | Yes      | Dual Voltage<br>LVCMOS     | PU/PD                        | 1         |
|                    |               | spi4_d0         | 4              | IO       |                            |                                 |                                      |                             |            |          |                            |                              | 0         |
|                    |               | gpio3_18        | 14             | IO       |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                            |                              |           |
| B19                | mdio_mclk     | mdio_mclk       | 0              | O        | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv4    | Yes      | Dual Voltage<br>LVCMOS     | PU/PD                        | 1         |
|                    |               | spi4_d1         | 4              | IO       |                            |                                 |                                      |                             |            |          |                            |                              | 0         |
|                    |               | gpio3_17        | 14             | IO       |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                            |                              |           |
| G5                 | nmin          | nmin            | 0              | I        | PU                         | PU                              | 0                                    | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS     | PU/PD                        | 1         |
| G3                 | porz          | porz            | 0              | I        | OFF                        | OFF                             | 0                                    | 1.8/3.3                     | vddshv1    | Yes      | IHHV1833                   | PU/PD                        |           |
| G4                 | resetn        | resetn          | 0              | I        | PU                         | PU                              | 0                                    | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS     | PU/PD                        |           |
| B18                | rgmii0_rxc    | rgmii0_rxc      | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv4    | Yes      | Dual Voltage<br>LVCMOS     | PU/PD                        | 0         |
|                    |               | cam_strobe      | 3              | O        |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | mmc_clk         | 5              | IO       |                            |                                 |                                      |                             |            |          |                            |                              | 1         |
|                    |               | gpio3_25        | 14             | IO       |                            |                                 |                                      |                             |            |          |                            |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                            |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|-----------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| C18                | rgmii0_rxtcl  | rgmii0_rxtcl    | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv4    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cam_shutter     | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | mmc_cmd         | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio3_26        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| C16                | rgmii0_txc    | rgmii0_txc      | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv4    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | cam_strobe      | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | spi4_sclk       | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | mmc_clk         | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio3_19        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
| C17                | rgmii0_txtcl  | rgmii0_txtcl    | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv4    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | cam_shutter     | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | spi4_cs0        | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | mmc_cmd         | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio3_20        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
| A20                | rgmii0_rxd0   | rgmii0_rxd0     | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv4    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | mmc_dat3        | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio3_30        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               |                 |                |          |                            |                                 |                                      |                             |            |          |                        |                              |           |
| C20                | rgmii0_rxd1   | rgmii0_rxd1     | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv4    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | mmc_dat2        | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio3_29        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| B20                | rgmii0_rxd2   | rgmii0_rxd2     | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv4    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | mmc_dat1        | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio3_28        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| A19                | rgmii0_rxd3   | rgmii0_rxd3     | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv4    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | mmc_dat0        | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio3_27        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| F17                | rgmii0_txd0   | rgmii0_txd0     | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv4    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mmc_dat3        | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio3_24        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3]        | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|------------------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| E17                | rgmii0_txd1   | rgmii0_txd1            | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv4    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mmc_dat2               | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio3_23               | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| D16                | rgmii0_txd2   | rgmii0_txd2            | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv4    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | eCAP1_in_PWM1_out      | 3              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | mmc_dat1               | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio3_22               | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| E16                | rgmii0_txd3   | rgmii0_txd3            | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv4    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mmc_dat0               | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio3_21               | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| F4                 | rstoutn       | rstoutn                | 0              | O        | PD                         | drive 1 (OFF)                   | 0                                    | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
| J6                 | rtck          | rtck                   | 0              | O        | PU                         | drive clk<br>(OFF)              | 0                                    | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | gpio4_27               | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| M2                 | spi1_sclk     | spi1_sclk              | 0              | IO       | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | uart3_rxd              | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio4_0                | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| L1                 | spi2_sclk     | spi2_sclk              | 0              | IO       | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | uart3_rxd              | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | ehrpwm1A               | 2              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | timer3                 | 3              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio4_5                | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| R6                 | spi1_cs0      | spi1_cs0               | 0              | IO       | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 1         |
|                    |               | uart3_txd              | 1              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio4_3                | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| R5                 | spi1_cs1      | spi1_cs1               | 0              | IO       | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 1         |
|                    |               | spi3_cs1               | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | timer6                 | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | ehrpwm1_tripzone_input | 7              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio4_4                | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3]   | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|-------------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| T5                 | spi1_d0       | spi1_d0           | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | uart3_rtsn        | 1              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio4_2           | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| U6                 | spi1_d1       | spi1_d1           | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | uart3_ctsn        | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio4_1           | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| L2                 | spi2_cs0      | spi2_cs0          | 0              | IO       | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 1         |
|                    |               | uart3_txd         | 1              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | ehrpwm1B          | 2              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | timer4            | 3              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio4_8           | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| R7                 | spi2_d0       | spi2_d0           | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | uart3_rtsn        | 1              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | timer1            | 3              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio4_7           | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sysboot7          | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| N4                 | spi2_d1       | spi2_d1           | 0              | IO       | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | uart3_ctsn        | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | timer5            | 3              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | eCAP1_in_PWM1_out | 7              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio4_6           | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| J2                 | tcclk         | tcclk             | 0              | I        | PU                         | PU                              | 0                                    | 1.8/3.3                     | vddshv1    | Yes      | IQ1833                 | PU/PD                        |           |
| J1                 | tdi           | tdi               | 0              | I        | PU                         | PU                              | 0                                    | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | gpio4_25          | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| J4                 | tdo           | tdo               | 0              | O        | PU                         | PU                              | 0                                    | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | gpio4_26          | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| J3                 | tms           | tms               | 0              | IO       | OFF                        | OFF                             | 0                                    | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
| J5                 | trstn         | trstn             | 0              | I        | PD                         | PD                              | 0                                    | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|-----------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| F14                | uart1_ctsn    | uart1_ctsn      | 0              | I        | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv3    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 1         |
|                    |               | xref_clk1       | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | uart3_rxd       | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpmc_a16        | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | spi4_sclk       | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | spi1_cs2        | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | timer3          | 6              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | ehrpwm1_syncl   | 7              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | clkout0         | 8              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | vin2a_hsync0    | 9              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpmc_a12        | 10             | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpmc_clk        | 11             | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | dcan1_tx        | 12             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio4_15        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| C14                | uart1_rtsn    | uart1_rtsn      | 0              | O        | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv3    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | uart3_txd       | 2              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpmc_a17        | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | spi4_cs0        | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | spi1_cs3        | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | timer4          | 6              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | ehrpwm1_synco   | 7              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | qspi1_rtclk     | 8              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2a_vsync0    | 9              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpmc_a13        | 10             | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | dcan1_rx        | 12             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio4_16        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               |                 |                |          |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               |                 |                |          |                            |                                 |                                      |                             |            |          |                        |                              |           |
| F13                | uart1_rxd     | uart1_rxd       | 0              | I        | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv3    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 1         |
|                    |               | spi4_d1         | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | qspi1_rtclk     | 5              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a12        | 10             | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | mcan_tx         | 12             | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio4_13        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3]   | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|-------------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| E14                | uart1_txd     | uart1_bxd         | 0              | O        | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv3    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | spi4_d0           | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a13          | 10             | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | mcan_rx           | 12             | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio4_14          | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| F15                | uart2_ctsn    | uart2_ctsn        | 0              | I        | OFF                        | OFF                             | 15                                   | 1.8/3.3                     | vddshv3    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 1         |
|                    |               | xref_clk1         | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpmc_a18          | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | spi3_sclk         | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | qspi1_cs1         | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | timer7            | 6              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | vin2a_hsync0      | 9              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpmc_clk          | 10             | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | mcan_tx           | 12             | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio4_19          | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| F16                | uart2_rtsn    | uart2_rtsn        | 0              | O        | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv3    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | eCAP1_in_PWM1_out | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a19          | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | spi3_cs0          | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | timer8            | 6              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | vin2a_vsync0      | 9              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | mcan_rx           | 12             | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio4_20          | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| D14                | uart2_rxd     | uart2_rxd         | 0              | I        | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv3    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 1         |
|                    |               | spi3_d1           | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | timer1            | 6              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | ehrpwm1A          | 7              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpmc_clk          | 10             | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a12          | 11             | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | dcan1_tx          | 12             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio4_17          | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1]                                                         | BALL NAME [2]  | SIGNAL NAME [3] | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|----------------------------------------------------------------------------|----------------|-----------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| D15                                                                        | uart2_txd      | uart2_txd       | 0              | O        | PU                         | PU                              | 15                                   | 1.8/3.3                     | vddshv3    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                                                                            |                | spi3_d0         | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                                                                            |                | timer2          | 6              | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                                                                            |                | ehrpwm1B        | 7              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                                                                            |                | gpmc_a13        | 11             | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                                                                            |                | dcan1_rx        | 12             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                                                                            |                | gpio4_18        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                                                                            |                | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| H12, H13, H7,<br>J10, J11, J15,<br>K12, L12, L15,<br>N12, N16, P10,<br>P14 | vdd            | vdd             |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| P22                                                                        | vdda_adc       | vdda_adc        |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| A14                                                                        | vdda_csi       | vdda_csi        |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| U19                                                                        | vdda_dac       | vdda_dac        |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| N8                                                                         | vdda_ddr_dsp   | vdda_ddr_dsp    |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| M8                                                                         | vdda_gmac_core | vdda_gmac_core  |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| E21                                                                        | vdda_osc       | vdda_osc        |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| H14                                                                        | vdda_per       | vdda_per        |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| G12, J7, L16,<br>P13, T11                                                  | vdds18v        | vdds18v         |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| P7, T9                                                                     | vdds18v_ddr1   | vdds18v_ddr1    |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| G7                                                                         | vdds18v_ddr2   | vdds18v_ddr2    |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| T16, V21                                                                   | vdds18v_ddr3   | vdds18v_ddr3    |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| K2, K7, L7, M7                                                             | vddshv1        | vddshv1         |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| B8, G11, G8, G9                                                            | vddshv2        | vddshv2         |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| G14                                                                        | vddshv3        | vddshv3         |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| A18, E20                                                                   | vddshv4        | vddshv4         |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| H17, J16, J21                                                              | vddshv5        | vddshv5         |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| AA16, T10, T12,<br>T13                                                     | vddshv6        | vddshv6         |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| AA1, AB6, R1, T7,<br>T8                                                    | vdds_ddr1      | vdds_ddr1       |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| C2, E2, G6                                                                 | vdds_ddr2      | vdds_ddr2       |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| AA22, AB19, T15                                                            | vdds_ddr3      | vdds_ddr3       |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |
| K8, L8, M9, P11,<br>P12, P8, P9                                            | vdd_dspeve     | vdd_dspeve      |                | PWR      |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3]            | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|----------------------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| F22                | vin1a_clk0    | vin1a_clk0                 | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_pclk                   | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | clkout0                    | 4              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio1_30                   | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp3_acltx | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| G18                | vin1a_d0      | vin1a_d0                   | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_data2                  | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio2_3                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp3_axr1  | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| G21                | vin1a_d1      | vin1a_d1                   | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_data3                  | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio2_4                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp3_axr2  | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| G22                | vin1a_d2      | vin1a_d2                   | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_data4                  | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio2_5                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp3_axr3  | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| H18                | vin1a_d3      | vin1a_d3                   | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_data5                  | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio2_6                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp3_axr4  | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| H20                | vin1a_d4      | vin1a_d4                   | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_data6                  | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio2_7                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp3_axr5  | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| H19                | vin1a_d5      | vin1a_d5                   | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_data7                  | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio2_8                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | xref_clk2<br>mcasp3_ahclkx | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| H22                | vin1a_d6      | vin1a_d6                   | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_data8                  | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio2_9                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp3_fsx   | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|-----------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| H21                | vin1a_d7      | vin1a_d7        | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_data9       | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio2_10        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| J17                | vin1a_d8      | vin1a_d8        | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_data10      | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin1b_d0        | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a8         | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sys_nirq2       | 7              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio2_11        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| K22                | vin1a_d9      | vin1a_d9        | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_data11      | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin1b_d1        | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a9         | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sys_nirq1       | 7              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio2_12        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| K21                | vin1a_d10     | vin1a_d10       | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_data12      | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin1b_d2        | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a10        | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sys_nirq2       | 7              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio2_13        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| K18                | vin1a_d11     | vin1a_d11       | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_data13      | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin1b_d3        | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a11        | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | sys_nirq1       | 7              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio2_14        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |

**表 4-1. Pin Attributes<sup>(1)</sup> (continued)**

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3]        | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|------------------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| K17                | vin1a_d12     | vin1a_d12              | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_data14             | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin1b_d4               | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a12               | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | dma_evt1               | 6              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio2_15               | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| K19                | vin1a_d13     | vin1a_d13              | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_wen                | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin1b_d5               | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a13               | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | dma_evt2               | 6              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio2_16               | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| K20                | vin1a_d14     | vin1a_d14              | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_fid                | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin1b_d6               | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a14               | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio2_17               | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| L21                | vin1a_d15     | vin1a_d15              | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_data15             | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin1b_d7               | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a15               | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio2_18               | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off             | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| F21                | vin1a_de0     | vin1a_de0              | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_hsync              | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin1b_clk1             | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | clkout1                | 4              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio1_31               | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>atl_clk1 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3]            | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|----------------------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| F20                | vin1a_fld0    | vin1a_fld0                 | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_vsync                  | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2b_clk1                 | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | clkout2                    | 4              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio2_0                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp3_aclkr | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| F19                | vin1a_hsync0  | vin1a_hsync0               | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_data0                  | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin1a_de0                  | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio2_1                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp3_fsr   | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| G19                | vin1a_vsync0  | vin1a_vsync0               | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        | 0         |
|                    |               | cpi_data1                  | 1              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio2_2                    | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp3_axr0  | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| L22                | vin2a_clk0    | vin2a_clk0                 | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | gpio2_19                   | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off                 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| M17                | vin2a_de0     | vin2a_de0                  | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | cam_strobe                 | 1              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | vin2b_hsync1               | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2b_de1                  | 5              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio4_21                   | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off                 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| M18                | vin2a_fld0    | vin2a_fld0                 | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv5    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | cam_shutter                | 1              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | vin2b_vsync1               | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpio4_22                   | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off                 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| AB17               | vout1_clk     | vout1_clk                  | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | vin1a_d12                  | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | clkout0                    | 4              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | vin2a_clk0                 | 9              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio2_20                   | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off                 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|-----------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| U17                | vout1_de      | vout1_de        | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_aclcx    | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin1a_d13       | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | clkout1         | 4              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio2_21        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| W17                | vout1_fld     | vout1_fld       | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_fsx      | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin1a_d14       | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | clkout2         | 4              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio2_22        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| AA17               | vout1_hsync   | vout1_hsync     | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_aclkr    | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin1a_d15       | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2a_de0       | 9              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio2_23        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| U16                | vout1_vsync   | vout1_vsync     | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_fsr      | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2a_fld0      | 9              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio2_24        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| W16                | vout1_d0      | vout1_d0        | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_axr0     | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | mmc_clk         | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio2_25        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| V16                | vout1_d1      | vout1_d1        | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_axr1     | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | mmc_cmd         | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio2_26        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|-----------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| U15                | vout1_d2      | vout1_d2        | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_axr2     | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | mcasp1_axr8     | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | mmc_dat0        | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio2_27        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| V15                | vout1_d3      | vout1_d3        | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_axr3     | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | mcasp1_axr9     | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | mmc_dat1        | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio2_28        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| Y15                | vout1_d4      | vout1_d4        | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_axr4     | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | mcasp1_axr10    | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | mmc_dat2        | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | gpio2_29        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| W15                | vout1_d5      | vout1_d5        | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_axr5     | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | mcasp1_axr11    | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | mmc_dat3        | 5              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 1         |
|                    |               | vin2a_clk0      | 9              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio2_30        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
| AA15               | vout1_d6      | vout1_d6        | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_axr6     | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | mcasp1_axr12    | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | emu2            | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | vin2a_de0       | 9              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio2_31        | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3]   | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|-------------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| AB15               | vout1_d7      | vout1_d7          | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_axr7       | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | eCAP1_in_PWM1_out | 3              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | mcasp1_axr13      | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | emu3              | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | vin2a_fld0        | 9              | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_0           | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| AA14               | vout1_d8      | vout1_d8          | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_axr8       | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2a_d0          | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a20          | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | emu4              | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_1           | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| AB14               | vout1_d9      | vout1_d9          | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_axr9       | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2a_d1          | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a21          | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | emu5              | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_2           | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| U13                | vout1_d10     | vout1_d10         | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_axr10      | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2a_d2          | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a22          | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | emu6              | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_3           | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| V13                | vout1_d11     | vout1_d11         | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_axr11      | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2a_d3          | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a23          | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | emu7              | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_4           | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off        | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3]             | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|-----------------------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| Y13                | vout1_d12     | vout1_d12                   | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_axr12                | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2a_d4                    | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a24                    | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | emu8                        | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_5                     | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp2_ahclkx | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| W13                | vout1_d13     | vout1_d13                   | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_axr13                | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2a_d5                    | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a25                    | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | emu9                        | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_6                     | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp2_aclkr  | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| U11                | vout1_d14     | vout1_d14                   | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_axr14                | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2a_d6                    | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a26                    | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | emu10                       | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_7                     | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp2_aclkx  | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| V11                | vout1_d15     | vout1_d15                   | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_axr15                | 1              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2a_d7                    | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a27                    | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | emu11                       | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_8                     | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp2_fsx    | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3]           | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|---------------------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| U9                 | vout1_d16     | vout1_d16                 | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | mcasp1_ahclkx             | 1              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | vin2a_d8                  | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a0                   | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | mcasp1_axr8               | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2b_d0                  | 5              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | emu12                     | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_9                   | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>atl_clk0    | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| W11                | vout1_d17     | vout1_d17                 | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | vin2a_d9                  | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a1                   | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | mcasp1_axr9               | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2b_d1                  | 5              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | emu13                     | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_10                  | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp2_fsr  | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               |                           |                |          |                            |                                 |                                      |                             |            |          |                        |                              |           |
| V9                 | vout1_d18     | vout1_d18                 | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | vin2a_d10                 | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a2                   | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | mcasp1_axr10              | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2b_d2                  | 5              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | emu14                     | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_11                  | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp2_axr0 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               |                           |                |          |                            |                                 |                                      |                             |            |          |                        |                              |           |
| W9                 | vout1_d19     | vout1_d19                 | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | vin2a_d11                 | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a3                   | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | mcasp1_axr11              | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2b_d3                  | 5              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | emu15                     | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_12                  | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp2_axr1 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               |                           |                |          |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3]           | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]    | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|--------------------|---------------|---------------------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|------------------------|------------------------------|-----------|
| U8                 | vout1_d20     | vout1_d20                 | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | vin2a_d12                 | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a4                   | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | mcasp1_axr12              | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2b_d4                  | 5              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | emu16                     | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_13                  | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp2_axr2 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| W8                 | vout1_d21     | vout1_d21                 | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | vin2a_d13                 | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a5                   | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | mcasp1_axr13              | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2b_d5                  | 5              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | emu17                     | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_14                  | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp2_axr3 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| U7                 | vout1_d22     | vout1_d22                 | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | vin2a_d14                 | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a6                   | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | mcasp1_axr14              | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2b_d6                  | 5              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | emu18                     | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_15                  | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp2_axr4 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |
| V7                 | vout1_d23     | vout1_d23                 | 0              | O        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv6    | Yes      | Dual Voltage<br>LVCMOS | PU/PD                        |           |
|                    |               | vin2a_d15                 | 2              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | gpmc_a7                   | 3              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | mcasp1_axr15              | 4              | IO       |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | vin2b_d7                  | 5              | I        |                            |                                 |                                      |                             |            |          |                        |                              | 0         |
|                    |               | emu19                     | 6              | O        |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | gpio3_16                  | 14             | IO       |                            |                                 |                                      |                             |            |          |                        |                              |           |
|                    |               | Driver off<br>mcasp2_axr5 | 15             | I        |                            |                                 |                                      |                             |            |          |                        |                              |           |

表 4-1. Pin Attributes<sup>(1)</sup> (continued)

| BALL NUMBER<br>[1]                                                                                                                                                                                                                                               | BALL NAME [2] | SIGNAL NAME [3] | MUXMODE<br>[4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET REL.<br>STATE [7] | BALL<br>RESET REL.<br>MUXMODE<br>[8] | I/O<br>VOLTAGE<br>VALUE [9] | POWER [10] | HYS [11] | BUFFER<br>TYPE [12]   | PULL<br>UP/DOWN<br>TYPE [13] | DSIS [14] |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-----------------|----------------|----------|----------------------------|---------------------------------|--------------------------------------|-----------------------------|------------|----------|-----------------------|------------------------------|-----------|
| A1, A17, A22, A8,<br>AB1, AB12, AB16,<br>AB2, AB21, AB22,<br>AB7, B22, E1,<br>G10, G16, H10,<br>H11, H15, H16,<br>H8, H9, J22, K1,<br>K10, K11, K13,<br>K14, K15, K16,<br>K9, M10, M11,<br>M12, M13, M16,<br>N10, N7, P1, P15,<br>P16, R12, R16,<br>R9, T14, V22 | vss           | vss             |                | GND      |                            |                                 |                                      |                             |            |          |                       |                              |           |
| P21                                                                                                                                                                                                                                                              | vssa_adc      | vssa_adc        |                | GND      |                            |                                 |                                      |                             |            |          |                       |                              |           |
| B14                                                                                                                                                                                                                                                              | vssa_csi      | vssa_csi        |                | GND      |                            |                                 |                                      |                             |            |          |                       |                              |           |
| T19                                                                                                                                                                                                                                                              | vssa_dac      | vssa_dac        |                | GND      |                            |                                 |                                      |                             |            |          |                       |                              |           |
| D21                                                                                                                                                                                                                                                              | vssa_osc0     | vssa_osc0       |                | GND      |                            |                                 |                                      |                             |            |          |                       |                              |           |
| C22                                                                                                                                                                                                                                                              | vssa_osc1     | vssa_osc1       |                | GND      |                            |                                 |                                      |                             |            |          |                       |                              |           |
| E22                                                                                                                                                                                                                                                              | xi_osc0       | xi_osc0         | 0              | I        |                            |                                 | 0                                    | 1.8                         | vdda_osc   | Yes      | LVCMS<br>Analog       |                              |           |
| B21                                                                                                                                                                                                                                                              | xi_osc1       | xi_osc1         | 0              | I        |                            |                                 | 0                                    | 1.8                         | vdda_osc   | Yes      | LVCMS<br>Analog       |                              |           |
| D22                                                                                                                                                                                                                                                              | xo_osc0       | xo_osc0         | 0              | O        |                            |                                 | 0                                    | 1.8                         | vdda_osc   | Yes      | LVCMS<br>Analog       |                              |           |
| C21                                                                                                                                                                                                                                                              | xo_osc1       | xo_osc1         | 0              | O        |                            |                                 | 0                                    | 1.8                         | vdda_osc   | Yes      | LVCMS<br>Analog       |                              |           |
| M1                                                                                                                                                                                                                                                               | xref_clk0     | xref_clk0       | 0              | I        | PD                         | PD                              | 15                                   | 1.8/3.3                     | vddshv1    | Yes      | Dual Voltage<br>LVCMS | PU/PD                        |           |
|                                                                                                                                                                                                                                                                  |               | clkout0         | 1              | O        |                            |                                 |                                      |                             |            |          |                       |                              |           |
|                                                                                                                                                                                                                                                                  |               | spi3_cs0        | 4              | IO       |                            |                                 |                                      |                             |            |          |                       |                              | 1         |
|                                                                                                                                                                                                                                                                  |               | spi2_cs1        | 5              | IO       |                            |                                 |                                      |                             |            |          |                       |                              | 1         |
|                                                                                                                                                                                                                                                                  |               | spi1_cs0        | 6              | IO       |                            |                                 |                                      |                             |            |          |                       |                              | 1         |
|                                                                                                                                                                                                                                                                  |               | spi1_cs1        | 7              | IO       |                            |                                 |                                      |                             |            |          |                       |                              | 1         |
|                                                                                                                                                                                                                                                                  |               | gpio3_31        | 14             | IO       |                            |                                 |                                      |                             |            |          |                       |                              |           |
|                                                                                                                                                                                                                                                                  |               | Driver off      | 15             | I        |                            |                                 |                                      |                             |            |          |                       |                              |           |

(1) NA in this table stands for Not Applicable.

(2) For more information on recommended operating conditions, see [Section 5.4, Recommended Operating Conditions](#).

(3) The pullup or pulldown block strength is equal to: minimum = 50  $\mu$ A, typical = 100  $\mu$ A, maximum = 250  $\mu$ A.

(4) The output impedance settings of this IO cell are programmable; by default, the value is DS[1:0] = 10, this means 40  $\Omega$ . For more information on DS[1:0] register configuration, see the Device TRM.

(5) In PUX / PDY, x and y = 60 to 300  $\mu$ A.

The output impedance settings (or drive strengths) of this IO are programmable (60  $\Omega$ , 80  $\Omega$ , 120  $\Omega$ ) depending on the values of the I[2:0] registers.

## 4.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

1. **SIGNAL NAME:** The name of the signal passing through the pin.

注: The subsystem multiplexing signals are not described in 表 4-1 and 表 4-29.

2. **DESCRIPTION:** Description of the signal

3. **TYPE:** Signal direction and type:

- I = Input
- O = Output
- IO = Input or output
- D = Open Drain
- DS = Differential
- A = Analog
- PWR = Power
- GND = Ground

4. **BALL:** Associated ball(s) bottom

注: For more information, see the Control Module / Control Module Register Manual section of the Device TRM.

### 4.3.1 VIP

注: For more information, see the Video Input Port (VIP) section of the Device TRM.

#### 注意

The IO timings provided in [Section 5.9, Timing Requirements and Switching Characteristics](#) are only valid for VIN1 and VIN2 if signals within a single IOSET are used. The IOSETs are defined in [表 5-28](#) and [表 5-29](#).

表 4-2. VIP Signal Descriptions

| SIGNAL NAME          | DESCRIPTION                                                                                                                            | TYPE | BALL |
|----------------------|----------------------------------------------------------------------------------------------------------------------------------------|------|------|
| <b>Video Input 1</b> |                                                                                                                                        |      |      |
| vin1a_clk0           | Video Input 1 Port A Clock input. Input clock for 8-bit 16-bit or 24-bit Port A video capture. Input data is sampled on the CLK0 edge. | I    | F22  |
| vin1a_d0             | Video Input 1 Port A Data input                                                                                                        | I    | G18  |

**表 4-2. VIP Signal Descriptions (continued)**

| SIGNAL NAME          | DESCRIPTION                                | TYPE | BALL           |
|----------------------|--------------------------------------------|------|----------------|
| vin1a_d1             | Video Input 1 Port A Data input            | I    | G21            |
| vin1a_d2             | Video Input 1 Port A Data input            | I    | G22            |
| vin1a_d3             | Video Input 1 Port A Data input            | I    | H18            |
| vin1a_d4             | Video Input 1 Port A Data input            | I    | H20            |
| vin1a_d5             | Video Input 1 Port A Data input            | I    | H19            |
| vin1a_d6             | Video Input 1 Port A Data input            | I    | H22            |
| vin1a_d7             | Video Input 1 Port A Data input            | I    | H21            |
| vin1a_d8             | Video Input 1 Port A Data input            | I    | J17            |
| vin1a_d9             | Video Input 1 Port A Data input            | I    | K22            |
| vin1a_d10            | Video Input 1 Port A Data input            | I    | K21            |
| vin1a_d11            | Video Input 1 Port A Data input            | I    | K18            |
| vin1a_d12            | Video Input 1 Port A Data input            | I    | AB17, K17      |
| vin1a_d13            | Video Input 1 Port A Data input            | I    | K19, U17       |
| vin1a_d14            | Video Input 1 Port A Data input            | I    | K20, W17       |
| vin1a_d15            | Video Input 1 Port A Data input            | I    | AA17, L21      |
| vin1a_de0            | Video Input 1 Port A Field ID input        | I    | F19, F21       |
| vin1a_fld0           | Video Input 1 Port A Field ID input        | I    | F20            |
| vin1a_hsync0         | Video Input 1 Port A Horizontal Sync input | I    | F19            |
| vin1a_vsync0         | Video Input 1 Port A Vertical Sync input   | I    | G19            |
| vin1b_clk1           | Video Input 1 Port B Clock input           | I    | F21            |
| vin1b_d0             | Video Input 1 Port B Data input            | I    | J17            |
| vin1b_d1             | Video Input 1 Port B Data input            | I    | K22            |
| vin1b_d2             | Video Input 1 Port B Data input            | I    | K21            |
| vin1b_d3             | Video Input 1 Port B Data input            | I    | K18            |
| vin1b_d4             | Video Input 1 Port B Data input            | I    | K17            |
| vin1b_d5             | Video Input 1 Port B Data input            | I    | K19            |
| vin1b_d6             | Video Input 1 Port B Data input            | I    | K20            |
| vin1b_d7             | Video Input 1 Port B Data input            | I    | L21            |
| vin1b_de1            | Video Input 1 Port B Field ID input        | I    | W7             |
| vin1b_hsync1         | Video Input 1 Port B Horizontal Sync input | I    | W7             |
| vin1b_vsync1         | Video Input 1 Port B Vertical Sync input   | I    | W6             |
| <b>Video Input 2</b> |                                            |      |                |
| vin2a_clk0           | Video Input 2 Port A Clock input           | I    | AB17, L22, W15 |

表 4-2. VIP Signal Descriptions (continued)

| SIGNAL NAME  | DESCRIPTION                                | TYPE | BALL                |
|--------------|--------------------------------------------|------|---------------------|
| vin2a_d0     | Video Input 2 Port A Data input            | I    | AA14                |
| vin2a_d1     | Video Input 2 Port A Data input            | I    | AB14                |
| vin2a_d2     | Video Input 2 Port A Data input            | I    | U13                 |
| vin2a_d3     | Video Input 2 Port A Data input            | I    | V13                 |
| vin2a_d4     | Video Input 2 Port A Data input            | I    | Y13                 |
| vin2a_d5     | Video Input 2 Port A Data input            | I    | W13                 |
| vin2a_d6     | Video Input 2 Port A Data input            | I    | U11                 |
| vin2a_d7     | Video Input 2 Port A Data input            | I    | V11                 |
| vin2a_d8     | Video Input 2 Port A Data input            | I    | U9                  |
| vin2a_d9     | Video Input 2 Port A Data input            | I    | W11                 |
| vin2a_d10    | Video Input 2 Port A Data input            | I    | V9                  |
| vin2a_d11    | Video Input 2 Port A Data input            | I    | W9                  |
| vin2a_d12    | Video Input 2 Port A Data input            | I    | U8                  |
| vin2a_d13    | Video Input 2 Port A Data input            | I    | W8                  |
| vin2a_d14    | Video Input 2 Port A Data input            | I    | U7                  |
| vin2a_d15    | Video Input 2 Port A Data input            | I    | V7                  |
| vin2a_de0    | Video Input 2 Port A Field ID input        | I    | AA15, AA17, M17, W7 |
| vin2a_fld0   | Video Input 2 Port A Field ID input        | I    | AB15, M18, U16      |
| vin2a_hsync0 | Video Input 2 Port A Horizontal Sync input | I    | F14, F15, W7        |
| vin2a_vsync0 | Video Input 2 Port A Vertical Sync input   | I    | C14, F16, W6        |
| vin2b_clk1   | Video Input 2 Port B Clock input           | I    | F20                 |
| vin2b_d0     | Video Input 2 Port B Data input            | I    | U9                  |
| vin2b_d1     | Video Input 2 Port B Data input            | I    | W11                 |
| vin2b_d2     | Video Input 2 Port B Data input            | I    | V9                  |
| vin2b_d3     | Video Input 2 Port B Data input            | I    | W9                  |
| vin2b_d4     | Video Input 2 Port B Data input            | I    | U8                  |
| vin2b_d5     | Video Input 2 Port B Data input            | I    | W8                  |
| vin2b_d6     | Video Input 2 Port B Data input            | I    | U7                  |
| vin2b_d7     | Video Input 2 Port B Data input            | I    | V7                  |
| vin2b_de1    | Video Input 2 Port B Field ID input        | I    | M17                 |
| vin2b_hsync1 | Video Input 2 Port B Horizontal Sync input | I    | M17                 |
| vin2b_vsync1 | Video Input 2 Port B Vertical Sync input   | I    | M18                 |

### 4.3.2 DSS

**表 4-3. DSS Signal Descriptions**

| SIGNAL NAME               | DESCRIPTION                                                                             | TYPE | BALL |
|---------------------------|-----------------------------------------------------------------------------------------|------|------|
| <b>DPI Video Output 1</b> |                                                                                         |      |      |
| vout1_clk                 | Video Output 1 Clock output                                                             | O    | AB17 |
| vout1_d0                  | Video Output 1 Data output                                                              | O    | W16  |
| vout1_d1                  | Video Output 1 Data output                                                              | O    | V16  |
| vout1_d2                  | Video Output 1 Data output                                                              | O    | U15  |
| vout1_d3                  | Video Output 1 Data output                                                              | O    | V15  |
| vout1_d4                  | Video Output 1 Data output                                                              | O    | Y15  |
| vout1_d5                  | Video Output 1 Data output                                                              | O    | W15  |
| vout1_d6                  | Video Output 1 Data output                                                              | O    | AA15 |
| vout1_d7                  | Video Output 1 Data output                                                              | O    | AB15 |
| vout1_d8                  | Video Output 1 Data output                                                              | O    | AA14 |
| vout1_d9                  | Video Output 1 Data output                                                              | O    | AB14 |
| vout1_d10                 | Video Output 1 Data output                                                              | O    | U13  |
| vout1_d11                 | Video Output 1 Data output                                                              | O    | V13  |
| vout1_d12                 | Video Output 1 Data output                                                              | O    | Y13  |
| vout1_d13                 | Video Output 1 Data output                                                              | O    | W13  |
| vout1_d14                 | Video Output 1 Data output                                                              | O    | U11  |
| vout1_d15                 | Video Output 1 Data output                                                              | O    | V11  |
| vout1_d16                 | Video Output 1 Data output                                                              | O    | U9   |
| vout1_d17                 | Video Output 1 Data output                                                              | O    | W11  |
| vout1_d18                 | Video Output 1 Data output                                                              | O    | V9   |
| vout1_d19                 | Video Output 1 Data output                                                              | O    | W9   |
| vout1_d20                 | Video Output 1 Data output                                                              | O    | U8   |
| vout1_d21                 | Video Output 1 Data output                                                              | O    | W8   |
| vout1_d22                 | Video Output 1 Data output                                                              | O    | U7   |
| vout1_d23                 | Video Output 1 Data output                                                              | O    | V7   |
| vout1_de                  | Video Output 1 Data Enable output                                                       | O    | U17  |
| vout1_fld                 | Video Output 1 Field ID output. This signal is not used for embedded sync modes.        | O    | W17  |
| vout1_hsync               | Video Output 1 Horizontal Sync output. This signal is not used for embedded sync modes. | O    | AA17 |
| vout1_vsync               | Video Output 1 Vertical Sync output. This signal is not used for embedded sync modes.   | O    | U16  |

### 4.3.3 SD\_DAC

注: For more information, see the Video Encoder / Video Encoder Overview of the Device TRM.

**表 4-4. CVIDEO SD\_DAC Signal Descriptions**

| SIGNAL NAME  | DESCRIPTION                                     | TYPE | BALL |
|--------------|-------------------------------------------------|------|------|
| cvideo_tvout | SD_DAC TV analog composite output               | A    | T17  |
| cvideo_vfb   | SD_DAC input feedback thru resistor to out      | A    | P17  |
| cvideo_rset  | SD_DAC input reference current resistor setting | A    | T18  |

#### 4.3.4 ADC

注: For more information, see the ADC / ADC Overview of the Device TRM.

**表 4-5. ADC Signal Descriptions**

| SIGNAL NAME | DESCRIPTION                    | TYPE | BALL |
|-------------|--------------------------------|------|------|
| adc_in0     | ADC analog channel input 0     | A    | M19  |
| adc_in1     | ADC analog channel input 1     | A    | M20  |
| adc_in2     | ADC analog channel input 2     | A    | M21  |
| adc_in3     | ADC analog channel input 3     | A    | M22  |
| adc_in4     | ADC analog channel input 4     | A    | N22  |
| adc_in5     | ADC analog channel input 5     | A    | N21  |
| adc_in6     | ADC analog channel input 6     | A    | P19  |
| adc_in7     | ADC analog channel input 7     | A    | P18  |
| adc_vrefp   | ADC positive reference voltage | A    | P20  |

#### 4.3.5 Camera Control

注: Camera Control is not available on this device, and must be left unconnected.

注: For more information, see the Imaging Subsystem (ISS) section of the Device TRM.

**表 4-6. Camera Control Signal Descriptions**

| SIGNAL NAME | DESCRIPTION                       | TYPE | BALL              |
|-------------|-----------------------------------|------|-------------------|
| cam_strobe  | Camera flash activation trigger   | O    | A6, B18, C16, M17 |
| cam_shutter | Camera mechanical shutter control | O    | C6, C18, C17, M18 |
| cam_nreset  | Camera sensor reset               | IO   | W6                |

#### 4.3.6 CPI

注: CPI is not available on this device, and must be left unconnected.

**表 4-7. CPI Signal Descriptions**

| SIGNAL NAME | DESCRIPTION                       | TYPE | BALL |
|-------------|-----------------------------------|------|------|
| cpi_pclk    | Camera pixel clock                | I    | F22  |
| cpi_hsync   | Camera horizontal synchronization | IO   | F21  |
| cpi_vsync   | Camera vertical synchronization   | IO   | F20  |
| cpi_data0   | Camera parallel data 0            | I    | F19  |
| cpi_data1   | Camera parallel data 1            | I    | G19  |
| cpi_data2   | Camera parallel data 2            | I    | G18  |
| cpi_data3   | Camera parallel data 3            | I    | G21  |
| cpi_data4   | Camera parallel data 4            | I    | G22  |
| cpi_data5   | Camera parallel data 5            | I    | H18  |
| cpi_data6   | Camera parallel data 6            | I    | H20  |
| cpi_data7   | Camera parallel data 7            | I    | H19  |
| cpi_data8   | Camera parallel data 8            | I    | H22  |

**表 4-7. CPI Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION                                                          | TYPE | BALL |
|-------------|----------------------------------------------------------------------|------|------|
| cpi_data9   | Camera parallel data 9                                               | I    | H21  |
| cpi_data10  | Camera parallel data 10                                              | I    | J17  |
| cpi_data11  | Camera parallel data 11                                              | I    | K22  |
| cpi_data12  | Camera parallel data 12                                              | I    | K21  |
| cpi_data13  | Camera parallel data 13                                              | I    | K18  |
| cpi_data14  | Camera parallel data 14                                              | I    | K17  |
| cpi_data15  | Camera parallel data 15                                              | I    | L21  |
| cpi_wen     | Camera parallel external write enable                                | I    | K19  |
| cpi_fid     | Camera parallel field identification for interlaced sensors (i mode) | IO   | K20  |

### 4.3.7 CSI2

注: ISS is not available on this device, and must be left unconnected.

注: For more information, see the Imaging Subsystem of the Device TRM.

**表 4-8. CSI 2 Signal Descriptions**

| SIGNAL NAME | DESCRIPTION                                                                       | TYPE | BALL |
|-------------|-----------------------------------------------------------------------------------|------|------|
| csi2_0_dx0  | Serial Differential data/clock positive input - lane 0 (position 1)               | I    | A11  |
| csi2_0_dy0  | Serial Differential data/clock negative input - lane 0 (position 1)               | I    | B11  |
| csi2_0_dx1  | Serial Differential data/clock positive input - lane 1 (position 2)               | I    | A12  |
| csi2_0_dy1  | Serial Differential data/clock negative input - lane 1 (position 2)               | I    | B12  |
| csi2_0_dx2  | Serial Differential data/clock positive input - lane 2 (position 3)               | I    | A13  |
| csi2_0_dy2  | Serial Differential data/clock negative input - lane 2 (position 3)               | I    | B13  |
| csi2_0_dx3  | Serial Differential data/clock positive input - lane 3 (position 4)               | I    | A15  |
| csi2_0_dy3  | Serial Differential data/clock negative input - lane 3 (position 4)               | I    | B15  |
| csi2_0_dx4  | Serial Differential data positive input only - lane 4 (position 5) <sup>(1)</sup> | I    | A16  |
| csi2_0_dy4  | Serial Differential data negative input only - lane 4 (position 5) <sup>(1)</sup> | I    | B16  |

(1) Lane 4 (position 5) supports only data. For more information see Imaging Subsystem of the Device TRM.

### 4.3.8 EMIF

注: For more information, see the Memory Subsystem / EMIF Controller section of the Device TRM.

注: The index number 1 which is part of the EMIF1 signal prefixes (ddr1\_\*) listed in 表 4-9, EMIF Signal Descriptions, column "SIGNAL NAME" is not to be confused with DDR1 type of SDRAM memories.

**表 4-9. EMIF Signal Descriptions**

| SIGNAL NAME | DESCRIPTION                                | TYPE | BALL |
|-------------|--------------------------------------------|------|------|
| ddr1_cke0   | EMIF1 Clock Enable 0                       | O    | F3   |
| ddr1_nck    | EMIF1 Negative Clock                       | O    | G2   |
| ddr1_odt0   | EMIF1 On-Die Termination for Chip Select 0 | O    | P2   |
| ddr1_rasn   | EMIF1 Row Address Strobe                   | O    | F1   |
| ddr1_rst    | EMIF1 Reset output                         | O    | N1   |
| ddr1_wen    | EMIF1 Write Enable                         | O    | E3   |
| ddr1_csn0   | EMIF1 Chip Select 0                        | O    | B2   |
| ddr1_ck     | EMIF1 Clock                                | O    | G1   |
| ddr1_casn   | EMIF1 Column Address Strobe                | O    | F2   |
| ddr1_ba0    | EMIF1 Bank Address                         | O    | B3   |
| ddr1_ba1    | EMIF1 Bank Address                         | O    | A3   |
| ddr1_ba2    | EMIF1 Bank Address                         | O    | D2   |
| ddr1_a0     | EMIF1 Address Bus                          | O    | U4   |
| ddr1_a1     | EMIF1 Address Bus                          | O    | C1   |
| ddr1_a2     | EMIF1 Address Bus                          | O    | D3   |
| ddr1_a3     | EMIF1 Address Bus                          | O    | R4   |

**表 4-9. EMIF Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION        | TYPE | BALL |
|-------------|--------------------|------|------|
| ddr1_a4     | EMIF1 Address Bus  | O    | T4   |
| ddr1_a5     | EMIF1 Address Bus  | O    | N3   |
| ddr1_a6     | EMIF1 Address Bus  | O    | T2   |
| ddr1_a7     | EMIF1 Address Bus  | O    | N2   |
| ddr1_a8     | EMIF1 Address Bus  | O    | T1   |
| ddr1_a9     | EMIF1 Address Bus  | O    | U1   |
| ddr1_a10    | EMIF1 Address Bus  | O    | D1   |
| ddr1_a11    | EMIF1 Address Bus  | O    | R3   |
| ddr1_a12    | EMIF1 Address Bus  | O    | U2   |
| ddr1_a13    | EMIF1 Address Bus  | O    | C3   |
| ddr1_a14    | EMIF1 Address Bus  | O    | R2   |
| ddr1_a15    | EMIF1 Address Bus  | O    | V1   |
| ddr1_d0     | EMIF1 Data Bus     | IO   | AA6  |
| ddr1_d1     | EMIF1 Data Bus     | IO   | AA8  |
| ddr1_d2     | EMIF1 Data Bus     | IO   | Y8   |
| ddr1_d3     | EMIF1 Data Bus     | IO   | AA7  |
| ddr1_d4     | EMIF1 Data Bus     | IO   | AB4  |
| ddr1_d5     | EMIF1 Data Bus     | IO   | Y5   |
| ddr1_d6     | EMIF1 Data Bus     | IO   | AA4  |
| ddr1_d7     | EMIF1 Data Bus     | IO   | Y6   |
| ddr1_d8     | EMIF1 Data Bus     | IO   | AA18 |
| ddr1_d9     | EMIF1 Data Bus     | IO   | Y21  |
| ddr1_d10    | EMIF1 Data Bus     | IO   | AA21 |
| ddr1_d11    | EMIF1 Data Bus     | IO   | Y22  |
| ddr1_d12    | EMIF1 Data Bus     | IO   | AA19 |
| ddr1_d13    | EMIF1 Data Bus     | IO   | AB20 |
| ddr1_d14    | EMIF1 Data Bus     | IO   | Y17  |
| ddr1_d15    | EMIF1 Data Bus     | IO   | AB18 |
| ddr1_d16    | EMIF1 Data Bus     | IO   | AA3  |
| ddr1_d17    | EMIF1 Data Bus     | IO   | AA2  |
| ddr1_d18    | EMIF1 Data Bus     | IO   | Y3   |
| ddr1_d19    | EMIF1 Data Bus     | IO   | V2   |
| ddr1_d20    | EMIF1 Data Bus     | IO   | U3   |
| ddr1_d21    | EMIF1 Data Bus     | IO   | V3   |
| ddr1_d22    | EMIF1 Data Bus     | IO   | Y2   |
| ddr1_d23    | EMIF1 Data Bus     | IO   | Y1   |
| ddr1_d24    | EMIF1 Data Bus     | IO   | U21  |
| ddr1_d25    | EMIF1 Data Bus     | IO   | T20  |
| ddr1_d26    | EMIF1 Data Bus     | IO   | R21  |
| ddr1_d27    | EMIF1 Data Bus     | IO   | U20  |
| ddr1_d28    | EMIF1 Data Bus     | IO   | R22  |
| ddr1_d29    | EMIF1 Data Bus     | IO   | V20  |
| ddr1_d30    | EMIF1 Data Bus     | IO   | W22  |
| ddr1_d31    | EMIF1 Data Bus     | IO   | U22  |
| ddr1_ecc_d0 | EMIF1 ECC Data Bus | IO   | Y11  |
| ddr1_ecc_d1 | EMIF1 ECC Data Bus | IO   | AA12 |
| ddr1_ecc_d2 | EMIF1 ECC Data Bus | IO   | AA11 |

表 4-9. EMIF Signal Descriptions (continued)

| SIGNAL NAME   | DESCRIPTION                                                                                                                                  | TYPE | BALL |
|---------------|----------------------------------------------------------------------------------------------------------------------------------------------|------|------|
| ddr1_ecc_d3   | EMIF1 ECC Data Bus                                                                                                                           | IO   | Y9   |
| ddr1_ecc_d4   | EMIF1 ECC Data Bus                                                                                                                           | IO   | AA13 |
| ddr1_ecc_d5   | EMIF1 ECC Data Bus                                                                                                                           | IO   | AB11 |
| ddr1_ecc_d6   | EMIF1 ECC Data Bus                                                                                                                           | IO   | AA9  |
| ddr1_ecc_d7   | EMIF1 ECC Data Bus                                                                                                                           | IO   | AB9  |
| ddr1_dqm0     | EMIF1 Data Mask                                                                                                                              | IO   | AB8  |
| ddr1_dqm1     | EMIF1 Data Mask                                                                                                                              | IO   | Y18  |
| ddr1_dqm2     | EMIF1 Data Mask                                                                                                                              | IO   | AB3  |
| ddr1_dqm3     | EMIF1 Data Mask                                                                                                                              | IO   | W21  |
| ddr1_dqm_ecc  | EMIF1 ECC Data Mask                                                                                                                          | IO   | AB13 |
| ddr1_dqs0     | Data strobe 0 input/output for byte 0 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading. | IO   | AA5  |
| ddr1_dqs1     | Data strobe 1 input/output for byte 1 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading. | IO   | AA20 |
| ddr1_dqs2     | Data strobe 2 input/output for byte 2 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading. | IO   | W1   |
| ddr1_dqs3     | Data strobe 3 input/output for byte 3 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading. | IO   | T21  |
| ddr1_dqsn0    | Data strobe 0 invert                                                                                                                         | IO   | AB5  |
| ddr1_dqsn1    | Data strobe 1 invert                                                                                                                         | IO   | Y20  |
| ddr1_dqsn2    | Data strobe 2 invert                                                                                                                         | IO   | W2   |
| ddr1_dqsn3    | Data strobe 3 invert                                                                                                                         | IO   | T22  |
| ddr1_dqsn_ecc | EMIF1 ECC Complementary Data strobe                                                                                                          | IO   | AB10 |
| ddr1_dqs_ecc  | EMIF1 ECC Data strobe input/output. This signal is output to the EMIF1 memory when writing and input when reading.                           | IO   | AA10 |

### 4.3.9 GPMC

注: For more information, see the Memory Subsystem / General-Purpose Memory Controller section of the Device TRM.

表 4-10. GPMC Signal Descriptions

| SIGNAL NAME | DESCRIPTION                                                                               | TYPE | BALL |
|-------------|-------------------------------------------------------------------------------------------|------|------|
| gpmc_ad0    | GPMC Data 0 in A/D nonmultiplexed mode and additionally Address 1 in A/D multiplexed mode | IO   | E8   |
| gpmc_ad1    | GPMC Data 1 in A/D nonmultiplexed mode and additionally Address 2 in A/D multiplexed mode | IO   | A7   |
| gpmc_ad2    | GPMC Data 2 in A/D nonmultiplexed mode and additionally Address 3 in A/D multiplexed mode | IO   | F8   |
| gpmc_ad3    | GPMC Data 3 in A/D nonmultiplexed mode and additionally Address 4 in A/D multiplexed mode | IO   | B7   |
| gpmc_ad4    | GPMC Data 4 in A/D nonmultiplexed mode and additionally Address 5 in A/D multiplexed mode | IO   | A6   |
| gpmc_ad5    | GPMC Data 5 in A/D nonmultiplexed mode and additionally Address 6 in A/D multiplexed mode | IO   | F7   |
| gpmc_ad6    | GPMC Data 6 in A/D nonmultiplexed mode and additionally Address 7 in A/D multiplexed mode | IO   | E7   |
| gpmc_ad7    | GPMC Data 7 in A/D nonmultiplexed mode and additionally Address 8 in A/D multiplexed mode | IO   | C6   |
| gpmc_ad8    | GPMC Data 8 in A/D nonmultiplexed mode and additionally Address 9 in A/D multiplexed mode | IO   | B6   |

**表 4-10. GPMC Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION                                                                                 | TYPE | BALL               |
|-------------|---------------------------------------------------------------------------------------------|------|--------------------|
| gpmc_ad9    | GPMC Data 9 in A/D nonmultiplexed mode and additionally Address 10 in A/D multiplexed mode  | IO   | A5                 |
| gpmc_ad10   | GPMC Data 10 in A/D nonmultiplexed mode and additionally Address 11 in A/D multiplexed mode | IO   | D6                 |
| gpmc_ad11   | GPMC Data 11 in A/D nonmultiplexed mode and additionally Address 12 in A/D multiplexed mode | IO   | C5                 |
| gpmc_ad12   | GPMC Data 12 in A/D nonmultiplexed mode and additionally Address 13 in A/D multiplexed mode | IO   | B5                 |
| gpmc_ad13   | GPMC Data 13 in A/D nonmultiplexed mode and additionally Address 14 in A/D multiplexed mode | IO   | D7                 |
| gpmc_ad14   | GPMC Data 14 in A/D nonmultiplexed mode and additionally Address 15 in A/D multiplexed mode | IO   | B4                 |
| gpmc_ad15   | GPMC Data 15 in A/D nonmultiplexed mode and additionally Address 16 in A/D multiplexed mode | IO   | A4                 |
| gpmc_a0     | GPMC Address 0. Only used to effectively address 8-bit data nonmultiplexed memories         | O    | U9                 |
| gpmc_a1     | GPMC address 1 in A/D nonmultiplexed mode and Address 17 in A/D multiplexed mode            | O    | W11                |
| gpmc_a2     | GPMC address 2 in A/D nonmultiplexed mode and Address 18 in A/D multiplexed mode            | O    | V9                 |
| gpmc_a3     | GPMC address 3 in A/D nonmultiplexed mode and Address 19 in A/D multiplexed mode            | O    | W9                 |
| gpmc_a4     | GPMC address 4 in A/D nonmultiplexed mode and Address 20 in A/D multiplexed mode            | O    | U8                 |
| gpmc_a5     | GPMC address 5 in A/D nonmultiplexed mode and Address 21 in A/D multiplexed mode            | O    | W8                 |
| gpmc_a6     | GPMC address 6 in A/D nonmultiplexed mode and Address 22 in A/D multiplexed mode            | O    | U7                 |
| gpmc_a7     | GPMC address 7 in A/D nonmultiplexed mode and Address 23 in A/D multiplexed mode            | O    | V7                 |
| gpmc_a8     | GPMC address 8 in A/D nonmultiplexed mode and Address 24 in A/D multiplexed mode            | O    | J17                |
| gpmc_a9     | GPMC address 9 in A/D nonmultiplexed mode and Address 25 in A/D multiplexed mode            | O    | K22                |
| gpmc_a10    | GPMC address 10 in A/D nonmultiplexed mode and Address 26 in A/D multiplexed mode           | O    | K21                |
| gpmc_a11    | GPMC address 11 in A/D nonmultiplexed mode and unused in A/D multiplexed mode               | O    | K18                |
| gpmc_a12    | GPMC address 12 in A/D nonmultiplexed mode and unused in A/D multiplexed mode               | O    | D14, F13, F14, K17 |
| gpmc_a13    | GPMC address 13 in A/D nonmultiplexed mode and unused in A/D multiplexed mode               | O    | C14, D15, E14, K19 |
| gpmc_a14    | GPMC address 14 in A/D nonmultiplexed mode and unused in A/D multiplexed mode               | O    | K20                |
| gpmc_a15    | GPMC address 15 in A/D nonmultiplexed mode and unused in A/D multiplexed mode               | O    | L21                |
| gpmc_a16    | GPMC address 16 in A/D nonmultiplexed mode and unused in A/D multiplexed mode               | O    | F14                |
| gpmc_a17    | GPMC address 17 in A/D nonmultiplexed mode and unused in A/D multiplexed mode               | O    | C14                |
| gpmc_a18    | GPMC address 18 in A/D nonmultiplexed mode and unused in A/D multiplexed mode               | O    | F15                |
| gpmc_a19    | GPMC address 19 in A/D nonmultiplexed mode and unused in A/D multiplexed mode               | O    | F16                |
| gpmc_a20    | GPMC address 20 in A/D nonmultiplexed mode and unused in A/D multiplexed mode               | O    | AA14               |

表 4-10. GPMC Signal Descriptions (continued)

| SIGNAL NAME             | DESCRIPTION                                                                       | TYPE | BALL               |
|-------------------------|-----------------------------------------------------------------------------------|------|--------------------|
| gpmc_a21                | GPMC address 21 in A/D nonmultiplexed mode and unused in A/D multiplexed mode     | O    | AB14               |
| gpmc_a22                | GPMC address 22 in A/D nonmultiplexed mode and unused in A/D multiplexed mode     | O    | U13                |
| gpmc_a23                | GPMC address 23 in A/D nonmultiplexed mode and unused in A/D multiplexed mode     | O    | V13                |
| gpmc_a24                | GPMC address 24 in A/D nonmultiplexed mode and unused in A/D multiplexed mode     | O    | Y13                |
| gpmc_a25                | GPMC address 25 in A/D nonmultiplexed mode and unused in A/D multiplexed mode     | O    | W13                |
| gpmc_a26                | GPMC address 26 in A/D nonmultiplexed mode and unused in A/D multiplexed mode     | O    | U11                |
| gpmc_a27                | GPMC address 27 in A/D nonmultiplexed mode and Address 27 in A/D multiplexed mode | O    | V11                |
| gpmc_cs0                | GPMC Chip Select 0 (active low)                                                   | O    | C10                |
| gpmc_cs1                | GPMC Chip Select 1 (active low)                                                   | O    | E10                |
| gpmc_cs2                | GPMC Chip Select 2 (active low)                                                   | O    | D10                |
| gpmc_cs3                | GPMC Chip Select 3 (active low)                                                   | O    | A9                 |
| gpmc_cs4                | GPMC Chip Select 4 (active low)                                                   | O    | B9                 |
| gpmc_cs5                | GPMC Chip Select 5 (active low)                                                   | O    | F10                |
| gpmc_cs6                | GPMC Chip Select 6 (active low)                                                   | O    | C8                 |
| gpmc_cs7                | GPMC Chip Select 7 (active low)                                                   | O    | W6                 |
| gpmc_clk <sup>(1)</sup> | GPMC Clock output                                                                 | IO   | C12, D14, F14, F15 |
| gpmc_advn_ale           | GPMC address valid active low or address latch enable                             | O    | F12                |
| gpmc_oen_ren            | GPMC output enable active low or read enable                                      | O    | A10                |
| gpmc_wen                | GPMC write enable active low                                                      | O    | B10                |
| gpmc_ben0               | GPMC lower-byte enable active low                                                 | O    | D12                |
| gpmc_ben1               | GPMC upper-byte enable active low                                                 | O    | E12                |
| gpmc_wait0              | GPMC external indication of wait 0                                                | I    | D8                 |
| gpmc_wait1              | GPMC external indication of wait 1                                                | I    | W7                 |

(1) The gpio6\_16.clkout0 signal can be used as an “always-on” alternative to gpmc\_clk provided that the external device can support the associated timing. See 表 5-32, *GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - 1 Load* and 表 5-34, *GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - 5 Loads* for timing information.

#### 4.3.10 Timers

注: For more information, see the Timers section of the Device TRM.

表 4-11. Timers Signal Descriptions

| SIGNAL NAME | DESCRIPTION                    | TYPE | BALL        |
|-------------|--------------------------------|------|-------------|
| timer1      | PWM output/event trigger input | IO   | D14, R7     |
| timer2      | PWM output/event trigger input | IO   | D15, D6     |
| timer3      | PWM output/event trigger input | IO   | C5, F14, L1 |
| timer4      | PWM output/event trigger input | IO   | C14, C6, L2 |
| timer5      | PWM output/event trigger input | IO   | E7, N4      |
| timer6      | PWM output/event trigger input | IO   | F7, R5      |
| timer7      | PWM output/event trigger input | IO   | B6, F15     |
| timer8      | PWM output/event trigger input | IO   | F16         |

### 4.3.11 I<sup>2</sup>C

注: For more information, see the Serial Communication Interface / Multimaster I2C Controller / I2C Environment / I2C Pins for Typical Connections in I2C Mode section of the Device TRM.

**表 4-12. I<sup>2</sup>C Signal Descriptions**

| SIGNAL NAME                                      | DESCRIPTION | TYPE | BALL |
|--------------------------------------------------|-------------|------|------|
| <b>Inter-Integrated Circuit Interface (I2C1)</b> |             |      |      |
| i2c1_scl                                         | I2C1 Clock  | IOD  | L3   |
| i2c1_sda                                         | I2C1 Data   | IOD  | L4   |
| <b>Inter-Integrated Circuit Interface (I2C2)</b> |             |      |      |
| i2c2_scl                                         | I2C2 Clock  | IOD  | L6   |
| i2c2_sda                                         | I2C2 Data   | IOD  | L5   |

### 4.3.12 UART

注: For more information see the Serial Communication Interface UART section of the Device TRM.

**注意**

The IO timings provided in [Section 5.9, Timing Requirements and Switching Characteristics](#) are only valid if signals within a single IOSET are used. The IOSETs are defined in [表 5-43](#).

**表 4-13. UART Signal Descriptions**

| SIGNAL NAME                                                | DESCRIPTION                      | TYPE | BALL            |
|------------------------------------------------------------|----------------------------------|------|-----------------|
| <b>Universal Asynchronous Receiver/Transmitter (UART1)</b> |                                  |      |                 |
| uart1_ctsn                                                 | UART1 clear to send active low   | I    | F14             |
| uart1_rtsn                                                 | UART1 request to send active low | O    | C14             |
| uart1_rxd                                                  | UART1 Receive Data               | I    | F13             |
| uart1_txd                                                  | UART1 Transmit Data              | O    | E14             |
| <b>Universal Asynchronous Receiver/Transmitter (UART2)</b> |                                  |      |                 |
| uart2_ctsn                                                 | UART2 clear to send active low   | I    | F15             |
| uart2_rtsn                                                 | UART2 request to send active low | O    | F16             |
| uart2_rxd                                                  | UART2 Receive Data               | I    | D14, E7         |
| uart2_txd                                                  | UART2 Transmit Data              | O    | D15, F7         |
| <b>Universal Asynchronous Receiver/Transmitter (UART3)</b> |                                  |      |                 |
| uart3_ctsn                                                 | UART3 clear to send active low   | I    | N4, U6          |
| uart3_rtsn                                                 | UART3 request to send active low | O    | R7, T5          |
| uart3_rxd                                                  | UART3 Receive Data               | I    | F14, L1, M2, W7 |
| uart3_txd                                                  | UART3 Transmit Data              | O    | C14, L2, R6, W6 |

### 4.3.13 McSPI

注: For more information, see the Serial Communication Interface / Multichannel Serial Peripheral Interface (McSPI) section of the Device TRM.

#### 注意

The IO timings provided in [Section 5.9, Timing Requirements and Switching Characteristics](#) are applicable for all combinations of signals for SPI2 and SPI4. However, the timings are only valid for SPI1 and SPI3 if signals within a single IOSET are used. The IOSETs are defined in [表 5-46](#).

**表 4-14. SPI Signal Descriptions**

| SIGNAL NAME                          | DESCRIPTION                                          | TYPE | BALL        |
|--------------------------------------|------------------------------------------------------|------|-------------|
| <b>Serial Peripheral Interface 1</b> |                                                      |      |             |
| spi1_sclk                            | SPI1 Clock                                           | IO   | M2          |
| spi1_d0                              | SPI1 Data. Can be configured as either MISO or MOSI. | IO   | T5          |
| spi1_d1                              | SPI1 Data. Can be configured as either MISO or MOSI. | IO   | U6          |
| spi1_cs0                             | SPI1 Chip Select                                     | IO   | M1, R6      |
| spi1_cs1                             | SPI1 Chip Select                                     | IO   | M1, R5      |
| spi1_cs2                             | SPI1 Chip Select                                     | IO   | F14, W7     |
| spi1_cs3                             | SPI1 Chip Select                                     | IO   | C14, W6     |
| <b>Serial Peripheral Interface 2</b> |                                                      |      |             |
| spi2_sclk                            | SPI2 Clock                                           | IO   | L1          |
| spi2_d0                              | SPI2 Data. Can be configured as either MISO or MOSI. | IO   | R7          |
| spi2_d1                              | SPI2 Data. Can be configured as either MISO or MOSI. | IO   | N4          |
| spi2_cs0                             | SPI2 Chip Select                                     | IO   | A4, L2      |
| spi2_cs1                             | SPI2 Chip Select                                     | IO   | B4, M1      |
| <b>Serial Peripheral Interface 3</b> |                                                      |      |             |
| spi3_sclk                            | SPI3 Clock                                           | IO   | C6, F15     |
| spi3_d0                              | SPI3 Data. Can be configured as either MISO or MOSI. | IO   | D15, E7     |
| spi3_d1                              | SPI3 Data. Can be configured as either MISO or MOSI. | IO   | D14, F7     |
| spi3_cs0                             | SPI3 Chip Select                                     | IO   | B6, F16, M1 |
| spi3_cs1                             | SPI3 Chip Select                                     | IO   | A5, R5      |
| <b>Serial Peripheral Interface 4</b> |                                                      |      |             |
| spi4_sclk                            | SPI4 Clock                                           | IO   | C16, F14    |
| spi4_d0                              | SPI4 Data. Can be configured as either MISO or MOSI. | IO   | B17, E14    |
| spi4_d1                              | SPI4 Data. Can be configured as either MISO or MOSI. | IO   | B19, F13    |
| spi4_cs0                             | SPI4 Chip Select                                     | IO   | C14, C17    |

### 4.3.14 QSPI

注: For more information see the Serial Communication Interface / Quad Serial Peripheral Interface section of the Device TRM.

注意

The IO timings provided in [Section 5.9, Timing Requirements and Switching Characteristics](#) are only valid if signals within a single IOSET are used. The IOSETs are defined in [表 5-49](#).

**表 4-15. QSPI Signal Descriptions**

| SIGNAL NAME | DESCRIPTION                                                                                                                                       | TYPE | BALL             |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------|------|------------------|
| qspi1_sclk  | QSPI1 Serial Clock                                                                                                                                | O    | C8               |
| qspi1_rtclk | QSPI1 Return Clock Input. Must be connected from QSPI1_SCLK on PCB. Refer to PCB Guidelines for QSPI1                                             | I    | B7, C14, D8, F13 |
| qspi1_d0    | QSPI1 Data[0]. This pin is output data for all commands/writes and for dual read and quad read modes it becomes input data pin during read phase. | IO   | B9               |
| qspi1_d1    | QSPI1 Data[1]. Input read data in all modes.                                                                                                      | IO   | F10              |
| qspi1_d2    | QSPI1 Data[2]. This pin is used only in quad read mode as input data pin during read phase                                                        | IO   | A9               |
| qspi1_d3    | QSPI1 Data[3]. This pin is used only in quad read mode as input data pin during read phase                                                        | IO   | D10              |
| qspi1_cs0   | QSPI1 Chip Select[0]. This pin is used for QSPI1 boot modes.                                                                                      | IO   | E10              |
| qspi1_cs1   | QSPI1 Chip Select[1]                                                                                                                              | IO   | F15              |

#### 4.3.15 McASP

注: For more information, see the Serial Communication Interface / Multichannel Audio Serial Port (McASP) section of the Device TRM.

注意

The IO timings provided in [Section 5.9, Timing Requirements and Switching Characteristics](#) are only valid if signals within a single IOSET are used. The IOSETs are defined in [表 5-56](#).

**表 4-16. McASP Signal Descriptions**

| SIGNAL NAME                             | DESCRIPTION                  | TYPE | BALL           |
|-----------------------------------------|------------------------------|------|----------------|
| <b>Multichannel Audio Serial Port 1</b> |                              |      |                |
| mcasp1_axr0                             | McASP1 Transmit/Receive Data | IO   | W16            |
| mcasp1_axr1                             | McASP1 Transmit/Receive Data | IO   | V16            |
| mcasp1_axr2                             | McASP1 Transmit/Receive Data | IO   | U15            |
| mcasp1_axr3                             | McASP1 Transmit/Receive Data | IO   | V15            |
| mcasp1_axr4                             | McASP1 Transmit/Receive Data | IO   | Y15            |
| mcasp1_axr5                             | McASP1 Transmit/Receive Data | IO   | W15            |
| mcasp1_axr6                             | McASP1 Transmit/Receive Data | IO   | AA15           |
| mcasp1_axr7                             | McASP1 Transmit/Receive Data | IO   | AB15           |
| mcasp1_axr8                             | McASP1 Transmit/Receive Data | IO   | AA14, U15, U9  |
| mcasp1_axr9                             | McASP1 Transmit/Receive Data | IO   | AB14, V15, W11 |
| mcasp1_axr10                            | McASP1 Transmit/Receive Data | IO   | U13, V9, Y15   |
| mcasp1_axr11                            | McASP1 Transmit/Receive Data | IO   | V13, W15, W9   |
| mcasp1_axr12                            | McASP1 Transmit/Receive Data | IO   | AA15, U8, Y13  |
| mcasp1_axr13                            | McASP1 Transmit/Receive Data | IO   | AB15, W13, W8  |

表 4-16. McASP Signal Descriptions (continued)

| SIGNAL NAME                             | DESCRIPTION                                 | TYPE | BALL    |
|-----------------------------------------|---------------------------------------------|------|---------|
| mcasp1_axr14                            | McASP1 Transmit/Receive Data                | IO   | U11, U7 |
| mcasp1_axr15                            | McASP1 Transmit/Receive Data                | IO   | V11, V7 |
| mcasp1_fsx                              | McASP1 Transmit Frame Sync                  | IO   | W17     |
| mcasp1_aclkr                            | McASP1 Receive Bit Clock                    | IO   | AA17    |
| mcasp1_fsr                              | McASP1 Receive Frame Sync                   | IO   | U16     |
| mcasp1_ahclkx                           | McASP1 Transmit High-Frequency Master Clock | O    | U9      |
| mcasp1_aclkx                            | McASP1 Transmit Bit Clock                   | IO   | U17     |
| <b>Multichannel Audio Serial Port 2</b> |                                             |      |         |
| mcasp2_axr0                             | McASP2 Transmit/Receive Data                | IO   | D6, V9  |
| mcasp2_axr1                             | McASP2 Transmit/Receive Data                | IO   | C5, W9  |
| mcasp2_axr2                             | McASP2 Transmit/Receive Data                | IO   | B5, U8  |
| mcasp2_axr3                             | McASP2 Transmit/Receive Data                | IO   | D7, W8  |
| mcasp2_axr4                             | McASP2 Transmit/Receive Data                | IO   | B4, U7  |
| mcasp2_axr5                             | McASP2 Transmit/Receive Data                | IO   | A4, V7  |
| mcasp2_fsx                              | McASP2 Transmit Frame Sync                  | IO   | E7, V11 |
| mcasp2_aclkr                            | McASP2 Receive Bit Clock                    | IO   | B6, W13 |
| mcasp2_fsr                              | McASP2 Receive Frame Sync                   | IO   | A5, W11 |
| mcasp2_ahclkx                           | McASP2 Transmit High-Frequency Master Clock | O    | C6, Y13 |
| mcasp2_aclkx                            | McASP2 Transmit Bit Clock                   | IO   | F7, U11 |
| <b>Multichannel Audio Serial Port 3</b> |                                             |      |         |
| mcasp3_axr0                             | McASP3 Transmit/Receive Data                | IO   | G19     |
| mcasp3_axr1                             | McASP3 Transmit/Receive Data                | IO   | G18     |
| mcasp3_axr2                             | McASP3 Transmit/Receive Data                | IO   | G21     |
| mcasp3_axr3                             | McASP3 Transmit/Receive Data                | IO   | G22     |
| mcasp3_axr4                             | McASP3 Transmit/Receive Data                | IO   | H18     |
| mcasp3_axr5                             | McASP3 Transmit/Receive Data                | IO   | H20     |
| mcasp3_fsx                              | McASP3 Transmit Frame Sync                  | IO   | H22     |
| mcasp3_ahclkx                           | McASP3 Transmit High-Frequency Master Clock | O    | H19     |
| mcasp3_aclkx                            | McASP3 Transmit Bit Clock                   | IO   | F22     |
| mcasp3_aclkr                            | McASP3 Receive Bit Clock                    | IO   | F20     |
| mcasp3_fsr                              | McASP3 Receive Frame Sync                   | IO   | F19     |

#### 4.3.16 DCAN and MCAN

注: For more information, see the Serial Communication Interface / DCAN section of the Device TRM.

#### 注意

The IO timings provided in [Section 5.9, Timing Requirements and Switching Characteristics](#) are only valid if signals within a single IOSET are used. The IOSETs are defined in [表 5-60](#).

表 4-17. DCAN and MCAN Signal Descriptions

| SIGNAL NAME   | DESCRIPTION | TYPE | BALL |
|---------------|-------------|------|------|
| <b>DCAN 1</b> |             |      |      |

**表 4-17. DCAN and MCAN Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION             | TYPE | BALL         |
|-------------|-------------------------|------|--------------|
| dcan1_rx    | DCAN1 receive data pin  | IO   | C14, D15, N6 |
| dcan1_tx    | DCAN1 transmit data pin | IO   | D14, F14, N5 |
| <b>MCAN</b> |                         |      |              |
| mcan_rx     | MCAN receive data pin   | IO   | E14, F16, W6 |
| mcan_tx     | MCAN transmit data pin  | IO   | F13, F15, W7 |

#### 4.3.17 GMAC\_SW

注: For more information, see the Serial Communication Interfaces / Gigabit Ethernet Switch (GMAC\_SW) section of the Device TRM.

**表 4-18. GMAC Signal Descriptions**

| SIGNAL NAME  | DESCRIPTION                  | TYPE | BALL |
|--------------|------------------------------|------|------|
| rgmii0_rxc   | RGMII0 Receive Clock         | I    | B18  |
| rgmii0_rxctl | RGMII0 Receive Control       | I    | C18  |
| rgmii0_rxd0  | RGMII0 Receive Data          | I    | A20  |
| rgmii0_rxd1  | RGMII0 Receive Data          | I    | C20  |
| rgmii0_rxd2  | RGMII0 Receive Data          | I    | B20  |
| rgmii0_rxd3  | RGMII0 Receive Data          | I    | A19  |
| rgmii0_txc   | RGMII0 Transmit Clock        | O    | C16  |
| rgmii0_txctl | RGMII0 Transmit Enable       | O    | C17  |
| rgmii0_txd0  | RGMII0 Transmit Data         | O    | F17  |
| rgmii0_txd1  | RGMII0 Transmit Data         | O    | E17  |
| rgmii0_txd2  | RGMII0 Transmit Data         | O    | D16  |
| rgmii0_txd3  | RGMII0 Transmit Data         | O    | E16  |
| rgmii1_rxc   | RGMII1 Receive Clock         | I    | D7   |
| rgmii1_rxctl | RGMII1 Receive Control       | I    | C10  |
| rgmii1_rxd0  | RGMII1 Receive Data          | I    | F8   |
| rgmii1_rxd1  | RGMII1 Receive Data          | I    | A7   |
| rgmii1_rxd2  | RGMII1 Receive Data          | I    | E8   |
| rgmii1_rxd3  | RGMII1 Receive Data          | I    | D8   |
| rgmii1_txc   | RGMII1 Transmit Clock        | O    | C12  |
| rgmii1_txctl | RGMII1 Transmit Enable       | O    | D12  |
| rgmii1_txd0  | RGMII1 Transmit Data         | O    | B10  |
| rgmii1_txd1  | RGMII1 Transmit Data         | O    | A10  |
| rgmii1_txd2  | RGMII1 Transmit Data         | O    | F12  |
| rgmii1_txd3  | RGMII1 Transmit Data         | O    | E12  |
| mdio_d       | Management Data              | IO   | B17  |
| mdio_mclk    | Management Data Serial Clock | O    | B19  |

#### 4.3.18 SDIO Controller

注: For more information, see the SDIO Controller section of the Device TRM.

**注意**

The IO timings provided in [Section 5.9, Timing Requirements and Switching Characteristics](#) are only valid if signals within a single IOSET are used. The IOSETs are defined in [表 5-75](#).

**表 4-19. SDIO Controller Signal Descriptions**

| SIGNAL NAME               | DESCRIPTION     | TYPE | BALL                          |
|---------------------------|-----------------|------|-------------------------------|
| <b>Multi Media Card 1</b> |                 |      |                               |
| mmc_clk                   | MMC1 clock      | IO   | <a href="#">B18, C16, W16</a> |
| mmc_cmd                   | MMC1 command    | IO   | <a href="#">C17, C18, V16</a> |
| mmc_dat0                  | MMC1 data bit 0 | IO   | <a href="#">A19, E16, U15</a> |
| mmc_dat1                  | MMC1 data bit 1 | IO   | <a href="#">B20, D16, V15</a> |
| mmc_dat2                  | MMC1 data bit 2 | IO   | <a href="#">C20, E17, Y15</a> |
| mmc_dat3                  | MMC1 data bit 3 | IO   | <a href="#">A20, F17, W15</a> |

**4.3.19 GPIO**

注: For more information, see the General-Purpose Interface section of the Device TRM.

**注意**

The IO timings provided in [Section 5.9, Timing Requirements and Switching Characteristics](#) are only valid if signals within a single IOSET are used. The IOSETs are defined in [表 5-76](#).

**表 4-20. GPIOs Signal Descriptions**

| SIGNAL NAME   | DESCRIPTION                  | TYPE | BALL                |
|---------------|------------------------------|------|---------------------|
| <b>GPIO 1</b> |                              |      |                     |
| gpio1_0       | General-Purpose Input/Output | IO   | <a href="#">C12</a> |
| gpio1_1       | General-Purpose Input/Output | IO   | <a href="#">D12</a> |
| gpio1_2       | General-Purpose Input/Output | IO   | <a href="#">E12</a> |
| gpio1_3       | General-Purpose Input/Output | IO   | <a href="#">F12</a> |
| gpio1_4       | General-Purpose Input/Output | IO   | <a href="#">A10</a> |
| gpio1_5       | General-Purpose Input/Output | IO   | <a href="#">B10</a> |
| gpio1_6       | General-Purpose Input/Output | IO   | <a href="#">C10</a> |
| gpio1_7       | General-Purpose Input/Output | IO   | <a href="#">E10</a> |
| gpio1_8       | General-Purpose Input/Output | IO   | <a href="#">D10</a> |
| gpio1_9       | General-Purpose Input/Output | IO   | <a href="#">A9</a>  |
| gpio1_10      | General-Purpose Input/Output | IO   | <a href="#">B9</a>  |
| gpio1_11      | General-Purpose Input/Output | IO   | <a href="#">F10</a> |
| gpio1_12      | General-Purpose Input/Output | IO   | <a href="#">C8</a>  |
| gpio1_13      | General-Purpose Input/Output | IO   | <a href="#">D8</a>  |
| gpio1_14      | General-Purpose Input/Output | IO   | <a href="#">E8</a>  |
| gpio1_15      | General-Purpose Input/Output | IO   | <a href="#">A7</a>  |
| gpio1_16      | General-Purpose Input/Output | IO   | <a href="#">F8</a>  |
| gpio1_17      | General-Purpose Input/Output | IO   | <a href="#">B7</a>  |
| gpio1_18      | General-Purpose Input/Output | IO   | <a href="#">A6</a>  |

**表 4-20. GPIOs Signal Descriptions (continued)**

| SIGNAL NAME   | DESCRIPTION                  | TYPE | BALL |
|---------------|------------------------------|------|------|
| gpio1_19      | General-Purpose Input/Output | IO   | F7   |
| gpio1_20      | General-Purpose Input/Output | IO   | E7   |
| gpio1_21      | General-Purpose Input/Output | IO   | C6   |
| gpio1_22      | General-Purpose Input/Output | IO   | B6   |
| gpio1_23      | General-Purpose Input/Output | IO   | A5   |
| gpio1_24      | General-Purpose Input/Output | IO   | D6   |
| gpio1_25      | General-Purpose Input/Output | IO   | C5   |
| gpio1_26      | General-Purpose Input/Output | IO   | B5   |
| gpio1_27      | General-Purpose Input/Output | IO   | D7   |
| gpio1_28      | General-Purpose Input/Output | IO   | B4   |
| gpio1_29      | General-Purpose Input/Output | IO   | A4   |
| gpio1_30      | General-Purpose Input/Output | IO   | F22  |
| gpio1_31      | General-Purpose Input/Output | IO   | F21  |
| <b>GPIO 2</b> |                              |      |      |
| gpio2_0       | General-Purpose Input/Output | IO   | F20  |
| gpio2_1       | General-Purpose Input/Output | IO   | F19  |
| gpio2_2       | General-Purpose Input/Output | IO   | G19  |
| gpio2_3       | General-Purpose Input/Output | IO   | G18  |
| gpio2_4       | General-Purpose Input/Output | IO   | G21  |
| gpio2_5       | General-Purpose Input/Output | IO   | G22  |
| gpio2_6       | General-Purpose Input/Output | IO   | H18  |
| gpio2_7       | General-Purpose Input/Output | IO   | H20  |
| gpio2_8       | General-Purpose Input/Output | IO   | H19  |
| gpio2_9       | General-Purpose Input/Output | IO   | H22  |
| gpio2_10      | General-Purpose Input/Output | IO   | H21  |
| gpio2_11      | General-Purpose Input/Output | IO   | J17  |
| gpio2_12      | General-Purpose Input/Output | IO   | K22  |
| gpio2_13      | General-Purpose Input/Output | IO   | K21  |
| gpio2_14      | General-Purpose Input/Output | IO   | K18  |
| gpio2_15      | General-Purpose Input/Output | IO   | K17  |
| gpio2_16      | General-Purpose Input/Output | IO   | K19  |
| gpio2_17      | General-Purpose Input/Output | IO   | K20  |
| gpio2_18      | General-Purpose Input/Output | IO   | L21  |
| gpio2_19      | General-Purpose Input/Output | IO   | L22  |
| gpio2_20      | General-Purpose Input/Output | IO   | AB17 |
| gpio2_21      | General-Purpose Input/Output | IO   | U17  |
| gpio2_22      | General-Purpose Input/Output | IO   | W17  |
| gpio2_23      | General-Purpose Input/Output | IO   | AA17 |
| gpio2_24      | General-Purpose Input/Output | IO   | U16  |
| gpio2_25      | General-Purpose Input/Output | IO   | W16  |
| gpio2_26      | General-Purpose Input/Output | IO   | V16  |
| gpio2_27      | General-Purpose Input/Output | IO   | U15  |
| gpio2_28      | General-Purpose Input/Output | IO   | V15  |
| gpio2_29      | General-Purpose Input/Output | IO   | Y15  |
| gpio2_30      | General-Purpose Input/Output | IO   | W15  |
| gpio2_31      | General-Purpose Input/Output | IO   | AA15 |
| <b>GPIO 3</b> |                              |      |      |

表 4-20. GPIOs Signal Descriptions (continued)

| SIGNAL NAME   | DESCRIPTION                  | TYPE | BALL |
|---------------|------------------------------|------|------|
| gpio3_0       | General-Purpose Input/Output | IO   | AB15 |
| gpio3_1       | General-Purpose Input/Output | IO   | AA14 |
| gpio3_2       | General-Purpose Input/Output | IO   | AB14 |
| gpio3_3       | General-Purpose Input/Output | IO   | U13  |
| gpio3_4       | General-Purpose Input/Output | IO   | V13  |
| gpio3_5       | General-Purpose Input/Output | IO   | Y13  |
| gpio3_6       | General-Purpose Input/Output | IO   | W13  |
| gpio3_7       | General-Purpose Input/Output | IO   | U11  |
| gpio3_8       | General-Purpose Input/Output | IO   | V11  |
| gpio3_9       | General-Purpose Input/Output | IO   | U9   |
| gpio3_10      | General-Purpose Input/Output | IO   | W11  |
| gpio3_11      | General-Purpose Input/Output | IO   | V9   |
| gpio3_12      | General-Purpose Input/Output | IO   | W9   |
| gpio3_13      | General-Purpose Input/Output | IO   | U8   |
| gpio3_14      | General-Purpose Input/Output | IO   | W8   |
| gpio3_15      | General-Purpose Input/Output | IO   | U7   |
| gpio3_16      | General-Purpose Input/Output | IO   | V7   |
| gpio3_17      | General-Purpose Input/Output | IO   | B19  |
| gpio3_18      | General-Purpose Input/Output | IO   | B17  |
| gpio3_19      | General-Purpose Input/Output | IO   | C16  |
| gpio3_20      | General-Purpose Input/Output | IO   | C17  |
| gpio3_21      | General-Purpose Input/Output | IO   | E16  |
| gpio3_22      | General-Purpose Input/Output | IO   | D16  |
| gpio3_23      | General-Purpose Input/Output | IO   | E17  |
| gpio3_24      | General-Purpose Input/Output | IO   | F17  |
| gpio3_25      | General-Purpose Input/Output | IO   | B18  |
| gpio3_26      | General-Purpose Input/Output | IO   | C18  |
| gpio3_27      | General-Purpose Input/Output | IO   | A19  |
| gpio3_28      | General-Purpose Input/Output | IO   | B20  |
| gpio3_29      | General-Purpose Input/Output | IO   | C20  |
| gpio3_30      | General-Purpose Input/Output | IO   | A20  |
| gpio3_31      | General-Purpose Input/Output | IO   | M1   |
| <b>GPIO 4</b> |                              |      |      |
| gpio4_0       | General-Purpose Input/Output | IO   | M2   |
| gpio4_1       | General-Purpose Input/Output | IO   | U6   |
| gpio4_2       | General-Purpose Input/Output | IO   | T5   |
| gpio4_3       | General-Purpose Input/Output | IO   | R6   |
| gpio4_4       | General-Purpose Input/Output | IO   | R5   |
| gpio4_5       | General-Purpose Input/Output | IO   | L1   |
| gpio4_6       | General-Purpose Input/Output | IO   | N4   |
| gpio4_7       | General-Purpose Input/Output | IO   | R7   |
| gpio4_8       | General-Purpose Input/Output | IO   | L2   |
| gpio4_9       | General-Purpose Input/Output | IO   | N5   |
| gpio4_10      | General-Purpose Input/Output | IO   | N6   |
| gpio4_11      | General-Purpose Input/Output | IO   | W7   |
| gpio4_12      | General-Purpose Input/Output | IO   | W6   |
| gpio4_13      | General-Purpose Input/Output | IO   | F13  |

**表 4-20. GPIOs Signal Descriptions (continued)**

| SIGNAL NAME             | DESCRIPTION                  | TYPE | BALL |
|-------------------------|------------------------------|------|------|
| gpio4_14                | General-Purpose Input/Output | IO   | E14  |
| gpio4_15                | General-Purpose Input/Output | IO   | F14  |
| gpio4_16                | General-Purpose Input/Output | IO   | C14  |
| gpio4_17                | General-Purpose Input/Output | IO   | D14  |
| gpio4_18                | General-Purpose Input/Output | IO   | D15  |
| gpio4_19                | General-Purpose Input/Output | IO   | F15  |
| gpio4_20                | General-Purpose Input/Output | IO   | F16  |
| gpio4_21                | General-Purpose Input/Output | IO   | M17  |
| gpio4_22                | General-Purpose Input/Output | IO   | M18  |
| gpio4_25                | General-Purpose Input/Output | IO   | J1   |
| gpio4_26                | General-Purpose Input/Output | IO   | J4   |
| gpio4_27                | General-Purpose Input/Output | IO   | J6   |
| gpio4_28 <sup>(1)</sup> | General-Purpose Input/Output | IO   | H1   |
| gpio4_29 <sup>(1)</sup> | General-Purpose Input/Output | IO   | H2   |

(1) gpio4\_28 is multiplexed with EMU0 and gpio4\_29 is multiplexed with EMU1. These pins will be sampled at reset release by the test and emulation logic. Therefore, if they are used as GPIO pins, they must return to the high state whenever the device enters reset. This can be controlled by logic driven from rstoutn. After the device exits reset (indicated by rstoutn rising), these can return to GPIO mode.

#### 4.3.20 ePWM

注: For more information, see Pulse Width Modulation Subsystem (PWMSS) section of the Device TRM.

**表 4-21. PWM Signal Descriptions**

| SIGNAL NAME            | DESCRIPTION                      | TYPE | BALL                   |
|------------------------|----------------------------------|------|------------------------|
| <b>PWMSS1</b>          |                                  |      |                        |
| ehrpwm1A               | EHRPWM1 Output A                 | O    | D12, D14, L1           |
| ehrpwm1B               | EHRPWM1 Output B                 | O    | D15, E12, L2           |
| ehrpwm1_tripzone_input | EHRPWM1 Trip Zone Input          | IO   | F12, R5                |
| eCAP1_in_PWM1_out      | ECAP1 Capture Input / PWM Output | IO   | A5, AB15, D16, F16, N4 |
| ehrpwm1_synci          | EHRPWM1 Sync Input               | I    | A10, F14               |
| ehrpwm1_synco          | EHRPWM1 Sync Output              | O    | B10, C14               |

#### 4.3.21 ATL

注: For more information, see the Audio Tracking Logic (ATL) section of the Device TRM.

**表 4-22. ATL Signal Descriptions**

| SIGNAL NAME | DESCRIPTION                  | TYPE | BALL |
|-------------|------------------------------|------|------|
| atl_clk0    | Audio Tracking Logic Clock 0 | O    | U9   |
| atl_clk1    | Audio Tracking Logic Clock 1 | O    | F21  |

#### 4.3.22 Test Interfaces

注: For more information, see the On-Chip Debug Support section of the Device TRM.

表 4-23. Debug Signal Descriptions

| SIGNAL NAME         | DESCRIPTION                                                                          | TYPE | BALL |
|---------------------|--------------------------------------------------------------------------------------|------|------|
| rtck                | JTAG return clock                                                                    | O    | J6   |
| tclk                | JTAG test clock                                                                      | I    | J2   |
| tdi                 | JTAG test data                                                                       | I    | J1   |
| tdo                 | JTAG test port data                                                                  | O    | J4   |
| tms                 | JTAG test port mode select. An external pullup resistor should be used on this ball. | IO   | J3   |
| trstn               | JTAG test reset                                                                      | I    | J5   |
| emu0 <sup>(1)</sup> | Emulator pin 0                                                                       | IO   | H1   |
| emu1 <sup>(1)</sup> | Emulator pin 1                                                                       | IO   | H2   |
| emu2                | Emulator pin 2                                                                       | O    | AA15 |
| emu3                | Emulator pin 3                                                                       | O    | AB15 |
| emu4                | Emulator pin 4                                                                       | O    | AA14 |
| emu5                | Emulator pin 5                                                                       | O    | AB14 |
| emu6                | Emulator pin 6                                                                       | O    | U13  |
| emu7                | Emulator pin 7                                                                       | O    | V13  |
| emu8                | Emulator pin 8                                                                       | O    | Y13  |
| emu9                | Emulator pin 9                                                                       | O    | W13  |
| emu10               | Emulator pin 10                                                                      | O    | U11  |
| emu11               | Emulator pin 11                                                                      | O    | V11  |
| emu12               | Emulator pin 12                                                                      | O    | U9   |
| emu13               | Emulator pin 13                                                                      | O    | W11  |
| emu14               | Emulator pin 14                                                                      | O    | V9   |
| emu15               | Emulator pin 15                                                                      | O    | W9   |
| emu16               | Emulator pin 16                                                                      | O    | U8   |
| emu17               | Emulator pin 17                                                                      | O    | W8   |
| emu18               | Emulator pin 18                                                                      | O    | U7   |
| emu19               | Emulator pin 19                                                                      | O    | V7   |

(1) EMU0 and EMU1 are multiplexed with GPIO. These pins will be sampled at reset release by the test and emulation logic. Therefore, if they are used as GPIO pins, they must return to the high state whenever the device enters reset. This can be controlled by logic driven from rstoutn. After the device exits reset (indicated by rstoutn rising), these can return to GPIO mode.

### 4.3.23 System and Miscellaneous

#### 4.3.23.1 Sysboot

注: For more information, see the Initialization (ROM Code) section of the Device TRM.

表 4-24. Sysboot Signal Descriptions

| SIGNAL NAME | DESCRIPTION                                                                                                                                | TYPE | BALL |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------|------|------|
| sysboot0    | Boot Mode Configuration 0. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I    | E8   |
| sysboot1    | Boot Mode Configuration 1. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I    | A7   |
| sysboot2    | Boot Mode Configuration 2. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I    | F8   |
| sysboot3    | Boot Mode Configuration 3. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I    | B7   |
| sysboot4    | Boot Mode Configuration 4. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I    | A6   |

**表 4-24. Sysboot Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION                                                                                                                                 | TYPE | BALL |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------|------|------|
| sysboot5    | Boot Mode Configuration 5. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.  | I    | F7   |
| sysboot6    | Boot Mode Configuration 6. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.  | I    | E7   |
| sysboot7    | Boot Mode Configuration 7. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.  | I    | R7   |
| sysboot8    | Boot Mode Configuration 8. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.  | I    | B6   |
| sysboot9    | Boot Mode Configuration 9. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.  | I    | A5   |
| sysboot10   | Boot Mode Configuration 10. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I    | D6   |
| sysboot11   | Boot Mode Configuration 11. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I    | C5   |
| sysboot12   | Boot Mode Configuration 12. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I    | B5   |
| sysboot13   | Boot Mode Configuration 13. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I    | D7   |
| sysboot14   | Boot Mode Configuration 14. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I    | B4   |
| sysboot15   | Boot Mode Configuration 15. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I    | A4   |

#### 4.3.23.2 Power, Reset and Clock Management (PRCM)

注: For more information, see Power, Reset, and Clock Management section of the Device TRM.

**表 4-25. PRCM Signal Descriptions**

| SIGNAL NAME | DESCRIPTION                                                                                                                                                                                                                                                                                                                                        | TYPE | BALL                    |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------------------------|
| clkout0     | Device Clock output 1. Can be used externally for devices with non-critical timing requirements, or for debug, or as a reference clock on GPMC as described in 表 5-32, GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - 1 Load and 表 5-34, GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - 5 Loads. | O    | AB17, C12, F14, F22, M1 |
| clkout1     | Device Clock output 2. Can be used as a system clock for other devices.                                                                                                                                                                                                                                                                            | O    | F12, F21, U17           |
| clkout2     | Device Clock output 3. Can be used as a system clock for other devices.                                                                                                                                                                                                                                                                            | O    | A10, F20, W17           |
| rstoutn     | Reset out (Active low). This pin asserts low in response to any global reset condition on the device.                                                                                                                                                                                                                                              | O    | F4                      |
| resetn      | Device Reset Input                                                                                                                                                                                                                                                                                                                                 | I    | G4                      |
| porz        | Power on Reset (active low). This pin must be asserted low until all device supplies are valid (see reset sequence/requirements).                                                                                                                                                                                                                  | I    | G3                      |
| xref_clk0   | External Reference Clock 0. For Audio and other Peripherals.                                                                                                                                                                                                                                                                                       | I    | M1                      |
| xref_clk1   | External Reference Clock 1. For Audio and other Peripherals.                                                                                                                                                                                                                                                                                       | I    | F14, F15                |
| xref_clk2   | External Reference Clock 2. For Audio and other Peripherals.                                                                                                                                                                                                                                                                                       | I    | H19                     |
| xi_osc0     | System Oscillator OSC0 Crystal input / LVCMOS clock input. Functions as the input connection to a crystal when the internal oscillator OSC0 is used. Functions as an LVCMOS-compatible input clock when an external oscillator is used.                                                                                                            | I    | E22                     |
| xi_osc1     | Auxiliary Oscillator OSC1 Crystal input / LVCMOS clock input. Functions as the input connection to a crystal when the internal oscillator OSC1 is used. Functions as an LVCMOS-compatible input clock when an external oscillator is used                                                                                                          | I    | B21                     |
| xo_osc0     | System Oscillator OSC0 Crystal output                                                                                                                                                                                                                                                                                                              | O    | D22                     |
| xo_osc1     | Auxiliary Oscillator OSC1 Crystal output                                                                                                                                                                                                                                                                                                           | O    | C21                     |

#### 4.3.23.3 Enhanced Direct Memory Access (EDMA)

注: For more information, see the DMA Controllers / Enhanced DMA section of the Device TRM.

表 4-26. EDMA Signal Descriptions

| SIGNAL NAME | DESCRIPTION                | TYPE | BALL     |
|-------------|----------------------------|------|----------|
| dma_evt1    | Enhanced DMA Event Input 1 | I    | C12, K17 |
| dma_evt2    | Enhanced DMA Event Input 2 | I    | D12, K19 |
| dma_evt3    | Enhanced DMA Event Input 3 | I    | E12      |
| dma_evt4    | Enhanced DMA Event Input 4 | I    | F12, D8  |

#### 4.3.23.4 Interrupt Controllers (INTC)

注: For more information, see the Interrupt Controllers section of the Device TRM.

表 4-27. INTC Signal Descriptions

| SIGNAL NAME | DESCRIPTION                                                                                                                             | TYPE | BALL     |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------|------|----------|
| nmin        | Non maskable interrupt input - active-low. This pin can be optionally routed to the DSP NMI input or as generic input to the Arm cores. | I    | G5       |
| sys_nirq1   | External interrupt event to any device INTC                                                                                             | I    | K18, K22 |
| sys_nirq2   | External interrupt event to any device INTC                                                                                             | I    | J17, K21 |

#### 4.3.24 Power Supplies

注: For more information, see Power, Reset, and Clock Management / PRCM Subsystem Environment / External Voltage Inputs section of the Device TRM.

表 4-28. Power Supply Signal Descriptions

| SIGNAL NAME  | DESCRIPTION                                             | TYPE | BALL                                                                                                                                                                                                                      |
|--------------|---------------------------------------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| vdd          | Core voltage domain supply                              | PWR  | H7, H12, H13, J10, J11, J15, K12, L12, L15, N12, N16, P10, P14                                                                                                                                                            |
| vss          | Ground                                                  | GND  | A1, A8, A17, A22, B22, E1, G10, G16, H8, H9, H10, H11, H15, H16, J22, K1, K9, K10, K11, K13, K14, K15, K16, M10, M11, M12, M13, M16, N7, N10, P1, P15, P16, R9, R12, R16, T14, V22, AB1, AB2, AB7, AB12, AB16, AB21, AB22 |
| vdd_dspeve   | DSP-EVE voltage domain supply                           | PWR  | K8, L8, M9, P8, P9, P11, P12                                                                                                                                                                                              |
| vdda_per     | PER PLL and PER HSDIVIDER analog power supply           | PWR  | H14                                                                                                                                                                                                                       |
| vdda_ddr_dsp | EVE PLL, DPLL_DDR and DDR HSDIVIDER analog power supply | PWR  | N8                                                                                                                                                                                                                        |

**表 4-28. Power Supply Signal Descriptions (continued)**

| SIGNAL NAME                      | DESCRIPTION                                                                       | TYPE | BALL                   |
|----------------------------------|-----------------------------------------------------------------------------------|------|------------------------|
| vdda_gmac_core                   | GMAC PLL, GMAC HSDIVIDER, DPLL_CORE and CORE HSDIVIDER analog power supply        | PWR  | M8                     |
| vdda_osc                         | IO supply for oscillator section                                                  | PWR  | E21                    |
| vssa_osc0                        | OSC0 analog ground                                                                | GND  | D21                    |
| vssa_osc1                        | OSC1 analog ground                                                                | GND  | C22                    |
| vdda_csi                         | CSI analog power supply                                                           | PWR  | A14                    |
| vssa_csi                         | CSI analog ground                                                                 | GND  | B14                    |
| vdda_dac                         | DAC analog power supply                                                           | PWR  | U19                    |
| vssa_dac                         | DAC analog ground                                                                 | GND  | T19                    |
| vdda_adc                         | ADC analog power supply                                                           | PWR  | P22                    |
| vssa_adc                         | ADC analog ground                                                                 | GND  | P21                    |
| vdds18v                          | 1.8V power supply and Power Group bias supply                                     | PWR  | G12, J7, L16, P13, T11 |
| vdds18v_ddr1                     | 1.8v bias supply for Byte0, Byte2, ECC Byte, Addr Cmd                             | PWR  | P7, T9                 |
| vdds18v_ddr2                     | 1.8v bias supply for Addr Cmd                                                     | PWR  | G7                     |
| vdds18v_ddr3                     | 1.8v bias supply for Byte1, Byte3                                                 | PWR  | T16, V21               |
| vdds_ddr1                        | IO power supply for Byte0, Byte2, ECC Byte, Addr Cmd                              | PWR  | R1, T7, T8, AA1, AB6   |
| vdds_ddr2                        | IO power supply for Addr Cmd                                                      | PWR  | C2, E2, G6             |
| vdds_ddr3                        | IO power supply for Byte1, Byte3                                                  | PWR  | T15, AA22, AB19        |
| vddshv1                          | Dual Voltage (1.8V or 3.3V) power supply for the GENERAL Power Group pins         | PWR  | K2, K7, L7, M7         |
| vddshv2                          | Dual Voltage (1.8V or 3.3V) power supply for the GPMC Power Group pins            | PWR  | G8, G9, G11, B8        |
| vddshv3                          | Dual Voltage (1.8V or 3.3V) power supply for the UART1 and UART2 Power Group pins | PWR  | G14                    |
| vddshv4                          | Dual Voltage (1.8V or 3.3V) power supply for the RGMII Power Group pins           | PWR  | A18, E20               |
| vddshv5                          | Dual Voltage (1.8V or 3.3V) power supply for the VIN1 Power Group pins            | PWR  | H17, J16, J21          |
| vddshv6                          | Dual Voltage (1.8V or 3.3V) power supply for the VOUT1 Power Group pins           | PWR  | T10, T12, T13, AA16    |
| cap_vddram_core1 <sup>(1)</sup>  | SRAM array supply for core voltage domain memories                                | CAP  | N15                    |
| cap_vddram_core2 <sup>(1)</sup>  | SRAM array supply for core voltage domain memories                                | CAP  | M15                    |
| cap_vddram_dspeve <sup>(1)</sup> | SRAM array supply for DSP-EVE memories                                            | CAP  | M14                    |

(1) This pin must always be connected via a 1-uF capacitor to vss.

4.4 Pin Multiplexing

表 4-29 describes the device pin multiplexing (no characteristics are provided in this table).

注: 表 4-29, *Pin Multiplexing* doesn't take into account subsystem multiplexing signals. Subsystem multiplexing signals are described in 4.3, *Signal Descriptions*.

注: For more information, see the Control Module / Control Module Functional Description / Pad Configuration Registers section of the Device TRM.

注: Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration (Hi-Z mode is not an input signal).

注: When a pad is set into a pin multiplexing mode which is not defined, that pad's behavior is undefined. This should be avoided.

注: In some cases 表 4-29 may present more than one signal per muxmode for the same ball. First signal in the list is the dominant function as selected via CTRL\_CORE\_PAD\_\* register.

All other signals are virtual functions that present alternate multiplexing options. This virtual functions are controlled via CTRL\_CORE\_ALT\_SELECT\_MUX or CTRL\_CORE\_VIP\_MUX\_SELECT register. For more information on how to use this options, please refer to Device TRM, Chapter *Control Module*, Section *Pad Configuration Registers*.

注意

The IO timings provided in Section 5.9, *Timing Requirements and Switching Characteristics* are only valid if signals within a single IOSET are used. The IOSETs are defined in the corresponding tables.

表 4-29. Pin Multiplexing

| ADDRESS | REGISTER NAME | BALL<br>NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|---------|---------------|----------------|-----------------------------------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|
|         |               |                | 0                                             | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 14 | 15 |
|         |               | E22            | xi_osc0                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | N2             | ddr1_a7                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |

表 4-29. Pin Multiplexing (continued)

| ADDRESS | REGISTER NAME | BALL<br>NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|---------|---------------|----------------|-----------------------------------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|
|         |               |                | 0                                             | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 14 | 15 |
|         |               | AB4            | ddr1_d4                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | W1             | ddr1_dqs2                                     |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | U3             | ddr1_d20                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | C1             | ddr1_a1                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | M19            | adc_in0                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | U1             | ddr1_a9                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | Y6             | ddr1_d7                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | A15            | csi2_0_dx3                                    |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | V1             | ddr1_a15                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AA2            | ddr1_d17                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | T1             | ddr1_a8                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | R3             | ddr1_a11                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AA3            | ddr1_d16                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | Y1             | ddr1_d23                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | Y17            | ddr1_d14                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AA20           | ddr1_dqs1                                     |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AA6            | ddr1_d0                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | F3             | ddr1_cke0                                     |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | Y20            | ddr1_dqsn1                                    |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | N21            | adc_in5                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | T2             | ddr1_a6                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | W2             | ddr1_dqsn2                                    |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | E3             | ddr1_wen                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | P18            | adc_in7                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AA11           | ddr1_ecc_d<br>2                               |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | B3             | ddr1_ba0                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | T17            | cvideo_tvout                                  |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | W22            | ddr1_d30                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | B21            | xi_osc1                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | V3             | ddr1_d21                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | T20            | ddr1_d25                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | A11            | csi2_0_dx0                                    |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | G2             | ddr1_nck                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | U21            | ddr1_d24                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | Y9             | ddr1_ecc_d<br>3                               |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | R21            | ddr1_d26                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | U4             | ddr1_a0                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |

表 4-29. Pin Multiplexing (continued)

| ADDRESS | REGISTER NAME | BALL<br>NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|---------|---------------|----------------|-----------------------------------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|
|         |               |                | 0                                             | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 14 | 15 |
|         |               | AB18           | ddr1_d15                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | A3             | ddr1_ba1                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | D2             | ddr1_ba2                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | B15            | csi2_0_dy3                                    |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AA21           | ddr1_d10                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AA8            | ddr1_d1                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | B13            | csi2_0_dy2                                    |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AB8            | ddr1_dqm0                                     |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | M22            | adc_in3                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | D1             | ddr1_a10                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | Y3             | ddr1_d18                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | C21            | xo_osc1                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | M20            | adc_in1                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | R22            | ddr1_d28                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AA9            | ddr1_ecc_d<br>6                               |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | N3             | ddr1_a5                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | P2             | ddr1_odt0                                     |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | T4             | ddr1_a4                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AB10           | ddr1_dqsn_<br>ecc                             |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AB3            | ddr1_dqm2                                     |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AA12           | ddr1_ecc_d<br>1                               |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AA4            | ddr1_d6                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | T18            | cvideo_rset                                   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | N22            | adc_in4                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | R4             | ddr1_a3                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | V20            | ddr1_d29                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AB13           | ddr1_dqm_e<br>cc                              |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AA5            | ddr1_dqs0                                     |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | A16            | csi2_0_dx4                                    |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | R2             | ddr1_a14                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | Y2             | ddr1_d22                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | Y21            | ddr1_d9                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | W21            | ddr1_dqm3                                     |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | P20            | adc_vrefp                                     |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | Y5             | ddr1_d5                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | F2             | ddr1_casn                                     |   |   |   |   |   |   |   |   |   |    |    |    |    |    |

表 4-29. Pin Multiplexing (continued)

| ADDRESS | REGISTER NAME | BALL<br>NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|---------|---------------|----------------|-----------------------------------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|
|         |               |                | 0                                             | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 14 | 15 |
|         |               | AB20           | ddr1_d13                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | B11            | csi2_0_dy0                                    |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AB9            | ddr1_ecc_d7                                   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | D22            | xo_osc0                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | U2             | ddr1_a12                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | P19            | adc_in6                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AA18           | ddr1_d8                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | U22            | ddr1_d31                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | Y18            | ddr1_dqm1                                     |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | A13            | csi2_0_dx2                                    |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | T22            | ddr1_dqsn3                                    |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | G1             | ddr1_ck                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | P17            | cvideo_vfb                                    |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | G3             | porz                                          |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | T21            | ddr1_dqs3                                     |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | Y22            | ddr1_d11                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AA19           | ddr1_d12                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AB5            | ddr1_dqsn0                                    |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | U20            | ddr1_d27                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AA13           | ddr1_ecc_d4                                   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | B16            | csi2_0_dy4                                    |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | F1             | ddr1_rasn                                     |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | D3             | ddr1_a2                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AA10           | ddr1_dqs_ecc                                  |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AA7            | ddr1_d3                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | B2             | ddr1_csn0                                     |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | N1             | ddr1_rst                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | V2             | ddr1_d19                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | Y8             | ddr1_d2                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | B12            | csi2_0_dy1                                    |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | C3             | ddr1_a13                                      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | A12            | csi2_0_dx1                                    |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | AB11           | ddr1_ecc_d5                                   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | M21            | adc_in2                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|         |               | Y11            | ddr1_ecc_d0                                   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |

表 4-29. Pin Multiplexing (continued)

| ADDRESS | REGISTER NAME                | BALL<br>NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) |              |             |        |           |                            |         |          |   |   |    |    |    |          |                                 |
|---------|------------------------------|----------------|-----------------------------------------------|--------------|-------------|--------|-----------|----------------------------|---------|----------|---|---|----|----|----|----------|---------------------------------|
|         |                              |                | 0                                             | 1            | 2           | 3      | 4         | 5                          | 6       | 7        | 8 | 9 | 10 | 11 | 12 | 14       | 15                              |
| 0x1400  | CTRL_CORE_PAD_GPMC_CLK       | C12            | gpmc_clk                                      | rgmii1_txc   |             |        |           |                            | clkout0 | dma_evt1 |   |   |    |    |    | gpio1_0  | Driver off                      |
| 0x1404  | CTRL_CORE_PAD_GPMC_BEN0      | D12            | gpmc_ben0                                     | rgmii1_txctl |             |        |           | ehrpwm1A                   |         | dma_evt2 |   |   |    |    |    | gpio1_1  | Driver off                      |
| 0x1408  | CTRL_CORE_PAD_GPMC_BEN1      | E12            | gpmc_ben1                                     | rgmii1_txd3  |             |        |           | ehrpwm1B                   |         | dma_evt3 |   |   |    |    |    | gpio1_2  | Driver off                      |
| 0x140C  | CTRL_CORE_PAD_GPMC_ADV_N_ALE | F12            | gpmc_adv_n_ale                                | rgmii1_txd2  |             |        |           | ehrpwm1_tri<br>pzone_input | clkout1 | dma_evt4 |   |   |    |    |    | gpio1_3  | Driver off                      |
| 0x1410  | CTRL_CORE_PAD_GPMC_OEN_REN   | A10            | gpmc_oen_ren                                  | rgmii1_txd1  |             |        |           | ehrpwm1_syn<br>nci         | clkout2 |          |   |   |    |    |    | gpio1_4  | Driver off                      |
| 0x1414  | CTRL_CORE_PAD_GPMC_WEN       | B10            | gpmc_wen                                      | rgmii1_txd0  |             |        |           | ehrpwm1_syn<br>nco         |         |          |   |   |    |    |    | gpio1_5  | Driver off                      |
| 0x1418  | CTRL_CORE_PAD_GPMC_CS0       | C10            | gpmc_cs0                                      | rgmii1_rxctl |             |        |           |                            |         |          |   |   |    |    |    | gpio1_6  | Driver off                      |
| 0x141C  | CTRL_CORE_PAD_GPMC_CS1       | E10            | gpmc_cs1                                      | qspi1_cs0    |             |        |           |                            |         |          |   |   |    |    |    | gpio1_7  | Driver off                      |
| 0x1420  | CTRL_CORE_PAD_GPMC_CS2       | D10            | gpmc_cs2                                      | qspi1_d3     |             |        |           |                            |         |          |   |   |    |    |    | gpio1_8  | Driver off                      |
| 0x1424  | CTRL_CORE_PAD_GPMC_CS3       | A9             | gpmc_cs3                                      | qspi1_d2     |             |        |           |                            |         |          |   |   |    |    |    | gpio1_9  | Driver off                      |
| 0x1428  | CTRL_CORE_PAD_GPMC_CS4       | B9             | gpmc_cs4                                      | qspi1_d0     |             |        |           |                            |         |          |   |   |    |    |    | gpio1_10 | Driver off                      |
| 0x142C  | CTRL_CORE_PAD_GPMC_CS5       | F10            | gpmc_cs5                                      | qspi1_d1     |             |        |           |                            |         |          |   |   |    |    |    | gpio1_11 | Driver off                      |
| 0x1430  | CTRL_CORE_PAD_GPMC_CS6       | C8             | gpmc_cs6                                      | qspi1_sclk   |             |        |           |                            |         |          |   |   |    |    |    | gpio1_12 | Driver off                      |
| 0x1434  | CTRL_CORE_PAD_GPMC_WAIT0     | D8             | gpmc_wait0                                    | rgmii1_rxd3  | qspi1_rtclk |        |           |                            |         | dma_evt4 |   |   |    |    |    | gpio1_13 | Driver off                      |
| 0x1438  | CTRL_CORE_PAD_GPMC_AD0       | E8             | gpmc_ad0                                      | rgmii1_rxd2  |             |        |           |                            |         |          |   |   |    |    |    | gpio1_14 | sysboot0                        |
| 0x143C  | CTRL_CORE_PAD_GPMC_AD1       | A7             | gpmc_ad1                                      | rgmii1_rxd1  |             |        |           |                            |         |          |   |   |    |    |    | gpio1_15 | sysboot1                        |
| 0x1440  | CTRL_CORE_PAD_GPMC_AD2       | F8             | gpmc_ad2                                      | rgmii1_rxd0  |             |        |           |                            |         |          |   |   |    |    |    | gpio1_16 | sysboot2                        |
| 0x1444  | CTRL_CORE_PAD_GPMC_AD3       | B7             | gpmc_ad3                                      | qspi1_rtclk  |             |        |           |                            |         |          |   |   |    |    |    | gpio1_17 | sysboot3                        |
| 0x1448  | CTRL_CORE_PAD_GPMC_AD4       | A6             | gpmc_ad4                                      | cam_strobe   |             |        |           |                            |         |          |   |   |    |    |    | gpio1_18 | sysboot4                        |
| 0x144C  | CTRL_CORE_PAD_GPMC_AD5       | F7             | gpmc_ad5                                      |              | uart2_txd   | timer6 | spi3_d1   |                            |         |          |   |   |    |    |    | gpio1_19 | sysboot5<br>mcasp2_acl<br>lkx   |
| 0x1450  | CTRL_CORE_PAD_GPMC_AD6       | E7             | gpmc_ad6                                      |              | uart2_rxd   | timer5 | spi3_d0   |                            |         |          |   |   |    |    |    | gpio1_20 | sysboot6<br>mcasp2_fsx          |
| 0x1454  | CTRL_CORE_PAD_GPMC_AD7       | C6             | gpmc_ad7                                      | cam_shutter  |             | timer4 | spi3_sclk |                            |         |          |   |   |    |    |    | gpio1_21 | Driver off<br>mcasp2_ahc<br>lkx |

**表 4-29. Pin Multiplexing (continued)**

| ADDRESS | REGISTER NAME              | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*(3:0)) |            |            |                   |          |   |   |   |   |   |    |    |    |          |                        |
|---------|----------------------------|-------------|-----------------------------------------------|------------|------------|-------------------|----------|---|---|---|---|---|----|----|----|----------|------------------------|
|         |                            |             | 0                                             | 1          | 2          | 3                 | 4        | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 14       | 15                     |
| 0x1458  | CTRL_CORE_PAD_GPMC_AD8     | B6          | gpmc_ad8                                      |            |            | timer7            | spi3_cs0 |   |   |   |   |   |    |    |    | gpio1_22 | sysboot8 mcas2_aclkr   |
| 0x145C  | CTRL_CORE_PAD_GPMC_AD9     | A5          | gpmc_ad9                                      |            |            | eCAP1_in_PWM1_out | spi3_cs1 |   |   |   |   |   |    |    |    | gpio1_23 | sysboot9 mcas2_fsr     |
| 0x1460  | CTRL_CORE_PAD_GPMC_AD10    | D6          | gpmc_ad10                                     |            |            | timer2            |          |   |   |   |   |   |    |    |    | gpio1_24 | sysboot10 mcas2_axr0   |
| 0x1464  | CTRL_CORE_PAD_GPMC_AD11    | C5          | gpmc_ad11                                     |            |            | timer3            |          |   |   |   |   |   |    |    |    | gpio1_25 | sysboot11 mcas2_axr1   |
| 0x1468  | CTRL_CORE_PAD_GPMC_AD12    | B5          | gpmc_ad12                                     |            |            |                   |          |   |   |   |   |   |    |    |    | gpio1_26 | sysboot12 mcas2_axr2   |
| 0x146C  | CTRL_CORE_PAD_GPMC_AD13    | D7          | gpmc_ad13                                     | rgmii1_rxc |            |                   |          |   |   |   |   |   |    |    |    | gpio1_27 | sysboot13 mcas2_axr3   |
| 0x1470  | CTRL_CORE_PAD_GPMC_AD14    | B4          | gpmc_ad14                                     |            |            |                   | spi2_cs1 |   |   |   |   |   |    |    |    | gpio1_28 | sysboot14 mcas2_axr4   |
| 0x1474  | CTRL_CORE_PAD_GPMC_AD15    | A4          | gpmc_ad15                                     |            |            |                   | spi2_cs0 |   |   |   |   |   |    |    |    | gpio1_29 | sysboot15 mcas2_axr5   |
| 0x1478  | CTRL_CORE_PAD_VIN1A_CLK0   | F22         | vin1a_clk0                                    | cpi_pclk   |            |                   | clkout0  |   |   |   |   |   |    |    |    | gpio1_30 | Driver off mcas3_aclkx |
| 0x147C  | CTRL_CORE_PAD_VIN1A_DE0    | F21         | vin1a_de0                                     | cpi_hsync  | vin1b_clk1 |                   | clkout1  |   |   |   |   |   |    |    |    | gpio1_31 | Driver off atl_clk1    |
| 0x1480  | CTRL_CORE_PAD_VIN1A_FLD0   | F20         | vin1a_fld0                                    | cpi_vsync  | vin2b_clk1 |                   | clkout2  |   |   |   |   |   |    |    |    | gpio2_0  | Driver off mcas3_aclkr |
| 0x1484  | CTRL_CORE_PAD_VIN1A_HSYNC0 | F19         | vin1a_hsync0                                  | cpi_data0  | vin1a_de0  |                   |          |   |   |   |   |   |    |    |    | gpio2_1  | Driver off mcas3_fsr   |
| 0x1488  | CTRL_CORE_PAD_VIN1A_VSYNC0 | G19         | vin1a_vsync0                                  | cpi_data1  |            |                   |          |   |   |   |   |   |    |    |    | gpio2_2  | Driver off mcas3_axr0  |
| 0x148C  | CTRL_CORE_PAD_VIN1A_D0     | G18         | vin1a_d0                                      | cpi_data2  |            |                   |          |   |   |   |   |   |    |    |    | gpio2_3  | Driver off mcas3_axr1  |
| 0x1490  | CTRL_CORE_PAD_VIN1A_D1     | G21         | vin1a_d1                                      | cpi_data3  |            |                   |          |   |   |   |   |   |    |    |    | gpio2_4  | Driver off mcas3_axr2  |
| 0x1494  | CTRL_CORE_PAD_VIN1A_D2     | G22         | vin1a_d2                                      | cpi_data4  |            |                   |          |   |   |   |   |   |    |    |    | gpio2_5  | Driver off mcas3_axr3  |
| 0x1498  | CTRL_CORE_PAD_VIN1A_D3     | H18         | vin1a_d3                                      | cpi_data5  |            |                   |          |   |   |   |   |   |    |    |    | gpio2_6  | Driver off mcas3_axr4  |
| 0x149C  | CTRL_CORE_PAD_VIN1A_D4     | H20         | vin1a_d4                                      | cpi_data6  |            |                   |          |   |   |   |   |   |    |    |    | gpio2_7  | Driver off mcas3_axr5  |

表 4-29. Pin Multiplexing (continued)

| ADDRESS | REGISTER NAME             | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) |                  |              |          |                 |           |          |           |   |            |    |    |    |          |                                |
|---------|---------------------------|-------------|-----------------------------------------------|------------------|--------------|----------|-----------------|-----------|----------|-----------|---|------------|----|----|----|----------|--------------------------------|
|         |                           |             | 0                                             | 1                | 2            | 3        | 4               | 5         | 6        | 7         | 8 | 9          | 10 | 11 | 12 | 14       | 15                             |
| 0x14A0  | CTRL_CORE_PAD_VIN1A_D5    | H19         | vin1a_d5                                      | cpi_data7        |              |          |                 |           |          |           |   |            |    |    |    | gpio2_8  | xref_clk2<br>mcasp3_ahc<br>lkx |
| 0x14A4  | CTRL_CORE_PAD_VIN1A_D6    | H22         | vin1a_d6                                      | cpi_data8        |              |          |                 |           |          |           |   |            |    |    |    | gpio2_9  | Driver off<br>mcasp3_fsx       |
| 0x14A8  | CTRL_CORE_PAD_VIN1A_D7    | H21         | vin1a_d7                                      | cpi_data9        |              |          |                 |           |          |           |   |            |    |    |    | gpio2_10 | Driver off                     |
| 0x14AC  | CTRL_CORE_PAD_VIN1A_D8    | J17         | vin1a_d8                                      | cpi_data10       | vin1b_d0     | gpmc_a8  |                 |           |          | sys_nirq2 |   |            |    |    |    | gpio2_11 | Driver off                     |
| 0x14B0  | CTRL_CORE_PAD_VIN1A_D9    | K22         | vin1a_d9                                      | cpi_data11       | vin1b_d1     | gpmc_a9  |                 |           |          | sys_nirq1 |   |            |    |    |    | gpio2_12 | Driver off                     |
| 0x14B4  | CTRL_CORE_PAD_VIN1A_D10   | K21         | vin1a_d10                                     | cpi_data12       | vin1b_d2     | gpmc_a10 |                 |           |          | sys_nirq2 |   |            |    |    |    | gpio2_13 | Driver off                     |
| 0x14B8  | CTRL_CORE_PAD_VIN1A_D11   | K18         | vin1a_d11                                     | cpi_data13       | vin1b_d3     | gpmc_a11 |                 |           |          | sys_nirq1 |   |            |    |    |    | gpio2_14 | Driver off                     |
| 0x14BC  | CTRL_CORE_PAD_VIN1A_D12   | K17         | vin1a_d12                                     | cpi_data14       | vin1b_d4     | gpmc_a12 |                 |           | dma_evt1 |           |   |            |    |    |    | gpio2_15 | Driver off                     |
| 0x14C0  | CTRL_CORE_PAD_VIN1A_D13   | K19         | vin1a_d13                                     | cpi_wen          | vin1b_d5     | gpmc_a13 |                 |           | dma_evt2 |           |   |            |    |    |    | gpio2_16 | Driver off                     |
| 0x14C4  | CTRL_CORE_PAD_VIN1A_D14   | K20         | vin1a_d14                                     | cpi_fid          | vin1b_d6     | gpmc_a14 |                 |           |          |           |   |            |    |    |    | gpio2_17 | Driver off                     |
| 0x14C8  | CTRL_CORE_PAD_VIN1A_D15   | L21         | vin1a_d15                                     | cpi_data15       | vin1b_d7     | gpmc_a15 |                 |           |          |           |   |            |    |    |    | gpio2_18 | Driver off                     |
| 0x14CC  | CTRL_CORE_PAD_VIN2A_CLK0  | L22         | vin2a_clk0                                    |                  |              |          |                 |           |          |           |   |            |    |    |    | gpio2_19 | Driver off                     |
| 0x14D0  | CTRL_CORE_PAD_VIN2A_DE0   | M17         | vin2a_de0                                     | cam_strobe       | vin2b_hsync1 |          |                 | vin2b_de1 |          |           |   |            |    |    |    | gpio4_21 | Driver off                     |
| 0x14D4  | CTRL_CORE_PAD_VIN2A_FLD0  | M18         | vin2a_fld0                                    | cam_shutter      | vin2b_vsync1 |          |                 |           |          |           |   |            |    |    |    | gpio4_22 | Driver off                     |
| 0x14D8  | CTRL_CORE_PAD_VOUT1_CLK   | AB17        | vout1_clk                                     |                  | vin1a_d12    |          | clkout0         |           |          |           |   | vin2a_clk0 |    |    |    | gpio2_20 | Driver off                     |
| 0x14DC  | CTRL_CORE_PAD_VOUT1_DE    | U17         | vout1_de                                      | mcasp1_acl<br>kx | vin1a_d13    |          | clkout1         |           |          |           |   |            |    |    |    | gpio2_21 | Driver off                     |
| 0x14E0  | CTRL_CORE_PAD_VOUT1_FLD   | W17         | vout1_fld                                     | mcasp1_fsx       | vin1a_d14    |          | clkout2         |           |          |           |   |            |    |    |    | gpio2_22 | Driver off                     |
| 0x14E4  | CTRL_CORE_PAD_VOUT1_HSYNC | AA17        | vout1_hsync                                   | mcasp1_acl<br>kr | vin1a_d15    |          |                 |           |          |           |   | vin2a_de0  |    |    |    | gpio2_23 | Driver off                     |
| 0x14E8  | CTRL_CORE_PAD_VOUT1_VSYNC | U16         | vout1_vsync                                   | mcasp1_fsr       |              |          |                 |           |          |           |   | vin2a_fld0 |    |    |    | gpio2_24 | Driver off                     |
| 0x14EC  | CTRL_CORE_PAD_VOUT1_D0    | W16         | vout1_d0                                      | mcasp1_axr<br>0  |              |          |                 | mmc_clk   |          |           |   |            |    |    |    | gpio2_25 | Driver off                     |
| 0x14F0  | CTRL_CORE_PAD_VOUT1_D1    | V16         | vout1_d1                                      | mcasp1_axr<br>1  |              |          |                 | mmc_cmd   |          |           |   |            |    |    |    | gpio2_26 | Driver off                     |
| 0x14F4  | CTRL_CORE_PAD_VOUT1_D2    | U15         | vout1_d2                                      | mcasp1_axr<br>2  |              |          | mcasp1_axr<br>8 | mmc_dat0  |          |           |   |            |    |    |    | gpio2_27 | Driver off                     |
| 0x14F8  | CTRL_CORE_PAD_VOUT1_D3    | V15         | vout1_d3                                      | mcasp1_axr<br>3  |              |          | mcasp1_axr<br>9 | mmc_dat1  |          |           |   |            |    |    |    | gpio2_28 | Driver off                     |

**表 4-29. Pin Multiplexing (continued)**

| ADDRESS | REGISTER NAME           | BALL<br>NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) |                |           |          |                   |              |          |       |   |   |            |    |    |    |          |                              |
|---------|-------------------------|----------------|-----------------------------------------------|----------------|-----------|----------|-------------------|--------------|----------|-------|---|---|------------|----|----|----|----------|------------------------------|
|         |                         |                | 0                                             | 1              | 2         | 3        | 4                 | 5            | 6        | 7     | 8 | 9 | 10         | 11 | 12 | 14 | 15       |                              |
| 0x14FC  | CTRL_CORE_PAD_VOUT1_D4  | Y15            | vout1_d4                                      | mcasp1_axr4    |           |          |                   | mcasp1_axr10 | mmc_dat2 |       |   |   |            |    |    |    | gpio2_29 | Driver off                   |
| 0x1500  | CTRL_CORE_PAD_VOUT1_D5  | W15            | vout1_d5                                      | mcasp1_axr5    |           |          |                   | mcasp1_axr11 | mmc_dat3 |       |   |   | vin2a_clk0 |    |    |    | gpio2_30 | Driver off                   |
| 0x1504  | CTRL_CORE_PAD_VOUT1_D6  | AA15           | vout1_d6                                      | mcasp1_axr6    |           |          |                   | mcasp1_axr12 |          | emu2  |   |   | vin2a_de0  |    |    |    | gpio2_31 | Driver off                   |
| 0x1508  | CTRL_CORE_PAD_VOUT1_D7  | AB15           | vout1_d7                                      | mcasp1_axr7    |           |          | eCAP1_in_PWM1_out | mcasp1_axr13 |          | emu3  |   |   | vin2a_fld0 |    |    |    | gpio3_0  | Driver off                   |
| 0x150C  | CTRL_CORE_PAD_VOUT1_D8  | AA14           | vout1_d8                                      | mcasp1_axr8    | vin2a_d0  | gpmc_a20 |                   |              |          | emu4  |   |   |            |    |    |    | gpio3_1  | Driver off                   |
| 0x1510  | CTRL_CORE_PAD_VOUT1_D9  | AB14           | vout1_d9                                      | mcasp1_axr9    | vin2a_d1  | gpmc_a21 |                   |              |          | emu5  |   |   |            |    |    |    | gpio3_2  | Driver off                   |
| 0x1514  | CTRL_CORE_PAD_VOUT1_D10 | U13            | vout1_d10                                     | mcasp1_axr10   | vin2a_d2  | gpmc_a22 |                   |              |          | emu6  |   |   |            |    |    |    | gpio3_3  | Driver off                   |
| 0x1518  | CTRL_CORE_PAD_VOUT1_D11 | V13            | vout1_d11                                     | mcasp1_axr11   | vin2a_d3  | gpmc_a23 |                   |              |          | emu7  |   |   |            |    |    |    | gpio3_4  | Driver off                   |
| 0x151C  | CTRL_CORE_PAD_VOUT1_D12 | Y13            | vout1_d12                                     | mcasp1_axr12   | vin2a_d4  | gpmc_a24 |                   |              |          | emu8  |   |   |            |    |    |    | gpio3_5  | Driver off<br>mcasp2_ahc_lkx |
| 0x1520  | CTRL_CORE_PAD_VOUT1_D13 | W13            | vout1_d13                                     | mcasp1_axr13   | vin2a_d5  | gpmc_a25 |                   |              |          | emu9  |   |   |            |    |    |    | gpio3_6  | Driver off<br>mcasp2_acl_kr  |
| 0x1524  | CTRL_CORE_PAD_VOUT1_D14 | U11            | vout1_d14                                     | mcasp1_axr14   | vin2a_d6  | gpmc_a26 |                   |              |          | emu10 |   |   |            |    |    |    | gpio3_7  | Driver off<br>mcasp2_acl_kx  |
| 0x1528  | CTRL_CORE_PAD_VOUT1_D15 | V11            | vout1_d15                                     | mcasp1_axr15   | vin2a_d7  | gpmc_a27 |                   |              |          | emu11 |   |   |            |    |    |    | gpio3_8  | Driver off<br>mcasp2_fsx     |
| 0x152C  | CTRL_CORE_PAD_VOUT1_D16 | U9             | vout1_d16                                     | mcasp1_ahc_lkx | vin2a_d8  | gpmc_a0  | mcasp1_axr8       | vin2b_d0     | emu12    |       |   |   |            |    |    |    | gpio3_9  | Driver off<br>atl_clk0       |
| 0x1530  | CTRL_CORE_PAD_VOUT1_D17 | W11            | vout1_d17                                     |                | vin2a_d9  | gpmc_a1  | mcasp1_axr9       | vin2b_d1     | emu13    |       |   |   |            |    |    |    | gpio3_10 | Driver off<br>mcasp2_fsr     |
| 0x1534  | CTRL_CORE_PAD_VOUT1_D18 | V9             | vout1_d18                                     |                | vin2a_d10 | gpmc_a2  | mcasp1_axr10      | vin2b_d2     | emu14    |       |   |   |            |    |    |    | gpio3_11 | Driver off<br>mcasp2_axr0    |
| 0x1538  | CTRL_CORE_PAD_VOUT1_D19 | W9             | vout1_d19                                     |                | vin2a_d11 | gpmc_a3  | mcasp1_axr11      | vin2b_d3     | emu15    |       |   |   |            |    |    |    | gpio3_12 | Driver off<br>mcasp2_axr1    |
| 0x153C  | CTRL_CORE_PAD_VOUT1_D20 | U8             | vout1_d20                                     |                | vin2a_d12 | gpmc_a4  | mcasp1_axr12      | vin2b_d4     | emu16    |       |   |   |            |    |    |    | gpio3_13 | Driver off<br>mcasp2_axr2    |
| 0x1540  | CTRL_CORE_PAD_VOUT1_D21 | W8             | vout1_d21                                     |                | vin2a_d13 | gpmc_a5  | mcasp1_axr13      | vin2b_d5     | emu17    |       |   |   |            |    |    |    | gpio3_14 | Driver off<br>mcasp2_axr3    |
| 0x1544  | CTRL_CORE_PAD_VOUT1_D22 | U7             | vout1_d22                                     |                | vin2a_d14 | gpmc_a6  | mcasp1_axr14      | vin2b_d6     | emu18    |       |   |   |            |    |    |    | gpio3_15 | Driver off<br>mcasp2_axr4    |
| 0x1548  | CTRL_CORE_PAD_VOUT1_D23 | V7             | vout1_d23                                     |                | vin2a_d15 | gpmc_a7  | mcasp1_axr15      | vin2b_d7     | emu19    |       |   |   |            |    |    |    | gpio3_16 | Driver off<br>mcasp2_axr5    |

表 4-29. Pin Multiplexing (continued)

| ADDRESS | REGISTER NAME              | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) |            |              |                   |           |          |            |                            |           |   |    |    |    |          |            |
|---------|----------------------------|-------------|-----------------------------------------------|------------|--------------|-------------------|-----------|----------|------------|----------------------------|-----------|---|----|----|----|----------|------------|
|         |                            |             | 0                                             | 1          | 2            | 3                 | 4         | 5        | 6          | 7                          | 8         | 9 | 10 | 11 | 12 | 14       | 15         |
| 0x154C  | CTRL_CORE_PAD_MCAN_TX      | W7          | mcan_tx                                       | vin2a_de0  | vin2a_hsync0 | spi1_cs2          | uart3_rxd |          | gpmc_wait1 | vin1b_hsync1               | vin1b_de1 |   |    |    |    | gpio4_11 | Driver off |
| 0x1550  | CTRL_CORE_PAD_MCAN_RX      | W6          | mcan_rx                                       | cam_nreset | vin2a_vsync0 | spi1_cs3          | uart3_txd | gpmc_cs7 |            | vin1b_vsync1               |           |   |    |    |    | gpio4_12 | Driver off |
| 0x1554  | CTRL_CORE_PAD_MDIO_MCLK    | B19         | mdio_mclk                                     |            |              |                   | spi4_d1   |          |            |                            |           |   |    |    |    | gpio3_17 | Driver off |
| 0x1558  | CTRL_CORE_PAD_MDIO_D       | B17         | mdio_d                                        |            |              |                   | spi4_d0   |          |            |                            |           |   |    |    |    | gpio3_18 | Driver off |
| 0x155C  | CTRL_CORE_PAD_RGMII0_TXC   | C16         | rgmii0_txc                                    |            |              | cam_strobe        | spi4_sclk | mmc_clk  |            |                            |           |   |    |    |    | gpio3_19 | Driver off |
| 0x1560  | CTRL_CORE_PAD_RGMII0_TXCTL | C17         | rgmii0_txctl                                  |            |              | cam_shutter       | spi4_cs0  | mmc_cmd  |            |                            |           |   |    |    |    | gpio3_20 | Driver off |
| 0x1564  | CTRL_CORE_PAD_RGMII0_TXD3  | E16         | rgmii0_txd3                                   |            |              |                   |           | mmc_dat0 |            |                            |           |   |    |    |    | gpio3_21 | Driver off |
| 0x1568  | CTRL_CORE_PAD_RGMII0_TXD2  | D16         | rgmii0_txd2                                   |            |              | eCAP1_in_PWM1_out |           | mmc_dat1 |            |                            |           |   |    |    |    | gpio3_22 | Driver off |
| 0x156C  | CTRL_CORE_PAD_RGMII0_TXD1  | E17         | rgmii0_txd1                                   |            |              |                   |           | mmc_dat2 |            |                            |           |   |    |    |    | gpio3_23 | Driver off |
| 0x1570  | CTRL_CORE_PAD_RGMII0_TXD0  | F17         | rgmii0_txd0                                   |            |              |                   |           | mmc_dat3 |            |                            |           |   |    |    |    | gpio3_24 | Driver off |
| 0x1574  | CTRL_CORE_PAD_RGMII0_RXC   | B18         | rgmii0_rxc                                    |            |              | cam_strobe        |           | mmc_clk  |            |                            |           |   |    |    |    | gpio3_25 | Driver off |
| 0x1578  | CTRL_CORE_PAD_RGMII0_RXCTL | C18         | rgmii0_rxctl                                  |            |              | cam_shutter       |           | mmc_cmd  |            |                            |           |   |    |    |    | gpio3_26 | Driver off |
| 0x157C  | CTRL_CORE_PAD_RGMII0_RXD3  | A19         | rgmii0_rxd3                                   |            |              |                   |           | mmc_dat0 |            |                            |           |   |    |    |    | gpio3_27 | Driver off |
| 0x1580  | CTRL_CORE_PAD_RGMII0_RXD2  | B20         | rgmii0_rxd2                                   |            |              |                   |           | mmc_dat1 |            |                            |           |   |    |    |    | gpio3_28 | Driver off |
| 0x1584  | CTRL_CORE_PAD_RGMII0_RXD1  | C20         | rgmii0_rxd1                                   |            |              |                   |           | mmc_dat2 |            |                            |           |   |    |    |    | gpio3_29 | Driver off |
| 0x1588  | CTRL_CORE_PAD_RGMII0_RXD0  | A20         | rgmii0_rxd0                                   |            |              |                   |           | mmc_dat3 |            |                            |           |   |    |    |    | gpio3_30 | Driver off |
| 0x158C  | CTRL_CORE_PAD_XREF_CLK0    | M1          | xref_clk0                                     | clkout0    |              |                   | spi3_cs0  | spi2_cs1 | spi1_cs0   | spi1_cs1                   |           |   |    |    |    | gpio3_31 | Driver off |
| 0x1590  | CTRL_CORE_PAD_SPI1_SCLK    | M2          | spi1_sclk                                     | uart3_rxd  |              |                   |           |          |            |                            |           |   |    |    |    | gpio4_0  | Driver off |
| 0x1594  | CTRL_CORE_PAD_SPI1_D1      | U6          | spi1_d1                                       | uart3_ctsn |              |                   |           |          |            |                            |           |   |    |    |    | gpio4_1  | Driver off |
| 0x1598  | CTRL_CORE_PAD_SPI1_D0      | T5          | spi1_d0                                       | uart3_rtsn |              |                   |           |          |            |                            |           |   |    |    |    | gpio4_2  | Driver off |
| 0x159C  | CTRL_CORE_PAD_SPI1_CS0     | R6          | spi1_cs0                                      | uart3_txd  |              |                   |           |          |            |                            |           |   |    |    |    | gpio4_3  | Driver off |
| 0x15A0  | CTRL_CORE_PAD_SPI1_CS1     | R5          | spi1_cs1                                      | spi3_cs1   |              |                   | timer6    |          |            | ehrpwm1_tri<br>pzone_input |           |   |    |    |    | gpio4_4  | Driver off |
| 0x15A4  | CTRL_CORE_PAD_SPI2_SCLK    | L1          | spi2_sclk                                     | uart3_rxd  | ehrpwm1A     | timer3            |           |          |            |                            |           |   |    |    |    | gpio4_5  | Driver off |
| 0x15A8  | CTRL_CORE_PAD_SPI2_D1      | N4          | spi2_d1                                       | uart3_ctsn |              | timer5            |           |          |            | eCAP1_in_PWM1_out          |           |   |    |    |    | gpio4_6  | Driver off |

**表 4-29. Pin Multiplexing (continued)**

| ADDRESS | REGISTER NAME            | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) |                   |           |          |           |             |        |                  |             |              |          |          |          |          |            |
|---------|--------------------------|-------------|-----------------------------------------------|-------------------|-----------|----------|-----------|-------------|--------|------------------|-------------|--------------|----------|----------|----------|----------|------------|
|         |                          |             | 0                                             | 1                 | 2         | 3        | 4         | 5           | 6      | 7                | 8           | 9            | 10       | 11       | 12       | 14       | 15         |
| 0x15AC  | CTRL_CORE_PAD_SPI2_D0    | R7          | spi2_d0                                       | uart3_rtsn        |           | timer1   |           |             |        |                  |             |              |          |          |          | gpio4_7  | sysboot7   |
| 0x15B0  | CTRL_CORE_PAD_SPI2_CS0   | L2          | spi2_cs0                                      | uart3_txd         | ehrpwm1B  | timer4   |           |             |        |                  |             |              |          |          |          | gpio4_8  | Driver off |
| 0x15B8  | CTRL_CORE_PAD_DCAN1_RX   | N6          | dcan1_rx                                      |                   |           |          |           |             |        |                  |             |              |          |          |          | gpio4_10 | Driver off |
| 0x15B4  | CTRL_CORE_PAD_DCAN1_TX   | N5          | dcan1_tx                                      |                   |           |          |           |             |        |                  |             |              |          |          |          | gpio4_9  | Driver off |
| 0x15BC  | CTRL_CORE_PAD_UART1_RXD  | F13         | uart1_rxd                                     |                   |           |          | spi4_d1   | qspi1_rtclk |        |                  |             |              | gpmc_a12 |          | mcan_tx  | gpio4_13 | Driver off |
| 0x15C0  | CTRL_CORE_PAD_UART1_TXD  | E14         | uart1_txd                                     |                   |           |          | spi4_d0   |             |        |                  |             |              | gpmc_a13 |          | mcan_rx  | gpio4_14 | Driver off |
| 0x15C4  | CTRL_CORE_PAD_UART1_CTSN | F14         | uart1_ctsn                                    | xref_clk1         | uart3_rxd | gpmc_a16 | spi4_sclk | spi1_cs2    | timer3 | ehrpwm1_syncl    | clkout0     | vin2a_hsync0 | gpmc_a12 | gpmc_clk | dcan1_tx | gpio4_15 | Driver off |
| 0x15C8  | CTRL_CORE_PAD_UART1_RTSN | C14         | uart1_rtsn                                    |                   | uart3_txd | gpmc_a17 | spi4_cs0  | spi1_cs3    | timer4 | ehrpwm1_synconco | qspi1_rtclk | vin2a_vsync0 | gpmc_a13 |          | dcan1_rx | gpio4_16 | Driver off |
| 0x15CC  | CTRL_CORE_PAD_UART2_RXD  | D14         | uart2_rxd                                     |                   |           |          | spi3_d1   |             | timer1 | ehrpwm1A         |             |              | gpmc_clk | gpmc_a12 | dcan1_tx | gpio4_17 | Driver off |
| 0x15D0  | CTRL_CORE_PAD_UART2_TXD  | D15         | uart2_txd                                     |                   |           |          | spi3_d0   |             | timer2 | ehrpwm1B         |             |              |          | gpmc_a13 | dcan1_rx | gpio4_18 | Driver off |
| 0x15D4  | CTRL_CORE_PAD_UART2_CTSN | F15         | uart2_ctsn                                    |                   | xref_clk1 | gpmc_a18 | spi3_sclk | qspi1_cs1   | timer7 |                  |             | vin2a_hsync0 | gpmc_clk |          | mcan_tx  | gpio4_19 | Driver off |
| 0x15D8  | CTRL_CORE_PAD_UART2_RTSN | F16         | uart2_rtsn                                    | eCAP1_in_PWM1_out |           | gpmc_a19 | spi3_cs0  |             | timer8 |                  |             | vin2a_vsync0 |          |          | mcan_rx  | gpio4_20 | Driver off |
| 0x15DC  | CTRL_CORE_PAD_I2C1_SDA   | L4          | i2c1_sda                                      |                   |           |          |           |             |        |                  |             |              |          |          |          |          |            |
| 0x15E0  | CTRL_CORE_PAD_I2C1_SCL   | L3          | i2c1_scl                                      |                   |           |          |           |             |        |                  |             |              |          |          |          |          |            |
| 0x15E4  | CTRL_CORE_PAD_I2C2_SDA   | L5          | i2c2_sda                                      |                   |           |          |           |             |        |                  |             |              |          |          |          |          |            |
| 0x15E8  | CTRL_CORE_PAD_I2C2_SCL   | L6          | i2c2_scl                                      |                   |           |          |           |             |        |                  |             |              |          |          |          |          |            |
| 0x15EC  | CTRL_CORE_PAD_TMS        | J3          | tms                                           |                   |           |          |           |             |        |                  |             |              |          |          |          |          |            |
| 0x15F0  | CTRL_CORE_PAD_TDI        | J1          | tdi                                           |                   |           |          |           |             |        |                  |             |              |          |          |          | gpio4_25 | Driver off |
| 0x15F4  | CTRL_CORE_PAD_TDO        | J4          | tdo                                           |                   |           |          |           |             |        |                  |             |              |          |          |          | gpio4_26 | Driver off |
| 0x15F8  | CTRL_CORE_PAD_TCLK       | J2          | tclk                                          |                   |           |          |           |             |        |                  |             |              |          |          |          |          |            |
| 0x15FC  | CTRL_CORE_PAD_TRSTN      | J5          | trstn                                         |                   |           |          |           |             |        |                  |             |              |          |          |          |          |            |
| 0x1600  | CTRL_CORE_PAD_RTCK       | J6          | rtck                                          |                   |           |          |           |             |        |                  |             |              |          |          |          | gpio4_27 | Driver off |
| 0x1604  | CTRL_CORE_PAD_EMU0       | H1          | emu0                                          |                   |           |          |           |             |        |                  |             |              |          |          |          | gpio4_28 | Driver off |
| 0x1608  | CTRL_CORE_PAD_EMU1       | H2          | emu1                                          |                   |           |          |           |             |        |                  |             |              |          |          |          | gpio4_29 | Driver off |

表 4-29. Pin Multiplexing (continued)

| ADDRESS | REGISTER NAME             | BALL<br>NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
|---------|---------------------------|----------------|-----------------------------------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|
|         |                           |                | 0                                             | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 14 | 15 |
| 0x160C  | CTRL_CORE_PAD_<br>RESETN  | G4             | resetn                                        |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
| 0x1610  | CTRL_CORE_PAD_<br>NMIN    | G5             | nmin                                          |   |   |   |   |   |   |   |   |   |    |    |    |    |    |
| 0x1614  | CTRL_CORE_PAD_<br>RSTOUTN | F4             | rstoutn                                       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |

1. NA in table stands for Not Applicable.

## 4.5 Connections for Unused Pins

This section describes the connection requirements of the unused and reserved balls.

注: The following balls are reserved: A2 / F6 / A21 / B1

These balls must be left unconnected.

注: All unused power supply balls must be supplied with the voltages specified in the [Section 5.4, Recommended Operating Conditions](#), unless alternative tie-off options are included in [4.3, Signal Descriptions](#).

**表 4-30. Unused Balls Specific Connection Requirements**

| Balls                                                               | Connection Requirements                                                                                     |
|---------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|
| B21 / E22 / J5 / AA10 / AA5 / AA20 / W1 / T21                       | These balls must be connected to GND through an external pull resistor if unused                            |
| J2 / G5 / G4 / L3 / L4 / AB10 / J3 / AB5 / Y20 / W2 / T22 / L6 / L5 | These balls must be connected to the corresponding power supply through an external pull resistor if unused |
| M19 / M20 / M21 / M22 / N22 / N21 / P19 / P18 / P20                 | These balls must be connected together to GND through a single external 10k-ohm resistor if unused.         |

注: All other unused signal balls **with** a Pad Configuration Register can be left unconnected with their internal pullup or pulldown resistor enabled.

注: All other unused signal balls **without** Pad Configuration Register can be left unconnected.

## 5 Specifications

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注: For more information, see Power, Reset and Clock Management / PRCM Subsystem Environment / External Voltage Inputs or Initialization / Preinitialization / Power Requirements section of the Device TRM.

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注: The index number 1 which is part of the EMIF1 signal prefixes (ddr1\_\*) listed in 4.3.8, *EMIF*, column "SIGNAL NAME" are not to be confused with DDR1 type of SDRAM memories.

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注: Audio Back End (ABE) module is not supported for this family of devices, but "ABE" name is still present in some clock or DPLL names.

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### 注意

All IO Cells are NOT Fail-safe compliant and should not be externally driven in absence of their IO supply.

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| PARAMETER <sup>(3)</sup>                           |                                                                                                                      |                                                                                         | MIN  | MAX                         | UNIT |
|----------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|------|-----------------------------|------|
| V <sub>SUPPLY</sub> (Steady-State)                 | Supply Voltage Ranges (Steady-State)                                                                                 | Core (vdd, vdd_dspeve)                                                                  | -0.3 | 1.5                         | V    |
|                                                    |                                                                                                                      | Analog (vdda_per, vdda_ddr_dsp, vdda_gmac_core, vdda_osc, vdda_csi, vdda_dac, vdda_adc) | -0.3 | 2.0                         | V    |
|                                                    |                                                                                                                      | vdds_ddr1, vdds_ddr2, vdds_ddr3 (1.35V mode)                                            | -0.3 | 1.65                        | V    |
|                                                    |                                                                                                                      | vdds_ddr1, vdds_ddr2, vdds_ddr3 (1.5V mode)                                             | -0.3 | 1.8                         | V    |
|                                                    |                                                                                                                      | vdds_ddr1, vdds_ddr2, vdds_ddr3 (1.8V mode)                                             | -0.3 | 2.1                         | V    |
|                                                    |                                                                                                                      | vdds18v, vdds18v_ddr1, vdds18v_ddr2, vdds18v_ddr3                                       | -0.3 | 2.1                         | V    |
|                                                    |                                                                                                                      | vddshv1-6 (1.8V mode)                                                                   | -0.3 | 2.1                         | V    |
|                                                    |                                                                                                                      | vddshv1-6 (3.3V mode)                                                                   | -0.3 | 3.8                         | V    |
| V <sub>IO</sub> (Steady-State)                     | Input and Output Voltage Ranges (Steady-State)                                                                       | Core I/Os                                                                               | -0.3 | 1.5                         | V    |
|                                                    |                                                                                                                      | Analog I/Os                                                                             | -0.3 | 2.0                         | V    |
|                                                    |                                                                                                                      | I/O 1.35V                                                                               | -0.3 | 1.65                        | V    |
|                                                    |                                                                                                                      | I/O 1.5V                                                                                | -0.3 | 1.8                         | V    |
|                                                    |                                                                                                                      | 1.8V I/Os                                                                               | -0.3 | 2.1                         | V    |
|                                                    |                                                                                                                      | 3.3V I/Os                                                                               | -0.3 | 3.8                         | V    |
| SR                                                 | Maximum slew rate, all supplies                                                                                      |                                                                                         |      | 10 <sup>5</sup>             | V/s  |
| V <sub>IO</sub> (Transient Overshoot / Undershoot) | Input and Output Voltage Ranges (Transient Overshoot / Undershoot)<br>Note: valid for up to 20% of the signal period |                                                                                         |      | 0.2×VDD <sup>(4)</sup>      | V    |
| T <sub>J</sub>                                     | Operating junction temperature range                                                                                 | Automotive                                                                              | -40  | +125                        | °C   |
| T <sub>STG</sub>                                   | Storage temperature range after soldered onto PC Board                                                               |                                                                                         | -55  | +150                        | °C   |
| Latch-up I-Test                                    | I-test <sup>(5)</sup> , All I/Os (if different levels then one line per level)                                       |                                                                                         | -100 | 100                         | mA   |
| Latch-up OV-Test                                   | Over-voltage Test <sup>(6)</sup> , All supplies (if different levels then one line per level)                        |                                                                                         | N/A  | 1.5×V <sub>supply max</sub> | V    |

(1) Stresses beyond those listed as absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under [Section 5.4, Recommended Operating Conditions](#), is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to VSS, unless otherwise noted.

(3) See I/Os supplied by this power pin in [Table 4-1 Pin Attributes](#).

(4) VDD is the voltage on the corresponding power-supply pin(s) for the IO.

(5) Per JEDEC JESD78 at 125°C with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.

(6) Per JEDEC JESD78 at 125°C.

## 5.2 ESD Ratings

|                                          |                                                         |                                  | VALUE | UNIT |
|------------------------------------------|---------------------------------------------------------|----------------------------------|-------|------|
| V <sub>ESD</sub> Electrostatic discharge | Human-Body model (HBM), per AEC Q100-002 <sup>(1)</sup> |                                  | ±1000 | V    |
|                                          | Charged-device model (CDM), per AEC Q100-011            | All pins                         | ±250  |      |
|                                          |                                                         | Corner pins (A1, AB1, A22, AB22) | ±750  |      |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Power on Hour (POH) Limits

| IP  | Duty Cycle | Voltage Domain | Voltage (V) (max) | Frequency (MHz) (max) | T <sub>J</sub> (°C)               | POH   |
|-----|------------|----------------|-------------------|-----------------------|-----------------------------------|-------|
| All | 100%       | All            | All Support OPPs  |                       | Automotive Profile <sup>(1)</sup> | 20000 |

## Power on Hour (POH) Limits (*continued*)

- (1) Automotive profile is defined as 20000 power on hours with junction temperature as follows: 5%@-40°C, 65%@70°C, 20%@110°C, 10%@125°C.

## 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                               | DESCRIPTION                                                                    | MIN <sup>(2)</sup> | NOM  | MAX DC <sup>(3)</sup> | MAX <sup>(2)</sup> | UNIT                |
|-----------------------------------------|--------------------------------------------------------------------------------|--------------------|------|-----------------------|--------------------|---------------------|
| <b>Input Power Supply Voltage Range</b> |                                                                                |                    |      |                       |                    |                     |
| vdd                                     | Core voltage domain supply                                                     | See 5.5            |      |                       |                    | V                   |
| vdd_dspeve                              | DSP-EVE voltage domain supply                                                  | See 5.5            |      |                       |                    | V                   |
| vdda_per                                | PER PLL and PER HSDIVIDER analog power supply                                  | 1.71               | 1.80 | 1.836                 | 1.89               | V                   |
|                                         | Maximum noise (peak-peak)                                                      |                    | 50   |                       |                    | mV <sub>PPmax</sub> |
| vdda_ddr_dsp                            | EVE PLL, DPLL_DDR and DDR HSDIVIDER analog power supply                        | 1.71               | 1.80 | 1.836                 | 1.89               | V                   |
|                                         | Maximum noise (peak-peak)                                                      |                    | 50   |                       |                    | mV <sub>PPmax</sub> |
| vdda_gmac_core                          | GMAC PLL, GMAC HSDIVIDER, DPLL_CORE and CORE HSDIVIDER analog power supply     | 1.71               | 1.80 | 1.836                 | 1.89               | V                   |
|                                         | Maximum noise (peak-peak)                                                      |                    | 50   |                       |                    | mV <sub>PPmax</sub> |
| vdda_osc                                | I/O supply for oscillator section                                              | 1.71               | 1.80 | 1.836                 | 1.89               | V                   |
|                                         | Maximum noise (peak-peak)                                                      |                    | 50   |                       |                    | mV <sub>PPmax</sub> |
| vdda_csi                                | CSI analog power supply                                                        | 1.71               | 1.80 | 1.836                 | 1.89               | V                   |
|                                         | Maximum noise (peak-peak)                                                      |                    | 50   |                       |                    | mV <sub>PPmax</sub> |
| vdda_dac                                | DAC analog power supply                                                        | 1.71               | 1.80 | 1.836                 | 1.89               | V                   |
|                                         | Maximum noise (peak-peak)                                                      |                    | 50   |                       |                    | mV <sub>PPmax</sub> |
| vdda_adc                                | ADC analog power supply                                                        | 1.71               | 1.80 | 1.836                 | 1.89               | V                   |
|                                         | Maximum noise (peak-peak)                                                      |                    | 50   |                       |                    | mV <sub>PPmax</sub> |
| vdds18v                                 | 1.8V power supply and Power Group bias supply                                  | 1.71               | 1.80 | 1.836                 | 1.89               | V                   |
|                                         | Maximum noise (peak-peak)                                                      |                    | 50   |                       |                    | mV <sub>PPmax</sub> |
| vdds18v_ddr1                            | 1.8v bias supply for Byte0, Byte2, ECC Byte, Addr Cmd                          | 1.71               | 1.80 | 1.836                 | 1.89               | V                   |
|                                         | Maximum noise (peak-peak)                                                      |                    | 50   |                       |                    | mV <sub>PPmax</sub> |
| vdds18v_ddr2                            | 1.8v bias supply for Addr Cmd                                                  | 1.71               | 1.80 | 1.836                 | 1.89               | V                   |
|                                         | Maximum noise (peak-peak)                                                      |                    | 50   |                       |                    | mV <sub>PPmax</sub> |
| vdds18v_ddr3                            | 1.8v bias supply for Byte1, Byte3                                              | 1.71               | 1.80 | 1.836                 | 1.89               | V                   |
|                                         | Maximum noise (peak-peak)                                                      |                    | 50   |                       |                    | mV <sub>PPmax</sub> |
| vdds_ddr1                               | EMIF power supply (1.8V for DDR2 mode / 1.5V for DDR3 mode / 1.35V DDR3L mode) | 1.35-V Mode        | 1.28 | 1.35                  | 1.377              | 1.42                |
|                                         |                                                                                | 1.5-V Mode         | 1.43 | 1.50                  | 1.53               | 1.57                |
|                                         |                                                                                | 1.8-V Mode         | 1.71 | 1.80                  | 1.836              | 1.89                |
|                                         | Maximum noise (peak-peak)                                                      | 1.35-V Mode        |      | 50                    |                    |                     |
|                                         |                                                                                | 1.5-V Mode         |      |                       |                    |                     |
|                                         |                                                                                | 1.8-V Mode         |      |                       |                    |                     |
| vdds_ddr2                               | EMIF power supply (1.8V for DDR2 mode / 1.5V for DDR3 mode / 1.35V DDR3L mode) | 1.35-V Mode        | 1.28 | 1.35                  | 1.377              | 1.42                |
|                                         |                                                                                | 1.5-V Mode         | 1.43 | 1.50                  | 1.53               | 1.57                |
|                                         |                                                                                | 1.8-V Mode         | 1.71 | 1.80                  | 1.836              | 1.89                |
|                                         | Maximum noise (peak-peak)                                                      | 1.35-V Mode        |      | 50                    |                    |                     |
|                                         |                                                                                | 1.5-V Mode         |      |                       |                    |                     |
|                                         |                                                                                | 1.8-V Mode         |      |                       |                    |                     |

## Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                     | DESCRIPTION                                                                       |             | MIN <sup>(2)</sup> |  | NOM  | MAX DC <sup>(3)</sup> | MAX <sup>(2)</sup> | UNIT                |
|-------------------------------|-----------------------------------------------------------------------------------|-------------|--------------------|--|------|-----------------------|--------------------|---------------------|
| vdds_ddr3                     | EMIF power supply (1.8V for DDR2 mode / 1.5V for DDR3 mode / 1.35V DDR3L mode)    | 1.35-V Mode | 1.28               |  | 1.35 | 1.377                 | 1.42               | V                   |
|                               |                                                                                   | 1.5-V Mode  | 1.43               |  | 1.50 | 1.53                  | 1.57               |                     |
|                               |                                                                                   | 1.8-V Mode  | 1.71               |  | 1.80 | 1.836                 | 1.89               |                     |
|                               | Maximum noise (peak-peak)                                                         | 1.35-V Mode |                    |  | 50   |                       |                    | mV <sub>PPmax</sub> |
|                               |                                                                                   | 1.5-V Mode  |                    |  |      |                       |                    |                     |
|                               |                                                                                   | 1.8-V Mode  |                    |  |      |                       |                    |                     |
| vddshv1                       | Dual Voltage (1.8V or 3.3V) power supply for the GENERAL Power Group pins         | 1.8-V Mode  | 1.71               |  | 1.80 | 1.836                 | 1.89               | V                   |
|                               |                                                                                   | 3.3-V Mode  | 3.135              |  | 3.30 | 3.366                 | 3.465              |                     |
|                               | Maximum noise (peak-peak)                                                         | 1.8-V Mode  |                    |  | 50   |                       |                    | mV <sub>PPmax</sub> |
|                               |                                                                                   | 3.3-V Mode  |                    |  |      |                       |                    |                     |
| vddshv2                       | Dual Voltage (1.8V or 3.3V) power supply for the GPMC Power Group pins            | 1.8-V Mode  | 1.71               |  | 1.80 | 1.836                 | 1.89               | V                   |
|                               |                                                                                   | 3.3-V Mode  | 3.135              |  | 3.30 | 3.366                 | 3.465              |                     |
|                               | Maximum noise (peak-peak)                                                         | 1.8-V Mode  |                    |  | 50   |                       |                    | mV <sub>PPmax</sub> |
|                               |                                                                                   | 3.3-V Mode  |                    |  |      |                       |                    |                     |
| vddshv3                       | Dual Voltage (1.8V or 3.3V) power supply for the UART1 and UART2 Power Group pins | 1.8-V Mode  | 1.71               |  | 1.80 | 1.836                 | 1.89               | V                   |
|                               |                                                                                   | 3.3-V Mode  | 3.135              |  | 3.30 | 3.366                 | 3.465              |                     |
|                               | Maximum noise (peak-peak)                                                         | 1.8-V Mode  |                    |  | 50   |                       |                    | mV <sub>PPmax</sub> |
|                               |                                                                                   | 3.3-V Mode  |                    |  |      |                       |                    |                     |
| vddshv4                       | Dual Voltage (1.8V or 3.3V) power supply for the RGMII Power Group pins           | 1.8-V Mode  | 1.71               |  | 1.80 | 1.836                 | 1.89               | V                   |
|                               |                                                                                   | 3.3-V Mode  | 3.135              |  | 3.30 | 3.366                 | 3.465              |                     |
|                               | Maximum noise (peak-peak)                                                         | 1.8-V Mode  |                    |  | 50   |                       |                    | mV <sub>PPmax</sub> |
|                               |                                                                                   | 3.3-V Mode  |                    |  |      |                       |                    |                     |
| vddshv5                       | Dual Voltage (1.8V or 3.3V) power supply for the VIN1 Power Group pins            | 1.8-V Mode  | 1.71               |  | 1.80 | 1.836                 | 1.89               | V                   |
|                               |                                                                                   | 3.3-V Mode  | 3.135              |  | 3.30 | 3.366                 | 3.465              |                     |
|                               | Maximum noise (peak-peak)                                                         | 1.8-V Mode  |                    |  | 50   |                       |                    | mV <sub>PPmax</sub> |
|                               |                                                                                   | 3.3-V Mode  |                    |  |      |                       |                    |                     |
| vddshv6                       | Dual Voltage (1.8V or 3.3V) power supply for the VOUT1 Power Group pins           | 1.8-V Mode  | 1.71               |  | 1.80 | 1.836                 | 1.89               | V                   |
|                               |                                                                                   | 3.3-V Mode  | 3.135              |  | 3.30 | 3.366                 | 3.465              |                     |
|                               | Maximum noise (peak-peak)                                                         | 1.8-V Mode  |                    |  | 50   |                       |                    | mV <sub>PPmax</sub> |
|                               |                                                                                   | 3.3-V Mode  |                    |  |      |                       |                    |                     |
| vss                           | Ground supply                                                                     |             | 0                  |  |      |                       |                    | V                   |
| vssa_osc0                     | OSC0 analog ground                                                                |             | 0                  |  |      |                       |                    | V                   |
| vssa_osc1                     | OSC1 analog ground                                                                |             | 0                  |  |      |                       |                    | V                   |
| vssa_csi                      | CSI analog ground supply                                                          |             | 0                  |  |      |                       |                    | V                   |
| vssa_dac                      | DAC analog ground supply                                                          |             | 0                  |  |      |                       |                    | V                   |
| vssa_adc                      | ADC analog ground supply                                                          |             | 0                  |  |      |                       |                    | V                   |
| T <sub>J</sub> <sup>(1)</sup> | Operating junction temperature range                                              | Automotive  | -40                |  |      |                       | 125 <sup>(4)</sup> | °C                  |

(1) Refer to Power on Hours table for limitations.

## Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

- (2) The voltage at the device ball should never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, etc.
- (3) The DC voltage at the device ball should never be above the MAX DC voltage to avoid impact on device reliability and lifetime POH (Power-On-Hours). The MAX DC voltage is defined as the highest allowed DC regulated voltage, without transients, seen at the ball.
- (4) The TSHUT feature of the SoC resets the device by default when one of the on-die temp sensors reports 123 °C. This is intended to protect the device from exceeding 125 °C. Though not recommended, the TSHUT temperature threshold can be modified in software if other mechanisms are in place to avoid exceeding 125 °C. Refer to the device TRM for details on the TSHUT feature.

## 5.5 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each OPP (operating performance point) for processor clocks and device core clocks.

表 5-1 describes the maximum supported frequency per speed grade for the devices.

**表 5-1. Speed Grade Maximum Frequency**

| DEVICE SPEED | MAXIMUM FREQUENCY (MHz) |     |       |     |                |               |     |
|--------------|-------------------------|-----|-------|-----|----------------|---------------|-----|
|              | DSP                     | EVE | IPU   | L3  | DDR3/DDR3L     | DDR2          | ADC |
| DRA78xxD     | 500                     | 500 | 212.8 | 266 | 532 (DDR-1066) | 400 (DDR-800) | 20  |
| DRA78xxR     | 750                     | 667 | 212.8 | 266 | 532 (DDR-1066) | 400 (DDR-800) | 20  |
| DRA78xxS     | 1000                    | 900 | 212.8 | 266 | 532 (DDR-1066) | 400 (DDR-800) | 20  |

### 5.5.1 AVS Requirements

Adaptive Voltage Scaling (AVS) is required on most of the vdd\_\* supplies as defined in 表 5-2.

**表 5-2. AVS Requirements per vdd\_\* Supply**

| SUPPLY     | AVS REQUIRED?     |
|------------|-------------------|
| vdd        | Yes, for all OPPs |
| vdd_dspeve | Yes, for all OPPs |

### 5.5.2 Voltage And Core Clock Specifications

表 5-3 shows the recommended OPP per voltage domain.

**表 5-3. Voltage Domains Operating Performance Points**

| DOMAIN      | CONDITION                                   | OPP_NOM                           |                            |                    | OPP_OD             |                    |                    | OPP_HIGH/OPP_PLUS <sup>(6)</sup> |                    |                       |                    |
|-------------|---------------------------------------------|-----------------------------------|----------------------------|--------------------|--------------------|--------------------|--------------------|----------------------------------|--------------------|-----------------------|--------------------|
|             |                                             | MIN <sup>(2)</sup>                | NOM <sup>(1)</sup>         | MAX <sup>(2)</sup> | MIN <sup>(2)</sup> | NOM <sup>(1)</sup> | MAX <sup>(2)</sup> | MIN <sup>(2)</sup>               | NOM <sup>(1)</sup> | MAX DC <sup>(3)</sup> | MAX <sup>(2)</sup> |
| VD_CORE (V) | BOOT (Before AVS is enabled) <sup>(4)</sup> | 1.02                              | 1.06                       | 1.11               | Not Applicable     |                    |                    | Not Applicable                   |                    |                       |                    |
|             | After AVS is enabled <sup>(4)</sup>         | AVS Voltage <sup>(5)</sup> – 3.5% | AVS Voltage <sup>(5)</sup> | 1.20               | Not Applicable     |                    |                    | Not Applicable                   |                    |                       |                    |

表 5-3. Voltage Domains Operating Performance Points (continued)

| DOMAIN           | CONDITION                                         | OPP_NOM                                    |                                  |                    | OPP_OD                                     |                                  |                                       | OPP_HIGH/OPP_PLUS <sup>(6)</sup>           |                                  |                                       |                                       |
|------------------|---------------------------------------------------|--------------------------------------------|----------------------------------|--------------------|--------------------------------------------|----------------------------------|---------------------------------------|--------------------------------------------|----------------------------------|---------------------------------------|---------------------------------------|
|                  |                                                   | MIN <sup>(2)</sup>                         | NOM <sup>(1)</sup>               | MAX <sup>(2)</sup> | MIN <sup>(2)</sup>                         | NOM <sup>(1)</sup>               | MAX <sup>(2)</sup>                    | MIN <sup>(2)</sup>                         | NOM <sup>(1)</sup>               | MAX DC <sup>(3)</sup>                 | MAX <sup>(2)</sup>                    |
| VD_DSPEVE<br>(V) | BOOT (Before<br>AVS is enabled)<br><sup>(4)</sup> | 1.02                                       | 1.06                             | 1.11               | Not Applicable                             |                                  |                                       | Not Applicable                             |                                  |                                       |                                       |
|                  | After AVS is<br>enabled <sup>(4)</sup>            | AVS<br>Voltage<br><sup>(5)</sup> –<br>3.5% | AVS<br>Voltage<br><sup>(5)</sup> | 1.11               | AVS<br>Voltage<br><sup>(5)</sup> –<br>3.5% | AVS<br>Voltage<br><sup>(5)</sup> | AVS<br>Voltage<br><sup>(5)</sup> + 5% | AVS<br>Voltage<br><sup>(5)</sup> –<br>3.5% | AVS<br>Voltage<br><sup>(5)</sup> | AVS<br>Voltage<br><sup>(5)</sup> + 2% | AVS<br>Voltage<br><sup>(5)</sup> + 5% |

(1) In a typical implementation, the power supply should target the NOM voltage.

(2) The voltage at the device ball should never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, etc.

(3) The DC voltage at the device ball should never be above the MAX DC voltage to avoid impact on device reliability and lifetime POH (Power-On-Hours). The MAX DC voltage is defined as the highest allowed DC regulated voltage, without transients, seen at the ball.

(4) For all OPPs, AVS must be enabled to avoid impact on device reliability, lifetime POH (Power-On-Hours), and device power.

(5) The AVS voltages are device-dependent, voltage domain-dependent, and OPP-dependent. They must be read from the STD\_FUSE\_OPP. For information about STD\_FUSE\_OPP Registers address, please refer to Control Module Section of the TRM. The power supply should be adjustable over the following ranges for each required OPP:

- OPP\_NOM: 0.85V - 1.06V
- OPP\_OD: 0.94V - 1.15V
- OPP\_HIGH: 1.05V - 1.25V
- OPP\_PLUS: 1.05V - 1.25V

The AVS Voltages will be within the above specified ranges.

(6) The required PRCM and DCC software configuration sequence for OPP\_PLUS (DSP 1 GHz or EVE 900 MHz) is different than other OPPs. For details refer to [DRA78x SoC for Automotive Infotainment Silicon Revision 2.0](#), section titled "PRCM Software Configuration for OPP\_PLUS".

表 5-4 describes the standard processor clocks speed characteristics vs OPP of the device.

表 5-4. Supported OPP vs Max Frequency<sup>(1)(2)</sup>

| DESCRIPTION      | OPP_NOM         | OPP_OD          | OPP_HIGH        | OPP_PLUS        |
|------------------|-----------------|-----------------|-----------------|-----------------|
|                  | MAX FREQ. (MHz) | MAX FREQ. (MHz) | MAX FREQ. (MHz) | MAX FREQ. (MHz) |
| <b>VD_DSPEVE</b> |                 |                 |                 |                 |
| DSP_CLK          | 500             | 709             | 750             | 1000            |
| EVE_FCLK         | 500             | 667             | 667             | 900             |
| <b>VD_CORE</b>   |                 |                 |                 |                 |
| CORE_IPU1_CLK    | 212.8           | N/A             | N/A             | N/A             |
| L3_CLK           | 266             | N/A             | N/A             | N/A             |
| DDR3 / DDR3L     | 532 (DDR-1066)  | N/A             | N/A             | N/A             |
| DDR2             | 400 (DDR-800)   | N/A             | N/A             | N/A             |
| ADC              | 20              | N/A             | N/A             | N/A             |

(1) N/A in this table stands for Not Applicable.

(2) Maximum supported frequency is limited according to the Device Speed Grade (see [表 5-1](#)).

### 5.5.3 Maximum Supported Frequency

Device modules either receive their clock directly from an external clock input, directly from a PLL, or from a PRCM. [表 5-5](#) lists the clock source options for each module on this device, along with the maximum frequency that module can accept. To ensure proper module functionality, the device PLLs and dividers must be programmed not to exceed the maximum frequencies listed in this table.

**表 5-5. Maximum Supported Frequency**

| Module              |                  |            |                          | Clock Sources       |                               |                         |
|---------------------|------------------|------------|--------------------------|---------------------|-------------------------------|-------------------------|
| Instance Name       | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name     | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| ADC                 | OCF_CLK          | Int        | 133                      | L4PER2_L3_GICLK     | CORE_X2_CLK                   | DPLL_CORE               |
|                     | ADC_CLK          | Func       | 20                       | ADC_CLK             | SYS_CLK1                      | OSC0                    |
|                     |                  |            |                          |                     | SYS_CLK2                      | OSC1                    |
|                     |                  |            |                          |                     | XREF_CLK0                     | xref_clk0               |
| ATL                 | ATL_ICLK_L3      | Int        | 266                      | ATL_L3_GICLK        | CORE_X2_CLK                   | DPLL_CORE               |
|                     | ATLPCLK          | Func       | 266                      | ATL_GFCLK           | CORE_X2_CLK                   | DPLL_CORE               |
|                     |                  |            |                          |                     | FUNC_32K_CLK                  | OSC1                    |
|                     |                  |            |                          |                     |                               | RTC Oscillator          |
| COUNTER_32K         | COUNTER_32K_FCLK | Func       | 0.032                    | FUNC_32K_CLK        | SYS_CLK1/610                  | OSC0                    |
|                     | COUNTER_32K_ICLK | Int        | 38.4                     | WKUPAON_GICLK       | SYS_CLK1                      | OSC0                    |
| CTRL_MODULE_BANDGAP | L3INSTR_TS_GCLK  | Int        | 5                        | L3INSTR_TS_GCLK     | SYS_CLK1                      | OSC0                    |
|                     |                  |            |                          |                     | ABE_LP_CLK                    | DPLL_DDR                |
| CTRL_MODULE_CORE    | L4CFG_L4_GICLK   | Int        | 133                      | L4_ICLK             | CORE_X2_CLK                   | DPLL_CORE               |
| CTRL_MODULE_WKUP    | WKUPAON_GICLK    | Int        | 38.4                     | WKUPAON_GICLK       | SYS_CLK1                      | OSC0                    |
|                     |                  |            |                          |                     | ABE_LP_CLK                    | DPLL_DDR                |
| DCAN1               | DCAN1_FCLK       | Func       | 20                       | DCAN1_SYS_CLK       | SYS_CLK1                      | OSC0                    |
|                     |                  |            |                          |                     | SYS_CLK2                      | OSC1                    |
|                     | DCAN1_ICLK       | Int        | 133                      | WKUPAON_GICLK       | SYS_CLK1                      | OSC0                    |
|                     |                  |            |                          |                     | ABE_LP_CLK                    | DPLL_DDR                |
| MCAN                | MCAN_FCLK        | Func       | 80                       | MCAN_CLK            | MCAN_CLK                      | DPLL_GMAC_DSP           |
|                     | MCAN_ICLK        | Int        | 133                      | L4PER2_L3_GICLK     | CORE_X2_CLK                   | DPLL_CORE               |
| DLL                 | EMIF_DLL_FCLK    | Func       | 266                      | EMIF_DLL_GCLK       | EMIF_DLL_GCLK                 | DPLL_DDR                |
| DSP1                | DSP1_FICLK       | Int & Func | DSP_CLK                  | DSP1_GFCLK          | DSP_GFCLK                     | DPLL_EVE_VID_DSP        |
|                     |                  |            |                          |                     |                               | DPLL_CORE               |
|                     |                  |            |                          |                     |                               | DPLL_GMAC_DSP           |
| DSP2                | DSP2_FICLK       | Int & Func | DSP_CLK                  | DSP2_GFCLK          | DSP_GFCLK                     | DPLL_EVE_VID_DSP        |
|                     |                  |            |                          |                     |                               | DPLL_CORE               |
|                     |                  |            |                          |                     |                               | DPLL_GMAC_DSP           |
| DSS                 | DSS_FCK_CLK      | Int & Func | 192                      | DSS_GFCLK           | DSS_GFCLK                     | DPLL_PER                |
|                     | DSS_VP_CLK       | Func       | 165                      | VID_PIX_CLK         | VID_PIX_CLK                   | DPLL_EVE_VID_DSP        |
| DSS DISPC           | DISPC_FCK_CLK    | Int & Func | 192                      | DSS_GFCLK           | DSS_GFCLK                     | DPLL_PER                |
|                     | DISPC_CLK1       | Int        | 165                      | VID_PIX_CLK         | VID_PIX_CLK                   | DPLL_EVE_VID_DSP        |
| EFUSE_CTRL_CUST     | ocp_clk          | Int        | 133                      | CUSTEFUSE_L4_GICLK  | CORE_X2_CLK                   | DPLL_CORE               |
|                     | sys_clk          | Func       | 38.4                     | CUSTEFUSE_SYS_GFCLK | SYS_CLK1                      | OSC0                    |
| ELM                 | ELM_ICLK         | Int        | 133                      | L4PER_L3_GICLK      | CORE_X2_CLK                   | DPLL_CORE               |
| EMIF_OCP_FW         | L3_CLK           | Int        | 266                      | EMIF_L3_GICLK       | CORE_X2_CLK                   | DPLL_CORE               |
|                     | L4_CLKEN         | Int        | 133                      | EMIF_L4_GICLK       | CORE_X2_CLK                   | DPLL_CORE               |
| EMIF_PHY            | EMIF_PHY_FCLK    | Func       | DDR                      | EMIF_PHY_GCLK       | EMIF_PHY_GCLK                 | DPLL_DDR                |
|                     | EMIF_DLL_FCLK    | Int        | 266                      | EMIF_DLL_GCLK       | -                             | DPLL_DDR                |

表 5-5. Maximum Supported Frequency (continued)

| Module          |                  |            |                          | Clock Sources     |                               |                         |
|-----------------|------------------|------------|--------------------------|-------------------|-------------------------------|-------------------------|
| Instance Name   | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name   | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| EMIF            | EMIF_ICLK        | Int        | 266                      | EMIF_L3_GICLK     | CORE_X2_CLK                   | DPLL_CORE               |
|                 | EMIF_L3_ICLK     | Int        | 266                      | L3_EOCP_GICLK     | -                             | -                       |
|                 | EMIF_FICLK       | Func       | DDR/2                    | EMIF_PHY_GCLK/2   | EMIF_PHY_GCLK                 | DPLL_DDR                |
| EVE             | EVE_FCLK         | Func       | EVE_FCLK                 | EVE_CLK           | EVE_GCLK                      | DPLL_CORE               |
|                 |                  |            |                          |                   |                               | DPLL_GMAC_DSP           |
|                 |                  |            |                          |                   | EVE_GFCLK                     | DPLL_EVE_VID_DSP        |
| GMAC_SW         | CPTS_RFT_CLK     | Func       | 266                      | GMAC_RFT_CLK      | L3_ICLK                       | DPLL_CORE               |
|                 |                  |            |                          |                   | SYS_CLK1                      | OSC0                    |
|                 | MAIN_CLK         | Int        | 125                      | GMAC_MAIN_CLK     | GMAC_250M_CLK                 | DPLL_GMAC_DSP           |
|                 | MHZ_250_CLK      | Func       | 250                      | GMII_250MHZ_CLK   | GMII_250MHZ_CLK               | DPLL_GMAC_DSP           |
|                 | MHZ_5_CLK        | Func       | 5                        | RGMII_5MHZ_CLK    | RMII_50MHZ_CLK/10             | DPLL_GMAC_DSP           |
|                 | MHZ_50_CLK       | Func       | 50                       | RMII_50MHZ_CLK    | GMAC_RMII_HS_CLK              | DPLL_GMAC_DSP           |
| GPIO1           | GPIO1_ICLK       | Int        | 38.4                     | WKUPAON_GICLK     | SYS_CLK1                      | OSC0                    |
|                 | GPIO1_DBCLK      | Func       | 0.032                    | WKUPAON_32K_GFCLK | SYS_CLK1/610                  | OSC0                    |
| GPIO2           | GPIO2_ICLK       | Int        | 133                      | L4PER_L3_GICLK    | CORE_X2_CLK                   | DPLL_CORE               |
|                 | GPIO2_DBCLK      | Func       | 0.032                    | FUNC_32K_CLK      | SYS_CLK1/610                  | OSC0                    |
| GPIO3           | GPIO3_ICLK       | Int        | 133                      | L4PER_L3_GICLK    | CORE_X2_CLK                   | DPLL_CORE               |
|                 | GPIO3_DBCLK      | Func       | 0.032                    | FUNC_32K_CLK      | SYS_CLK1/610                  | OSC0                    |
| GPIO4           | GPIO4_ICLK       | Int        | 133                      | L4PER_L3_GICLK    | CORE_X2_CLK                   | DPLL_CORE               |
|                 | GPIO4_DBCLK      | Func       | 0.032                    | FUNC_32K_CLK      | SYS_CLK1/610                  | OSC0                    |
| GPMC            | GPMC_ICLK        | Int & Func | 266                      | L3MAIN1_L3_GICLK  | CORE_X2_CLK                   | DPLL_CORE               |
| I2C1            | I2C1_ICLK        | Int        | 133                      | L4PER_L3_GICLK    | CORE_X2_CLK                   | DPLL_CORE               |
|                 | I2C1_FCLK        | Func       | 96                       | PER_96M_GFCLK     | FUNC_192M_CLK                 | DPLL_PER                |
| I2C2            | I2C2_ICLK        | Int        | 133                      | L4PER_L3_GICLK    | CORE_X2_CLK                   | DPLL_CORE               |
|                 | I2C2_FCLK        | Func       | 96                       | PER_96M_GFCLK     | FUNC_192M_CLK                 | DPLL_PER                |
| IEEE1500_2_OC_P | PI_L3CLK         | Int & Func | 266                      | L3INIT_L3_GICLK   | CORE_X2_CLK                   | DPLL_CORE               |
| IPU1            | IPU1_GFCLK       | Int & Func | IPU_CLK                  | IPU1_GFCLK        | DPLL_ABE_X2_CLK               | DPLL_DDR                |
|                 |                  |            |                          |                   | CORE_IPU_ISS_BOOT_CLK         | DPLL_CORE               |
| L3_INSTR        | L3_CLK           | Int        | L3_CLK                   | L3INSTR_L3_GICLK  | CORE_X2_CLK                   | DPLL_CORE               |
| L4_CFG          | L4_CFG_CLK       | Int        | 133                      | L4CFG_L3_GICLK    | CORE_X2_CLK                   | DPLL_CORE               |
| L4_PER1         | L4_PER1_CLK      | Int        | 133                      | L4PER_L3_GICLK    | CORE_X2_CLK                   | DPLL_CORE               |
| L4_PER2         | L4_PER2_CLK      | Int        | 133                      | L4PER2_L3_GICLK   | CORE_X2_CLK                   | DPLL_CORE               |
| L4_PER3         | L4_PER3_CLK      | Int        | 133                      | L4PER3_L3_GICLK   | CORE_X2_CLK                   | DPLL_CORE               |
| L4_WKUP         | L4_WKUP_CLK      | Int        | 38.4                     | WKUPAON_GICLK     | SYS_CLK1                      | OSC0                    |
|                 |                  |            |                          |                   | ABE_LP_CLK                    | DPLL_DDR                |
| MAILBOX1        | MAILBOX1_FLCK    | Int        | 133                      | L4CFG_L3_GICLK    | CORE_X2_CLK                   | DPLL_CORE               |
| MAILBOX2        | MAILBOX2_FLCK    | Int        | 133                      | L4CFG_L3_GICLK    | CORE_X2_CLK                   | DPLL_CORE               |

**表 5-5. Maximum Supported Frequency (continued)**

| Module        |                  |            |                          | Clock Sources    |                               |                         |
|---------------|------------------|------------|--------------------------|------------------|-------------------------------|-------------------------|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name  | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| MCASP1        | MCASP1_AHCLKR    | Func       | 50                       | MCASP1_AHCLKR    | ABE_24M_GFCLK                 | DPLL_DDR                |
|               |                  |            |                          |                  | ABE_SYS_CLK                   | SYS_CLK1                |
|               |                  |            |                          |                  | FUNC_24M_GFCLK                | DPLL_PER                |
|               |                  |            |                          |                  | SYS_CLK1                      | OSC0                    |
|               |                  |            |                          |                  | ATL_CLK0                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK1                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK2                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK3                      | Module ATL              |
|               |                  |            |                          |                  | SYS_CLK2                      | OSC1                    |
|               |                  |            |                          |                  | XREF_CLK0                     | REF_CLKIN0              |
|               |                  |            |                          |                  | XREF_CLK1                     | REF_CLKIN1              |
|               |                  |            |                          |                  | XREF_CLK2                     | REF_CLKIN2              |
|               | MCASP1_AHCLKX    | Func       | 50                       | MCASP1_AHCLKX    | ABE_24M_GFCLK                 | DPLL_DDR                |
|               |                  |            |                          |                  | ABE_SYS_CLK                   | SYS_CLK1                |
|               |                  |            |                          |                  | FUNC_24M_GFCLK                | DPLL_PER                |
|               |                  |            |                          |                  | SYS_CLK1                      | OSC0                    |
|               |                  |            |                          |                  | ATL_CLK0                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK1                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK2                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK3                      | Module ATL              |
|               |                  |            |                          |                  | SYS_CLK2                      | OSC1                    |
|               |                  |            |                          |                  | XREF_CLK0                     | REF_CLKIN0              |
|               |                  |            |                          |                  | XREF_CLK1                     | REF_CLKIN1              |
|               |                  |            |                          |                  | XREF_CLK2                     | REF_CLKIN2              |
|               | MCASP1_FCLK      | Func       | 133                      | MCASP1_AUX_GFCLK | L4_ICLK                       | DPLL_CORE               |
|               | MCASP1_ICLK      | Int        | 266                      | IPU_L3_GICLK     | SYS_CLK1                      | OSC0                    |
|               |                  |            |                          |                  | CORE_X2_CLK                   | DPLL_CORE               |

表 5-5. Maximum Supported Frequency (continued)

| Module        |                  |            |                          | Clock Sources    |                               |                         |
|---------------|------------------|------------|--------------------------|------------------|-------------------------------|-------------------------|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name  | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| MCASP2        | MCASP2_AHCLKR    | Func       | 50                       | MCASP6_AHCLKR    | ABE_24M_GFCLK                 | DPLL_DDR                |
|               |                  |            |                          |                  | ABE_SYS_CLK                   | SYS_CLK1                |
|               |                  |            |                          |                  | FUNC_24M_GFCLK                | DPLL_PER                |
|               |                  |            |                          |                  | SYS_CLK1                      | OSC0                    |
|               |                  |            |                          |                  | ATL_CLK0                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK1                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK2                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK3                      | Module ATL              |
|               |                  |            |                          |                  | SYS_CLK2                      | OSC1                    |
|               |                  |            |                          |                  | XREF_CLK0                     | REF_CLKIN0              |
|               |                  |            |                          |                  | XREF_CLK1                     | REF_CLKIN1              |
|               |                  |            |                          |                  | XREF_CLK2                     | REF_CLKIN2              |
|               | MCASP2_AHCLKX    | Func       | 50                       | MCASP4_AHCLKX    | ABE_24M_GFCLK                 | DPLL_DDR                |
|               |                  |            |                          |                  | ABE_SYS_CLK                   | SYS_CLK1                |
|               |                  |            |                          |                  | FUNC_24M_GFCLK                | DPLL_PER                |
|               |                  |            |                          |                  | SYS_CLK1                      | OSC0                    |
|               |                  |            |                          |                  | ATL_CLK0                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK1                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK2                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK3                      | Module ATL              |
|               |                  |            |                          |                  | SYS_CLK2                      | OSC1                    |
|               |                  |            |                          |                  | XREF_CLK0                     | REF_CLKIN0              |
|               |                  |            |                          |                  | XREF_CLK1                     | REF_CLKIN1              |
|               |                  |            |                          |                  | XREF_CLK2                     | REF_CLKIN2              |
|               | MCASP2_FCLK      | Func       | 133                      | MCASP4_AUX_GFCLK | L4_ICLK                       | DPLL_CORE               |
|               |                  |            |                          |                  | SYS_CLK1                      | OSC0                    |
|               | MCASP2_ICLK      | Int        | 133                      | L4PER2_L3_GICLK  | CORE_X2_CLK                   | DPLL_CORE               |

**表 5-5. Maximum Supported Frequency (continued)**

| Module        |                  |            |                          | Clock Sources    |                               |                         |
|---------------|------------------|------------|--------------------------|------------------|-------------------------------|-------------------------|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name  | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| MCASP3        | MCASP3_AHCLKR    | Func       | 50                       | MCASP7_AHCLKR    | ABE_24M_GFCLK                 | DPLL_DDR                |
|               |                  |            |                          |                  | ABE_SYS_CLK                   | SYS_CLK1                |
|               |                  |            |                          |                  | FUNC_24M_GFCLK                | DPLL_PER                |
|               |                  |            |                          |                  | SYS_CLK1                      | OSC0                    |
|               |                  |            |                          |                  | ATL_CLK0                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK1                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK2                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK3                      | Module ATL              |
|               |                  |            |                          |                  | SYS_CLK2                      | OSC1                    |
|               |                  |            |                          |                  | XREF_CLK0                     | REF_CLKIN0              |
|               |                  |            |                          |                  | XREF_CLK1                     | REF_CLKIN1              |
|               |                  |            |                          |                  | XREF_CLK2                     | REF_CLKIN2              |
|               | MCASP3_AHCLKX    | Func       | 50                       | MCASP5_AHCLKX    | ABE_24M_GFCLK                 | DPLL_DDR                |
|               |                  |            |                          |                  | ABE_SYS_CLK                   | SYS_CLK1                |
|               |                  |            |                          |                  | FUNC_24M_GFCLK                | DPLL_PER                |
|               |                  |            |                          |                  | SYS_CLK1                      | OSC0                    |
|               |                  |            |                          |                  | ATL_CLK0                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK1                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK2                      | Module ATL              |
|               |                  |            |                          |                  | ATL_CLK3                      | Module ATL              |
|               |                  |            |                          |                  | SYS_CLK2                      | OSC1                    |
|               |                  |            |                          |                  | XREF_CLK0                     | REF_CLKIN0              |
|               |                  |            |                          |                  | XREF_CLK1                     | REF_CLKIN1              |
|               |                  |            |                          |                  | XREF_CLK2                     | REF_CLKIN2              |
|               | MCASP3_FCLK      | Func       | 133                      | MCASP5_AUX_GFCLK | L4_ICLK                       | DPLL_CORE               |
|               |                  |            |                          |                  | SYS_CLK1                      | OSC0                    |
|               | MCASP3_ICLK      | Int        | 133                      | L4PER2_L3_GICLK  | CORE_X2_CLK                   | DPLL_CORE               |
| MCSPI1        | SPI1_ICLK        | Int        | 133                      | L4PER_L3_GICLK   | CORE_X2_CLK                   | DPLL_CORE               |
|               | SPI1_FCLK        | Func       | 48                       | PER_48M_GFCLK    | FUNC_192M_CLK                 | DPLL_PER                |
| MCSPI2        | SPI2_ICLK        | Int        | 133                      | L4PER_L3_GICLK   | CORE_X2_CLK                   | DPLL_CORE               |
|               | SPI2_FCLK        | Func       | 48                       | PER_48M_GFCLK    | FUNC_192M_CLK                 | DPLL_PER                |
| MCSPI3        | SPI3_ICLK        | Int        | 133                      | L4PER_L3_GICLK   | CORE_X2_CLK                   | DPLL_CORE               |
|               | SPI3_FCLK        | Func       | 48                       | PER_48M_GFCLK    | FUNC_192M_CLK                 | DPLL_PER                |
| MCSPI4        | SPI4_ICLK        | Int        | 133                      | L4PER_L3_GICLK   | CORE_X2_CLK                   | DPLL_CORE               |
|               | SPI4_FCLK        | Func       | 48                       | PER_48M_GFCLK    | FUNC_192M_CLK                 | DPLL_PER                |
| MMC1          | MMC_CLK_32K      | Func       | 0.032                    | FUNC_32K_CLK     | SYS_CLK1/610                  | OSC0                    |
|               | MMC_FCLK         | Func       | 192                      | MMC4_GFCLK       | FUNC_192M_CLK                 | DPLL_PER                |
|               |                  |            | 48                       |                  | FUNC_48M_FCLK                 | DPLL_PER                |
|               | MMC_ICLK         | Int        | 133                      | L3INIT_L3_GICLK  | CORE_X2_CLK                   | DPLL_CORE               |
| MMU_EDMA      | MMU_CLK          | Int        | 266                      | L3MAIN1_L3_GICLK | CORE_X2_CLK                   | DPLL_CORE               |
| OCMC_RAM      | OCMC_L3_CLK      | Int        | 266                      | L3MAIN1_L3_GICLK | CORE_X2_CLK                   | DPLL_CORE               |
| OCP_WP_NOC    | PICLKOCPL3       | Int        | 266                      | L3INSTR_L3_GICLK | CORE_X2_CLK                   | DPLL_CORE               |
| PWMSS1        | PWMSS1_GICLK     | Int & Func | 133                      | L4PER2_L3_GICLK  | CORE_X2_CLK                   | DPLL_CORE               |

表 5-5. Maximum Supported Frequency (continued)

| Module        |                  |            |                          | Clock Sources   |                               |                         |
|---------------|------------------|------------|--------------------------|-----------------|-------------------------------|-------------------------|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| QSPI          | QSPI_ICLK        | Int        | 266                      | L4PER2_L3_GICLK | CORE_X2_CLK                   | DPLL_CORE               |
|               | QSPI_FCLK        | Func       | 128                      | QSPI_GFCLK      | FUNC_128M_CLK                 | DPLL_PER                |
| RTI1          | OCP_CLK_PI       | Int        | 133                      | WKUPAON_GICLK   | PER_QSPI_CLK                  | DPLL_PER                |
|               | RTI_CLK_PI       | Func       | 13                       | RTI1_CLK        | CORE_X2_CLK                   | DPLL_CORE               |
|               |                  |            |                          |                 | SYS_CLK1/4                    | OSC0                    |
|               |                  |            |                          |                 | SYS_CLK2/4                    | OSC1                    |
| RTI2          | OCP_CLK_PI       | Int        | 133                      | WKUPAON_GICLK   | FUNC_32K_CLK                  | OSC0                    |
|               | RTI_CLK_PI       | Func       | 13                       | RTI2_CLK        | CORE_X2_CLK                   | DPLL_CORE               |
|               |                  |            |                          |                 | SYS_CLK1/4                    | OSC0                    |
|               |                  |            |                          |                 | SYS_CLK2/4                    | OSC1                    |
| RTI3          | OCP_CLK_PI       | Int        | 133                      | WKUPAON_GICLK   | FUNC_32K_CLK                  | OSC0                    |
|               | RTI_CLK_PI       | Func       | 13                       | RTI3_CLK        | CORE_X2_CLK                   | DPLL_CORE               |
|               |                  |            |                          |                 | SYS_CLK1/4                    | OSC0                    |
|               |                  |            |                          |                 | SYS_CLK2/4                    | OSC1                    |
| RTI4          | OCP_CLK_PI       | Int        | 133                      | WKUPAON_GICLK   | FUNC_32K_CLK                  | OSC0                    |
|               | RTI_CLK_PI       | Func       | 13                       | RTI4_CLK        | CORE_X2_CLK                   | DPLL_CORE               |
|               |                  |            |                          |                 | SYS_CLK1/4                    | OSC0                    |
|               |                  |            |                          |                 | SYS_CLK2/4                    | OSC1                    |
| RTI5          | OCP_CLK_PI       | Int        | 133                      | WKUPAON_GICLK   | FUNC_32K_CLK                  | OSC0                    |
|               | RTI_CLK_PI       | Func       | 13                       | RTI5_CLK        | CORE_X2_CLK                   | DPLL_CORE               |
|               |                  |            |                          |                 | SYS_CLK1/4                    | OSC0                    |
|               |                  |            |                          |                 | SYS_CLK2/4                    | OSC1                    |
| SD_DAC        | CLKDAC           | Func       | 50                       | VID_PIX_CLK     | VID_PIX_CLK                   | DPLL_EVE_VID_DSP        |
| SL2           | piclk            | Int        | IVA_GCLK                 | IVA_GCLK        | IVA_GFCLK                     | DPLL_IVA                |
| SPINLOCK      | SPINLOCK_ICLK    | Int        | 133                      | L4CFG_L3_GICLK  | CORE_X2_CLK                   | DPLL_CORE               |
| TIMER1        | TIMER1_ICLK      | Int        | 133                      | WKUPAON_GICLK   | SYS_CLK1                      | OSC0                    |
|               |                  |            |                          |                 | ABE_LP_CLK                    | DPLL_DDR                |
|               | TIMER1_FCLK      | Func       | 38.4                     | TIMER1_GFCLK    | SYS_CLK1                      | OSC0                    |
|               |                  |            |                          |                 | FUNC_32K_CLK                  | OSC0                    |
|               |                  |            |                          |                 | SYS_CLK2                      | OSC1                    |
|               |                  |            |                          |                 | XREF_CLK0                     | xref_clk0               |
|               |                  |            |                          |                 | XREF_CLK1                     | xref_clk1               |
|               |                  |            |                          |                 | ABE_GICLK                     | DPLL_DDR                |
| TIMER2        | TIMER2_ICLK      | Int        | 133                      | L4PER_L3_GICLK  | CORE_X2_CLK                   | DPLL_CORE               |
|               | TIMER2_FCLK      | Func       | 100                      | TIMER2_GFCLK    | SYS_CLK1                      | OSC0                    |
|               |                  |            |                          |                 | FUNC_32K_CLK                  | OSC0                    |
|               |                  |            |                          |                 | SYS_CLK2                      | OSC1                    |
|               |                  |            |                          |                 | XREF_CLK0                     | xref_clk0               |
|               |                  |            |                          |                 | XREF_CLK1                     | xref_clk1               |
|               |                  |            |                          |                 | ABE_GICLK                     | DPLL_DDR                |

**表 5-5. Maximum Supported Frequency (continued)**

| Module        |                  |            |                          | Clock Sources   |                               |                         |
|---------------|------------------|------------|--------------------------|-----------------|-------------------------------|-------------------------|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| TIMER3        | TIMER3_ICLK      | Int        | 133                      | L4PER_L3_GICLK  | CORE_X2_CLK                   | DPLL_CORE               |
|               | TIMER3_FCLK      | Func       | 100                      | TIMER3_GFCLK    | SYS_CLK1                      | OSC0                    |
|               |                  |            |                          |                 | FUNC_32K_CLK                  | OSC0                    |
|               |                  |            |                          |                 | SYS_CLK2                      | OSC1                    |
|               |                  |            |                          |                 | XREF_CLK0                     | xref_clk0               |
|               |                  |            |                          |                 | XREF_CLK1                     | xref_clk1               |
| TIMER4        | TIMER4_ICLK      | Int        | 133                      | L4PER_L3_GICLK  | CORE_X2_CLK                   | DPLL_CORE               |
|               | TIMER4_FCLK      | Func       | 100                      | TIMER4_GFCLK    | ABE_GICLK                     | DPLL_DDR                |
|               |                  |            |                          |                 | SYS_CLK1                      | OSC0                    |
|               |                  |            |                          |                 | FUNC_32K_CLK                  | OSC0                    |
|               |                  |            |                          |                 | SYS_CLK2                      | OSC1                    |
|               |                  |            |                          |                 | XREF_CLK0                     | xref_clk0               |
| TIMER5        | TIMER5_ICLK      | Int        | 133                      | IPU_L3_GICLK    | CORE_X2_CLK                   | DPLL_CORE               |
|               | TIMER5_FCLK      | Func       | 100                      | TIMER5_GFCLK    | XREF_CLK1                     | xref_clk1               |
|               |                  |            |                          |                 | ABE_GICLK                     | DPLL_DDR                |
|               |                  |            |                          |                 | CLKOUTMUX0_CLK                | CLKOUTMUX0              |
|               |                  |            |                          |                 | SYS_CLK1                      | OSC0                    |
|               |                  |            |                          |                 | FUNC_32K_CLK                  | OSC0                    |
| TIMER6        | TIMER6_ICLK      | Int        | 133                      | IPU_L3_GICLK    | CORE_X2_CLK                   | DPLL_CORE               |
|               | TIMER6_FCLK      | Func       | 100                      | TIMER6_GFCLK    | SYS_CLK1                      | OSC0                    |
|               |                  |            |                          |                 | FUNC_32K_CLK                  | OSC0                    |
|               |                  |            |                          |                 | SYS_CLK2                      | OSC1                    |
|               |                  |            |                          |                 | XREF_CLK0                     | xref_clk0               |
|               |                  |            |                          |                 | XREF_CLK1                     | xref_clk1               |
| TIMER7        | TIMER7_ICLK      | Int        | 133                      | IPU_L3_GICLK    | CORE_X2_CLK                   | DPLL_CORE               |
|               | TIMER7_FCLK      | Func       | 100                      | TIMER7_GFCLK    | ABE_GICLK                     | DPLL_DDR                |
|               |                  |            |                          |                 | CLKOUTMUX0_CLK                | CLKOUTMUX0              |
|               |                  |            |                          |                 | SYS_CLK1                      | OSC0                    |
|               |                  |            |                          |                 | FUNC_32K_CLK                  | OSC0                    |
|               |                  |            |                          |                 | SYS_CLK2                      | OSC1                    |

表 5-5. Maximum Supported Frequency (continued)

| Module        |                  |            |                          | Clock Sources    |                               |                         |
|---------------|------------------|------------|--------------------------|------------------|-------------------------------|-------------------------|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name  | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| TIMER8        | TIMER8_ICLK      | Int        | 133                      | IPU_L3_GICLK     | CORE_X2_CLK                   | DPLL_CORE               |
|               | TIMER8_FCLK      | Func       | 100                      | TIMER8_GFCLK     | SYS_CLK1                      | OSC0                    |
|               |                  |            |                          |                  | FUNC_32K_CLK                  | OSC0                    |
|               |                  |            |                          |                  | SYS_CLK2                      | OSC1                    |
|               |                  |            |                          |                  | XREF_CLK0                     | xref_clk0               |
|               |                  |            |                          |                  | XREF_CLK1                     | xref_clk1               |
|               |                  |            |                          |                  | ABE_GICLK                     | DPLL_DDR                |
|               |                  |            |                          |                  | CLKOUTMUX0_CLK                | CLKOUTMUX0              |
| TPCC          | TPCC_GCLK        | Int        | 266                      | L3MAIN1_L3_GICLK | CORE_X2_CLK                   | DPLL_CORE               |
| TPTC1         | TPTC0_GCLK       | Int        | 266                      | L3MAIN1_L3_GICLK | CORE_X2_CLK                   | DPLL_CORE               |
| TPTC2         | TPTC1_GCLK       | Int        | 266                      | L3MAIN1_L3_GICLK | CORE_X2_CLK                   | DPLL_CORE               |
| UART1         | UART1_FCLK       | Func       | 192                      | UART1_GFCLK      | FUNC_192M_CLK                 | DPLL_PER                |
|               |                  |            | 48                       |                  | FUNC_48M_FCLK                 | DPLL_PER                |
|               | UART1_ICLK       | Int        | 133                      | L4PER_L3_GICLK   | CORE_X2_CLK                   | DPLL_CORE               |
| UART2         | UART2_FCLK       | Func       | 192                      | UART2_GFCLK      | FUNC_192M_CLK                 | DPLL_PER                |
|               |                  |            | 48                       |                  | FUNC_48M_FCLK                 | DPLL_PER                |
|               | UART2_ICLK       | Int        | 133                      | L4PER_L3_GICLK   | CORE_X2_CLK                   | DPLL_CORE               |
| UART3         | UART3_FCLK       | Func       | 192                      | UART3_GFCLK      | FUNC_192M_CLK                 | DPLL_PER                |
|               |                  |            | 48                       |                  | FUNC_48M_FCLK                 | DPLL_PER                |
|               | UART3_ICLK       | Int        | 133                      | L4PER_L3_GICLK   | CORE_X2_CLK                   | DPLL_CORE               |
| VCP1          | VCP1_CLK         | Int        | 266                      | L3MAIN1_L3_GICLK | CORE_X2_CLK                   | DPLL_CORE               |
| VIP1          | PROC_CLK         | Func       | 266                      | VIP1_GCLK        | L3_ICLK                       | DPLL_CORE               |
|               | L3_CLK           | Int        |                          |                  | CORE_ISS_MAIN_CLK             | DPLL_CORE               |
|               | L4_CLK           | Int        | 133                      | VIP1_GCLKDIV2    | VIP1_GCLK/2                   | DPLL_CORE               |

## 5.6 Power Consumption Summary

注: Maximum power consumption for this SoC depends on the specific use conditions for the end system. Contact your TI representative for assistance in estimating maximum power consumption for the end system use case.

## 5.7 Electrical Characteristics

注: The data specified in 表 5-6 through 表 5-10 are subject to change.

注: The interfaces or signals described in 表 5-6 through 表 5-10 correspond to the interfaces or signals available in multiplexing mode 0 (Function 1).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY/GPIO combination in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

**表 5-6. LVCMOS DDR DC Electrical Characteristics**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                                                                                                                                                                                          |                                                        |                      | MIN                         | NOM | MAX                         | UNIT |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------|----------------------|-----------------------------|-----|-----------------------------|------|
| Signal Names in MUXMODE 0 (Single-Ended Signals) ABF: ddr1_d[31:0], ddr1_a[15:0], ddr1_dqm[3:0], ddr1_ba[2:0], ddr1_csn[1:0], ddr1_cke[1:0], ddr1_odt[0], ddr1_casn, ddr1_rasn, ddr1_wen, ddr1_rst, ddr1_ecc_d[7:0], ddr1_dqm_ecc; |                                                        |                      |                             |     |                             |      |
| Driver Mode                                                                                                                                                                                                                        |                                                        |                      |                             |     |                             |      |
| V <sub>OH</sub>                                                                                                                                                                                                                    | High-level output threshold (I <sub>OH</sub> = 0.1 mA) |                      | 0.9×VDD <sub>S</sub>        |     |                             | V    |
| V <sub>OL</sub>                                                                                                                                                                                                                    | Low-level output threshold (I <sub>OL</sub> = 0.1 mA)  |                      |                             |     | 0.1×VDD <sub>S</sub>        | V    |
| C <sub>PAD</sub>                                                                                                                                                                                                                   | Pad capacitance (including package capacitance)        |                      |                             |     | 3                           | pF   |
| Z <sub>O</sub>                                                                                                                                                                                                                     | Output impedance (drive strength)                      | I[2:0] = 000 (Imp80) |                             | 80  |                             | Ω    |
|                                                                                                                                                                                                                                    |                                                        | I[2:0] = 001 (Imp60) |                             | 60  |                             |      |
|                                                                                                                                                                                                                                    |                                                        | I[2:0] = 010 (Imp48) |                             | 48  |                             |      |
|                                                                                                                                                                                                                                    |                                                        | I[2:0] = 011 (Imp40) |                             | 40  |                             |      |
|                                                                                                                                                                                                                                    |                                                        | I[2:0] = 100 (Imp34) |                             | 34  |                             |      |
| Single-Ended Receiver Mode                                                                                                                                                                                                         |                                                        |                      |                             |     |                             |      |
| V <sub>IH</sub>                                                                                                                                                                                                                    | High-level input threshold                             | DDR3/DDR3L           | VREF+0.1                    |     | VDD <sub>S</sub> +0.2       | V    |
| V <sub>IL</sub>                                                                                                                                                                                                                    | Low-level input threshold                              | DDR3/DDR3L           | -0.2                        |     | VREF-0.1                    | V    |
| V <sub>CM</sub>                                                                                                                                                                                                                    | Input common-mode voltage                              |                      | VREF<br>-1%VDD <sub>S</sub> |     | VREF+<br>1%VDD <sub>S</sub> | V    |
| C <sub>PAD</sub>                                                                                                                                                                                                                   | Pad capacitance (including package capacitance)        |                      |                             |     |                             | pF   |
| Signal Names in MUXMODE 0 (Differential Signals): ddr1_dqs[3:0], ddr1_dqsn[3:0], ddr1_ck, ddr1_nck, ddr1_dqs_ecc, ddr1_dqsn_ecc;                                                                                                   |                                                        |                      |                             |     |                             |      |
| Driver Mode                                                                                                                                                                                                                        |                                                        |                      |                             |     |                             |      |
| V <sub>OH</sub>                                                                                                                                                                                                                    | High-level output threshold (I <sub>OH</sub> = 0.1 mA) |                      | 0.9×VDD <sub>S</sub>        |     |                             | V    |
| V <sub>OL</sub>                                                                                                                                                                                                                    | Low-level output threshold (I <sub>OL</sub> = 0.1 mA)  |                      |                             |     | 0.1×VDD <sub>S</sub>        | V    |
| C <sub>PAD</sub>                                                                                                                                                                                                                   | Pad capacitance (including package capacitance)        |                      |                             |     | 3                           | pF   |
| Z <sub>O</sub>                                                                                                                                                                                                                     | Output impedance (drive strength)                      | I[2:0] = 000 (Imp80) |                             | 80  |                             | Ω    |
|                                                                                                                                                                                                                                    |                                                        | I[2:0] = 001 (Imp60) |                             | 60  |                             |      |
|                                                                                                                                                                                                                                    |                                                        | I[2:0] = 010 (Imp48) |                             | 48  |                             |      |
|                                                                                                                                                                                                                                    |                                                        | I[2:0] = 011 (Imp40) |                             | 40  |                             |      |
|                                                                                                                                                                                                                                    |                                                        | I[2:0] = 100 (Imp34) |                             | 34  |                             |      |
| Single-Ended Receiver Mode                                                                                                                                                                                                         |                                                        |                      |                             |     |                             |      |
| V <sub>IH</sub>                                                                                                                                                                                                                    | High-level input threshold                             | DDR3/DDR3L           | VREF+0.1                    |     | VDD <sub>S</sub> +0.2       | V    |
| V <sub>IL</sub>                                                                                                                                                                                                                    | Low-level input threshold                              | DDR3/DDR3L           | -0.2                        |     | VREF-0.1                    | V    |
| V <sub>CM</sub>                                                                                                                                                                                                                    | Input common-mode voltage                              |                      | VREF<br>-1%VDD <sub>S</sub> |     | VREF+<br>1%VDD <sub>S</sub> | V    |
| C <sub>PAD</sub>                                                                                                                                                                                                                   | Pad capacitance (including package capacitance)        |                      |                             |     | 3                           | pF   |

表 5-6. LVCMOS DDR DC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                         |                                                 |            | MIN             | NOM | MAX             | UNIT |
|-----------------------------------|-------------------------------------------------|------------|-----------------|-----|-----------------|------|
| <b>Differential Receiver Mode</b> |                                                 |            |                 |     |                 |      |
| V <sub>SWING</sub>                | Input voltage swing                             | DDR3/DDR3L | 0.4×vdds        |     | 0.6×vdds        | V    |
| V <sub>CM</sub>                   | Input common-mode voltage                       |            | VREF<br>-1%VDDS |     | VREF+<br>1%VDDS | V    |
| C <sub>PAD</sub>                  | Pad capacitance (including package capacitance) |            |                 |     | 3               | pF   |

(1) VDDS in this table stands for corresponding power supply (i.e. vdds\_ddr1 or vdds\_ddr2). For more information on the power supply name and the corresponding ball, see 表 4-1, POWER [10] column.

表 5-7. Dual Voltage LVCMOS I2C DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                                 |                                                                                                                                                           | MIN                   | NOM | MAX      | UNIT |
|---------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-----|----------|------|
| <b>Signal Names in MUXMODE 0:</b> i2c2_scl; i2c1_scl; i2c1_sda; i2c2_sda; |                                                                                                                                                           |                       |     |          |      |
| <b>Balls ABF:</b> L3, L4, L6, L5;                                         |                                                                                                                                                           |                       |     |          |      |
| <b>I<sup>2</sup>C Standard Mode – 1.8 V</b>                               |                                                                                                                                                           |                       |     |          |      |
| V <sub>IH</sub>                                                           | Input high-level threshold                                                                                                                                | 0.7×VDDS              |     |          | V    |
| V <sub>IL</sub>                                                           | Input low-level threshold                                                                                                                                 |                       |     | 0.3×VDDS | V    |
| V <sub>hys</sub>                                                          | Hysteresis                                                                                                                                                | 0.1×VDDS              |     |          | V    |
| I <sub>I</sub>                                                            | Input current at each I/O pin with an input voltage between 0.1×VDDS to 0.9×VDDS                                                                          |                       |     | 12       | μA   |
| I <sub>OZ</sub>                                                           | I <sub>OZ</sub> (I <sub>PAD</sub> Current) at each IO pin. PAD is swept from 0 to VDDS and the Max(I(PAD)) is measured and is reported as I <sub>OZ</sub> |                       |     | 12       | μA   |
| C <sub>I</sub>                                                            | Input capacitance                                                                                                                                         |                       |     | 10       | pF   |
| V <sub>OL3</sub>                                                          | Output low-level threshold open-drain at 3-mA sink current                                                                                                |                       |     | 0.2×VDDS | V    |
| I <sub>OLmin</sub>                                                        | Low-level output current @V <sub>OL</sub> =0.2×VDDS                                                                                                       | 3                     |     |          | mA   |
| t <sub>OF</sub>                                                           | Output fall time from V <sub>IHmin</sub> to V <sub>ILmax</sub> with a bus capacitance CB from 5 pF to 400 pF                                              |                       |     | 250      | ns   |
| <b>I<sup>2</sup>C Fast Mode – 1.8 V</b>                                   |                                                                                                                                                           |                       |     |          |      |
| V <sub>IH</sub>                                                           | Input high-level threshold                                                                                                                                | 0.7×VDDS              |     |          | V    |
| V <sub>IL</sub>                                                           | Input low-level threshold                                                                                                                                 |                       |     | 0.3×VDDS | V    |
| V <sub>hys</sub>                                                          | Hysteresis                                                                                                                                                | 0.1×VDDS              |     |          | V    |
| I <sub>I</sub>                                                            | Input current at each I/O pin with an input voltage between 0.1×VDDS to 0.9×VDDS                                                                          |                       |     | 12       | μA   |
| I <sub>OZ</sub>                                                           | I <sub>OZ</sub> (I <sub>PAD</sub> Current) at each IO pin. PAD is swept from 0 to VDDS and the Max(I(PAD)) is measured and is reported as I <sub>OZ</sub> |                       |     | 12       | μA   |
| C <sub>I</sub>                                                            | Input capacitance                                                                                                                                         |                       |     | 10       | pF   |
| V <sub>OL3</sub>                                                          | Output low-level threshold open-drain at 3-mA sink current                                                                                                |                       |     | 0.2×VDDS | V    |
| I <sub>OLmin</sub>                                                        | Low-level output current @V <sub>OL</sub> =0.2×VDDS                                                                                                       | 3                     |     |          | mA   |
| t <sub>OF</sub>                                                           | Output fall time from V <sub>IHmin</sub> to V <sub>ILmax</sub> with a bus capacitance CB from 10 pF to 400 pF                                             | 20+0.1×C <sub>b</sub> |     | 250      | ns   |
| <b>I<sup>2</sup>C Standard Mode – 3.3 V</b>                               |                                                                                                                                                           |                       |     |          |      |
| V <sub>IH</sub>                                                           | Input high-level threshold                                                                                                                                | 0.7×VDDS              |     |          | V    |
| V <sub>IL</sub>                                                           | Input low-level threshold                                                                                                                                 |                       |     | 0.3×VDDS | V    |
| V <sub>hys</sub>                                                          | Hysteresis                                                                                                                                                | 0.05×VDD<br>S         |     |          | V    |
| I <sub>I</sub>                                                            | Input current at each I/O pin with an input voltage between 0.1×VDDS to 0.9×VDDS                                                                          | 31                    |     | 80       | μA   |
| I <sub>OZ</sub>                                                           | I <sub>OZ</sub> (I <sub>PAD</sub> Current) at each IO pin. PAD is swept from 0 to VDDS and the Max(I(PAD)) is measured and is reported as I <sub>OZ</sub> | 31                    |     | 80       | μA   |
| C <sub>I</sub>                                                            | Input capacitance                                                                                                                                         |                       |     | 10       | pF   |

**表 5-7. Dual Voltage LVCMOS I2C DC Electrical Characteristics (continued)**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                               |                                                                                                                                                                  | MIN                   | NOM | MAX                  | UNIT    |
|-----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-----|----------------------|---------|
| $V_{OL3}$                               | Output low-level threshold open-drain at 3-mA sink current                                                                                                       |                       |     | 0.4                  | V       |
| $I_{OLmin}$                             | Low-level output current @ $V_{OL}=0.4V$                                                                                                                         | 3                     |     |                      | mA      |
| $I_{OLmin}$                             | Low-level output current @ $V_{OL}=0.6V$ for full drive load (400pF/400KHz)                                                                                      | 6                     |     |                      | mA      |
| $t_{OF}$                                | Output fall time from $V_{IHmin}$ to $V_{ILmax}$ with a bus capacitance CB from 5 pF to 400 pF                                                                   |                       |     | 250                  | ns      |
| <b>I<sup>2</sup>C Fast Mode – 3.3 V</b> |                                                                                                                                                                  |                       |     |                      |         |
| $V_{IH}$                                | Input high-level threshold                                                                                                                                       | $0.7 \times V_{DD5}$  |     |                      | V       |
| $V_{IL}$                                | Input low-level threshold                                                                                                                                        |                       |     | $0.3 \times V_{DD5}$ | V       |
| $V_{hys}$                               | Hysteresis                                                                                                                                                       | $0.05 \times V_{DD5}$ |     |                      | V       |
| $I_I$                                   | Input current at each I/O pin with an input voltage between $0.1 \times V_{DD5}$ to $0.9 \times V_{DD5}$                                                         | 31                    |     | 80                   | $\mu A$ |
| $I_{OZ}$                                | $I_{OZ}(I_{PAD})$ Current) at each IO pin. PAD is swept from 0 to $V_{DD5}$ and the $Max(I(PAD))$ is measured and is reported as $I_{OZ}$                        | 31                    |     | 80                   | $\mu A$ |
| $C_I$                                   | Input capacitance                                                                                                                                                |                       |     | 10                   | pF      |
| $V_{OL3}$                               | Output low-level threshold open-drain at 3-mA sink current                                                                                                       |                       |     | 0.4                  | V       |
| $I_{OLmin}$                             | Low-level output current @ $V_{OL}=0.4V$                                                                                                                         | 3                     |     |                      | mA      |
| $I_{OLmin}$                             | Low-level output current @ $V_{OL}=0.6V$ for full drive load (400pF/400KHz)                                                                                      | 6                     |     |                      | mA      |
| $t_{OF}$                                | Output fall time from $V_{IHmin}$ to $V_{ILmax}$ with a bus capacitance CB from 10 pF to 200 pF (Proper External Resistor Value should be used as per I2C spec)  | $20 + 0.1 \times C_b$ |     | 250                  | ns      |
|                                         | Output fall time from $V_{IHmin}$ to $V_{ILmax}$ with a bus capacitance CB from 300 pF to 400 pF (Proper External Resistor Value should be used as per I2C spec) | 40                    |     | 290                  |         |

(1)  $V_{DD5}$  in this table stands for corresponding power supply (i.e. vddshv3). For more information on the power supply name and the corresponding ball, see 表 4-1, POWER [10] column.

**表 5-8. IQ1833 Buffers DC Electrical Characteristics**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                               |                                                 | MIN                   | NOM | MAX                   | UNIT    |
|-----------------------------------------|-------------------------------------------------|-----------------------|-----|-----------------------|---------|
| <b>Signal Names in MUXMODE 0:</b> tclk; |                                                 |                       |     |                       |         |
| <b>Balls ABF:</b> J2;                   |                                                 |                       |     |                       |         |
| <b>1.8-V Mode</b>                       |                                                 |                       |     |                       |         |
| $V_{IH}$                                | Input high-level threshold                      | $0.75 \times V_{DD5}$ |     |                       | V       |
| $V_{IL}$                                | Input low-level threshold                       |                       |     | $0.25 \times V_{DD5}$ | V       |
| $V_{HYS}$                               | Input hysteresis voltage                        | 100                   |     |                       | mV      |
| $I_{IN}$                                | Input current at each I/O pin                   | 2                     |     | 11                    | $\mu A$ |
| $C_{PAD}$                               | Pad capacitance (including package capacitance) |                       |     | 1                     | pF      |
| <b>3.3-V Mode</b>                       |                                                 |                       |     |                       |         |
| $V_{IH}$                                | Input high-level threshold                      | 2.0                   |     |                       | V       |
| $V_{IL}$                                | Input low-level threshold                       |                       |     | 0.6                   | V       |
| $V_{HYS}$                               | Input hysteresis voltage                        | 400                   |     |                       | mV      |
| $I_{IN}$                                | Input current at each I/O pin                   | 5                     |     | 11                    | $\mu A$ |
| $C_{PAD}$                               | Pad capacitance (including package capacitance) |                       |     | 1                     | pF      |

(1)  $V_{DD5}$  in this table stands for corresponding power supply (i.e. vddshv1). For more information on the power supply name and the corresponding ball, see 表 4-1, POWER [10] column.

表 5-9. IHHV1833 Buffers DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                               |                                                 | MIN  | NOM | MAX | UNIT    |
|-----------------------------------------|-------------------------------------------------|------|-----|-----|---------|
| <b>Signal Names in MUXMODE 0:</b> porz; |                                                 |      |     |     |         |
| <b>Balls ABF:</b> G3;                   |                                                 |      |     |     |         |
| <b>1.8-V Mode</b>                       |                                                 |      |     |     |         |
| $V_{IH}$                                | Input high-level threshold                      | 1.2  |     |     | V       |
| $V_{IL}$                                | Input low-level threshold                       |      |     | 0.4 | V       |
| $V_{HYS}$                               | Input hysteresis voltage                        | 40   |     |     | mV      |
| $I_{IN}$                                | Input current at each I/O pin                   | 0.02 |     | 1   | $\mu$ A |
| $C_{PAD}$                               | Pad capacitance (including package capacitance) |      |     | 1   | pF      |
| <b>3.3-V Mode</b>                       |                                                 |      |     |     |         |
| $V_{IH}$                                | Input high-level threshold                      | 1.2  |     |     | V       |
| $V_{IL}$                                | Input low-level threshold                       |      |     | 0.4 | V       |
| $V_{HYS}$                               | Input hysteresis voltage                        | 40   |     |     | mV      |
| $I_{IN}$                                | Input current at each I/O pin                   | 5    |     | 8   | $\mu$ A |
| $C_{PAD}$                               | Pad capacitance (including package capacitance) |      |     | 1   | pF      |

表 5-10. LVCMOS Analog OSC Buffers DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                             | DESCRIPTION                                                     | MIN                   | NOM  | MAX                   | UNIT |
|-----------------------------------------------------------------------|-----------------------------------------------------------------|-----------------------|------|-----------------------|------|
| <b>Signal Names in MUXMODE 0:</b> xi_osc0, xo_osc0, xi_osc1, xo_osc1; |                                                                 |                       |      |                       |      |
| <b>Balls ABF:</b> E22, D22, B21, C21;                                 |                                                                 |                       |      |                       |      |
| $V_{IH}$                                                              | Input high-level threshold                                      | $0.65 \times V_{DD5}$ |      |                       | V    |
| $V_{IL}$                                                              | Input low-level threshold                                       |                       |      | $0.35 \times V_{DD5}$ | V    |
| $I_{OH}$                                                              |                                                                 | hfenable=0            | 1.18 |                       | mA   |
|                                                                       |                                                                 | hfenable=1            | 2    |                       | mA   |
| $I_{OL}$                                                              |                                                                 | hfenable=0            | 2    |                       | mA   |
|                                                                       |                                                                 | hfenable=1            | 3.2  |                       | mA   |
| $V_{HYS}$                                                             | Input hysteresis voltage                                        | MODE-1                | 150  |                       | mV   |
| $C_{PAD}$                                                             | Capacitance connected on input and output Pad on Board, CL1=CL2 | 12                    |      | 24                    | pF   |

(1)  $V_{DD5}$  in this table stands for corresponding power supply (i.e. vdda\_osc). For more information on the power supply name and the corresponding ball, see 表 4-1, POWER [10] column.

表 5-11. Dual Voltage LVCMOS DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER         | DESCRIPTION                                                                                                                              | MIN                   | NOM | MAX                   | UNIT    |
|-------------------|------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-----|-----------------------|---------|
| <b>1.8-V Mode</b> |                                                                                                                                          |                       |     |                       |         |
| $V_{IH}$          | Input high-level threshold                                                                                                               | $0.65 \times V_{DD5}$ |     |                       | V       |
| $V_{IL}$          | Input low-level threshold                                                                                                                |                       |     | $0.35 \times V_{DD5}$ | V       |
| $V_{HYS}$         | Input hysteresis voltage                                                                                                                 | 100                   |     |                       | mV      |
| $V_{OH}$          | Output high-level threshold ( $I_{OH} = 2$ mA)                                                                                           | $V_{DD5} - 0.45$      |     |                       | V       |
| $V_{OL}$          | Output low-level threshold ( $I_{OL} = 2$ mA)                                                                                            |                       |     | 0.45                  | V       |
| $I_{DRIVE}$       | Pin Drive strength at PAD Voltage = 0.45V or $V_{DD5} - 0.45V$                                                                           | 6                     |     |                       | mA      |
| $I_{IN}$          | Input current at each I/O pin                                                                                                            |                       |     | 16                    | $\mu$ A |
| $I_{OZ}$          | $I_{OZ}(I_{PAD}$ Current) at each IO pin. PAD is swept from 0 to $V_{DD5}$ and the $Max(I(PAD))$ is measured and is reported as $I_{OZ}$ |                       |     | 11.5                  | $\mu$ A |

**表 5-11. Dual Voltage LVCMOS DC Electrical Characteristics (continued)**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                      | DESCRIPTION                                                                                                                           | MIN      | NOM | MAX | UNIT     |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|----------|-----|-----|----------|
| $I_{IN}$ with pulldown enabled | Input current at each I/O pin with weak pulldown enabled measured when PAD = VDD5                                                     | 60       | 120 | 200 | $\mu$ A  |
| $I_{IN}$ with pullup enabled   | Input current at each I/O pin with weak pullup enabled measured when PAD = 0                                                          | 60       | 120 | 210 | $\mu$ A  |
| $C_{PAD}$                      | Pad capacitance (including package capacitance)                                                                                       |          |     | 4   | pF       |
| $Z_O$                          | Output impedance (drive strength)                                                                                                     |          | 40  |     | $\Omega$ |
| <b>3.3-V Mode</b>              |                                                                                                                                       |          |     |     |          |
| $V_{IH}$                       | Input high-level threshold                                                                                                            | 2        |     |     | V        |
| $V_{IL}$                       | Input low-level threshold                                                                                                             |          |     | 0.8 | V        |
| $V_{HYS}$                      | Input hysteresis voltage                                                                                                              | 200      |     |     | mV       |
| $V_{OH}$                       | Output high-level threshold ( $I_{OH} = 100\mu$ A)                                                                                    | VDD5-0.2 |     |     | V        |
| $V_{OL}$                       | Output low-level threshold ( $I_{OL} = 100\mu$ A)                                                                                     |          |     | 0.2 | V        |
| $I_{DRIVE}$                    | Pin Drive strength at PAD Voltage = 0.45V or VDD5-0.45V                                                                               | 6        |     |     | mA       |
| $I_{IN}$                       | Input current at each I/O pin                                                                                                         |          |     | 64  | $\mu$ A  |
| $I_{OZ}$                       | $I_{OZ}(I_{PAD}$ Current) at each IO pin. PAD is swept from 0 to VDD5 and the Max( $I(PAD)$ ) is measured and is reported as $I_{OZ}$ |          |     | 64  | $\mu$ A  |
| $I_{IN}$ with pulldown enabled | Input current at each I/O pin with weak pulldown enabled measured when PAD = VDD5                                                     | 10       | 100 | 290 | $\mu$ A  |
| $I_{IN}$ with pullup enabled   | Input current at each I/O pin with weak pullup enabled measured when PAD = 0                                                          | 40       | 100 | 200 | $\mu$ A  |
| $C_{PAD}$                      | Pad capacitance (including package capacitance)                                                                                       |          |     | 4   | pF       |
| $Z_O$                          | Output impedance (drive strength)                                                                                                     |          | 40  |     | $\Omega$ |

(1) VDD5 in this table stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see 表 4-1, POWER [10] column.

**表 5-12. Analog-to-Digital ADC Subsystem Electrical Specifications**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                        | CONDITIONS                                           | MIN  | NOM       | MAX      | UNIT     |
|----------------------------------|------------------------------------------------------|------|-----------|----------|----------|
| <b>Analog Input</b>              |                                                      |      |           |          |          |
| Full-scale Input Range           |                                                      |      | adc_vrefp |          | V        |
| Vref                             | Should be less than or equal to vdds_18v.            | 1.62 |           | vdds_18v | V        |
| Differential Non-Linearity (DNL) |                                                      | -1   |           | 1        | LSB      |
| Integral Non-Linearity (INL)     | adc_vrefp = vdds_18v                                 |      |           | $\pm 2$  | LSB      |
| Gain Error                       | adc_vrefp = vdds_18v                                 |      | $\pm 4$   |          | LSB      |
| Offset Error                     | adc_vrefp = vdds_18v                                 |      | $\pm 3$   |          | LSB      |
| Input Sampling Capacitance       |                                                      |      | 3.2       | 5        | pF       |
| Input Frequency adc_in[7:0]      |                                                      | 0    |           | 30       | kHz      |
| Signal-to-Noise Ratio (SNR)      | Input Signal: 30 kHz sine wave at -0.5 dB Full Scale |      | 50        |          | dB       |
| Total Harmonic Distortion (THD)  | 1.8 Vpp, 30 kHz sine wave                            |      | 60        |          | dB       |
| Spurious Free Dynamic Range      | 1.8 Vpp, 30 kHz sine wave                            |      | 60        |          | dB       |
| Signal-to-Noise Plus Distortion  | 1.8 Vpp, 30 kHz sine wave                            |      | 50        |          | dB       |
| adc_vrefp Input Impedance        |                                                      |      | 20        |          | $\Omega$ |
| <b>Sampling Dynamics</b>         |                                                      |      |           |          |          |

表 5-12. Analog-to-Digital ADC Subsystem Electrical Specifications (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                          | CONDITIONS               | MIN    | NOM | MAX          | UNIT         |
|------------------------------------|--------------------------|--------|-----|--------------|--------------|
| Time from Start to Start           |                          | 17     |     |              | Clock Cycles |
| Conversion Time + Error Correction |                          | 10 + 1 |     |              | Clock Cycles |
| Acquisition time                   |                          | 4      |     |              | Clock Cycles |
| Throughput Rate                    | CLK = 20 MHz (Pin : clk) |        |     | 1            | MSPS         |
| Channel to Channel Isolation       |                          |        | 90  |              | dB           |
| ADC Clock Frequency                |                          |        |     | See<br>表 5-1 | MHz          |

- (1) Connect adc\_vrefp to vdda\_adc when not using a positive external reference voltage.
- (2) This parameter is valid when the respective AIN terminal is configured to operate as a general-purpose ADC input.
- (3) The maximum sample rate assumes a conversion time of 13 ADC clock cycles with the acquisition time configured for the minimum of 2 ADC clock cycles, where it takes a total of 15 ADC clock cycles to sample the analog input and convert it to a positive binary weighted digital value.

## 5.8 Thermal Characteristics

For reliability and operability concerns, the maximum junction temperature of the Device has to be at or below the  $T_J$  value identified in [Section 5.4, Recommended Operating Conditions](#).

A BCI compact thermal model for this Device is available and recommended for use when modeling thermal performance in a system.

Therefore, it is recommended to perform thermal simulations at the system level with the worst case device power consumption.

### 5.8.1 Package Thermal Characteristics

表 5-13 provides the thermal resistance characteristics for the package used on this device.

注: Power dissipation of 4.14 W and an ambient temperature of 65°C is assumed for ABF package.

表 5-13. Thermal Resistance Characteristics

| NO. | PARAMETER         | DESCRIPTION             | °C/W <sup>(1)</sup> | AIR FLOW (m/s) <sup>(2)</sup> |
|-----|-------------------|-------------------------|---------------------|-------------------------------|
| T1  | $R_{\theta_{JC}}$ | Junction-to-case        | 1.41                | N/A                           |
| T2  | $R_{\theta_{JB}}$ | Junction-to-board       | 5.96                | N/A                           |
| T3  | $R_{\theta_{JA}}$ | Junction-to-free air    | 15.4                | 0                             |
| T4  |                   | Junction-to-moving air  | 13.1                | 1                             |
| T5  |                   |                         | 12.2                | 2                             |
| T6  |                   |                         | 11.6                | 3                             |
| T7  | $\Psi_{JT}$       | Junction-to-free air    | 0.94                | 0                             |
| T8  |                   | Junction-to-package top | 0.94                | 1                             |
| T9  |                   |                         | 0.94                | 2                             |
| T10 |                   |                         | 0.94                | 3                             |
| T11 | $\Psi_{JB}$       | Junction-to-free air    | 5.12                | 0                             |
| T12 |                   | Junction-to-board       | 4.78                | 1                             |
| T13 |                   |                         | 4.63                | 2                             |
| T14 |                   |                         | 4.52                | 3                             |

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [ $R\theta_{JC}$ ] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(2) m/s = meters per second

## 5.9 Timing Requirements and Switching Characteristics

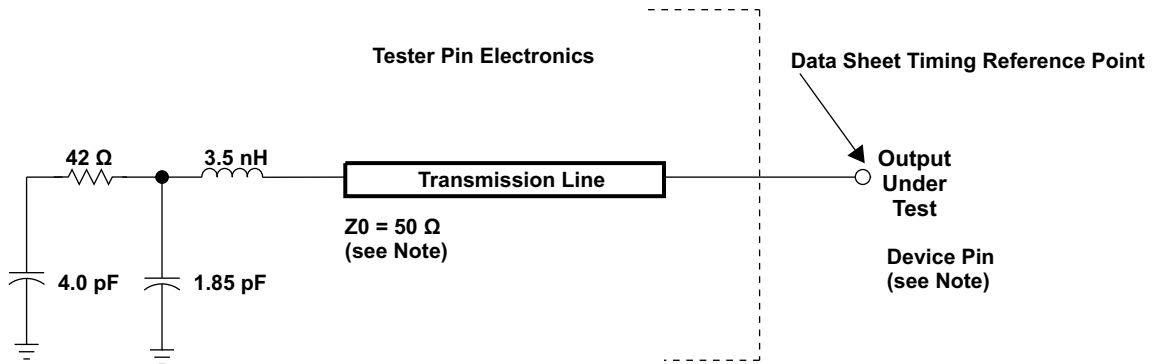
### 5.9.1 Timing Parameters and Information

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of pin names and other related terminologies have been abbreviated as follows:

**Table 5-14. Timing Parameters**

| SUBSCRIPTS |                                        |
|------------|----------------------------------------|
| SYMBOL     | PARAMETER                              |
| c          | Cycle time (period)                    |
| d          | Delay time                             |
| dis        | Disable time                           |
| en         | Enable time                            |
| h          | Hold time                              |
| su         | Setup time                             |
| START      | Start bit                              |
| t          | Transition time                        |
| v          | Valid time                             |
| w          | Pulse duration (width)                 |
| X          | Unknown, changing, or don't care level |
| F          | Fall time                              |
| H          | High                                   |
| L          | Low                                    |
| R          | Rise time                              |
| V          | Valid                                  |
| IV         | Invalid                                |
| AE         | Active Edge                            |
| FE         | First Edge                             |
| LE         | Last Edge                              |
| Z          | High impedance                         |

### 5.9.1.1 Parameter Information



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

pm\_tstcirc\_prs403

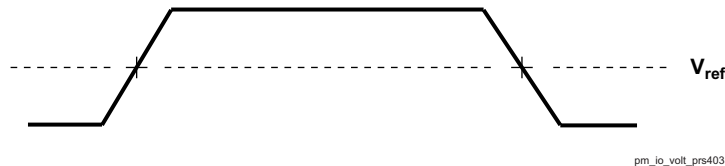
Figure 5-1. Test Load Circuit for AC Timing Measurements

The load capacitance value stated is only for characterization and measurement of AC timing signals.

This load capacitance value does not indicate the maximum load the device is capable of driving.

#### 5.9.1.1.1 1.8 V and 3.3 V Signal Transition Levels

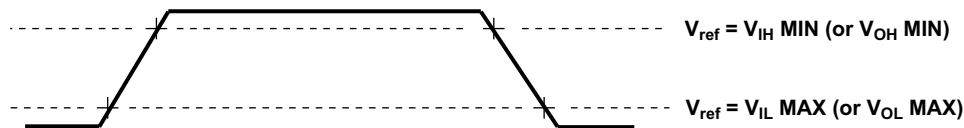
All input and output timing parameters are referenced to  $V_{ref}$  for both "0" and "1" logic levels.  $V_{ref} = (V_{DD} I/O)/2$ .



pm\_io\_volt\_prs403

Figure 5-2. Input and Output Voltage Reference Levels for AC Timing Measurements

All rise and fall transition timing parameters are referenced to  $V_{IL}$  MAX and  $V_{IH}$  MIN for input clocks,  $V_{OL}$  MAX and  $V_{OH}$  MIN for output clocks.



pm\_transvolt\_prs403

Figure 5-3. Rise and Fall Transition Time Voltage Reference Levels

#### 5.9.1.1.2 1.8 V and 3.3 V Signal Transition Rates

The default SLEWCONTROL settings in each pad configuration register must be used to ensure timings, unless specific instructions otherwise are given in the individual timing subsections of the datasheet.

All timings are tested with an input edge rate of 4 volts per nanosecond (4 V/ns).

#### **5.9.1.1.3 Timing Parameters and Board Routing Analysis**

The timing parameter values specified in this data manual do not include delays by board routes. As a good board design practice, such delays must always be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends utilizing the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the [Using IBIS Models for timing Analysis](#) application report. If needed, external logic hardware such as buffers may be used to compensate any timing differences.

### **5.9.2 Interface Clock Specifications**

#### **5.9.2.1 Interface Clock Terminology**

The interface clock is used at the system level to sequence the data and/or to control transfers accordingly with the interface protocol.

#### **5.9.2.2 Interface Clock Frequency**

The two interface clock characteristics are:

- The maximum clock frequency
- The maximum operating frequency

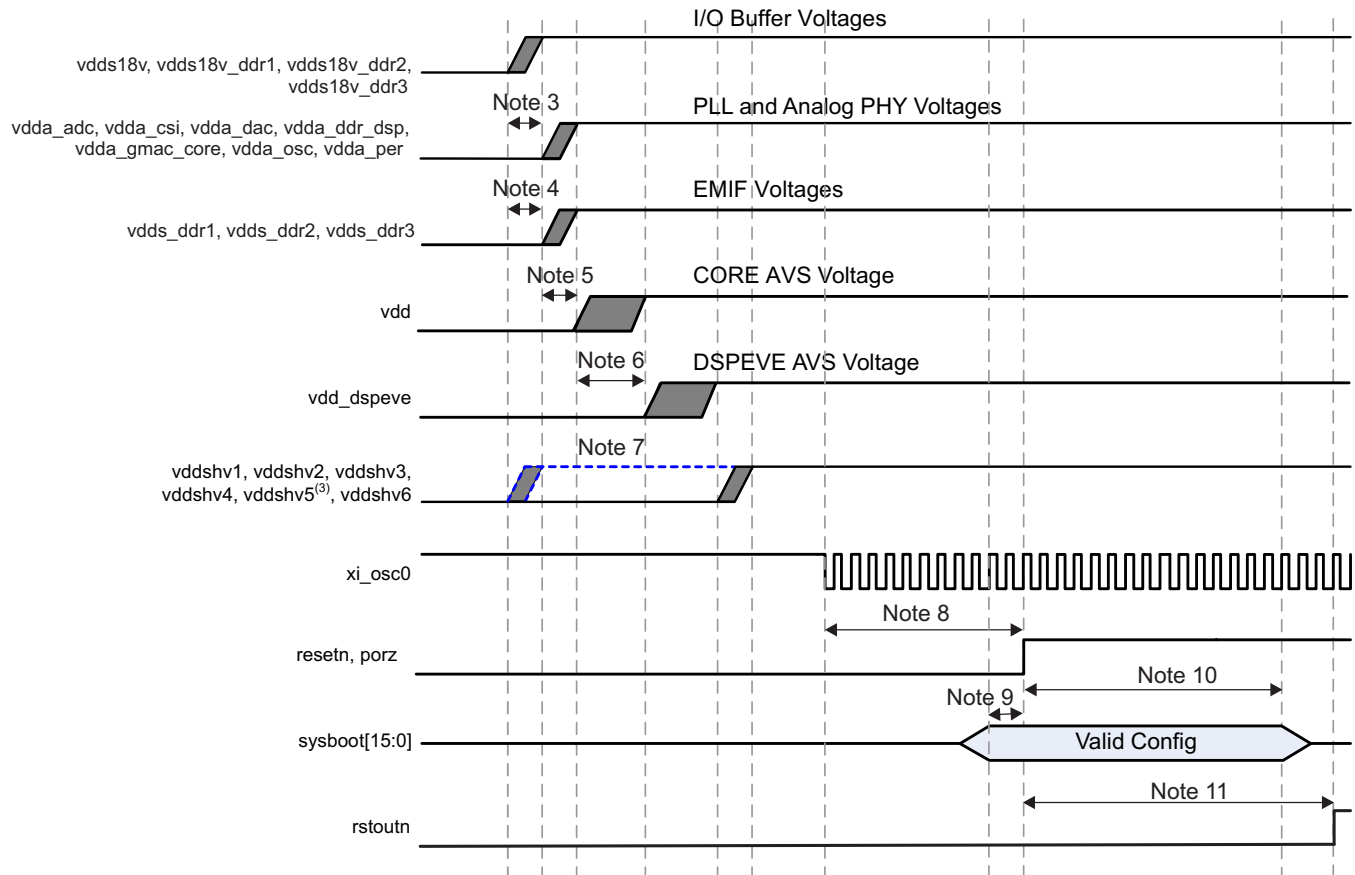
The interface clock frequency documented in this document is the maximum clock frequency, which corresponds to the maximum frequency programmable on this output clock. This frequency defines the maximum limit supported by the Device IC and does not take into account any system consideration (PCB, peripherals).

The system designer will have to consider these system considerations and the Device IC timing characteristics as well to define properly the maximum operating frequency that corresponds to the maximum frequency supported to transfer the data on this interface.

### 5.9.3 Power Supply Sequences

This section describes the power-up and power-down sequence required to ensure proper device operation.

Figure 5-4 through Figure 5-8, and associated notes describes the device Recommended Power Sequencing.

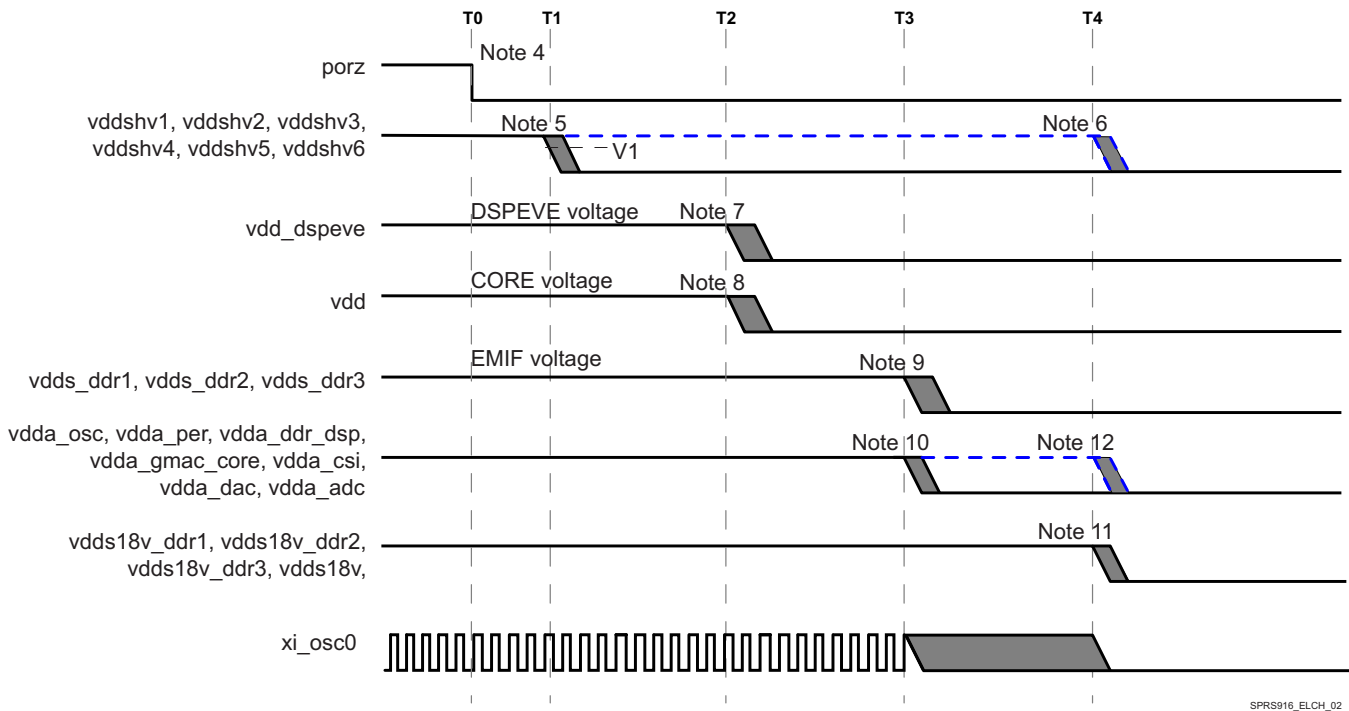


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**Figure 5-4. Power-Up Sequencing**

- (1) Grey shaded areas are windows where it is valid to ramp-up a voltage rail.
- (2) Blue dashed lines are not valid windows but show alternate ramp-up possibilities based on whether I/O voltage levels are 1.8V or 3.3V (see associated note for more details).
- (3) vdds18v\_\* and vdda\_\* rails should not be combined for best performance to avoid transient switching noise impacts on analog domains. vdda\_\* should not ramp-up before vdds18v\_\* but could ramp concurrently if design ensures final operational voltage will not be reached until after vdds18v\_\*. The preferred sequence is to follow all vdds18v\_\* to ensure circuit components and PCB design do not cause an inadvertent violation.
- (4) vdds\_ddr\* should not ramp-up before vdds18v\_\*. The preferred sequence is to follow all vdds18v\_\* to ensure circuit components and PCB design do not cause an inadvertent violation. vdds\_ddr\* can ramp-up before, concurrently or after vdda\_\*, there are no dependencies between vdds\_ddr\* and vdda\_\* domains.
  - vdds\_ddr\* supplies can be combined with vdds18v\_\* and vdds18v\_ddr supplies for DDR2 mode of operation (1.8V) and ramped up together for simplified power sequencing.
  - If vdds18v\_ddr and vdds\_ddr\* are kept separate from vdds18v\_\* on board, then this combined DDR supply can come up together or after the vdds18v\_\* supply. The DDR supply in this case should never ramp up before the vdds18v\_\*.
- (5) vdd should not ramp-up before vdds18v\_\* or vdds\_ddr\* domains.
- (6) vdd\_dspeve must not exceed vdd core supply and maintain at least 150mV lower voltage on vdd\_dspeve vs vdd. vdd\_dspeve could ramp concurrently with vdd if design ensures final operational voltage will not be reached until after vdd and maintains minimum of 150mV less than vdd during entire ramp time. The preferred sequence is to follow vdd to ensure circuit components and PCB design do not cause an inadvertent violation.

- (7) If any of the vddshv[1-6] power rails are used for 1.8V I/O signaling, then these rails can be combined with vdds18v\_\*. If 3.3V I/O signaling is required, then these rails must be the last to ramp following vdd\_dspeve.
- (8) resetn and porz must remain asserted low for a minimum of 12P<sup>(12)</sup> after xi\_osc0 is stable at a valid frequency.
- (9) Setup time: SYSBOOT[15:0] pins must be valid 2P<sup>(12)</sup> before porz is de-asserted high.
- (10) Hold time: SYSBOOT[15:0] pins must be valid 15P<sup>(12)</sup> after porz is de-asserted high.
- (11) resetn to rstoutn delay is 2ms.
- (12)  $P = 1/(\text{SYS\_CLK1}/610)$  frequency in ns.
- (13) Ramped Up is defined as reaching the minimum operational voltage level for the corresponding power domain. For information about voltage levels, refer to , *Recommended Operating Conditions*.



**Figure 5-5. Recommended Power-Down Sequencing**

- (1)  $T1 \geq 100 \mu\text{s}$ ;  $T2 = 500 \mu\text{s}$ ;  $T3 = 1.0 \text{ ms}$ ;  $T4 = 1.5 \text{ ms}$ ;  $V1 = 2.7 \text{ V}$ . All "Tn" markers are intended to show total elapsed time, not interval times.
- (2) Terminology:
  - $V_{\text{OPR MIN}}$  = Minimum Operational Voltage level that ensures device functionality and specified performance in [Section 5.4, Recommended Operating Conditions](#).
  - $V_{\text{OFF}}$  = OFF Voltage level is defined to be less than 0.6 V where any current draw has no impact to POH.
  - Ramp Down = transition time from  $V_{\text{OPR MIN}}$  to  $V_{\text{OFF}}$  and is slew rate independent.
- (3) General timing diagram items:
  - Grey shaded areas show valid transition times for supplies between  $V_{\text{OPR MIN}}$  and  $V_{\text{OFF}}$ .
  - Blue dashed lines are not valid windows but show alternate ramp possibilities based on the associated note.
  - Dashed vertical lines show approximate elapse times based upon T1 recommended PMIC power-down sequencer circuit performance.
- (4) porz must be asserted low for 100  $\mu\text{s}$  min to ensure SoC is set to a safe functional state before any voltage begins to ramp down.
- (5) vddshv[1-6] domains supplied by 3.3 V:
  - must remain greater than 2.7 V to enable Dual Voltage GPIO selector circuit operation for 100  $\mu\text{s}$  min after porz is asserted low.
  - must be in first group of supplies ramping down after porz has been asserted low for 100  $\mu\text{s}$  min.
  - must not exceed vdds18v by more than 2 V during ramp down, see [Figure 5-6, "vdds18v versus vddshv\[1-6\] Discharge Relationship"](#).
- (6) vddshv[1-6] domains supplied by 1.8 V must ramp down concurrently with vdds18v and be sourced from common vdds18v supply.
- (7) vdd\_dspeve domain can ramp down before or concurrently with vdd.
- (8) vdd must ramp down after or concurrently with vdd\_dspeve.
- (9) vdds\_ddr[1-3] domains:
  - should ramp down after vdd begins ramping down.

- If DDR2 memory is used (requiring 1.8V supply),
  - then vdds\_dds[1-3] can be combined with vdds18v and vdds18v\_dds[1-3] domains and sourced from a common supply. Accordingly, all domains can ramp down concurrently with vdds18v.
  - if vdds\_dds[1-3] and vdds18v\_dds[1-3] are combined but kept separate from vdds18v, then the combined 1.8V DDR supply can ramp down before or concurrently with vdds18v.

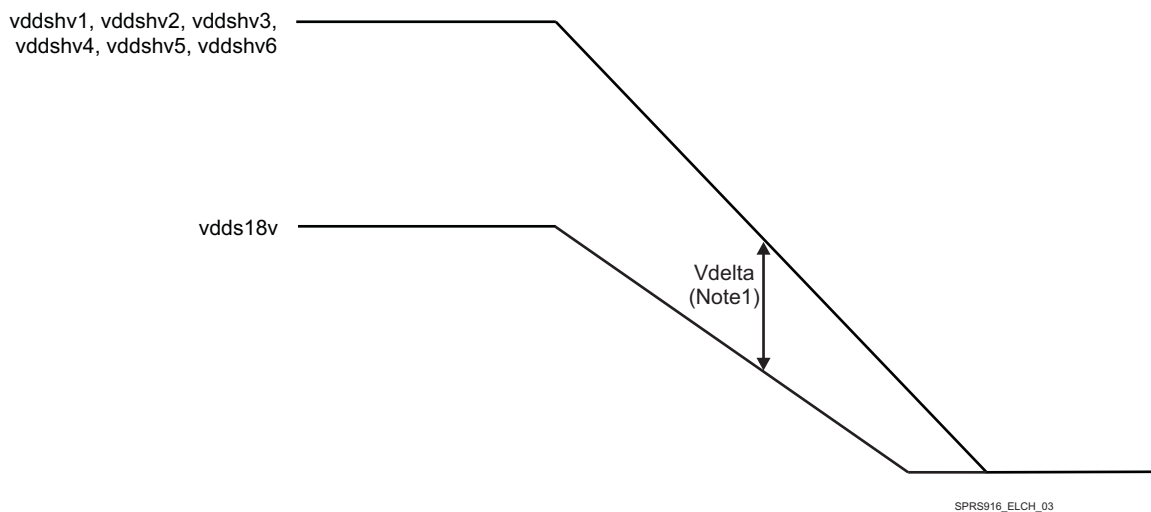
(10) vdda\_\* domains:

- can ramp down before, concurrently or after vdds\_dds[1-3], there is no dependency between these supplies.
- can ramp down before or concurrently with vdds18v.
- must satisfy the vdds18v versus vdda\_\* discharge relationship (see [Figure 5-8](#)) if any of the vdda\_\* disable point is later or discharge rate is slower than vdds18v.

(11) vdds18v domain:

- should maintain  $V_{OPR\ MIN}$  ( $V_{NOM} - 5\% = 1.71\ V$ ) until all other supplies start to ramp down.
- must satisfy the vdds18v versus vddshv[1-6] discharge relationship (see [Figure 5-6](#)) if any of the vddshv[1-6] is operating at 3.3 V.
- must satisfy the vdds18v versus vdds\_dds[1-3] discharge relationship ( see [Figure 5-7](#)) if vdds\_dds[1-3] discharge rate is slower than vdds18v.

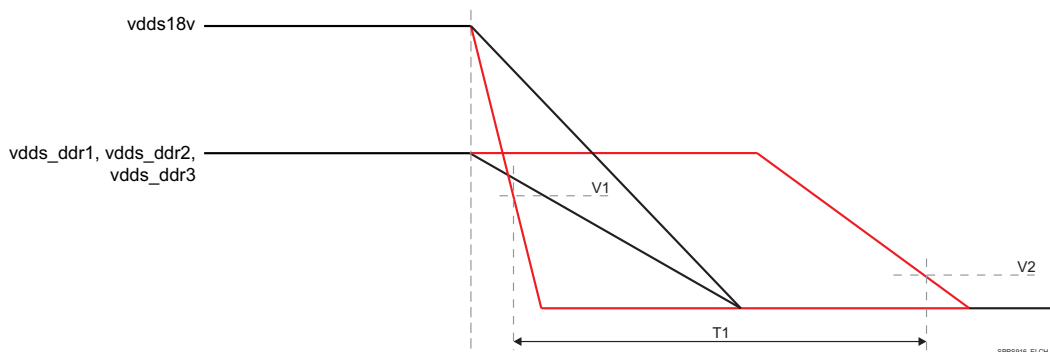
[Figure 5-6](#) describes vddshv[1-6] supplies falling before vdds18v supplies delta.



**Figure 5-6. vdds18v versus vddshv[1-6] Discharge Relationship**

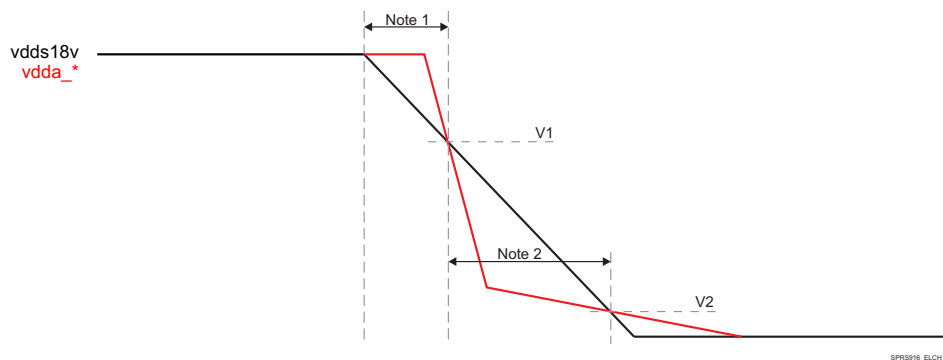
(1) Vdelta MAX = 2V

If vdds18v and vdds\_dds\* are disabled at the same time due to a loss of input power event or if vdds\_dds\* discharges more slowly than vdds18v, analysis has shown no reliability impacts when the elapsed time period beginning with vdds18v dropping below 1.0 V and ending with vdds\_dds\* dropping below 0.6 V is less than 10 ms (Figure 5-7).



**Figure 5-7. vdds18v and vdds\_dds\* Discharge Relationship<sup>(1)</sup>**

(1)  $V1 > 1.0 \text{ V}$ ;  $V2 < 0.6 \text{ V}$ ;  $T1 < 10\text{ms}$ .

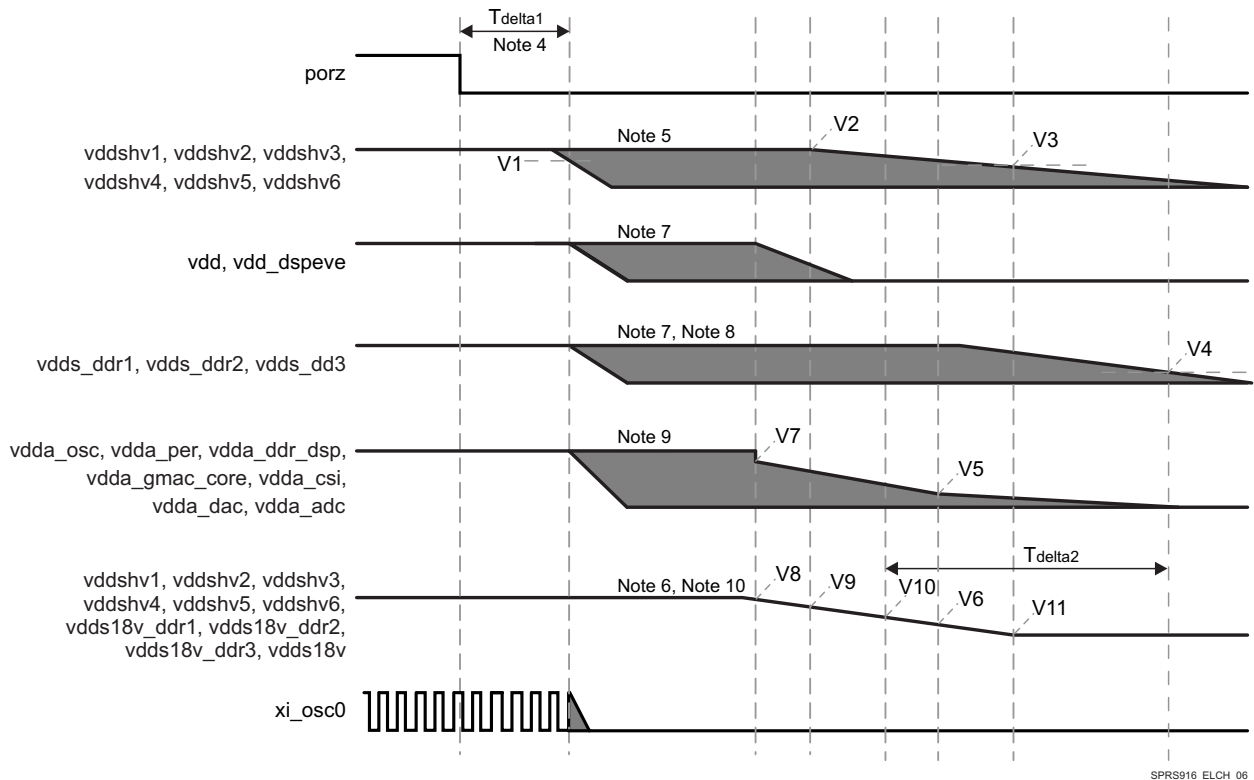


**Figure 5-8. vdds18v and vdda\_\* Discharge Relationship<sup>(3)</sup>**

- (1) vdda\_\* can be  $\geq$  vdds18v, until vdds18v drops below 1.62 V.
- (2) vdds18v must be  $\geq$  vdda\_\*, until vdds18v reaches 0.6 V.
- (3)  $V1 = 1.62 \text{ V}$ ;  $V2 < 0.6 \text{ V}$ .

Figure 5-6 through Figure 5-9 and associated notes described the device Abrupt Power Down Sequence.

A "loss of input power event" occurs when the system's input power is unexpectedly removed. Normally, the recommended power-down sequence should be followed and can be accomplished within 1.5-2 ms of elapsed time. This is the typical range of elapsed time available following a loss of power event, see 7.3.7, *Loss of Input Power Event* for design recommendations. If sufficient elapse time is not provided, then an "abrupt" power-down sequence can be supported without impacting POH reliability if all of the following conditions are met (Figure 5-9).



**Figure 5-9. Abrupt Power-Down Sequencing<sup>(1)</sup>**

- (1) V1 = 2.7 V; V2 = 3.3 V; V3 = 2.0 V; V4 = V5 = V6 = 0.6 V; V7 = V8 = 1.62 V; V9 = 1.3 V; V10 = 1.0 V; V11 = 0.0 V;  $T_{\Delta 1} > 100 \mu s$ ;  $T_{\Delta 2} < 10 ms$ .
- (2) Terminology:
  - $V_{OPR MIN}$  = Minimum Operational Voltage level that ensures device functionality and specified performance in Section 5.4, *Recommended Operating Conditions*.
  - $V_{OFF}$  = OFF Voltage level is defined to be less than 0.6 V, where any current draw has no impact to POH.
  - Ramp Down = transition time from  $V_{OPR MIN}$  to  $V_{OFF}$  and is slew rate independent.
- (3) General timing diagram items:
  - Grey shaded areas show valid transition times for supplies between  $V_{OPR MIN}$  and  $V_{OFF}$ .
  - Dashed vertical lines show approximate elapse times based upon TI recommended PMIC power-down sequencer circuit performance.
- (4) porz must be asserted low for 100  $\mu s$  min to ensure SoC is set to a safe functional state before any voltage begins to ramp down.
- (5) vddshv[1-6] domains supplied by 3.3 V:
  - must remain greater than 2.7 V to enable Dual Voltage GPIO selector circuit operation for 100  $\mu s$  min, after porz is asserted low.
  - must not exceed vdds18v voltage level by more than 2V during ramp down, until vdds18v drops below  $V_{OFF}$  (0.6 V).
- (6) vddshv[1-6] domains supplied by 1.8 V must ramp down concurrently with vdds18v and be sourced from common vdds18v supply.
- (7) vdd\_speve, vdd, vdds\_dds[1-3], vdda\_\* domains can all start to ramp down in any order after 100  $\mu s$  low assertion of porz.
- (8) vdds\_dds\* domains:
  - can remain at  $V_{OPR MIN}$  or a level greater than vdds18v during ramp down.
  - elapsed time from vdds18v dropping below 1.0 V to vdds\_dds[1-3] dropping below 0.6 V must not exceed 10 ms.
- (9) vdda\_\* domains:

- can start to ramp down before or concurrently with vdds18v.
  - must not exceed vdds18v voltage level after vdds18v drops below 1.62 V until vdds18v drops below  $V_{OFF}$  (0.6 V).
- (10) vdds18v domain should maintain a minimum level of 1.62 V ( $V_{NOM} - 10\%$ ) until vdd\_dspeve and vdd start to ramp down.

## 5.9.4 Clock Specifications

### NOTE

For more information, see Power, Reset, and Clock Management / PRCM Subsystem Environment / External Clock Signals and Clock Management Functional Description section of the Device TRM.

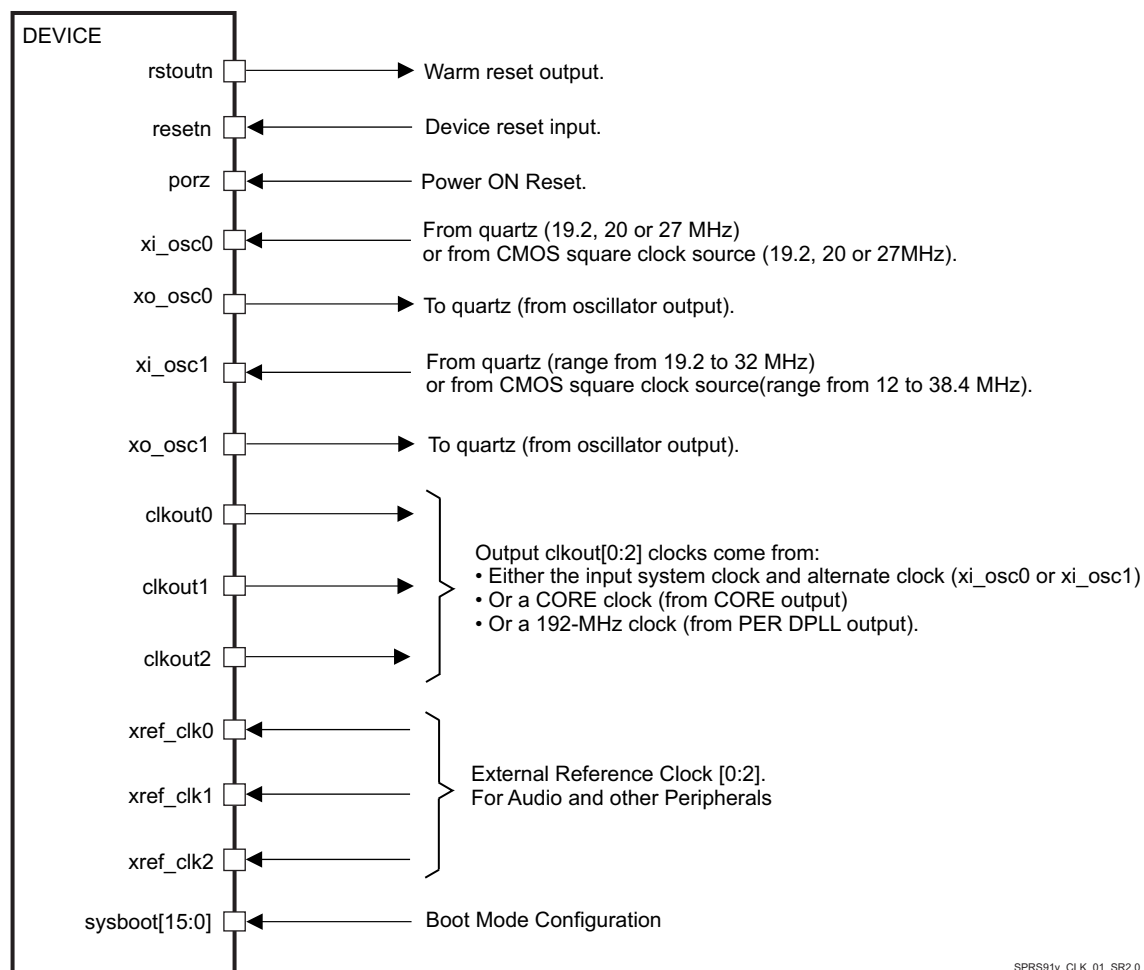
### NOTE

Audio Back End (ABE) module is not supported for this family of devices, but “ABE” name is still present in some clock or DPLL names.

The device operation requires the following clocks:

- The system clocks, SYS\_CLK1(Mandatory) and SYS\_CLK2(Optional) are the main clock sources of the device. They supply the reference clock to the DPLLs as well as functional clock to several modules.

Figure 5-10 shows the external input clock sources and the output clocks to peripherals.



**Figure 5-10. Clock Interface**

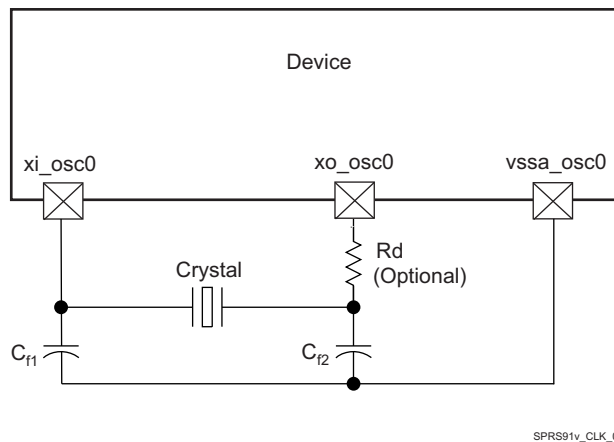
#### 5.9.4.1 Input Clocks / Oscillators

- The source of the internal system clock (SYS\_CLK1) could be either:
  - A CMOS clock that enters on the xi\_osc0 ball (with xo\_osc0 left unconnected on the CMOS clock case).
  - A crystal oscillator clock managed by xi\_osc0 and xo\_osc0.
- The source of the internal system clock (SYS\_CLK2) could be either:
  - A CMOS clock that enters on the xi\_osc1 ball (with xo\_osc1 left unconnected on the CMOS clock case).
  - A crystal oscillator clock managed by xi\_osc1 and xo\_osc1.

SYS\_CLK1 is received directly from oscillator OSC0. For more information about SYS\_CLK1 see Device TRM, Chapter: *Power, Reset, and Clock Management*.

##### 5.9.4.1.1 OSC0 External Crystal

An external crystal is connected to the device pins. [Figure 5-11](#) describes the crystal implementation.



**Figure 5-11. Crystal Implementation**

#### NOTE

The load capacitors,  $C_{f1}$  and  $C_{f2}$  in [Figure 5-11](#), should be chosen such that the below equation is satisfied.  $C_L$  in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator xi\_osc0, xo\_osc0, and vssa\_osc0 pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

**Figure 5-12. Load Capacitance Equation**

The crystal must be in the fundamental mode of operation and parallel resonant. [Table 5-15](#) summarizes the required electrical constraints.

**Table 5-15. OSC0 Crystal Electrical Characteristics**

| NAME                  | DESCRIPTION                                                                     | MIN          | TYP | MAX | UNIT     |
|-----------------------|---------------------------------------------------------------------------------|--------------|-----|-----|----------|
| $f_p$                 | Parallel resonance crystal frequency                                            | 19.2, 20, 27 |     |     | MHz      |
| $C_{f1}$              | $C_{f1}$ load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$ | 12           |     | 24  | pF       |
| $C_{f2}$              | $C_{f2}$ load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$ | 12           |     | 24  | pF       |
| $ESR(C_{f1}, C_{f2})$ | Crystal ESR                                                                     |              |     | 100 | $\Omega$ |

**Table 5-15. OSC0 Crystal Electrical Characteristics (continued)**

| NAME                    | DESCRIPTION                                             |                                    | MIN                      | TYP           | MAX  | UNIT |
|-------------------------|---------------------------------------------------------|------------------------------------|--------------------------|---------------|------|------|
| C <sub>O</sub>          | Crystal shunt capacitance                               | ESR = 30 Ω<br>ESR = 40 Ω           | 19.2 MHz, 20 MHz, 27 MHz |               | 7    | pF   |
|                         |                                                         | ESR = 50 Ω                         | 19.2 MHz, 20 MHz         |               | 7    | pF   |
|                         |                                                         |                                    | 27 MHz                   |               | 5    | pF   |
|                         |                                                         | ESR = 60 Ω                         | 19.2 MHz, 20 MHz         |               | 7    | pF   |
|                         |                                                         |                                    | 27 MHz                   | Not Supported |      | -    |
|                         |                                                         | ESR = 80 Ω                         | 19.2 MHz, 20 MHz         |               | 5    | pF   |
|                         |                                                         |                                    | 27 MHz                   | Not Supported |      | -    |
|                         |                                                         | ESR = 100 Ω                        | 19.2 MHz, 20 MHz         |               | 3    | pF   |
|                         |                                                         |                                    | 27 MHz                   | Not Supported |      | -    |
| L <sub>M</sub>          | Crystal motional inductance for f <sub>p</sub> = 20 MHz |                                    |                          | 10.16         |      | mH   |
| C <sub>M</sub>          | Crystal motional capacitance                            |                                    |                          | 3.42          |      | fF   |
| f <sub>j(xi_osc0)</sub> | Frequency accuracy <sup>(1)</sup> , xi_osc0             | Ethernet not used                  |                          |               | ±200 | ppm  |
|                         |                                                         | Ethernet RGMII using derived clock |                          |               | ±50  | ppm  |

(1) Crystal characteristics should account for tolerance+stability+aging.

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

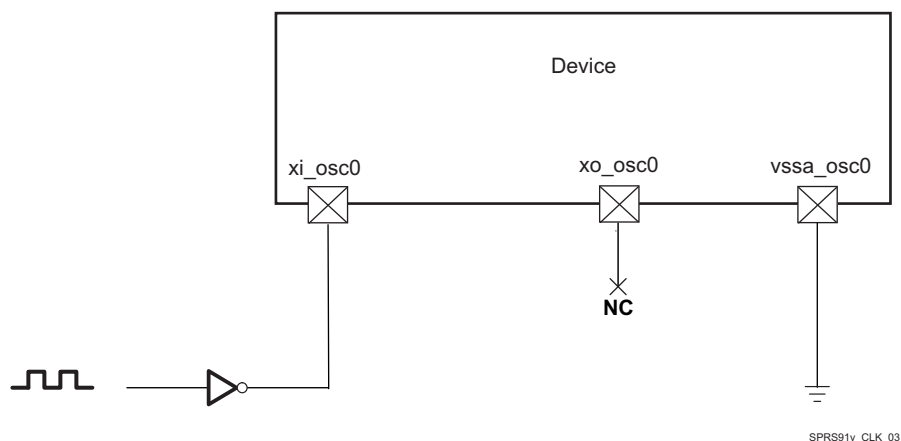
Table 5-16 details the switching characteristics of the oscillator and the requirements of the input clock.

**Table 5-16. Oscillator Switching Characteristics—Crystal Mode**

| NAME            | DESCRIPTION           | MIN              | TYP | MAX | UNIT |
|-----------------|-----------------------|------------------|-----|-----|------|
| f <sub>p</sub>  | Oscillation frequency | 19.2, 20, 27 MHz |     |     | MHz  |
| t <sub>sx</sub> | Start-up time         |                  |     | 4   | ms   |

#### 5.9.4.1.2 OSC0 Input Clock

A 1.8-V LVCMOS-Compatible Clock Input can be used instead of the internal oscillator to provide the SYS\_CLK1 clock input to the system. The external connections to support this are shown in Figure 5-13. The xi\_osc0 pin is connected to the 1.8-V LVCMOS-Compatible clock source. The xi\_osc0 pin is left unconnected. The vssa\_osc0 pin is connected to board ground (vss).



**Figure 5-13. 1.8-V LVCMOS-Compatible Clock Input**

Table 5-17 summarizes the OSC0 input clock electrical characteristics.

**Table 5-17. OSC0 Input Clock Electrical Characteristics—Bypass Mode**

| NAME            | DESCRIPTION               | MIN          | TYP   | MAX   | UNIT |
|-----------------|---------------------------|--------------|-------|-------|------|
| f               | Frequency                 | 19.2, 20, 27 |       |       | MHz  |
| C <sub>IN</sub> | Input capacitance         | 2.184        | 2.384 | 2.584 | pF   |
| I <sub>IN</sub> | Input current (3.3V mode) | 4            | 6     | 10    | μA   |

Table 5-18 details the OSC0 input clock timing requirements.

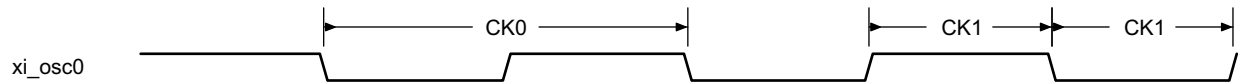
**Table 5-18. OSC0 Input Clock Timing Requirements**

| NAME | DESCRIPTION                 |                                             | MIN                                | TYP | MAX                            | UNIT |
|------|-----------------------------|---------------------------------------------|------------------------------------|-----|--------------------------------|------|
| CK0  | 1 / t <sub>c(xi_osc0)</sub> | Frequency, xi_osc0                          | 19.2, 20, 27                       |     |                                | MHz  |
| CK1  | t <sub>w(xi_osc0)</sub>     | Pulse duration, xi_osc0 low or high         | 0.45 × t <sub>c(xi_osc0)</sub>     |     | 0.55 × t <sub>c(xi_osc0)</sub> | ns   |
|      | t <sub>j(xi_osc0)</sub>     | Period jitter <sup>(1)</sup> , xi_osc0      |                                    |     | 0.01 × t <sub>c(xi_osc0)</sub> | ns   |
|      | t <sub>R(xi_osc0)</sub>     | Rise time, xi_osc0                          |                                    |     | 5                              | ns   |
|      | t <sub>F(xi_osc0)</sub>     | Fall time, xi_osc0                          |                                    |     | 5                              | ns   |
|      | t <sub>j(xi_osc0)</sub>     | Frequency accuracy <sup>(2)</sup> , xi_osc0 | Ethernet not used                  |     | ±200                           | ppm  |
|      |                             |                                             | Ethernet RGMII using derived clock |     | ±50                            | ppm  |

(1) Period jitter is meant here as follows:

- The maximum value is the difference between the longest measured clock period and the expected clock period
- The minimum value is the difference between the shortest measured clock period and the expected clock period

(2) Crystal characteristics should account for tolerance+stability+aging.



SPRS91v\_CLK\_04

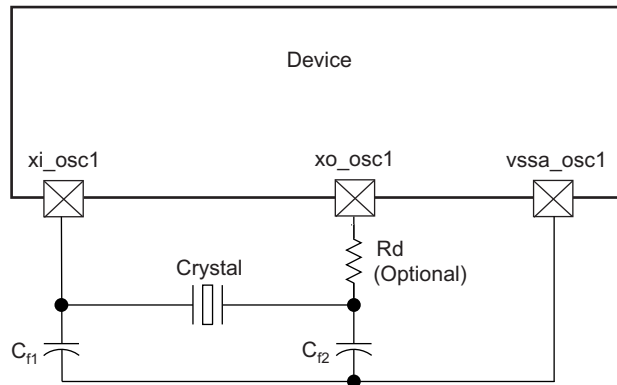
**Figure 5-14. xi\_osc0 Input Clock**

#### 5.9.4.1.3 Auxiliary Oscillator OSC1 Input Clock

SYS\_CLK2 is received directly from oscillator OSC1. For more information about SYS\_CLK2 see Device TRM, Chapter: *Power, Reset, and Clock Management*.

##### 5.9.4.1.3.1 OSC1 External Crystal

An external crystal is connected to the device pins. Figure 5-15 describes the crystal implementation.



SPRS91v\_CLK\_05

**Figure 5-15. Crystal Implementation**

**NOTE**

The load capacitors,  $C_{f1}$  and  $C_{f2}$  in [Figure 5-15](#), should be chosen such that the below equation is satisfied.  $C_L$  in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator  $xi\_osc1$ ,  $xo\_osc1$ , and  $vssa\_osc1$  pins.

$$C_L = \frac{C_{f1} C_{f2}}{C_{f1} + C_{f2}}$$

**Figure 5-16. Load Capacitance Equation**

The crystal must be in the fundamental mode of operation and parallel resonant. [Table 5-19](#) summarizes the required electrical constraints.

**Table 5-19. OSC1 Crystal Electrical Characteristics**

| NAME                                   | DESCRIPTION                                                                                            |             |                                    | MIN                   | TYP   | MAX | UNIT |
|----------------------------------------|--------------------------------------------------------------------------------------------------------|-------------|------------------------------------|-----------------------|-------|-----|------|
| f <sub>p</sub>                         | Parallel resonance crystal frequency                                                                   |             |                                    | Range from 19.2 to 32 |       |     | MHz  |
| C <sub>f1</sub>                        | C <sub>f1</sub> load capacitance for crystal parallel resonance with C <sub>f1</sub> = C <sub>f2</sub> |             |                                    | 12                    |       | 24  | pF   |
| C <sub>f2</sub>                        | C <sub>f2</sub> load capacitance for crystal parallel resonance with C <sub>f1</sub> = C <sub>f2</sub> |             |                                    | 12                    |       | 24  | pF   |
| ESR(C <sub>f1</sub> ,C <sub>f2</sub> ) | Crystal ESR                                                                                            |             |                                    |                       |       | 100 | Ω    |
| C <sub>O</sub>                         | Crystal shunt capacitance                                                                              | ESR = 30 Ω  | 19.2 MHz ≤ f <sub>p</sub> ≤ 32 MHz |                       |       | 7   | pF   |
|                                        |                                                                                                        | ESR = 40 Ω  | 19.2 MHz ≤ f <sub>p</sub> ≤ 32 MHz |                       |       | 5   | pF   |
|                                        |                                                                                                        | ESR = 50 Ω  | 19.2 MHz ≤ f <sub>p</sub> ≤ 25 MHz |                       |       | 7   | pF   |
|                                        |                                                                                                        |             | 25 MHz < f <sub>p</sub> ≤ 27 MHz   |                       |       | 5   | pF   |
|                                        |                                                                                                        |             | 27 MHz < f <sub>p</sub> ≤ 32 MHz   | Not Supported         |       |     | -    |
|                                        |                                                                                                        | ESR = 60 Ω  | 19.2 MHz ≤ f <sub>p</sub> ≤ 23 MHz |                       |       | 7   | pF   |
|                                        |                                                                                                        |             | 23 MHz < f <sub>p</sub> ≤ 25 MHz   |                       |       | 5   | pF   |
|                                        |                                                                                                        |             | 25 MHz < f <sub>p</sub> ≤ 32 MHz   | Not Supported         |       |     | -    |
|                                        |                                                                                                        | ESR = 80 Ω  | 19.2 MHz ≤ f <sub>p</sub> ≤ 23 MHz |                       |       | 5   | pF   |
|                                        |                                                                                                        |             | 23 MHz < f <sub>p</sub> ≤ 25 MHz   |                       |       | 3   | pF   |
|                                        |                                                                                                        |             | 25 MHz < f <sub>p</sub> ≤ 32 MHz   | Not Supported         |       |     | -    |
|                                        |                                                                                                        | ESR = 100 Ω | 19.2 MHz ≤ f <sub>p</sub> ≤ 20 MHz |                       |       | 3   | pF   |
| 20 MHz < f <sub>p</sub> ≤ 32 MHz       | Not Supported                                                                                          |             |                                    | -                     |       |     |      |
| L <sub>M</sub>                         | Crystal motional inductance for f <sub>p</sub> = 20 MHz                                                |             |                                    |                       | 10.16 |     | mH   |
| C <sub>M</sub>                         | Crystal motional capacitance                                                                           |             |                                    |                       | 3.42  |     | fF   |

**Table 5-19. OSC1 Crystal Electrical Characteristics (continued)**

| NAME            | DESCRIPTION                                 | MIN                                | TYP | MAX  | UNIT |
|-----------------|---------------------------------------------|------------------------------------|-----|------|------|
| $t_{j(xiosc0)}$ | Frequency accuracy <sup>(1)</sup> , xi_osc1 | Ethernet not used                  |     | ±200 | ppm  |
|                 |                                             | Ethernet RGMII using derived clock |     | ±50  | ppm  |

(1) Crystal characteristics should account for tolerance+stability+aging.

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

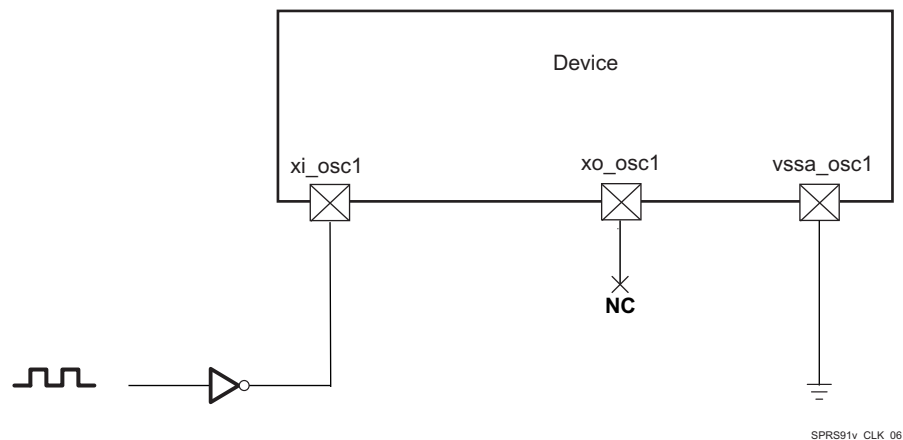
Table 5-20 details the switching characteristics of the oscillator and the requirements of the input clock.

**Table 5-20. Oscillator Switching Characteristics—Crystal Mode**

| NAME     | DESCRIPTION           | MIN                   | TYP | MAX | UNIT |
|----------|-----------------------|-----------------------|-----|-----|------|
| $f_p$    | Oscillation frequency | Range from 19.2 to 32 |     |     | MHz  |
| $t_{sX}$ | Start-up time         |                       |     | 4   | ms   |

#### 5.9.4.1.3.2 OSC1 Input Clock

A 1.8-V LVCMOS-Compatible Clock Input can be used instead of the internal oscillator to provide the SYS\_CLK2 clock input to the system. The external connections to support this are shown in, Figure 5-17. The xi\_osc1 pin is connected to the 1.8-V LVCMOS-Compatible clock sources. The xo\_osc1 pin is left unconnected. The vssa\_osc1 pin is connected to board ground (VSS).



**Figure 5-17. 1.8-V LVCMOS-Compatible Clock Input**

Table 5-21 summarizes the OSC1 input clock electrical characteristics.

**Table 5-21. OSC1 Input Clock Electrical Characteristics—Bypass Mode**

| NAME     | DESCRIPTION                  | MIN                   | TYP   | MAX   | UNIT |
|----------|------------------------------|-----------------------|-------|-------|------|
| $f$      | Frequency                    | Range from 12 to 38.4 |       |       | MHz  |
| $C_{IN}$ | Input capacitance            | 2.819                 | 3.019 | 3.219 | pF   |
| $I_{IN}$ | Input current (3.3V mode)    | 4                     | 6     | 10    | μA   |
| $t_{sX}$ | Start-up time <sup>(1)</sup> | See <sup>(2)</sup>    |       |       | ms   |

(1) To switch from bypass mode to crystal or from crystal mode to bypass mode, there is a waiting time about 100 μs; however, if the chip comes from bypass mode to crystal mode the crystal will start-up after time mentioned in Table 5-20,  $t_{sX}$  parameter.

(2) Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is in application mode and receives a wave. The switching time in this case is about 100 μs.

Table 5-22 details the OSC1 input clock timing requirements.

**Table 5-22. OSC1 Input Clock Timing Requirements**

| NAME | DESCRIPTION           |                                             | MIN                                | TYP | MAX                                          | UNIT |
|------|-----------------------|---------------------------------------------|------------------------------------|-----|----------------------------------------------|------|
| CK0  | $1 / t_{c(xi\_osc1)}$ | Frequency, xi_osc1                          | Range from 12 to 38.4              |     |                                              | MHz  |
| CK1  | $t_{w(xi\_osc1)}$     | Pulse duration, xi_osc1 low or high         | $0.45 \times t_{c(xi\_osc1)}$      |     | $0.55 \times t_{c(xi\_osc1)}$                | ns   |
|      | $t_{j(xi\_osc1)}$     | Period jitter <sup>(1)</sup> , xi_osc1      |                                    |     | $0.01 \times t_{c(xi\_osc1)}$ <sup>(3)</sup> | ns   |
|      | $t_{R(xi\_osc1)}$     | Rise time, xi_osc1                          |                                    |     | 5                                            | ns   |
|      | $t_{F(xi\_osc1)}$     | Fall time, xi_osc1                          |                                    |     | 5                                            | ns   |
|      | $t_{j(xi\_osc1)}$     | Frequency accuracy <sup>(2)</sup> , xi_osc1 | Ethernet not used                  |     | ±200                                         | ppm  |
|      |                       |                                             | Ethernet RGMII using derived clock |     | ±50                                          | ppm  |

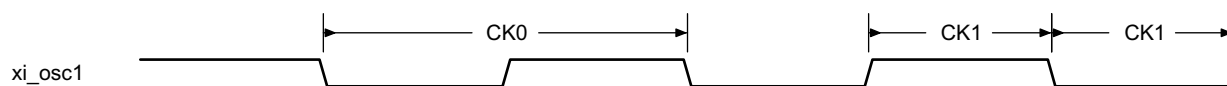
(1) Period jitter is meant here as follows:

- The maximum value is the difference between the longest measured clock period and the expected clock period
- The minimum value is the difference between the shortest measured clock period and the expected clock period

(2) Crystal characteristics should account for tolerance+stability+aging.

(3) The Period jitter requirement for osc1 can be relaxed to  $0.02 \times t_{c(xi\_osc1)}$  under the following constraints:

- The osc1/SYS\_CLK2 clock bypasses all device PLLs
- The osc1/SYS\_CLK2 clock is only used to source the DSS pixel clock outputs



SPRS91v\_CLK\_07

**Figure 5-18. xi\_osc1 Input Clock**

#### 5.9.4.1.4 RC On-die Oscillator Clock

RCOSC\_32K\_CLK is received directly through a network of resistor and capacitor (an RC network) inside of the SoC. This RC oscillator do not have good frequency stability. The Frequency range is described in [Table 5-23](#), which depends on the temperature. For more information about RCOSC\_32K\_CLK see the Device TRM, Chapter: *Power, Reset, and Clock Management*.

**Table 5-23. RC On-die Oscillator Clock Frequency Range**

| NAME          | DESCRIPTION            | MIN                 | TYP | MAX | UNIT |
|---------------|------------------------|---------------------|-----|-----|------|
| RCOSC_32K_CLK | Internal RC Oscillator | Range from 28 to 42 |     |     | kHz  |

#### 5.9.4.2 Output Clocks

The device provides three output clocks. Summary of these output clocks are as follows:

- clkout1 - Device Clock output 1. Can be used as a system clock for other devices. The source of the clkout1 could be either:
  - The input system clock and alternate clock (xi\_osc0 or xi\_osc1)
  - CORE clock (from CORE output)
  - 192-MHz clock (from PER DPLL output)
- clkout2 - Device Clock output 2. Can be used as a system clock for other devices. The source of the clkout2 could be either:
  - The input system clock and alternate clock (xi\_osc0 or xi\_osc1)
  - CORE clock (from CORE output)
  - 192-MHz clock (from PER DPLL output)

- clkout3 - Device Clock output 3. Can be used as a system clock for other devices. The source of the clkout3 could be either:
  - The input system clock and alternate clock (xi\_osc0 or xi\_osc1)
  - CORE clock (from CORE output)
  - 192-MHz clock (from PER DPLL output)

For more information about Output Clocks see Device TRM, Chapter: *Power, Reset, and Clock Management*.

### 5.9.4.3 DPLLs, DLLs

#### NOTE

For more information, see:

- Power, Reset, and Clock Management / Clock Management Functional Description / Internal Clock Sources / Generators / Generic DPLL Overview Section and
- Display Subsystem / Display Subsystem Overview section of the Device TRM.

To generate high-frequency clocks, the device supports multiple on-chip DPLLs controlled directly by the PRCM module.

- They have their own independent power domain (each one embeds its own switch and can be controlled as an independent functional power domain)
- They are fed with ALWAYS ON system clock, with independent control per DPLL.

The different DPLLs managed by the PRCM are listed below:

- DPLL\_CORE: It supplies all interface clocks and also few module functional clocks.
- DPLL\_PER: It supplies several clock sources: a 192-MHz clock for the display functional clock , a 96-MHz functional clock to subsystems and peripherals.
- DPLL\_GMAC\_DSP: It supplies RGMII, EVE1 and DSP0 module functional clocks.
- DPLL\_EVE\_VID\_DSP: It provides a few module functional clocks (EVE\_GFCLK, VID\_PIX\_CLK and DSP1\_CLK).
- DPLL\_DDR: It generates clocks for the one External Memory Interface (EMIF) controller and its associated EMIF PHYs.

#### NOTE

The following DPLLs are controlled by the clock manager located in the always-on Core power domain (CM\_CORE\_AON):

- DPLL\_CORE, DPLL\_DDR, DPLL\_GMAC\_DSP, DPLL\_PER, DPLL\_EVE\_VID\_DSP.

For more information on CM\_CORE\_AON and CM\_CORE or PRCM DPLLs, see the Power, Reset, and Clock Management (PRCM) chapter of the Device TRM.

#### 5.9.4.3.1 DPLL Characteristics

The DPLL has three relevant input clocks. One of them is the reference clock (CLKINP) used to generated the synthesized clock but can also be used as the bypass clock whenever the DPLL enters a bypass mode. It is therefore mandatory. The second one is a fast bypass clock (CLKINPULOW) used when selected as the bypass clock and is optional. The third clock (CLKINPHIF) is explained in the next paragraph.

The DPLL has three output clocks (namely CLKOUT, CLKOUTX2, and CLKOUTHIF). CLKOUT and CLKOUTX2 run at the bypass frequency whenever the DPLL enters a bypass mode. Both of them are generated from the lock frequency divided by a post-divider (namely M2 post-divider). The third clock, CLKOUTHIF, has no automatic bypass capability. It is an output of a post-divider (M3 post-divider) with the input clock selectable between the internal lock clock (Fdpll) and CLKINPHIF input of the PLL through an asynchronous multiplexing.

For more information, see the Power, Reset, and Clock Management chapter of the Device TRM.

Table 5-24 summarizes DPLL type described in Section 5.9.4.3, *DPLLs, DLLs Specifications*.

**Table 5-24. DPLL Control**

| DPLL NAME        | CONTROLLED BY PRCM |
|------------------|--------------------|
| DPLL_CORE        | Yes <sup>(1)</sup> |
| DPLL_EVE_VID_DSP | Yes <sup>(1)</sup> |
| DPLL_GMAC_DSP    | Yes <sup>(1)</sup> |
| DPLL_PER         | Yes <sup>(1)</sup> |
| DPLL_DDR         | Yes <sup>(1)</sup> |

(1) DPLL is in the always-on domain.

Table 5-25 and summarize the DPLL characteristics and assume testing over recommended operating conditions.

**Table 5-25. DPLL Characteristics**

| NAME                    | DESCRIPTION                                                              | MIN               | TYP | MAX                               | UNIT | COMMENTS                                                                                            |
|-------------------------|--------------------------------------------------------------------------|-------------------|-----|-----------------------------------|------|-----------------------------------------------------------------------------------------------------|
| $f_{\text{input}}$      | CLKINP input frequency                                                   | 0.032             |     | 52                                | MHz  | $F_{\text{INP}}$                                                                                    |
| $f_{\text{internal}}$   | Internal reference frequency                                             | 0.15              |     | 52                                | MHz  | REFCLK                                                                                              |
| $f_{\text{CLKINPHIF}}$  | CLKINPHIF input frequency                                                | 10                |     | 1400                              | MHz  | $F_{\text{INPHIF}}$                                                                                 |
| $f_{\text{CLKINPULOW}}$ | CLKINPULOW input frequency                                               | 0.001             |     | 600                               | MHz  | Bypass mode: $f_{\text{CLKOUT}} = f_{\text{CLKINPULOW}} / (M1 + 1)$ if ulowclken = 1 <sup>(6)</sup> |
| $f_{\text{CLKOUT}}$     | CLKOUT output frequency                                                  | 20 <sup>(1)</sup> |     | 1800 <sup>(2)</sup>               | MHz  | $[M / (N + 1)] \times F_{\text{INP}} \times [1 / M2]$ (in locked condition)                         |
| $f_{\text{CLKOUTX2}}$   | CLKOUTx2 output frequency                                                | 40 <sup>(1)</sup> |     | 2200 <sup>(2)</sup>               | MHz  | $2 \times [M / (N + 1)] \times F_{\text{INP}} \times [1 / M2]$ (in locked condition)                |
| $f_{\text{CLKOUTHIF}}$  | CLKOUTHIF output frequency                                               | 20 <sup>(3)</sup> |     | 1400 <sup>(4)</sup>               | MHz  | $F_{\text{INPHIF}} / M3$ if clkinphifsel = 1                                                        |
|                         |                                                                          | 40 <sup>(3)</sup> |     | 2200 <sup>(4)</sup>               | MHz  | $2 \times [M / (N + 1)] \times F_{\text{INP}} \times [1 / M3]$ if clkinphifsel = 0                  |
| $f_{\text{CLKDCOLDO}}$  | DCOCLKLDO output frequency                                               | 40                |     | 2800                              | MHz  | $2 \times [M / (N + 1)] \times F_{\text{INP}}$ (in locked condition)                                |
| $t_{\text{lock}}$       | Frequency lock time                                                      |                   |     | $6 + 350 \times \text{REFCLK}$    | μs   |                                                                                                     |
| $p_{\text{lock}}$       | Phase lock time                                                          |                   |     | $6 + 500 \times \text{REFCLK}$    | μs   |                                                                                                     |
| $t_{\text{relock-L}}$   | Relock time—Frequency lock <sup>(5)</sup> (LP relock time from bypass)   |                   |     | $6 + 70 \times \text{REFCLK}$     | μs   | DPLL in LP relock time: lowcurrstdby = 1                                                            |
| $p_{\text{relock-L}}$   | Relock time—Phase lock <sup>(5)</sup> (LP relock time from bypass)       |                   |     | $6 + 120 \times \text{REFCLK}$    | μs   | DPLL in LP relock time: lowcurrstdby = 1                                                            |
| $t_{\text{relock-F}}$   | Relock time—Frequency lock <sup>(5)</sup> (fast relock time from bypass) |                   |     | $3.55 + 70 \times \text{REFCLK}$  | μs   | DPLL in fast relock time: lowcurrstdby = 0                                                          |
| $p_{\text{relock-F}}$   | Relock time—Phase lock <sup>(5)</sup> (fast relock time from bypass)     |                   |     | $3.55 + 120 \times \text{REFCLK}$ | μs   | DPLL in fast relock time: lowcurrstdby = 0                                                          |

(1) The minimum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.

For M2 > 1, the minimum frequency on these clocks will further scale down by factor of M2.

(2) The maximum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.

(3) The minimum frequency on CLKOUTHIF is assuming M3 = 1. For M3 > 1, the minimum frequency on this clock will further scale down by factor of M3.

(4) The maximum frequency on CLKOUTHIF is assuming M3 = 1.

(5) Relock time assumes typical operating conditions, 10°C maximum temperature drift.

(6) Bypass mode:  $f_{\text{CLKOUT}} = F_{\text{INP}}$  if ulowclken = 0. For more information, see the Device TRM.

### 5.9.4.3.2 DLL Characteristics

Table 5-26 summarizes the DLL characteristics and assumes testing over recommended operating conditions.

Table 5-26. DLL Characteristics

| NAME                | DESCRIPTION                                                              | MIN | TYP | MAX | UNIT   |
|---------------------|--------------------------------------------------------------------------|-----|-----|-----|--------|
| $f_{\text{input}}$  | Input clock frequency (EMIF_DLL_FCLK)                                    |     |     | 266 | MHz    |
| $t_{\text{lock}}$   | Lock time                                                                |     |     | 50k | cycles |
| $t_{\text{relock}}$ | Relock time (a change of the DLL frequency implies that DLL must relock) |     |     | 50k | cycles |

#### 5.9.4.3.2.1 DPLL and DLL Noise Isolation

##### NOTE

For more information on DPLL and DLL decoupling capacitor requirements, see the External Capacitors / Voltage Decoupling Capacitors / I/O and Analog Voltage Decoupling / VDDA Power Domain section.

### 5.9.5 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals must transition between  $V_{\text{IH}}$  and  $V_{\text{IL}}$  (or between  $V_{\text{IL}}$  and  $V_{\text{IH}}$ ) in a monotonic manner. Monotonic transitions are more easily ensured with faster switching signals. Slower input transitions are more susceptible to glitches due to noise and special care should be taken for slow input clocks.

### 5.9.6 Peripherals

#### 5.9.6.1 Timing Test Conditions

All timing requirements and switching characteristics are valid over the recommended operating conditions unless otherwise specified.

### 5.9.6.2 VIP

The device includes 1 Video Input Ports (VIP).

表 5-27, 图 5-19 and 图 5-20 present timings and switching characteristics of the VIPs.

**表 5-27. Timing Requirements for VIP <sup>(1)(2)</sup>**

| NO. | PARAMETER              | DESCRIPTION                                                                                                                                      | Mode             | MIN                   | MAX | UNIT |
|-----|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|------------------|-----------------------|-----|------|
| V1  | $t_{c(CLK)}$           | Cycle time, vinx_clki <sup>(3)(5)</sup>                                                                                                          |                  | 5.99 <sup>(1)</sup>   |     | ns   |
| V2  | $t_{w(CLKH)}$          | Pulse duration, vinx_clki high <sup>(3)(5)</sup>                                                                                                 |                  | 0.45×P <sup>(2)</sup> |     | ns   |
| V3  | $t_{w(CLKL)}$          | Pulse duration, vinx_clki low <sup>(3)(5)</sup>                                                                                                  |                  | 0.45×P <sup>(2)</sup> |     | ns   |
| V4  | $t_{su(CTL/DATA-CLK)}$ | Input setup time, Control (vinx_dei, vinx_vsynci, vinx_fldi, vinx_hsynci) and Data (vinx_dn) valid to vinx_clki transition <sup>(3)(4)(5)</sup>  | All other IOSETs | 2.52                  |     | ns   |
|     |                        |                                                                                                                                                  | VIN2 IOSET4      | 2.52                  |     | ns   |
|     |                        |                                                                                                                                                  | VIN2 IOSET5      | 3.7                   |     | ns   |
|     |                        |                                                                                                                                                  | VIN2 IOSET6      | 4.2                   |     | ns   |
| V5  | $t_{h(CLK-CTL/DATA)}$  | Input hold time, Control (vinx_dei, vinx_vsynci, vinx_fldi, vinx_hsynci) and Data (vinx_dn) valid from vinx_clki transition <sup>(3)(4)(5)</sup> | All other IOSETs | -0.05                 |     | ns   |
|     |                        |                                                                                                                                                  | VIN2 IOSET4      | 3                     |     | ns   |
|     |                        |                                                                                                                                                  | VIN2 IOSET5      | 1                     |     | ns   |
|     |                        |                                                                                                                                                  | VIN2 IOSET6      | 1                     |     | ns   |

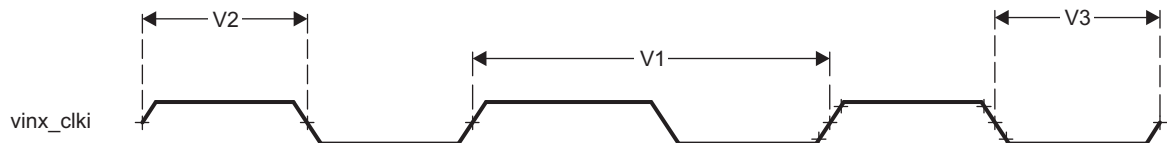
(1) For maximum frequency of 165 MHz.

(2) P = vinx\_clki period.

(3) x in vinx = 1a, 1b, 2a and 2b.

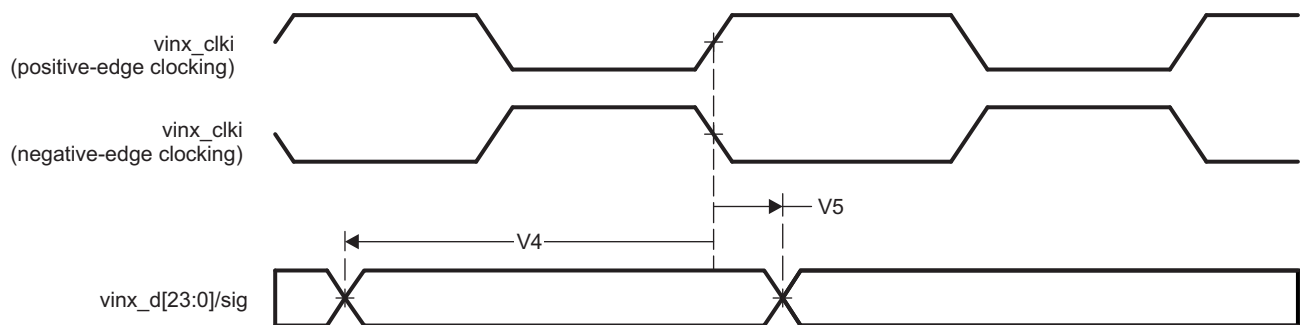
(4) n in dn = 0 to 7 when x = 1b, 2b;  
n = 0 to 23 when x = 1a and 2a;

(5) i in clki, dei, vsynci, hsynci and fldi = 0 or 1.



SPRS91v\_VIP\_01

**图 5-19. Video Input Ports Clock Signal**



SPRS8xx\_VIP\_02

**图 5-20. Video Input Ports Timings**

注意

The IO timings provided in this section are only valid for VIN1 and VIN2 if signals within a single IOSET are used. The IOSETs are defined in 表 5-28 and 表 5-29.

In 表 5-28 and 表 5-29 are presented the specific groupings of signals (IOSET) for use with vin1a, vin1b, vin2a and vin2b.

表 5-28. VIN1 IOSETs

| SIGNALS      | IOSET1 |     | IOSET2 |     | IOSET3 |     | IOSET4 |     |
|--------------|--------|-----|--------|-----|--------|-----|--------|-----|
|              | BALL   | MUX | BALL   | MUX | BALL   | MUX | BALL   | MUX |
| vin1a        |        |     |        |     |        |     |        |     |
| vin1a_clk0   | F22    | 0   | F22    | 0   | F22    | 0   | F22    | 0   |
| vin1a_de0    | F21    | 0   | F21    | 0   | F21    | 0   | F19    | 2   |
| vin1a_fid0   | F20    | 0   | F20    | 0   | F20    | 0   | F20    | 0   |
| vin1a_hsync0 | F19    | 0   | F19    | 0   | F19    | 0   | F19    | 0   |
| vin1a_vsync0 | G19    | 0   | G19    | 0   | G19    | 0   | G19    | 0   |
| vin1a_d0     | G18    | 0   | G18    | 0   | G18    | 0   | G18    | 0   |
| vin1a_d1     | G21    | 0   | G21    | 0   | G21    | 0   | G21    | 0   |
| vin1a_d2     | G22    | 0   | G22    | 0   | G22    | 0   | G22    | 0   |
| vin1a_d3     | H18    | 0   | H18    | 0   | H18    | 0   | H18    | 0   |
| vin1a_d4     | H20    | 0   | H20    | 0   | H20    | 0   | H20    | 0   |
| vin1a_d5     | H19    | 0   | H19    | 0   | H19    | 0   | H19    | 0   |
| vin1a_d6     | H22    | 0   | H22    | 0   | H22    | 0   | H22    | 0   |
| vin1a_d7     | H21    | 0   | H21    | 0   | H21    | 0   | H21    | 0   |
| vin1a_d8     | J17    | 0   |        |     | J17    | 0   |        |     |
| vin1a_d9     | K22    | 0   |        |     | K22    | 0   |        |     |
| vin1a_d10    | K21    | 0   |        |     | K21    | 0   |        |     |
| vin1a_d11    | K18    | 0   |        |     | K18    | 0   |        |     |
| vin1a_d12    | K17    | 0   |        |     | AB17   | 2   |        |     |
| vin1a_d13    | K19    | 0   |        |     | U17    | 2   |        |     |
| vin1a_d14    | K20    | 0   |        |     | W17    | 2   |        |     |
| vin1a_d15    | L21    | 0   |        |     | AA17   | 2   |        |     |
| vin1b        |        |     |        |     |        |     |        |     |
| vin1b_clk1   |        |     |        |     |        |     | F21    | 2   |
| vin1b_hsync1 |        |     |        |     |        |     | W7     | 7   |
| vin1b_vsync1 |        |     |        |     |        |     | W6     | 7   |
| vin1b_d0     |        |     |        |     |        |     | J17    | 2   |
| vin1b_d1     |        |     |        |     |        |     | K22    | 2   |
| vin1b_d2     |        |     |        |     |        |     | K21    | 2   |
| vin1b_d3     |        |     |        |     |        |     | K18    | 2   |
| vin1b_d4     |        |     |        |     |        |     | K17    | 2   |
| vin1b_d5     |        |     |        |     |        |     | K19    | 2   |
| vin1b_d6     |        |     |        |     |        |     | K20    | 2   |
| vin1b_d7     |        |     |        |     |        |     | L21    | 2   |
| vin1b_de1    |        |     |        |     |        |     | W7     | 8   |



**表 5-29. VIN2 IOSETs**

| SIGNALS      | IOSET1 |     | IOSET2 |     | IOSET3 |     | IOSET4 |     | IOSET5 |     | IOSET6 |     |
|--------------|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|
|              | BALL   | MUX | BALL   | MUX | BALL   | MUX | BALL   | MUX | BALL   | MUX | BALL   | MUX |
| <b>vin2a</b> |        |     |        |     |        |     |        |     |        |     |        |     |
| vin2a_clk0   | L22    | 0   | AB17   | 9   | L22    | 0   | L22    | 0   | L22    | 0   | W15    | 9   |
| vin2a_de0    | M17    | 0   | AA17   | 9   |        |     | AA15   | 9   | W7     | 1   | AA17   | 9   |
| vin2a_fld0   | M18    | 0   | U16    | 9   |        |     | AB15   | 9   | AB15   | 9   | U16    | 9   |
| vin2a_hsync0 |        |     | W7     | 2   | F14    | 9   | F15    | 9   | F15    | 9   | W7     | 2   |
| vin2a_vsync0 | W6     | 2   | W6     | 2   | C14    | 9   | F16    | 9   | F16    | 9   | W6     | 2   |
| vin2a_d0     | AA14   | 2   | AA14   | 2   | AA14   | 2   | AA14   | 2   | AA14   | 2   | AA14   | 2   |
| vin2a_d1     | AB14   | 2   | AB14   | 2   | AB14   | 2   | AB14   | 2   | AB14   | 2   | AB14   | 2   |
| vin2a_d2     | U13    | 2   | U13    | 2   | U13    | 2   | U13    | 2   | U13    | 2   | U13    | 2   |
| vin2a_d3     | V13    | 2   | V13    | 2   | V13    | 2   | V13    | 2   | V13    | 2   | V13    | 2   |
| vin2a_d4     | Y13    | 2   | Y13    | 2   | Y13    | 2   | Y13    | 2   | Y13    | 2   | Y13    | 2   |
| vin2a_d5     | W13    | 2   | W13    | 2   | W13    | 2   | W13    | 2   | W13    | 2   | W13    | 2   |
| vin2a_d6     | U11    | 2   | U11    | 2   | U11    | 2   | U11    | 2   | U11    | 2   | U11    | 2   |
| vin2a_d7     | V11    | 2   | V11    | 2   | V11    | 2   | V11    | 2   | V11    | 2   | V11    | 2   |
| vin2a_d8     |        |     | U9     | 2   |        |     |        |     |        |     | U9     | 2   |
| vin2a_d9     |        |     | W11    | 2   |        |     |        |     |        |     | W11    | 2   |
| vin2a_d10    |        |     | V9     | 2   |        |     |        |     |        |     | V9     | 2   |
| vin2a_d11    |        |     | W9     | 2   |        |     |        |     |        |     | W9     | 2   |
| vin2a_d12    |        |     | U8     | 2   |        |     |        |     |        |     | U8     | 2   |
| vin2a_d13    |        |     | W8     | 2   |        |     |        |     |        |     | W8     | 2   |
| vin2a_d14    |        |     | U7     | 2   |        |     |        |     |        |     | U7     | 2   |
| vin2a_d15    |        |     | V7     | 2   |        |     |        |     |        |     | V7     | 2   |
| <b>vin2b</b> |        |     |        |     |        |     |        |     |        |     |        |     |
| vin2b_clk1   |        |     |        |     | F20    | 2   |        |     |        |     |        |     |
| vin2b_hsync1 |        |     |        |     | M17    | 2   |        |     |        |     |        |     |
| vin2b_vsync1 |        |     |        |     | M18    | 2   |        |     |        |     |        |     |
| vin2b_d0     |        |     |        |     | U9     | 5   |        |     |        |     |        |     |
| vin2b_d1     |        |     |        |     | W11    | 5   |        |     |        |     |        |     |
| vin2b_d2     |        |     |        |     | V9     | 5   |        |     |        |     |        |     |
| vin2b_d3     |        |     |        |     | W9     | 5   |        |     |        |     |        |     |
| vin2b_d4     |        |     |        |     | U8     | 5   |        |     |        |     |        |     |
| vin2b_d5     |        |     |        |     | W8     | 5   |        |     |        |     |        |     |

**表 5-29. VIN2 IOSETs (continued)**

| SIGNALS  | IOSET1 |     | IOSET2 |     | IOSET3 |     | IOSET4 |     | IOSET5 |     | IOSET6 |     |
|----------|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|
|          | BALL   | MUX | BALL   | MUX | BALL   | MUX | BALL   | MUX | BALL   | MUX | BALL   | MUX |
| vin2b_d6 |        |     |        |     | U7     | 5   |        |     |        |     |        |     |
| vin2b_d7 |        |     |        |     | V7     | 5   |        |     |        |     |        |     |

### 5.9.6.3 DSS

Display Parallel Interfaces (DPI) channels are available in DSS named DPI Video Output 1.

Every VOUT interface consists of:

- 24-bit data bus (data[23:0])
- Horizontal synchronization signal (HSYNC)
- Vertical synchronization signal (VSYNC)
- Data enable (DE)
- Field ID (FID)
- Pixel clock (CLK)

#### 注

For more information, see the Display Subsystem section of the Device TRM.

#### 注意

All pads/balls configured as vout\*\_ signals must be programmed to use slow slew rate by setting the corresponding CTRL\_CORE\_PAD\_\*[SLEWCONTROL] register field to SLOW (0b1).

表 5-30 and 図 5-21 assume testing over the recommended operating conditions and electrical characteristic conditions.

表 5-30. DPI Video Output 1 Switching Characteristics<sup>(1)(2)</sup>

| NO. | PARAMETER                | DESCRIPTION                                                                                                                           | MODE | MIN     | MAX  | UNIT |
|-----|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------|------|---------|------|------|
| D1  | $t_{c(\text{clk})}$      | Cycle time, output pixel clock vouti_clk                                                                                              |      | 6.73    |      | ns   |
| D2  | $t_{w(\text{clkL})}$     | Pulse duration, output pixel clock vouti_clk low                                                                                      |      | P×0.5-1 |      | ns   |
| D3  | $t_{w(\text{clkH})}$     | Pulse duration, output pixel clock vouti_clk high                                                                                     |      | P×0.5-1 |      | ns   |
| D5  | $t_{d(\text{clk-ctlV})}$ | Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid                                                | DPI1 | -1.33   | 1.01 | ns   |
| D6  | $t_{d(\text{clk-dV})}$   | Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fid valid | DPI1 | -1.33   | 1.01 | ns   |

- (1) P = output vout1\_clk period in ns.
- (2) All pads/balls configured as vout1\_\* signals must be programmed to use slow slew rate by setting the corresponding CTRL\_CORE\_PAD\_\*[SLEWCONTROL] register field to SLOW (0b1).
- (3) SERDES transceivers may be sensitive to the jitter profile of vout1\_clk. See Application Note [SPRAC62](#) for additional guidance.

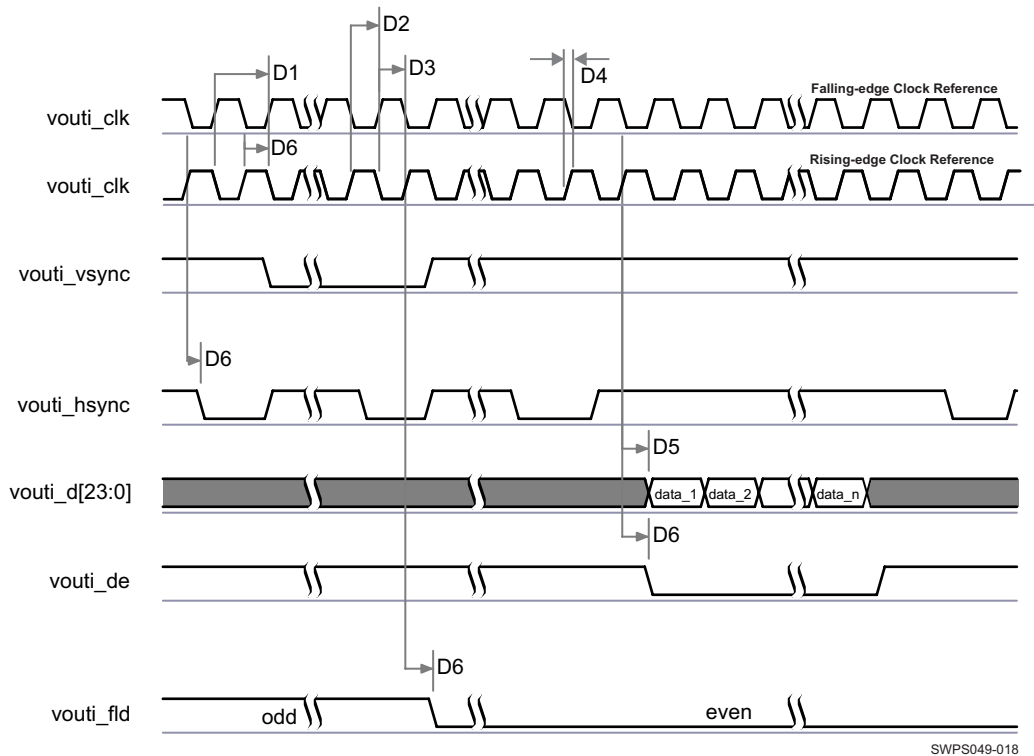


图 5-21. DPI Video Output<sup>(1)(2)(3)</sup>

- (1) The configuration of assertion of the data can be programmed on the falling or rising edge of the pixel clock.
- (2) The polarity and the pulse width of vout1\_hsync and vout1\_vsync are programmable, refer to the DSS section of the device TRM.
- (3) The vout1\_clk frequency can be configured, refer to the DSS section of the device TRM.

#### 5.9.6.4 EMIF

The device has a dedicated interface to DDR3 and DDR3L SDRAM. It supports JEDEC standard compliant DDR3 and DDR3L SDRAM devices with the following features:

- 16-bit or 32-bit data path to external SDRAM memory
- Memory device capacity: 128Mb, 256Mb, 512Mb, 1Gb, 2Gb, 4Gb and 8Gb devices (Single die only)
- One interface with associated DDR3/DDR3L PHYs

#### 注

For more information, see the EMIF Controller section of the Device TRM.

#### 5.9.6.5 GPMC

The GPMC is the unified memory controller that interfaces external memory devices such as:

- Asynchronous SRAM-like memories and ASIC devices
- Asynchronous page mode and synchronous burst NOR flash
- NAND flash

注

For more information, see the General-Purpose Memory Controller section of the Device TRM.

### 5.9.6.5.1 GPMC/NOR Flash Interface Synchronous Timing

表 5-31 和 表 5-32, 表 5-33 和 表 5-34 assume testing over the recommended operating conditions and electrical characteristic conditions below (see 图 5-22, 图 5-23, 图 5-24, 图 5-25, 图 5-26 and 图 5-27).

**表 5-31. GPMC/NOR Flash Interface Timing Requirements - Synchronous Mode - 1 Load**

| NO. | PARAMETER            | DESCRIPTION                                               | MIN | MAX | UNIT |
|-----|----------------------|-----------------------------------------------------------|-----|-----|------|
| F12 | $t_{su}(dV-clkH)$    | Setup time, read gpmc_ad[15:0] valid before gpmc_clk high | 1.9 |     | ns   |
| F13 | $t_h(clkH-dV)$       | Hold time, read gpmc_ad[15:0] valid after gpmc_clk high   | 1   |     | ns   |
| F21 | $t_{su}(waitV-clkH)$ | Setup time, gpmc_wait[1:0] valid before gpmc_clk high     | 1.9 |     | ns   |
| F22 | $t_h(clkH-waitV)$    | Hold Time, gpmc_wait[1:0] valid after gpmc_clk high       | 1   |     | ns   |

注

Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see the Device TRM.

**表 5-32. GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - 1 Load**

| NO. | PARAMETER          | DESCRIPTION                                                                    | MIN   | MAX    | UNIT |
|-----|--------------------|--------------------------------------------------------------------------------|-------|--------|------|
| F0  | $t_c(clk)$         | Cycle time, output clock gpmc_clk period <sup>(12)</sup>                       | 11.3  |        | ns   |
| F2  | $t_d(clkH-nCSV)$   | Delay time, gpmc_clk rising edge to gpmc_cs[7:0] transition <sup>(14)</sup>    | F-0.8 | F+3.1  | ns   |
| F3  | $t_d(clkH-nCSIV)$  | Delay time, gpmc_clk rising edge to gpmc_cs[7:0] invalid <sup>(14)</sup>       | E-0.8 | E+3.1  | ns   |
| F4  | $t_d(ADDV-clk)$    | Delay time, gpmc_a[27:0] address bus valid to gpmc_clk first edge              | B-0.8 | B+3.1  | ns   |
| F5  | $t_d(clkH-ADDIV)$  | Delay time, gpmc_clk rising edge to gpmc_a[27:0] gpmc address bus invalid      | -0.8  |        | ns   |
| F6  | $t_d(nBEV-clk)$    | Delay time, gpmc_ben[1:0] valid to gpmc_clk rising edge                        | B-3.8 | B+1.1  | ns   |
| F7  | $t_d(clkH-nBEIV)$  | Delay time, gpmc_clk rising edge to gpmc_ben[1:0] invalid                      | D-0.4 | D+1.1  | ns   |
| F8  | $t_d(clkH-nADV)$   | Delay time, gpmc_clk rising edge to gpmc_advn_ale transition <sup>(14)</sup>   | G-0.8 | G+3.1  | ns   |
| F9  | $t_d(clkH-nADVIV)$ | Delay time, gpmc_clk rising edge to gpmc_advn_ale invalid <sup>(14)</sup>      | D-0.8 | D+3.1  | ns   |
| F10 | $t_d(clkH-nOE)$    | Delay time, gpmc_clk rising edge to gpmc_oen_ren transition <sup>(14)</sup>    | H-0.8 | H+2.1  | ns   |
| F11 | $t_d(clkH-nOEIV)$  | Delay time, gpmc_clk rising edge to gpmc_oen_ren invalid <sup>(14)</sup>       | E-0.8 | E+2.1  | ns   |
| F14 | $t_d(clkH-nWE)$    | Delay time, gpmc_clk rising edge to gpmc_wen transition <sup>(14)</sup>        | I-0.8 | I+3.1  | ns   |
| F15 | $t_d(clkH-Data)$   | Delay time, gpmc_clk rising edge to gpmc_ad[15:0] data bus transition          | J-1.1 | J+3.92 | ns   |
| F17 | $t_d(clkH-nBE)$    | Delay time, gpmc_clk rising edge to gpmc_ben[1:0] transition                   | J-1.1 | J+3.8  | ns   |
| F18 | $t_w(nCSV)$        | Pulse duration, gpmc_cs[7:0] low                                               | A     |        | ns   |
| F19 | $t_w(nBEV)$        | Pulse duration, gpmc_ben[1:0] low                                              | C     |        | ns   |
| F20 | $t_w(nADV)$        | Pulse duration, gpmc_advn_ale low                                              | K     |        | ns   |
| F23 | $t_d(CLK-GPIO)$    | Delay time, gpmc_clk transition to gpio6_16.clkout0 transition <sup>(13)</sup> | 1.2   | 6.1    | ns   |

**表 5-33. GPMC/NOR Flash Interface Timing Requirements - Synchronous Mode - 5 Loads**

| NO. | PARAMETER            | DESCRIPTION                                               | MIN | MAX | UNIT |
|-----|----------------------|-----------------------------------------------------------|-----|-----|------|
| F12 | $t_{su}(dV-clkH)$    | Setup time, read gpmc_ad[15:0] valid before gpmc_clk high | 2.5 |     | ns   |
| F13 | $t_h(clkH-dV)$       | Hold time, read gpmc_ad[15:0] valid after gpmc_clk high   | 1.9 |     | ns   |
| F21 | $t_{su}(waitV-clkH)$ | Setup time, gpmc_wait[1:0] valid before gpmc_clk high     | 2.5 |     | ns   |

**表 5-33. GPMC/NOR Flash Interface Timing Requirements - Synchronous Mode - 5 Loads (continued)**

| NO. | PARAMETER                  | DESCRIPTION                                         | MIN | MAX | UNIT |
|-----|----------------------------|-----------------------------------------------------|-----|-----|------|
| F22 | $t_{h(\text{clkH-waitV})}$ | Hold Time, gpmc_wait[1:0] valid after gpmc_clk high | 1.9 |     | ns   |

**表 5-34. GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - 5 Loads**

| NO. | PARAMETER                   | DESCRIPTION                                                                    | MIN        | MAX        | UNIT |
|-----|-----------------------------|--------------------------------------------------------------------------------|------------|------------|------|
| F0  | $t_{c(\text{clk})}$         | Cycle time, output clock gpmc_clk period <sup>(12)</sup>                       | 15.04      |            | ns   |
| F2  | $t_{d(\text{clkH-nCSV})}$   | Delay time, gpmc_clk rising edge to gpmc_cs[7:0] transition <sup>(14)</sup>    | F+0.7 (6)  | F+6.1 (6)  | ns   |
| F3  | $t_{d(\text{clkH-nCSIV})}$  | Delay time, gpmc_clk rising edge to gpmc_cs[7:0] invalid <sup>(14)</sup>       | E+0.7 (5)  | E+6.1 (5)  | ns   |
| F4  | $t_{d(\text{ADDV-clk})}$    | Delay time, gpmc_a[27:0] address bus valid to gpmc_clk first edge              | B+0.7 (2)  | B+6.1 (2)  | ns   |
| F5  | $t_{d(\text{clkH-ADDIV})}$  | Delay time, gpmc_clk rising edge to gpmc_a[27:0] gpmc address bus invalid      | 0.7        |            | ns   |
| F6  | $t_{d(\text{nBEV-clk})}$    | Delay time, gpmc_ben[1:0] valid to gpmc_clk rising edge                        | B-4.9      | B+0.4      | ns   |
| F7  | $t_{d(\text{clkH-nBEIV})}$  | Delay time, gpmc_clk rising edge to gpmc_ben[1:0] invalid                      | D-0.4      | D+4.9      | ns   |
| F8  | $t_{d(\text{clkH-nADV})}$   | Delay time, gpmc_clk rising edge to gpmc_adv_nale transition <sup>(14)</sup>   | G+0.7 (7)  | G+6.1 (7)  | ns   |
| F9  | $t_{d(\text{clkH-nADVIV})}$ | Delay time, gpmc_clk rising edge to gpmc_adv_nale invalid <sup>(14)</sup>      | D+0.7 (4)  | D+6.1 (4)  | ns   |
| F10 | $t_{d(\text{clkH-nOE})}$    | Delay time, gpmc_clk rising edge to gpmc_oen_ren transition <sup>(14)</sup>    | H+0.7 (8)  | H+5.1 (8)  | ns   |
| F11 | $t_{d(\text{clkH-nOEIV})}$  | Delay time, gpmc_clk rising edge to gpmc_oen_ren invalid <sup>(14)</sup>       | E+0.7 (5)  | E+5.1 (5)  | ns   |
| F14 | $t_{d(\text{clkH-nWE})}$    | Delay time, gpmc_clk rising edge to gpmc_wen transition <sup>(14)</sup>        | I+0.7 (9)  | I+6.1 (9)  | ns   |
| F15 | $t_{d(\text{clkH-Data})}$   | Delay time, gpmc_clk rising edge to gpmc_ad[15:0] data bus transition          | J-0.4 (10) | J+4.9 (10) | ns   |
| F17 | $t_{d(\text{clkH-nBE})}$    | Delay time, gpmc_clk rising edge to gpmc_ben[1:0] transition                   | J-0.4 (10) | J+4.9 (10) | ns   |
| F18 | $t_{w(\text{nCSV})}$        | Pulse duration, gpmc_cs[7:0] low                                               | A (1)      |            | ns   |
| F19 | $t_{w(\text{nBEV})}$        | Pulse duration, gpmc_ben[1:0] low                                              | C (3)      |            | ns   |
| F20 | $t_{w(\text{nADV})}$        | Pulse duration, gpmc_adv_nale low                                              | K (11)     |            | ns   |
| F23 | $t_{d(\text{CLK-GPIO})}$    | Delay time, gpmc_clk transition to gpio6_16.clkout0 transition <sup>(13)</sup> | 1.2        | 6.1        | ns   |

- (1) For single read:  $A = (\text{CSRdOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK period}$   
For burst read:  $A = (\text{CSRdOffTime} - \text{CSOnTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK period}$   
For burst write:  $A = (\text{CSWrOffTime} - \text{CSOnTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK period}$   
with n the page burst access number.
- (2)  $B = \text{ClkActivationTime} \times \text{GPMC\_FCLK}$
- (3) For single read:  $C = \text{RdCycleTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$   
For burst read:  $C = (\text{RdCycleTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$   
For Burst write:  $C = (\text{WrCycleTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$  with n the page burst access number.
- (4) For single read:  $D = (\text{RdCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$   
For burst read:  $D = (\text{RdCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$   
For burst write:  $D = (\text{WrCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$
- (5) For single read:  $E = (\text{CSRdOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$   
For burst read:  $E = (\text{CSRdOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$   
For burst write:  $E = (\text{CSWrOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$
- (6) For nCS falling edge (CS activated):  
Case GpmcFCLKDivider = 0 :  
 $F = 0.5 \times \text{CSExtraDelay} \times \text{GPMC\_FCLK}$   
Case GpmcFCLKDivider = 1:  
 $F = 0.5 \times \text{CSExtraDelay} \times \text{GPMC\_FCLK}$  if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)  
 $F = (1 + 0.5 \times \text{CSExtraDelay}) \times \text{GPMC\_FCLK}$  otherwise  
Case GpmcFCLKDivider = 2:  
 $F = 0.5 \times \text{CSExtraDelay} \times \text{GPMC\_FCLK}$  if ((CSOnTime - ClkActivationTime) is a multiple of 3)  
 $F = (1 + 0.5 \times \text{CSExtraDelay}) \times \text{GPMC\_FCLK}$  if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)  
 $F = (2 + 0.5 \times \text{CSExtraDelay}) \times \text{GPMC\_FCLK}$  if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)  
Case GpmcFCLKDivider = 3:  
 $F = 0.5 \times \text{CSExtraDelay} \times \text{GPMC\_FCLK}$  if ((CSOnTime - ClkActivationTime) is a multiple of 4)  
 $F = (1 + 0.5 \times \text{CSExtraDelay}) \times \text{GPMC\_FCLK}$  if ((CSOnTime - ClkActivationTime - 1) is a multiple of 4)  
 $F = (2 + 0.5 \times \text{CSExtraDelay}) \times \text{GPMC\_FCLK}$  if ((CSOnTime - ClkActivationTime - 2) is a multiple of 4)

$F = (3 + 0.5 \times \text{CSEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{CSOnTime} - \text{ClkActivationTime} - 3)$  is a multiple of 4)

(7) For ADV falling edge (ADV activated):

Case GpmcFCLKDivider = 0 :

$G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}$

Case GpmcFCLKDivider = 1:

$G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}$  if  $(\text{ClkActivationTime}$  and  $\text{ADVOnTime}$  are odd) or  $(\text{ClkActivationTime}$  and  $\text{ADVOnTime}$  are even)

$G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}$  otherwise

Case GpmcFCLKDivider = 2:

$G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}$  if  $((\text{ADVOnTime} - \text{ClkActivationTime})$  is a multiple of 3)

$G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{ADVOnTime} - \text{ClkActivationTime} - 1)$  is a multiple of 3)

$G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{ADVOnTime} - \text{ClkActivationTime} - 2)$  is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:

Case GpmcFCLKDivider = 0:

$G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}$

Case GpmcFCLKDivider = 1:

$G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}$  if  $(\text{ClkActivationTime}$  and  $\text{ADVRdOffTime}$  are odd) or  $(\text{ClkActivationTime}$  and  $\text{ADVRdOffTime}$  are even)

$G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}$  otherwise

Case GpmcFCLKDivider = 2:

$G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}$  if  $((\text{ADVRdOffTime} - \text{ClkActivationTime})$  is a multiple of 3)

$G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{ADVRdOffTime} - \text{ClkActivationTime} - 1)$  is a multiple of 3)

$G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{ADVRdOffTime} - \text{ClkActivationTime} - 2)$  is a multiple of 3)

Case GpmcFCLKDivider = 3:

$G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}$  if  $((\text{ADVRdOffTime} - \text{ClkActivationTime})$  is a multiple of 4)

$G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{ADVRdOffTime} - \text{ClkActivationTime} - 1)$  is a multiple of 4)

$G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{ADVRdOffTime} - \text{ClkActivationTime} - 2)$  is a multiple of 4)

$G = (3 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{ADVRdOffTime} - \text{ClkActivationTime} - 3)$  is a multiple of 4)

For ADV rising edge (ADV deactivated) in Writing mode:

Case GpmcFCLKDivider = 0:

$G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}$

Case GpmcFCLKDivider = 1:

$G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}$  if  $(\text{ClkActivationTime}$  and  $\text{ADVWrOffTime}$  are odd) or  $(\text{ClkActivationTime}$  and  $\text{ADVWrOffTime}$  are even)

$G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}$  otherwise

Case GpmcFCLKDivider = 2:

$G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}$  if  $((\text{ADVWrOffTime} - \text{ClkActivationTime})$  is a multiple of 3)

$G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{ADVWrOffTime} - \text{ClkActivationTime} - 1)$  is a multiple of 3)

$G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{ADVWrOffTime} - \text{ClkActivationTime} - 2)$  is a multiple of 3)

Case GpmcFCLKDivider = 3:

$G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}$  if  $((\text{ADVWrOffTime} - \text{ClkActivationTime})$  is a multiple of 4)

$G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{ADVWrOffTime} - \text{ClkActivationTime} - 1)$  is a multiple of 4)

$G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{ADVWrOffTime} - \text{ClkActivationTime} - 2)$  is a multiple of 4)

$G = (3 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{ADVWrOffTime} - \text{ClkActivationTime} - 3)$  is a multiple of 4)

(8) For OE falling edge (OE activated):

Case GpmcFCLKDivider = 0:

$H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}$

Case GpmcFCLKDivider = 1:

$H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}$  if  $(\text{ClkActivationTime}$  and  $\text{OEOnTime}$  are odd) or  $(\text{ClkActivationTime}$  and  $\text{OEOnTime}$  are even)

$H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}$  otherwise

Case GpmcFCLKDivider = 2:

$H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}$  if  $((\text{OEOnTime} - \text{ClkActivationTime})$  is a multiple of 3)

$H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{OEOnTime} - \text{ClkActivationTime} - 1)$  is a multiple of 3)

$H = (2 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{OEOnTime} - \text{ClkActivationTime} - 2)$  is a multiple of 3)

Case GpmcFCLKDivider = 3:

$H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}$  if  $((\text{OEOnTime} - \text{ClkActivationTime})$  is a multiple of 4)

$H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{OEOnTime} - \text{ClkActivationTime} - 1)$  is a multiple of 4)

$H = (2 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{OEOnTime} - \text{ClkActivationTime} - 2)$  is a multiple of 4)

$H = (3 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{OEOnTime} - \text{ClkActivationTime} - 3)$  is a multiple of 4)

For OE rising edge (OE deactivated):

Case GpmcFCLKDivider = 0:

$H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}$

Case GpmcFCLKDivider = 1:

$H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}$  if  $(\text{ClkActivationTime}$  and  $\text{OEOffTime}$  are odd) or  $(\text{ClkActivationTime}$  and  $\text{OEOffTime}$  are even)

$H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}$  otherwise

Case GpmcFCLKDivider = 2:

$H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}$  if  $((\text{OEOffTime} - \text{ClkActivationTime})$  is a multiple of 3)

$H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{OEOffTime} - \text{ClkActivationTime} - 1)$  is a multiple of 3)

$H = (2 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{OEOffTime} - \text{ClkActivationTime} - 2)$  is a multiple of 3)

Case GpmcFCLKDivider = 3:

- $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}$  if  $((\text{OEOffTime} - \text{ClkActivationTime})$  is a multiple of 4)
- $H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{OEOffTime} - \text{ClkActivationTime} - 1)$  is a multiple of 4)
- $H = (2 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{OEOffTime} - \text{ClkActivationTime} - 2)$  is a multiple of 4)
- $H = (3 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{OEOffTime} - \text{ClkActivationTime} - 3)$  is a multiple of 4)

(9) For WE falling edge (WE activated):

Case GpmcFCLKDivider = 0:

-  $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}$

Case GpmcFCLKDivider = 1:

-  $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}$  if  $(\text{ClkActivationTime}$  and  $\text{WEOnTime}$  are odd) or  $(\text{ClkActivationTime}$  and  $\text{WEOnTime}$  are even)

-  $I = (1 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}$  otherwise

Case GpmcFCLKDivider = 2:

-  $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}$  if  $((\text{WEOnTime} - \text{ClkActivationTime})$  is a multiple of 3)

-  $I = (1 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{WEOnTime} - \text{ClkActivationTime} - 1)$  is a multiple of 3)

-  $I = (2 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{WEOnTime} - \text{ClkActivationTime} - 2)$  is a multiple of 3)

Case GpmcFCLKDivider = 3:

-  $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}$  if  $((\text{WEOnTime} - \text{ClkActivationTime})$  is a multiple of 4)

-  $I = (1 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{WEOnTime} - \text{ClkActivationTime} - 1)$  is a multiple of 4)

-  $I = (2 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{WEOnTime} - \text{ClkActivationTime} - 2)$  is a multiple of 4)

-  $I = (3 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{WEOnTime} - \text{ClkActivationTime} - 3)$  is a multiple of 4)

For WE rising edge (WE deactivated):

Case GpmcFCLKDivider = 0:

-  $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}$

Case GpmcFCLKDivider = 1:

-  $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}$  if  $(\text{ClkActivationTime}$  and  $\text{WEOffTime}$  are odd) or  $(\text{ClkActivationTime}$  and  $\text{WEOffTime}$  are even)

-  $I = (1 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}$  otherwise

Case GpmcFCLKDivider = 2:

-  $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}$  if  $((\text{WEOffTime} - \text{ClkActivationTime})$  is a multiple of 3)

-  $I = (1 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{WEOffTime} - \text{ClkActivationTime} - 1)$  is a multiple of 3)

-  $I = (2 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{WEOffTime} - \text{ClkActivationTime} - 2)$  is a multiple of 3)

Case GpmcFCLKDivider = 3:

-  $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}$  if  $((\text{WEOffTime} - \text{ClkActivationTime})$  is a multiple of 4)

-  $I = (1 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{WEOffTime} - \text{ClkActivationTime} - 1)$  is a multiple of 4)

-  $I = (2 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{WEOffTime} - \text{ClkActivationTime} - 2)$  is a multiple of 4)

-  $I = (3 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}$  if  $((\text{WEOffTime} - \text{ClkActivationTime} - 3)$  is a multiple of 4)

(10)  $J = \text{GPMC\_FCLK}$  period, where  $\text{GPMC\_FCLK}$  is the General Purpose Memory Controller internal functional clock

(11) For read:

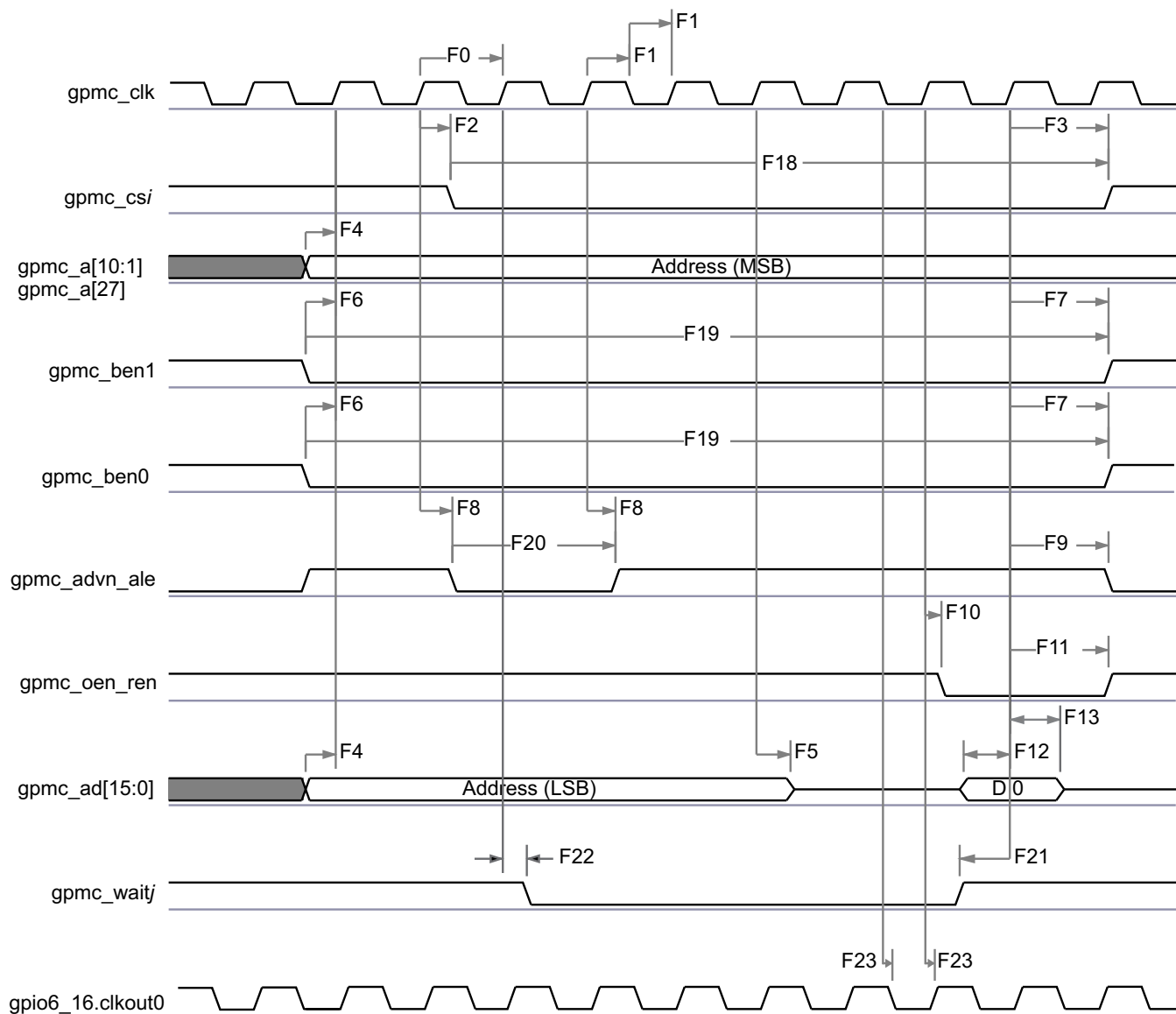
$K = (\text{ADVRdOffTime} - \text{ADVOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$

For write:  $K = (\text{ADVWrOffTime} - \text{ADVOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$

(12) The gpmc\_clk output clock maximum and minimum frequency is programmable in the I/F module by setting the  $\text{GPMC\_CONFIG1\_CSx}$  configuration register bit fields GpmcFCLKDivider

(13) gpio6\_16 programmed to  $\text{MUXMODE}=9$  (clkout1),  $\text{CM\_CLKSEL\_CLKOUTMUX1}$  programmed to 7 ( $\text{CORE\_DPLL\_OUT\_DCLK}$ ),  $\text{CM\_CLKSEL\_CORE\_DPLL\_OUT\_CLK\_CLKOUTMUX}$  programmed to 1.

(14)  $\text{CSEXTRADELAY} = 0$ ,  $\text{ADVEXTRADELAY} = 0$ ,  $\text{WEEXTRADELAY} = 0$ ,  $\text{OEEXTRADELAY} = 0$ . Extra half-GPMC\_FCLK cycle delay mode is not timed.

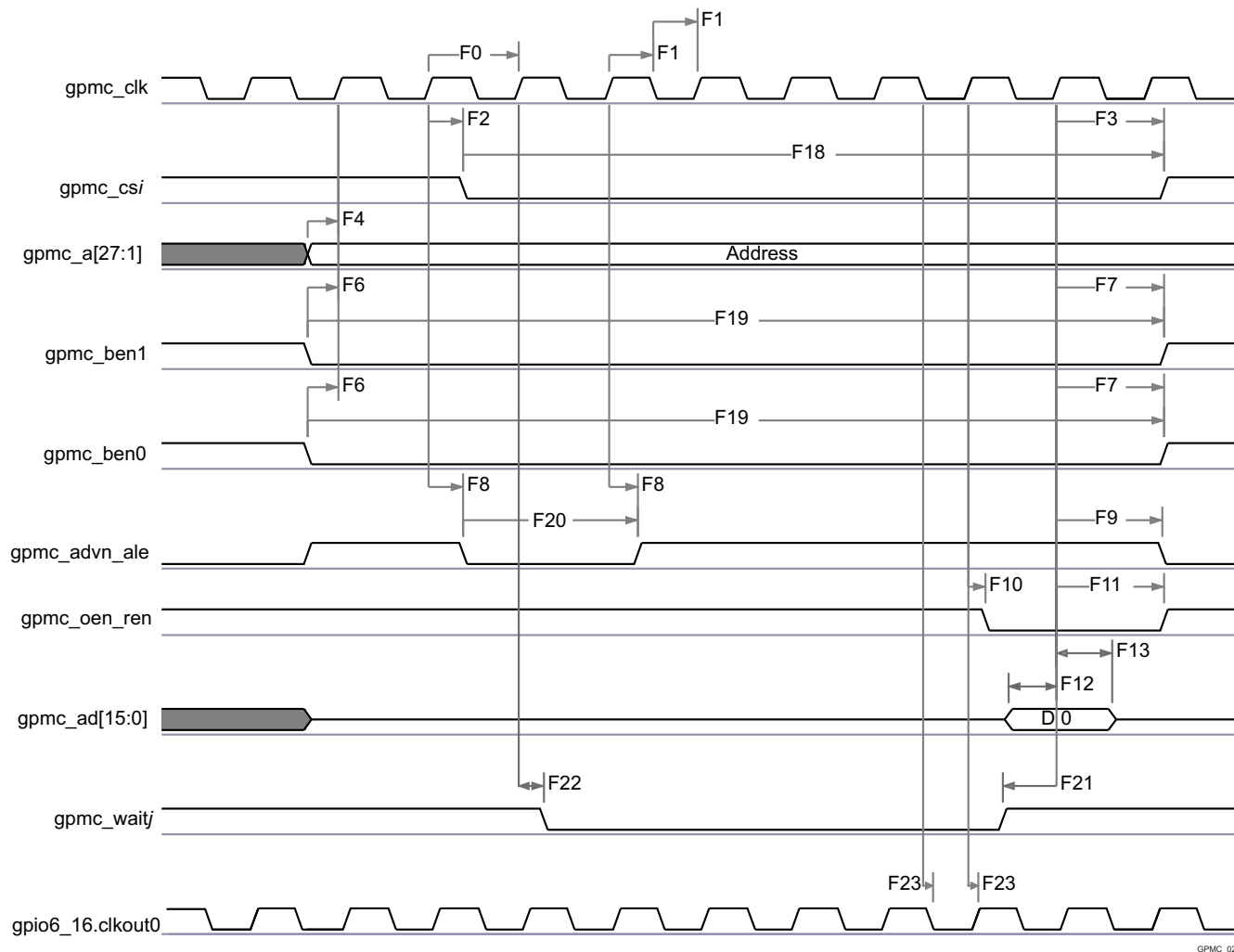


GPMC\_01

5-22. GPMC / Multiplexed 16bits NOR Flash - Synchronous Single Read -  
(GpmcFCLKDivider = 0)<sup>(1)(2)</sup>

(1) In gpmc\_csi, i = 0 to 7.

(2) In gpmc\_waitj, j = 0 to 1.

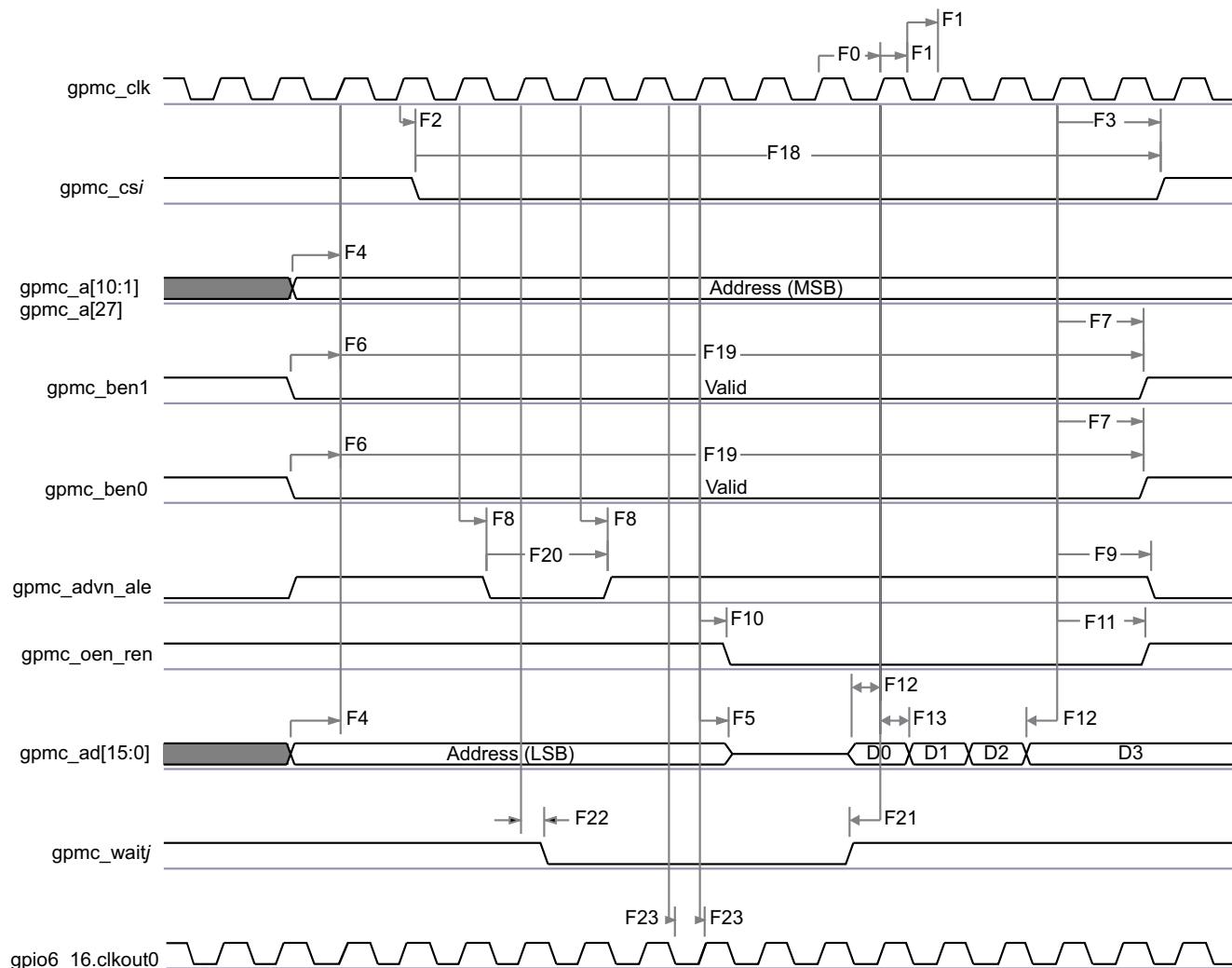


GPMC\_02

图 5-23. GPMC / Non-Multiplexed 16bits NOR Flash - Synchronous Single Read -  
(GpmcFCLKDivider = 0)<sup>(1)(2)</sup>

(1) In gpmc\_csi, i = 0 to 7.

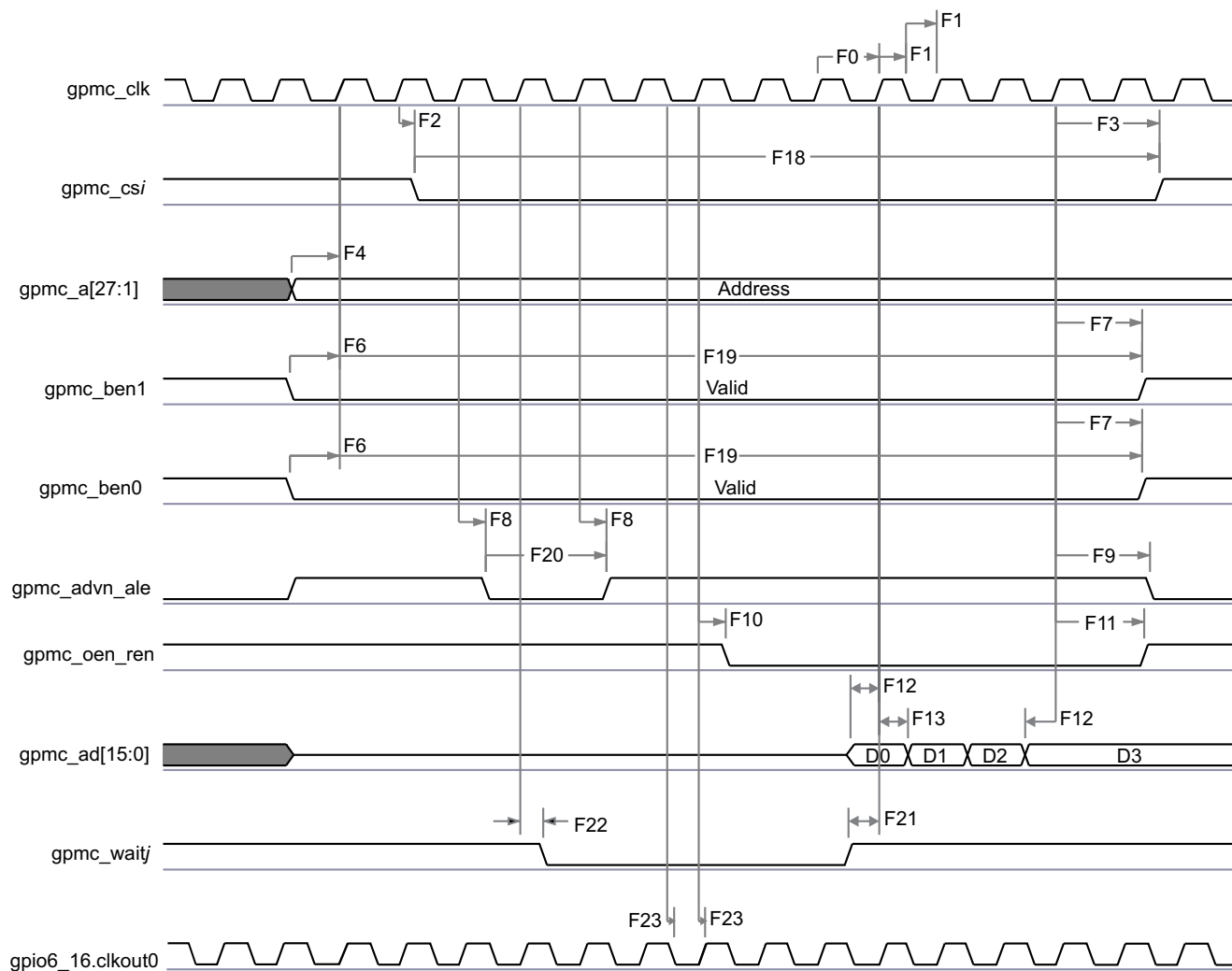
(2) In gpmc\_waitj, j = 0 to 1.



GPMC\_03

**5-24. GPMC / Multiplexed 16bits NOR Flash - Synchronous Burst Read 4x16 bits - (GpmcFCLKDivider = 0)<sup>(1)(2)</sup>**

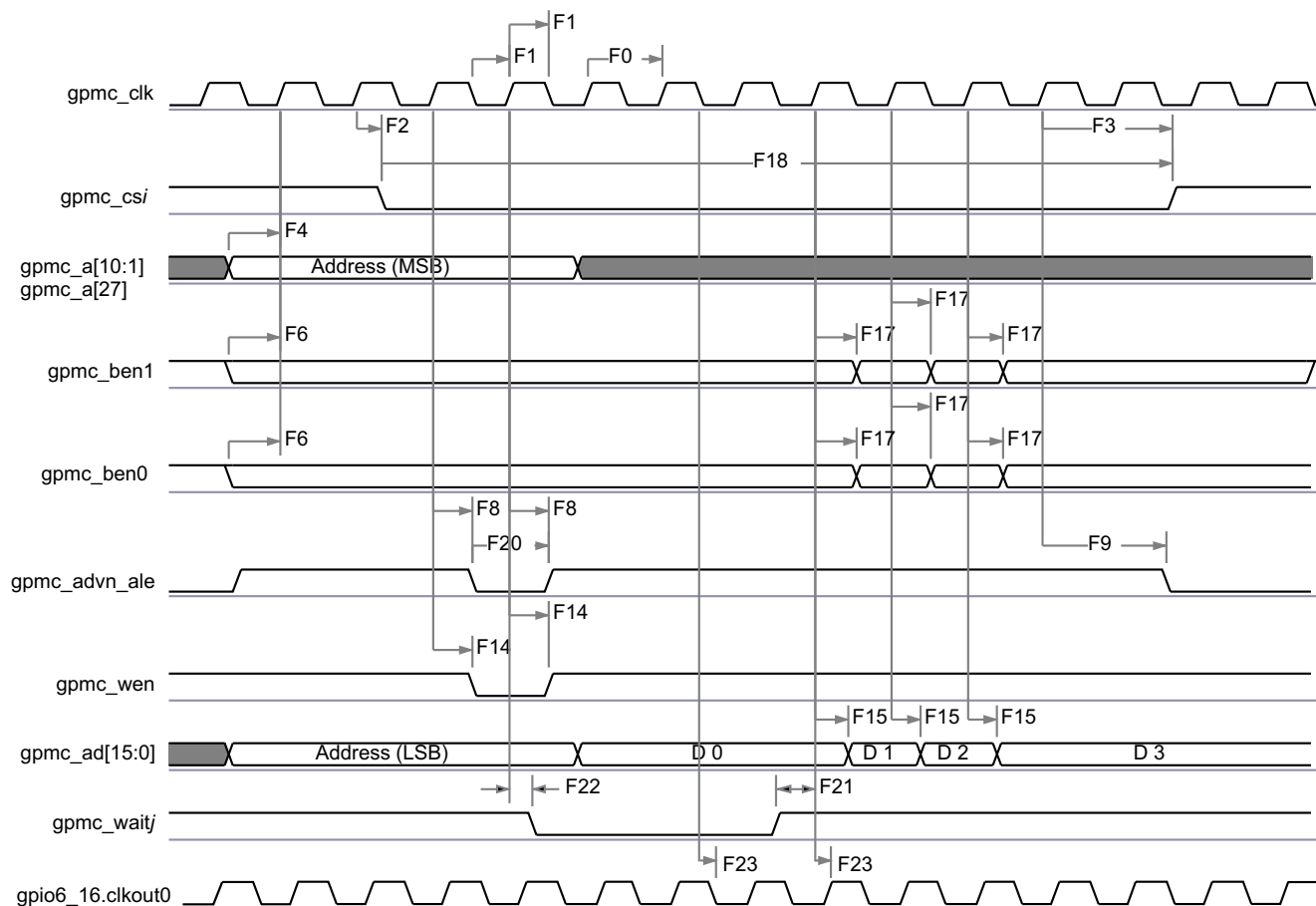
- (1) In gpmc\_csi, i= 0 to 7.  
(2) In gpmc\_waitj, j = 0 to 1.



GPMC\_04

图 5-25. GPMC / Non-Multiplexed 16bits NOR Flash - Synchronous Burst Read 4x16 bits -  
(GpmcFCLKDivider = 0)<sup>(1)(2)</sup>

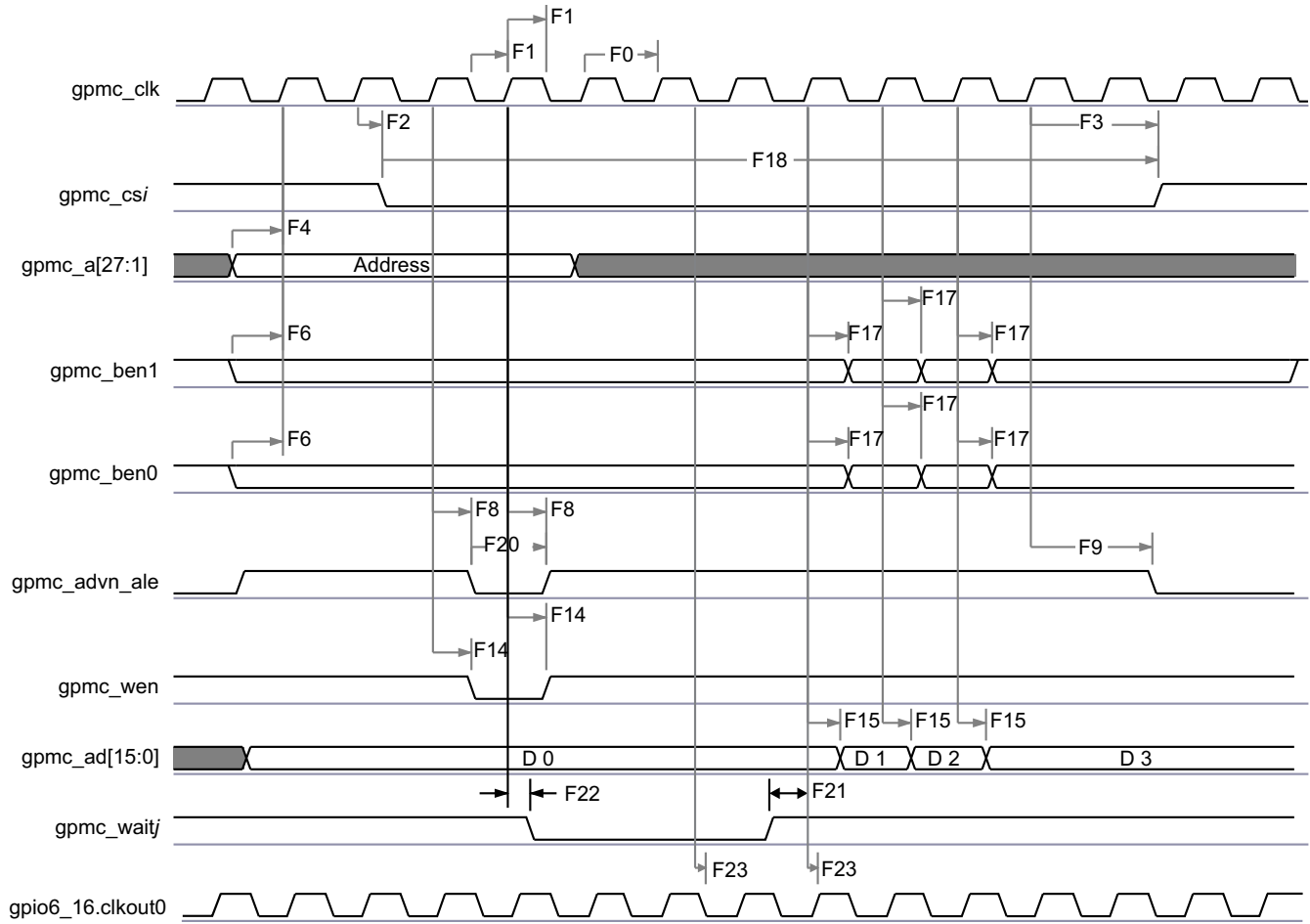
- (1) In gpmc\_csi, i = 0 to 7.  
(2) In gpmc\_waitj, j = 0 to 1.



GPMC\_05

图 5-26. GPMC / Multiplexed 16bits NOR Flash - Synchronous Burst Write 4x16bits -  
(GpmcFCLKDivider = 0)<sup>(1)(2)</sup>

- (1) In “gpmc\_csi”, i = 0 to 7.  
(2) In “gpmc\_waitj”, j = 0 to 1.



GPMC\_06

**图 5-27. GPMC / Non-Multiplexed 16bits NOR Flash - Synchronous Burst Write 4x16bits - (GpmcFCLKDivider = 0)<sup>(1)(2)</sup>**

(1) In “gpmc\_csi”, i = 1 to 7.

(2) In “gpmc\_waitj”, j = 0 to 1.

#### 5.9.6.5.2 GPMC/NOR Flash Interface Asynchronous Timing

表 5-35 和 表 5-36 assume testing over the recommended operating conditions and electrical characteristic conditions below (see 图 5-28, 图 5-29, 图 5-30, 图 5-31, 图 5-32 and 图 5-33).

**表 5-35. GPMC/NOR Flash Interface Timing Requirements - Asynchronous Mode**

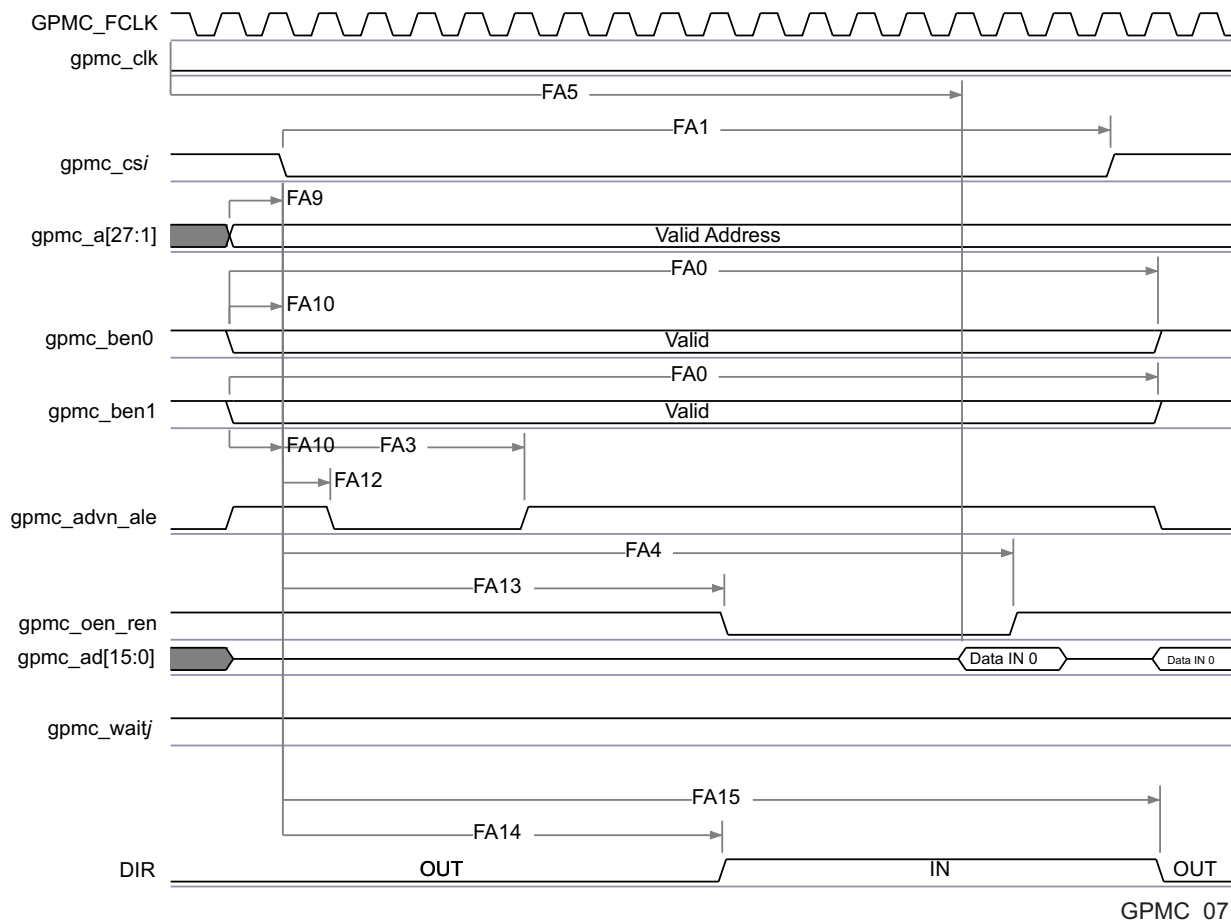
| NO.  | PARAMETER              | DESCRIPTION                                                      | MIN | MAX              | UNIT   |
|------|------------------------|------------------------------------------------------------------|-----|------------------|--------|
| FA5  | $t_{acc(DAT)}$         | Data Maximum Access Time (GPMC_FCLK cycles)                      |     | H <sup>(1)</sup> | cycles |
| FA20 | $t_{acc1-pgmode(DAT)}$ | Page Mode Successive Data Maximum Access Time (GPMC_FCLK cycles) |     | P <sup>(2)</sup> | cycles |
| FA21 | $t_{acc2-pgmode(DAT)}$ | Page Mode First Data Maximum Access Time (GPMC_FCLK cycles)      |     | H <sup>(1)</sup> | cycles |
| -    | $t_{su(DV-OEH)}$       | Setup time, read gpmc_ad[15:0] valid before gpmc_oen_ren high    | 1.9 |                  | ns     |
| -    | $t_h(OEH-DV)$          | Hold time, read gpmc_ad[15:0] valid after gpmc_oen_ren high      | 1   |                  | ns     |

- (1)  $H = \text{Access Time} \times (\text{TimeParaGranularity} + 1)$   
 (2)  $P = \text{PageBurstAccessTime} \times (\text{TimeParaGranularity} + 1)$

**表 5-36. GPMC/NOR Flash Interface Switching Characteristics - Asynchronous Mode**

| NO.  | PARAMETER            | DESCRIPTION                                                                       | MIN     | MAX     | UNIT |
|------|----------------------|-----------------------------------------------------------------------------------|---------|---------|------|
| -    | $t_{r(DO)}$          | Rising time, gpmc_ad[15:0] output data                                            | 0.447   | 4.067   | ns   |
| -    | $t_{f(DO)}$          | Falling time, gpmc_ad[15:0] output data                                           | 0.43    | 4.463   | ns   |
| FA0  | $t_{w(nBEV)}$        | Pulse duration, gpmc_ben[1:0] valid time                                          |         | N       | ns   |
| FA1  | $t_{w(nCSV)}$        | Pulse duration, gpmc_cs[7:0] low                                                  |         | A       | ns   |
| FA3  | $t_{d(nCSV-nADVIV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_advn_ale invalid                           | B - 0.2 | B + 2.0 | ns   |
| FA4  | $t_{d(nCSV-nOEIV)}$  | Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren invalid (Single read)              | C - 0.2 | C + 2.0 | ns   |
| FA9  | $t_{d(AV-nCSV)}$     | Delay time, address bus valid to gpmc_cs[7:0] valid                               | J - 0.2 | J + 2.0 | ns   |
| FA10 | $t_{d(nBEV-nCSV)}$   | Delay time, gpmc_ben[1:0] valid to gpmc_cs[7:0] valid                             | J - 0.2 | J + 2.0 | ns   |
| FA12 | $t_{d(nCSV-nADVIV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_advn_ale valid                             | K - 0.2 | K + 2.0 | ns   |
| FA13 | $t_{d(nCSV-nOEIV)}$  | Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren valid                              | L - 0.2 | L + 2.0 | ns   |
| FA16 | $t_{w(AIV)}$         | Pulse duration, address invalid between 2 successive R/W accesses                 | G       |         | ns   |
| FA18 | $t_{d(nCSV-nOEIV)}$  | Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren invalid (Burst read)               | I - 0.2 | I + 2.0 | ns   |
| FA20 | $t_{w(AV)}$          | Pulse duration, address valid : 2nd, 3rd and 4th accesses                         | D       |         | ns   |
| FA25 | $t_{d(nCSV-nWEV)}$   | Delay time, gpmc_cs[7:0] valid to gpmc_wen valid                                  | E - 2   | E + 2.0 | ns   |
| FA27 | $t_{d(nCSV-nWEIV)}$  | Delay time, gpmc_cs[7:0] valid to gpmc_wen invalid                                | F - 0.2 | F + 2.0 | ns   |
| FA28 | $t_{d(nWEV-DV)}$     | Delay time, gpmc_wen valid to data bus valid                                      |         | 2       | ns   |
| FA29 | $t_{d(DV-nCSV)}$     | Delay time, data bus valid to gpmc_cs[7:0] valid                                  | J - 0.2 | J + 2.0 | ns   |
| FA37 | $t_{d(nOEIV-AIV)}$   | Delay time, gpmc_oen_ren valid to gpmc_ad[15:0] multiplexed address bus phase end |         | 2       | ns   |

- (1) For single read:  $N = \text{RdCycleTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$   
 For single write:  $N = \text{WrCycleTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$   
 For burst read:  $N = (\text{RdCycleTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$   
 For burst write:  $N = (\text{WrCycleTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$
- (2) For single read:  $A = (\text{CSRdOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$   
 For single write:  $A = (\text{CSWrOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$   
 For burst read:  $A = (\text{CSRdOffTime} - \text{CSOnTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK period}$   
 For burst write:  $A = (\text{CSWrOffTime} - \text{CSOnTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK period}$   
 with n the page burst access number.
- (3) For reading:  $B = ((\text{ADVrdOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{ADVExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}$   
 For writing:  $B = ((\text{ADVWrOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{ADVExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}$
- (4)  $C = ((\text{OEOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{OEExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}$  For single read:  $C = \text{RdCycleTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$
- (5)  $J = (\text{CSOnTime} \times (\text{TimeParaGranularity} + 1) + 0.5 \times \text{CSEExtraDelay}) \times \text{GPMC\_FCLK}$
- (6)  $K = ((\text{ADVOnTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{ADVExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}$
- (7)  $L = ((\text{OEOnTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{OEExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}$
- (8)  $G = \text{Cycle2CycleDelay} \times \text{GPMC\_FCLK} \times (\text{TimeParaGranularity} + 1)$
- (9)  $I = ((\text{OEOffTime} + (n - 1) \times \text{PageBurstAccessTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{OEExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}$
- (10)  $D = \text{PageBurstAccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$
- (11)  $E = ((\text{WEOnTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{WEExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}$
- (12)  $F = ((\text{WEOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{WEExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}$



**FIG 5-28. GPMC / NOR Flash - Asynchronous Read - Single Word Timing<sup>(1)(2)(3)</sup>**

- (1) In gpmc\_csi, i = 0 to 7. In gpmc\_waitj, j = 0 to 1.
- (2) FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- (3) GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.
- (4) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

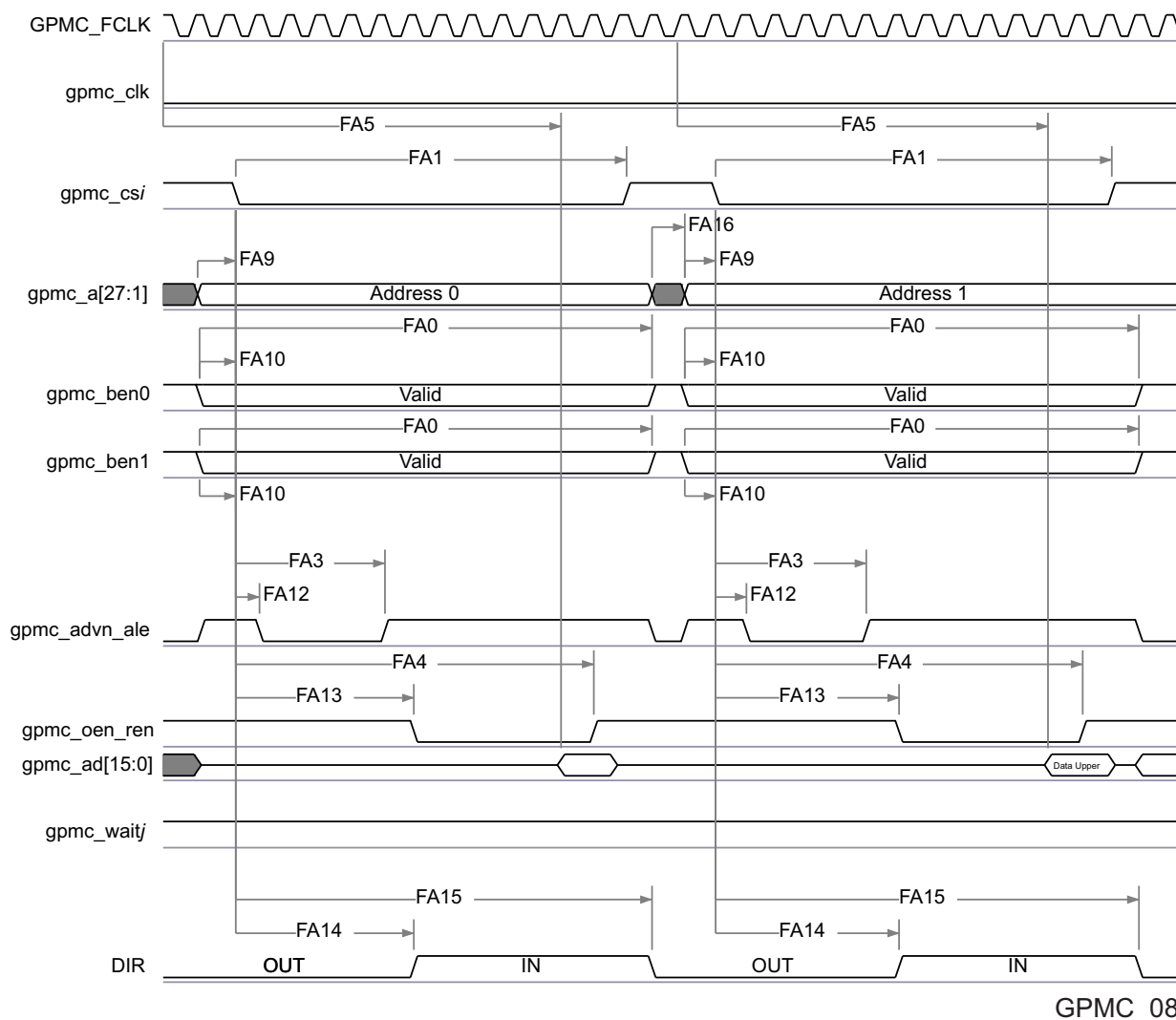
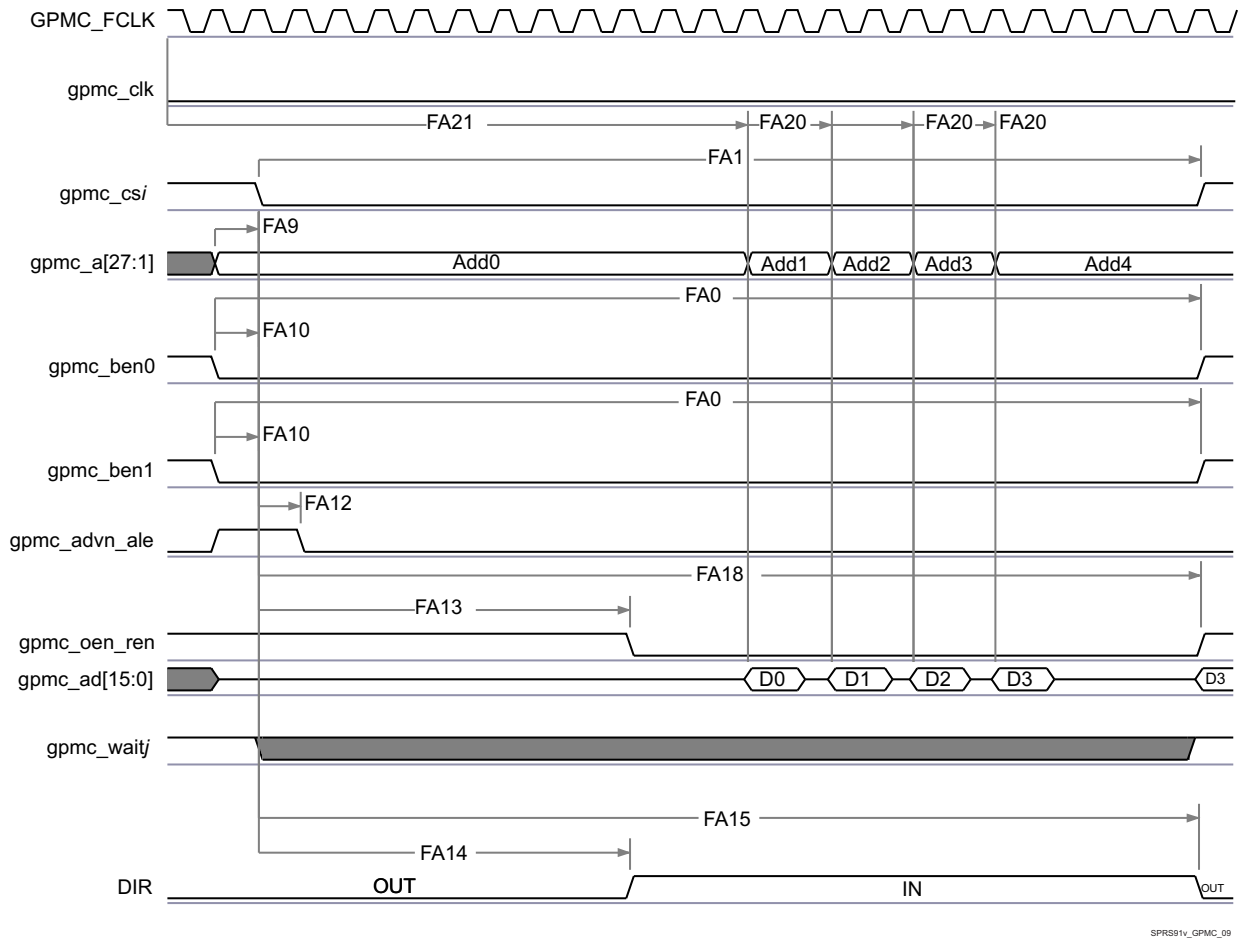


图 5-29. GPMC / NOR Flash - Asynchronous Read - 32-bit Timing<sup>(1)(2)(3)</sup>

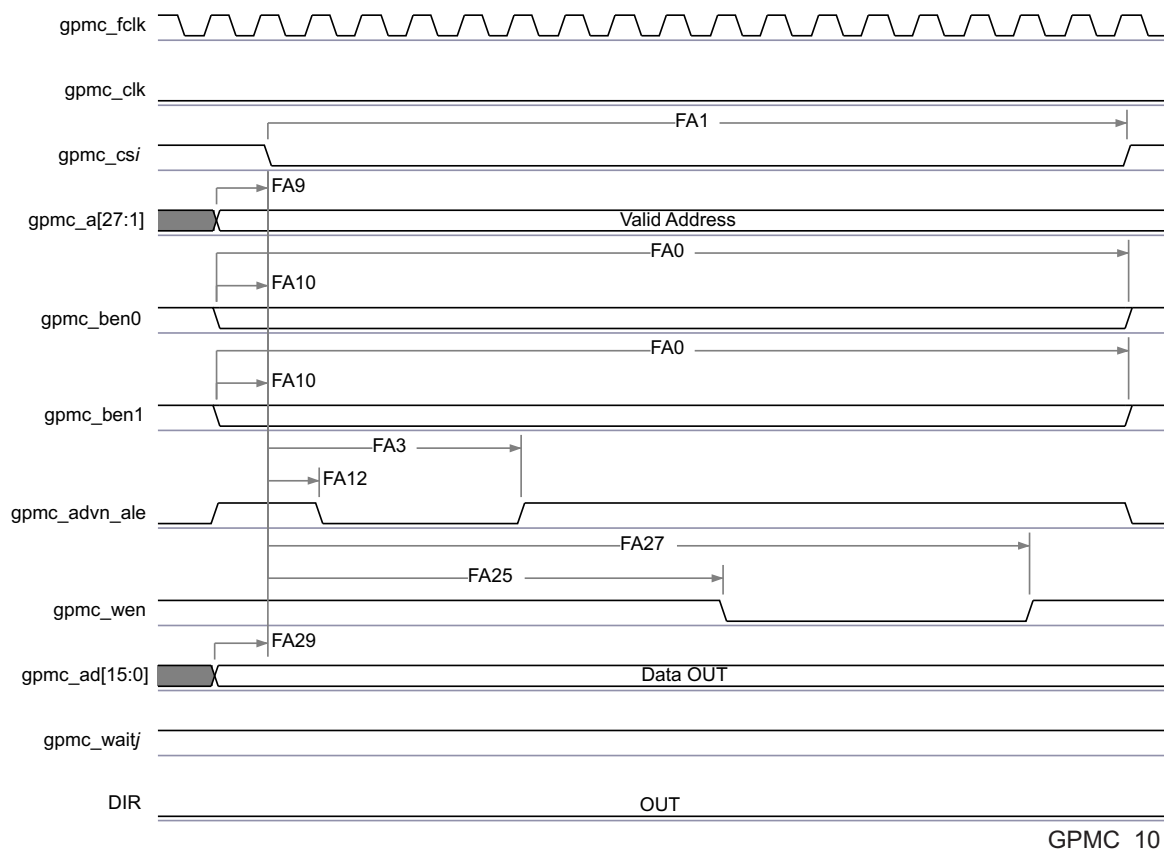
- (1) In "gpmc\_csi", i = 0 to 7. In "gpmc\_waitj", j = 0 to 1.
- (2) FA5 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value should be stored inside AccessTime register bits field
- (3) GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally
- (4) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.



SPRS91v\_GPMC\_09

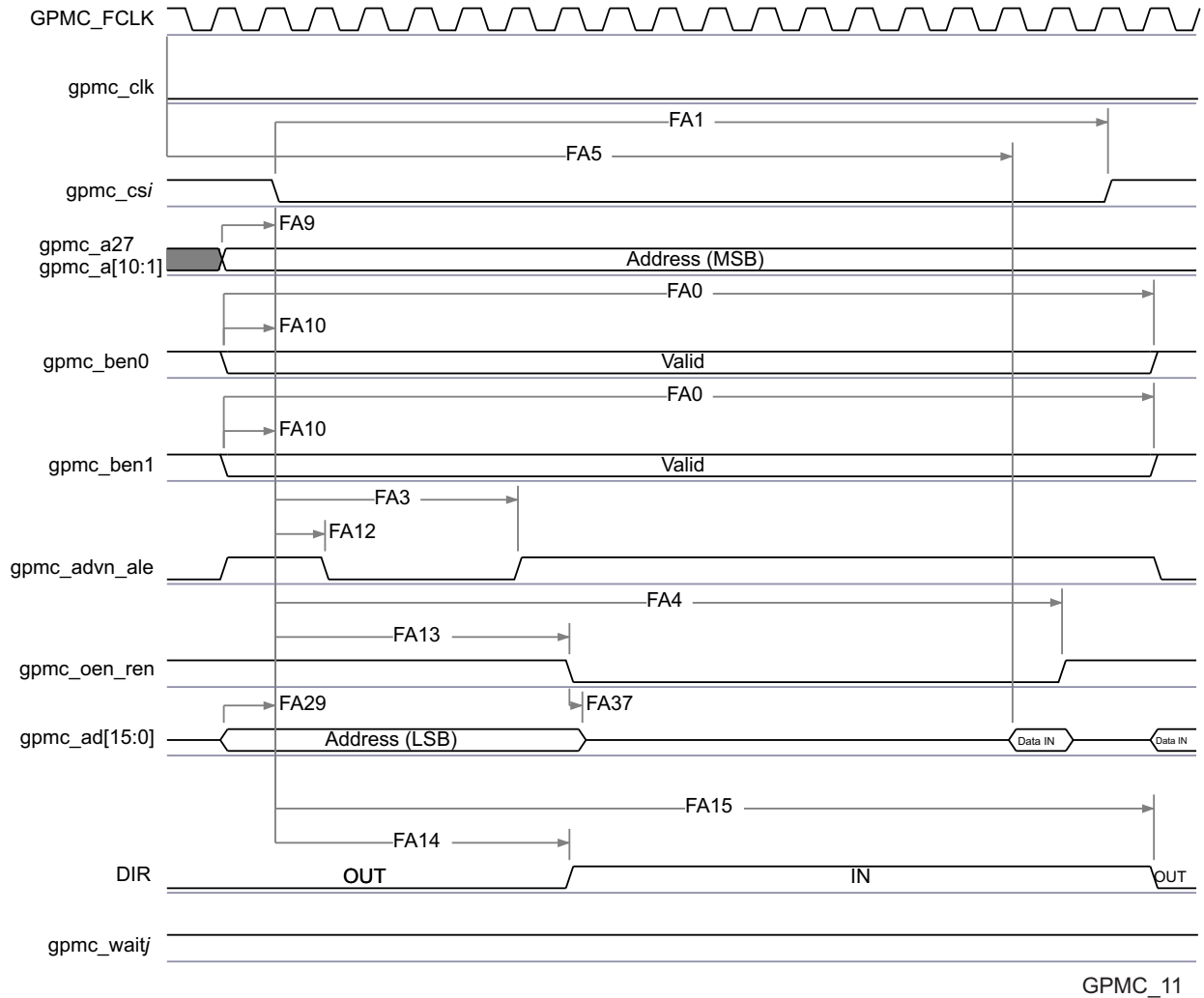
**5-30. GPMC / NOR Flash - Asynchronous Read - Page Mode 4x16-bit Timing<sup>(1)(2)(3)(4)</sup>**

- (1) In "gpmc\_csi", i = 0 to 7. In "gpmc\_waitj", j = 0 to 1
- (2) FA21 parameter illustrates amount of time required to internally sample first input Page Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, First input Page Data will be internally sampled by active functional clock edge. FA21 calculation is detailed in a separated application note (ref ...) and should be stored inside AccessTime register bits field.
- (3) FA20 parameter illustrates amount of time required to internally sample successive input Page Data. It is expressed in number of GPMC functional clock cycles. After each access to input Page Data, next input Page Data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input Page Data (excluding first input Page Data). FA20 value should be stored in PageBurstAccessTime register bits field.
- (4) GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally
- (5) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.



**FIG 5-31. GPMC / NOR Flash - Asynchronous Write - Single Word Timing<sup>(1)</sup>**

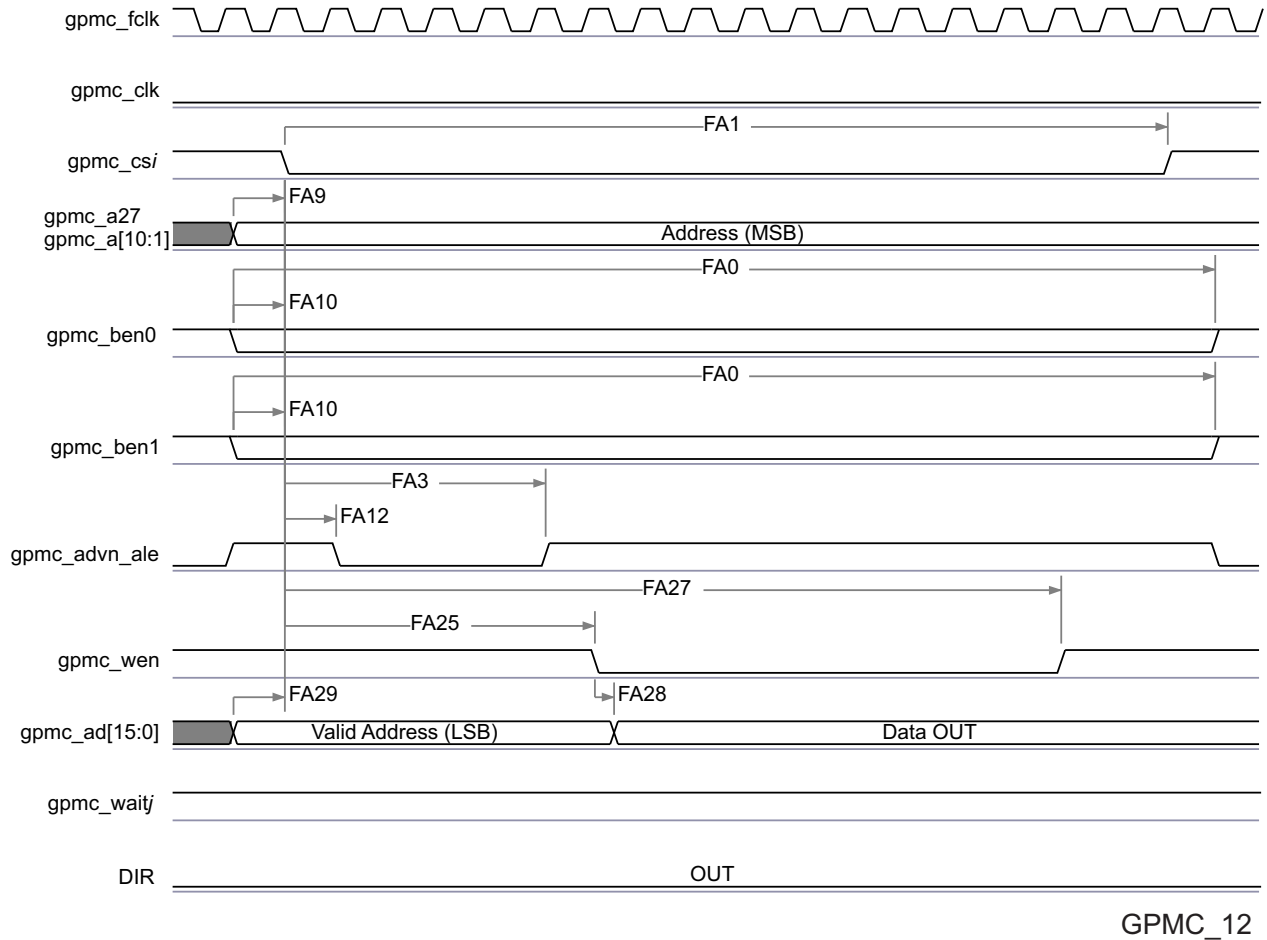
- (1) In "gpmc\_csi", i = 0 to 7. In "gpmc\_waitj", j = 0 to 1.
- (2) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.



GPMC\_11

**图 5-32. GPMC / Multiplexed NOR Flash - Asynchronous Read - Single Word Timing<sup>(1)(2)(3)</sup>**

- (1) In "gpmc\_csi", i = 0 to 7. In "gpmc\_waitj", j = 0 to 1
- (2) FA5 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value should be stored inside AccessTime register bits field.
- (3) GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally
- (4) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.



**图 5-33. GPMC / Multiplexed NOR Flash - Asynchronous Write - Single Word Timing<sup>(1)</sup>**

- (1) In "gpmc\_csi", i = 0 to 7. In "gpmc\_waitj", j = 0 to 1.  
(2) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

### 5.9.6.5.3 GPMC/NAND Flash Interface Asynchronous Timing

表 5-37 和 表 5-38 假设测试 over 的 recommended operating conditions 和 electrical characteristic conditions below (see 图 5-34, 图 5-35, 图 5-36 和 图 5-37).

**表 5-37. GPMC/NAND Flash Interface Timing Requirements<sup>(1)</sup>**

| NO.   | PARAMETER        | DESCRIPTION                                                   | MIN | MAX | UNIT   |
|-------|------------------|---------------------------------------------------------------|-----|-----|--------|
| GNF12 | $t_{acc}(DAT)$   | Data maximum access time (GPMC_FCLK Cycles)                   |     | J   | cycles |
| -     | $t_{su}(DV-OEH)$ | Setup time, read gpmc_ad[15:0] valid before gpmc_oen_ren high | 1.9 |     | ns     |
| -     | $t_h(OEH-DV)$    | Hold time, read gpmc_ad[15:0] valid after gpmc_oen_ren high   | 1   |     | ns     |

- (1)  $J = \text{AccessTime} \times (\text{TimeParaGranularity} + 1)$

**表 5-38. GPMC/NAND Flash Interface Switching Characteristics**

| NO.  | PARAMETER        | DESCRIPTION                                      | MIN                    | MAX                    | UNIT |
|------|------------------|--------------------------------------------------|------------------------|------------------------|------|
| -    | $t_{r}(DO)$      | Rising time, gpmc_ad[15:0] output data           | 0.447                  | 4.067                  | ns   |
| -    | $t_{f}(DO)$      | Falling time, gpmc_ad[15:0] output data          | 0.43                   | 4.463                  | ns   |
| GNF0 | $t_w(nWEV)$      | Pulse duration, gpmc_wen valid time              |                        | A <sup>(1)</sup>       | ns   |
| GNF1 | $t_d(nCSV-nWEV)$ | Delay time, gpmc_cs[7:0] valid to gpmc_wen valid | B - 0.2 <sup>(2)</sup> | B + 2.0 <sup>(2)</sup> | ns   |

**表 5-38. GPMC/NAND Flash Interface Switching Characteristics (continued)**

| NO.   | PARAMETER            | DESCRIPTION                                              | MIN                     | MAX                     | UNIT |
|-------|----------------------|----------------------------------------------------------|-------------------------|-------------------------|------|
| GNF2  | $t_{d(CLEH-nWEV)}$   | Delay time, gpmc_ben[1:0] high to gpmc_wen valid         | C - 0.2 <sup>(3)</sup>  | C + 2.0 <sup>(3)</sup>  | ns   |
| GNF3  | $t_{d(nWEV-DV)}$     | Delay time, gpmc_ad[15:0] valid to gpmc_wen valid        | D - 0.2 <sup>(4)</sup>  | D + 2.0 <sup>(4)</sup>  | ns   |
| GNF4  | $t_{d(nWEIV-DIV)}$   | Delay time, gpmc_wen invalid to gpmc_ad[15:0] invalid    | E - 0.2 <sup>(5)</sup>  | E + 2.0 <sup>(5)</sup>  | ns   |
| GNF5  | $t_{d(nWEIV-CLEIV)}$ | Delay time, gpmc_wen invalid to gpmc_ben[1:0] invalid    | F - 0.2 <sup>(6)</sup>  | F + 2.0 <sup>(6)</sup>  | ns   |
| GNF6  | $t_{d(nWEIV-nCSIV)}$ | Delay time, gpmc_wen invalid to gpmc_cs[7:0] invalid     | G - 0.2 <sup>(7)</sup>  | G + 2.0 <sup>(7)</sup>  | ns   |
| GNF7  | $t_{d(ALEH-nWEV)}$   | Delay time, gpmc_adv_n_ale high to gpmc_wen valid        | C - 0.2 <sup>(3)</sup>  | C + 2.0 <sup>(3)</sup>  | ns   |
| GNF8  | $t_{d(nWEIV-ALEIV)}$ | Delay time, gpmc_wen invalid to gpmc_adv_n_ale invalid   | F - 0.2 <sup>(6)</sup>  | F + 2.0 <sup>(6)</sup>  | ns   |
| GNF9  | $t_{c(nWE)}$         | Cycle time, write cycle time                             |                         | H <sup>(8)</sup>        | ns   |
| GNF10 | $t_{d(nCSV-nOEIV)}$  | Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren valid     | I - 0.2 <sup>(9)</sup>  | I + 2.0 <sup>(9)</sup>  | ns   |
| GNF13 | $t_{w(nOEIV)}$       | Pulse duration, gpmc_oen_ren valid time                  |                         | K                       | ns   |
| GNF14 | $t_{c(nOE)}$         | Cycle time, read cycle time                              |                         | L <sup>(10)</sup>       | ns   |
| GNF15 | $t_{d(nOEIV-nCSIV)}$ | Delay time, gpmc_oen_ren invalid to gpmc_cs[7:0] invalid | M - 0.2 <sup>(11)</sup> | M + 2.0 <sup>(11)</sup> | ns   |

(1)  $A = (WEOffTime - WEOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK$

(2)  $B = ((WEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK$

(3)  $C = ((WEOnTime - ADVOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - ADVExtraDelay)) \times GPMC\_FCLK$

(4)  $D = (WEOnTime \times (TimeParaGranularity + 1) + 0.5 \times WEEExtraDelay) \times GPMC\_FCLK$

(5)  $E = (WrCycleTime - WEOffTime \times (TimeParaGranularity + 1) - 0.5 \times WEEExtraDelay) \times GPMC\_FCLK$

(6)  $F = (ADVWrOffTime - WEOffTime \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - WEEExtraDelay)) \times GPMC\_FCLK$

(7)  $G = (CSWrOffTime - WEOffTime \times (TimeParaGranularity + 1) + 0.5 \times (CSEExtraDelay - WEEExtraDelay)) \times GPMC\_FCLK$

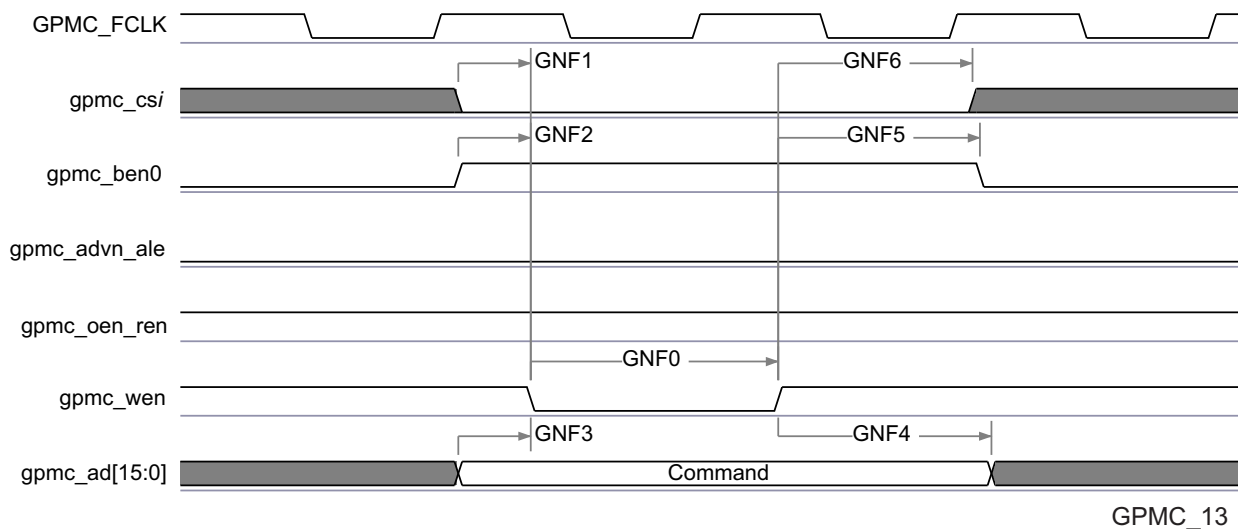
(8)  $H = WrCycleTime \times (1 + TimeParaGranularity) \times GPMC\_FCLK$

(9)  $I = ((OEOffTime + (n - 1) \times PageBurstAccessTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK$

(10)  $K = (OEOffTime - OEOnTime) \times (1 + TimeParaGranularity) \times GPMC\_FCLK$

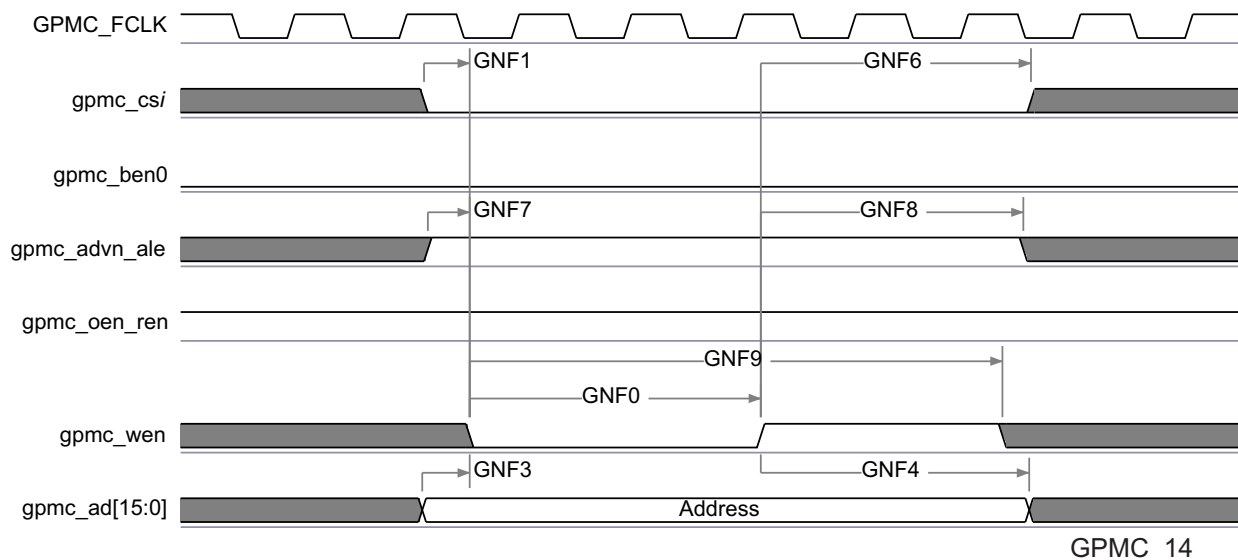
(11)  $L = RdCycleTime \times (1 + TimeParaGranularity) \times GPMC\_FCLK$

(12)  $M = (CSRdOffTime - OEOffTime \times (TimeParaGranularity + 1) + 0.5 \times (CSEExtraDelay - OEEExtraDelay)) \times GPMC\_FCLK$



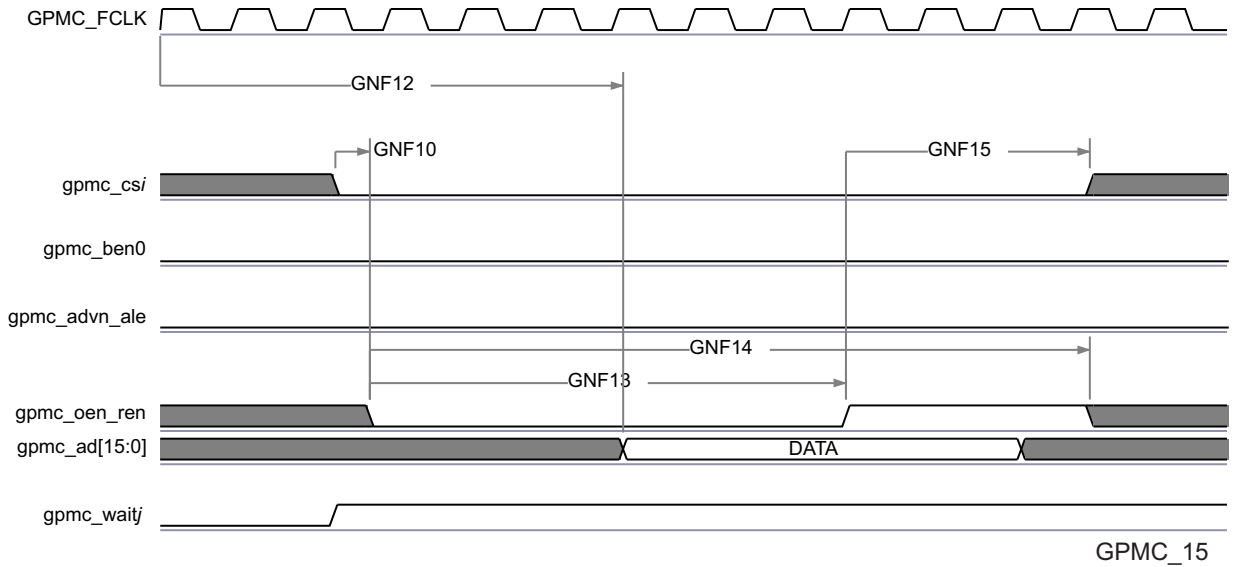
✖ 5-34. GPMC / NAND Flash - Command Latch Cycle Timing<sup>(1)</sup>

(1) In gpmc\_csi, i = 0 to 7.



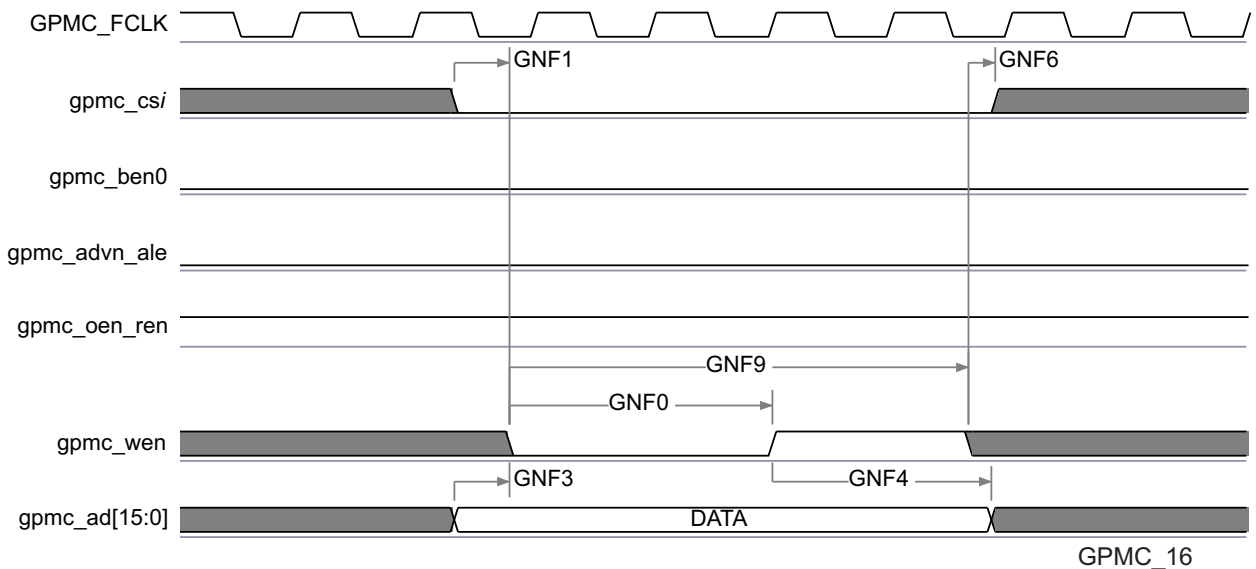
✖ 5-35. GPMC / NAND Flash - Address Latch Cycle Timing<sup>(1)</sup>

(1) In gpmc\_csi, i = 0 to 7.



**图 5-36. GPMC / NAND Flash - Data Read Cycle Timing<sup>(1)(2)(3)</sup>**

- (1) GNF12 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
- (2) GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.
- (3) In gpmc\_csi, i = 0 to 7. In gpmc\_waitj, j = 0 to 1.



**图 5-37. GPMC / NAND Flash - Data Write Cycle Timing<sup>(1)</sup>**

- (1) In gpmc\_csi, i = 0 to 7.

**注**

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bitfield for each corresponding pad control register.

The pad control registers are presented 表 4-29 and described in Device TRM, *Control Module* section.

### 5.9.6.6 GP Timers

The device has eight GP timers: TIMER1 through TIMER8.

- TIMER1 (1-ms tick) includes a specific function to generate accurate tick interrupts to the operating system and it belongs to the PD\_WKUPAON domain.
- TIMER2 through TIMER8 belong to the PD\_COREAON module.

Each timer can be clocked from the system clock (19.2, 20, or 27 MHz) or the 32-kHz clock. Select the clock source at the power, reset, and clock management (PRCM) module level.

Each timer provides an interrupt through the device IRQ\_CROSSBAR.

Each timer is connected to an external pin by their PWM output or their event capture input pin (for external timer triggering).

#### 5.9.6.6.1 GP Timer Features

The following are the main features of the GP timer controllers:

- Level 4 (L4) slave interface support:
  - 32-bit data bus width
  - 32- or 16-bit access supported
  - 8-bit access not supported
  - 10-bit address bus width
  - Burst mode not supported
  - Write nonposted transaction mode supported
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Compare and capture modes
- Autoreload mode
- Start and stop mode
- Programmable divider clock source ( $2_n$ , where  $n = [0:8]$ )
- Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
- Dedicated GP output signal for using the `TIMERi_GPO_CFG` signal
- On-the-fly read/write register (while counting)
- 1-ms tick with 32.768-Hz functional clock generated (only TIMER1)

### 5.9.6.7 I2C

The device includes 2 inter-integrated circuit (I2C) modules which provide an interface to other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus™) specification version 2.1. External components attached to this 2-wire serial bus can transmit/receive 8-bit data to/from the device through the I2C module.

---

注

Note that, I2C1 and I2C2, due to characteristics of the open drain IO cells, HS mode is not supported.

---

---

注

Inter-integrated circuit  $i$  ( $i=1$  to  $2$ ) module is also referred to as I2Ci.

---

## 注

For more information, see the Multimaster I2C Controller section of the Device TRM.

表 5-39 和 图 5-38 assume testing over the recommended operating conditions and electrical characteristic conditions below.

**表 5-39. Timing Requirements for I2C Input Timings<sup>(1)</sup>**

| NO. | PARAMETER           | DESCRIPTION                                                                   | STANDARD MODE    |                     | FAST MODE           |                    | UNIT    |
|-----|---------------------|-------------------------------------------------------------------------------|------------------|---------------------|---------------------|--------------------|---------|
|     |                     |                                                                               | MIN              | MAX                 | MIN                 | MAX                |         |
| 1   | $t_{c(SCL)}$        | Cycle time, SCL                                                               | 10               |                     | 2.5                 |                    | $\mu s$ |
| 2   | $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition)          | 4.7              |                     | 0.6                 |                    | $\mu s$ |
| 3   | $t_{h(SDAL-SCLL)}$  | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4                |                     | 0.6                 |                    | $\mu s$ |
| 4   | $t_{w(SCLL)}$       | Pulse duration, SCL low                                                       | 4.7              |                     | 1.3                 |                    | $\mu s$ |
| 5   | $t_{w(SCLH)}$       | Pulse duration, SCL high                                                      | 4                |                     | 0.6                 |                    | $\mu s$ |
| 6   | $t_{su(SDAV-SCLH)}$ | Setup time, SDA valid before SCL high                                         | 250              |                     | 100 <sup>(2)</sup>  |                    | ns      |
| 7   | $t_{h(SCLL-SDAV)}$  | Hold time, SDA valid after SCL low                                            | 0 <sup>(3)</sup> | 3.45 <sup>(4)</sup> | 0 <sup>(3)</sup>    | 0.9 <sup>(4)</sup> | $\mu s$ |
| 8   | $t_{w(SDAH)}$       | Pulse duration, SDA high between STOP and START conditions                    | 4.7              |                     | 1.3                 |                    | $\mu s$ |
| 9   | $t_r(SDA)$          | Rise time, SDA                                                                |                  | 1000                | $20 + 0.1C_b^{(5)}$ | 300                | ns      |
| 10  | $t_r(SCL)$          | Rise time, SCL                                                                |                  | 1000                | $20 + 0.1C_b^{(5)}$ | 300                | ns      |
| 11  | $t_f(SDA)$          | Fall time, SDA                                                                |                  | 300                 | $20 + 0.1C_b^{(5)}$ | 300                | ns      |
| 12  | $t_f(SCL)$          | Fall time, SCL                                                                |                  | 300                 | $20 + 0.1C_b^{(5)}$ | 300                | ns      |
| 13  | $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition)                     | 4                |                     | 0.6                 |                    | $\mu s$ |
| 14  | $t_w(SP)$           | Pulse duration, spike (must be suppressed)                                    |                  |                     | 0                   | 50                 | ns      |
| 15  | $C_b^{(5)}$         | Capacitive load for each bus line                                             |                  | 400                 |                     | 400                | pF      |

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.

(2) A Fast-mode I<sup>2</sup>C-bus™ device can be used in a Standard-mode I<sup>2</sup>C-bus system, but the requirement  $t_{su(SDA-SCLH)} \geq 250$  ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_r \max + t_{su(SDA-SCLH)} = 1000 + 250 = 1250$  ns (according to the Standard-mode I<sup>2</sup>C-Bus Specification) before the SCL line is released.

(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the  $V_{IHmin}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL.

(4) The maximum  $t_{h(SDA-SCLL)}$  has only to be met if the device does not stretch the low period [ $t_{w(SCLL)}$ ] of the SCL signal.

(5)  $C_b$  = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

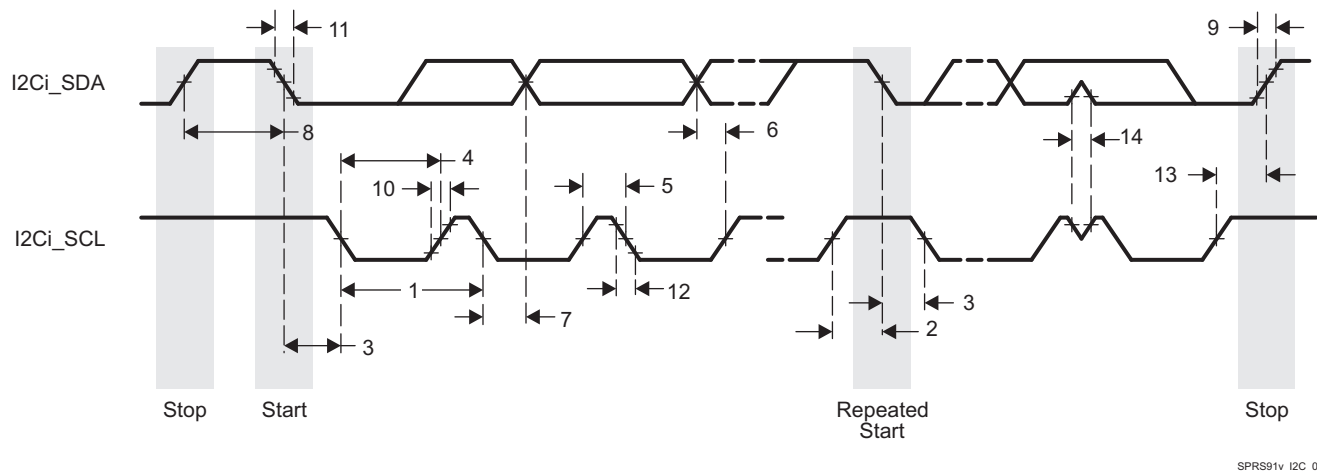


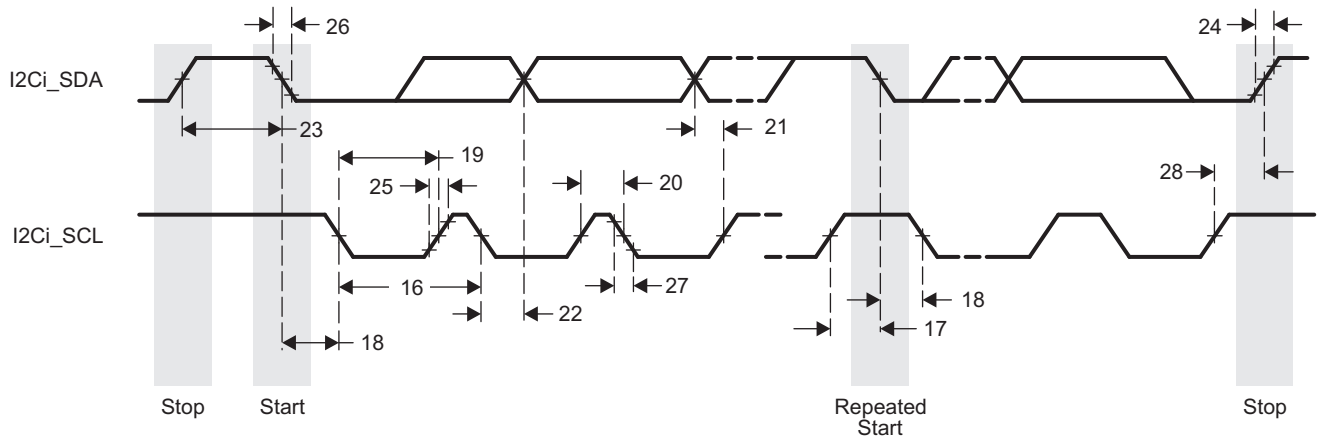
图 5-38. I2C Receive Timing

表 5-40 和 图 5-39 assume testing over the recommended operating conditions and electrical characteristic conditions below.

表 5-40. Switching Characteristics Over Recommended Operating Conditions for I2C Output Timings<sup>(2)</sup>

| NO. | PARAMETER           | DESCRIPTION                                                                   | STANDARD MODE |      | FAST MODE           |     | UNIT    |
|-----|---------------------|-------------------------------------------------------------------------------|---------------|------|---------------------|-----|---------|
|     |                     |                                                                               | MIN           | MAX  | MIN                 | MAX |         |
| 16  | $t_{c(SCL)}$        | Cycle time, SCL                                                               | 10            |      | 2.5                 |     | $\mu s$ |
| 17  | $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition)          | 4.7           |      | 0.6                 |     | $\mu s$ |
| 18  | $t_h(SDAL-SCLL)$    | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4             |      | 0.6                 |     | $\mu s$ |
| 19  | $t_w(SCLL)$         | Pulse duration, SCL low                                                       | 4.7           |      | 1.3                 |     | $\mu s$ |
| 20  | $t_w(SCLH)$         | Pulse duration, SCL high                                                      | 4             |      | 0.6                 |     | $\mu s$ |
| 21  | $t_{su(SDAV-SCLH)}$ | Setup time, SDA valid before SCL high                                         | 250           |      | 100                 |     | ns      |
| 22  | $t_h(SCLL-SDAV)$    | Hold time, SDA valid after SCL low (for I2C bus devices)                      | 0             | 3.45 | 0                   | 0.9 | $\mu s$ |
| 23  | $t_w(SDAH)$         | Pulse duration, SDA high between STOP and START conditions                    | 4.7           |      | 1.3                 |     | $\mu s$ |
| 24  | $t_r(SDA)$          | Rise time, SDA                                                                |               | 1000 | $20 + 0.1C_b^{(1)}$ | 300 | ns      |
| 25  | $t_r(SCL)$          | Rise time, SCL                                                                |               | 1000 | $20 + 0.1C_b^{(1)}$ | 300 | ns      |
| 26  | $t_f(SDA)$          | Fall time, SDA                                                                |               | 300  | $20 + 0.1C_b^{(1)}$ | 300 | ns      |
| 27  | $t_f(SCL)$          | Fall time, SCL                                                                |               | 300  | $20 + 0.1C_b^{(1)}$ | 300 | ns      |
| 28  | $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition)                     | 4             |      | 0.6                 |     | $\mu s$ |
| 29  | $C_p$               | Capacitance for each I2C pin                                                  |               | 10   |                     | 10  | pF      |

- (1)  $C_b$  = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.
- (2) Software must properly configure the I2C module registers to achieve the timings shown in this table. See the Device TRM for details.



SPRS91v\_I2C\_02

**图 5-39. I2C Transmit Timing**

### 5.9.6.8 UART

The UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU. There are 3 UART modules in the device. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices.

The UARTi (where i = 1 to 3) include the following features:

- 16C750 compatibility
- 64-byte FIFO buffer for receiver and 64-byte FIFO for transmitter
- Baud generation based on programmable divisors N (where N = 1...16 384) operating from a fixed functional clock of 48 MHz or 192 MHz
- Break character detection and generation
- Configurable data format:
  - Data bit: 5, 6, 7, or 8 bits
  - Parity bit: Even, odd, none
  - Stop-bit: 1, 1.5, 2 bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)

#### 注

For more information, see the UART section of the Device TRM.

表 5-41, 表 5-42 和 图 5-40 assume testing over the recommended operating conditions and electrical characteristic conditions below.

**表 5-41. Timing Requirements for UART**

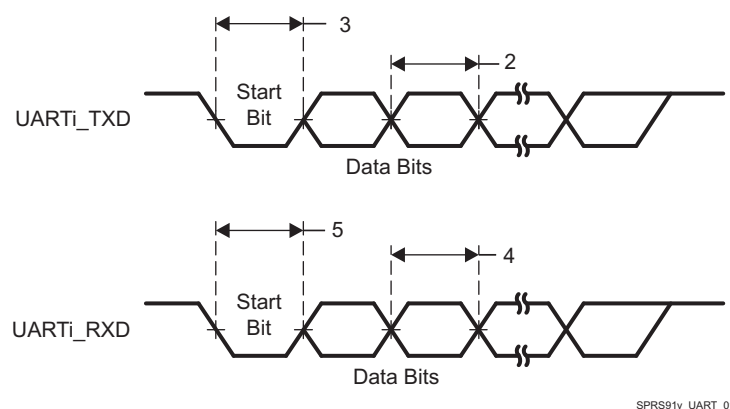
| NO. | PARAMETER     | DESCRIPTION                                             | MIN                  | MAX                  | UNIT |
|-----|---------------|---------------------------------------------------------|----------------------|----------------------|------|
| 4   | $t_{w(RX)}$   | Pulse width, receive data bit, 15/30/100pF high or low  | 0.96U <sup>(1)</sup> | 1.05U <sup>(1)</sup> | ns   |
| 5   | $t_{w(CTS)}$  | Pulse width, receive start bit, 15/30/100pF high or low | 0.96U <sup>(1)</sup> | 1.05U <sup>(1)</sup> | ns   |
|     | $t_d(RTS-TX)$ | Delay time, transmit start bit to transmit data         | P <sup>(2)</sup>     |                      | ns   |
|     | $t_d(CTS-TX)$ | Delay time, receive start bit to transmit data          | P <sup>(2)</sup>     |                      | ns   |

- (1)  $U$  = UART baud time =  $1/\text{programmed baud rate}$   
(2)  $P$  = Clock period of the reference clock (FCLK, usually 48 MHz or 192MHz).

**表 5-42. Switching Characteristics Over Recommended Operating Conditions for UART**

| NO. | PARAMETER           | DESCRIPTION                                               | MIN           | MAX           | UNIT |
|-----|---------------------|-----------------------------------------------------------|---------------|---------------|------|
|     | $f_{(\text{baud})}$ | Maximum programmable baud rate                            | 15 pF         | 12            | MHz  |
|     |                     |                                                           | 30 pF         | 0.23          |      |
|     |                     |                                                           | 100 pF        | 0.115         |      |
| 2   | $t_{w(\text{TX})}$  | Pulse width, transmit data bit, 15/30/100 pF high or low  | $U - 2^{(1)}$ | $U + 2^{(1)}$ | ns   |
| 3   | $t_{w(\text{RTS})}$ | Pulse width, transmit start bit, 15/30/100 pF high or low | $U - 2^{(1)}$ | $U + 2^{(1)}$ | ns   |

- (1)  $U$  = UART baud time =  $1/\text{programmed baud rate}$



SPRS91v\_UART\_01

**图 5-40. UART Timing**

**注意**

The IO timings provided in this section are only valid if signals within a single IOSET are used. The IOSETs are defined in 表 5-43.

In 表 5-43 are presented the specific groupings of signals (IOSET) for use with UART.

**表 5-43. UART1-3 IOSETs**

| SIGNALS      | IOSET1 |     | IOSET2 |     | IOSET3 |     |
|--------------|--------|-----|--------|-----|--------|-----|
|              | BALL   | MUX | BALL   | MUX | BALL   | MUX |
| <b>UART1</b> |        |     |        |     |        |     |
| uart1_rxd    | F13    | 0   | F13    | 0   |        |     |
| uart1_txd    | E14    | 0   | E14    | 0   |        |     |
| uart1_rtsn   |        |     | C14    | 0   |        |     |
| uart1_ctsn   |        |     | F14    | 0   |        |     |
| <b>UART2</b> |        |     |        |     |        |     |
| uart2_rxd    | E7     | 2   | D14    | 0   |        |     |
| uart2_txd    | F7     | 2   | D15    | 0   |        |     |
| uart2_rtsn   |        |     | F16    | 0   |        |     |
| uart2_ctsn   |        |     | F15    | 0   |        |     |
| <b>UART3</b> |        |     |        |     |        |     |
| uart3_rxd    | W7     | 4   | L1     | 1   | M2     | 1   |
| uart3_txd    | W6     | 4   | L2     | 1   | R6     | 1   |
| uart3_rtsn   |        |     | R7     | 1   | T5     | 1   |

**表 5-43. UART1-3 IOSETs (continued)**

| SIGNALS    | IOSET1 |     | IOSET2 |     | IOSET3 |     |
|------------|--------|-----|--------|-----|--------|-----|
|            | BALL   | MUX | BALL   | MUX | BALL   | MUX |
| uart3_ctsn |        |     | N4     | 1   | U6     | 1   |

### 5.9.6.9 McSPI

The McSPI is a master/slave synchronous serial bus. There are four separate McSPI modules (SPI1, SPI2, SPI3, and SPI4) in the device. All these four modules support up to four external devices (four chip selects) and are able to work as both master and slave.

The McSPI modules include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to four master channels, or single channel in slave mode
- Master multichannel mode:
  - Full duplex/half duplex
  - Transmit-only/receive-only/transmit-and-receive modes
  - Flexible input/output (I/O) port controls per channel
  - Programmable clock granularity
  - SPI configuration per channel. This means, clock definition, polarity enabling and word width
- Power management through wake-up capabilities
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel.
- Each SPI module supports multiple chip select pins spim\_cs[i], where i = 1 to 4.

#### 注

For more information, see the Serial Communication Interface section of the device TRM.

#### 注

The McSPIm module (m = 1 to 4) is also referred to as SPIm.

表 5-44, 图 5-41 和 图 5-42 present Timing Requirements for McSPI - Master Mode.

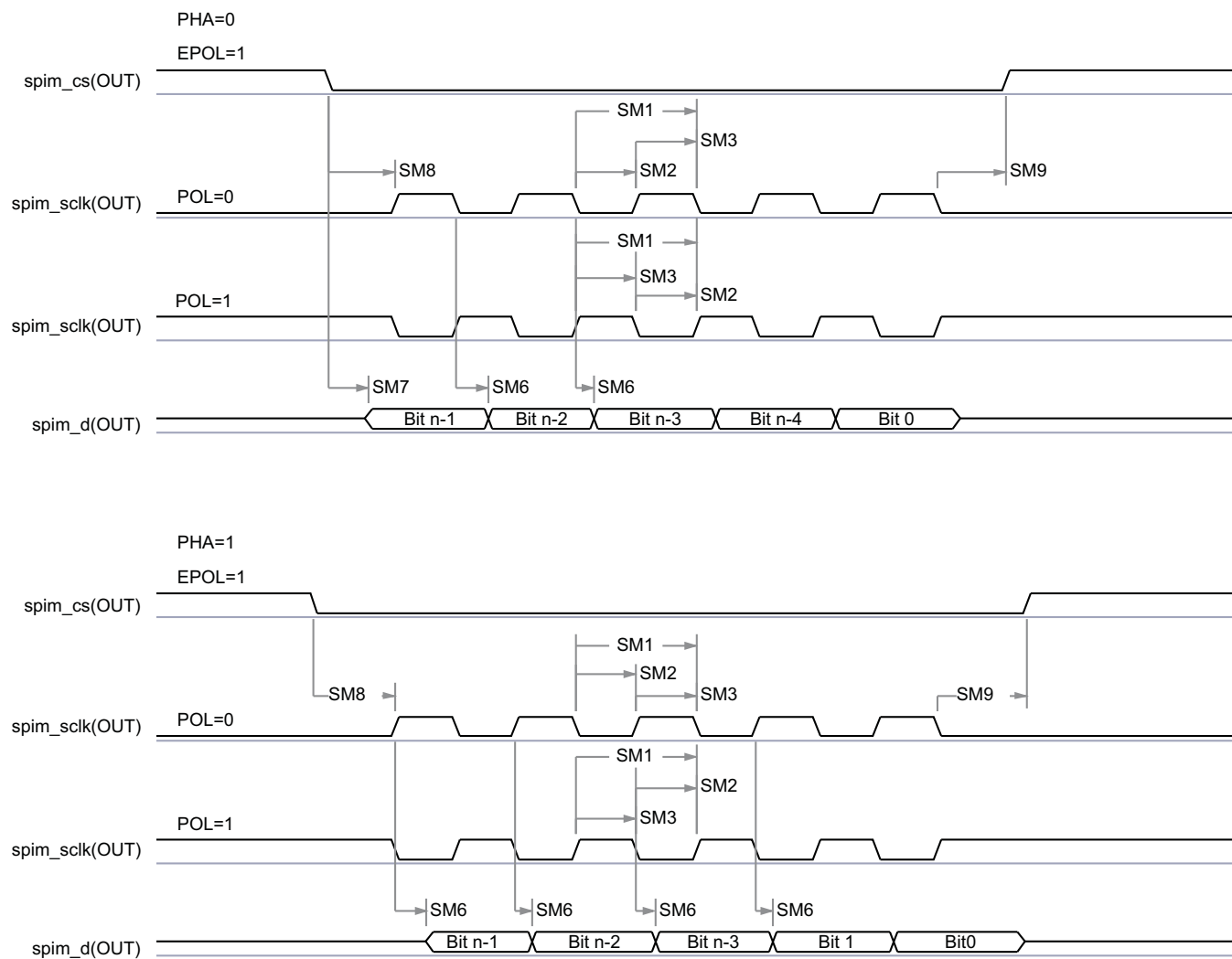
**表 5-44. Timing Requirements for SPI - Master Mode**

| NO. | PARAMETER             | DESCRIPTION                                                            | MODE           | MIN            | MAX  | UNIT |
|-----|-----------------------|------------------------------------------------------------------------|----------------|----------------|------|------|
| SM1 | $t_{C(SPICLK)}$       | Cycle time, spi_sclk <sup>(1) (2)</sup>                                | SPI1/2/3/<br>4 | 20.8           |      | ns   |
| SM2 | $t_{W(SPICLKL)}$      | Typical Pulse duration, spi_sclk low <sup>(1)</sup>                    |                | 0.5×P-1<br>(3) |      | ns   |
| SM3 | $t_{W(SPICLKH)}$      | Typical Pulse duration, spi_sclk high <sup>(1)</sup>                   |                | 0.5×P-1<br>(3) |      | ns   |
| SM4 | $t_{SU(MISO-SPICLK)}$ | Setup time, spi_d[x] valid before spi_sclk active edge <sup>(1)</sup>  |                | 2.29           |      | ns   |
| SM5 | $t_{H(SPICLK-MISO)}$  | Hold time, spi_d[x] valid after spi_sclk active edge <sup>(1)</sup>    |                | 2.67           |      | ns   |
| SM6 | $t_{d(SPICLK-SIMO)}$  | Delay time, spi_sclk active edge to spi_d[x] transition <sup>(1)</sup> | SPI1/2/4       | -3.57          | 3.57 | ns   |
|     |                       |                                                                        | SPI3           | -3.57          | 3.57 | ns   |
| SM7 | $t_{d(CS-SIMO)}$      | Delay time, spi_cs[x] active edge to spi_d[x] transition               |                |                | 3.57 | ns   |

表 5-44. Timing Requirements for SPI - Master Mode (continued)

| NO. | PARAMETER          | DESCRIPTION                                                         | MODE                   | MIN       | MAX | UNIT |
|-----|--------------------|---------------------------------------------------------------------|------------------------|-----------|-----|------|
| SM8 | $t_{d(CS-SPICLK)}$ | Delay time, spi_cs[x] active to spi_sclk first edge <sup>(1)</sup>  | MASTER<br>_PHA0<br>(4) | B-4.2 (5) |     | ns   |
|     |                    |                                                                     | MASTER<br>_PHA1<br>(4) | A-4.2 (6) |     | ns   |
| SM9 | $t_{d(SPICLK-CS)}$ | Delay time, spi_sclk last edge to spi_cs[x] inactive <sup>(1)</sup> | MASTER<br>_PHA0<br>(4) | A-4.2 (6) |     | ns   |
|     |                    |                                                                     | MASTER<br>_PHA1<br>(4) | B-4.2 (5) |     | ns   |

- (1) This timing applies to all configurations regardless of SPI\_CLK polarity and which clock edges are used to drive output data and capture input data.
- (2) Related to the SPI\_CLK maximum frequency.
- (3) P = SPICLK period.
- (4) SPI\_CLK phase is programmable with the PHA bit of the SPI\_CH(i)CONF register.
- (5)  $B = (TCS + 0.5) \times TSPICLKREF \times Fratio$ , where TCS is a bit field of the SPI\_CH(i)CONF register and Fratio = Even  $\geq 2$ .
- (6) When P = 20.8 ns,  $A = (TCS + 1) \times TSPICLKREF$ , where TCS is a bit field of the SPI\_CH(i)CONF register. When P > 20.8 ns,  $A = (TCS + 0.5) \times Fratio \times TSPICLKREF$ , where TCS is a bit field of the SPI\_CH(i)CONF register.
- (7) The IO timings provided in this section are applicable for all combinations of signals for spi1 and spi2. However, the timings are only valid for spi3 and spi4 if signals within a single IOSET are used. The IOSETs are defined in the following tables.



SPRS914v\_McSPI\_01

**5-41. McSPI - Master Mode Transmit**

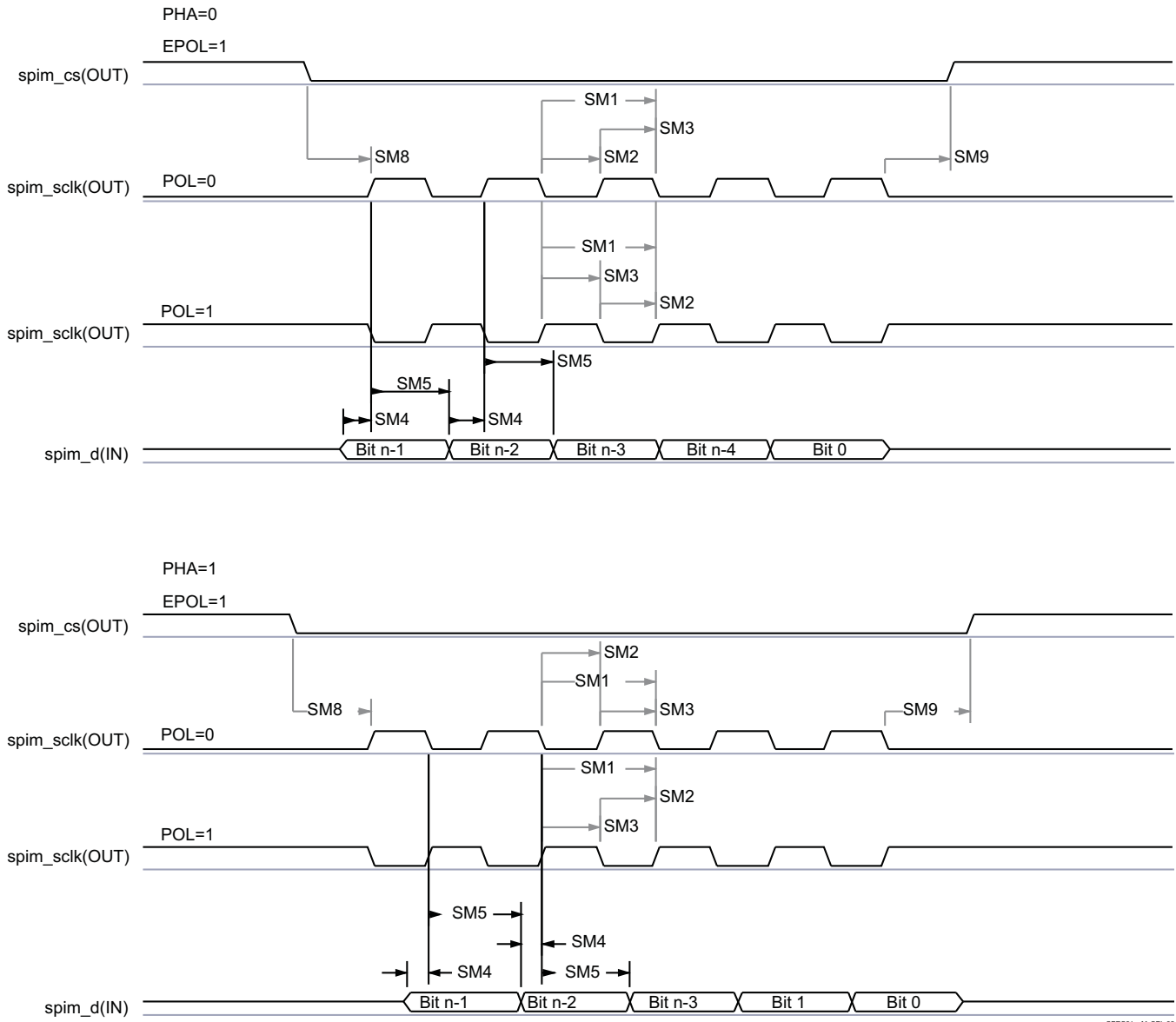


图 5-42. McSPI - Master Mode Receive

表 5-45, 图 5-43 和 图 5-44 present Timing Requirements for McSPI - Slave Mode.

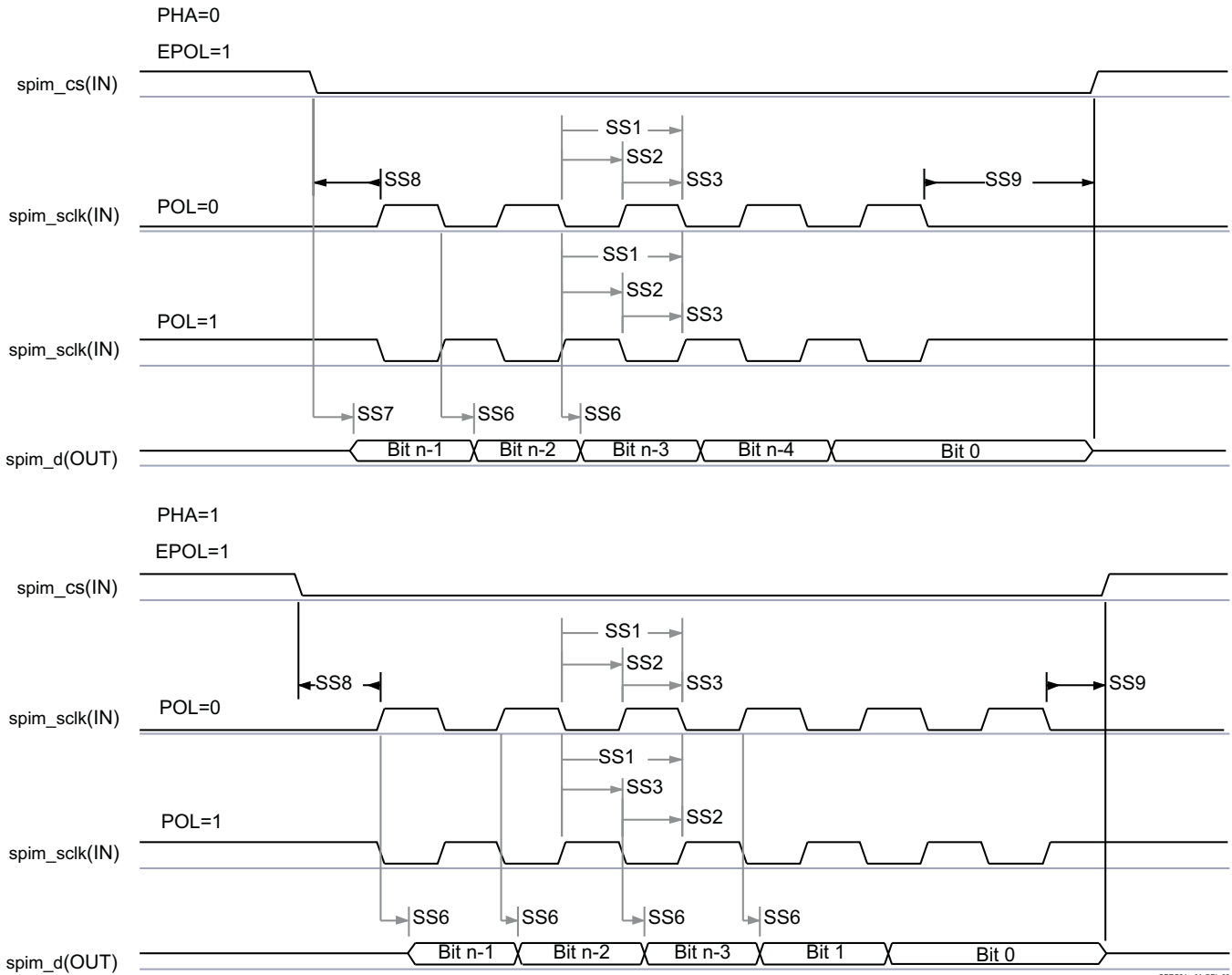
表 5-45. Timing Requirements for SPI - Slave Mode<sup>(5)</sup>

| NO.                                  | PARAMETER                           | DESCRIPTION                                                | MODE     | MIN    | MAX | UNIT |
|--------------------------------------|-------------------------------------|------------------------------------------------------------|----------|--------|-----|------|
| SS1 <sup>(1)</sup><br><sup>(2)</sup> | $t_c(\text{SPICLK})$                | Cycle time, spi_sclk                                       | SPI1     | 25     |     | ns   |
|                                      |                                     |                                                            | SPI2/3/4 | 33.3   |     | ns   |
| SS2 <sup>(1)</sup>                   | $t_w(\text{SPICLK})$ <sup>(3)</sup> | Typical Pulse duration, spi_sclk low                       |          | 0.45×P |     | ns   |
| SS3 <sup>(1)</sup>                   | $t_w(\text{SPICLK})$ <sup>(3)</sup> | Typical Pulse duration, spi_sclk high                      |          | 0.45×P |     | ns   |
| SS4 <sup>(1)</sup>                   | $t_{su}(\text{SIMO-SPICLK})$        | Setup time, spi_d[x] valid before spi_sclk active edge     |          | 2.82   |     | ns   |
| SS5 <sup>(1)</sup>                   | $t_h(\text{SPICLK-SIMO})$           | Hold time, spi_d[x] valid after spi_sclk active edge       |          | 2.82   |     | ns   |
| SS6 <sup>(1)</sup>                   | $t_d(\text{SPICLK-SOMI})$           | Delay time, spi_sclk active edge to mcspi_somi transition  | SPI1     | 2      | 9.8 | ns   |
|                                      |                                     |                                                            | SPI2/3/4 | 2      | 21  | ns   |
| SS7 <sup>(4)</sup>                   | $t_d(\text{CS-SOMI})$               | Delay time, spi_cs[x] active edge to mcspi_somi transition |          |        | 16  | ns   |
| SS8 <sup>(1)</sup>                   | $t_{su}(\text{CS-SPICLK})$          | Setup time, spi_cs[x] valid before spi_sclk first edge     |          | 2.82   |     | ns   |

**表 5-45. Timing Requirements for SPI - Slave Mode<sup>(5)</sup> (continued)**

| NO.                | PARAMETER          | DESCRIPTION                                         | MODE | MIN  | MAX | UNIT |
|--------------------|--------------------|-----------------------------------------------------|------|------|-----|------|
| SS9 <sup>(1)</sup> | $t_{H(SPICLK-CS)}$ | Hold time, spi_cs[x] valid after spi_sclk last edge |      | 2.82 |     | ns   |

- (1) This timing applies to all configurations regardless of SPI\_CLK polarity and which clock edges are used to drive output data and capture input data.
- (2) When operating the SPI interface in RX-only mode, the minimum Cycle time is 26ns (38.4MHz)
- (3) P = SPICLK period.
- (4) PHA = 0; SPI\_CLK phase is programmable with the PHA bit of the SPI\_CH(i)CONF register.
- (5) The IO timings provided in this section are applicable for all combinations of signals for spi1 and spi2. However, the timings are only valid for spi3 and spi4 if signals within a single IOSET are used. The IOSETs are defined in the following tables.



**图 5-43. McSPI - Slave Mode Transmit**

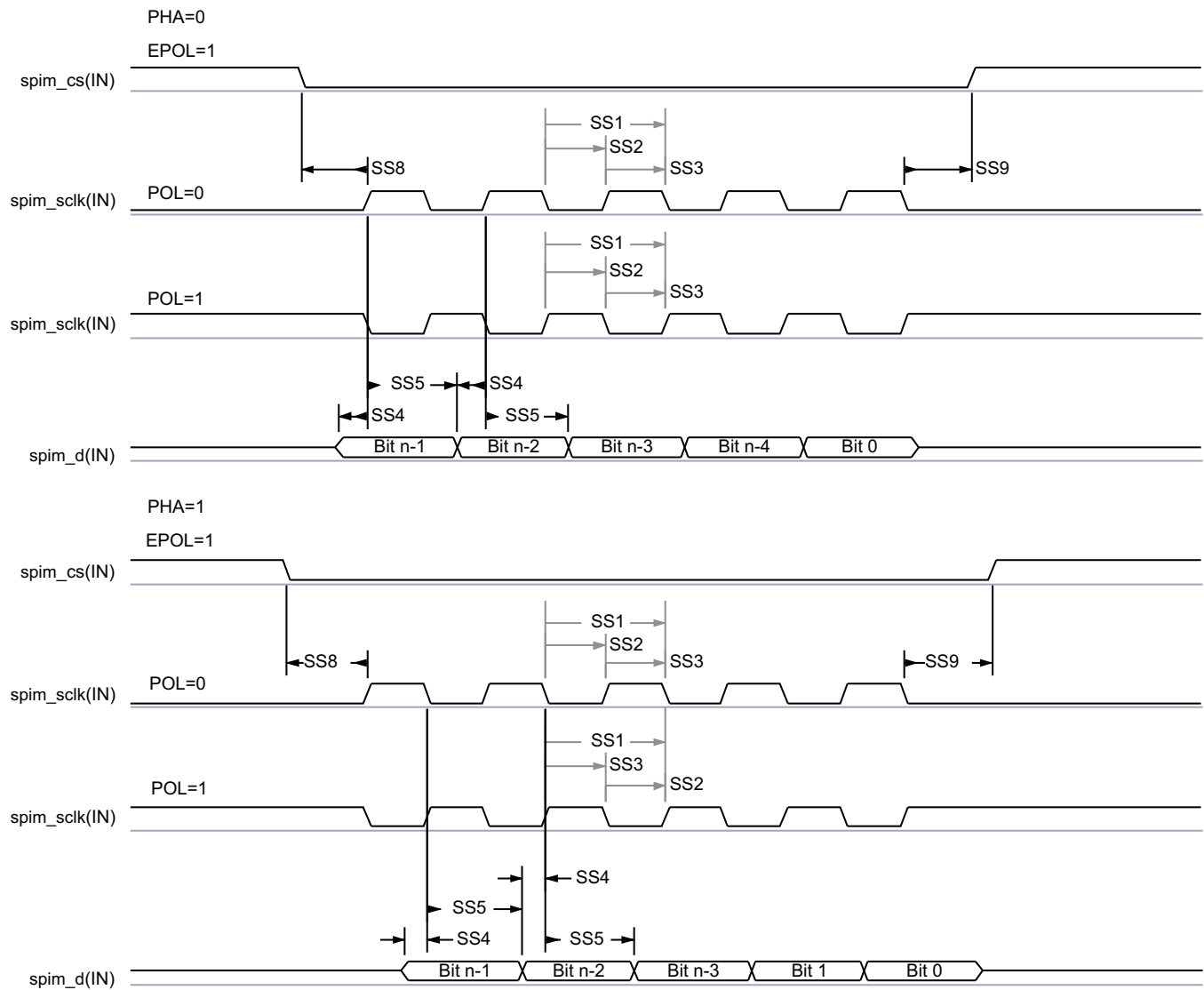


图 5-44. McSPI - Slave Mode Receive

注意

The IO timings provided in this section are applicable for all combinations of signals for SPI2 and SPI4. However, the timings are only valid for SPI1 and SPI3 if signals within a single IOSET are used. The IOSETs are defined in 表 5-46.

In 表 5-46 are presented the specific groupings of signals (IOSET) for use with McSPI.

表 5-46. McSPI1/3 IOSETs

| SIGNALS   | IOSET1 |     | IOSET2 |     | IOSET3 |     |
|-----------|--------|-----|--------|-----|--------|-----|
|           | BALL   | MUX | BALL   | MUX | BALL   | MUX |
| SPI1      |        |     |        |     |        |     |
| spi1_sclk | M2     | 0   | M2     | 0   | M2     | 0   |
| spi1_d1   | U6     | 0   | U6     | 0   | U6     | 0   |

**表 5-46. McSPI1/3 IOSETs (continued)**

| SIGNALS     | IOSET1 |     | IOSET2 |     | IOSET3 |     |
|-------------|--------|-----|--------|-----|--------|-----|
|             | BALL   | MUX | BALL   | MUX | BALL   | MUX |
| spi1_d0     | T5     | 0   | T5     | 0   | T5     | 0   |
| spi1_cs0    | R6     | 0   | R6     | 0   | R6     | 0   |
| spi1_cs1    |        |     |        |     | R5     | 0   |
| spi1_cs2    |        |     | F14    | 5   |        |     |
| spi1_cs3    |        |     | C14    | 5   |        |     |
| <b>SPI3</b> |        |     |        |     |        |     |
| spi3_sclk   | F15    | 4   | C6     | 4   |        |     |
| spi3_d1     | D14    | 4   | F7     | 4   |        |     |
| spi3_d0     | D15    | 4   | E7     | 4   |        |     |
| spi3_cs0    | F16    | 4   | B6     | 4   |        |     |

#### 5.9.6.10 QSPI

The Quad SPI (QSPI) module is a type of SPI module that allows single, dual or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. It works as a master only. There is one QSPI module in the device and it is primary intended for fast booting from quad-SPI flash memories.

General SPI features:

- Programmable clock divider
- Six pin interface (DCLK, CS\_N, DOUT, DIN, QDIN1, QDIN2)
- 4 external chip select signals
- Support for 3-, 4- or 6-pin SPI interface
- Programmable CS\_N to DOUT delay from 0 to 3 DCLKs
- Programmable signal polarities
- Programmable active clock edge
- Software controllable interface allowing for any type of SPI transfer

#### 注

For more information, see the Quad Serial Peripheral Interface section of the Device TRM.

#### 注意

The IO Timings provided in this section are only valid when all QSPI Chip Selects used in a system are configured to use the same Clock Mode (either Clock Mode 0 or Clock Mode 3).

表 5-47 和 表 5-48 present Timing and Switching Characteristics for Quad SPI Interface.

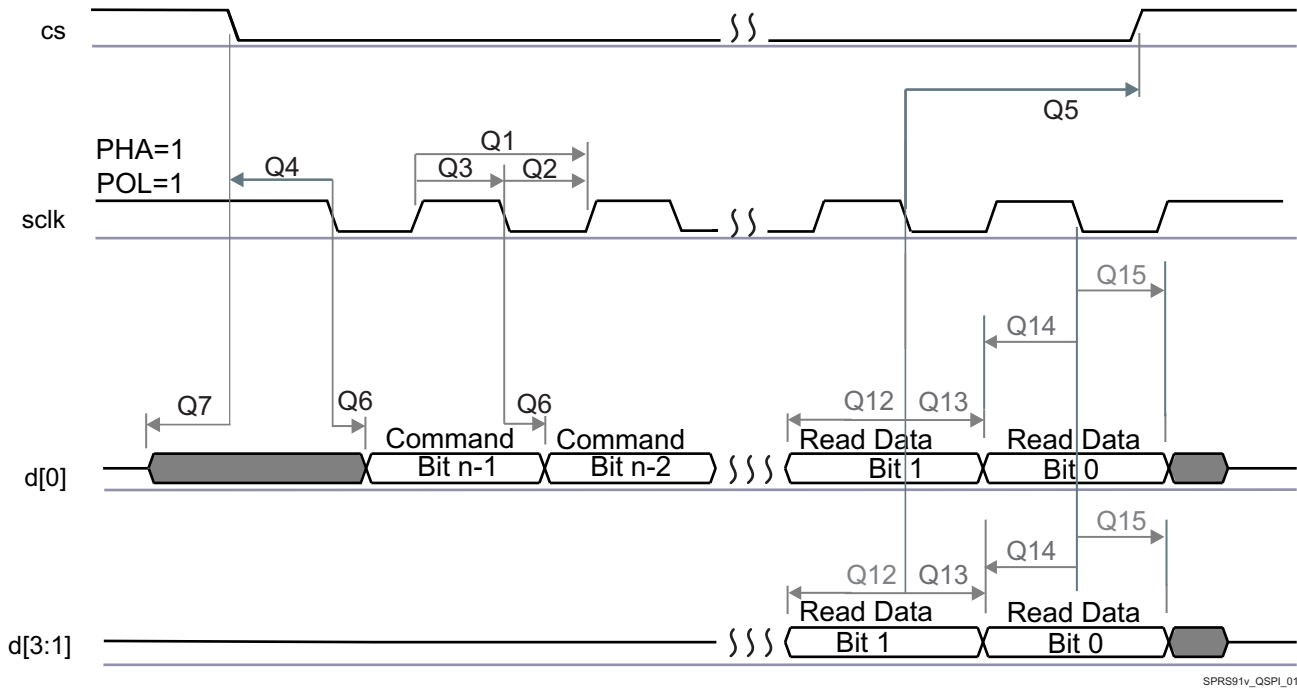
表 5-47. Switching Characteristics for QSPI

| No | PARAMETER                        | DESCRIPTION                                                  | Mode                              | MIN                          | MAX                          | UNIT |
|----|----------------------------------|--------------------------------------------------------------|-----------------------------------|------------------------------|------------------------------|------|
| 1  | $t_c(\text{SCLK})$               | Cycle time, sclk                                             | Default Timing Mode, Clock Mode 0 | 10.4                         |                              | ns   |
|    |                                  |                                                              | Default Timing Mode, Clock Mode 3 | 15.625                       |                              | ns   |
| 2  | $t_w(\text{SCLKL})$              | Pulse duration, sclk low                                     |                                   | $Y \times P - 1$<br>(1)      |                              | ns   |
| 3  | $t_w(\text{SCLKH})$              | Pulse duration, sclk high                                    |                                   | $Y \times P - 1$<br>(1)      |                              | ns   |
| 4  | $t_d(\text{CS-SCLK})$            | Delay time, sclk falling edge to cs active edge, CS3:0       | Default Timing Mode               | $-M \times P - 1$<br>(2) (3) | $-M \times P + 1$<br>(2) (3) | ns   |
| 5  | $t_d(\text{SCLK-CS})$            | Delay time, sclk falling edge to cs inactive edge, CS3:0     | Default Timing Mode               | $N \times P - 1$<br>(2) (3)  | $N \times P + 1$<br>(2) (3)  | ns   |
| 6  | $t_d(\text{SCLK-D1})$            | Delay time, sclk falling edge to d[0] transition             | Default Timing Mode               | -1                           | 1                            | ns   |
| 7  | $t_{\text{ena}}(\text{CS-D1LZ})$ | Enable time, cs active edge to d[0] driven (lo-z)            |                                   | -P-3.5                       | -P+2.5                       | ns   |
| 8  | $t_{\text{dis}}(\text{CS-D1Z})$  | Disable time, cs active edge to d[0] tri-stated (hi-z)       |                                   | -P-2.5                       | -P+2.0                       | ns   |
| 9  | $t_d(\text{SCLK-D1})$            | Delay time, sclk first falling edge to first d[0] transition | PHA=0 Only, Default Timing Mode   | -1-P                         | -1-P                         | ns   |

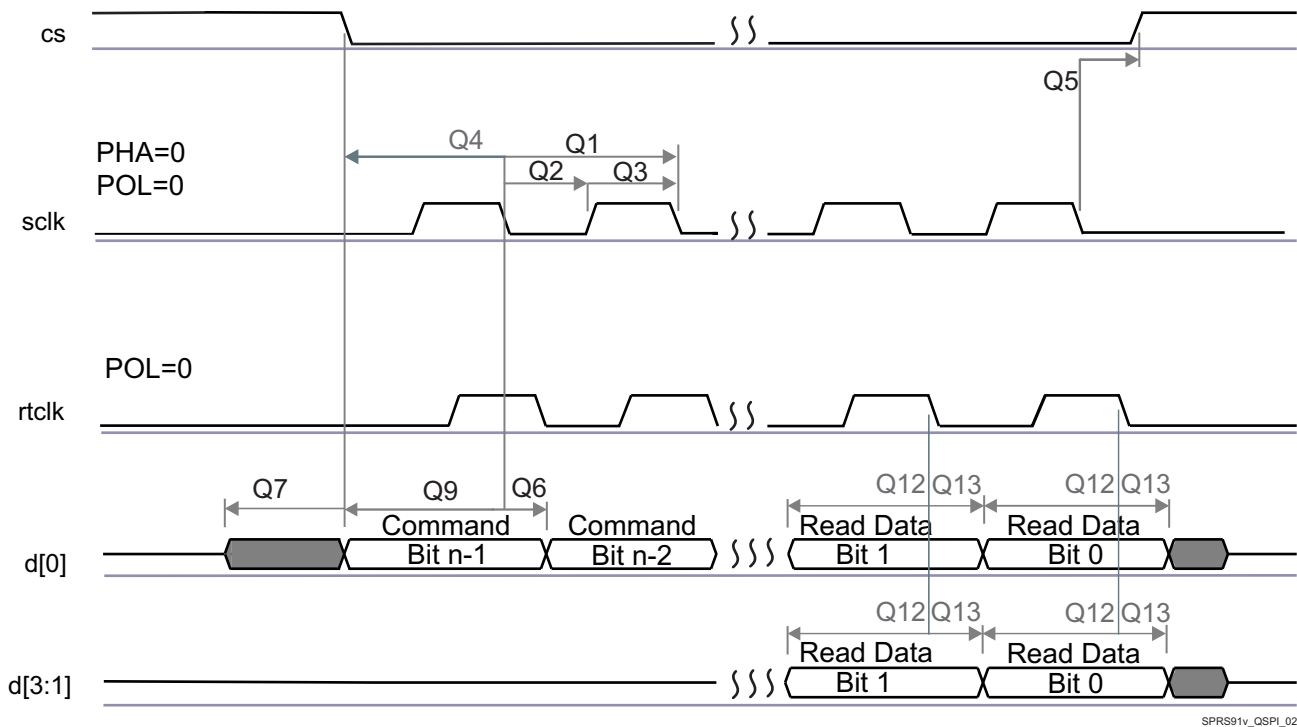
(1) The Y parameter is defined as follows: If DCLK\_DIV is 0 or ODD then, Y equals 0.5. If DCLK\_DIV is EVEN then, Y equals (DCLK\_DIV/2) / (DCLK\_DIV+1). For best performance, it is recommended to use a DCLK\_DIV of 0 or ODD to minimize the duty cycle distortion. The HSDIVIDER on CLKOUTX2\_H13 output of DPLL\_PER can be used to achieve the desired clock divider ratio. All required details about clock division factor DCLK\_DIV can be found in the device TRM.

(2) P = SCLK period.

(3) M=QSPI\_SPI\_DC\_REG.DDx + 1 when Clock Mode 0. M=QSPI\_SPI\_DC\_REG.DDx when Clock Mode 3. N = 2 when Clock Mode 0. N = 3 when Clock Mode 3.



5-45. QSPI Read (Clock Mode 3)



5-46. QSPI Read (Clock Mode 0)

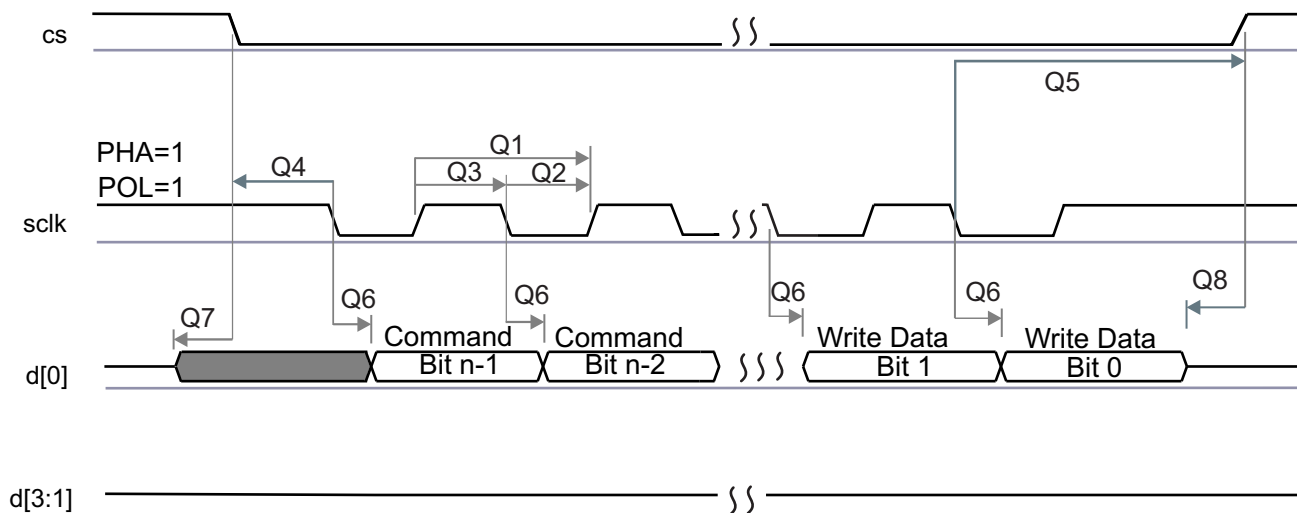
表 5-48. Timing Requirements for QSPI

| No | PARAMETER         | DESCRIPTION                                                       | MODE                              | MIN       | MAX | UNIT |
|----|-------------------|-------------------------------------------------------------------|-----------------------------------|-----------|-----|------|
| 12 | $t_{su}(D-RTCLK)$ | Setup time, d[3:0] valid before falling rtclk edge                | Default Timing Mode, Clock Mode 0 | 2.9       |     | ns   |
|    | $t_{su}(D-SCLK)$  | Setup time, d[3:0] valid before falling sclk edge                 | Default Timing Mode, Clock Mode 3 | 5.7       |     | ns   |
| 13 | $t_h(RTCLK-D)$    | Hold time, d[3:0] valid after falling rtclk edge                  | Default Timing Mode, Clock Mode 0 | -0.1      |     | ns   |
|    | $t_h(SCLK-D)$     | Hold time, d[3:0] valid after falling sclk edge                   | Default Timing Mode, Clock Mode 3 | 0.1       |     | ns   |
| 14 | $t_{su}(D-SCLK)$  | Setup time, final d[3:0] bit valid before final falling sclk edge | Default Timing Mode, Clock Mode 3 | 5.7-P (1) |     | ns   |
| 15 | $t_h(SCLK-D)$     | Hold time, final d[3:0] bit valid after final falling sclk edge   | Default Timing Mode, Clock Mode 3 | 0.1+P (1) |     | ns   |

(1) P = SCLK period.

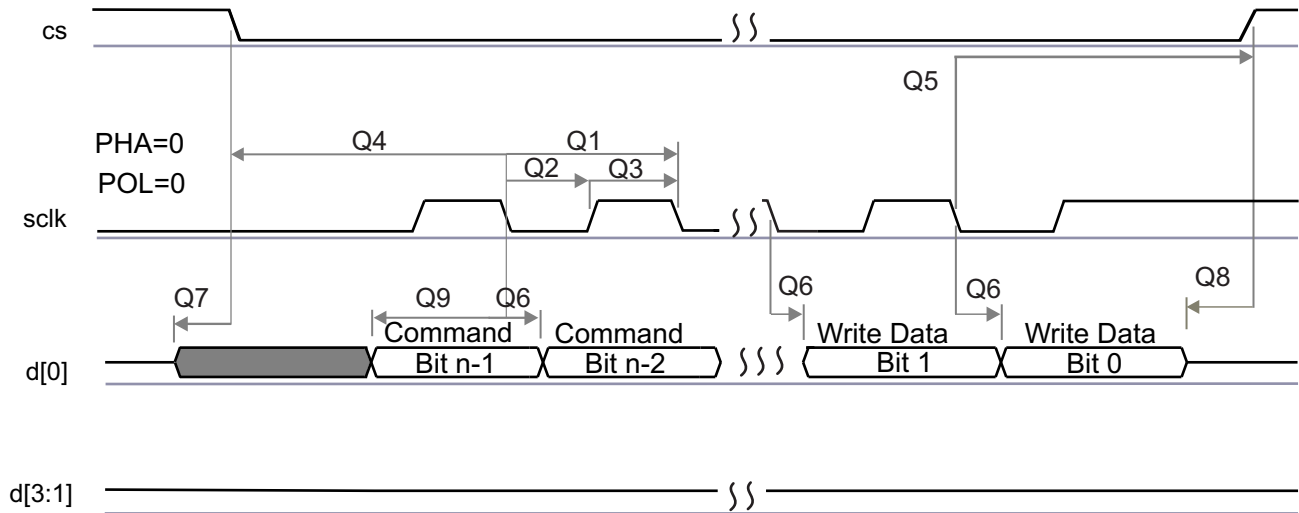
(2) Clock Modes 1 and 2 are not supported.

(3) The Device captures data on the falling clock edge in Clock Mode 0 and 3, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Modes 0 and 3.



SPRS91v\_QSPI\_03

图 5-47. QSPI Write (Clock Mode 3)



SPRS91v\_QSPI\_04

图 5-48. QSPI Write (Clock Mode 0)

注

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bitfield for each corresponding pad control register.

The pad control registers are presented in 表 4-29 and described in Device TRM, *Control Module* section.

注意

The IO timings provided in this section are only valid if signals within a single IOSET are used. The IOSETs are defined in 表 5-49.

In 表 5-49 are presented the specific groupings of signals (IOSET) for use with QSPI.

表 5-49. QSPI IOSETs

| SIGNALS     | IOSET1 |     | IOSET2 |     | IOSET3 |     | IOSET4 |     |
|-------------|--------|-----|--------|-----|--------|-----|--------|-----|
|             | BALL   | MUX | BALL   | MUX | BALL   | MUX | BALL   | MUX |
| qspi1_sclk  | C8     | 1   | C8     | 1   | C8     | 1   | C8     | 1   |
| qspi1_rtclk | C14    | 8   | B7     | 1   | F13    | 5   | D8     | 2   |
| qspi1_d0    | B9     | 1   | B9     | 1   | B9     | 1   | B9     | 1   |
| qspi1_d1    | F10    | 1   | F10    | 1   | F10    | 1   | F10    | 1   |
| qspi1_d2    | A9     | 1   | A9     | 1   | A9     | 1   | A9     | 1   |
| qspi1_d3    | D10    | 1   | D10    | 1   | D10    | 1   | D10    | 1   |
| qspi1_cs0   | E10    | 1   | E10    | 1   | E10    | 1   | E10    | 1   |
| qspi1_cs1   | F15    | 5   | F15    | 5   | F15    | 5   | F15    | 5   |

### 5.9.6.11 McASP

The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and inter-component digital audio interface transmission (DIT).

注

For more information, see the Serial Communication Interface section of the Device TRM.

表 5-50, 表 5-51, 表 5-52 和 图 5-49 present Timing Requirements for McASP1 to McASP3.

表 5-50. Timing Requirements for McASP1 <sup>(1)</sup>

| NO. | PARAMETER                   | DESCRIPTION                                   | MODE                                                                          | MIN                        | MAX | UNIT |
|-----|-----------------------------|-----------------------------------------------|-------------------------------------------------------------------------------|----------------------------|-----|------|
| 1   | $t_c(\text{AHCLKX})$        | Cycle time, AHCLKX                            |                                                                               | 20                         |     | ns   |
| 2   | $t_w(\text{AHCLKX})$        | Pulse duration, AHCLKX high or low            |                                                                               | 0.35P<br><sup>(2)</sup>    |     | ns   |
| 3   | $t_c(\text{ACLKR})$         | Cycle time, ACLKR/X                           | Any Other Conditions                                                          | 20                         |     | ns   |
|     |                             |                                               | ACLKX/AFSX (In Sync Mode), ACLKR/AFSR (In Async Mode), and AXR are all inputs | 15.258                     |     | ns   |
| 4   | $t_w(\text{ACLKR})$         | Pulse duration, ACLKR/X high or low           | Any Other Conditions                                                          | 0.5R - 3<br><sup>(3)</sup> |     | ns   |
|     |                             |                                               | ACLKX/AFSX (In Sync Mode), ACLKR/AFSR (In Async Mode), and AXR are all inputs | 0.38R<br><sup>(3)</sup>    |     | ns   |
| 5   | $t_{su}(\text{AFSRX-ACLK})$ | Setup time, AFSR/X input valid before ACLKR/X | ACLKR/X int                                                                   | 18.5                       |     | ns   |
|     |                             |                                               | ACLKR/X ext in<br>ACLKR/X ext out                                             | 3                          |     | ns   |
| 6   | $t_h(\text{ACLK-AFSRX})$    | Hold time, AFSR/X input valid after ACLKR/X   | ACLKR/X int                                                                   | 0.5                        |     | ns   |
|     |                             |                                               | ACLKR/X ext in<br>ACLKR/X ext out                                             | 0.4                        |     | ns   |
| 7   | $t_{su}(\text{AXR-ACLK})$   | Setup time, AXR input valid before ACLKR/X    | ACLKR/X int                                                                   | 18.5                       |     | ns   |
|     |                             |                                               | ACLKR/X ext in<br>ACLKR/X ext out                                             | 3                          |     | ns   |
| 8   | $t_h(\text{ACLK-AXR})$      | Hold time, AXR input valid after ACLKR/X      | ACLKR/X int                                                                   | 0.5                        |     | ns   |
|     |                             |                                               | ACLKR/X ext in<br>ACLKR/X ext out                                             | 0.4                        |     | ns   |

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1  
 ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0  
 ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1  
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1  
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0  
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.

表 5-51. Timing Requirements for McASP2 <sup>(1)</sup>

| NO. | PARAMETER            | DESCRIPTION                        | MODE                                                                                          | MIN                     | MAX | UNIT |
|-----|----------------------|------------------------------------|-----------------------------------------------------------------------------------------------|-------------------------|-----|------|
| 1   | $t_c(\text{AHCLKX})$ | Cycle time, AHCLKX                 |                                                                                               | 20                      |     | ns   |
| 2   | $t_w(\text{AHCLKX})$ | Pulse duration, AHCLKX high or low |                                                                                               | 0.35P<br><sup>(2)</sup> |     | ns   |
| 3   | $t_c(\text{ACLKR})$  | Cycle time, ACLKR/X                | Any Other Conditions                                                                          | 20                      |     | ns   |
|     |                      |                                    | IOSET1 only,<br>ACLKX/AFSX (In Sync Mode), ACLKR/AFSR (In Async Mode), and AXR are all inputs | 15.258                  |     | ns   |

**表 5-51. Timing Requirements for McASP2 <sup>(1)</sup> (continued)**

| NO. | PARAMETER            | DESCRIPTION                                   | MODE                                                                                       | MIN                     | MAX | UNIT |
|-----|----------------------|-----------------------------------------------|--------------------------------------------------------------------------------------------|-------------------------|-----|------|
| 4   | $t_{w(ACLKR)}$       | Pulse duration, ACLKR/X high or low           | Any Other Conditions                                                                       | 0.5R - 3 <sup>(3)</sup> |     | ns   |
|     |                      |                                               | IOSET1 only, ACLKX/AFSX (In Sync Mode), ACLKR/AFSR (In Async Mode), and AXR are all inputs | 0.38R <sup>(3)</sup>    |     | ns   |
| 5   | $t_{su}(AFSRX-ACLK)$ | Setup time, AFSR/X input valid before ACLKR/X | ACLKR/X int                                                                                | 18.5                    |     | ns   |
|     |                      |                                               | IOSET1 (vout1_*): ACLKR/X ext in<br>IOSET1 (vout1_*): ACLKR/X ext out                      | 4                       |     | ns   |
|     |                      |                                               | IOSET2 (gpmc_*): ACLKR/X ext in<br>IOSET2 (gpmc_*): ACLKR/X ext out                        | 3                       |     | ns   |
| 6   | $t_h(ACLK-AFSRX)$    | Hold time, AFSR/X input valid after ACLKR/X   | ACLKR/X int                                                                                | 0.5                     |     | ns   |
|     |                      |                                               | ACLKR/X ext in<br>ACLKR/X ext out                                                          | 0.4                     |     | ns   |
| 7   | $t_{su}(AXR-ACLK)$   | Setup time, AXR input valid before ACLKR/X    | ACLKR/X int                                                                                | 18.5                    |     | ns   |
|     |                      |                                               | IOSET1 (vout1_*): ACLKR/X ext in<br>IOSET1 (vout1_*): ACLKR/X ext out                      | 12                      |     | ns   |
|     |                      |                                               | IOSET2 (gpmc_*): ACLKR/X ext in<br>IOSET2 (gpmc_*): ACLKR/X ext out                        | 3                       |     | ns   |
| 8   | $t_h(ACLK-AXR)$      | Hold time, AXR input valid after ACLKR/X      | ACLKR/X int                                                                                | 0.5                     |     | ns   |
|     |                      |                                               | ACLKR/X ext in<br>ACLKR/X ext out                                                          | 0.4                     |     | ns   |

- (1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1  
 ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0  
 ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1  
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1  
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0  
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.

**表 5-52. Timing Requirements for McASP3 <sup>(1)</sup>**

| NO. | PARAMETER            | DESCRIPTION                                   | MODE                              | MIN      | MAX | UNIT |
|-----|----------------------|-----------------------------------------------|-----------------------------------|----------|-----|------|
| 1   | $t_c(AHCLKX)$        | Cycle time, AHCLKX                            |                                   | 20       |     | ns   |
| 2   | $t_w(AHCLKX)$        | Pulse duration, AHCLKX high or low            |                                   | 0.35P    |     | ns   |
| 3   | $t_c(ACLKR)$         | Cycle time, ACLKR/X                           |                                   | 20       |     | ns   |
| 4   | $t_w(ACLKR)$         | Pulse duration, ACLKR/X high or low           |                                   | 0.5R - 3 |     | ns   |
| 5   | $t_{su}(AFSRX-ACLK)$ | Setup time, AFSR/X input valid before ACLKR/X | ACLKR/X int                       | 18.2     |     | ns   |
|     |                      |                                               | ACLKR/X ext in<br>ACLKR/X ext out | 4        |     | ns   |
| 6   | $t_h(ACLK-AFSRX)$    | Hold time, AFSR/X input valid after ACLKR/X   | ACLKR/X int                       | 0.5      |     | ns   |
|     |                      |                                               | ACLKR/X ext in<br>ACLKR/X ext out | 0.4      |     | ns   |
|     | $t_{su}(AXR-ACLK)$   | Setup time, AXR input valid before ACLKX      | ACLKX int (ASYNC=0)               | 18.2     |     | ns   |
|     |                      |                                               | ACLKR/X ext in<br>ACLKR/X ext out | 12       |     | ns   |

表 5-52. Timing Requirements for McASP3 <sup>(1)</sup> (continued)

| NO. | PARAMETER         | DESCRIPTION                            | MODE                              | MIN | MAX | UNIT |
|-----|-------------------|----------------------------------------|-----------------------------------|-----|-----|------|
| 8   | $t_{h(ACLK-AXR)}$ | Hold time, AXR input valid after ACLKX | ACLKX int (ASYNCR=0)              | 0.5 |     | ns   |
|     |                   |                                        | ACLKR/X ext in<br>ACLKR/X ext out | 0.5 |     | ns   |

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1 (NOT SUPPORTED)

ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0

ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1

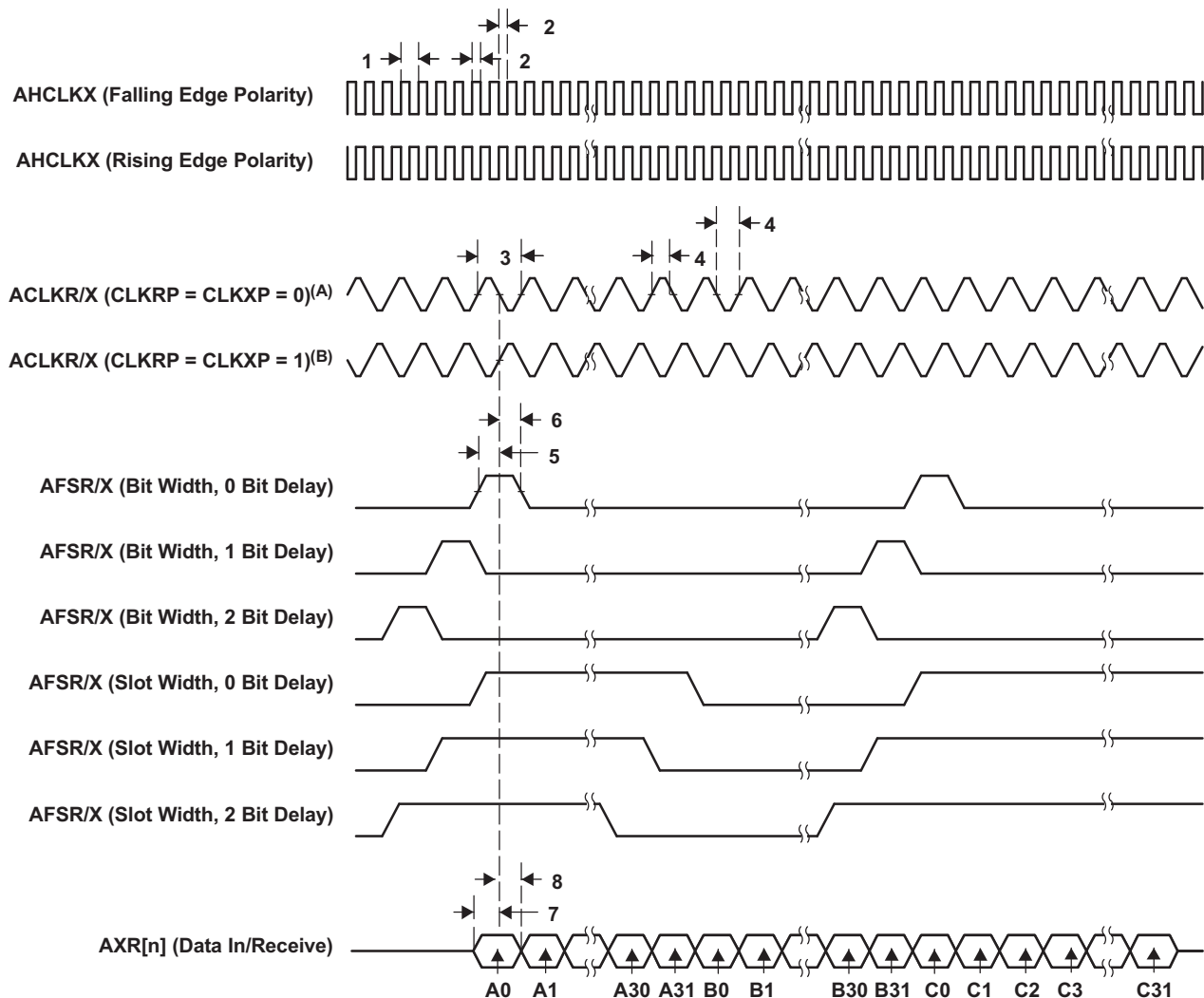
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1

ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0

ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.



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- A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).
- B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

图 5-49. McASP Input Timing

表 5-53, 表 5-54, 表 5-55 和 图 5-50 present Switching Characteristics Over Recommended Operating Conditions for McASP1 to McASP3.

**表 5-53. Switching Characteristics Over Recommended Operating Conditions for McASP1 <sup>(1)</sup>**

| NO. | PARAMETER         | DESCRIPTION                                              | MODE                              | MIN                       | MAX  | UNIT |
|-----|-------------------|----------------------------------------------------------|-----------------------------------|---------------------------|------|------|
| 9   | $t_{c(AHCLKX)}$   | Cycle time, AHCLKX                                       |                                   | 20                        |      | ns   |
| 10  | $t_{w(AHCLKX)}$   | Pulse duration, AHCLKX high or low                       |                                   | 0.5P - 2.5 <sup>(2)</sup> |      | ns   |
| 11  | $t_{c(ACLKR)}$    | Cycle time, ACLKR/X                                      |                                   | 20                        |      | ns   |
| 12  | $t_{w(ACLKR)}$    | Pulse duration, ACLKR/X high or low                      |                                   | 0.5P - 2.5 <sup>(3)</sup> |      | ns   |
| 13  | $t_d(ACLK-AFSXR)$ | Delay time, ACLKR/X transmit edge to AFSX/R output valid | ACLKR/X int                       | 0                         | 6    | ns   |
|     |                   |                                                          | ACLKR/X ext in<br>ACLKR/X ext out | 2                         | 22.2 | ns   |
| 14  | $t_d(ACLK-AXR)$   | Delay time, ACLKR/X transmit edge to AXR output valid    | ACLKR/X int                       | 0                         | 6    | ns   |
|     |                   |                                                          | ACLKR/X ext in<br>ACLKR/X ext out | 2                         | 22.2 | ns   |

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1

ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0

ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1

ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1

ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0

ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.

**表 5-54. Switching Characteristics Over Recommended Operating Conditions for McASP2 <sup>(1)</sup>**

| NO. | PARAMETER         | DESCRIPTION                                              | MODE                              | MIN                       | MAX  | UNIT |
|-----|-------------------|----------------------------------------------------------|-----------------------------------|---------------------------|------|------|
| 9   | $t_{c(AHCLKX)}$   | Cycle time, AHCLKX                                       |                                   | 20                        |      | ns   |
| 10  | $t_{w(AHCLKX)}$   | Pulse duration, AHCLKX high or low                       |                                   | 0.5P - 2.5 <sup>(2)</sup> |      | ns   |
| 11  | $t_{c(ACLKR)}$    | Cycle time, ACLKR/X                                      |                                   | 20                        |      | ns   |
| 12  | $t_{w(ACLKR)}$    | Pulse duration, ACLKR/X high or low                      |                                   | 0.5P - 2.5 <sup>(3)</sup> |      | ns   |
| 13  | $t_d(ACLK-AFSXR)$ | Delay time, ACLKR/X transmit edge to AFSX/R output valid | ACLKR/X int                       | 0                         | 6    | ns   |
|     |                   |                                                          | ACLKR/X ext in<br>ACLKR/X ext out | 2                         | 22.2 | ns   |
| 14  | $t_d(ACLK-AXR)$   | Delay time, ACLKR/X transmit edge to AXR output valid    | ACLKR/X int                       | 0                         | 6    | ns   |
|     |                   |                                                          | ACLKR/X ext in<br>ACLKR/X ext out | 2                         | 22.2 | ns   |

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1

ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0

ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1

ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1

ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0

ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.

**表 5-55. Switching Characteristics Over Recommended Operating Conditions for McASP3 <sup>(1)</sup>**

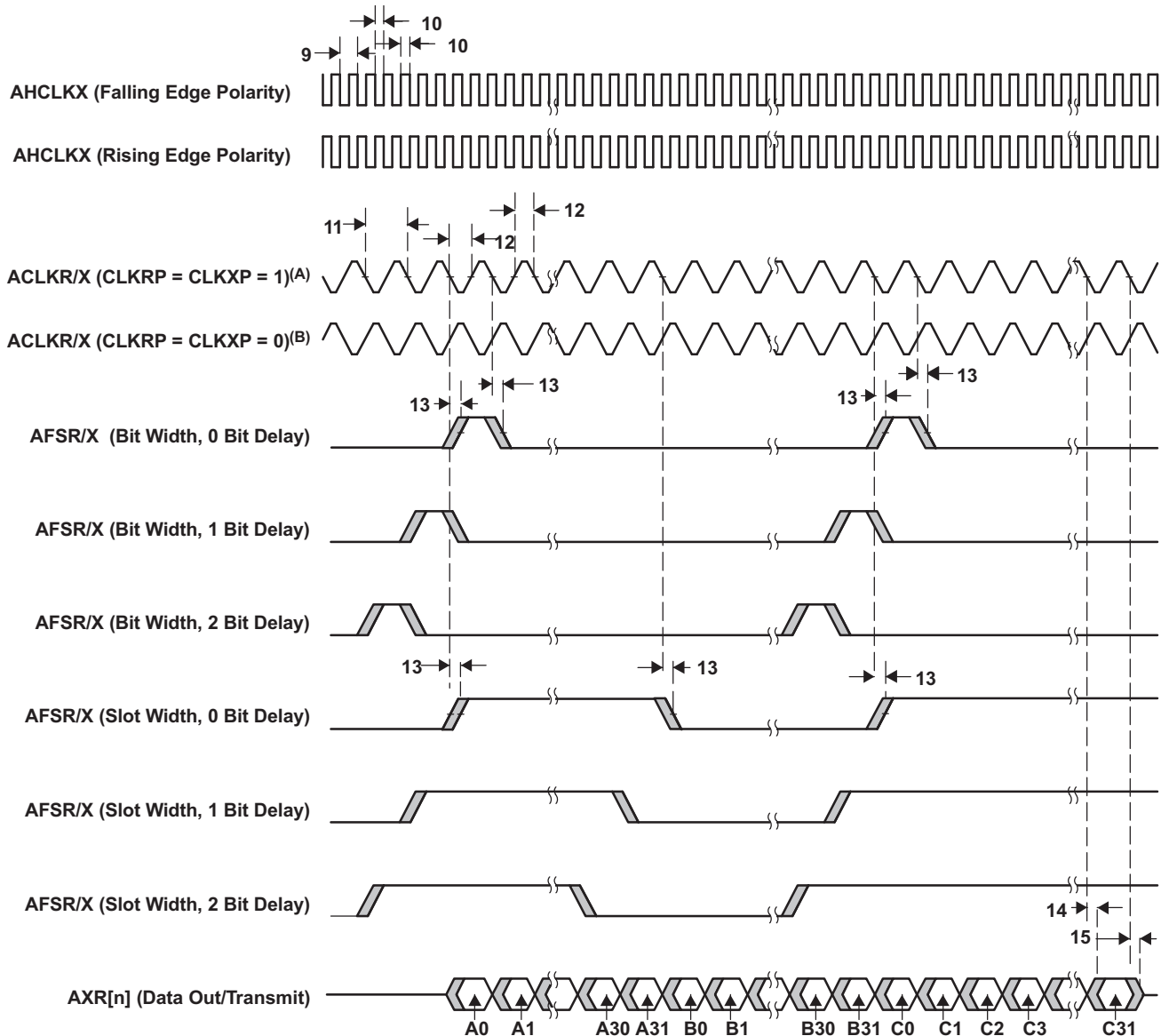
| NO. | PARAMETER       | DESCRIPTION                        | MODE | MIN        | MAX | UNIT |
|-----|-----------------|------------------------------------|------|------------|-----|------|
| 9   | $t_{c(AHCLKX)}$ | Cycle time, AHCLKX                 |      | 20         |     | ns   |
| 10  | $t_{w(AHCLKX)}$ | Pulse duration, AHCLKX high or low |      | 0.5P - 2.5 |     | ns   |
| 11  | $t_{c(ACLKR)}$  | Cycle time, ACLKR/X                |      | 20         |     | ns   |

表 5-55. Switching Characteristics Over Recommended Operating Conditions for McASP3 <sup>(1)</sup> (continued)

| NO. | PARAMETER         | DESCRIPTION                                              | MODE                              | MIN        | MAX  | UNIT |
|-----|-------------------|----------------------------------------------------------|-----------------------------------|------------|------|------|
| 12  | $t_{w(ACLKR)}$    | Pulse duration, ACLKR/X high or low                      |                                   | 0.5P - 2.5 |      | ns   |
| 13  | $t_d(ACLK-AFSXR)$ | Delay time, ACLKR/X transmit edge to AFSX/R output valid | ACLKR/X int                       | 0          | 6    | ns   |
|     |                   |                                                          | ACLKR/X ext in<br>ACLKR/X ext out | 2          | 23.1 | ns   |
| 14  | $t_d(ACLK-AXR)$   | Delay time, ACLKR/X transmit edge to AXR output valid    | ACLKR/X int                       | 0          | 6    | ns   |
|     |                   |                                                          | ACLKR/X ext in<br>ACLKR/X ext out | 2          | 23.1 | ns   |

- (1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1  
 ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0  
 ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1  
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1  
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0  
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

- (2) P = AHCLKX period in ns.  
 (3) R = ACLKR/X period in ns.



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- For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).
- For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

**图 5-50. McASP Output Timing**

**注**

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bitfield for each corresponding pad control register.

The pad control registers are presented 表 4-29 and described in Device TRM, *Control Module* section.

**注意**

The IO timings provided in this section are only valid if signals within a single IOSET are used. The IOSETs are defined in 表 5-56.

In 表 5-56 and 表 5-57 are presented the specific groupings of signals (IOSET) for use with McASP1 and McASP2.

**表 5-56. McASP1 IOSETs**

| SIGNALS      | IOSET1 |     | IOSET2 |     | IOSET3 |     |
|--------------|--------|-----|--------|-----|--------|-----|
|              | BALL   | MUX | BALL   | MUX | BALL   | MUX |
| mcasp1_aclkx | U17    | 1   | U17    | 1   | U17    | 1   |
| mcasp1_fsx   | W17    | 1   | W17    | 1   | W17    | 1   |
| mcasp1_aclkr | AA17   | 1   |        |     |        |     |
| mcasp1_fsr   | U16    | 1   |        |     |        |     |
| mcasp1_axr0  | W16    | 1   | W16    | 1   | W16    | 1   |
| mcasp1_axr1  | V16    | 1   | V16    | 1   | V16    | 1   |
| mcasp1_axr2  | U15    | 1   |        |     |        |     |
| mcasp1_axr3  | V15    | 1   |        |     |        |     |
| mcasp1_axr4  | Y15    | 1   |        |     |        |     |
| mcasp1_axr5  | W15    | 1   |        |     |        |     |
| mcasp1_axr6  | AA15   | 1   |        |     |        |     |
| mcasp1_axr7  | AB15   | 1   |        |     |        |     |
| mcasp1_axr8  | AA14   | 1   | AA14   | 1   | U15    | 4   |
| mcasp1_axr9  | AB14   | 1   | AB14   | 1   | V15    | 4   |
| mcasp1_axr10 |        |     | U13    | 1   | Y15    | 4   |
| mcasp1_axr11 |        |     | V13    | 1   | W15    | 4   |
| mcasp1_axr12 |        |     | Y13    | 1   | AA15   | 4   |
| mcasp1_axr13 |        |     | W13    | 1   | AB15   | 4   |
| mcasp1_axr14 |        |     | U11    | 1   | U7     | 4   |
| mcasp1_axr15 |        |     | V11    | 1   | V7     | 4   |

**表 5-57. McASP2 IOSETs**

| SIGNALS       | IOSET1 |                    | IOSET2 |                    |
|---------------|--------|--------------------|--------|--------------------|
|               | BALL   | MUX <sup>(1)</sup> | BALL   | MUX <sup>(1)</sup> |
| mcasp2_ahclkx | Y13    | 15                 | C6     | 15                 |
| mcasp2_aclkx  | U11    | 15                 | F7     | 15                 |
| mcasp2_fsx    | V11    | 15                 | E7     | 15                 |
| mcasp2_aclkr  | W13    | 15                 | B6     | 15                 |
| mcasp2_fsr    | W11    | 15                 | A5     | 15                 |
| mcasp2_axr0   | V9     | 15                 | D6     | 15                 |
| mcasp2_axr1   | W9     | 15                 | C5     | 15                 |
| mcasp2_axr2   | U8     | 15                 | B5     | 15                 |
| mcasp2_axr3   | W8     | 15                 | D7     | 15                 |
| mcasp2_axr4   | U7     | 15                 | B4     | 15                 |
| mcasp2_axr5   | V7     | 15                 | A4     | 15                 |

- (1) All McASP2 signals are virtual functions that present alternate multiplexing options. These virtual functions are controlled via CTRL\_CORE\_SMA\_SW\_\* registers. For more information on how to use these options, please refer to Device TRM, Chapter Control Module, Section Pad Configuration Registers.

## 5.9.6.12 DCAN and MCAN

### 5.9.6.12.1 DCAN

The device provides one DCAN interface for supporting distributed realtime control with a high level of security.

The DCAN interface implement the following features:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 MBit/s
- 64 message objects
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Suspend mode for debug support
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Message RAM single error correction and double error detection (SECDED) mechanism
- Direct access to Message RAM during test mode
- Support for two interrupt lines: Level 0 and Level 1, plus separate ECC interrupt line
- Local power down and wakeup support
- Automatic message RAM initialization
- Support for DMA access

### 5.9.6.12.2 MCAN

The device supports one MCAN module connecting to the CAN network through external (for the device) transceiver for connection to the physical layer. The MCAN module supports up to 5 Mbit/s data rate and is compliant to ISO 11898-1:2015.

The MCAN module implements the following features:

- Conforms with ISO 11898-1:2015
- Full CAN FD support (up to 64 data bytes)
- AUTOSAR and SAE J1939 support
- Up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, up to 32 elements
- Configurable Transmit Queue, up to 32 elements
- Configurable Transmit Event FIFO, up to 32 elements
- Up to 64 dedicated Receive Buffers
- Two configurable Receive FIFOs, up to 64 elements each
- Up to 128 filter elements
- Internal Loopback mode for self-test
- Maskable interrupts, two interrupt lines
- Two clock domains (CAN clock/Host clock)
- Parity/ECC support - Message RAM single error correction and double error detection (SECDED) mechanism
- Local power-down and wakeup support
- Timestamp Counter

注

For more information, see the Serial Communication Interfaces / DCAN and MCAN sections of the Device TRM.

注

Refer to the CAN Specification for calculations necessary to validate timing compliance. Jitter tolerance calculations must be performed to validate the implementation.

表 5-58 and 表 5-59 present Timing and Switching characteristics for DCAN and MCAN Interface.

**表 5-58. Timing Requirements for CAN Receive**

| NO. | PARAMETER               | DESCRIPTION                                      | MIN | NOM | MAX | UNIT |
|-----|-------------------------|--------------------------------------------------|-----|-----|-----|------|
|     | f(baud)                 | Maximum programmable baud rate                   |     |     | 1   | Mbps |
| -   | t <sub>d</sub> (CANnRX) | Delay time, CANnRX pin to receive shift register |     |     | 10  | ns   |

**表 5-59. Switching Characteristics Over Recommended Operating Conditions for CAN Transmit**

| NO. | PARAMETER               | DESCRIPTION                                                      | MIN | MAX | UNIT |
|-----|-------------------------|------------------------------------------------------------------|-----|-----|------|
|     | f(baud)                 | Maximum programmable baud rate                                   |     | 1   | Mbps |
| -   | t <sub>d</sub> (CANnTX) | Delay time, Transmit shift register to CANnTX pin <sup>(1)</sup> |     | 10  | ns   |

(1) These values do not include rise/fall times of the output buffer.

注意

The IO timings provided in this section are only valid if signals within a single IOSET are used. The IOSETs are defined in 表 5-60.

In 表 5-60 are presented the specific groupings of signals (IOSET) for use with DCAN and MCAN.

**表 5-60. DCAN and MCAN IOSETs**

| SIGNALS      | IOSET1 |     | IOSET2 |     | IOSET3 |     | IOSET4 |     |
|--------------|--------|-----|--------|-----|--------|-----|--------|-----|
|              | BALL   | MUX | BALL   | MUX | BALL   | MUX | BALL   | MUX |
| <b>DCAN1</b> |        |     |        |     |        |     |        |     |
| dcan1_tx     | N5     | 0   | D14    | 12  | F14    | 12  |        |     |
| dcan1_rx     | N6     | 0   | D15    | 12  | C14    | 12  |        |     |
| <b>MCAN</b>  |        |     |        |     |        |     |        |     |
| mcan_tx      |        |     | W7     | 0   | F13    | 12  | F15    | 12  |
| mcan_rx      |        |     | W6     | 0   | E14    | 12  | F16    | 12  |

### 5.9.6.13 GMAC\_SW

The two-port gigabit ethernet switch subsystem (GMAC\_SW) provides ethernet packet communication and can be configured as an ethernet switch. It provides Reduced Gigabit Media Independent Interface (RGMII), and the Management Data Input/Output (MDIO) for physical layer device (PHY) management.

注

For more information, see the Gigabit Ethernet Switch (GMAC\_SW) section of the Device TRM.

**注**

The Gigabit, Reduced and Media Independent Interface n (n = 0 to 1) are also referred to as RGMII<sub>n</sub>

### 5.9.6.13.1 GMAC MDIO Interface Timings

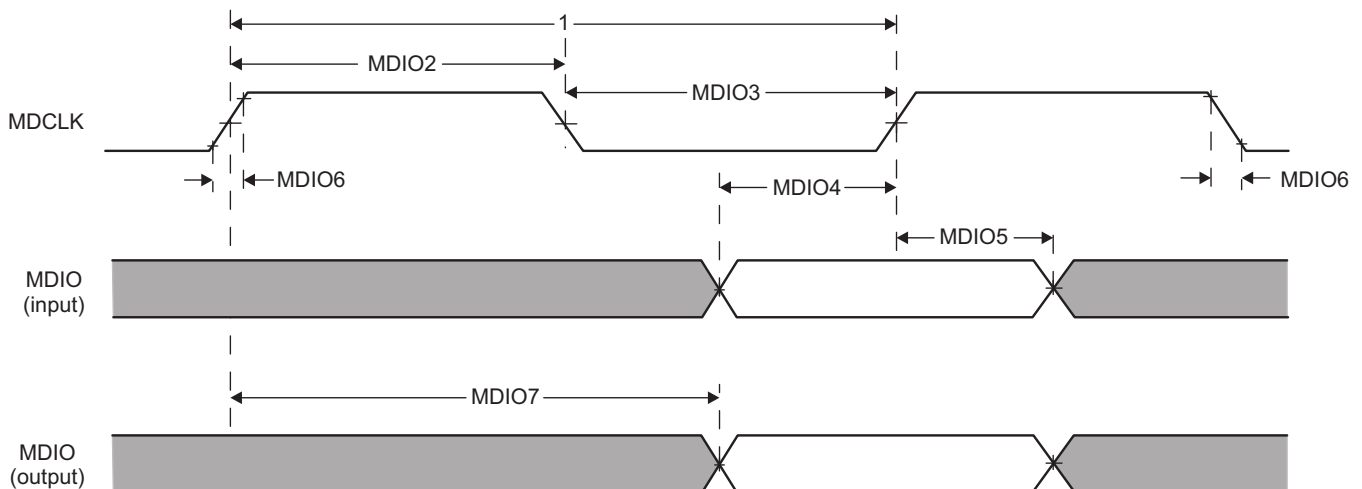
表 5-61, 表 5-62 和 图 5-51 present Timing Requirements for MDIO.

**表 5-61. Timing Requirements for MDIO Input**

| No | PARAMETER                 | DESCRIPTION                            | MIN | MAX | UNIT |
|----|---------------------------|----------------------------------------|-----|-----|------|
| 1  | $t_c(\text{MDC})$         | Cycle time, MDC                        | 400 |     | ns   |
| 2  | $t_w(\text{MDCH})$        | Pulse Duration, MDC High               | 160 |     | ns   |
| 3  | $t_w(\text{MDCL})$        | Pulse Duration, MDC Low                | 160 |     | ns   |
| 4  | $t_{su}(\text{MDIO-MDC})$ | Setup time, MDIO valid before MDC High | 90  |     | ns   |
| 5  | $t_h(\text{MDIO\_MDC})$   | Hold time, MDIO valid from MDC High    | 0   |     | ns   |

**表 5-62. Switching Characteristics Over Recommended Operating Conditions for MDIO Output**

| No | PARAMETER              | DESCRIPTION                        | MIN | MAX | UNIT |
|----|------------------------|------------------------------------|-----|-----|------|
| 6  | $t_t(\text{MDC})$      | Transition time, MDC               |     | 5   | ns   |
| 7  | $t_d(\text{MDC-MDIO})$ | Delay time, MDC High to MDIO valid | 10  | 390 | ns   |



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**图 5-51. GMAC MDIO diagrams**

### 5.9.6.13.2 GMAC RGMII Timings

表 5-63, 表 5-64 和 图 5-52 present timing requirements for receive RGMII operation.

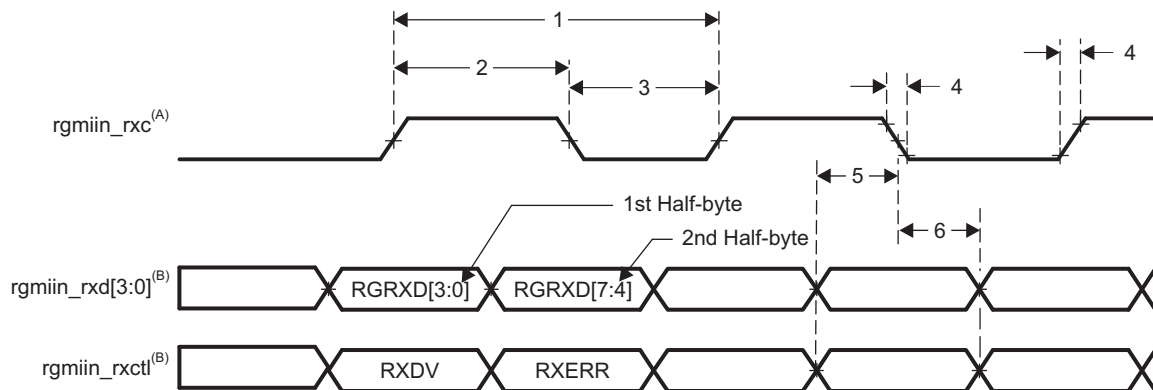
**表 5-63. Timing Requirements for rgmiin\_rxc - RGMII Operation**

| NO. | PARAMETER     | DESCRIPTION                     | SPEED     | MIN | MAX  | UNIT |
|-----|---------------|---------------------------------|-----------|-----|------|------|
| 1   | $t_{c(RXC)}$  | Cycle time, rgmiin_rxc          | 10 Mbps   | 360 | 440  | ns   |
|     |               |                                 | 100 Mbps  | 36  | 44   | ns   |
|     |               |                                 | 1000 Mbps | 7.2 | 8.8  | ns   |
| 2   | $t_{w(RXCH)}$ | Pulse duration, rgmiin_rxc high | 10 Mbps   | 160 | 240  | ns   |
|     |               |                                 | 100 Mbps  | 16  | 24   | ns   |
|     |               |                                 | 1000 Mbps | 3.6 | 4.4  | ns   |
| 3   | $t_{w(RXCL)}$ | Pulse duration, rgmiin_rxc low  | 10 Mbps   | 160 | 240  | ns   |
|     |               |                                 | 100 Mbps  | 16  | 24   | ns   |
|     |               |                                 | 1000 Mbps | 3.6 | 4.4  | ns   |
| 4   | $t_t(RXC)$    | Transition time, rgmiin_rxc     | 10 Mbps   |     | 0.75 | ns   |
|     |               |                                 | 100 Mbps  |     | 0.75 | ns   |
|     |               |                                 | 1000 Mbps |     | 0.75 | ns   |

**表 5-64. Timing Requirements for GMAC RGMII Input Receive for 10/100/1000 Mbps**

| NO. | PARAMETER          | DESCRIPTION                                                           | MIN  | MAX | UNIT |
|-----|--------------------|-----------------------------------------------------------------------|------|-----|------|
| 5   | $t_{su(RXD-RXCH)}$ | Setup time, receive selected signals valid before rgmiin_rxc high/low | 1.15 |     | ns   |
| 6   | $t_h(RXCH-RXD)$    | Hold time, receive selected signals valid after rgmiin_rxc high/low   | 1.15 |     | ns   |

- (1) For RGMII, receive selected signals include: rgmiin\_rxd[3:0] and rgmiin\_rxctl.
- (2) RGMII0 requires that the 4 data pins rgmiio\_rxd[3:0] and rgmiio\_rxctl have their board propagation delays matched within 50pS of rgmiio\_rxc.
- (3) RGMII1 requires that the 4 data pins rgmii1\_rxd[3:0] and rgmii1\_rxctl have their board propagation delays matched within 50pS of rgmii1\_rxc.



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- A. rgmiin\_rxc must be externally delayed relative to the data and control pins.
- B. Data and control information is received using both edges of the clocks. rgmiin\_rxd[3:0] carries data bits 3-0 on the rising edge of rgmiin\_rxc and data bits 7-4 on the falling edge of rgmiin\_rxc. Similarly, rgmiin\_rxctl carries RXDV on rising edge of rgmiin\_rxc and RXERR on falling edge of rgmiin\_rxc.

**图 5-52. GMAC Receive Interface Timing, RGMII operation**

表 5-65, 表 5-66 和 图 5-53 present switching characteristics for rgmiin\_txctl - RGMII Operation for 10/100/1000 Mbit/s

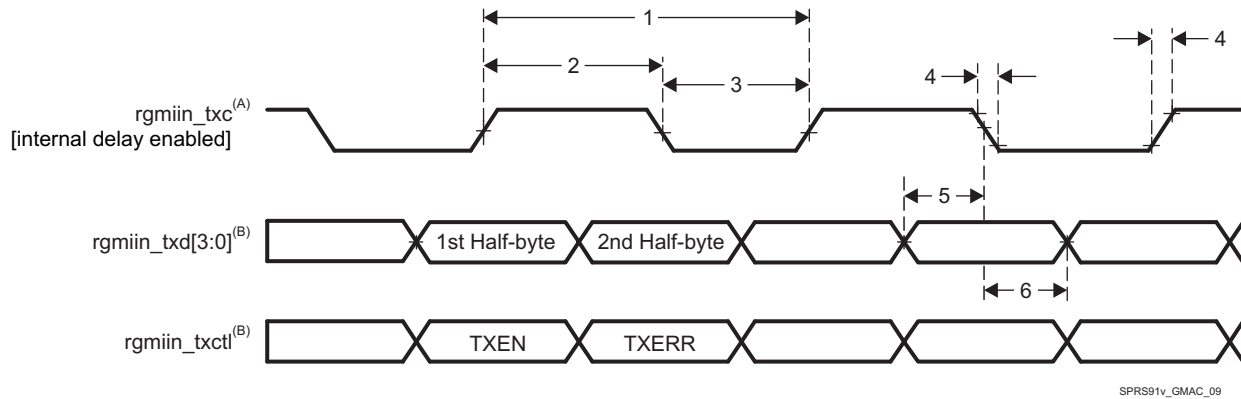
**表 5-65. Switching Characteristics Over Recommended Operating Conditions for rgmiin\_txctl - RGMIIIn  
Operation for 10/100/1000 Mbit/s**

| NO. | PARAMETER     | DESCRIPTION                     | SPEED     | MIN | MAX  | UNIT |
|-----|---------------|---------------------------------|-----------|-----|------|------|
| 1   | $t_{c(TXC)}$  | Cycle time, rgmiin_txc          | 10 Mbps   | 360 | 440  | ns   |
|     |               |                                 | 100 Mbps  | 36  | 44   | ns   |
|     |               |                                 | 1000 Mbps | 7.2 | 8.8  | ns   |
| 2   | $t_{w(TXCH)}$ | Pulse duration, rgmiin_txc high | 10 Mbps   | 160 | 240  | ns   |
|     |               |                                 | 100 Mbps  | 16  | 24   | ns   |
|     |               |                                 | 1000 Mbps | 3.6 | 4.4  | ns   |
| 3   | $t_{w(TXCL)}$ | Pulse duration, rgmiin_txc low  | 10 Mbps   | 160 | 240  | ns   |
|     |               |                                 | 100 Mbps  | 16  | 24   | ns   |
|     |               |                                 | 1000 Mbps | 3.6 | 4.4  | ns   |
| 4   | $t_t(TXC)$    | Transition time, rgmiin_txc     | 10 Mbps   |     | 0.75 | ns   |
|     |               |                                 | 100 Mbps  |     | 0.75 | ns   |
|     |               |                                 | 1000 Mbps |     | 0.75 | ns   |

**表 5-66. Switching Characteristics for GMAC RGMIIIn Output Transmit for 10/100/1000 Mbps <sup>(1)</sup>**

| NO. | PARAMETER          | DESCRIPTION                                                                 | MODE                                        | MIN | MAX | UNIT |
|-----|--------------------|-----------------------------------------------------------------------------|---------------------------------------------|-----|-----|------|
| 5   | $t_{osu(TXD-TXC)}$ | Output Setup time, transmit selected signals valid to rgmiin_txc high/low   | RGMII0, Internal Delay Enabled, 1000 Mbps   |     |     | ns   |
|     |                    |                                                                             | RGMII0, Internal Delay Enabled, 10/100 Mbps | 1.2 |     | ns   |
|     |                    |                                                                             | RGMII1, Internal Delay Enabled, 1000 Mbps   |     |     | ns   |
|     |                    |                                                                             | RGMII1, Internal Delay Enabled, 10/100 Mbps | 1.2 |     | ns   |
| 6   | $t_{oh(TXC-TXD)}$  | Output Hold time, transmit selected signals valid after rgmiin_txc high/low | RGMII0, Internal Delay Enabled, 1000 Mbps   |     |     | ns   |
|     |                    |                                                                             | RGMII0, Internal Delay Enabled, 10/100 Mbps | 1.2 |     | ns   |
|     |                    |                                                                             | RGMII1, Internal Delay Enabled, 1000 Mbps   |     |     | ns   |
|     |                    |                                                                             | RGMII1, Internal Delay Enabled, 10/100 Mbps | 1.2 |     | ns   |

- (1) For RGMII, transmit selected signals include: rgmiin\_txd[3:0] and rgmiin\_txctl.
- (2) RGMII0 1000Mbps operation is not supported.
- (3) RGMII1 1000Mbps operation is not supported.



- A. TxC is delayed internally before being driven to the rgmiin\_txc pin. This internal delay is always enabled.
- B. Data and control information is transmitted using both edges of the clocks. rgmiin\_txd[3:0] carries data bits 3-0 on the rising edge of rgmiin\_txc and data bits 7-4 on the falling edge of rgmiin\_txc. Similarly, rgmiin\_txctl carries TXEN on rising edge of rgmiin\_txc and TXERR of falling edge of rgmiin\_txc.

图 5-53. GMAC Transmit Interface Timing RGMII operation

#### 5.9.6.14 SDIO Controller

MMC interface is compliant with the SDIO3.0 standard v1.0, SD Part E1 and for generic SDIO devices, it supports the following applications:

- MMC 4-bit data, SD Default speed, SDR
- MMC 4-bit data, SD High speed, SDR
- MMC 4-bit data, UHS-I SDR12 (SD Standard v3.01), 4-bit data, SDR, half cycle
- MMC 4-bit data, UHS-I SDR25 (SD Standard v3.01), 4-bit data, SDR, half cycle

#### 注

For more information, see the SDIO Controller chapter of the Device TRM.

##### 5.9.6.14.1 MMC, SD Default Speed

图 5-54, 图 5-55, 表 5-67, and 表 5-68 present Timing requirements and Switching characteristics for MMC - SD and SDIO Default speed in receiver and transmitter mode.

表 5-67. Timing Requirements for MMC - Default Speed Mode

| NO. | PARAMETER           | DESCRIPTION                                                     | MIN   | MAX | UNIT |
|-----|---------------------|-----------------------------------------------------------------|-------|-----|------|
| DS5 | $t_{su(cmdV-clkH)}$ | Setup time, mmc_cmd valid before mmc_clk rising clock edge      | 5.11  |     | ns   |
| DS6 | $t_h(clkH-cmdV)$    | Hold time, mmc_cmd valid after mmc_clk rising clock edge        | 20.46 |     | ns   |
| DS7 | $t_{su(dV-clkH)}$   | Setup time, mmc_dat[i:0] valid before mmc_clk rising clock edge | 5.11  |     | ns   |
| DS8 | $t_h(clkH-dV)$      | Hold time, mmc_dat[i:0] valid after mmc_clk rising clock edge   | 20.46 |     | ns   |

(1) i in [i:0] = 3

表 5-68. Switching Characteristics for MMC - SD/SDIO Default Speed Mode

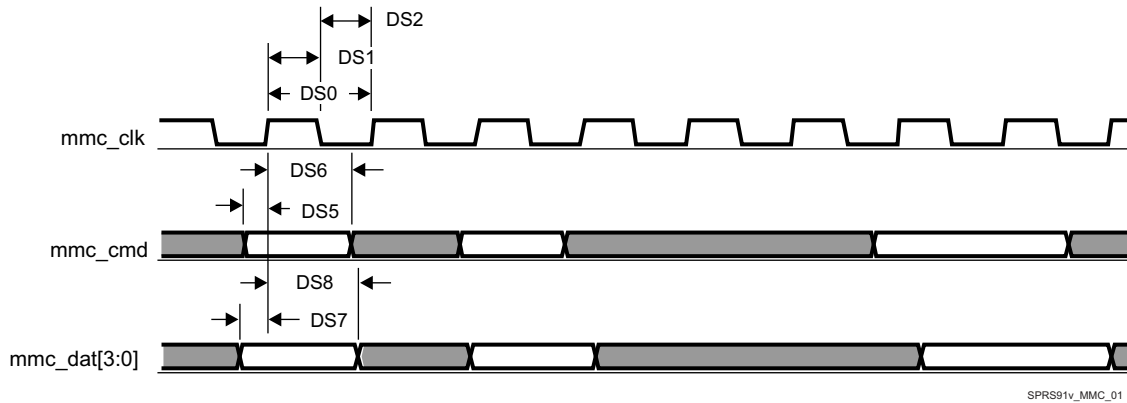
| NO. | PARAMETER   | DESCRIPTION                  | MIN         | MAX | UNIT |
|-----|-------------|------------------------------|-------------|-----|------|
| DS0 | fop(clk)    | Operating frequency, mmc_clk |             | 24  | MHz  |
| DS1 | $t_w(clkH)$ | Pulse duration, mmc_clk high | 0.5×P-0.270 |     | ns   |

**表 5-68. Switching Characteristics for MMC - SD/SDIO Default Speed Mode (continued)**

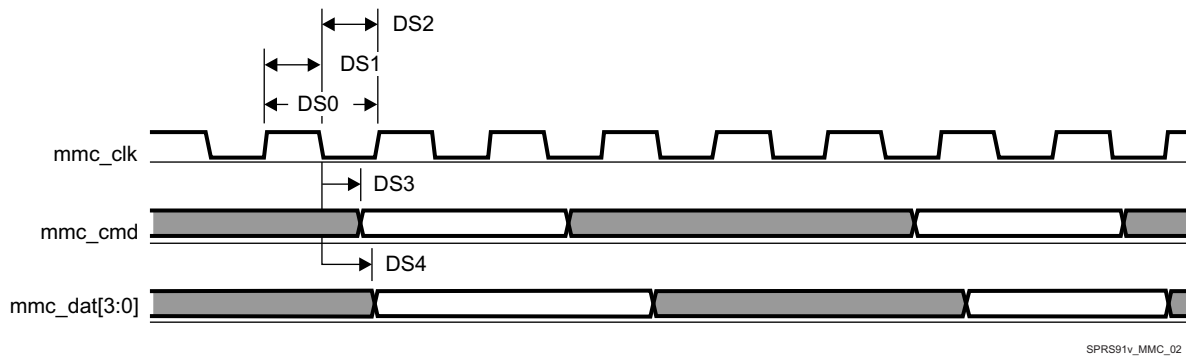
| NO. | PARAMETER                 | DESCRIPTION                                                       | MIN                    | MAX   | UNIT |
|-----|---------------------------|-------------------------------------------------------------------|------------------------|-------|------|
| DS2 | $t_{w(\text{clkL})}$      | Pulse duration, mmc_clk low                                       | $0.5 \times P - 0.270$ |       | ns   |
| DS3 | $t_{d(\text{clkL-cmdV})}$ | Delay time, mmc_clk falling clock edge to mmc_cmd transition      | -14.93                 | 14.93 | ns   |
| DS4 | $t_{d(\text{clkL-dV})}$   | Delay time, mmc_clk falling clock edge to mmc_dat[i:0] transition | -14.93                 | 14.93 | ns   |

(1) P = output mmc\_clk period in ns

(2) i in [i:0] = 3



**图 5-54. MMC/SD/SDIOj in - Default Speed - Receiver Mode**



**图 5-55. MMC/SD/SDIOj in - Default Speed - Transmitter Mode**

#### 5.9.6.14.2 MMC, SD High Speed

图 5-56, 图 5-57, 表 5-69, and 表 5-70 present Timing requirements and Switching characteristics for MMC - SD and SDIO High speed in receiver and transmitter mode.

**表 5-69. Timing Requirements for MMC - SD/SDIO High Speed Mode**

| NO. | PARAMETER                  | DESCRIPTION                                                     | MIN | MAX | UNIT |
|-----|----------------------------|-----------------------------------------------------------------|-----|-----|------|
| HS3 | $t_{su(\text{cmdV-clkH})}$ | Setup time, mmc_cmd valid before mmc_clk rising clock edge      | 5.3 |     | ns   |
| HS4 | $t_{h(\text{clkH-cmdV})}$  | Hold time, mmc_cmd valid after mmc_clk rising clock edge        | 2.6 |     | ns   |
| HS7 | $t_{su(\text{dV-clkH})}$   | Setup time, mmc_dat[i:0] valid before mmc_clk rising clock edge | 5.3 |     | ns   |
| HS8 | $t_{h(\text{clkH-dV})}$    | Hold time, mmc_dat[i:0] valid after mmc_clk rising clock edge   | 2.6 |     | ns   |

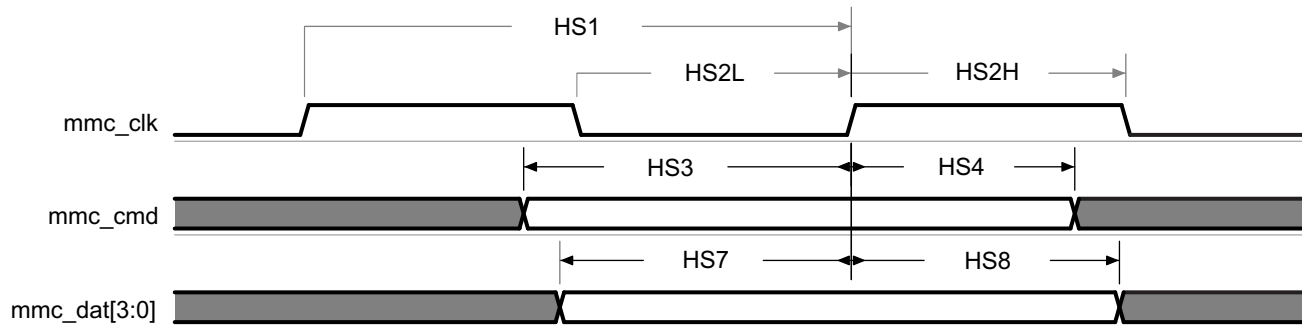
(1) i in [i:0] = 3

**表 5-70. Switching Characteristics for MMC - SD/SDIO High Speed Mode**

| NO.  | PARAMETER                  | DESCRIPTION                                                       | MIN         | MAX | UNIT |
|------|----------------------------|-------------------------------------------------------------------|-------------|-----|------|
| HS1  | fop(clk)                   | Operating frequency, mmc_clk                                      |             | 48  | MHz  |
| HS2H | t <sub>w</sub> (clkH)      | Pulse duration, mmc_clk high                                      | 0.5×P-0.270 |     | ns   |
| HS2L | t <sub>w</sub> (clkL)      | Pulse duration, mmc_clk low                                       | 0.5×P-0.270 |     | ns   |
| HS5  | t <sub>d</sub> (clkL-cmdV) | Delay time, mmc_clk falling clock edge to mmc_cmd transition      | -7.6        | 3.6 | ns   |
| HS6  | t <sub>d</sub> (clkL-dV)   | Delay time, mmc_clk falling clock edge to mmc_dat[i:0] transition | -7.6        | 3.6 | ns   |

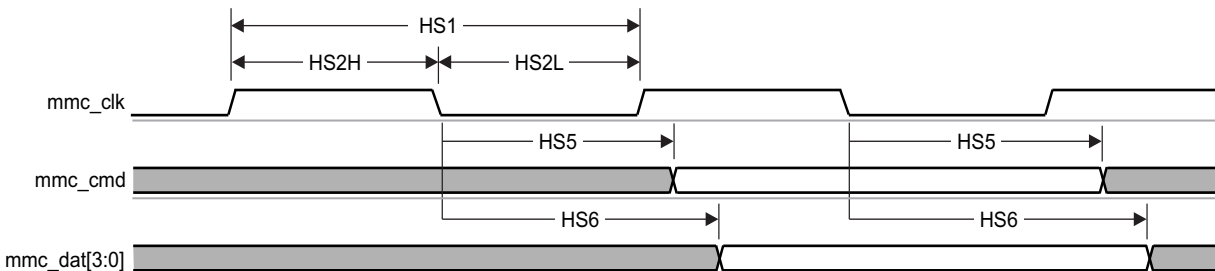
(1) P = output mmc\_clk period in ns

(2) i in [i:0] = 3



SPRS91v\_MMC\_03

**图 5-56. MMC/SD/SDIOj in - High Speed - Receiver Mode**



SPRS91v\_MMC\_04

**图 5-57. MMC/SD/SDIOj in - High Speed - Transmitter Mode**

#### 5.9.6.14.3 MMC, SD and SDIO SDR12 Mode

图 5-58, 图 5-59, 表 5-71, and 表 5-72 present Timing requirements and Switching characteristics for MMC - SD and SDIO SDR12 in receiver and transmitter mode.

**表 5-71. Timing Requirements for MMC - SDR12 Mode**

| NO.    | PARAMETER                   | DESCRIPTION                                                     | MIN   | MAX | UNIT |
|--------|-----------------------------|-----------------------------------------------------------------|-------|-----|------|
| SDR125 | t <sub>su</sub> (cmdV-clkH) | Setup time, mmc_cmd valid before mmc_clk rising clock edge      | 25.99 |     | ns   |
| SDR126 | t <sub>h</sub> (clkH-cmdV)  | Hold time, mmc_cmd valid after mmc_clk rising clock edge        | 1.6   |     | ns   |
| SDR127 | t <sub>su</sub> (dV-clkH)   | Setup time, mmc_dat[i:0] valid before mmc_clk rising clock edge | 25.99 |     | ns   |
| SDR128 | t <sub>h</sub> (clkH-dV)    | Hold time, mmc_dat[i:0] valid after mmc_clk rising clock edge   | 1.6   |     | ns   |

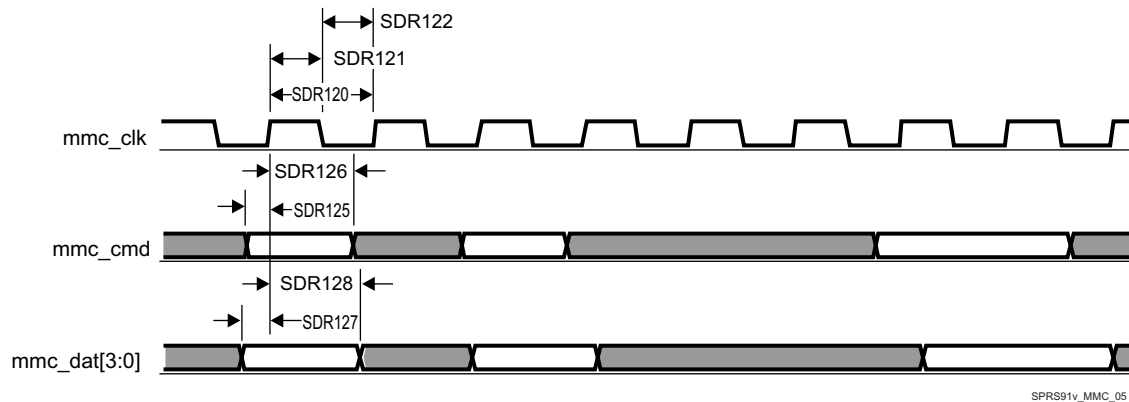
(1)  $i$  in  $[i:0] = 3$

**表 5-72. Switching Characteristics for MMC - SDR12 Mode**

| NO.    | PARAMETER                 | DESCRIPTION                                                       | MIN                    | MAX   | UNIT |
|--------|---------------------------|-------------------------------------------------------------------|------------------------|-------|------|
| SDR120 | fop(clk)                  | Operating frequency, mmc_clk                                      |                        | 24    | MHz  |
| SDR121 | $t_{w(\text{clkH})}$      | Pulse duration, mmc_clk high                                      | $0.5 \times P - 0.270$ |       | ns   |
| SDR122 | $t_{w(\text{clkL})}$      | Pulse duration, mmc_clk low                                       | $0.5 \times P - 0.270$ |       | ns   |
| SDR123 | $t_{d(\text{clkL-cmdV})}$ | Delay time, mmc_clk falling clock edge to mmc_cmd transition      | -19.13                 | 16.93 | ns   |
| SDR124 | $t_{d(\text{clkL-dV})}$   | Delay time, mmc_clk falling clock edge to mmc_dat[i:0] transition | -19.13                 | 16.93 | ns   |

(1) P = output mmc\_clk period in ns

(2)  $i$  in  $[i:0] = 3$



SPRS91v\_MMC\_05

**图 5-58. MMC/SD/SDIOj in - SDR12 - Receiver Mode**



SPRS91v\_MMC\_06

**图 5-59. MMC/SD/SDIOj in - SDR12 - Transmitter Mode**

#### 5.9.6.14.4 MMC, SD SDR25 Mode

图 5-60, 图 5-61, 表 5-73, and 表 5-74 present Timing requirements and Switching characteristics for MMC - SD and SDIO SDR25 in receiver and transmitter mode.

**表 5-73. Timing Requirements for MMC - SDR25 Mode <sup>(1)</sup>**

| NO.    | PARAMETER                  | DESCRIPTION                                                     | MIN | MAX | UNIT |
|--------|----------------------------|-----------------------------------------------------------------|-----|-----|------|
| SDR253 | $t_{su(\text{cmdV-clkH})}$ | Setup time, mmc_cmd valid before mmc_clk rising clock edge      | 5.3 |     | ns   |
| SDR254 | $t_h(\text{clkH-cmdV})$    | Hold time, mmc_cmd valid after mmc_clk rising clock edge        | 1.6 |     | ns   |
| SDR257 | $t_{su(\text{dV-clkH})}$   | Setup time, mmc_dat[i:0] valid before mmc_clk rising clock edge | 5.3 |     | ns   |
| SDR258 | $t_h(\text{clkH-dV})$      | Hold time, mmc_dat[i:0] valid after mmc_clk rising clock edge   | 1.6 |     | ns   |

(1) i in [i:0] = 3

表 5-74. Switching Characteristics for MMC - SDR25 Mode <sup>(2)</sup>

| NO.     | PARAMETER                  | DESCRIPTION                                                       | MIN         | MAX | UNIT |
|---------|----------------------------|-------------------------------------------------------------------|-------------|-----|------|
| SDR251  | fop(clk)                   | Operating frequency, mmc_clk                                      |             | 48  | MHz  |
| SDR252H | t <sub>w</sub> (clkH)      | Pulse duration, mmc_clk high                                      | 0.5×P-0.270 |     | ns   |
| SDR252L | t <sub>w</sub> (clkL)      | Pulse duration, mmc_clk low                                       | 0.5×P-0.270 |     | ns   |
| SDR255  | t <sub>d</sub> (clkL-cmdV) | Delay time, mmc_clk falling clock edge to mmc_cmd transition      | -8.8        | 6.6 | ns   |
| SDR256  | t <sub>d</sub> (clkL-dV)   | Delay time, mmc_clk falling clock edge to mmc_dat[i:0] transition | -8.8        | 6.6 | ns   |

(1) P = output mmc\_clk period in ns

(2) i in [i:0] = 3

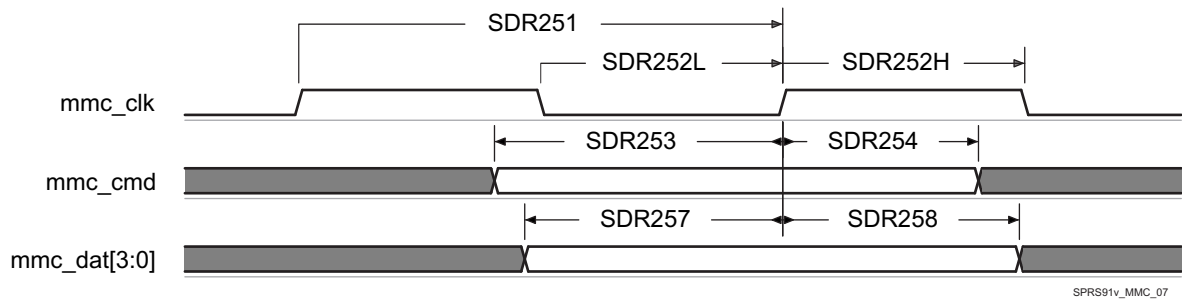


图 5-60. MMC/SD/SDIOj in - SDR25 - Receiver Mode

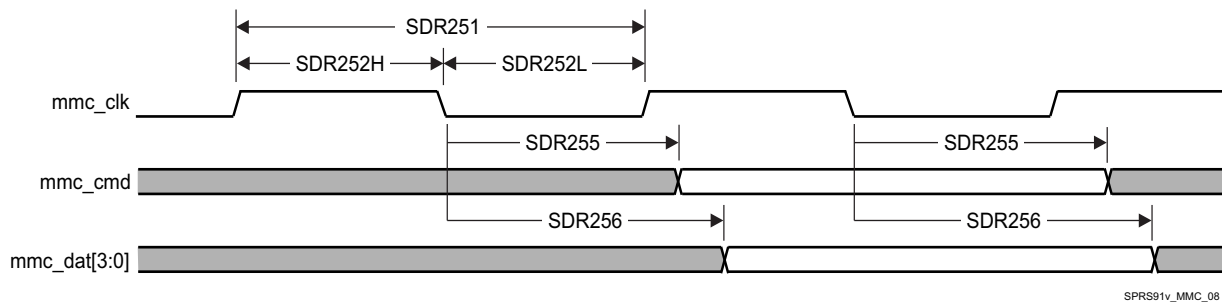


图 5-61. MMC/SD/SDIOj in - SDR25 - Transmitter Mode

**注意**

The IO timings provided in this section are only valid if signals within a single IOSET are used. The IOSETs are defined in 表 5-75.

In 表 5-75 are presented the specific groupings of signals (IOSET) for use with MMC.

表 5-75. MMC IOSETs

| SIGNALS  | IOSET1 |     | IOSET2 |     | IOSET3 |     |
|----------|--------|-----|--------|-----|--------|-----|
|          | BALL   | MUX | BALL   | MUX | BALL   | MUX |
| mmc_clk  | C16    | 5   | W16    | 5   | B18    | 5   |
| mmc_cmd  | C17    | 5   | V16    | 5   | C18    | 5   |
| mmc_dat0 | E16    | 5   | U15    | 5   | A19    | 5   |
| mmc_dat1 | D16    | 5   | V15    | 5   | B20    | 5   |

**表 5-75. MMC IOSETs (continued)**

| SIGNALS  | IOSET1              |     | IOSET2              |     | IOSET3              |     |
|----------|---------------------|-----|---------------------|-----|---------------------|-----|
|          | BALL                | MUX | BALL                | MUX | BALL                | MUX |
| mmc_dat2 | <a href="#">E17</a> | 5   | <a href="#">Y15</a> | 5   | <a href="#">C20</a> | 5   |
| mmc_dat3 | <a href="#">F17</a> | 5   | <a href="#">W15</a> | 5   | <a href="#">A20</a> | 5   |

### 5.9.6.15 GPIO

The general-purpose interface combines four general-purpose input/output (GPIO) banks. Each GPIO module provides up to 32 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 126 pins.

These pins can be configured for the following applications:

- Data input (capture)/output (drive)
- Keyboard interface with a debounce cell
- Interrupt generation in active mode upon the detection of external events. Detected events are processed by two parallel independent interrupt-generation submodules to support biprocessor operations
- Wake-up request generation in idle mode upon the detection of external events

#### 注

For more information, see the General-Purpose Interface chapter of the Device TRM.

#### 注

The general-purpose input/output i (i = 1 to 4) bank is also referred to as GPIOi.

#### 注意

The IO timings provided in this section are only valid if signals within a single IOSET are used. The IOSETs are defined in [表 5-76](#).

In [表 5-76](#) are presented the specific groupings of signals (IOSET) for use with GPIO.

**表 5-76. GPIO2/3/4 IOSETs**

| SIGNALS      | IOSET1               |     | IOSET2               |     |
|--------------|----------------------|-----|----------------------|-----|
|              | BALL                 | MUX | BALL                 | MUX |
| <b>GPIO2</b> |                      |     |                      |     |
| gpio2_11     |                      |     | <a href="#">J17</a>  | 14  |
| gpio2_12     |                      |     | <a href="#">K22</a>  | 14  |
| gpio2_13     |                      |     | <a href="#">K21</a>  | 14  |
| gpio2_14     |                      |     | <a href="#">K18</a>  | 14  |
| gpio2_20     |                      |     | <a href="#">AB17</a> | 14  |
| gpio2_23     | <a href="#">AA17</a> | 14  | <a href="#">AA17</a> | 14  |
| gpio2_24     | <a href="#">U16</a>  | 14  | <a href="#">U16</a>  | 14  |
| gpio2_27     | <a href="#">U15</a>  | 14  |                      |     |
| gpio2_28     | <a href="#">V15</a>  | 14  |                      |     |
| gpio2_29     | <a href="#">Y15</a>  | 14  |                      |     |
| gpio2_30     | <a href="#">W15</a>  | 14  |                      |     |
| gpio2_31     | <a href="#">AA15</a> | 14  |                      |     |

表 5-76. GPIO2/3/4 IOSETs (continued)

| SIGNALS  | IOSET1 |     | IOSET2 |     |
|----------|--------|-----|--------|-----|
|          | BALL   | MUX | BALL   | MUX |
| GPIO3    |        |     |        |     |
| gpio3_0  | AB15   | 14  |        |     |
| gpio3_9  | U9     | 14  | U9     | 14  |
| gpio3_10 | W11    | 14  | W11    | 14  |
| gpio3_11 | V9     | 14  | V9     | 14  |
| gpio3_12 | W9     | 14  | W9     | 14  |
| gpio3_13 | U8     | 14  | U8     | 14  |
| gpio3_14 | W8     | 14  | W8     | 14  |
| gpio3_15 | U7     | 14  |        |     |
| gpio3_16 | V7     | 14  |        |     |
| GPIO4    |        |     |        |     |
| gpio4_4  |        |     | R5     | 14  |
| gpio4_6  |        |     | N4     | 14  |
| gpio4_7  |        |     | R7     | 14  |
| gpio4_8  |        |     | L2     | 14  |
| gpio4_9  |        |     | N5     | 14  |
| gpio4_10 |        |     | N6     | 14  |

### 5.9.6.16 ATL

The device contains one ATL module that can be used for asynchronous sample rate conversion of audio. The ATL calculates the error between two time bases, such as audio syncs, and optionally generates an averaged clock using cycle stealing via software.

#### 注

For more detailed information on the ATL peripheral, see the Audio Tracking Logic (ATL) chapter of the device TRM.

#### 5.9.6.16.1 ATL Electrical Data/Timing

表 5-77 和 图 5-62 present switching characteristics for ATL

表 5-77. Switching Characteristics Over Recommended Operating Conditions for ATL\_CLKOUTx

| NO. | PARAMETER           | DESCRIPTION                      | MIN                       | MAX | UNIT |
|-----|---------------------|----------------------------------|---------------------------|-----|------|
| 1   | $t_{c(ATLCLKOUT)}$  | Cycle time, ATL_CLKOUTx          | 20                        |     | ns   |
| 2   | $t_{w(ATLCLKOUTL)}$ | Pulse Duration, ATL_CLKOUTx low  | $0.45 \times P - M^{(1)}$ |     | ns   |
| 3   | $t_{w(ATLCLKOUTH)}$ | Pulse Duration, ATL_CLKOUTx high | $0.45 \times P - M^{(1)}$ |     | ns   |

(1) P = ATL\_CLKOUTx period.  
M = internal ATL PCLK period.

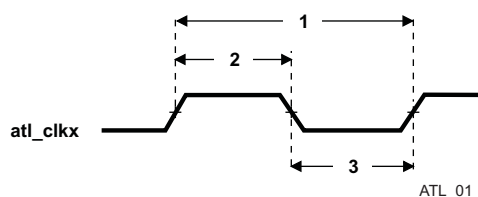


图 5-62. ATL\_CLKOUTx Timing

## 5.9.7 Emulation and Debug Subsystem

The device includes the following Test interfaces:

- IEEE 1149.1 Standard-Test-Access Port (JTAG)
- Trace Port Interface Unit (TPIU)

### 5.9.7.1 JTAG Electrical Data/Timing

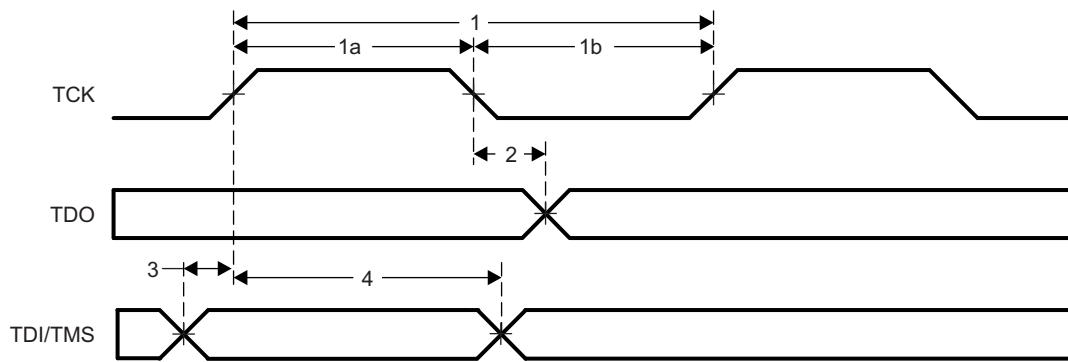
表 5-78, 表 5-79 和 图 5-63 assume testing over the recommended operating conditions and electrical characteristic conditions below.

**表 5-78. Timing Requirements for IEEE 1149.1 JTAG**

| NO. | PARAMETER                | DESCRIPTION                              | MIN   | MAX | UNIT |
|-----|--------------------------|------------------------------------------|-------|-----|------|
| 1   | $t_c(\text{TCK})$        | Cycle time, TCK                          | 62.29 |     | ns   |
| 1a  | $t_w(\text{TCKH})$       | Pulse duration, TCK high (40% of $t_c$ ) | 24.92 |     | ns   |
| 1b  | $t_w(\text{TCKL})$       | Pulse duration, TCK low(40% of $t_c$ )   | 24.92 |     | ns   |
| 3   | $t_{su}(\text{TDI-TCK})$ | Input setup time, TDI valid to TCK high  | 6.23  |     | ns   |
|     | $t_{su}(\text{TMS-TCK})$ | Input setup time, TMS valid to TCK high  | 6.23  |     | ns   |
| 4   | $t_h(\text{TCK-TDI})$    | Input hold time, TDI valid from TCK high | 31.15 |     | ns   |
|     | $t_h(\text{TCK-TMS})$    | Input hold time, TMS valid from TCK high | 31.15 |     | ns   |

**表 5-79. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG**

| NO. | PARAMETER               | DESCRIPTION                      | MIN | MAX  | UNIT |
|-----|-------------------------|----------------------------------|-----|------|------|
| 2   | $t_d(\text{TCKL-TDOV})$ | Delay time, TCK low to TDO valid | 0   | 30.5 | ns   |



SPRS91v\_JTAG\_01

**图 5-63. JTAG Timing**

表 5-80, 表 5-81 和 图 5-64 assume testing over the recommended operating conditions and electrical characteristic conditions below.

**表 5-80. Timing Requirements for IEEE 1149.1 JTAG With RTCK**

| NO. | PARAMETER                | DESCRIPTION                              | MIN   | MAX | UNIT |
|-----|--------------------------|------------------------------------------|-------|-----|------|
| 1   | $t_c(\text{TCK})$        | Cycle time, TCK                          | 62.29 |     | ns   |
| 1a  | $t_w(\text{TCKH})$       | Pulse duration, TCK high (40% of $t_c$ ) | 24.92 |     | ns   |
| 1b  | $t_w(\text{TCKL})$       | Pulse duration, TCK low(40% of $t_c$ )   | 24.92 |     | ns   |
| 3   | $t_{su}(\text{TDI-TCK})$ | Input setup time, TDI valid to TCK high  | 6.23  |     | ns   |
|     | $t_{su}(\text{TMS-TCK})$ | Input setup time, TMS valid to TCK high  | 6.23  |     | ns   |
| 4   | $t_h(\text{TCK-TDI})$    | Input hold time, TDI valid from TCK high | 31.15 |     | ns   |
|     | $t_h(\text{TCK-TMS})$    | Input hold time, TMS valid from TCK high | 31.15 |     | ns   |

表 5-81. Switching Characteristics Over Recommended Operating Conditions for  
IEEE 1149.1 JTAG With RTCK

| NO. | PARAMETER              | DESCRIPTION                                                                                                                                                                              | MIN   | MAX | UNIT |
|-----|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-----|------|
| 5   | $t_d(\text{TCK-RTCK})$ | Delay time, TCK to RTCK with no selected subpaths (i.e. ICEPick is the only tap selected - when the Arm is in the scan chain, the delay time is a function of the Arm functional clock). | 0     | 27  | ns   |
| 6   | $t_c(\text{RTCK})$     | Cycle time, RTCK                                                                                                                                                                         | 62.29 |     | ns   |
| 7   | $t_w(\text{RTCKH})$    | Pulse duration, RTCK high (40% of $t_c$ )                                                                                                                                                | 24.92 |     | ns   |
| 8   | $t_w(\text{RTCKL})$    | Pulse duration, RTCK low (40% of $t_c$ )                                                                                                                                                 | 24.92 |     | ns   |

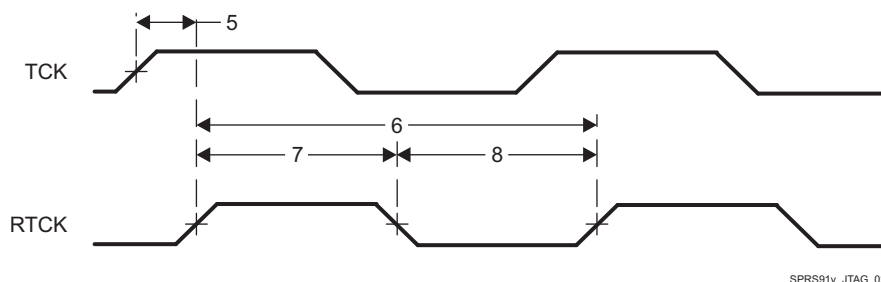


图 5-64. JTAG With RTCK Timing

## 5.9.7.2 Trace Port Interface Unit (TPIU)

### 5.9.7.2.1 TPIU PLL DDR Mode

表 5-82 和 图 5-65 假设测试 over the recommended operating conditions and electrical characteristic conditions below.

表 5-82. Switching Characteristics for TPIU

| NO.   | PARAMETER               | DESCRIPTION                                                  | MIN   | MAX  | UNIT |
|-------|-------------------------|--------------------------------------------------------------|-------|------|------|
| TPIU1 | $t_c(\text{clk})$       | Cycle time, TRACECLK period                                  | 5.56  |      | ns   |
| TPIU4 | $t_d(\text{clk-ctlV})$  | Skew time, TRACECLK transition to TRACECTL transition        | -1.61 | 1.98 | ns   |
| TPIU5 | $t_d(\text{clk-dataV})$ | Skew time, TRACECLK transition to TRACEDATA[17:0] transition | -1.61 | 1.98 | ns   |

(1) P = TRACECLK period in ns

(2) The listed pulse duration is a typical value

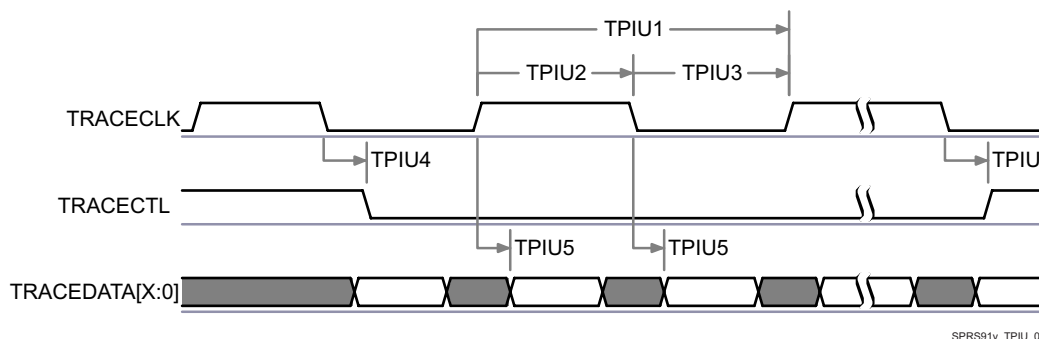


图 5-65. TPIU—PLL DDR Transmit Mode<sup>(1)</sup>

(1) In  $d[X:0]$ , X is equal to 15 or 17.

## 6 Detailed Description

### 6.1 Description

The DRA78x processor is offered in a 367-ball, 15×15-mm, 0.65-mm ball pitch (0.8mm spacing rules can be used on signals) with Via Channel™ Array (VCA) technology, ball grid array (S-PBGA) package.

The architecture is designed to deliver high-performance concurrencies for automotive co-processor, hybrid radio and amplifier applications in a cost-effective solution, providing full scalability from the DRA75x ("Jacinto 6 EP" and "Jacinto 6 Ex"), DRA74x "Jacinto 6", DRA72x "Jacinto 6 Eco", and DRA71x "Jacinto 6 Entry" family of infotainment processors, including voice, HMI, multimedia and smartphone projection mode capabilities.

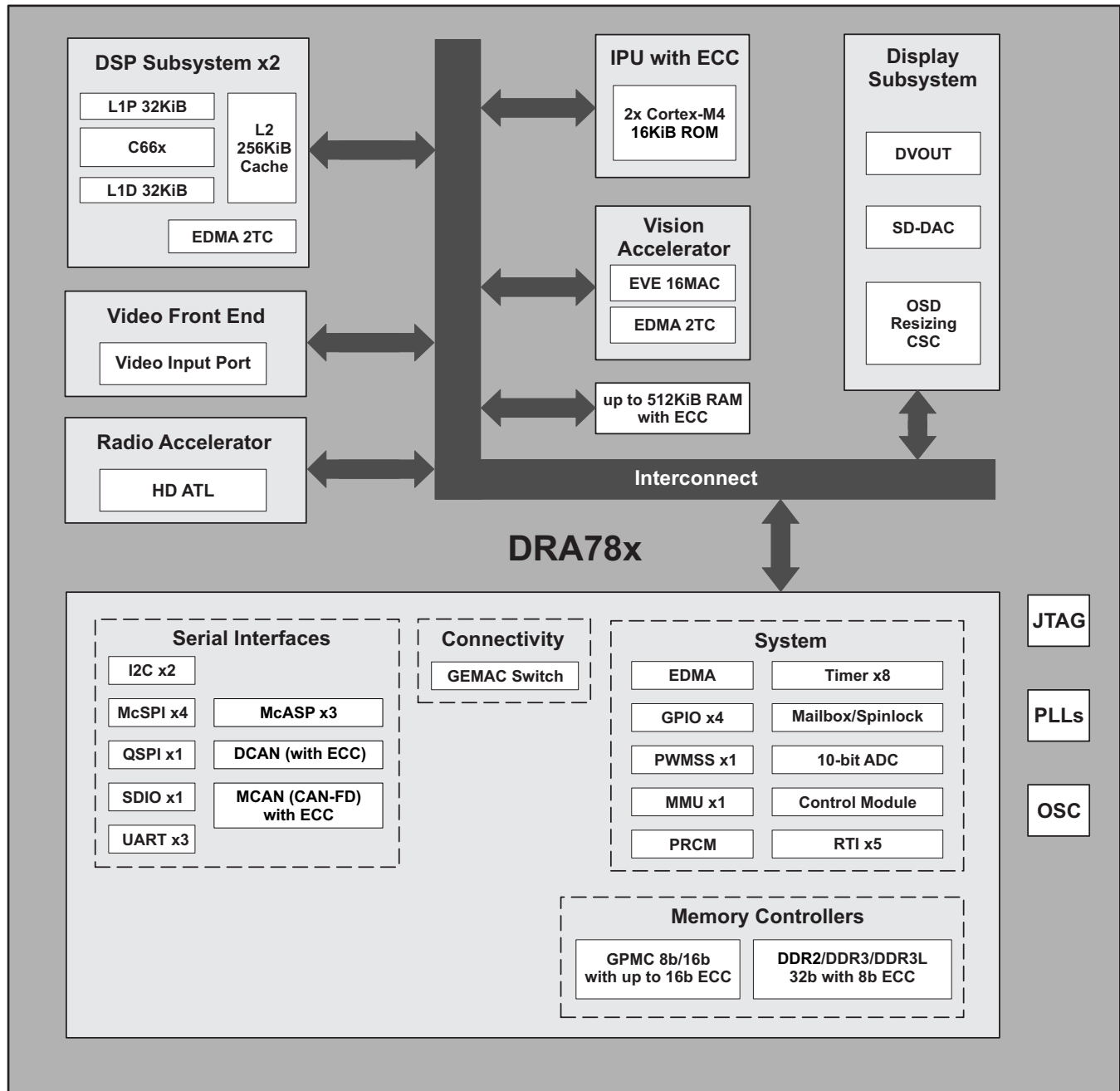
Additionally, TI provides a complete set of development tools for the Arm, and DSP, including C compilers and a debugging interface for visibility into source code execution.

The DRA78x Jacinto 6 RSP (Radio Sound Processor) device family is qualified according to the AEC-Q100 standard.

The device features a simplified power supply rail mapping which enables lower cost PMIC solutions.

### 6.2 Functional Block Diagram

 [6-1](#) is functional block diagram for the device.



func\_spr968-001

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图 6-1. DRA78x Block Diagram

## 6.3 DSP Subsystem

The device includes two identical instances (DSP1 and DSP2) of a digital signal processor (DSP) subsystem, based on the TI's standard TMS320C66x™ DSP CorePac core.

The TMS320C66x DSP core enhances the TMS320C674x™ core, which merges the C674x™ floating point and the C64x+™ fixed-point instruction set architectures. The C66x DSP is object-code compatible with the C64x+/C674x DSPs.

For more information on the TMS320C66x core CPU, see the *TMS320C66x DSP CPU and Instruction Set Reference Guide*, ([SPRUGH7](#)).

Each of the two DSP subsystems integrated in the device includes the following components:

- A TMS320C66x™ CorePac DSP core that encompasses:
  - L1 program-dedicated (L1P) cacheable memory
  - L1 data-dedicated (L1D) cacheable memory
  - L2 (program and data) cacheable memory
  - Extended Memory Controller (XMC)
  - External Memory Controller (EMC)
  - DSP CorePac located interrupt controller (INTC)
  - DSP CorePac located power-down controller (PDC)
- Dedicated enhanced data memory access engine - EDMA, to transfer data from/to memories and peripherals external to the DSP subsystem and to local DSP memory (most commonly L2 SRAM). The external DMA requests are passed through DSP system level (SYS) wakeup logic, and collected from the DSP1/DSP2 dedicated outputs of the device DMA Events Crossbar for each of the two subsystems.
- A level 2 (L2) interconnect network (DSP NoC) to allow connectivity between different modules of the subsystem or the remainder of the device via the device L3\_MAIN interconnect.
- Two memory management units (on EDMA L2 interconnect and DSP MDMA paths) for accessing the device L3\_MAIN interconnect address space.
- Dedicated system control logic (DSP\_SYSTEM) responsible for power management, clock generation, and connection to the device power, reset, and clock management (PRCM) module

The TMS320C66x Instruction Set Architecture (ISA) is the latest for the C6000 family. As with its predecessors (C64x, C64x+ and C674x), the C66x is an advanced VLIW architecture with 8 functional units (two multiplier units and six arithmetic logic units) that operate in parallel. The C66x CPU has a total of 64 general-purpose 32-bit registers.

Some features of the DSP C6000 family devices are:

- Advanced VLIW CPU with eight functional units (two multipliers and six ALUs) which:
  - Executes up to eight instructions per cycle for up to ten times the performance of typical DSPs
  - Allows designers to develop highly effective RISC-like code for fast development time
- Instruction packing:
  - Gives code size equivalence for eight instructions executed serially or in parallel
  - Reduces code size, program fetches, and power consumption
- Conditional execution of most instructions:
  - Reduces costly branching
  - Increases parallelism for higher sustained performance
- Efficient code execution on independent functional units:
  - Industry's most efficient C compiler on DSP benchmark suite
  - Industry's first assembly optimizer for fast development and improved parallelization
- 8-/16-/32-bit/64-bit data support, providing efficient memory support for a variety of applications.
- 40-bit arithmetic options which add extra precision for vocoders and other computationally intensive applications.
- Saturation and normalization to provide support for key arithmetic operations.
- Field manipulation and instruction extract, set, clear, and bit counting support common operation found in control and data manipulation applications.

The C66x CPU has the following additional features:

- Each multiplier can perform two  $16 \times 16$ -bit or four  $8 \times 8$  bit multiplies every clock cycle.
- Quad 8-bit and dual 16-bit instruction set extensions with data flow support.
- Support for non-aligned 32-bit (word) and 64-bit (double word) memory accesses.

- Special communication-specific instructions have been added to address common operations in error-correcting codes.
- Bit count and rotate hardware extends support for bit-level algorithms.
- Compact instructions: Common instructions (AND, ADD, LD, MPY) have 16-bit versions to reduce code size.
- Protected mode operation: A two-level system of privileged program execution to support higher-capability operating systems and system features such as memory protection.
- Exceptions support for error detection and program redirection to provide robust code execution
- Hardware support for modulo loop operation to reduce code size and allow interrupts during fully-pipelined code
- Each multiplier can perform  $32 \times 32$  bit multiplies
- Additional instructions to support complex multiplies allowing up to eight 16-bit multiply/add/subtracts per clock cycle

The TMS320C66x has the following key improvements to the ISA:

- 4x Multiply Accumulate improvement for both fixed and floating point
- Improvement of the floating point arithmetic
- Enhancement of the vector processing capability for fixed and floating point
- Addition of domain-specific instructions for complex arithmetic and matrix operations

**On the C66x ISA, the vector processing capability is improved by extending the width of the SIMD instructions.** The C674x DSP supports 2-way SIMD operations for 16-bit data and 4-way SIMD operations for 8-bit data. C66x enhances this capabilities with the addition of SIMD instructions for 32-bit data allowing operation on 128-bit vectors. For example the QMPY32 instruction is able to perform the element to element multiplication between two vectors of four 32-bit data each.

C66x ISA includes a set of specific instructions to handle complex arithmetic and matrix operations.

- **TMS320C66x DSP CorePac memory components:**
  - A 32-KiB L1 program memory (L1P) configurable as cache and/or SRAM:
    - When configured as a cache, the L1P is a 1-way set-associative cache with a 32-byte cache line
    - The DSP CorePac L1P memory controller provides bandwidth management, memory protection, and power-down functions
    - The L1P is capable of cache block and global coherence operations
    - The L1P controller has an Error Detection (ED) mechanism, including necessary SRAM
    - The L1P memory can be fully configured as a cache or SRAM
    - Page size for L1P memory is 2KB
  - A 32-KiB L1 data memory (L1D) configurable as cache and / or SRAM:
    - When configured as a cache, the L1D is a 2-way set-associative cache with a 64-byte cache line
    - The DSP CorePac L1D memory controller provides bandwidth management, memory protection, and power-down functions
    - The L1D memory can be fully configured as a cache or SRAM
    - No support for error correction or detection
    - Page size for L1D memory is 2KB
  - A 288-KiB (program and data) L2 memory, only part of which is cacheable:
    - When configured as a cache, the L2 memory is a 4-way set associative cache with a 128-byte cache line
    - Only 256 KiB of L2 memory can be configured as cache or SRAM
    - 32 KiB of the L2 memory is always mapped as SRAM
    - The L2 memory controller has an Error Correction Code (ECC) and ED mechanism, including necessary SRAM
    - The L2 memory controller supports hardware prefetching and also provides bandwidth management, memory protection, and power-down functions.
    - Page size for L2 memory is 16KB
- The **External Memory Controller (EMC)** is a bridge from the C66x CorePac to the rest of the DSP subsystem and device. It has :
  - a 32-bit configuration port (CFG) providing access to local subsystem resources (like DSP\_EDMA, DSP\_SYSTEM, and so forth) or to L3\_MAIN resources accessible via the CFG address range.
  - a 128-bit slave-DMA port (SDMA) which provides accesses of system masters outside the DSP subsystem to resources inside the DSP subsystem or C66x DSP CorePac memories, i.e. when the DSP subsystem is the slave in a transaction.
- The **Extended Memory Controller (XMC)** processes requests from the L2 Cache Controller (which are a result of CPU instruction fetches, load/store commands, cache operations) to device resources via the C66x DSP CorePac 128-bit master DMA (MDMA) port:
  - Memory protection for addresses outside C66x DSP CorePac generated over device L3\_MAIN on the MDMA port
  - Prefetch, multi-in-flight requests
- A DSP local **Interrupt Controller (INTC)** in the DSP C66x CorePac, interfaces the system events to the DSP C66x core CPU interrupt and exceptions inputs. The DSP subsystem C66x CorePac interrupt controller supports up to 128 system events of which 64 interrupts are external to DSP subsystems, collected from the DSP1/DSP2 dedicated outputs of the device Interrupt Crossbar.

- **Local Enhanced Direct Memory Access (EDMA) controller features:**
  - Channel controller (CC) : 64-channel, 128 PaRAM, 2 Queues
  - 2 x Third-party Transfer Controllers (TPTC0 and TPTC1):
    - Each TC has a 128-bit read port and a 128-bit write port
    - 2KiB FIFOs on each TPTC
  - 1-dimensional/2-dimensional (1D/2D) addressing
  - Chaining capability
- **DSP subsystem integrated MMUs:**
  - Two MMUs are integrated:
    - The MMU0 is located between DSP MDMA master port and the device L3\_MAIN interconnect and can be optionally bypassed
    - The MMU1 is located between the EDMA master port and the device L3\_MAIN interconnect
- A DSP local **Power-Down Controller (PDC)** is responsible to power-down various parts of the DSP C66x CorePac, or the entire DSP C66x CorePac.
- The DSP subsystem **System Control logic** provides:
  - Slave idle and master standby protocols with device PRCM for powerdown
  - OCP Disconnect handshake for init and target busses
  - Asynchronous reset
  - Power-down modes:
    - "Clockstop" mode featuring wake-up on interrupt event. The DMA event wake-up is managed in software.
- The device DSP subsystem is supplied by a PRCM DPLL, but each DSP1/2 **has integrated its own PLL module** outside the C66x CorePac for clock gating and division.
- **Each of the two device DSP subsystem has following port instances** to connect to remaining part of the device. See also :
  - A 128-bit initiator (DSP MDMA master) port for MDMA/Cache requests
  - A 128-bit initiator (DSP EDMA master) port for EDMA requests
  - A 32-bit initiator (DSP CFG master) port for configuration requests
  - A 128-bit target (DSP slave) port for requests to DSP memories and various peripherals
- **C66x DSP subsystems (DSPSS) safety aspects:**
  - Above mentioned memory ECC/ED mechanisms
  - MMUs enable mapping of only the necessary application space to the processor
  - Memory Protection Units internal to the DSPSS (in L1P, L1D and L2 memory controllers) and external to DSPSS (firewalls) to help define legal accesses and raise exceptions on illegal accesses
  - Exceptions: Memory errors, various DSP errors, MMU errors and some system errors are detected and cause exceptions. The exceptions could be handled by the DSP or by a designated safety processor at the chip level. Note that it may not be possible for the safety processor to completely handle some exceptions

**Unsupported features on the C66x DSP core for the device are:**

- The Extended Memory Controller MPAX (memory protection and address extension) 36-bit addressing is NOT supported

**Known DSP subsystem power mode restrictions for the device are:**

- "Full logic / RAM retention" mode featuring wake-up on both interrupt or DMA event (logic in "always on" domain). Only OFF mode is supported by DSP subsystem, **requiring full boot**.

For more information about C66x debug/trace support, see chapter *On-Chip Debug Support* of the device TRM.

## 6.4 IPU

The Imaging Processor Unit (IPU) subsystem contains two Arm® Cortex-M4 cores (IPU\_C0 and IPU\_C1) that share a common level 1 (L1) cache (called unicache). The two Cortex-M4 cores are completely homogeneous to one another. Any task possible using one Cortex-M4 core is also possible using the other Cortex-M4 core. Both Cortex-M4 cores could be used for tasks such as running RTOS, controlling ISP, SIMCOP, DSS, and other functions. It is software responsibility to distribute the various tasks between the Cortex-M4 cores for optimal performance. The integrated interrupt handling of the IPU subsystem allows it to function as an efficient control unit.

IPU is the boot master of this device with its own boot ROM.

The key features of the IPU subsystem are:

- Two Arm Cortex-M4 microprocessors (IPU\_C0 and IPU\_C1):
  - Armv7-M and Thumb®-2 instruction set architecture (ISA)
  - Armv6 SIMD and digital signal processor (DSP) extensions
  - Single-cycle MAC
  - Integrated nested vector interrupt controller (NVIC) (also called IPU\_Cx\_INTIC, where x = 0, 1)
  - Integrated bus matrix:
    - Bus arbiter
    - Bit-banding – atomic bit manipulation
    - Write buffer
    - Memory interface (I and D) plus system interface (S) and private peripheral bus (PPB)
  - Registers:
    - Thirteen general-purpose 32-bit registers
    - Link register (LR)
    - Program counter (PC)
    - Program status register, xPSR
    - Two banked SP registers
  - Integrated power management
  - Extensive debug capabilities
- Unicache interface:
  - AHBLite to unicache interface
  - Instruction and data interface
  - Supports interleaved Cortex-M4 requests
- L1 cache (IPU\_UNICACHE):
  - 32KiB divided into 16 banks
  - 4-way
  - Runs at twice the Cortex-M4 CPU frequency
  - Cache configuration lock/freeze/preload
  - Internal MMU:
    - 16-entry region-based address translation
    - Read/write control and access type control
    - Runs at twice the Cortex-M4 CPU frequency
    - Execute Never (XN) MMU protection policy
    - Little-endian format
  - OCP port for configuration and cache maintenance
- Subsystem counter timer module (SCTM) connected to unicache

- L2 master interface (MIF):
  - Splitter for access to memory or OCP ports
  - Interleaved bank request for fast memory access
- L2 internal memories:
  - 16KiB ROM – IPU\_ROM; used for device boot/initialization
  - 64KiB banked RAM – IPU\_RAM
- L2 MMU (IPU\_MMU): 32 entries with Table Walking Logic (TWL)
- Wake-up generator (IPU\_WUGEN): Generates wake-up request from external interrupts
- Two OCP ports at IPU boundary (connected to the L3\_MAIN interconnect):
  - Master port – allows the IPU to access system resources (memories and peripherals)
  - Slave port – allows other requestors to access a part of the IPU internal memory space
- Power management:
  - Local power-management control: Configurable through the IPU\_WUGEN registers.
  - Two sleep modes supported by Cortex-M4, controlled by its integrated interrupt controller (NVIC).
  - Cortex-M4 system is clock-gated in both sleep modes.
  - NVIC interrupt interface stays awake.
  - Supports L1 cache and L2 memories retention.
- Error-Correcting Code (ECC) supported for both L1 unicache and L2 RAM
- Debug/emulation features supported

For more information, see chapter *Dual Cortex-M4 IPU Subsystem* of the device TRM.

## 6.5 EVE

The embedded vision engine (EVE) module is a programmable imaging and vision processing engine, intended for use in devices that serve customer electronics imaging and vision applications. Its programmability meets late-in-development or post-silicon processing requirements, and lets third parties or customers add differentiating features in imaging and vision products.

The device includes one instantiation of the EVE engine. A single EVE module consists of an ARP32 scalar core, a vector coprocessor (VCOP) vector core, and an Enhanced DMA (EDMA3) controller.

The EVE engine includes the following main features:

- Two 128-bit interconnect initiator ports used for:
  - Paging between system-level memory (L3 SRAM/DDR) and EVE memory (primarily IBUF, WBUF)
  - ARP32 program fetches to system memory (through program cache)
  - ARP32 load or store requests to system memory
  - ARP32 program cache-related read requests, including prefetch/preload requests
- 128-bit interconnect target port used for system-level host or DMA access to EVE memory or MMR space
- Scalar core (ARP32) with the following features:
  - 32KB program cache (direct mapped and prefetch)
  - 32KB data memory (DMEM)
- Vector core (VCOP):
  - 32KB working buffer (WBUF)
  - 16KB image buffer low copy A (IBUFLA)
  - 16KB image buffer low copy B (IBUFLB)
  - 16KB image buffer high copy A (IBUFHA)
  - 16KB image buffer high copy B (IBUFHB)
- EDMA channel controller (EDMACC): 128 PaRAM entries, 2 Queues
- EDMA transfer controllers: two instances, 2k FIFO each

- Memory Management Units (MMUs):
  - 32-entry TLB per MMU
  - Page walking with hardware
  - EDMA accesses and ARP32 program or data accesses to system memory space
  - Can limit EVE accesses to desired subset of system addresses
- Configuration interconnect for MMR and debug accesses
- High-performance interconnect for high throughput and high concurrency data transfers between connected endpoints
- Multiple interrupts for interrupt mapping, DMA event mapping, and interprocessor handshaking
- Support for slave idle and master standby protocols for clock gating
- No support for retention and memory array off modes
- Error detection on all memories:
  - Single bit error detect on DMEM, WBUF, IBUFLA, IBUFLB, IBUFHA, and IBUFHB
  - Double bit error detect on program cache
- Invalid instruction detection in the two processor units (ARP32 and VCOP)
- Debug support:
  - Subsystem Counter Timer Module (SCTM) for counting and measuring of VCOP, EVE program cache, and EDMA performance-related state
  - Software Messaging System Event Trace (SMSET) for trace of software messages and hardware events
  - ARP32 debug support: State visibility, breakpoint, run control, cross-triggering
  - VCOP debug support: State visibility and run control
- Interprocessor communication: Internal Mailbox for DSP/EVE communication

For more information, see chapter *Embedded Vision Engine (EVE)* of the device TRM.

## 6.6 Memory Subsystem

### 6.6.1 EMIF

The EMIF module provides connectivity between DDR memory types and manages data bus read/write accesses between external memory and device subsystems which have master access to the L3\_MAIN interconnect and DMA capability.

The EMIF module has the following capabilities:

- Supports JEDEC standard-compliant DDR2-SDRAM and DDR3/DDR3L-SDRAM memory types
- 2-GiB SDRAM address range over one chip-select.
- Supports SDRAM devices with one, two, four or eight internal banks
- Data bus widths:
  - 128-bit L3\_MAIN (system) interconnect data bus width
  - 32-bit SDRAM data bus width
  - 16-bit SDRAM data bus width used in narrow mode
- Supported CAS latencies:
  - DDR3: 5, 6, 7, 8, 9, 10 and 11
  - DDR2: 2, 3, 4, 5, 6 and 7
- Supports 256-, 512-, 1024-, and 2048-word page sizes
- Supported burst length: 8
- Supports sequential burst type
- SDRAM auto initialization from reset or configuration change
- Supports self refresh and power-down modes for low power
- Partial array self-refresh mode for low power when DDR3 is used
- Output impedance (ZQ) calibration for DDR3
- Supports on-die termination (ODT) for DDR2 and DDR3
- Supports prioritized refresh
- Programmable SDRAM refresh rate and backlog counter
- Programmable SDRAM timing parameters
- Write and read leveling/calibration and data eye training for DDR3
- ECC on the SDRAM data bus:
  - 7-bit ECC over 32-bit data
  - 6-bit ECC over 16-bit data when narrow mode is used
  - 1-bit error correction and 2-bit error detection
  - Programmable address ranges to define ECC protected region
  - ECC calculated and stored on all writes to ECC protected address region
  - ECC verified on all reads from ECC protected address region
  - Statistics for 1-bit ECC and 2-bit ECC errors
  - The total width of the ECC DDR data bus is 8 bits

The EMIF module does not support:

- Burst chop for DDR3
- Interleave burst type
- Auto precharge because of better Bank Interleaving performance
- OCD calibration for DDR2
- CAS Read Latency of 2 and CAS Write Latency of 1 for DDR2
- DLL disabling from EMIF side

For more information, see section *DDR External Memory Interface (EMIF)* in chapter *Memory Subsystem* of the device TRM.

### 6.6.2 GPMC

The General Purpose Memory Controller (GPMC) is an external memory controller of the device. Its data access engine provides a flexible programming model for communication with all standard memories.

The GPMC supports the following various access types:

- Asynchronous read/write access
- Asynchronous read page access (4, 8, and 16 Word16)
- Synchronous read/write access
- Synchronous read/write burst access without wrap capability (4, 8 and 16 Word16)
- Synchronous read/write burst access with wrap capability (4, 8 and 16 Word16)
- Address-data-multiplexed (AD) access
- Address-address-data (AAD) multiplexed access
- Little- and big-endian access

The GPMC can communicate with a wide range of external devices:

- External asynchronous or synchronous 8-bit wide memory or device (non burst device)
- External asynchronous or synchronous 16-bit wide memory or device
- External 16-bit non-multiplexed NOR flash device
- External 16-bit address and data multiplexed NOR Flash device
- External 8-bit and 16-bit NAND flash device
- External 16-bit pseudo-SRAM (pSRAM) device

The main features of the GPMC are:

- 8- or 16-bit-wide data path to external memory device
- Supports up to eight CS regions of programmable size and programmable base addresses in a total address space of 1 GiB
- Supports transactions controlled by a firewall
- On-the-fly error code detection using the Bose-Chaudhuri-Hocquenghem (BCH) (t = 4, 8, or 16) or Hamming code to improve the reliability of NAND with a minimum effect on software (NAND flash with 512-byte page size or greater)
- Fully pipelined operation for optimal memory bandwidth use
- The clock to the external memory is provided from GPMC functional clock divided by 1, 2, 3, or 4
- Supports programmable autoclock gating when no access is detected
- Independent and programmable control signal timing parameters for setup and hold time on a per-chip basis. Parameters are set according to the memory device timing parameters, with a timing granularity of one GPMC functional clock cycle.
- Flexible internal access time control (WAIT state) and flexible handshake mode using external WAIT pin monitoring
- Support bus keeping
- Support bus turnaround
- Prefetch and write posting engine associated with a device DMA to achieve full performance from the NAND device with minimum effect on NOR/SRAM concurrent access

For more information, see section *General-Purpose Memory Controller (GPMC)* in chapter *Memory Subsystem* of the device TRM.

### 6.6.3 ELM

When reading from NAND flash memories, some level of error-correction is required. In the case of NAND modules with no internal correction capability, sometimes referred to as *bare NANDs*, the correction process is delegated to the memory controller.

The ELM supports the following features:

- 4, 8, and 16 bits per 512-byte block error location based on BCH algorithm
- Eight simultaneous processing contexts
- Page-based and continuous modes
- Interrupt generation when error location process completes:
  - When the full page has been processed in page mode
  - For each syndrome polynomial (checksum-like information) in continuous mode

For more information, see section *Error Location Module (ELM)* in chapter *Memory Subsystem* of the device TRM.

### 6.6.4 OCMC

There is one on-chip memory controller (OCMC) in the device.

The OCM Controller supports the following features:

- L3\_MAIN data interface:
  - Used for maximum throughput performance
  - 128-bit data bus width
  - Burst supported
- L4 interface:
  - Used for access to configuration registers
  - 32-bit data bus width
  - Only single accesses supported
  - The L4 associated OCMC clock is two times lower than the L3 associated OCMC clock
- Error correction and detection:
  - Single error correction and dual error detection
  - 9-bit Hamming error correction code (ECC) calculated on 128-bit data word which is concatenated with memory address bits
  - Hamming distance of 4
  - Enable/Disable mode control through a dedicated register
  - Single bit error correction on a read transaction
  - Exclusion of repeated addresses from correctable error address trace history
  - ECC valid for all write transactions to an enabled region
  - Sub-128-bit writes supported via read modify write
- ECC Error Status Reporting:
  - Trace history buffer (FIFO) with depth of 4 for corrected error address
  - Trace history buffer with depth of 4 for non correctable error address and also including double error detection
  - Interrupt generation for correctable and uncorrectable detected errors
- ECC Diagnostics Configuration:
  - Counters for single error correction (SEC), double error detection (DED) and address error events (AEE)
  - Programmable threshold registers for exceptions associated with SEC, DED and AEE counters
  - Register control for enabling and disabling of diagnostics
  - Configuration registers and ECC status accessible through L4 interconnect

- Circular buffer for sliced based VIP frame transfers:
  - Up to 12 programmable circular buffers mapped with unique virtual frame addresses
  - On the fly (with no additional latency) address translation from virtual to OCMC circular buffer memory space
  - Virtual frame size up to 8 MiB and circular buffer size up to 1 MiB
  - Error handling and reporting of illegal CBUF addressing
  - Underflow and Overflow status reporting and error handling
  - Last access read/write address history
- Two Interrupt outputs configured independently to service either ECC or CBUF interrupt events

The OCM controller does not have a memory protection logic and does not support endianness conversion.

For more information, see section *On-Chip Memory (OCM) Subsystem* in chapter *Memory Subsystem* of the device TRM.

## 6.7 Interprocessor Communication

### 6.7.1 Mailbox

Communication between the on-chip processors of the device uses a queued mailbox-interrupt mechanism.

The queued mailbox-interrupt mechanism allows the software to establish a communication channel between two processors through a set of registers and associated interrupt signals by sending and receiving messages (mailboxes).

The device implements the following mailbox types:

- System mailbox:
  - Number of instances: 2
  - Used for communication between: DSP1, DSP2, IPU subsystems
  - Reference name: MAILBOX1, MAILBOX2

Each mailbox module supports the following features:

- Parameters configurable at design time
  - Number of users
  - Number of mailbox message queues
  - Number of messages (FIFO depth) for each message queue
- 32-bit message width
- Message reception and queue-not-full notification using interrupts
- Support of 16-/32-bit addressing scheme
- Power management support

For more information, see chapter *Mailbox* of the device TRM.

### 6.7.2 Spinlock

The Spinlock module provides hardware assistance for synchronizing the processes running on multiple processors in the device:

- Digital signal processor (DSP) subsystems – DSP1 and DSP2
- Dual Cortex-M4 image processing unit (IPU) subsystems – IPU1 and IPU2

The Spinlock module implements 256 spinlocks (or hardware semaphores), which provide an efficient way to perform a lock operation of a device resource using a single read-access, avoiding the need of a read-modify-write bus transfer that the programmable cores are not capable of.

For more information, see chapter *Spinlock* of the device TRM.

## 6.8 Interrupt Controller

The device has a large number of interrupts to service the needs of its many peripherals and subsystems. The DSP (x2), and IPU, and EVE subsystems are capable of servicing these interrupts via their integrated interrupt controllers. In addition, each processor's interrupt controller is preceded by an Interrupt Controller Crossbar (IRQ\_CROSSBAR) that provides flexibility in mapping the device interrupts to processor interrupt inputs. For more information about IRQ crossbar, see chapter *Control Module* of the Device TRM.

### C66x DSP Subsystem Interrupt Controller (DSPx\_INTC, where x = 1, 2)

There are two Digital Signal Processing (DSP) subsystems in the device - DSP1, and DSP2. Each DSP subsystem integrates an interrupt controller - DSPx\_INTC, which interfaces the system events to the C66x core interrupt and exceptions inputs. It combines up to 128 interrupts into 12 prioritized interrupts presented to the C66x CPU.

For detailed information about this module, see chapter *DSP Subsystems* of the Device TRM.

### Dual Cortex-M4 IPU Subsystem Interrupt Controller (IPU\_Cx\_INTC, where x = 1, 2)

There is one Image Processing Unit (IPU) subsystem in the device. The IPU subsystem integrates two Arm® Cortex-M4 cores.

A Nested Vectored Interrupt Controller (NVIC) is integrated within each Cortex-M4. The interrupt mapping is the same for the two cores to facilitate parallel processing. The NVIC supports:

- 96 external interrupts (in addition to 16 Cortex-M4 internal interrupts), which are dynamically prioritized with 16 levels of priority defined for each core
- Low-latency exception and interrupt handling
- Prioritization and handling of exceptions
- Control of the local power management
- Debug accesses to the processor core

For detailed information about this module, refer to Arm *Cortex-M4 Technical Reference Manual* (available at [infocenter.arm.com/help/index.jsp](http://infocenter.arm.com/help/index.jsp)).

### EVE Subsystem Interrupt Controller (EVE\_INTC)

There is one Embedded Video Engine (EVE) subsystems in the device. The EVE subsystem integrates an interrupt controller - EVE\_INTC, which handles incoming interrupts, merging them with internal interrupt sources to drive ARP32's interrupt inputs. It also allows ARP32 to generate outgoing interrupts or events to synchronize with other system processors and EDMA.

The EVE\_INTC supports up to 32 active-high level interrupt inputs. Its architecture allows both hardware and software prioritization.

For detailed information about this module, see chapter *Embedded Vision Engine* of the Device TRM.

## 6.9 EDMA

The enhanced direct memory access module, also called EDMA, performs high-performance data transfers between two slave points, memories and peripheral devices without microprocessor unit (MPU) or digital signal processor (DSP) support during transfer. EDMA transfer is programmed through a logical EDMA channel, which allows the transfer to be optimally tailored to the requirements of the application.

The EDMA can also perform transfers between external memories and between device subsystems internal memories, with some performance loss caused by resource sharing between the read and write ports.

EDMA controller is based on two major principal blocks:

- EDMA third-party channel controller (EDMA\_TPCC)
- EDMA third-party transfer controller (EDMA\_TPTC)

The **EDMA\_TPCC** channel controller has following features:

- Fully orthogonal transfer description:
  - Three transfer dimensions.
  - A-synchronized transfers: one-dimension serviced per event.
  - AB-synchronized transfers: two-dimensions serviced per event.
  - Independent indexes on source and destination.
  - Chaining feature allows a 3-D transfer based on a single event.
- Flexible transfer definition:
  - Increment or FIFO transfer addressing modes.
  - Linking mechanism allows automatic PaRAM set update.
  - Chaining allows multiple transfers to execute with one event.
- Interrupt generation for the following:
  - Transfer completion.
  - Error conditions.
- Debug visibility:
  - Queue water marking/threshold.
  - Error and status recording to facilitate debug.
- 64 DMA request channels:
  - Event synchronization.
  - Chain synchronization (completion of one transfer triggers another transfer).
- Eight QDMA channels:
  - QDMA channels trigger automatically upon writing to a parameter RAM (PaRAM) set entry.
  - Support for programmable QDMA channel to PaRAM mapping.
- 512 PaRAM sets:
  - Each PaRAM set can be used for a DMA channel, QDMA channel, or link set.
- Two transfer controllers/event queues.
- 16 event entries per event queue.
- Memory protection support:
  - Proxy memory protection for TR submission.
  - Active memory protection for accesses to PaRAM and registers.

The **EDMA\_TPTC** transfer controller has the following features:

- Two transfer controllers (TC).
- 128-bit wide read and write ports per TC.
- Up to four in-flight transfer requests (TRs).
- Programmable priority level.
- Supports two-dimensional transfers with independent indexes on source and destination (EDMA\_TPCC manages the 3rd dimension).
- Support for increment or constant addressing mode transfers.
- Interrupt and error support.
- Memory-Mapped Register (MMR) bit fields are fixed position in 32-bit MMR regardless of endianness.

EDMA controller uses the shared MMU1 module for transferring to and from DSP module. This provides several benefits including:

- Protection of Host CPU memory regions from accidental corruption by EDMA TPTCs.
- Direct allocation of buffers in user space without the need for translation between CPU and DSP applications using EDMA TPTCs.

Accesses by the EDMA TPTCs (both TPTC0 and TPTC1) may optionally be routed through the MMU1.

The TPTC0 and TPTC1 routing allows EDMA transfer controller to be used to perform transfers using only the virtual addresses of the associated buffers.

For more information chapter *Enhanced DMA* of the device TRM.

## 6.10 Peripherals

### 6.10.1 VIP

The VIP module provides video capture functions for the device. VIP incorporates a multichannel raw video parser, various video processing blocks, and a flexible Video Port Direct Memory Access (VPDMA) engine to store incoming video in various formats. The device uses a single instantiation of the VIP module giving the ability of capturing up to two video streams.

A VIP module includes the following main features:

- Two independently configurable external video input capture slices (Slice 0 and Slice 1) each of which has two video input ports, Port A and Port B, where Port A can be configured as a 16/8-bit port, and Port B is a fixed 8-bit port.
- Each video Port A can be operated as a port with clock independent input channels (with interleaved or separated Y/C data input). Embedded sync and external sync modes are supported for all input configurations.
- Support for a single external asynchronous pixel clock, up to 165MHz per port.
- Pixel Clock Input Domain Port A supports up to one 16-bit input data bus, including BT.1120 style embedded sync for 16-bit data.
- Embedded Sync data interface mode supports single or multiplexed sources
- Discrete Sync data interface mode supports only single source input
- 16-bit data input plus discrete syncs can be configured to include:
  - 8-bit YUV422 (Y and U/V time interleaved)
  - 16-bit YUV422 (CbY and CrY time interleaved)
  - 16-bit RGB565
  - 16-bit RAW Capture
- Discrete sync modes include:
  - VSYNC + HSYNC (FID determined by FID signal pin or HSYNC/VSYNC skew)
  - VSYNC + ACTVID + FID
  - VBLANK + ACTVID (ACTVID toggles in VBLANK) + FID
  - VBLANK + ACTVID (no ACTVID toggles in VBLANK) + FID
- Multichannel parser (embedded syncs only)
  - Embedded syncs only
  - Pixel (2x or 4x) or Line multiplexed modes supported
  - Performs demultiplexing and basic error checking
  - Supports maximum of 9 channels in Line Mux (8 normal + 1 split line)
- Ancillary data capture support
  - For 16-bit input, ancillary data may be extracted from any single channel
  - For 8-bit time interleaved input, ancillary data can be chosen from the Luma channel, the Chroma channel, or both channels
  - Horizontal blanking interval data capture only supported when using discrete syncs (VSYNC + HSYNC or VSYNC + HBLANK)
  - Ancillary data extraction supported on multichannel capture as well as single source streams

- Format conversion and scaling
  - Programmable color space conversion
  - YUV422 to YUV444 conversion
  - YUV444 to YUV422 conversion
  - YUV422 to YUV420 conversion
  - YUV422 Source: YUV422 to YUV422, YUV422 to YUV420, YUV422 to YUV444, YUV422 to RGB888
  - Supports RAW to RAW (no processing)
  - Scaling and format conversions do not work for multiplexed input
- Supports up to 2047 pixels wide input - when scaling is engaged
- Supports up to 3840 pixels wide input - when only chroma up/down sampling is engaged, without scaling
- Supports up to 4095 pixels wide input - without scaling and chroma up/down sampling
- The maximum supported input resolution is further limited by pixel clock and feature-dependent constraints

For more information, see chapter *Video Input Port* of the device TRM.

### 6.10.2 DSS

The Display Subsystem (DSS) provides the logic to interface display peripherals. DSS integrates a DMA engine as part of DISPC module, which allows direct access to the memory frame buffer. Various pixel processing capabilities are supported, such as: color space conversion, filtering, scaling, blending, color keying, etc.

The supported display interfaces are:

- One parallel CMOS output, which can be used for MIPI® DPI 2.0, or BT-656 or BT-1120.
- One TV output, which is connected to the internal Video Encoder module (VENC). The VENC drives a single video digital-to-analog converter (SD\_DAC) supporting composite video mode.

The modules integrated in the display subsystem are:

- Display controller (DISPC), with the following main features
  - One direct memory access (DMA) engine
  - One graphics pipeline (GFX), two video pipelines (VID1 and VID2), and one write-back pipeline (WB)
  - Two overlay managers
  - Active Matrix color support for 12/16/18/24-bit (truncated or dithered encoded pixel values)
  - One Video Port (VP) with programmable timing generator to support:
    - DPI: up to 165 MHz pixel clock video formats defined in CEA-861-E and VESA DMT standards
    - VENC: NTSC/PAL standards with 60Hz/50Hz refresh rates
  - Supported maximum FrameBuffer width of 4096 for all pixel formats
  - Configurable output mode: progressive or interlaced
  - Selection between RGB and YUV422 output pixel formats (YUV4:2:2 only available when BT-656 or BT-1120 output mode is enabled)

For more information, see section *Display Controller* in chapter *Display Subsystem* of the device TRM.

- Video Encoder (VENC) with 10-bit standard definition video DAC (SD\_DAC).

For more information, see section *Video Encoder* in chapter *Display Subsystem* of the device TRM.

DSS provides two interfaces to L3\_MAIN interconnect

- One 128-bit master port (with MFLAG support). The DMA engine in DISPC uses this single master to read/write data from/to device system memory.

- One 32-bit slave port. Used for registers configuration. It is further connected internally to DISPC and VENC modules.

For more information, see chapter *Display Subsystem* of the device TRM.

### 6.10.3 ATL

The audio tracking logic (ATL) is used by HD Radio™ applications to synchronize the digital audio output to the baseband clock. This same IP can also be used generically to track errors between two reference signals (such as frame syncs) and generate a modulated clock output (using software-controlled cycle stealing) which averages to some desired frequency. This process can be used as a hardware assist for asynchronous sample rate conversion algorithms. The tracking range is limited, so direct conversion between the two standard sample rate groups frequencies from 44.1 to 48 kHz is not possible.

The ATL includes the following main features:

- One ATL module, containing four ATL instances, for HD Radio support and asynchronous sample rate conversion assistance
- Each instance tracks the time error between two syncs (local audio word select [AWS] and baseband word select [BWS])
- Each instance selects between 16 mux choices for each of AWS and BWS.
- Each instance generates modulated ATCLK\_OUT clock signal with software-initiated pulse stealing.
- Selection between INTERCONNECT clock or functional ATLPCLK to run error counting timers and to derive modulated ATCLK\_OUT clock outputs
- Clock and reset management: Receives clock and reset signals from the device power, reset, and clock management (PRCM) module. The PRCM module has its own dedicated clock domain (CD\_ATL). The module receives hardware reset from the CORE\_RST reset domain.
- Power management: The ATL belongs to the PD\_COREAON power domain.

For more information, see chapter *Audio Tracking Logic* of the device TRM.

### 6.10.4 ADC

The analog-to-digital converter (ADC) module is a successive-approximation-register (SAR) general-purpose analog-to-digital converter.

The main features of the ADC include:

- 10-bit data.
- 8 general-purpose ADC channels.
- 750 KSPS at 13.5-MHz ADC\_CLK.
- Programmable FSM sequencer.
- Support interrupts and status, with masking.

For more information, see chapter *ADC* of the device TRM.

### 6.10.5 Timers

The device includes several types of timers used by the system software, including eight general-purpose (GP) timers, and a 32-kHz synchronized timer (COUNTER\_32K).

#### 6.10.5.1 General-Purpose Timers

The device has eight GP timers: TIMER1 through TIMER8.

- TIMER1 (1-ms tick) includes a specific function to generate accurate tick interrupts to the operating system and it belongs to the PD\_WKUPAON domain.
- TIMER2 through TIMER8 belong to the PD\_COREAON module.

Each timer can be clocked from the system clock (19.2, 20, or 27 MHz) or the 32-kHz clock. Select the clock source at the power, reset, and clock management (PRCM) module level.

Each timer provides an interrupt through the device IRQ\_CROSSBAR.

The following are the main features of the GP timer controllers:

- Level 4 (L4) slave interface support:
  - 32-bit data bus width
  - 32-/16-bit access supported
  - 8-bit access not supported
  - 10-bit address bus width
  - Burst mode not supported
  - Write nonposted transaction mode supported
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Compare and capture modes
- Autoreload mode
- Start and stop mode
- Programmable divider clock source ( $2^n$ , where  $n = [0:8]$ )
- Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
- Dedicated GP output signal for using the `TIMERi_GPO_CFG` signal
- On-the-fly read/write register (while counting)
- 1-ms tick with 32.768-Hz functional clock generated (only TIMER1)

For more information, see section *General-Purpose Timers* in chapter *Timers* of the device TRM.

#### 6.10.5.2 32-kHz Synchronized Timer (COUNTER\_32K)

The 32-kHz synchronized timer (COUNTER\_32K) is a 32-bit counter clocked by the falling edge of the 32-kHz system clock.

The main features of the 32-kHz synchronized timer controller are:

- L4 slave interface (OCP) support:
  - 32-bit data bus width
  - 32-/16-bit access supported
  - 8-bit access not supported
  - 16-bit address bus width
  - Burst mode not supported
  - Write nonposted transaction mode not supported
- Only read operations are supported on the module registers; no write operation is supported (no error/no action on write).
- Free-running 32-bit upward counter
- Start and keep counting after power-on reset
- Automatic roll over to 0; highest value reached: 0xFFFF FFFF
- On-the-fly read (while counting)

For more information, see section *32-kHz Synchronized Timer (COUNTER\_32K)* in chapter *Timers* of the device TRM.

### 6.10.6 I2C

The device contains five multimaster inter-integrated circuit (I<sup>2</sup>C) controllers (I2Ci modules, where  $i = 1, 2$ ) each of which provides an interface between a local host (LH), such as a digital signal processor (DSP), and any I<sup>2</sup>C-bus-compatible device that connects through the I<sup>2</sup>C serial bus. External components attached to the I<sup>2</sup>C bus can serially transmit and receive up to 8 bits of data to and from the LH device through the 2-wire I<sup>2</sup>C interface.

Each multimaster I<sup>2</sup>C controller can be configured to act like a slave or master I<sup>2</sup>C-compatible device.

For more information, see section *Multimaster I2C Controller* in chapter *Serial Communication Interfaces* of the device TRM.

### 6.10.7 UART

The UART is a simple L4 slave peripheral that use the EDMA for data transfer or IRQ polling via CPU. There are 3 UART modules in the device. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices.

#### 6.10.7.1 UART Features

The UARTi (where  $i = 1$  to 3) include the following features:

- 16C750 compatibility
- 64-byte FIFO buffer for receiver and 64-byte FIFO for transmitter
- Programmable interrupt trigger levels for FIFOs
- Baud generation based on programmable divisors N (where  $N = 1 \dots 16,384$ ) operating from a fixed functional clock of 48 MHz or 192 MHz

Oversampling is programmed by software as 16 or 13. Thus, the baud rate computation is one of two options:

- Baud rate = (functional clock / 16) / N
- Baud rate = (functional clock / 13) / N
- This software programming mode enables higher baud rates with the same error amount without changing the clock source
- Break character detection and generation
- Configurable data format:
  - Data bit: 5, 6, 7, or 8 bits
  - Parity bit: Even, odd, none
  - Stop-bit: 1, 1.5, 2 bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)
- The 48 MHz functional clock option allows baud rates up to 3.6Mbps
- The 192 MHz functional clock option allows baud rates up to 12Mbps

For more information, see section *UART* in chapter *Serial Communication Interfaces* of the device TRM.

### 6.10.8 McSPI

The McSPI is a master/slave synchronous serial bus. There are four separate McSPI modules (SPI1, SPI2, SPI3, and SPI4) in the device. All these four modules are able to work as both master and slave and support the following chip selects:

- MCSPI1: spi1\_cs[0], spi1\_cs[1], spi1\_cs[2], spi1\_cs[3]
- MCSPI2: spi2\_cs[0], spi2\_cs[1]
- MCSPI3: spi3\_cs[0], spi3\_cs[1]
- MCSPI4: spi4\_cs[0]

The McSPI modules include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to four master channels, or single channel in slave mode
- Master multichannel mode:
  - Full duplex/half duplex
  - Transmit-only/receive-only/transmit-and-receive modes
  - Flexible input/output (I/O) port controls per channel
  - Programmable clock granularity
  - SPI configuration per channel. This means, clock definition, polarity enabling and word width
- Single interrupt line for multiple interrupt source events
- Power management through wake-up capabilities
- Enable the addition of a programmable start-bit for SPI transfer per channel (start-bit mode)
- Supports start-bit write command
- Supports start-bit pause and break sequence
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel

For more information, see section *Multichannel Serial Peripheral Interface* in chapter *Serial Communication Interfaces* of the device TRM.

### 6.10.9 QSPI

The quad serial peripheral interface (QSPI™) module is a kind of SPI module that allows single, dual, or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. The QSPI works as a master only.

The QSPI supports the following features:

- General SPI features:
  - Programmable clock divider
  - Six pin interface
  - Programmable length (from 1 to 128 bits) of the words transferred
  - Programmable number (from 1 to 4096) of the words transferred
  - 4 external chip-select signals
  - Support for 3-, 4-, or 6-pin SPI interface
  - Optional interrupt generation on word or frame (number of words) completion
  - Programmable delay between chip select activation and output data from 0 to 3 QSPI clock cycles
  - Programmable signal polarities
  - Programmable active clock edge
  - Software-controllable interface allowing for any type of SPI transfer
  - Control through L3\_MAIN configuration port
- Serial flash interface (SFI) features:
  - Serial flash read/write interface
  - Additional registers for defining read and write commands to the external serial flash device
  - 1 to 4 address bytes
  - Fast read support, where fast read requires dummy bytes after address bytes; 0 to 3 dummy bytes can be configured.
  - Dual read support
  - Quad read support
  - Little-endian support only
  - Linear increment addressing mode only

The QSPI supports only dual and quad reads. Dual or quad writes are not supported. In addition, there is no "pass through" mode supported where the data present on the QSPI input is sent to its output.

For more information, see section *Quad Serial Peripheral Interface* in chapter *Serial Communication Interfaces* of the device TRM.

### 6.10.10 McASP

The McASP functions as a general-purpose audio serial port optimized to the requirements of various audio applications. The McASP module can operate in both transmit and receive modes. The McASP is useful for time-division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an intercomponent digital audio interface transmission (DIT). The McASP has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component.

Although intercomponent digital audio interface reception (DIR) mode (i.e. S/PDIF stream receiving) is not natively supported by the McASP module, a specific TDM mode implementation for the McASP receivers allows an easy connection to external DIR components (for example, S/PDIF to I2S format converters).

The device has integrated 3 McASP modules with:

- McASP1 supports 16 channels with independent TX/RX clock/sync domain
- McASP2 and McASP3 support 6 channels with independent TX/RX clock/sync domain

For more information, see section *Multichannel Audio Serial Port* in chapter *Serial Communication Interfaces* of the device TRM.

### 6.10.11 DCAN

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time applications. CAN has high immunity to electrical interference and the ability to self-diagnose and repair data errors. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.

The device supports:

- One DCAN module, referred to as DCAN1

The DCAN interface implements the following features:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 MBit/s
- 64 message objects in a dedicated message RAM
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Suspend mode for debug support
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Message RAM single error correction and double error detection (SECEDED) mechanism
- Direct access to message RAM during test mode
- Support for two interrupt lines: Level 0 and Level 1, plus separate ECC interrupt line
- Local power down and wakeup support
- Automatic message RAM initialization
- Support for DMA access

For more information, see section *DCAN* in chapter *Serial Communication Interfaces* of the device TRM.

### 6.10.12 MCAN

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a high level of security. CAN has high immunity to electrical interference and the ability to self-diagnose and repair data errors. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

The MCAN module implements the following features:

- Conforms with ISO 11898-1:2015
- Full CAN FD support (up to 64 data bytes)
- AUTOSAR and SAE J1939 support
- Up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, up to 32 elements
- Configurable Transmit Queue, up to 32 elements
- Configurable Transmit Event FIFO, up to 32 elements
- Up to 64 dedicated Receive Buffers
- Two configurable Receive FIFOs, up to 64 elements each
- Up to 128 filter elements

- Internal Loopback mode for self-test
- Maskable interrupts, two interrupt lines
- Two clock domains (CAN clock/Host clock)
- Parity/ECC support - Message RAM single error correction and double error detection (SECCED) mechanism
- Local power-down and wakeup support
- Timestamp Counter

For more information, see section *MCAN* in chapter *Serial Communication Interfaces* of the device TRM.

### 6.10.13 GMAC\_SW

The three-port gigabit ethernet switch subsystem (GMAC\_SW) provides ethernet packet communication and can be configured as an ethernet switch. It provides the reduced gigabit media independent interface (RGMII), and the management data input output (MDIO) for physical layer device (PHY) management.

The GMAC\_SW subsystem provides the following features:

- Two Ethernet ports (port 1 and port 2) with RGMII interfaces plus internal Communications Port Programming Interface (CPPI 3.1) on port 0
- Synchronous 10/100/1000 Mbit operation
- Wire rate switching (802.1d)
- Non-blocking switch fabric
- Flexible logical FIFO-based packet buffer structure
- Four priority level Quality Of Service (QOS) support (802.1p)
- CPPI 3.1 compliant DMA controllers
- Support for Audio/Video Bridging (P802.1Qav/D6.0)
- Support for IEEE 1588 Clock Synchronization (2008 Annex D and Annex F)
  - Timing FIFO and time stamping logic embedded in the subsystem
- Device Level Ring (DLR) Support
- Energy Efficient Ethernet (EEE) support (802.3az)
- Flow Control Support (802.3x)
- Address Lookup Engine (ALE)
  - 1024 total address entries plus VLANs
  - Wire rate lookup
  - Host controlled time-based aging
  - Multiple spanning tree support (spanning tree per VLAN)
  - L2 address lock and L2 filtering support
  - MAC authentication (802.1x)
  - Receive-based or destination-based multicast and broadcast rate limits
  - MAC address blocking
  - Source port locking
  - OUI (Vendor ID) host accept/deny feature
  - Remapping of priority level of VLAN or ports
- VLAN support
  - 802.1Q compliant
    - Auto add port VLAN for untagged frames on ingress
    - Auto VLAN removal on egress and auto pad to minimum frame size
- Ethernet Statistics:
  - EtherStats and 802.3Stats Remote network Monitoring (RMON) statistics gathering (shared)
  - Programmable statistics interrupt mask when a statistic is above one half its 32-bit value

- Flow Control Support (802.3x)
- Digital loopback and FIFO loopback modes supported
- Maximum frame size 2016 bytes (2020 with VLAN)
- 8k (2048 × 32) internal CPPI buffer descriptor memory
- Management Data Input/Output (MDIO) module for PHY Management
- Programmable interrupt control with selected interrupt pacing
- Emulation support
- Programmable Transmit Inter Packet Gap (IPG)
- Reset isolation (switch function remains active even in case of all device resets except for POR pin reset and ICEPICK cold reset)
- Full duplex mode supported in 10/100/1000 Mbps. Half-duplex mode supported only in 10/100 Mbps.
- IEEE 802.3 gigabit Ethernet conformant

For more information, see section *Gigabit Ethernet Switch (GMAC\_SW)* in chapter *Serial Communication Interfaces* of the device TRM.

#### **6.10.14 SDIO**

The SDIO host controller provides an interface between a local host (LH) such as a microprocessor unit or digital signal processor and SDIO cards. It handles SDIO transactions with minimal LH intervention.

The SDIO host controller deals with SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit, and checking for syntactical correctness.

The application interface can send every SDIO command and poll for the status of the adapter or wait for an interrupt request, which is sent back in case of exceptions or to warn of end of operation.

The application interface can read card responses or flag registers. It can also mask individual interrupt sources. All these operations can be performed by reading and writing control registers. The SDIO host controller also supports two slave DMA channels.

Compliance with standards:

- SDIO command/response sets and interrupt/read-wait suspend-resume operations as defined in the SD part E1 specification v3.00
- SD command/response sets as defined in the SD Physical Layer specification v3.01
- SD Host Controller Standard Specification sets as defined in the SD card specification Part A2 v3.00

Main features of the SD/SDIO host controllers:

- Flexible architecture allowing support for new command structure
- 32-bit wide access bus to maximize bus throughput
- Designed for low power
- Programmable clock generation
- L4 slave interface supports:
  - 32-bit data bus width
  - 8/16/32 bit access supported
  - 9-bit address bus width
  - Streaming burst supported only with burst length up to 7
  - WNP supported
- Built-in 1024-byte buffer for read or write
- Two DMA channels, one interrupt line
- Supported data transfer rates up to SDR25 mode
- The SDIO controller is connected to 1,8V/3.3V compatible I/Os to support 1,8V/3.3V signaling

The differences between the SDIO host controller and a standard SD host controller defined by the *SD Card Specification, Part A2, SD Host Controller Standard Specification*, v3.00 are:

- The clock divider in the SDIO host controller supports a wider range of frequency than specified in the SD Memory Card Specifications, v3.0. The SDIO host controller supports odd and even clock ratios.
- The SDIO host controller supports configurable busy time-out.
- There is no external LED control

For more information, see chapter *SDIO Controller* of the device TRM.

### 6.10.15 GPIO

The general-purpose interface combines four general-purpose input/output (GPIO) banks.

Each GPIO module provides 32 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 126 pins.

These pins can be configured for the following applications:

- Data input (capture)/output (drive)
- Keyboard interface with a debounce cell
- Interrupt generation in active mode upon the detection of external events. Detected events are processed by two parallel independent interrupt-generation submodules to support biprocessor operations.
- Wake-up request generation in idle mode upon the detection of external events

For more information, see chapter *General-Purpose Interface* of the device TRM.

### 6.10.16 ePWM

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The ePWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross coupling or sharing of resources has been avoided; instead, the ePWM is built up from smaller single channel modules with separate resources and that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

Each ePWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Two PWM outputs (EPWM1A and EPWM2B) that can be used in the following configurations:
  - Two independent PWM outputs with single-edge operation
  - Two independent PWM outputs with dual-edge symmetric operation
  - One independent PWM output with dual-edge asymmetric operation
- Asynchronous override control of PWM signals through software.
- Hardware-locked (synchronized) phase relationship on a cycle-by-cycle basis.
- Dead-band generation with independent rising and falling edge delay control.
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions.
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs.
- Programmable event prescaling minimizes CPU overhead on interrupts.
- PWM chopping by high-frequency carrier signal, useful for pulse transformer gate drives.

For more information, see section *Enhanced PWM (ePWM) Module* in chapter *Pulse-Width Modulation Subsystem* of the device TRM.

### 6.10.17 eCAP

Uses for eCAP include:

- Sample rate measurements of audio inputs
- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module includes the following features:

- 32-bit time base counter
- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single shot capture of up to four event time-stamps
- Continuous mode capture of time-stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All above resources dedicated to a single input pin
- When not used in capture mode, the ECAP module can be configured as a single channel PWM output

For more information, see section *Enhanced Capture (eCAP) Module* in chapter *Pulse-Width Modulation Subsystem* of the device TRM.

#### 6.10.18 eQEP

A single track of slots patterns the periphery of an incremental encoder disk. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position, and zero reference.

To derive direction information, the lines on the disk are read out by two different photo-elements that "look" at the disk pattern with a mechanical shift of 1/4 the pitch of a line pair between them. This shift is realized with a reticle or mask that restricts the view of the photo-element to the desired part of the disk lines. As the disk rotates, the two photo-elements generate signals that are shifted 90 degrees out of phase from each other. These are commonly called the quadrature QEPA and QEPB signals. The clockwise direction for most encoders is defined as the QEPA channel going positive before the QEPB channel.

The encoder wheel typically makes one revolution for every revolution of the motor or the wheel may be at a geared rotation ratio with respect to the motor. Therefore, the frequency of the digital signal coming from the QEPA and QEPB outputs varies proportionally with the velocity of the motor. For example, a 2000-line encoder directly coupled to a motor running at 5000 revolutions per minute (rpm) results in a frequency of 166.6 KHz, so by measuring the frequency of either the QEPA or QEPB output, the processor can determine the velocity of the motor.

For more information, see section *Enhanced Quadrature Encoder Pulse (eQEP) Module* in chapter *Pulse-Width Modulation Subsystem* of the device TRM.

### 6.11 On-Chip Debug

Debugging a system that contains an embedded processor involves an environment that connects high-level debugging software running on a host computer to a low-level debug interface supported by the target device. Between these levels, a debug and trace controller (DTC) facilitates communication between the host debugger and the debug support logic on the target chip.

The DTC is a combination of hardware and software that connects the host debugger to the target system. The DTC uses one or more hardware interfaces and/or protocols to convert actions dictated by the debugger user to JTAG® commands and scans that execute the core hardware.

The debug software and hardware components let the user control multiple central processing unit (CPU) cores embedded in the device in a global or local manner. This environment provides:

- Synchronized global starting and stopping of multiple processors
- Starting and stopping of an individual processor

- Each processor can generate triggers that can be used to alter the execution flow of other processors

System topics include but are not limited to:

- System clocking and power-down issues
- Interconnection of multiple devices
- Trigger channels

The device deploys Texas Instrument's CTools debug technology for on-chip debug and trace support. It provides the following features:

- External debug interfaces:
  - Primary debug interface - IEEE1149.1 (JTAG) or IEEE1149.7 (complementary superset of JTAG)
    - Used for debugger connection
    - Default mode is IEEE1149.1 but debugger can switch to IEEE1149.7 via an IEEE1149.7 adapter module
    - Controls ICEPick™ (generic test access port [TAP] for dynamic TAP insertion) to allow the debugger to access several debug resources through its secondary (output) JTAG ports (for more information, see section *ICEPick Secondary TAPs* in chapter *On-Chip Debug Support* of the Device TRM).
  - Debug (trace) port
    - Can be used to export processor or system trace off-chip (to an external trace receiver)
    - Can be used for cross-triggering with an external device
    - Configured through debug resources manager (DRM) module instantiated in the debug subsystem
    - For more information about debug (trace) port, see sections *Debug (Trace) Port* and *Concurrent Debug Modes* in chapter *On-Chip Debug Support* of the Device TRM.
- JTAG based processor debug on:
  - C66x in DSP1, DSP2
  - Cortex-M4 (x2) in IPU
- Dynamic TAP insertion
  - Controlled by ICEPick
  - For more information, see section *Dynamic TAP Insertion* in chapter *On-Chip Debug Support* of the Device TRM
- Power and clock management
  - Debugger can get the status of the power domain associated to each TAP.
  - Debugger may prevent the application software switching off the power domain.
  - Application power management behavior can be preserved during debug across power transitions.
  - For more information, see section *Power and Clock Management* in chapter *On-Chip Debug Support* of the Device TRM.
- Reset management
  - Debugger can configure ICEPick to assert, block, or extend the reset of a given subsystem.
  - For more information, see section *Reset Management* in chapter *On-Chip Debug Support* of the Device TRM.

- Cross-triggering
  - Provides a way to propagate debug (trigger) events from one processor, subsystem, or module to another:
    - Subsystem A can be programmed to generate a debug event, which can then be exported as a global trigger across the device.
    - Subsystem B can be programmed to be sensitive to the trigger line input and to generate an action on trigger detection.
  - Two global trigger lines are implemented
  - Device-level cross-triggering is handled by the XTRIG (TI cross-trigger) module implemented in the debug subsystem
  - For more information about cross-triggering, see section *Cross-Triggering* in chapter *On-Chip Debug Support* of the Device TRM.
- Suspend
  - Provides a way to stop a closely coupled hardware process running on a peripheral module when the host processor enters debug state
  - For more information about suspend, see section *Suspend* in chapter *On-Chip Debug Support* of the Device TRM.
- Processor trace
  - C66x (DSP) processor trace is supported
  - Two exclusive trace sinks:
    - CoreSight Trace Port Interface Unit (CS\_TPIU) – trace export to an external trace receiver
  - For more information, see section *Processor Trace* in chapter *On-Chip Debug Support* of the Device TRM.

- System instrumentation (trace)
  - Supported by a CTools System Trace Module (CT\_STM), implementing MIPI System Trace Protocol (STP) (rev 2.0)
  - Real-time software trace
    - System-on-chip (SoC) software instrumentation through CT\_STM (STP2.0)
  - OCP watchpoint (OCP\_WP\_NOC)
    - OCP target traffic monitoring: OCP\_WP\_NOC can be configured to generate a trigger upon watchpoint match (that is, when target transaction attributes match the user-defined attributes).
    - SoC events trace
    - DMA transfer profiling
  - Statistics collector (performance probes)
    - Computes traffic statistics within a user-defined window and periodically reports to the user through the CT\_STM interface
    - Embedded in the L3\_MAIN interconnect
    - 10 instances:
      - 1 instance dedicated to target (SDRAM) load monitoring
      - 9 instances dedicated to master latency monitoring
  - Power-management events profiling (PM instrumentation [PMI])
    - Monitoring major power-management events. The PM state changes are handled as generic events and encapsulated in STP messages.
  - Clock-management events profiling CM instrumentation [CMI] for CM\_CORE\_AON clocks
    - Monitoring major clock management events. The CM state changes are handled as generic events and encapsulated in STP messages.
    - One instances
      - CM1 Instrumentation (CMI1) module mapped in the PD\_CORE\_AON power domain
  - For more information, see section *System Instrumentation* in chapter *On-Chip Debug Support* of the Device TRM.
- Performance monitoring
  - Supported by subsystem counter timer module (SCTM) for IPU

For more information, see chapter *On-Chip Debug Support* of the device TRM.

## 7 Applications, Implementation, and Layout

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test design implementation to confirm system functionality.

### 7.1 Introduction

This chapter is intended to communicate, guide and illustrate a PCB design strategy resulting in a PCB that can support TI's latest Application Processor. This Processor is a high-performance processor designed for automotive Infotainment based on enhanced OMAP™ architecture integrated on a 28-nm CMOS process technology.

These guidelines first focus on designing a robust Power Delivery Network (PDN) which is essential to achieve the desirable high performance processing available on Device. The general principles and step-by-step approach for implementing good power integrity (PI) with specific requirements will be described for the key Device power domains.

TI strongly believes that simulating a PCB's proposed PDN is required for first pass PCB design success. Key Device processor high-current power domains need to be evaluated for Power Rail IR Drop, Decoupling Capacitor Loop-Inductance and Power Rail Target Impedance. Only then can a PCB's PDN performance be truly accessed by comparing these model PI parameters vs. TI's recommended values. Ultimately for any high-volume product, TI recommends conducting a "Processor PDN Validation" test on prototype PCBs across processor "split lots" to verify PDN robustness meets desired performance goals for each customer's worst-case scenario. Please contact your TI representative to receive guidance on PDN PI modeling and validation testing.

Likewise, the methodology and requirements needed to route Device high-speed, differential interfaces , single-ended interfaces (i.e. DDR3, QSPI) and general purpose interfaces using LVCMOS drivers that meet timing requirements while minimizing signal integrity (SI) distortions on the PCB's signaling traces. Signal trace lengths and flight times are aligned with FR-4 standard specification for PCBs.

Several different PCB layout stack-up examples have been presented to illustrate a typical number of layers, signal assignments and controlled impedance requirements. Different Device interface signals demand more or less complexity for routing and controlled impedance stack-ups. Optimizing the PCB's PDN stack-up needs with all of these different types of signal interfaces will ultimately determine the final layer count and layer assignments in each customer's PCB design.

This guideline must be used as a supplement in complement to TI's Application Processor, Power Management IC (PMIC) and Audio Companion components along with other TI component technical documentation (i.e. Technical Reference Manual, Data Manual, Data Sheets, Silicon Errata, Pin-Out Spreadsheet, Application Notes, etc.).

### 注

Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, for customer boards. The data described in this appendix are intended as guidelines only.

### 注

These PCB guidelines are in a draft maturity and consequently, are subject to change depending on design verification testing conducted during IC development and validation. Note also that any references to Application Processor's ballout or pin muxing are subject to change following the processor's ballout maturity.

### 7.1.1 Initial Requirements and Guidelines

Unless otherwise specified, the characteristic impedance for single-ended interfaces is recommended to be between 35  $\Omega$  and 65  $\Omega$  to minimize the overshoot or undershoot on far-end loads.

Characteristic impedance for differential interfaces must be routed as differential traces on the same layer. The trace width and spacing must be chosen to yield the recommended differential impedance. For more information see [7.5.1](#).

The PDN must be optimized for low trace resistance and low trace inductance for all high-current power nets from PMIC to the device.

An external interface using a connector must be protected following the IEC61000-4-2 level 4 system ESD.

## 7.2 Power Optimizations

This section describes the necessary steps for designing a robust Power Distribution Network (PDN):

- [7.2.1, Step 1](#): PCB Stack-up
- [7.2.2, Step 2](#): Physical Placement
- [7.2.3, Step 3](#): Static Analysis
- [7.2.4, Step 4](#): Frequency Analysis

### 7.2.1 Step 1: PCB Stack-up

The PCB stack-up (layer assignment) is an important factor in determining the optimal performance of the power distribution system. An optimized PCB stack-up for higher power integrity performance can be achieved by following these recommendations:

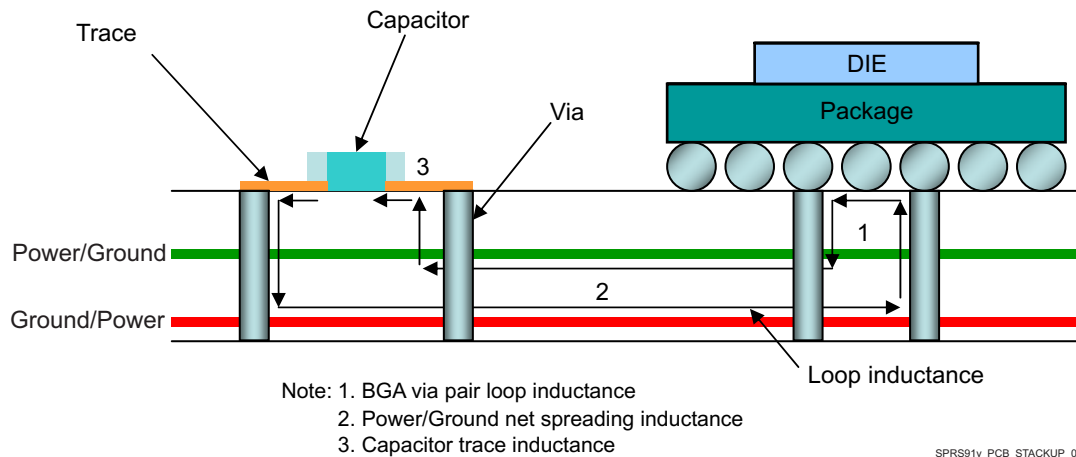
- Power and ground plane pairs must be closely coupled together. The capacitance formed between the planes can decouple the power supply at high frequencies. Whenever possible, the power and ground planes must be solid to provide continuous return path for return current.
- Use a thin dielectric between the power and ground plane pair. Capacitance is inversely proportional to the separation of the plane pair. Minimizing the separation distance (the dielectric thickness) maximizes the capacitance.
- Optimize the power and ground plane pair carrying high current supplies to key component power domains as close as possible to the same surface where these components are placed (see [Figure 7-1](#)). This will help to minimize "loop inductance" encountered between supply decoupling capacitors and component supply inputs and between power and ground plane pairs.

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#### 注

1-2oz Cu weight for power / ground plane is preferred to enable better PCB heat spreading, helping to reduce Processor junction temperatures. In addition, it is preferable to have the power / ground planes be adjacent to the PCB surface on which the Processor is mounted.

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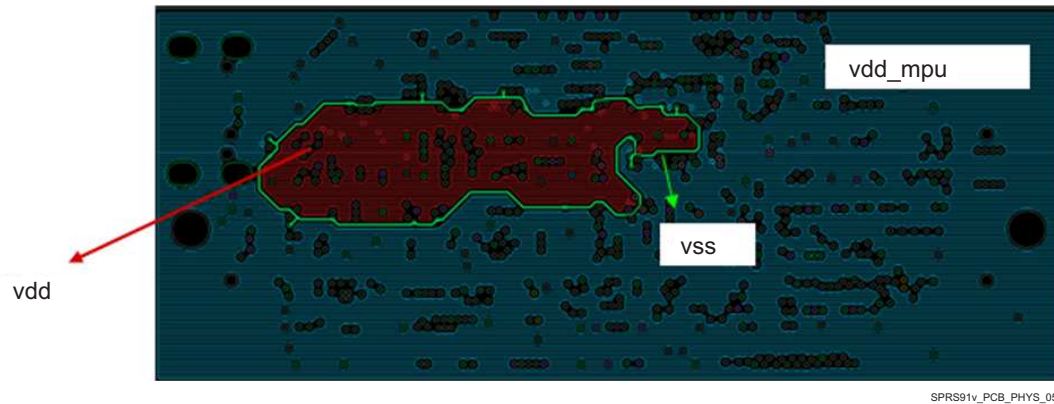
**FIG 7-1. Minimize Loop Inductance With Proper Layer Assignment**

The placement of power and ground planes in the PCB stackup (determined by layer assignment) has a significant impact on the parasitic inductances of power current path as shown in FIG 7-1. For this reason, it is recommended to consider layer order in the early stages of the PCB PDN design cycle, putting high-priority supplies in the top half of the stackup (assuming high load and priority components are mounted on the top-side of PCB) and low-priority supplies in the bottom half of the stackup as shown in the examples below (vias have parasitic inductances which impact the bottom layers more, so it is advised to put the sensitive and high-priority power supplies on the top/same layers).

## 7.2.2 Step 2: Physical Placement

A critical step in designing an optimized PDN is that proper care must be taken to making sure that the initial floor planning of the PCB layout is done with good power integrity design guidelines in mind. The following points are important for optimizing a PCB's PDN:

- Minimizing the physical distance between power sources and key high load components is the first step toward optimization. Placing source and load components on the same side of the PCB is desirable. This will minimize via inductance impact for high current loads and steps
- External trace routing between components must be as wide as possible. The wider the traces, the lower the DC resistance and consequently the lower the static IR drop.
- Whenever possible for the internal layers (routing and plane), wide traces and copper area fills are preferred for PDN layout. The routing of power nets in plane provide for more interplane capacitance and improved high frequency performance of the PDN.
- Whenever possible, use a via to component pin/pad ratio of 1:1 or better (i.e. especially decoupling capacitors, power inductors and current sensing resistors). Do not share vias among multiple capacitors for connecting power supply and ground planes.
- Placement of vias must be as close as possible or even within a component's solder pad if the PCB technology you are using provides this capability.
- To avoid any "ampacity" issue – maximum current-carrying capacity of each transitional via should be evaluated to determine the appropriate number of vias required to connect components.  
Adding vias to bring the "via-to-pad" ratio to 1:1 will improve PDN performance.
- For noise sensitive power supplies (i.e. Phase Lock-Loops, analog signals like audio and video), a Gnd shield can be used to isolate coplanar supplies that may have high step currents or high frequency switching transitions from coupling into low-noise supplies.



**Figure 7-2. Coplanar Shielding of Power Net Using Ground Guard-band**

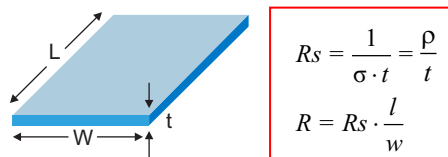
### 7.2.3 Step 3: Static Analysis

Delivering reliable power to circuits is always of critical importance because voltage drops (also known as IR drops) can happen at every level within an electronic system, on-chip, within a package, and across the board. Robust system performance can only be ensured by understanding how the system elements will perform under typical stressful Use Cases. Therefore, it is a good practice to perform a Static or DC Analysis.

Static or DC analysis and design methodology results in a PDN design that minimizes voltage or IR drops across power and ground planes, traces and vias. This ensures the application processor's internal transistors will be operating within their specified voltage ranges for proper functionality. The amount of IR drop that will be encountered is based upon amount power drawn for a desired Use Case and PCB trace (widths, geometry and number of parallel traces) and via (size, type and number) characteristics.

Components that are distant from their power source are particularly susceptible to IR drop. Designs that rely on battery power must minimize voltage drops to avoid unacceptable power loss that can negatively impact system performance. Early assessments a PDN's static (DC) performance helps to determine basic power distribution parameters such as best system input power point, optimal PCB layer stackup, and copper area needed for load currents.

The resistance  $R_s$  of a plane conductor for a unit length and unit width is called the **surface resistivity** (ohms per square).

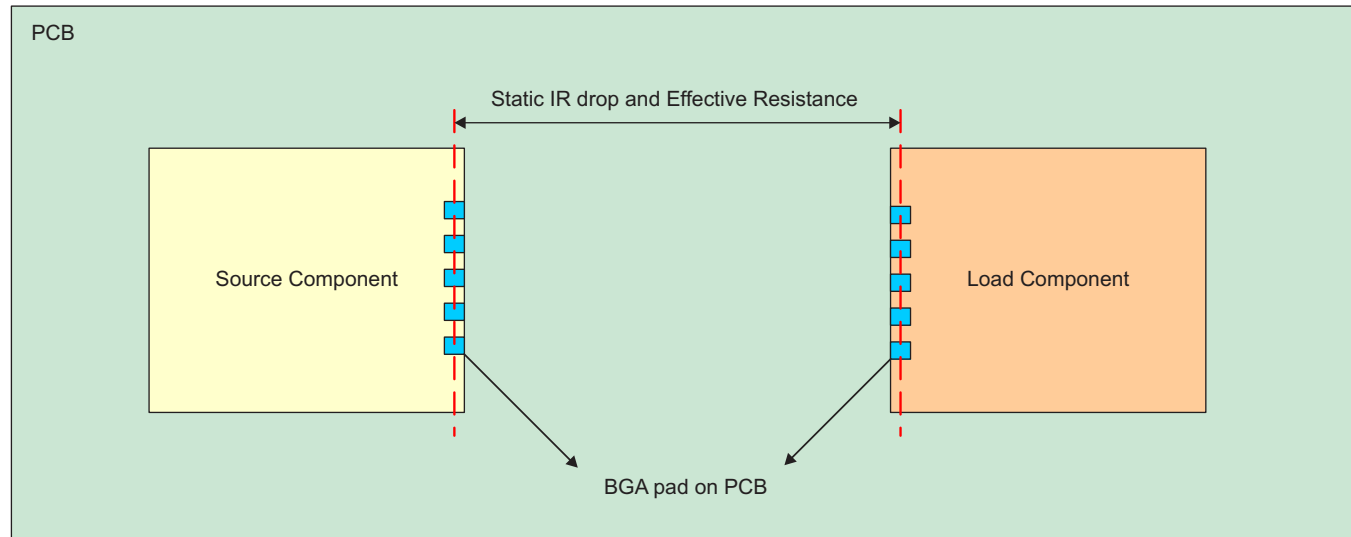


**Figure 7-3. Depiction of Sheet Resistivity and Resistance**

Ohm's Law ( $V = I \times R$ ) relates conduction current to voltage drop. At DC, the relation coefficient is a constant and represents the resistance of the conductor. Even current carrying conductors will dissipate power at high currents even though their resistance may be very small. Both voltage drop and power dissipation are proportional to the resistance of the conductor.

Figure 7-4 shows a PCB-level static IR drop budget defined between the power management device (PMIC) pins and the application processor's balls when the PMIC is supplying power.

- It is highly recommended to physically place the PMIC as close as possible to the processor and on the same side. The orientation of the PMIC vs. the processor should be aligned to minimize distance for the highest current rail.



SPRS906\_PCB\_STATIC\_02

#### 图 7-4. Static IR Drop Budget for PCB Only

The system-level IR drop budget is made up of three portions: on-chip, package, and PCB board. Static IR or dc analysis/design methodology consists of designing the PDN such that the voltage drop (under dc operating conditions) across power and ground pads of the transistors of the application processor device is within a specified value of the nominal voltage for proper functionality of the device.

A PCB system-level voltage drop budget for proper device functionality is typically 1.5% of nominal voltage. For a 1.35-V supply, this would be  $\leq 20$  mV.

To accurately analyze PCB static IR drop, the actual geometry of the PDN must be modeled properly and simulated to accurately characterize long distribution paths, copper weight impacts, electro-migration violations of current-carrying vias, and "Swiss-cheese" effects via placement has on power rails. It is recommended to perform the following analyses:

- Lumped resistance/IR drop analysis
- Distributed resistance/IR drop analysis

#### 注

The PMIC companion device supporting Processor has been designed with voltage sensing feedback loop capabilities that enable a remote sense of the SMPS output voltage at the point of use.

The NOTE above means the SMPS feedback signals and returns must be routed across PCB and connected to the Device input power ball for which a particular SMPS is supplying power. This feedback loop provides compensation for some of the voltage drop encountered across the PDN within limits. As such, the effective resistance of the PDN within this loop should be determined in order to optimize voltage compensation loop performance. The resistance of two PDN segments are of interest: one from the power inductor/bulk power filtering capacitor node to the Processor's input power and second is the entire PDN route from SMPS output pin/ball to the Processor input power.

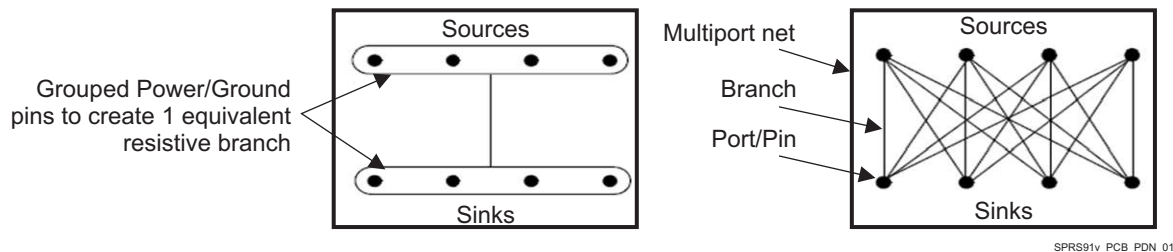
In the following sections each methodology is described in detail and an example has been provided of analysis flow that can be used by the PCB designer to validate compliance to the requirements on their PCB PDN design.

### 7.2.3.1 PDN Resistance and IR Drop

Lumped methodology consists of grouping all of the power pins on both the PMIC (voltage source) and processor (current sink) devices. Then the PMIC source is set to an expected Use Case voltage level and the processor load has its Use Case current sink value set as well. Now the lumped/effective resistance for the power rail trace/plane routes can be determined based upon the actual layout's power rail etch width, shape, length, via count and placement. Figure 7-5 illustrates the pin-grouping/lumped concept.

The lumped methodology consists of importing the PCB layout database (from Cadence Allegro tool or any other layout design tool) into the static IR drop modeling and simulation tool of preference for the PCB designer. This is followed by applying the correct PCB stack-up information (thickness, material properties) of the PCB dielectric and metallization layers. The material properties of dielectric consist of permittivity (Dk) and loss tangent (Df).

For the conductor layers, the correct conductivity needs to be programmed into the simulation tool. This is followed by pin-grouping of the power and ground nets, and applying appropriate voltage/current sources. The current and voltage information can be obtained from the power and voltage specifications of the device under different operating conditions / Use Cases.



**Figure 7-5. Pin-grouping concept: Lumped and Distributed Methodologies**

### 7.2.4 Step 4: Frequency Analysis

Delivering low noise voltage sources are very important to allowing a system to operate at the lowest possible Operational Performance Point (OPP) for any one Use Case. An OPP is a combination of the supply voltage level and clocking rate for key internal processor domains. A SCH and PCB designed to provide low noise voltage supplies will then enable the processor to enter optimal OPPs for each Use Case that in turn will minimize power dissipation and junction temperatures on-die. Therefore, it is a good engineering practice to perform a Frequency Analysis over the key power domains.

Frequency analysis and design methodology results in a PDN design that minimizes transient noise voltages at the processor's input power balls. This allows the processor's internal transistors to operate near the minimum specified operating supply voltage levels. To accomplish this one must evaluate how a voltage supply will change due to impedance variations over frequency. This analysis will focus on the decoupling capacitor network (VDD\_xxx and VSS/Gnd rails) at the load. Sufficient capacitance with a distribution of self-resonant points will provide for an overall lower impedance vs frequency response for each power domain.

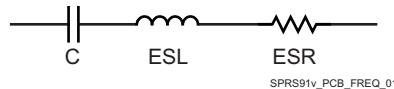
Decoupling components that are distant from their load's input power are susceptible to encountering spreading loop inductance from the PCB design. Early analysis of each key power domain's frequency response helps to determine basic decoupling capacitor placement, optimal footprint, layer assignment, and types needed for minimizing supply voltage noise/fluctuations due to switching and load current transients.

#### 注

Evaluation of loop inductance values for decoupling capacitors placed ~300mils closer to the load's input power balls has shown an 18% reduction in loop inductance due to reduced distance.

- Decoupling capacitors must be carefully placed in order to minimize loop inductance impact on supply voltage transients. A real capacitor has characteristics not only of capacitance but also inductance and resistance.

Figure 7-6 shows the parasitic model of a real capacitor. A real capacitor must be treated as an RLC circuit with effective series resistance (ESR) and effective series inductance (ESL).



**Figure 7-6. Characteristics of a Real Capacitor With ESL and ESR**

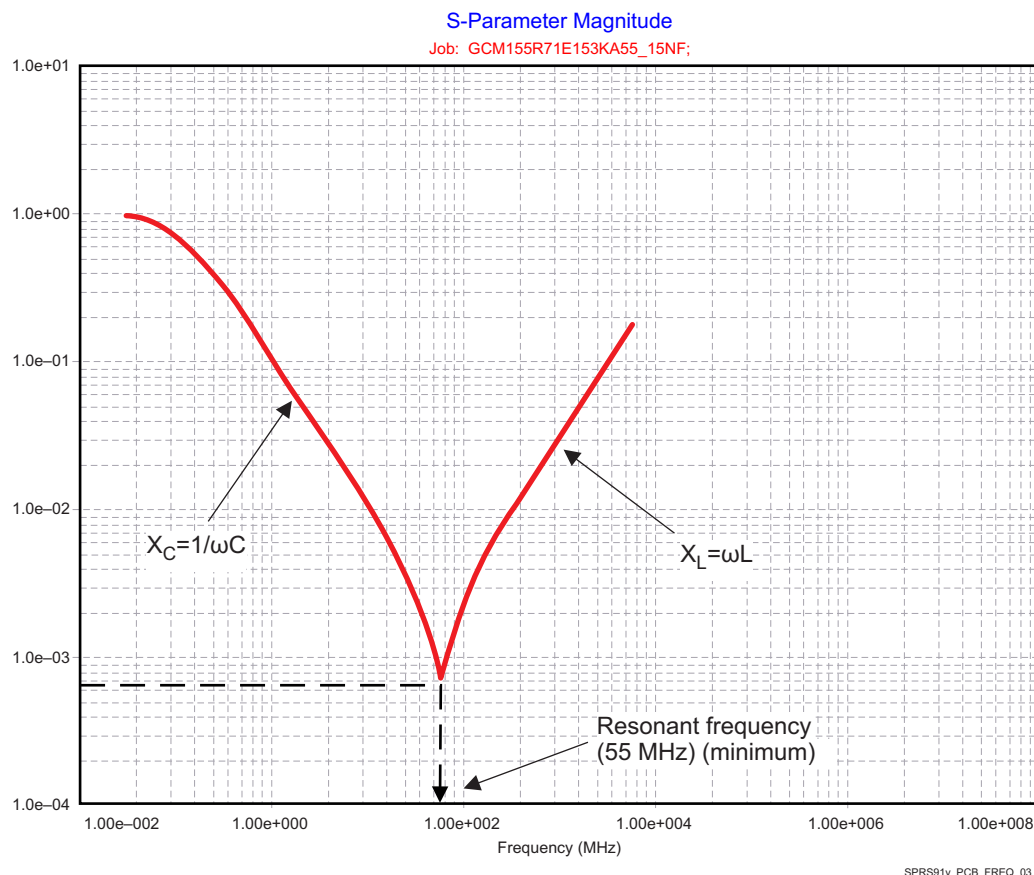
The magnitude of the impedance of this series model is given as:

$$|Z| = \sqrt{ESR^2 + \left( \omega ESL - \frac{1}{\omega C} \right)^2}$$

where :  $\omega = 2\pi f$

**Figure 7-7. Series Model Impedance Equation**

Figure 7-8 shows the resonant frequency response of a typical capacitor with a self-resonant frequency of 55 MHz. The impedance of the capacitor is a combination of its series resistance and reactive capacitance and inductance as shown in the equation above.



**Figure 7-8. Typical Impedance Profile of a Capacitor**

Because a capacitor has series inductance and resistance that impacts its effectiveness, it is important that the following recommendations are adopted in placing capacitors on the PDN.

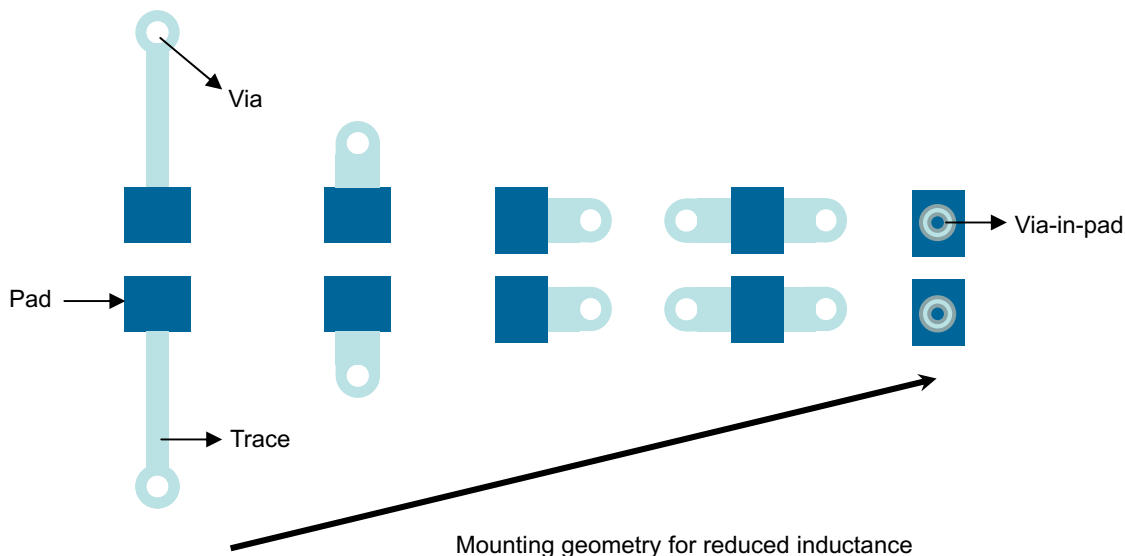
Wherever possible, mount the capacitor with the geometry that minimizes the mounting inductance and resistance. This was shown earlier in [Figure 7-1](#). The capacitor mounting inductance and resistance values include the inductance and resistance of the pads, trace, and vias. Whenever possible, use footprints that have the lowest inductance configuration as shown in [Figure 7-9](#).

The length of a trace used to connect a capacitor has a big impact on parasitic inductance and resistance of the mounting. This trace must be as short and as wide as possible. wherever possible, minimize distance to supply and Gnd vias by locating vias nearby or within the capacitor's solder pad landing. Further improvements can be made to the mounting by placing vias to the side of capacitor lands or doubling the number of vias as shown in [Figure 7-9](#). If the PCB manufacturing processes allow it and if cost-effective, via-in-pad (VIP) geometries are strongly recommended.

In addition to mounting inductance and resistance associated with placing a capacitor on the PCB, the effectiveness of a decoupling capacitor also depends on the spreading inductance and resistance that the capacitor sees with respect to the load. The spreading inductance and resistance is strongly dependent on the layer assignment in the PCB stack-up. Therefore, try to minimize X, Y and Z dimensions where the Z is due to PCB thickness (as shown in [Figure 7-9](#)).

From left (highest inductance) to right (lowest inductance) the capacitor footprint types shown in [Figure 7-9](#) are known as:

- 2-via, Skinny End Exit (2vSEE)
- 2-via, Wide End Exit (2vWEE)
- 2-via, Wide Side Exit (2vWSE)
- 4-via, Wide Side Exit (4vWSE)
- 2-via, In-Pad (2vVIP)



SPRS91v\_PCB\_FREQ\_04

**Figure 7-9. Capacitor Placement Geometry for Improved Mounting Inductance**

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Evaluation of loop inductance values for decoupling capacitor footprints 2vSEE (worst case) vs 4vWSE (2nd best) has shown a 30% reduction in inductance when 4vWSE footprint was used in place of 2vSEE.

### Decoupling Capacitor (Dcap) Strategy:

1. Use lowest inductance footprint and trace connection scheme possible for given PCB technology and layout area in order to minimize Dcap loop inductance to power pin as much as possible (see [Figure 7-9](#)).
2. Place Dcaps on "same-side" as component within their power plane outline to minimize "decoupling loop inductance". Target distance to power pin should be less than ~500mils depending upon PCB layout characteristics (plane's layer assignment and solid nature). Use PI modeling CAD tool to verify minimum inductance for top vs bottom-side placement.
3. Place Dcaps on "opposite-side" as component within their power plane outline if "same-side" is not feasible or if distance to power pin is greater than ~500mils for top-side location. Use PI modeling CAD tool to verify minimum inductance for top vs bottom-side placement.
4. Use minimum 10mil trace width for all voltage and gnd planes connections (i.e. Dcap pads, component power pins, etc.).
5. Place all voltage and gnd plane vias "as close as possible" to point of use (i.e. Dcap pads, component power pins, etc.).
6. Use a "Power/Gnd pad/pin to via" ratio of 1:1 whenever possible. Do not exceed 2:1 ratio for small number of vias within restricted PCB areas (i.e. underneath BGA components).

Frequency analysis for the CORE power domain (vdd) has yielded the Impedance vs Frequency responses shown in [7.3.8.2](#), vdd Example Analysis.

## **7.2.5 System ESD Generic Guidelines**

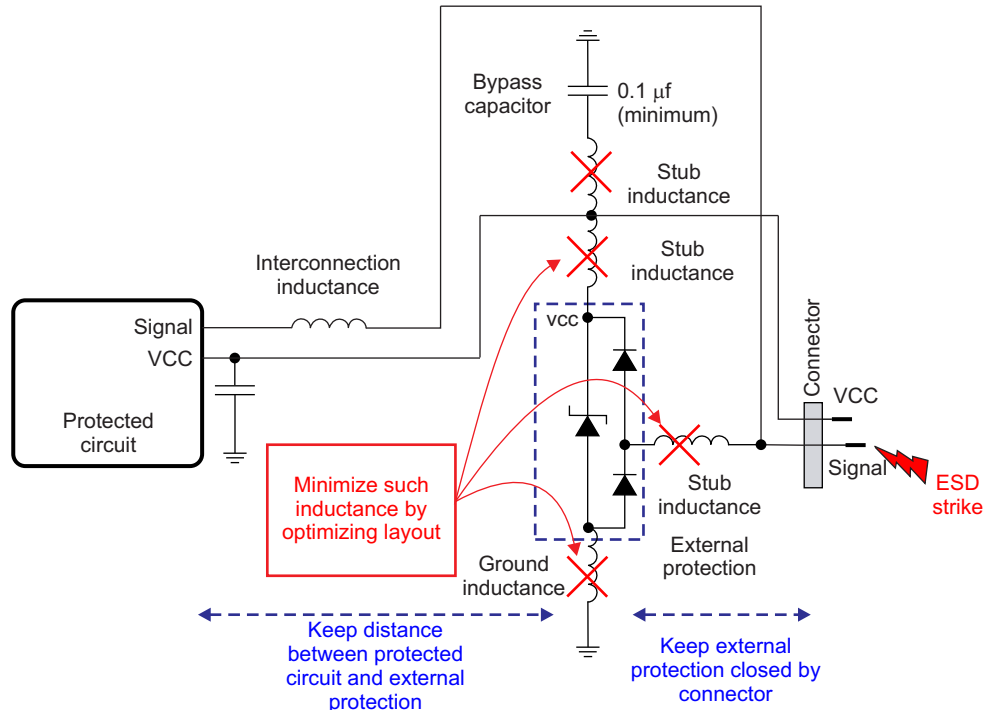
### **7.2.5.1 System ESD Generic PCB Guideline**

Protection devices must be placed close to the ESD source which means close to the connector. This allows the device to subtract the energy associated with an ESD strike before it reaches the internal circuitry of the application board.

To help minimize the residual voltage pulse that will be built-up at the protection device due to its nonzero turn-on impedance, it is mandatory to route the ESD device with minimum stub length so that the low-resistive, low-inductive path from the signal to the ground is granted and not increasing the impedance between signal and ground.

For ESD protection array being railed to a power supply when no decoupling capacitor is available in close vicinity, consider using a decoupling capacitor ( $\geq 0.1 \mu\text{F}$ ) tight to the VCC pin of the ESD protection. A positive strike will be partially diverted to this capacitance resulting in a lower residual voltage pulse.

Ensure that there is sufficient metallization for the supply of signals at the interconnect side (VCC and GND in [Figure 7-10](#)) from connector to external protection because the interconnect may see between 15-A to 30-A current in a short period of time during the ESD event.



SPRS91v\_PCB\_ESD\_01

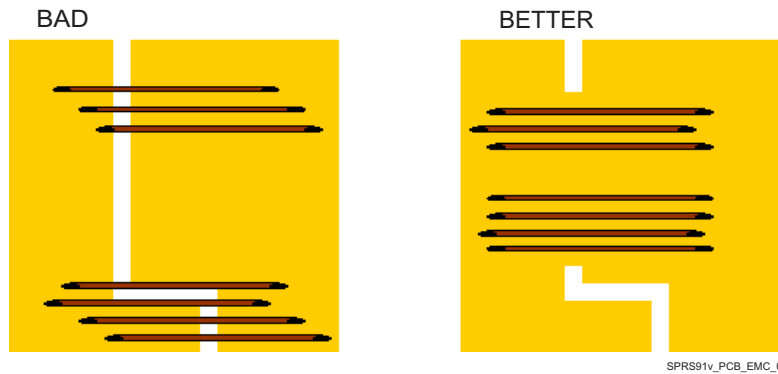
**図 7-10. Placement Recommendation for an ESD External Protection**

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To ensure normal behavior of the ESD protection (unwanted leakage), it is better to ground the ESD protection to the board ground rather than any local ground (example isolated shield or audio ground).

### 7.2.5.2 Miscellaneous EMC Guidelines to Mitigate ESD Immunity

- Avoid running critical signal traces (clocks, resets, interrupts, control signals, and so forth) near PCB edges.
- Add high frequency filtering: Decoupling capacitors close to the receivers rather than close to the drivers to minimize ESD coupling.
- Put a ground (guard) ring around the entire periphery of the PCB to act as a lightning rod.
- Connect the guard ring to the PCB ground plane to provide a low impedance path for ESD-coupled current on the ring.
- Fill unused portions of the PCB with ground plane.
- Minimize circuit loops between power and ground by using multilayer PCB with dedicated power and ground planes.
- Shield long line length (strip lines) to minimize radiated ESD.
- Avoid running traces over split ground planes. It is better to use a bridge connecting the two planes in one area.



✎ 7-11. Trace Examples

- Always route signal traces and their associated ground returns as close to one another as possible to minimize the loop area enclosed by current flow:
  - At high frequencies current follows the path of least inductance.
  - At low frequencies current flows through the path of least resistance.

### 7.2.5.3 ESD Protection System Design Consideration

ESD protection system design consideration is covered in of this document. The following are additional considerations for ESD protection in a system.

- Metallic shielding for both ESD and EMI
- Chassis GND isolation from the board GND
- Air gap designed on board to absorb ESD energy
- Clamping diodes to absorb ESD energy
- Capacitors to divert ESD energy
- The use of external ESD components on the DP/DM lines may affect signal quality and are not recommended.

### 7.2.6 EMI / EMC Issues Prevention

All high-speed digital integrated circuits can be sources of unwanted radiation, which can affect nearby sensitive circuitry and cause the final product to have radiated emissions levels above the limits allowed by the EMC regulations if some preventative steps are not taken.

Likewise, analog and digital circuits can be susceptible to interference from the outside world and picked up by the circuitry interconnections.

To minimize the potential for EMI/EMC issues, the following guidelines are recommended to be followed.

#### 7.2.6.1 Signal Bandwidth

To evaluate the frequency of a digital signal, an estimated rule of thumb is to consider its bandwidth  $f_{BW}$  with respect to its rise time,  $t_R$ :

$$f_{BW} \approx 0.35 / t_R$$

This frequency actually corresponds to the break point in the signal spectrum, where the harmonics start to decay at 40 dB per decade instead of 20 dB per decade.

## 7.2.6.2 Signal Routing

### 7.2.6.2.1 Signal Routing—Sensitive Signals and Shielding

Keep radio frequency (RF) sensitive circuitry (like GPS receivers, GSM/WCDMA, Bluetooth/WLAN transceivers, frequency modulation (FM) radio) away from high-speed ICs (the device, power and audio manager, chargers, memories, and so forth) and ideally on the opposite side of the PCB. For improved protection it is recommended to place these emission sources in a shield can. If the shield can have a removable lid (two-piece shield), ensure there is low contact impedance between the fence and the lid. Leave some space between the lid and the components under it to limit the high-frequency currents induced in the lid. Limit the shield size to put any potential shield resonances above the frequencies of interest; see [Figure 7-8](#), *Typical Impedance Profile of a Capacitor*.

### 7.2.6.2.2 Signal Routing—Outer Layer Routing

In case there is a need to use the outer layers for routing outside of shielded areas, it is recommended to route only static signals and ensure that these static signals do not carry any high-frequency components (due to parasitic coupling with other signals). In case of long traces, make provision for a bypass capacitor near the signal source.

Routing of high-frequency clock signals on outer layers, even for a short distance, is discouraged, because their emissions energy is concentrated at the discrete harmonics and can become significant even with poor radiators.

Coplanar shielding of traces on outer layers (placing ground near the sides of a track along its length) is effective only if the distance between the trace sides and the ground is smaller than the trace height above the ground reference plane. For modern multilayer PCBs this is often not possible, so coplanar shielding will not be effective. Do not route high-frequency traces near the periphery of the PCB, as the lack of a ground reference near the trace edges can increase EMI: see [7.2.6.3](#), *Ground Guidelines*.

## 7.2.6.3 Ground Guidelines

### 7.2.6.3.1 PCB Outer Layers

Ideally the areas on the top and bottom layers of the PCB that are not enclosed by a shield should be filled with ground after the routing is completed and connected with an adequate number of vias to the ground on the inner ground planes.

### 7.2.6.3.2 Metallic Frames

Ensure that all metallic parts are well connected to the PCB ground (like LCD screens metallic frames, antennas reference planes, connector cages, flex cables grounds, and so forth). If using flex PCB ribbon cables to bring high-frequency signals off the PCB, ensure they are adequately shielded (coaxial cables or flex ribbons with a solid reference ground).

### 7.2.6.3.3 Connectors

For high-frequency signals going to connectors choose a fully shielded connector, if possible (for example, SD card connectors). For signals going to external connectors or which are routed over long distances, it is recommended to reduce their bandwidth by using low-pass filters (resistor, capacitor (RC) combinations or lossy ferrite inductors). These filters will help to prevent emissions from the board and can also improve the immunity from external disturbances.

### 7.2.6.3.4 Guard Ring on PCB Edges

The major advantage of a multilayer PCB with ground-plane is the ground return path below each and every signal or power trace.

As shown in [Figure 7-12](#) the field lines of the signal return to PCB ground as long as an infinite ground is available.

Traces near the PCB-edges do not have this infinite ground and therefore may radiate more than the others. Thus, signals (clocks) or power traces (core power) identified to be critical must not be routed in the vicinity of PCB edges, or, if not avoidable, must be accompanied by a guard ring on the PCB edge.

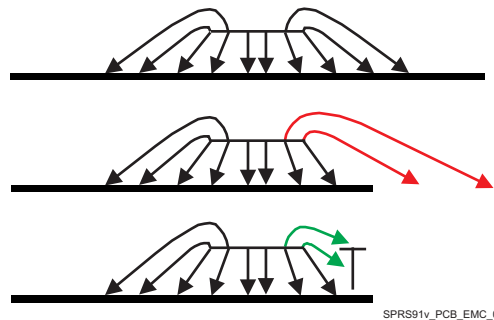


FIG 7-12. Field Lines of a Signal Above Ground



FIG 7-13. Guard Ring Routing

The intention of the guard ring is that HF-energy, that otherwise would have been emitted from the PCB edge, is reflected back into the board where it partially will be absorbed. For this purpose ground traces on the borders of all layers (including power layer) must be applied as shown in FIG 7-13.

As these traces must have the same (HF-) potential as the ground plane they must be connected to the ground plane at least every 10 mm.

#### 7.2.6.3.5 Analog and Digital Ground

For the optimum solution, the AGND and the DGND planes must be connected together at the power supply source in a same point. This ensures that both planes are at the same potential, while the transfer of noise from the digital to the analog domain is minimized.

### 7.3 Core Power Domains

This section provides boundary conditions and theoretical background to be applied as a guide for optimizing a PCB design. The decoupling capacitor and PDN characteristics tables shown below give recommended capacitors and PCB parameters to be followed for schematic and PCB designs. Board designs that meet the static and dynamic PDN characteristics shown in tables below will be aligned to the expected PDN performance needed to optimize SoC performance.

#### 7.3.1 General Constraints and Theory

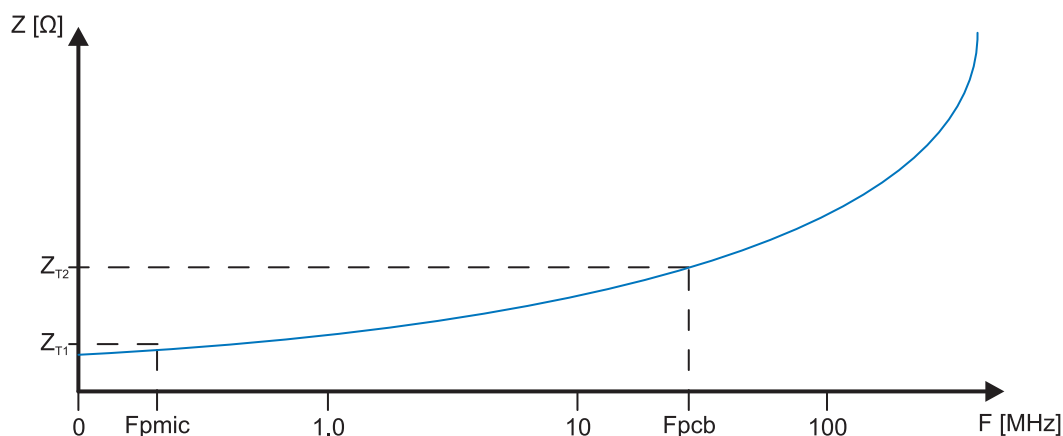
- Max PCB static/DC voltage drop (IRd) budget of **1.5% of supply voltage** when using PMICs **without remote sensing** as measured from PMIC's power inductor and filter capacitor node to Processor input including any ground return losses.
- Max PCB static/DC voltage drop (IRd) budget can be relaxed to **7.5% of supply voltage** when using TI recommended PMICs **with remote sensing** at the load as measured from PMIC's power inductor and filter capacitor node to Device's supply input including any ground return losses.

- PMIC component DM and guidelines should be referenced for the following:
  - Routing remote feedback sensing to optimize per each SMPS's implementation
  - Selecting power filtering capacitor values and PCB placement.
- Max Total Effective Resistance ( $R_{\text{eff}}$ ) budget can range from **4 – 100mΩ** for key Device power rails not including ground returns depending upon maximum load currents and maximum DC voltage drop budget (as discussed above).
- Max Device supply input voltage difference budget of **5mV** under max current loading shall be maintained across all balls connected to a common power rail. This represents any voltage difference that may exist between a remote sense point to any power input.
- Max PCB Loop Inductance (LL) budget between Device's power inputs and local bulk and high frequency decoupling capacitors including ground returns should range from **0.4 – 2.5nH depending upon maximum transient load currents.**
- Max PCB dynamic/AC peak-to-peak transient noise voltage budgets between PMIC and Device including ground returns are as follows:
  - **+/-3% of nominal supply voltage** for frequencies below the PMIC bandwidth (typ Fpmic ~ 200kHz)
  - **+/-5% of nominal supply voltage** for frequencies between Fpmic to Fpcb (typ 20 – 100MHz)
- Max PCB Impedance (Z) vs Frequency (F) budget between Device's power inputs and PMIC's output power filter node including ground return is determined by applying the Frequency Domain Target Impedance Method to determine the PCB's maximum frequency of interest (Fpcb). Ideally a properly designed and decoupled PDN will exhibit smoothly increasing Z vs. F curve. There are 2 general regions of interest as can be seen in [Figure 7-14](#).
  - 1<sup>st</sup> area is from DC (0Hz) up to Fpmic (typ a few 100 kHz) where a PMIC's transient response characteristic (i.e. Switching Freq, Compensation Loop BW) dominate. A PDN's Z is typically very low due to power filtering and bulk capacitor values when PDN has very low trace resistance (i.e. good Reff performance). The goal is to maintain a smoothly increasing Z that is less than Zt1 over this low frequency range. This will ensure that a max transient current event will not cause a voltage drop more than the PMIC's current step response can support (typ 3%).
  - 2<sup>nd</sup> area is from Fpmic up to Fpcb (typ 20-100MHz) where a PCB's inherent characteristics (i.e. parasitic capacitance, planar spreading inductances) dominate. A PDN's Z will naturally increase with frequency. At frequencies between Fpmic up to Fpcb, the goal is to maintain a smoothly increasing Z to be less than Zt2. This will ensure that the high frequency content of a max transient current event will not cause a voltage drop to be more than 5% of the min supply voltage.

$$Z_T = \frac{\text{Max Voltage Rail Drop}^{\text{Note1}}}{\text{Max Transient Current}^{\text{Note2}}}$$

$$Z_{T1} = \frac{(\text{Min Voltage}) \times (\text{PMIC's Step Responce})}{(\sim 50\% \text{ of Max DC Current})} = \frac{V_{\text{min}} \times 3\%(\text{typ})}{I_{\text{max}} \times \sim 50\%}$$

$$Z_{T2} = \frac{(\text{Min Voltage}) \times (\text{High-Freq Transient Noise})}{(\sim 50\% \text{ of Max DC Current})} = \frac{V_{\text{min}} \times 5\%(\text{typ})}{I_{\text{max}} \times \sim 50\%}$$



PCB\_CPD\_8

图 7-14. PDN's Target impedance

- 1.Voltage Rail Drop includes regulation accuracy, voltage distribution drops, and all dynamic events such as transient noise, AC ripple, voltage dips etc.
- 2.Typical max transient current is defined as 50% of max current draw possible.

### 7.3.2 Voltage Decoupling

Recommended power supply decoupling capacitors main characteristics for commercial products whose ambient temperature is not to exceed +85C are shown in table below:

表 7-1. Commercial Applications Recommended Decoupling Capacitors Characteristics<sup>(1)(2)(3)</sup>

| Value | Voltage [V] | Package | Stability | Dielectric | Capacitance Tolerance | Temp Range [°C] | Temp Sensitivity [%] | REFERENCE          |
|-------|-------------|---------|-----------|------------|-----------------------|-----------------|----------------------|--------------------|
| 22μF  | 6,3         | 0603    | Class 2   | X5R        | - / + 20%             | -55 to + 85     | - / + 15             | GRM188R60J226MEA0L |
| 10μF  | 4,0         | 0402    | Class 2   | X5R        | - / + 20%             | -55 to + 85     | - / + 15             | GRM155R60G106ME44  |
| 4.7μF | 6,3         | 0402    | Class 2   | X5R        | - / + 20%             | -55 to + 85     | - / + 15             | GRM155R60J475ME95  |
| 2.2μF | 6,3         | 0402    | Class 2   | X5R        | - / + 20%             | -55 to + 85     | - / + 15             | GRM155R60J225ME95  |
| 1μF   | 6,3         | 0201    | Class 2   | X5R        | - / + 20%             | -55 to + 85     | - / + 15             | GRM033R60J105MEA2  |

**表 7-1. Commercial Applications Recommended Decoupling Capacitors Characteristics<sup>(1)(2)(3)</sup> (continued)**

| Value | Voltage [V] | Package | Stability | Dielectric | Capacitance Tolerance | Temp Range [°C] | Temp Sensitivity [%] | REFERENCE         |
|-------|-------------|---------|-----------|------------|-----------------------|-----------------|----------------------|-------------------|
| 470nF | 6,3         | 0201    | Class 2   | X5R        | - / + 20%             | -55 to + 85     | - / + 15             | GRM033R60G474ME90 |
| 220nF | 6,3         | 0201    | Class 2   | X5R        | - / + 20%             | -55 to + 85     | - / + 15             | GRM033R60J224ME90 |
| 100nF | 6,3         | 0201    | Class 2   | X5R        | - / + 20%             | -55 to + 85     | - / + 15             | GRM033R60J104ME19 |

(1) Minimum value for each PCB capacitor: 100 nF.

(2) Among the different capacitors, 470 nF is recommended (not required) to filter at 5-MHz to 10-MHz frequency range.

(3) In comparison with the EIA Class 1 dielectrics, Class 2 dielectric capacitors tend to have severe temperature drift, high dependence of capacitance on applied voltage, high voltage coefficient of dissipation factor, high frequency coefficient of dissipation, and problems with aging due to gradual change of crystal structure. Aging causes gradual exponential loss of capacitance and decrease of dissipation factor.

Recommended power supply decoupling capacitors main characteristics for automotive products are shown in table below:

**表 7-2. Automotive Applications Recommended Decoupling Capacitors Characteristics<sup>(1)(2)</sup>**

| Value | Voltage [V] | Package | Stability | Dielectric | Capacitance Tolerance | Temp Range [°C] | Temp Sensitivity [%] | REFERENCE         |
|-------|-------------|---------|-----------|------------|-----------------------|-----------------|----------------------|-------------------|
| 22μF  | 6,3         | 1206    | Class 2   | X7R        | - / + 20%             | -55 to + 125    | - / + 15             | GCM31CR70J226ME23 |
| 10μF  | 6,3         | 0805    | Class 2   | X7R        | - / + 20%             | -55 to + 125    | - / + 15             | GCM21BR70J106ME22 |
| 4.7μF | 10          | 0805    | Class 2   | X7R        | - / + 20%             | -55 to + 125    | - / + 15             | GCM21BC71A475MA73 |
| 2.2μF | 6,3         | 0603    | Class 2   | X7R        | - / + 20%             | -55 to + 125    | - / + 15             | GCM188R70J225ME22 |
| 1μF   | 16          | 0603    | Class 2   | X7R        | - / + 20%             | -55 to + 125    | - / + 15             | GCM188R71C105MA64 |
| 470nF | 16          | 0603    | Class 2   | X7R        | - / + 20%             | -55 to + 125    | - / + 15             | GCM188R71C474MA55 |
| 220nF | 25          | 0603    | Class 2   | X7R        | - / + 20%             | -55 to + 125    | - / + 15             | GCM188L81C224MA37 |
| 100nF | 16          | 0402    | Class 2   | X7R        | - / + 20%             | -55 to + 125    | - / + 15             | GCM155R71C104MA55 |

(1) Minimum value for each PCB capacitor: 100 nF.

(2) Among the different capacitors, 470 nF is recommended (not required) to filter at 5-MHz to 10-MHz frequency range.

### 7.3.3 Static PDN Analysis

One power net parameter derived from a PCB's PDN static analysis is the Effective Resistance (R<sub>eff</sub>). This is the total PCB power net routing resistance that is the sum of all the individual power net segments used to deliver a supply voltage to the point of load and includes any series resistive elements (i.e. current sensing resistor) that may be installed between the PMIC outputs and Processor inputs.

### 7.3.4 Dynamic PDN Analysis

Three power net parameters derived from a PCB's PDN dynamic analysis are the Loop Inductance (LL), Impedance (Z) and PCB Frequency of Interest (F<sub>pcb</sub>).

- LL values shown are the recommended max PCB trace inductance between a decoupling capacitor's power supply and ground reference terminals when viewed from the decoupling capacitor with a "theoretical shorted" applied across the Processor's supply inputs to ground reference.
- Z values shown are the recommended max PCB trace impedances allowed between F<sub>pmic</sub> up to F<sub>pcb</sub> frequency range that limits transient noise drops to no more than 5% of min supply voltage during max transient current events.
- F<sub>pcb</sub> (Frequency of Interest) is defined to be a power rail's max frequency after which adding a reasonable number of decoupling capacitors no longer significantly reduces the power rail impedance below the desired impedance target (Z<sub>t2</sub>). This is due to the dominance of the PCB's parasitic planar spreading and internal package inductances.

表 7-3. Recommended PDN and Decoupling Characteristics <sup>(1)(2)(3)(4)(5)</sup>

| PDN Analysis:                         | Static                                  | Dynamic                                        |                       |                                            | Number of Recommended Decoupling Capacitors per Supply |           |           |     |        |        |       |       |
|---------------------------------------|-----------------------------------------|------------------------------------------------|-----------------------|--------------------------------------------|--------------------------------------------------------|-----------|-----------|-----|--------|--------|-------|-------|
| Supply                                | Max $R_{eff}$<br><sup>(7)</sup><br>[mΩ] | Dec. Cap.<br>Max LL <sup>(8) (6)</sup><br>[nH] | Max Impedance<br>[mΩ] | Frequency<br>range<br>of Interest<br>[MHz] | 100<br>nF <sup>(6)</sup>                               | 220<br>nF | 470<br>nF | 1μF | 2.2 μF | 4.7 μF | 10 μF | 22 μF |
| vdd_dspeve                            | 33                                      | 2.5                                            | 54                    | ≤20                                        | 6                                                      | 1         | 1         | 1   | 1      | 1      |       | 1     |
| vdd                                   | 83                                      | 2                                              | 87                    | ≤50                                        | 6                                                      | 1         | 1         | 1   | 1      | 1      |       |       |
| vdds_dds1,<br>vdds_dds2,<br>vdds_dds3 | 33                                      | 2.5                                            | 200                   | ≤100                                       | 8                                                      | 4         |           | 2   |        | 2      |       | 1     |
| cap_vddram_cor<br>e1                  | N/A                                     | 6                                              | N/A                   | N/A                                        |                                                        |           |           | 1   |        |        |       |       |
| cap_vddram_cor<br>e2                  | N/A                                     | 6                                              | N/A                   | N/A                                        |                                                        |           |           | 1   |        |        |       |       |
| cap_vddram_dsp<br>eve                 | N/A                                     | 6                                              | N/A                   | N/A                                        |                                                        |           |           | 1   |        |        |       |       |

- (1) For more information on peak-to-peak noise values, see the Recommended Operating Conditions table of the Electrical Characteristics chapter.
- (2) ESL must be as low as possible and must not exceed 0.5 nH.
- (3) The PDN (Power Delivery Network) impedance characteristics are defined versus the device activity (that runs at different frequency) based on the Recommended Operating Conditions table of the Electrical Characteristics chapter.
- (4) The static drop requirement drives the maximum acceptable PCB resistance between the PMIC or the external SMPS and the processor power balls.
- (5) Assuming that the external SMPS (power IC) feedback sense is taken close to processor power balls.
- (6) High-frequency (30 to 70MHz) PCB decoupling capacitors
- (7) Maximum Total  $R_{eff}$  from PMIC output to remote sensing feedback point located as close to the Device's point of load as possible.
- (8) Maximum Loop Inductance for decoupling capacitor.

### 7.3.5 Power Supply Mapping

TPS65917 is a Power management IC (PMIC) that can be used for the Device design. TI is now investigating an optimized solution for high power use cases so the TPS65917 is subject to change. An alternate dual converter power solution using LP8732Q and LP8733Q are recommended. TI requires the use of one of these PMIC solutions for the following reasons:

- TI has validated its use with the Device
- Board level margins including transient response and output accuracy are analyzed and optimized for the entire system
- Support for power sequencing requirements (refer to [Section 5.9.3 Power Sequencing](#))
- Support for Adaptive Voltage Scaling (AVS) Class 0 requirements, including TI provided software

It is possible that some voltage domains on the device are unused in some systems. In such cases, to ensure device reliability, it is still required that the supply pins for the specific voltage domains are connected to some core power supply output.

These unused supplies though can be combined with any of the core supplies that are used (active) in the system. e.g. if IVA and GPU domains are not used, they can be combined with the CORE domain, thereby having a single power supply driving the combined CORE, IVA and GPU domains.

For the combined rail, the following relaxations do apply:

- The AVS voltage of active rail in the combined rail needs to be used to set the power supply
- The decoupling capacitance should be set according to the active rail in the combined rail

Whenever we allow for combining of rails mapped on any of the SMPSEs, the PDN guidelines that are the most stringent of the rails combined should be implemented for the particular supply rail.

表 7-4 illustrates the approved and validated power supply connections to the Device for the SMPS outputs of the TPS65917 and LP8732 combined with LP8733 PMICs.

**表 7-4. Power Supply Connections**

| TPS65917 | Dual Converter Solution | Valid Combination 1:                   |
|----------|-------------------------|----------------------------------------|
| SMPS1    | LP8733Q Buck0           | vdd_dspeve                             |
| SMPS2    | LP8733Q Buck1           | vdd                                    |
| SMPS3    | LP8732Q Buck0           | vdds18v, vdds18v_ddr[3:1], vddshv[6:1] |
| SMPS4    | LP8732Q Buck1           | vdds_ddr1, vdds_ddr2, vdds_ddr3        |

表 7-5 illustrates the LP8733 and LP8732 OTP IDs required for DRA78x processor systems using different DDR memory types.

**表 7-5. OTP ID Memory Types Support**

| DDR Type | LP8733Q     | LP8732Q     |
|----------|-------------|-------------|
|          | OTP Version | OTP Version |
| DDR2     | 2A          | 2D          |
| DDR3     | 2A          | 2F          |
| DDR3L    | 2A          | 2E          |

### 7.3.6 DPLL Voltage Requirement

The voltage input to the DPLLs has a low noise requirement. Board designs should supply these voltage inputs with a low noise LDO to ensure they are isolated from any potential digital switching noise. The TPS65917 PMIC LDOLN output or LDO0 on LP8733Q dual power solution is specifically designed to meet this low noise requirement.

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For more information about Input Voltage Sources, see *DPLLs, DLLs Specifications*

表 7-6 present the voltage inputs that supply the DPLLs.

**表 7-6. Input Voltage Power Supplies for the DPLLs**

| POWER SUPPLY   | DPLLs                                                                      |
|----------------|----------------------------------------------------------------------------|
| vdda_per       | DPLL_PER and PER HSDIVIDER analog power supply                             |
| vdda_ddr_dsp   | DPLL_EVE_VID_DSP, DPLL_DDR and DDR HSDIVIDER analog power supply           |
| vdda_gmac_core | GMAC PLL, GMAC HSDIVIDER, DPLL_CORE and CORE HSDIVIDER analog power supply |

### 7.3.7 Loss of Input Power Event

A few key PDN design items needed to enable a controlled and compliant SoC power down sequence for a “Loss of Input Power” event are:

- “Loss of Input Power” early warning
  - TI EVM and Reference Design Study SCHs and PDNs achieve this by using the 1st Stage Converter’s (i.e. LM536033-Q1) Power Good status output to enable and disable the 2nd Stage PMIC devices (i.e. TPS65917/919, LP8733, and LP8732). If a different 1st Stage Converter is used, care must be taken to ensure an adequate “PG\_Status” or “Vbatt\_Status” signal is provided that can disable 2nd Stage PMIC to begin a controlled and compliant SoC power down sequence. The total elapsed time from asserting “PG\_Status” low until SoC’s PMIC input voltage reaches minimum level of 2.75V should be minimum of 1.5ms and 2ms preferred.

- Maximize discharge time of 1st Stage Vout (VSYS\_3V3 power rail = input voltage to SoC PMIC).
  - TI EVM and Reference Design Study SCHs and PDNs achieve this by opening an in-line load switch immediately upon “PG\_Status” low assertion in order to remove the SoC’s 3.3V IO load current from VSYS\_3V3. This will extend the VSYS\_3V3 power rail’s discharge time in order to maximize elapsed time for allowing SoC PMIC to execute a controlled and compliant power down sequence. Care should be taken to either disable or isolate any additional peripheral components that may be loading the VSYS\_3V3 rail as well.
- Sufficient bulk decoupling capacitance on the 1st Stage Vout (VSYS\_3V3 per PDN) that allows for desired 1.5 – 2ms elapsed time as described above.
  - TI EVM and Reference Design Study SCHs and PDNs achieve this by using 200uF of total capacitance on VSYS\_3V3. The 1st Stage Converter (i.e. LM536033-Q1) can typically drive a max of 400uF to help extend VSYS\_3V3 discharge time for a compliant SoC power down sequence.
- Optimizing the 2nd Stage SoC PMIC’s OTP settings that determines SoC power up and down sequences and total elapsed time needed for a controlled sequence.
  - TI EVM and Reference Design Study SCHs and PDNs achieve this by using optimized OTPs per the SCH and components used. The definition of these OTPs is captured in the detailed timing diagrams for both power up and down sequences. The PDN diagram typically shows a recommended PMIC OTP ID based upon the SoC and DDR memory types.

### 7.3.8 Example PCB Design

The following sections describe an example PCB design and its resulting PDN performance for the vdd\_dspeve key processor power domain.

#### 注

Materials presented in this section are based on generic PDN analysis on PCB boards and are not specific to systems integrating the Device.

#### 7.3.8.1 Example Stack-up

Layer Assignments:

- Layer Top: Signal and Segmented Power Plane
  - Processor and PMIC components placed on Top-side
- Layer 2: Gnd Plane1
- Layer 3: Signals
- Layer n: Power Plane1
- Layer n+1: Power Plane 2
- Layer n+2: Signal
- Layer n+3: Gnd Plane2
- Layer Bottom: Signal and Segmented Power Planes
  - Decoupling caps, etc.

Via Technology: Through-hole

Copper Weight:

- ½ oz for all signal layers.
- 1-2oz for all power plane for improved PCB heat spreading.

#### 7.3.8.2 vdd\_dspeve Example Analysis

Maximum acceptable PCB resistance ( $R_{\text{eff}}$ ) between the PMIC and Processor input power balls should not exceed 33mΩ per 表 7-3 and (7).

Maximum decoupling capacitance loop inductance (LL) between Processor input power balls and decoupling capacitances should not exceed 2.5nH per 表 7-3 and (7) (ESL NOT included).

Impedance target for key frequency of interest between Processor input power balls and PMIC's SMPS output power balls should not exceed 54mΩ per 表 7-3 and (7).

表 7-7. Example PCB vdd\_dspeve PI Analysis Summary

| Parameter                                                        | Recommendation         | Example PCB              |
|------------------------------------------------------------------|------------------------|--------------------------|
| OPP                                                              | OPP_NOM                |                          |
| Clocking Rate                                                    | 500 MHz                |                          |
| Voltage Level                                                    | 1 V                    | 1 V                      |
| Max Current Draw                                                 | 1 A                    | 1 A                      |
| Max Effective Resistance: Power Inductor Segment Total $R_{eff}$ | 13 mΩ                  | 11.4 mΩ                  |
| Max Loop Inductance                                              | < 2.5 nH               | 0.73 - 1.58 nH           |
| Impedance Target                                                 | 54 mΩ for $F < 20$ MHz | 28.8 mΩ for $F < 20$ MHz |

図 7-15 shows a PCB layout example and the resulting PI analysis results.

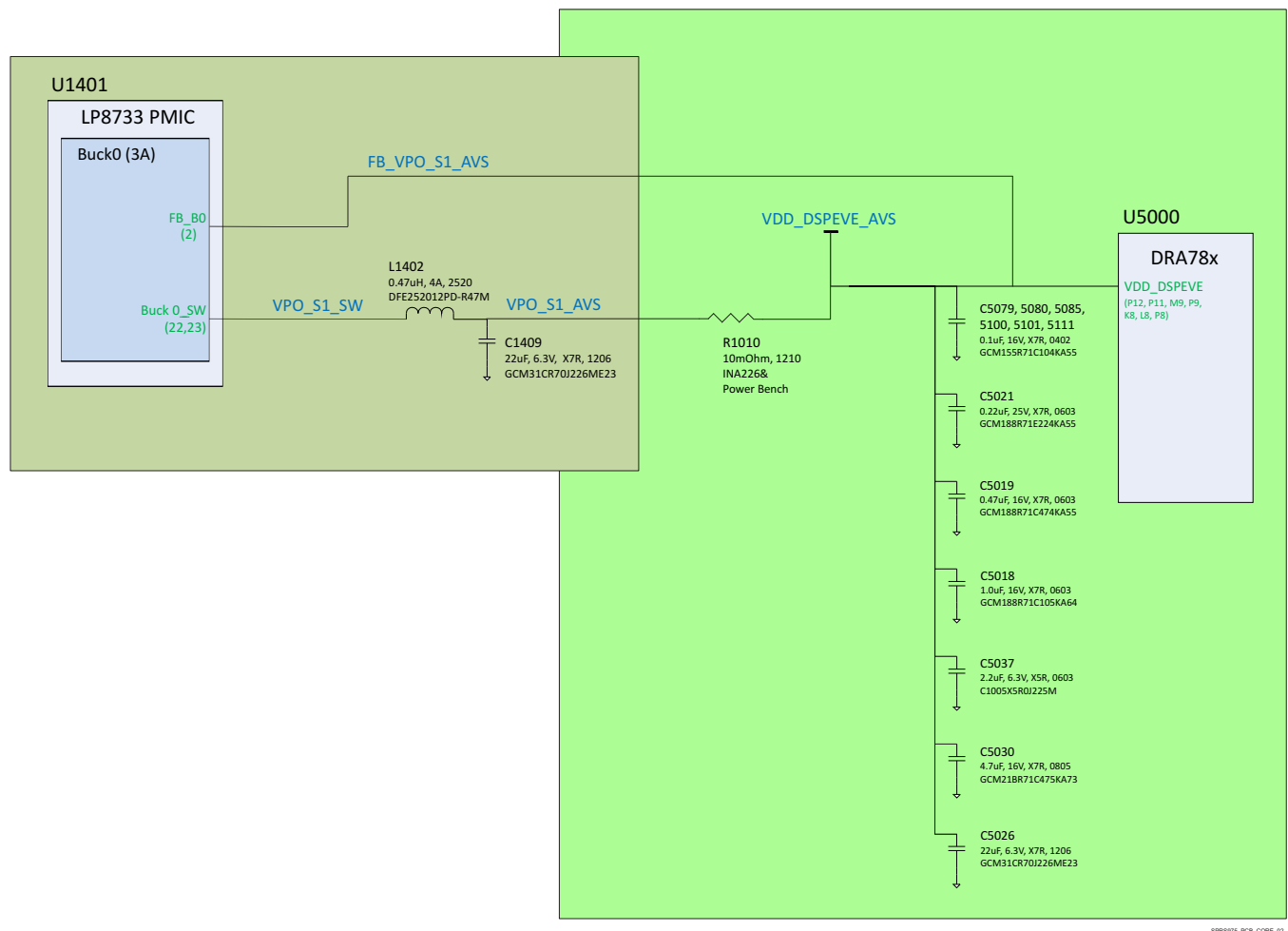


图 7-15. vdd\_dspeve Simplified SCH Diagram

表 7-8. DCap Scheme

| Vaule [uF]                           | Size | Qty | Capacitance [uF] |
|--------------------------------------|------|-----|------------------|
| Cap Type: Automotive GCM series, X7R |      |     |                  |
| 22                                   | 1206 | 1   | 22               |
| 4.7                                  | 805  | 1   | 4.7              |
| 2.2                                  | 603  | 1   | 2.2              |
| 1                                    | 603  | 1   | 1                |
| 0.47                                 | 603  | 1   | 0.47             |
| 0.22                                 | 603  | 1   | 0.22             |
| 0.1                                  | 402  | 6   | 0.6              |
| <b>Totals</b>                        |      | 12  | 31.19            |

IR Drop: vdd\_dspeve

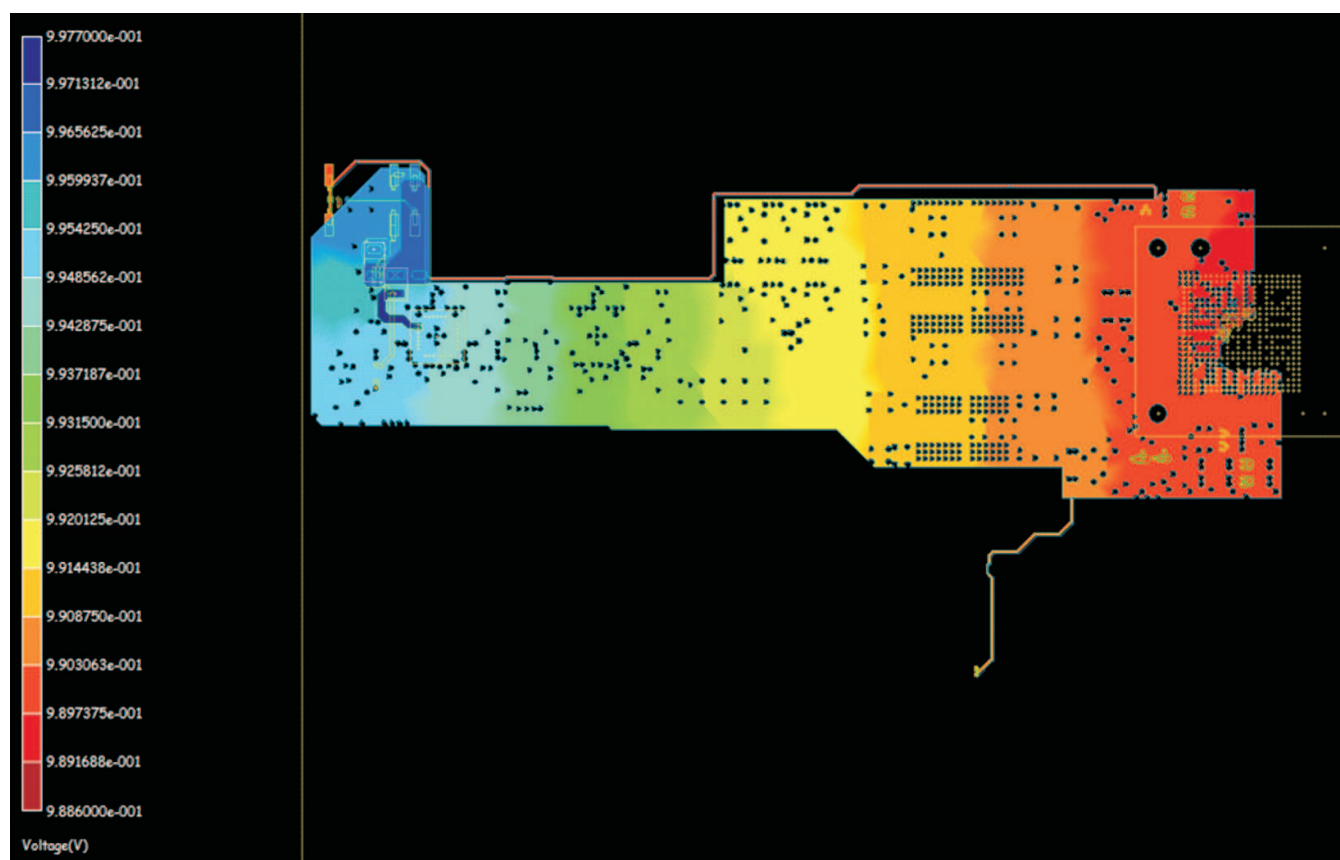


图 7-16. vdd\_dspeve Voltage/IR Drop [All Layers]

Dynamic analysis of this PCB design for the CORE power domain determined the vdd\_dspeve decoupling capacitor loop inductance and impedance vs frequency analysis shown below. As you can see, the loop inductance values ranged from 0.68 –1.79nH and were less than maximum 2.0nH recommended.

表 7-9. Decoupling Design Detail Summary

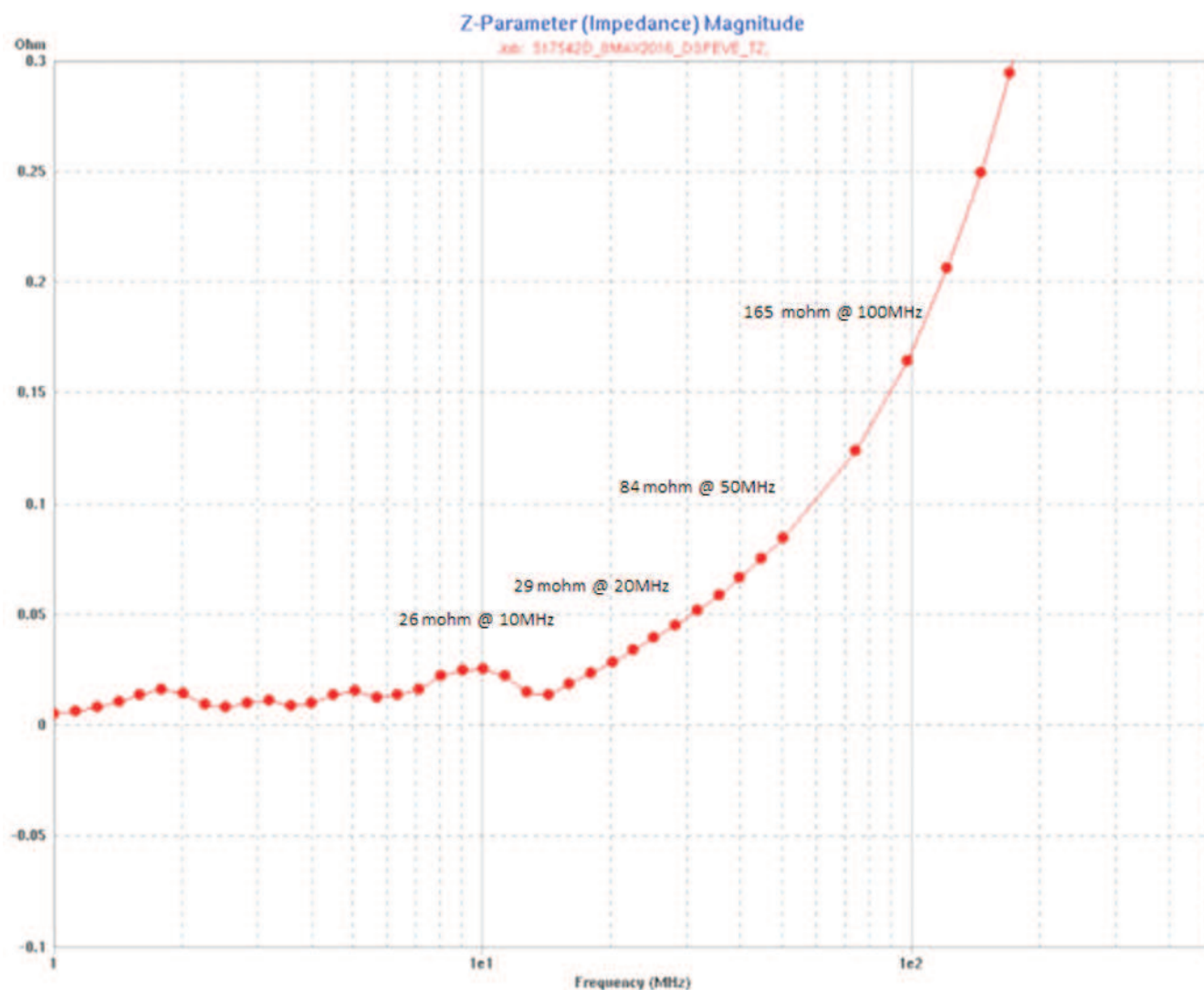
| Cap Reference Description | Loop Inductance at 50MHz [nH] | Footprint Types | PCB Side | Distance to Ball-Field [mils] | Value | Size |
|---------------------------|-------------------------------|-----------------|----------|-------------------------------|-------|------|
| C5101                     | 0.73                          | 2vWEE           | Bottom   | 82                            | 0.1   | 0402 |
| C5100                     | 0.78                          | 2vWEE           | Bottom   | 107                           | 0.1   | 0402 |

**表 7-9. Decoupling Design Detail Summary (continued)**

| Cap Reference Description | Loop Inductance at 50MHz [nH] | Footprint Types | PCB Side | Distance to Ball-Field [mils] | Value | Size |
|---------------------------|-------------------------------|-----------------|----------|-------------------------------|-------|------|
| C5085                     | 0.84                          | 2vWEE           | Bottom   | 35                            | 0.1   | 0402 |
| C5019                     | 1.09                          | 4vWE            | Top      | 631                           | 0.47  | 0603 |
| C5111                     | 1.09                          | 4vWE            | Bottom   | 681                           | 0.1   | 0402 |
| C5030                     | 1.11                          | 4vWE            | Top      | 738                           | 4.7   | 0805 |
| C5037                     | 1.11                          | 4vWE            | Top      | 563                           | 2.2   | 0603 |
| C5018                     | 1.14                          | 4vWE            | Top      | 681                           | 1     | 0603 |
| C5021                     | 1.17                          | 4vWE            | Top      | 761                           | 0.22  | 0603 |
| C5026                     | 1.18                          | 4vWE            | Top      | 792                           | 22    | 1206 |
| C5079                     | 1.32                          | 4vWE            | Bottom   | 542                           | 0.1   | 0402 |
| C5080                     | 1.58                          | 4vWE            | Bottom   | 602                           | 0.1   | 0402 |

(1) Distances are wrt "middle of Ball Field", Ref pt between: U5000-M9 to middle of Dcap's power pad unless specified

☒ 7-17 shows vdd\_dspeve Impedance vs Frequency characteristics.



SPRS91v\_PCB\_CORE\_08

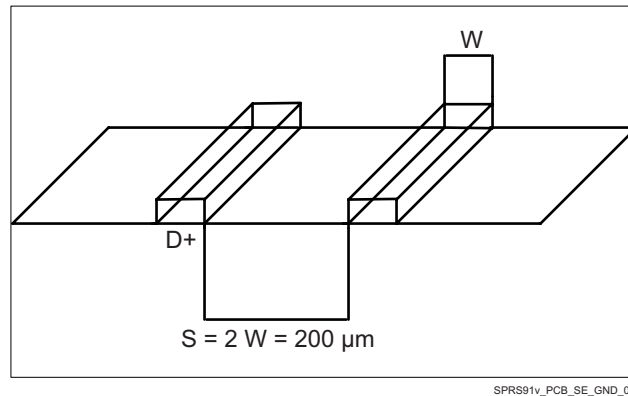
**☒ 7-17. vdd\_dspeve Impedance vs Frequency**

## 7.4 Single-Ended Interfaces

### 7.4.1 General Routing Guidelines

The following paragraphs detail the routing guidelines that must be observed when routing the various functional LVCMOS interfaces.

- Line spacing:
  - For a line width equal to  $W$ , the spacing between two lines must be  $2W$ , at least. This minimizes the crosstalk between switching signals between the different lines. On the PCB, this is not achievable everywhere (for example, when breaking signals out from the device package), but it is recommended to follow this rule as much as possible. When violating this guideline, minimize the length of the traces running parallel to each other (see [Figure 7-18](#)).



**Figure 7-18. Ground Guard Illustration**

- Length matching (unless otherwise specified):
  - For bus or traces at frequencies less than 10 MHz, the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 25 mm.
  - For bus or traces at frequencies greater than 10 MHz, the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 2.5 mm.
- Characteristic impedance
  - Unless otherwise specified, the characteristic impedance for single-ended interfaces is recommended to be between 35-Ω and 65-Ω.
- Multiple peripheral support
  - For interfaces where multiple peripherals have to be supported in the star topology, the length of each branch has to be balanced. Before closing the PCB design, it is highly recommended to verify signal integrity based on simulations including actual PCB extraction.

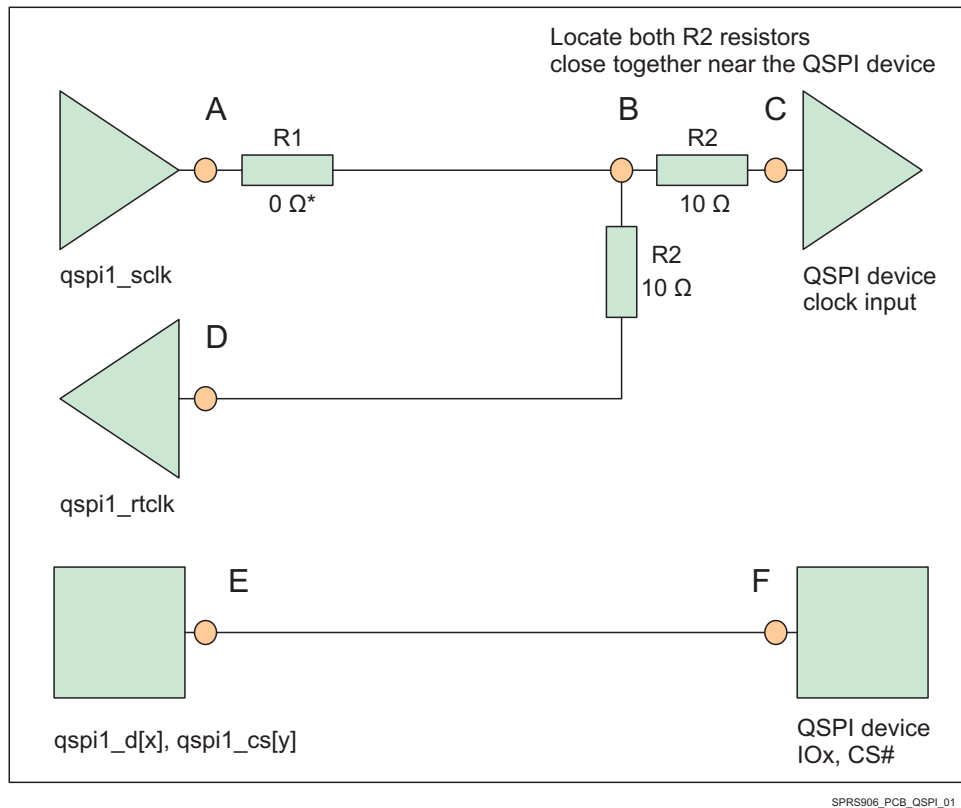
### 7.4.2 QSPI Board Design and Layout Guidelines

The following section details the routing guidelines that must be observed when routing the QSPI interfaces.

#### 7.4.2.1 If QSPI is operated in Mode 0 (POL=0, PHA=0):

- The qspi1\_sclk output signal must be looped back into the qspi1\_rtclk input.
- The signal propagation delay from the qspi1\_sclk ball to the QSPI device CLK input pin (A to C) must be approximately equal to the signal propagation delay from the QSPI device CLK pin to the qspi1\_rtclk ball (C to D).
- The signal propagation delay from the QSPI device CLK pin to the qspi1\_rtclk ball (C to D) must be approximately equal to the signal propagation delay of the control and data signals between the QSPI device and the SoC device (E to F, or F to E).

- The signal propagation delay from the qspi1\_sclk signal to the series terminators ( $R2 = 10\ \Omega$ ) near the QSPI device must be  $< 450\text{pS}$  ( $\sim 7\text{cm}$  as stripline or  $\sim 8\text{cm}$  as microstrip)
- $50\ \Omega$  PCB routing is recommended along with series terminations, as shown in [Figure 7-19](#).
- Propagation delays and matching:
  - A to C = C to D = E to F
  - Matching skew:  $< 60\text{pS}$
  - A to B  $< 450\text{pS}$
  - B to C = as small as possible ( $< 60\text{pS}$ )



**Figure 7-19. QSPI Interface High Level Schematic Mode 0 (POL=0, PHA=0)**

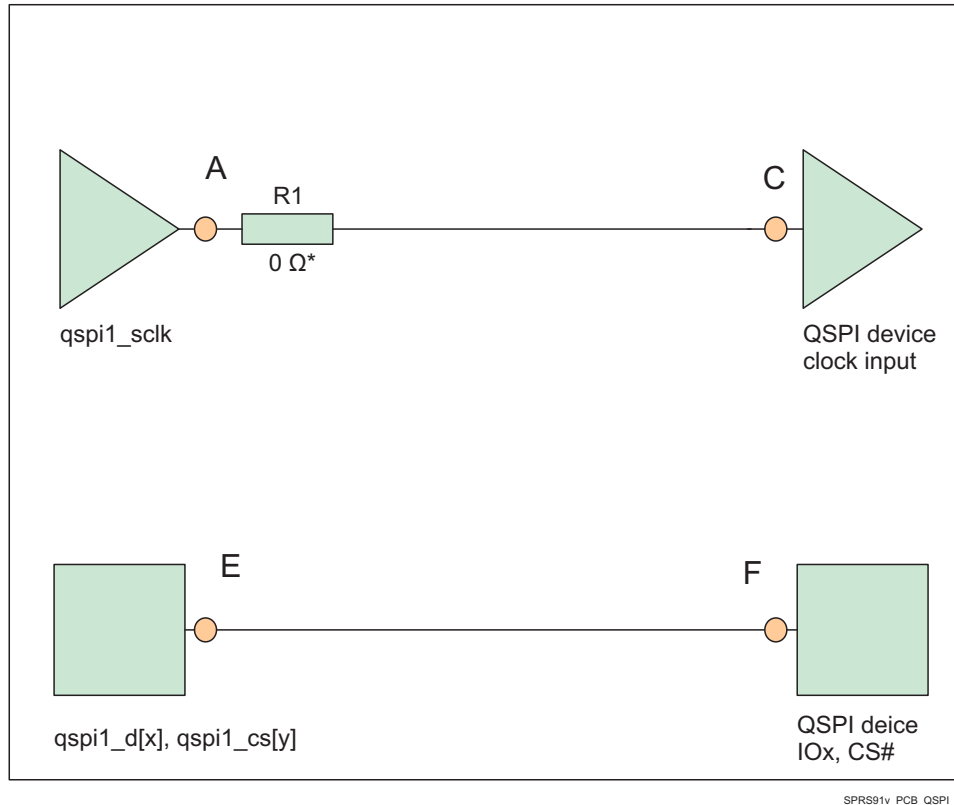
注

\* $0\ \Omega$  resistor (R1), located as close as possible to the qspi1\_sclk pin, is placeholder for fine-tuning if needed.

#### 7.4.2.2 If QSPI is operated in Mode 3 (POL=1, PHA=1):

- The qspi1\_rtclk input can be left unconnected.
- The signal propagation delay from the qspi1\_sclk signal to the QSPI device CLK pin (A to C) must be approximately equal to the signal propagation delay of the control and data signals between the QSPI device and the SoC device (E to F, or F to E).
- The signal propagation delay from the qspi1\_sclk signal to the QSPI device CLK pin (A to C) must be  $< 450\text{pS}$  ( $\sim 7\text{cm}$  as stripline or  $\sim 8\text{cm}$  as microstrip).
- $50\ \Omega$  PCB routing is recommended along with series terminations, as shown in [Figure 7-20](#).

- Propagation delays and matching:
  - A to C = E to F.
  - Matching skew: < 60Ps
  - A to B < 450pS



SPRS91v\_PCB\_QSPI\_01

图 7-20. QSPI Interface High Level Schematic Mode 3 (POL=1, PHA=1)

注

\*0 Ω resistor (R1), located as close as possible to the qspi1\_sclk pin, is placeholder for fine-tuning if needed.

## 7.5 Differential Interfaces

### 7.5.1 General Routing Guidelines

To maximize signal integrity, proper routing techniques for differential signals are important for high-speed designs. The following general routing guidelines describe the routing guidelines for differential lanes and differential signals.

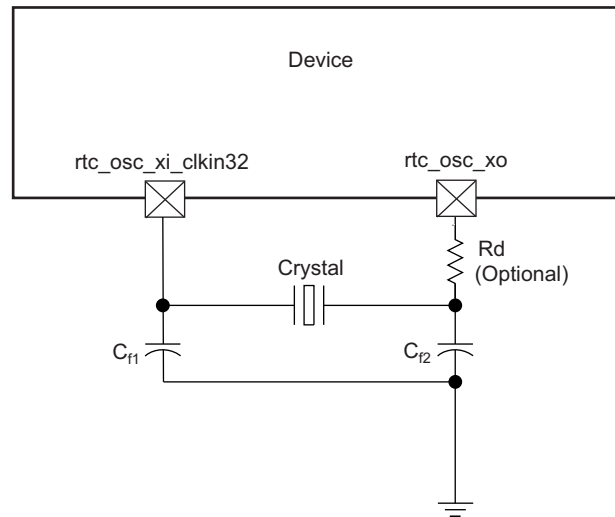
- As much as possible, no other high-frequency signals must be routed in close proximity to the differential pair.
- Must be routed as differential traces on the same layer. The trace width and spacing must be chosen to yield the differential impedance value recommended.
- Minimize external components on differential lanes (like external ESD, probe points).
- Through-hole pins are not recommended.
- Differential lanes mustn't cross image planes (ground planes).
- No sharp bend on differential lanes.

- Number of vias on the differential pairs must be minimized, and identical on each line of the differential pair. In case of multiple differential lanes in the same interface, all lines should have the same number of vias.
- Shielded routing is to be promoted as much as possible (for instance, signals must be routed on internal layers that are inside power and/or ground planes).

## 7.6 Clock Routing Guidelines

### 7.6.1 Oscillator Ground Connection

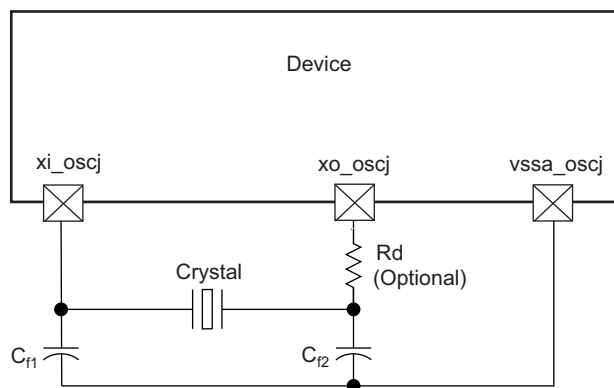
Although the impedance of a ground plane is low it is, of course, not zero. Therefore, any noise current in the ground plane causes a voltage drop in the ground. [Figure 7-21](#) shows the grounding scheme for slow (low frequency) clock generated from the internal oscillator.



SPRS91v\_PCB\_CLK\_OSC\_02

**Figure 7-21. Grounding Scheme for Low-Frequency Clock**

[Figure 7-22](#) shows the grounding scheme for high-frequency clock.



SPRS91v\_PCB\_CLK\_OSC\_03

(1) j in \*\_osc = 0 or 1

**Figure 7-22. Grounding Scheme for High-Frequency Clock**

## 7.7 DDR2 Board Design and Layout Guidelines

### 7.7.1 DDR2 General Board Layout Guidelines

To help ensure good signaling performance, consider the following board design guidelines:

- Avoid crossing splits in the power plane.
- Minimize Vref noise.
- Use the widest trace that is practical between decoupling capacitors and memory module.
- Maintain a single reference.
- Minimize ISI by keeping impedances matched.
- Minimize crosstalk by isolating sensitive bits, such as strobes, and avoiding return path discontinuities.
- Use proper low-pass filtering on the Vref pins.
- Keep the stub length as short as possible.
- Add additional spacing for on-clock and strobe nets to eliminate crosstalk.
- Maintain a common ground reference for all bypass and decoupling capacitors.
- Take into account the differences in propagation delays between microstrip and stripline nets when evaluating timing constraints.

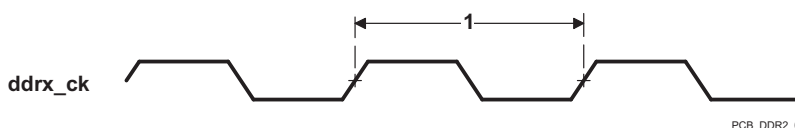
### 7.7.2 DDR2 Board Design and Layout Guidelines

#### 7.7.2.1 Board Designs

TI only supports board designs that follow the guidelines outlined in this document. The switching characteristics and the timing diagram for the DDR2 memory controller are shown in 表 7-10 and 图 7-23.

**表 7-10. Switching Characteristics Over Recommended Operating Conditions for DDR2 Memory Controller**

| NO.   | PARAMETER         | DESCRIPTION         | MIN | MAX | UNIT |
|-------|-------------------|---------------------|-----|-----|------|
| DDR21 | $t_{c(DDR\_CLK)}$ | Cycle time, DDR_CLK | 2.5 | 8   | ns   |



**图 7-23. DDR2 Memory Controller Clock Timing**

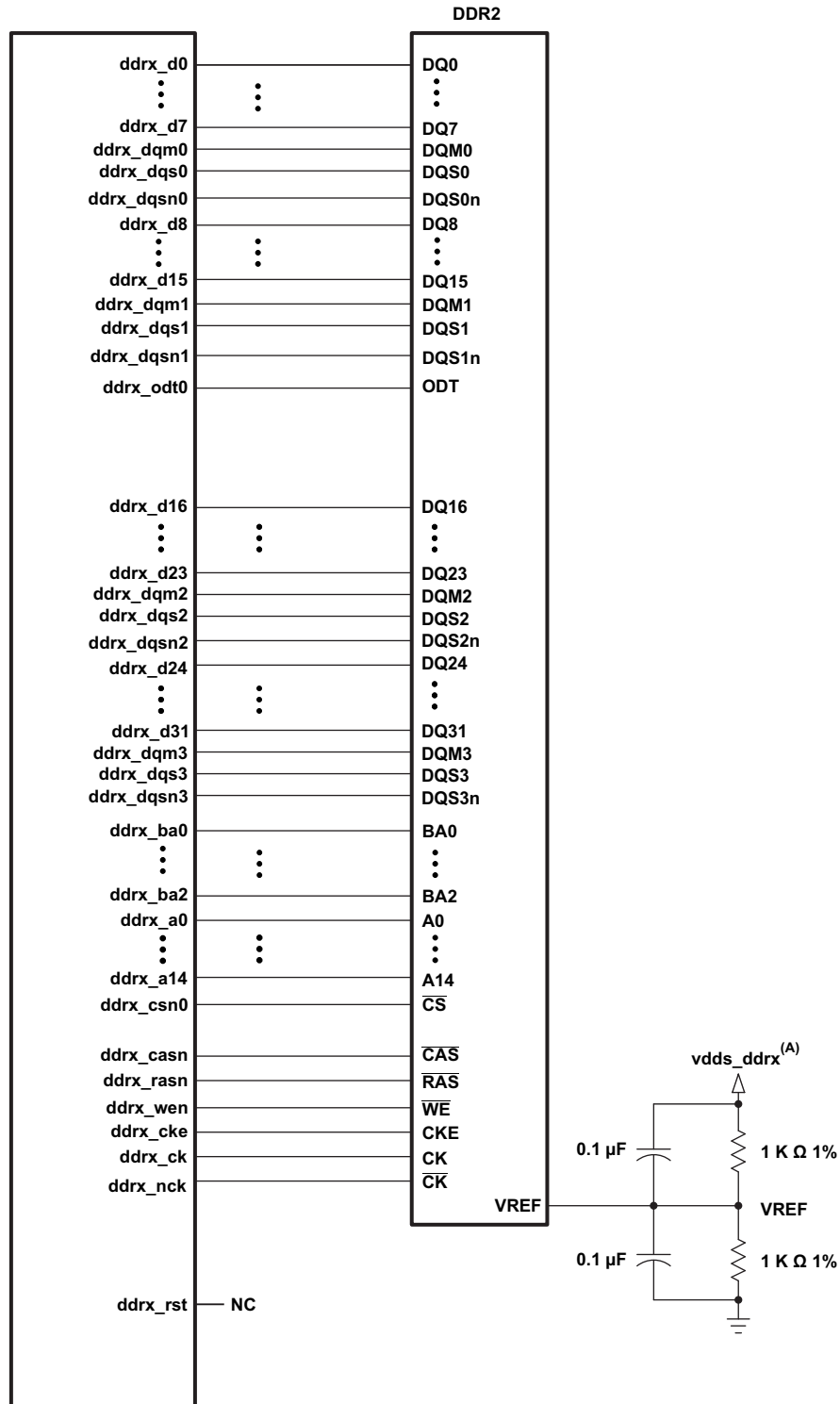
#### 7.7.2.2 DDR2 Interface

This section provides the timing specification for the DDR2 interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR2 memory system without the need for a complex timing closure process. For more information regarding the guidelines for using this DDR2 specification, see the *Understanding TI's PCB Routing Rule-Based DDR Timing Specification* Application Report (Literature Number: [SPRAAV0](#)).

##### 7.7.2.2.1 DDR2 Interface Schematic

图 7-24 shows the DDR2 interface schematic for a x32 DDR2 memory system. In 图 7-25 the x16 DDR2 system schematic is identical except that the high-word DDR2 device is deleted.

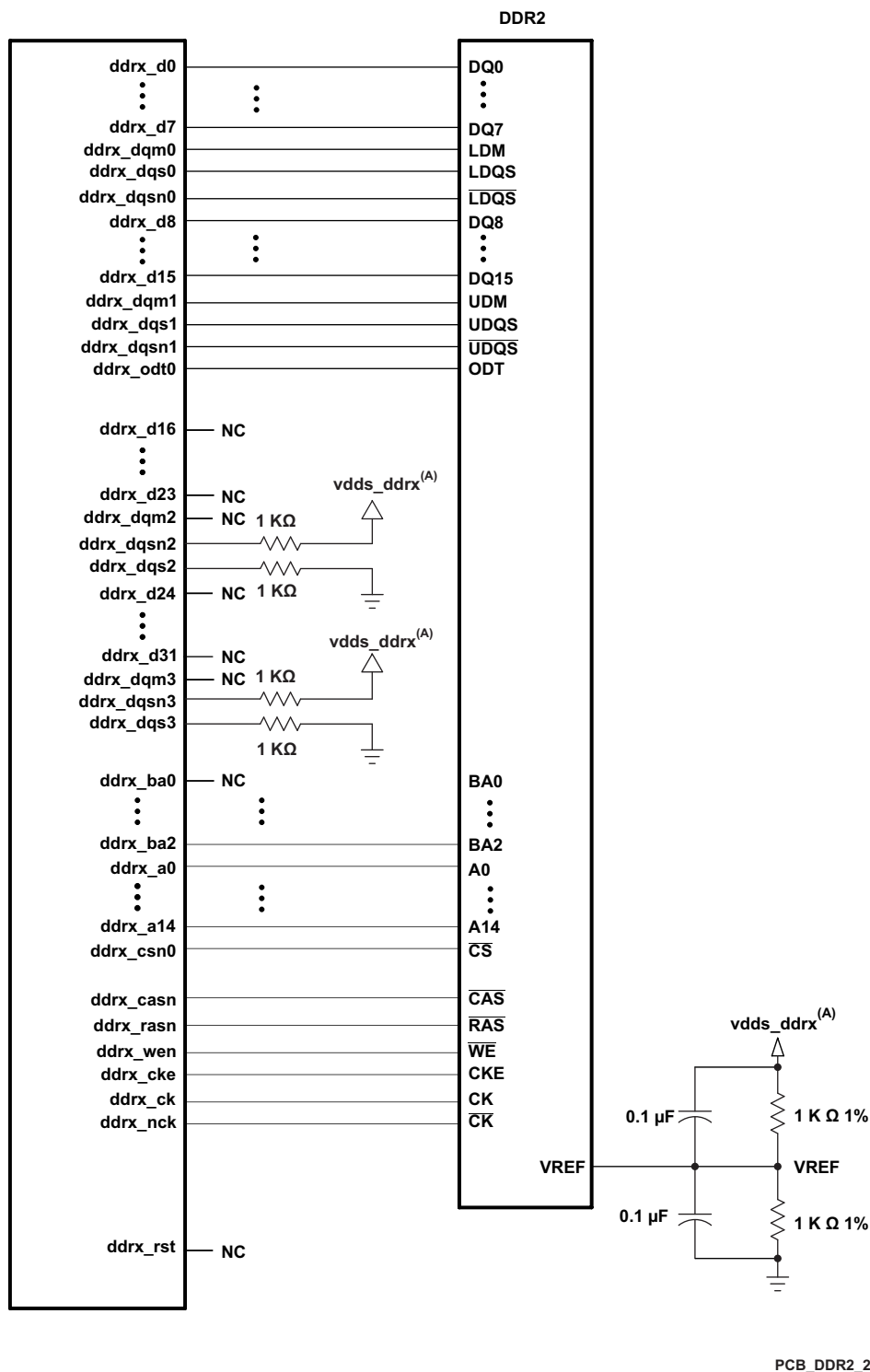
When not using all or part of a DDR2 interface, the proper method of handling the unused pins is to tie off the ddrx\_dqs<sub>i</sub> pins to ground via a 1k-Ω resistor and to tie off the ddrx\_dqs<sub>n</sub>i pins to the corresponding vdds\_ddrx supply via a 1k-Ω resistor. This needs to be done for each byte not used. The vdds\_ddrx and ddrx\_vref0 power supply pins need to be connected to their respective power supplies even if DDRx is not being used. All other DDR interface pins can be left unconnected. Note that the supported modes for use of the DDR EMIF are 32-bits wide, 16-bits wide, or not used.



PCB\_DDR2\_1

- A. vdds\_ddrx is the power supply for the DDR2 memories and the Device DDR2 interface.
- B. One of these capacitors can be eliminated if the divider and its capacitors are placed near a VREF pin.

**7-24. 32-Bit DDR2 High-Level Schematic**



- A. vdds\_ddrx is the power supply for the DDR2 memories and the Device DDR2 interface.  
B. One of these capacitors can be eliminated if the divider and its capacitors are placed near a VREF pin.

7-25. 16-Bit DDR2 High-Level Schematic

### 7.7.2.2.2 Compatible JEDEC DDR2 Devices

表 7-11 shows the parameters of the JEDEC DDR2 devices that are compatible with this interface. Generally, the DDR2 interface is compatible with x16/x32 DDR2-800 speed grade DDR2 devices.

**表 7-11. Compatible JEDEC DDR2 Devices (Per Interface)**

| NO.  | PARAMETER                                    | MIN      | MAX | UNIT    |
|------|----------------------------------------------|----------|-----|---------|
| CJ21 | JEDEC DDR2 device speed grade <sup>(1)</sup> | DDR2-800 |     |         |
| CJ22 | JEDEC DDR2 device bit width                  | x16      | x32 | Bits    |
| CJ23 | JEDEC DDR2 device count <sup>(2)</sup>       | 1        | 1   | Devices |

(1) Higher DDR2 speed grades are supported due to inherent JEDEC DDR2 backwards compatibility.

(2) One DDR2 device is used for a 16-bit DDR2 and 32-bit DDR2 memory system.

### 7.7.2.2.3 PCB Stackup

The minimum stackup required for routing the Device is a six-layer stackup as shown in 表 7-12. Additional layers may be added to the PCB stackup to accommodate other circuitry or to reduce the size of the PCB footprint.

**表 7-12. Minimum PCB Stackup**

| LAYER | TYPE   | DESCRIPTION      |
|-------|--------|------------------|
| 1     | Signal | External Routing |
| 2     | Plane  | Ground           |
| 3     | Plane  | Power            |
| 4     | Signal | Internal routing |
| 5     | Plane  | Ground           |
| 6     | Signal | External Routing |

Complete stackup specifications are provided in 表 7-13.

表 7-13. PCB Stackup Specifications

| NO.   | PARAMETER                                                                          | MIN | TYP | MAX | UNIT |
|-------|------------------------------------------------------------------------------------|-----|-----|-----|------|
| PS21  | PCB routing/plane layers                                                           | 6   |     |     |      |
| PS22  | Signal routing layers                                                              | 3   |     |     |      |
| PS23  | Full ground reference layers under DDR2 routing region <sup>(1)</sup>              | 1   |     |     |      |
| PS24  | Full vdds_ddrx power reference layers under the DDR2 routing region <sup>(1)</sup> | 1   |     |     |      |
| PS25  | Number of reference plane cuts allowed within DDR routing region <sup>(2)</sup>    |     |     | 0   |      |
| PS26  | Number of layers between DDR2 routing layer and reference plane <sup>(3)</sup>     |     |     | 0   |      |
| PS27  | PCB routing feature size                                                           |     | 4   |     | Mils |
| PS28  | PCB trace width, w                                                                 |     | 4   |     | Mils |
| PS29  | Single-ended impedance, Zo                                                         | 50  |     | 75  | Ω    |
| PS210 | Impedance control <sup>(4)</sup>                                                   | Z-5 | Z   | Z+5 | Ω    |

(1) Ground reference layers are preferred over power reference layers. Be sure to include bypass caps to accommodate reference layer return current as the trace routes switch routing layers. A full ground reference layer should be placed adjacent to each DDR routing layer in PCB stack up.

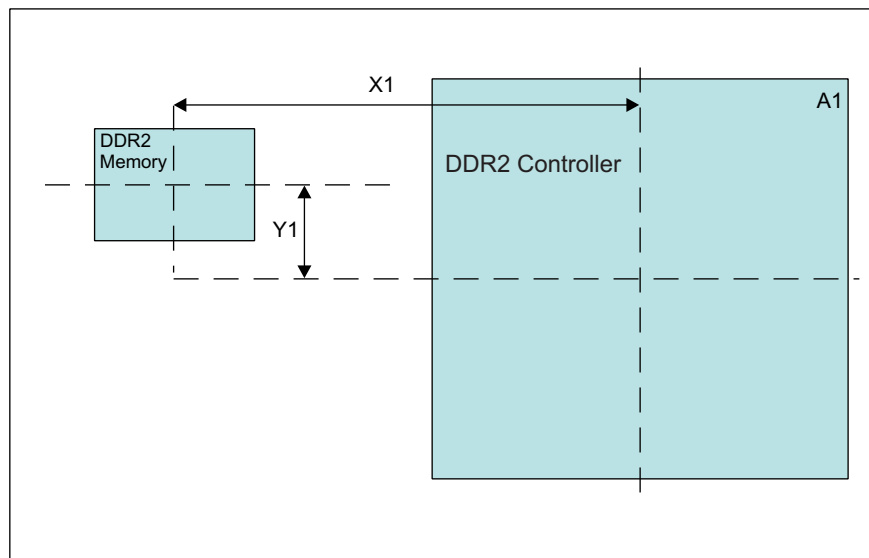
(2) No traces should cross reference plane cuts within the DDR routing region. High-speed signal traces crossing reference plane cuts create large return current paths which can lead to excessive crosstalk and EMI radiation.

(3) Reference planes are to be directly adjacent to the signal plane to minimize the size of the return current loop.

(4) Z is the nominal singled-ended impedance selected for the PCB specified by PS29.

#### 7.7.2.2.4 Placement

Figure 7-26 shows the required placement for the Device as well as the DDR2 devices. The dimensions for this figure are defined in Table 7-14. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16-bit DDR memory system, the high-word DDR2 device is omitted from the placement.



PCB\_DDR2\_3

**Figure 7-26. Device and DDR2 Device Placement**

**Table 7-14. Placement Specifications DDR2**

| NO.   | PARAMETER                                                                | MIN | MAX  | UNIT |
|-------|--------------------------------------------------------------------------|-----|------|------|
| KOD21 | X1                                                                       |     | 1100 | Mils |
| KOD22 | Y1                                                                       |     | 500  | Mils |
| KOD24 | DDR2 keepout region <sup>(1)</sup>                                       |     |      |      |
| KOD25 | Clearance from non-DDR2 signal to DDR2 keepout region <sup>(2) (3)</sup> | 4   |      | W    |

(1) DDR2 keepout region to encompass entire DDR2 routing area.

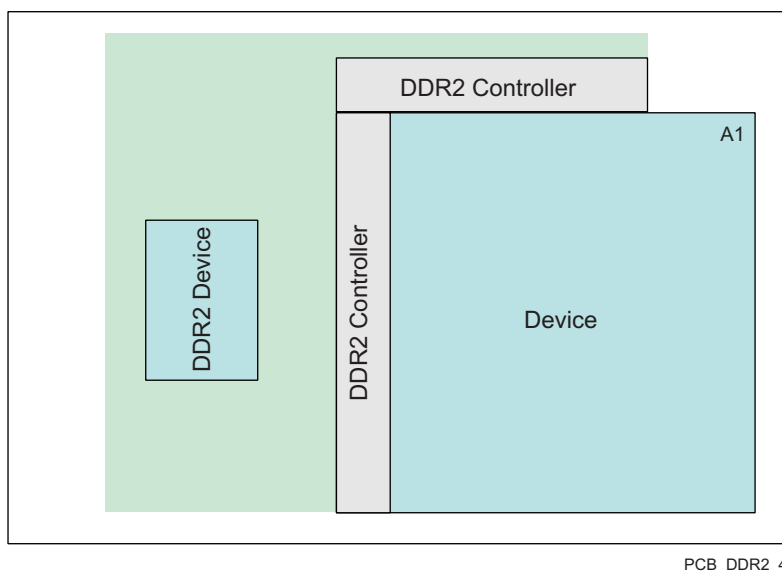
(2) Non-DDR2 signals allowed within DDR2 keepout region provided they are separated from DDR2 routing layers by a ground plane.

(3) If a device has more than one DDR controller, the signals from the other controller(s) are considered non-DDR2 and should be separated by this specification.

### 7.7.2.2.5 DDR2 Keepout Region

The region of the PCB used for the DDR2 circuitry must be isolated from other signals. The DDR2 keepout region is defined for this purpose and is shown in [Figure 7-27](#). The size of this region varies with the placement and DDR routing. Additional clearances required for the keepout region are shown in [Table 7-14](#).

The region shown in [Table 7-14](#) should encompass all the DDR2 circuitry and varies depending on placement. Non-DDR2 signals should not be routed on the DDR signal layers within the DDR2 keepout region. Non-DDR2 signals may be routed in the region, provided they are routed on layers separated from DDR2 signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the vdds\_ddrx power plane should cover the entire keepout region. Routes for the two DDR interfaces must be separated by at least 4x; the more separation, the better.



**Figure 7-27. DDR2 Keepout Region**

### 7.7.2.2.6 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR2 and other circuitry. [Table 7-15](#) contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DDR2 interfaces and DDR2 device. Additional bulk bypass capacitance may be needed for other circuitry.

**Table 7-15. Bulk Bypass Capacitors**

| NO.  | PARAMETER                                                                    | MIN | TYP | MAX | UNIT          |
|------|------------------------------------------------------------------------------|-----|-----|-----|---------------|
| BC21 | vdds_ddrx bulk bypass capacitor ( $\geq 1\mu\text{F}$ ) count <sup>(1)</sup> |     | 10  |     | Devices       |
| BC22 | vdds_ddrx bulk bypass total capacitance                                      |     | 50  |     | $\mu\text{F}$ |

(1) These devices should be placed near the devices they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors and DDR2 signal routing.

### 7.7.2.2.7 High-Speed Bypass Capacitors

TI recommends that a PDN/power integrity analysis is performed to ensure that capacitor selection and placement is optimal for a given implementation. This section provides guidelines that can serve as a good starting point.

High-speed (HS) bypass capacitors are critical for proper DDR2 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, processor/DDR power, and processor/DDR ground connections. [Table 7-16](#) contains the specification for the HS bypass capacitors as well as for the power connections on the PCB. Generally speaking, it is good to:

1. Fit as many HS bypass capacitors as possible.
2. HS bypass capacitor value is  $< 1\mu\text{F}$
3. Minimize the distance from the bypass cap to the pins/balls being bypassed.
4. Use the smallest physical sized capacitors possible with the highest capacitance readily available.
5. Connect the bypass capacitor pads to their vias using the widest traces possible and using the largest hole size via possible.
6. Minimize via sharing. Note the limites on via sharing shown in 表 7-16.

**表 7-16. High-Speed Bypass Capacitors**

| NO.   | PARAMETER                                                                                     | MIN  | TYP                | MAX                 | UNIT          |
|-------|-----------------------------------------------------------------------------------------------|------|--------------------|---------------------|---------------|
| HS21  | HS bypass capacitor package size <sup>(1)</sup>                                               |      | 0201               | 0402                | 10 Mils       |
| HS22  | Distance, HS bypass capacitor to processor being bypassed <sup>(2)(3)(4)</sup>                |      |                    | 400 <sup>(12)</sup> | Mils          |
| HS23  | Processor HS bypass capacitor count <sup>(12)</sup>                                           |      | 12 <sup>(11)</sup> |                     | Devices       |
| HS24  | Processor HS bypass capacitor total capacitance per vdds_ddrx rail <sup>(12)</sup>            |      | 3.4                |                     | $\mu\text{F}$ |
| HS25  | Number of connection vias for each device power/ground ball per vdds_ddrx rail <sup>(5)</sup> | 1    |                    |                     | Vias          |
| HS26  | Trace length from device power/ground ball to connection via <sup>(2)</sup>                   |      | 35                 | 70                  | Mils          |
| HS27  | Distance, HS bypass capacitor to DDR device being bypassed <sup>(6)</sup>                     |      |                    | 150                 | Mils          |
| HS28  | Number of connection vias for each HS capacitor <sup>(8)(9)</sup>                             |      | 4 <sup>(14)</sup>  |                     | Vias          |
| HS29  | DDR2 device HS bypass capacitor count <sup>(7)</sup>                                          |      | 12 <sup>(13)</sup> |                     | Devices       |
| HS210 | DDR2 device HS bypass capacitor total capacitance <sup>(7)</sup>                              | 0.85 |                    |                     | $\mu\text{F}$ |
| HS211 | Trace length from bypass capacitor connect to connection via <sup>(2)(9)</sup>                |      | 35                 | 100                 | Mils          |
| HS212 | Number of connection vias for each DDR2 device power/ground ball <sup>(10)</sup>              | 1    |                    |                     | Vias          |
| HS213 | Trace length from DDR2 device power/ground ball to connection via <sup>(2)(8)</sup>           |      | 35                 | 60                  | Mils          |

(1) LxW, 10-mil units, that is, a 0402 is a 40x20-mil surface-mount capacitor.

(2) Closer/shorter is better.

(3) Measured from the nearest processor power/ground ball to the center of the capacitor package.

(4) Three of these capacitors should be located underneath the processor, between the cluster of vdds\_ddrx balls and ground balls, between the DDR interfaces on the package.

(5) See the Via Channel™ escape for the processor package.

(6) Measured from the DDR2 device power/ground ball to the center of the capacitor package.

(7) Per DDR2 device.

(8) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board. No sharing of vias is permitted on the same side of the board.

(9) An HS bypass capacitor may share a via with a DDR device mounted on the same side of the PCB. A wide trace should be used for the connection and the length from the capacitor pad to the DDR device pad should be less than 150 mils.

(10) Up to a total of two pairs of DDR power/ground balls may share a via.

(11) The capacitor recommendations in this data manual reflect only the needs of this processor. Please see the memory vendor's guidelines for determining the appropriate decoupling capacitor arrangement for the memory device itself.

(12) For more information, see 7.3, Core Power Domains

(13) For more information refer to DDR2 specification.

(14) Preferred configuration is 4 vias: 2 to power and 2 to ground.

### 7.7.2.2.8 Net Classes

表 7-17 lists the clock net classes for the DDR2 interface. 表 7-18 lists the signal net classes, and associated clock net classes, for the signals in the DDR2 interface. These net classes are used for the termination and routing rules that follow.

表 7-17. Clock Net Class Definitions

| CLOCK NET CLASS     | PIN NAMES              |
|---------------------|------------------------|
| CK                  | ddrx_ck / ddrx_nck     |
| DQS0                | ddrx_dqs0 / ddrx_dqsn0 |
| DQS1                | ddrx_dqs1 / ddrx_dqsn1 |
| DQS2 <sup>(1)</sup> | ddrx_dqs2 / ddrx_dqsn2 |
| DQS3 <sup>(1)</sup> | ddrx_dqs3 / ddrx_dqsn3 |

(1) Only used on 32-bit wide DDR2 memory systems.

表 7-18. Signal Net Class Definitions

| SIGNAL NET CLASS   | ASSOCIATED CLOCK NET CLASS | PIN NAMES                                                                                 |
|--------------------|----------------------------|-------------------------------------------------------------------------------------------|
| ADDR_CTRL          | CK                         | ddrx_ba[2:0], ddrx_a[14:0], ddrx_csnj, ddrx_casn, ddrx_rasn, ddrx_wen, ddrx_cke, ddrx_odt |
| DQ0                | DQS0                       | ddrx_d[7:0], ddrx_dqm0                                                                    |
| DQ1                | DQS1                       | ddrx_d[15:8], ddrx_dqm1                                                                   |
| DQ2 <sup>(1)</sup> | DQS2                       | ddrx_d[23:16], ddrx_dqm2                                                                  |
| DQ3 <sup>(1)</sup> | DQS3                       | ddrx_d[31:24], ddrx_dqm3                                                                  |

(1) Only used on 32-bit wide DDR2 memory systems.

#### 7.7.2.2.9 DDR2 Signal Termination

Signal terminators are NOT required in CK, ADDR\_CTRL, and DATA net classes. Serial terminators may be used to reduce EMI risk; however, serial terminations are the only type permitted. ODTs are integrated on the data byte net classes. They should be enabled to ensure signal integrity. 表 7-19 shows the specifications for the series terminators.

表 7-19. DDR2 Signal Terminations

| NO.  | PARAMETER                                                 | MIN | TYP | MAX            | UNIT     |
|------|-----------------------------------------------------------|-----|-----|----------------|----------|
| ST21 | CK net class <sup>(1)(2)</sup>                            | 0   |     | 10             | $\Omega$ |
| ST22 | ADDR_CTRL net class <sup>(1)(2)(3)(4)</sup>               | 0   |     | Z <sub>o</sub> | $\Omega$ |
| ST23 | Data byte net classes (DQS0-DQS3, DQ0-DQ3) <sup>(5)</sup> | 0   |     | Z <sub>o</sub> | $\Omega$ |

(1) Only series termination is permitted, parallel or SST specifically disallowed on board.

(2) Only required for EMI reduction.

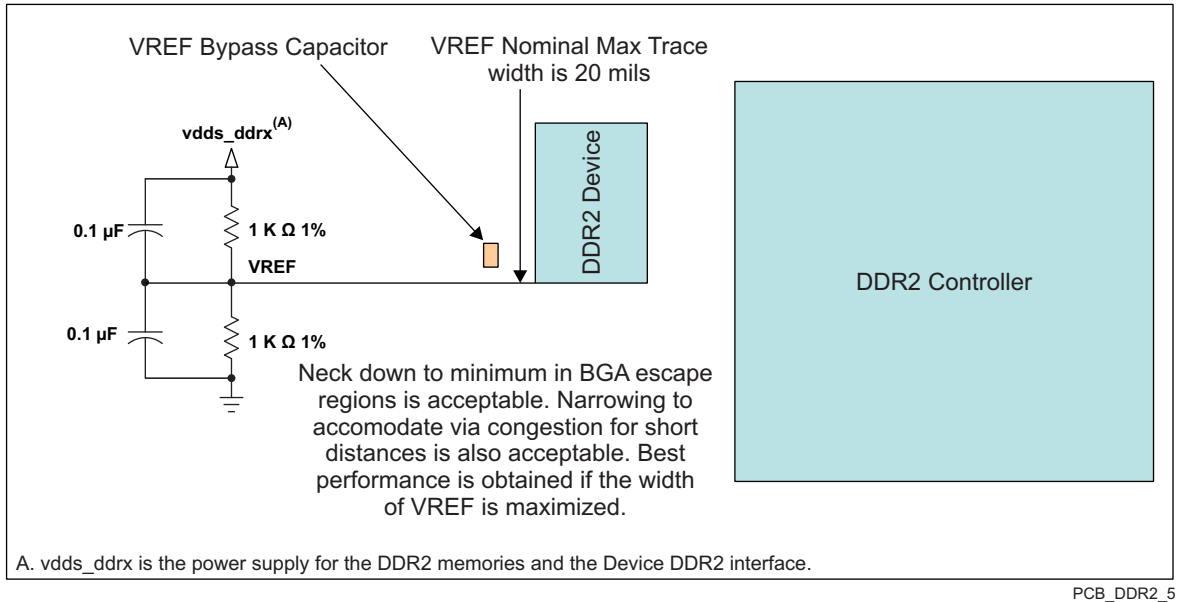
(3) Terminator values larger than typical only recommended to address EMI issues.

(4) Termination value should be uniform across net class.

(5) No external terminations allowed for data byte net classes ODT is to be used.

#### 7.7.2.2.10 VREF Routing

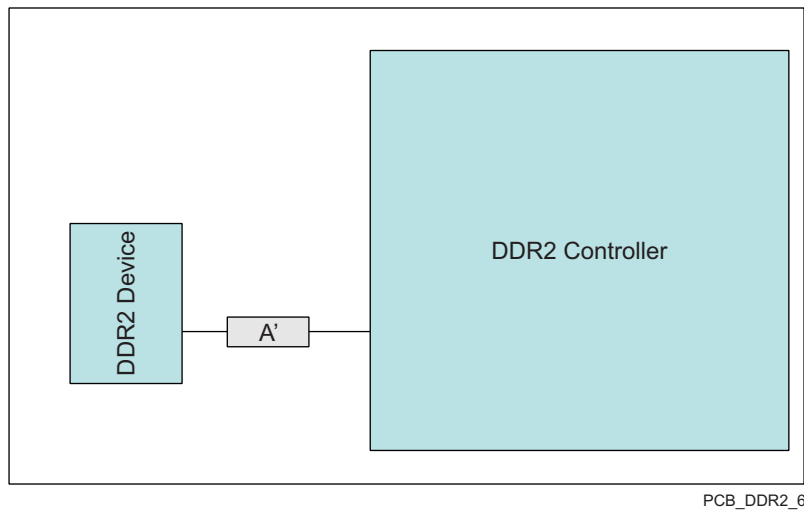
VREF (ddrx\_vref0) is used as a reference by the input buffers of the DDR2 memories. VREF is intended to be half the DDR2 power supply voltage and should be created using a resistive divider as shown in 图 7-25. Other methods of creating VREF are not recommended. 图 7-28 shows the layout guidelines for VREF.



**图 7-28. VREF Routing and Topology**

### 7.7.2.3 DDR2 CK and ADDR\_CTRL Routing

图 7-29 shows the topology of the routing for the CK and ADDR\_CTRL net classes. The route is a point to point connection with required skew matching.



**图 7-29. CK and ADDR\_CTRL Routing and Topology**

**表 7-20. CK and ADDR\_CTRL Routing Specification**

| NO.   | PARAMETER                                                             | MIN | MAX | UNIT |
|-------|-----------------------------------------------------------------------|-----|-----|------|
| RSC21 | Center-to-center ddrx_ck - ddrx_nck spacing                           |     | 2w  |      |
| RSC22 | ddrx_ck / ddrx_nck skew                                               |     | 5   | ps   |
| RSC25 | Center-to-center CK to other DDR2 trace spacing <sup>(2)</sup>        | 4w  |     |      |
| RSC26 | CK/ADDR_CTRL trace length <sup>(3)</sup>                              |     | 680 | ps   |
| RSC27 | ADDR_CTRL-to-CK skew mismatch                                         |     | 25  | ps   |
| RSC28 | ADDR_CTRL-to-ADDR_CTRL skew mismatch                                  |     | 25  | ps   |
| RSC29 | Center-to-center ADDR_CTRL to other DDR2 trace spacing <sup>(2)</sup> | 4w  |     |      |

表 7-20. CK and ADDR\_CTRL Routing Specification (continued)

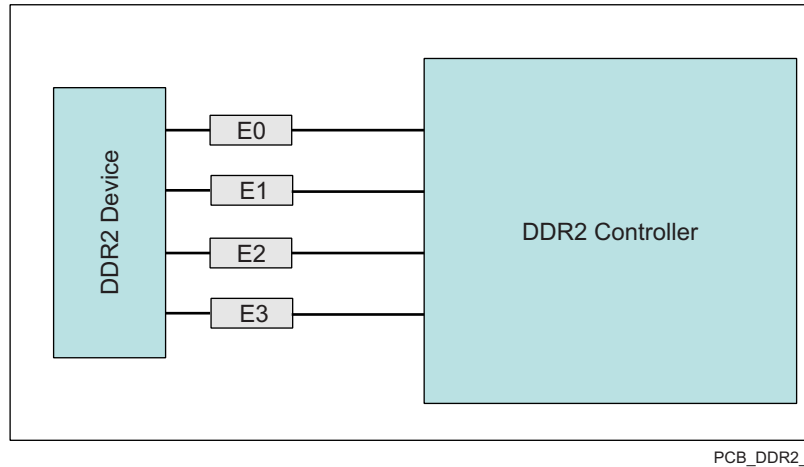
| NO.    | PARAMETER                                                                  | MIN | MAX | UNIT |
|--------|----------------------------------------------------------------------------|-----|-----|------|
| RSC210 | Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing <sup>(2)</sup> | 3w  |     |      |

(1) Series terminator, if used, should be located closest to the Device.

(2) Center-to-center spacing is allowed to fall to minimum 2w for up to 500 mils of routed length to accommodate BGA escape and routing congestion.

(3) This is the longest routing length of the CK and ADDR\_CTRL net classes.

☒ 7-30 shows the topology and routing for the DQS and DQ net classes; the routes are point to point. Skew matching across bytes is not needed nor recommended. The termination resistor should be placed near the processor.



☒ 7-30. DQS and DQ Routing and Topology

表 7-21. DQS and DQ Routing Specification

| NO.     | PARAMETER                                                          | MIN | MAX | UNIT |
|---------|--------------------------------------------------------------------|-----|-----|------|
| RSDQ21  | Center-to-center DQS-DQSn spacing in E0 E1 E2 E3                   | 2w  |     |      |
| RSDQ22  | DQS-DQSn skew in E0 E1 E2 E3                                       |     | 5   | ps   |
| RSDQ23  | Center-to-center DQS to other DDR2 trace spacing <sup>(1)</sup>    | 4w  |     |      |
| RSDQ24  | DQS/DQ trace length <sup>(2)(3)(4)</sup>                           |     | 325 | ps   |
| RSDQ25  | DQ-to-DQS skew mismatch <sup>(2)(3)(4)</sup>                       |     | 10  | ps   |
| RSDQ26  | DQ-to-DQ skew mismatch <sup>(2)(3)(4)</sup>                        |     | 10  | ps   |
| RSDQ27  | DQ-to-DQ/DQS via count mismatch <sup>(2)(3)(4)</sup>               |     | 1   | Vias |
| RSDQ28  | Center-to-center DQ to other DDR2 trace spacing <sup>(1)(5)</sup>  | 4w  |     |      |
| RSDQ29  | Center-to-center DQ to other DQ trace spacing <sup>(1)(6)(7)</sup> | 3w  |     |      |
| RSDQ210 | DQ/DQS E skew mismatch <sup>(2)(3)(4)</sup>                        |     | 25  | ps   |

(1) Center-to-center spacing is allowed to fall to minimum 2w for up to 500 mils of routed length to accommodate BGA escape and routing congestion.

(2) A 16-bit DDR memory system has two sets of data net classes; one for data byte 0, and one for data byte 1, each with an associated DQS (2 DQSs) per DDR EMIF used.

(3) A 32-bit DDR memory system has four sets of data net classes; one each for data bytes 0 through 3, and each associated with a DQS (4 DQSs) per DDR EMIF used.

(4) There is no need, and it is not recommended, to skew match across data bytes; that is, from DQS0 and data byte 0 to DQS1 and data byte1.

(5) DQs from other DQS domains are considered *other DDR2 trace*.

(6) DQs from other data bytes are considered *other DDR2 trace*.

(7) This is the longest routing distance of each of the DQS and DQ net classes.

## 7.8 DDR3 Board Design and Layout Guidelines

## 7.8.1 DDR3 General Board Layout Guidelines

To help ensure good signaling performance, consider the following board design guidelines:

- Avoid crossing splits in the power plane.
- Use the widest trace that is practical between decoupling capacitors and memory module.
- Maintain a single reference
- Minimize ISI by keeping impedances matched.
- Minimize crosstalk by isolating sensitive bits, such as strobes, and avoiding return path discontinuities.
- Keep the stub length as short as possible.
- Add additional spacing for on-clock and strobe nets to eliminate crosstalk.
- Maintain a common ground reference for all bypass and decoupling capacitors.
- Take into account the differences in propagation delays between microstrip and stripline nets when evaluating timing constraints.

## 7.8.2 DDR3 Board Design and Layout Guidelines

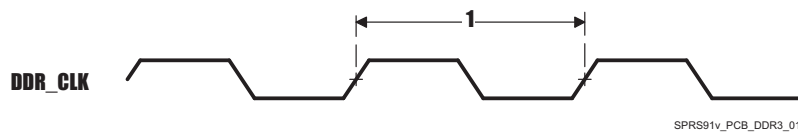
### 7.8.2.1 Board Designs

TI only supports board designs using DDR3 memory that follow the guidelines in this document. The switching characteristics and timing diagram for the DDR3 memory controller are shown in 表 7-22 and 图 7-31.

**表 7-22. Switching Characteristics Over Recommended Operating Conditions for DDR3 Memory Controller**

| NO. | PARAMETER         |                     | MIN   | MAX                | UNIT |
|-----|-------------------|---------------------|-------|--------------------|------|
| 1   | $t_{c(DDR\_CLK)}$ | Cycle time, DDR_CLK | 1.875 | 2.5 <sup>(1)</sup> | ns   |

(1) This is the absolute maximum the clock period can be. Actual maximum clock period may be limited by DDR3 speed grade and operating frequency (see the DDR3 memory device data sheet).



**图 7-31. DDR3 Memory Controller Clock Timing**

### 7.8.2.2 DDR3 Device Combinations

There are several possible combinations of device counts and single- or dual-side mounting, 表 7-23 summarizes the supported device configurations.

**表 7-23. Supported DDR3 Device Combinations**

| NUMBER OF DDR3 DEVICES | DDR3 DEVICE WIDTH (BITS) | ECC DEVICE WIDTH (BITS) | MIRRORED?        | DDR3 EMIF WIDTH (BITS) |
|------------------------|--------------------------|-------------------------|------------------|------------------------|
| 1                      | 1x16                     | -                       | N                | 16                     |
| 2                      | 2x8                      | -                       | Y <sup>(1)</sup> | 16                     |
| 2                      | 2x16                     | -                       | N                | 32                     |
| 2                      | 2x16                     | -                       | Y <sup>(1)</sup> | 32                     |
| 2                      | 1x16                     | 1x8                     | N                | 16                     |
| 3                      | 2x8                      | 1x8                     | N                | 16                     |
| 3                      | 2x16                     | 1x8                     | N                | 32                     |

- (1) Two DDR3 devices are mirrored when one device is placed on the top of the board and the second device is placed on the bottom of the board.

### 7.8.2.3 DDR3 Interface Schematic

#### 7.8.2.3.1 32-Bit DDR3 Interface

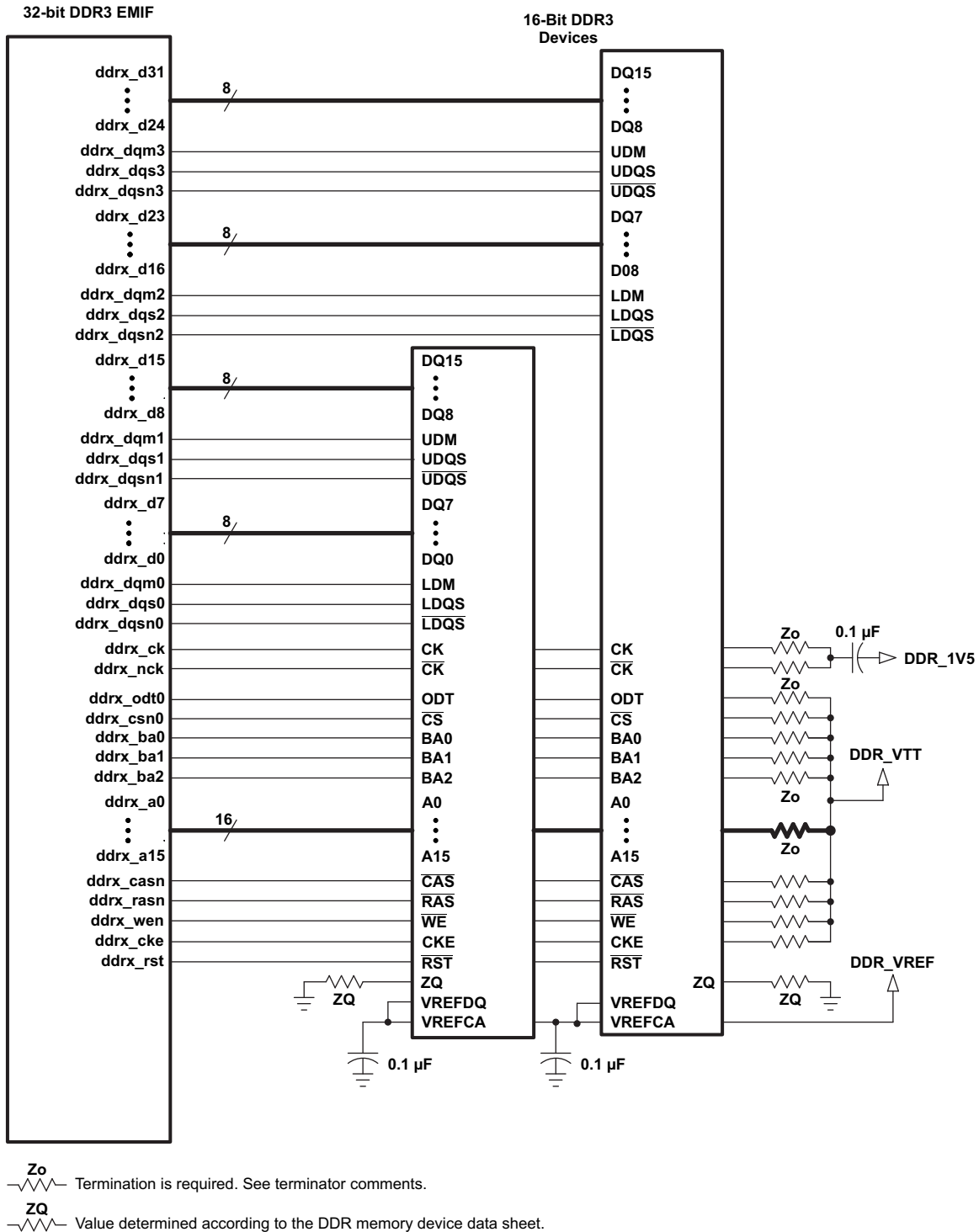
The DDR3 interface schematic varies, depending upon the width of the DDR3 devices used and the width of the bus used (16 or 32 bits). General connectivity is straightforward and very similar. 16-bit DDR devices look like two 8-bit devices. [Figure 7-32](#) shows the schematic connections for 32-bit interfaces using x16 devices.

#### 7.8.2.3.2 16-Bit DDR3 Interface

Note that the 16-bit wide interface schematic is practically identical to the 32-bit interface (see [Figure 7-32](#)); only the high-word DDR memories are removed and the unused DQS inputs are tied off.

When not using all or part of a DDR interface, the proper method of handling the unused pins is to tie off the `ddrx_dqsi` pins to ground via a 1k- $\Omega$  resistor and to tie off the `ddrx_dqsn` pins to the corresponding `vdds_ddrx` supply via a 1k- $\Omega$  resistor. This needs to be done for each byte not used. Although these signals have internal pullups and pulldowns, external pullups and pulldowns provide additional protection against external electrical noise causing activity on the signals.

The `vdds_ddr` and `vdds18v_ddrx` power supply pins need to be connected to their respective power supplies even if upper data byte lanes are not being used. All other DDR interface pins can be left unconnected. Note that the supported modes for use of the DDR EMIF are 32-bits wide, 16-bits wide, or not used.



7-32. 32-Bit, One-Bank DDR3 Interface Schematic Using Two 16-Bit DDR3 Devices

#### 7.8.2.4 Compatible JEDEC DDR3 Devices

表 7-24 shows the parameters of the JEDEC DDR3 devices that are compatible with this interface. Generally, the DDR3 interface is compatible with DDR3-1066 devices in the x8 or x16 widths.

表 7-24. Compatible JEDEC DDR3 Devices

| N O. | PARAMETER                                    | CONDITION                        | MIN       | MAX       | UNIT    |
|------|----------------------------------------------|----------------------------------|-----------|-----------|---------|
| 1    | JEDEC DDR3 device speed grade <sup>(1)</sup> | DDR clock rate = 400MHz          | DDR3-800  | DDR3-1600 |         |
|      |                                              | 400MHz < DDR clock rate ≤ 533MHz | DDR3-1066 | DDR3-1600 |         |
| 2    | JEDEC DDR3 device bit width                  |                                  | x8        | x16       | Bits    |
| 3    | JEDEC DDR3 device count <sup>(2)</sup>       |                                  | 1         | 3         | Devices |

(1) Refer to 表 7-22 Switching Characteristics Over Recommended Operating Conditions for DDR3 Memory Controller for the range of supported DDR clock rates.

(2) For valid DDR3 device configurations and device counts, see 表 7-23 DDR3 Device Combinations.

#### 7.8.2.5 PCB Stackup

The minimum stackup for routing the DDR3 interface is a six-layer stack up as shown in 表 7-25. Additional layers may be added to the PCB stackup to accommodate other circuitry, enhance SI/EMI performance, or to reduce the size of the PCB footprint. Complete stackup specifications are provided in 表 7-26.

表 7-25. Six-Layer PCB Stackup Suggestion

| LAYER | TYPE   | DESCRIPTION                           |
|-------|--------|---------------------------------------|
| 1     | Signal | Top routing mostly vertical           |
| 2     | Plane  | Ground                                |
| 3     | Plane  | Split power plane                     |
| 4     | Plane  | Split power plane or Internal routing |
| 5     | Plane  | Ground                                |
| 6     | Signal | Bottom routing mostly horizontal      |

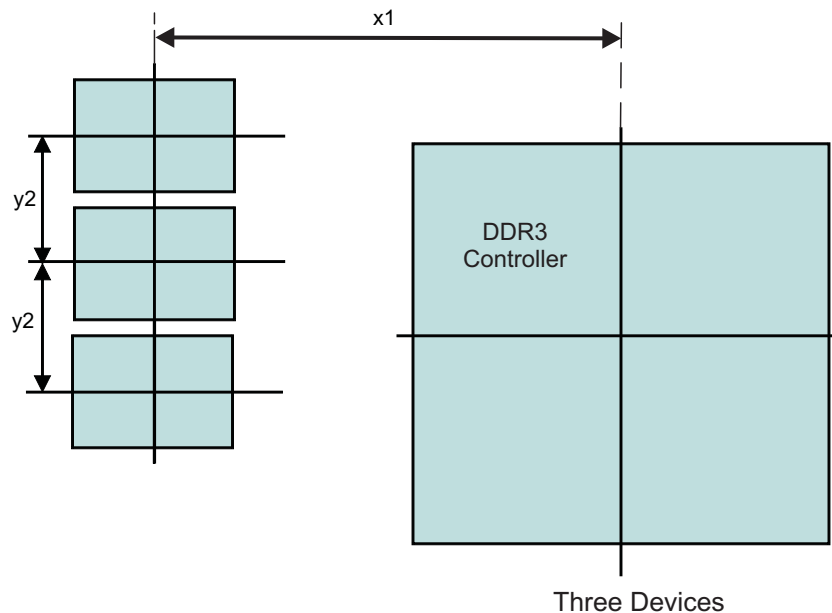
**表 7-26. PCB Stackup Specifications**

| NO.  | PARAMETER                                                                       | MIN | TYP | MAX | UNIT |
|------|---------------------------------------------------------------------------------|-----|-----|-----|------|
| PS1  | PCB routing/plane layers                                                        | 6   |     |     |      |
| PS2  | Signal routing layers                                                           | 3   |     |     |      |
| PS3  | Full ground reference layers under DDR3 routing region <sup>(1)</sup>           | 1   |     |     |      |
| PS4  | Full 1.5-V power reference layers under the DDR3 routing region <sup>(1)</sup>  | 1   |     |     |      |
| PS5  | Number of reference plane cuts allowed within DDR routing region <sup>(2)</sup> |     |     | 0   |      |
| PS6  | Number of layers between DDR3 routing layer and reference plane <sup>(3)</sup>  |     |     | 0   |      |
| PS7  | PCB routing feature size                                                        |     | 4   |     | Mils |
| PS8  | PCB trace width, w                                                              |     | 4   |     | Mils |
| PS9  | Single-ended impedance, Z <sub>0</sub>                                          | 50  |     | 75  | Ω    |
| PS10 | Impedance control <sup>(5)</sup>                                                | Z-5 | Z   | Z+5 | Ω    |

- (1) Ground reference layers are preferred over power reference layers. Be sure to include bypass caps to accommodate reference layer return current as the trace routes switch routing layers.
- (2) No traces should cross reference plane cuts within the DDR routing region. High-speed signal traces crossing reference plane cuts create large return current paths which can lead to excessive crosstalk and EMI radiation.
- (3) Reference planes are to be directly adjacent to the signal plane to minimize the size of the return current loop.
- (4) An 18-mil pad assumes Via Channel is the most economical BGA escape. A 20-mil pad may be used if additional layers are available for power routing. An 18-mil pad is required for minimum layer count escape.
- (5) Z is the nominal singled-ended impedance selected for the PCB specified by PS9.

### 7.8.2.6 Placement

图 7-33 shows the required placement for the processor as well as the DDR3 devices. The dimensions for this figure are defined in 表 7-27. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16-bit DDR memory system, the high-word DDR3 devices are omitted from the placement.



SPRS91v\_PCB\_DDR3\_04

**图 7-33. Placement Specifications**

表 7-27. Placement Specifications

| No.   | PARAMETER                                                               | MIN | MAX  | UNIT |
|-------|-------------------------------------------------------------------------|-----|------|------|
| KOD31 | X1                                                                      |     | 1700 | Mils |
| KOD34 | Y1                                                                      |     | 1800 | Mils |
| KOD35 | Y2                                                                      |     | 600  | Mils |
| KOD36 | DDR3 keepout region <sup>(1)</sup>                                      |     |      |      |
| KOD37 | Clearance from non-DDR3 signal to DDR3 keepout region <sup>(2)(3)</sup> | 4   |      | W    |

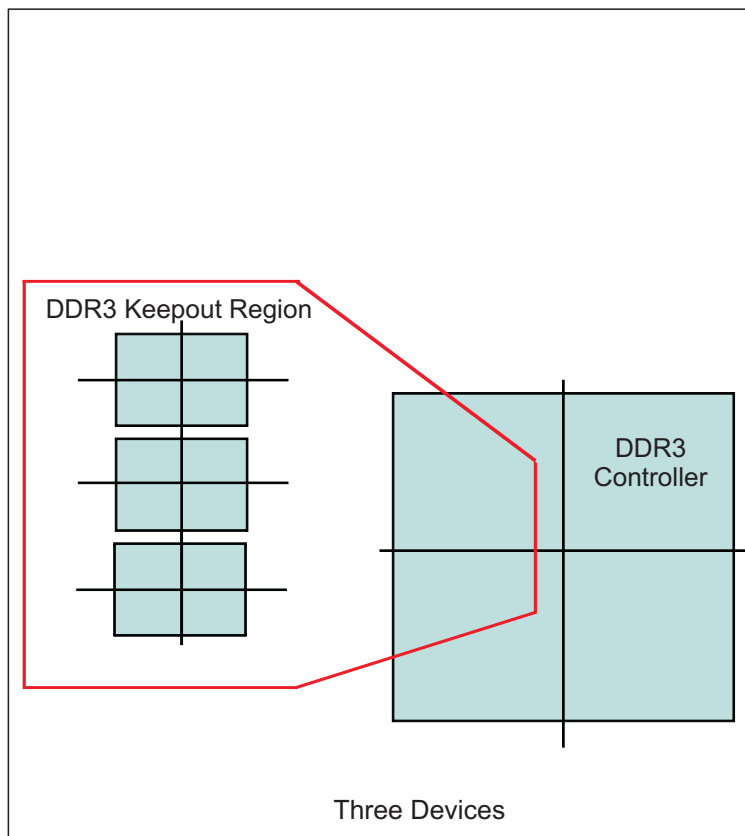
(1) DDR3 keepout region to encompass entire DDR3 routing area.

(2) Non-DDR3 signals allowed within DDR3 keepout region provided they are separated from DDR3 routing layers by a ground plane.

(3) If a device has more than one DDR controller, the signals from the other controller(s) are considered non-DDR3 and should be separated by this specification.

### 7.8.2.7 DDR3 Keepout Region

The region of the PCB used for DDR3 circuitry must be isolated from other signals. The DDR3 keepout region is defined for this purpose and is shown in [图 7-34](#). The size of this region varies with the placement and DDR routing. Additional clearances required for the keepout region are shown in [表 7-27](#). Non-DDR3 signals should not be routed on the DDR signal layers within the DDR3 keepout region. Non-DDR3 signals may be routed in the region, provided they are routed on layers separated from the DDR signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.5-V DDR3 power plane should cover the entire keepout region. Also note that the two signals from the DDR3 controller should be separated from each other by the specification in [表 7-27](#) (see [KOD37](#)).



SPRS91v\_PCB\_DDR3\_05

**图 7-34. DDR3 Keepout Region**

### 7.8.2.8 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR3 and other circuitry. 表 7-28 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DDR3 controllers and DDR3 devices. Additional bulk bypass capacitance may be needed for other circuitry.

**表 7-28. Bulk Bypass Capacitors**

| NO. | PARAMETER                                            | MIN | MAX | UNIT    |
|-----|------------------------------------------------------|-----|-----|---------|
| 1   | vdds_ddrx bulk bypass capacitor count <sup>(1)</sup> | 1   |     | Devices |
| 2   | vdds_ddrx bulk bypass total capacitance              | 22  |     | μF      |

(1) These devices should be placed near the devices they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors and DDR3 signal routing.

### 7.8.2.9 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR3 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, processor/DDR power, and processor/DDR ground connections. 表 7-29 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB. Generally speaking, it is good to:

1. Fit as many HS bypass capacitors as possible.
2. Minimize the distance from the bypass cap to the pins/balls being bypassed.
3. Use the smallest physical sized capacitors possible with the highest capacitance readily available.
4. Connect the bypass capacitor pads to their vias using the widest traces possible and using the largest hole size via possible.
5. Minimize via sharing. Note the limites on via sharing shown in 表 7-29.

**表 7-29. High-Speed Bypass Capacitors**

| NO. | PARAMETER                                                                           | MIN                           | TYP  | MAX  | UNIT    |
|-----|-------------------------------------------------------------------------------------|-------------------------------|------|------|---------|
| 1   | HS bypass capacitor package size <sup>(1)</sup>                                     |                               | 0201 | 0402 | 10 Mils |
| 2   | Distance, HS bypass capacitor to processor being bypassed <sup>(2)(3)(4)</sup>      |                               |      | 400  | Mils    |
| 3   | Processor HS bypass capacitor count per vdds_ddrx rail <sup>(12)</sup>              | See 表 7-3 and <sup>(11)</sup> |      |      | Devices |
| 4   | Processor HS bypass capacitor total capacitance per vdds_ddrx rail <sup>(12)</sup>  | See 表 7-3 and <sup>(11)</sup> |      |      | μF      |
| 5   | Number of connection vias for each device power/ground ball <sup>(5)</sup>          |                               |      |      | Vias    |
| 6   | Trace length from device power/ground ball to connection via <sup>(2)</sup>         |                               | 35   | 70   | Mils    |
| 7   | Distance, HS bypass capacitor to DDR device being bypassed <sup>(6)</sup>           |                               |      | 150  | Mils    |
| 8   | DDR3 device HS bypass capacitor count <sup>(7)</sup>                                | 12                            |      |      | Devices |
| 9   | DDR3 device HS bypass capacitor total capacitance <sup>(7)</sup>                    | 0.85                          |      |      | μF      |
| 10  | Number of connection vias for each HS capacitor <sup>(8)(9)</sup>                   | 2                             |      |      | Vias    |
| 11  | Trace length from bypass capacitor connect to connection via <sup>(2)(9)</sup>      |                               | 35   | 100  | Mils    |
| 12  | Number of connection vias for each DDR3 device power/ground ball <sup>(10)</sup>    | 1                             |      |      | Vias    |
| 13  | Trace length from DDR3 device power/ground ball to connection via <sup>(2)(8)</sup> |                               | 35   | 60   | Mils    |

(1) LxW, 10-mil units, that is, a 0402 is a 40x20-mil surface-mount capacitor.

(2) Closer/shorter is better.

(3) Measured from the nearest processor power/ground ball to the center of the capacitor package.

(4) Three of these capacitors should be located underneath the processor, between the cluster of DDR\_1V5 balls and ground balls, between the DDR interfaces on the package.

(5) See the Via Channel™ escape for the processor package.

(6) Measured from the DDR3 device power/ground ball to the center of the capacitor package.

(7) Per DDR3 device.

(8) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board. No sharing of vias is permitted on the same side of the board.

(9) An HS bypass capacitor may share a via with a DDR device mounted on the same side of the PCB. A wide trace should be used for the connection and the length from the capacitor pad to the DDR device pad should be less than 150 mils.

(10) Up to a total of two pairs of DDR power/ground balls may share a via.

(11) The capacitor recommendations in this data manual reflect only the needs of this processor. Please see the memory vendor's guidelines for determining the appropriate decoupling capacitor arrangement for the memory device itself.

(12) For more information, see 7.3, Core Power Domains.

### 7.8.2.9.1 Return Current Bypass Capacitors

Use additional bypass capacitors if the return current reference plane changes due to DDR3 signals hopping from one signal layer to another. The bypass capacitor here provides a path for the return current to hop planes along with the signal. As many of these return current bypass capacitors should be used as possible. These are returns for signal current, the signal via size may be used for these capacitors.

### 7.8.2.10 Net Classes

表 7-30 lists the clock net classes for the DDR3 interface. 表 7-31 lists the signal net classes, and associated clock net classes, for signals in the DDR3 interface. These net classes are used for the termination and routing rules that follow.

**表 7-30. Clock Net Class Definitions**

| CLOCK NET CLASS     | processor PIN NAMES    |
|---------------------|------------------------|
| CK                  | ddrx_ck/ddrx_nck       |
| DQS0                | ddrx_dqs0 / ddrx_dqsn0 |
| DQS1                | ddrx_dqs1 / ddrx_dqsn1 |
| DQS2 <sup>(1)</sup> | ddrx_dqs2 / ddrx_dqsn2 |
| DQS3 <sup>(1)</sup> | ddrx_dqs3 / ddrx_dqsn3 |

(1) Only used on 32-bit wide DDR3 memory systems.

**表 7-31. Signal Net Class Definitions**

| SIGNAL NET CLASS   | ASSOCIATED CLOCK NET CLASS | processor PIN NAMES                                                                        |
|--------------------|----------------------------|--------------------------------------------------------------------------------------------|
| ADDR_CTRL          | CK                         | ddrx_ba[2:0], ddrx_a[15:0], ddrx_csnj, ddrx_casn, ddrx_rasn, ddrx_wen, ddrx_cke, ddrx_odti |
| DQ0                | DQS0                       | ddrx_d[7:0], ddrx_dqm0                                                                     |
| DQ1                | DQS1                       | ddrx_d[15:8], ddrx_dqm1                                                                    |
| DQ2 <sup>(1)</sup> | DQS2                       | ddrx_d[23:16], ddrx_dqm2                                                                   |
| DQ3 <sup>(1)</sup> | DQS3                       | ddrx_d[31:24], ddrx_dqm3                                                                   |

(1) Only used on 32-bit wide DDR3 memory systems.

### 7.8.2.11 DDR3 Signal Termination

Signal terminators are required for the CK and ADDR\_CTRL net classes. The data lines are terminated by ODT and, thus, the PCB traces should be unterminated. Detailed termination specifications are covered in the routing rules in the following sections.

### 7.8.2.12 VTT

Like VREF, the nominal value of the VTT supply is half the DDR3 supply voltage. Unlike VREF, VTT is expected to source and sink current, specifically the termination current for the ADDR\_CTRL net class Thevenin terminators. VTT is needed at the end of the address bus and it should be routed as a power sub-plane. VTT should be bypassed near the terminator resistors.

### 7.8.2.13 CK and ADDR\_CTRL Topologies and Routing Definition

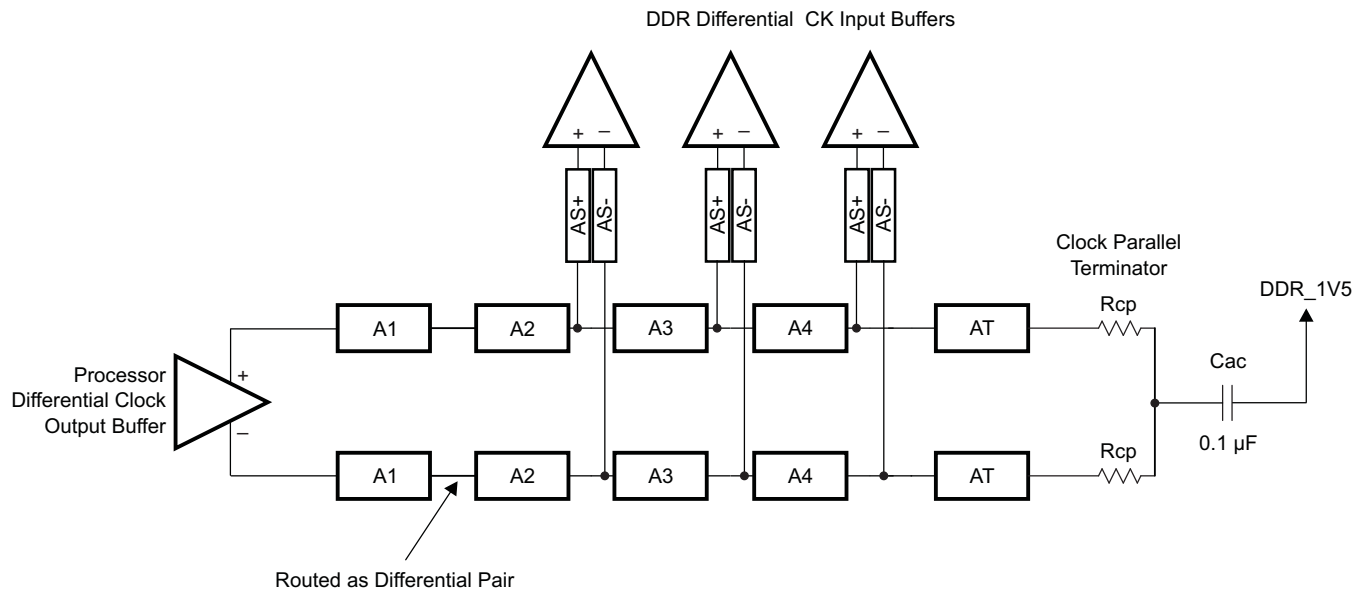
The CK and ADDR\_CTRL net classes are routed similarly and are length matched to minimize skew between them. CK is a bit more complicated because it runs at a higher transition rate and is differential. The following subsections show the topology and routing for various DDR3 configurations for CK and ADDR\_CTRL. The figures in the following subsections define the terms for the routing specification detailed in 表 7-32.

### 7.8.2.13.1 Three DDR3 Devices

Three DDR3 devices are supported on the DDR EMIF consisting of two x16 DDR3 devices and one device for ECC, arranged as one bank (CS). These three devices may be mounted on a single side of the PCB, or may be mirrored in two pairs to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

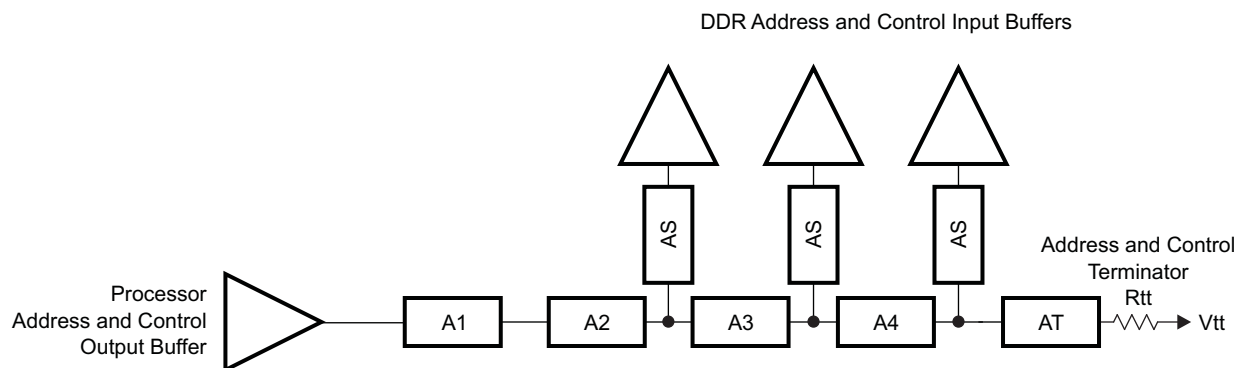
#### 7.8.2.13.1.1 CK and ADDR\_CTRL Topologies, Three DDR3 Devices

Figure 7-35 shows the topology of the CK net classes and Figure 7-36 shows the topology for the corresponding ADDR\_CTRL net classes.



SPRS91v\_PCB\_DDR3\_06

Figure 7-35. CK Topology for Three DDR3 Devices



SPRS91v\_PCB\_DDR3\_07

Figure 7-36. ADDR\_CTRL Topology for Three DDR3 Devices

#### 7.8.2.13.1.2 CK and ADDR\_CTRL Routing, Three DDR3 Devices

Figure 7-37 shows the CK routing for three DDR3 devices placed on the same side of the PCB. Figure 7-38 shows the corresponding ADDR\_CTRL routing.

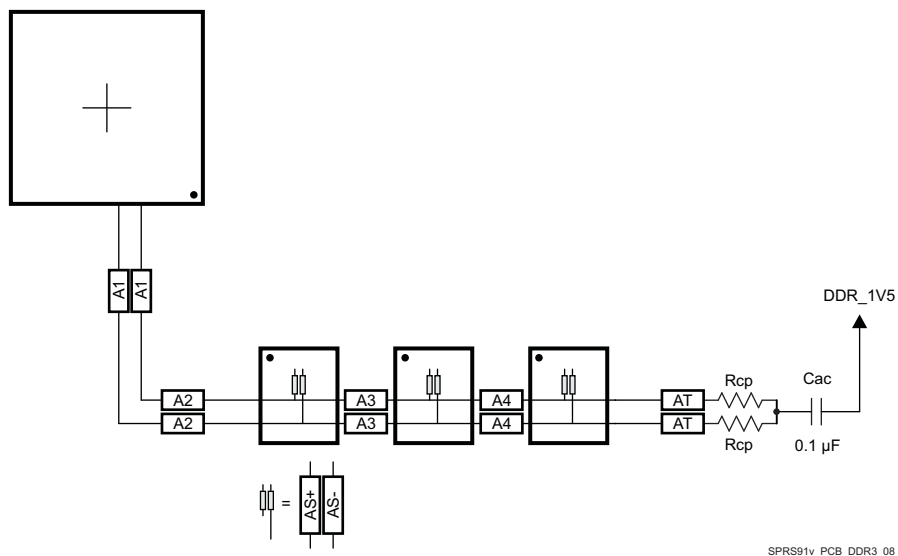


Figure 7-37. CK Routing for Three Single-Side DDR3 Devices

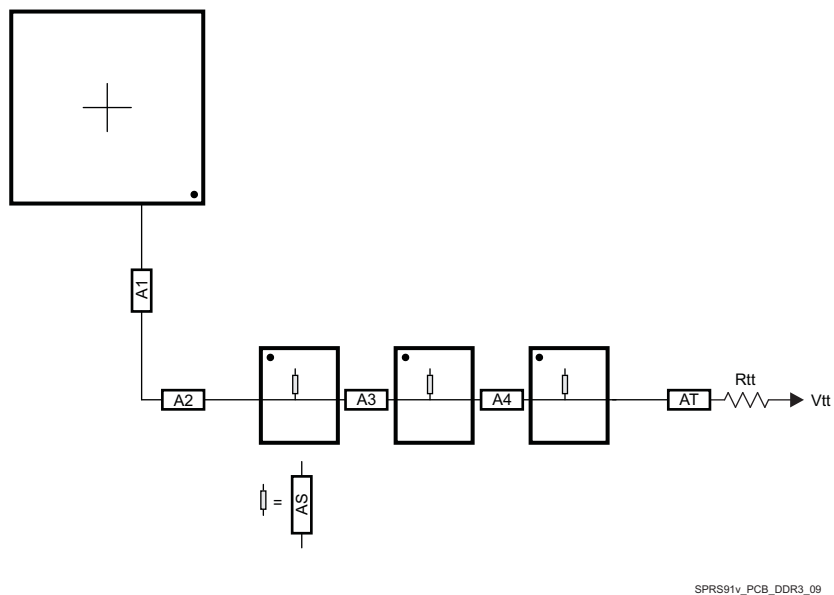
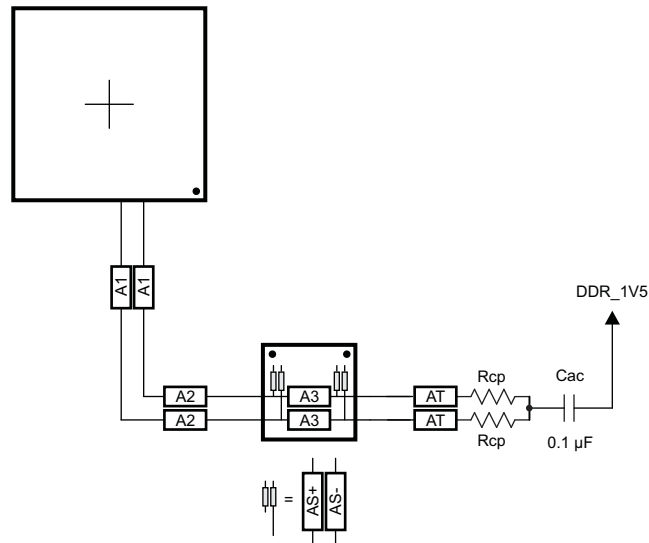


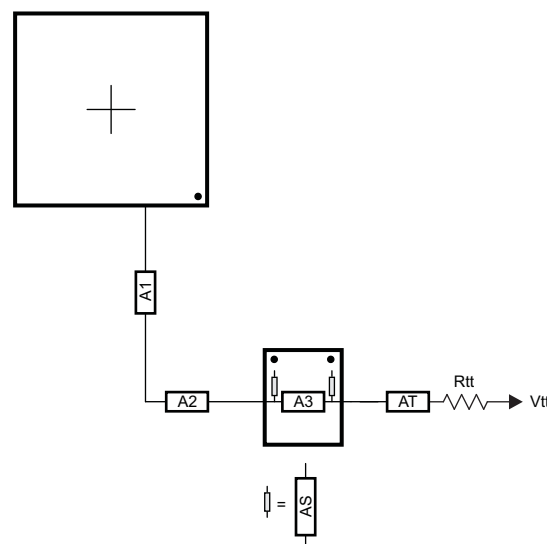
Figure 7-38. ADDR\_CTRL Routing for Three Single-Side DDR3 Devices

To save PCB space, the two DDR3 memories may be mounted as one mirrored pair at a cost of increased routing and assembly complexity. Figure 7-39 and Figure 7-40 show the routing for CK and ADDR\_CTRL, respectively, for two DDR3 devices mirrored in a pair configuration.



SPRS91v\_PCB\_DDR3\_10

7-39. CK Routing for Two Mirrored DDR3 Devices



SPRS91v\_PCB\_DDR3\_11

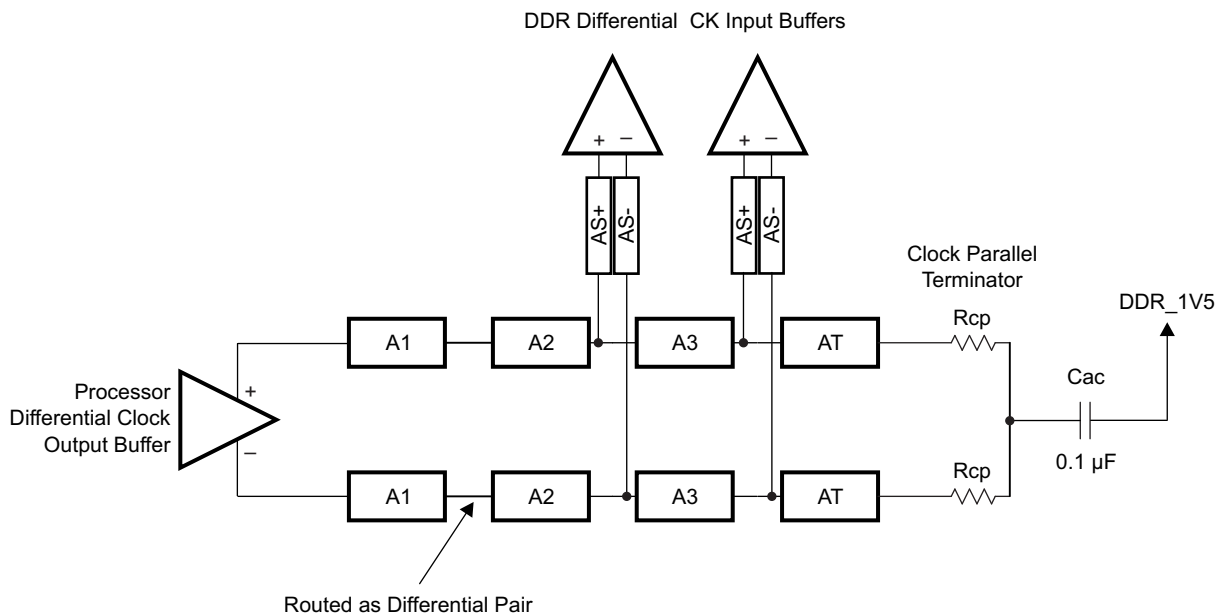
7-40. ADDR\_CTRL Routing for Two Mirrored DDR3 Devices

### 7.8.2.13.2 Two DDR3 Devices

Two DDR3 devices are supported on the DDR EMIF consisting of two x8 DDR3 devices arranged as one bank (CS), 16 bits wide, or two x16 DDR3 devices arranged as one bank (CS), 32 bits wide. These two devices may be mounted on a single side of the PCB, or may be mirrored in a pair to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

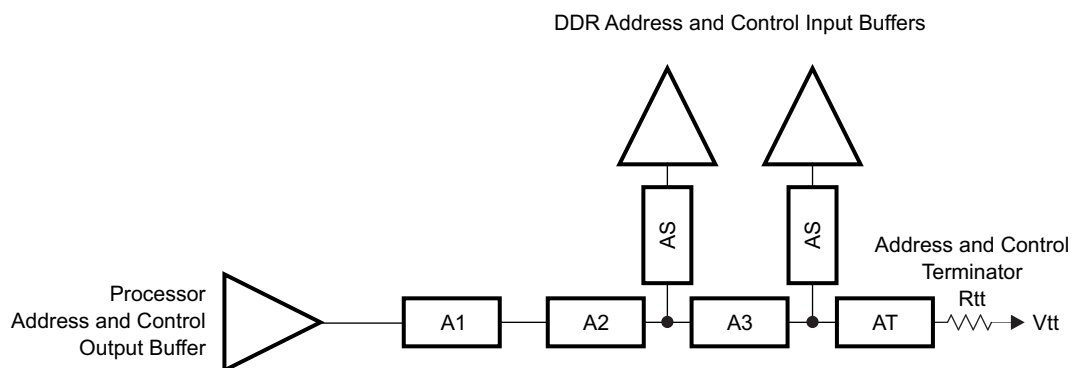
#### 7.8.2.13.2.1 CK and ADDR\_CTRL Topologies, Two DDR3 Devices

7-41 shows the topology of the CK net classes and 7-42 shows the topology for the corresponding ADDR\_CTRL net classes.



SPRS91v\_PCB\_DDR3\_12

7-41. CK Topology for Two DDR3 Devices

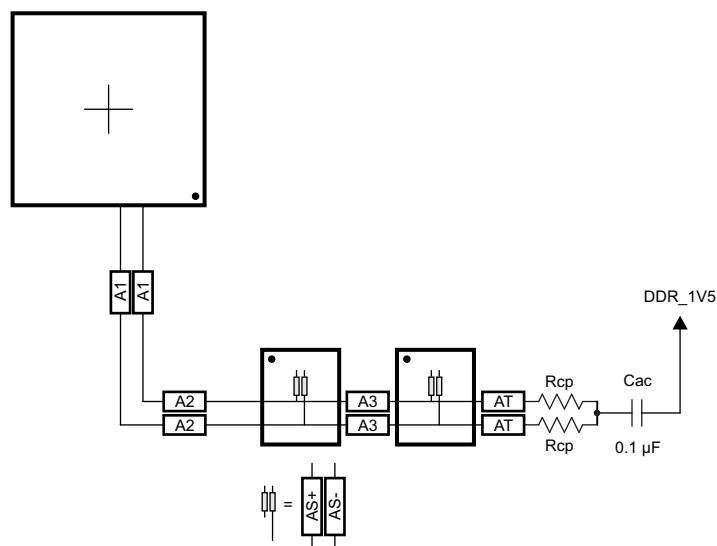


SPRS91v\_PCB\_DDR3\_13

7-42. ADDR\_CTRL Topology for Two DDR3 Devices

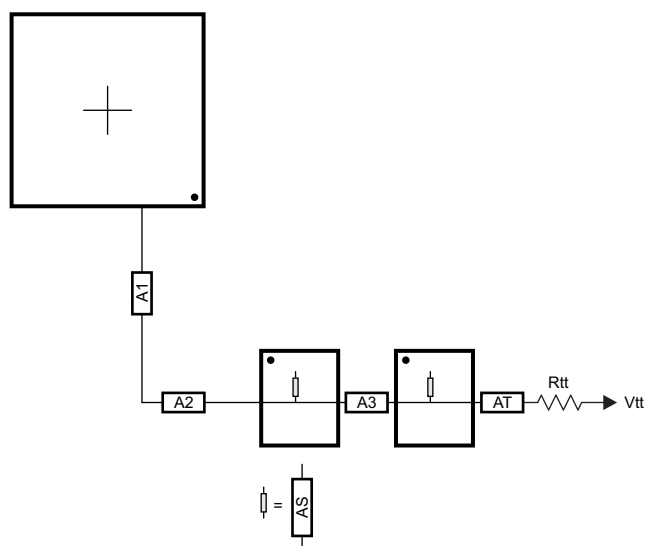
#### 7.8.2.13.2.2 CK and ADDR\_CTRL Routing, Two DDR3 Devices

7-43 shows the CK routing for two DDR3 devices placed on the same side of the PCB. 7-44 shows the corresponding ADDR\_CTRL routing.



SPRS91v\_PCB\_DDR3\_14

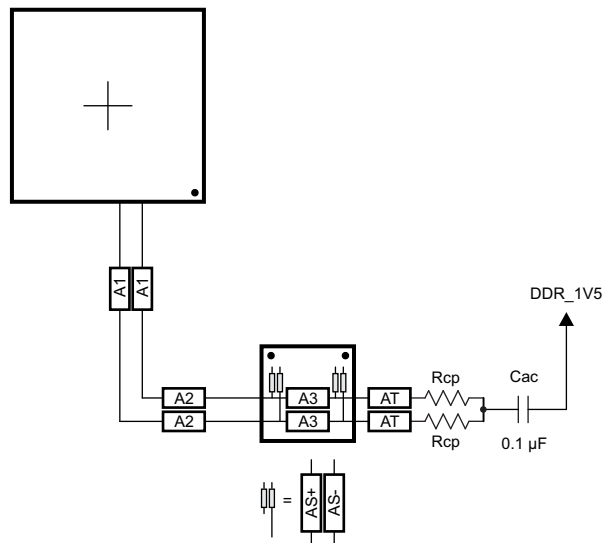
7-43. CK Routing for Two Single-Side DDR3 Devices



SPRS91v\_PCB\_DDR3\_15

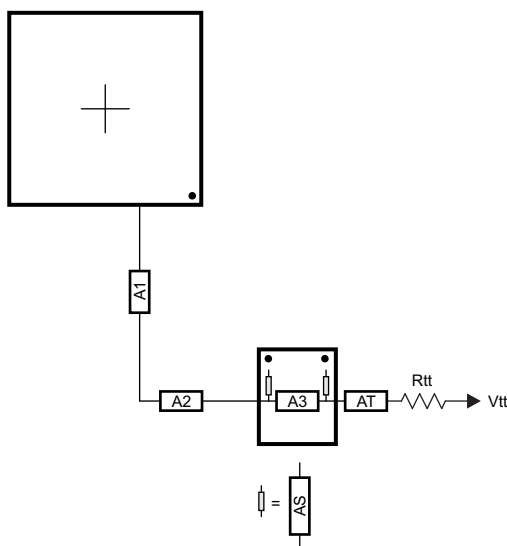
7-44. ADDR\_CTRL Routing for Two Single-Side DDR3 Devices

To save PCB space, the two DDR3 memories may be mounted as a mirrored pair at a cost of increased routing and assembly complexity. 7-45 and 7-46 show the routing for CK and ADDR\_CTRL, respectively, for two DDR3 devices mirrored in a single-pair configuration.



SPRS91v\_PCB\_DDR3\_16

**7-45. CK Routing for Two Mirrored DDR3 Devices**



SPRS91v\_PCB\_DDR3\_17

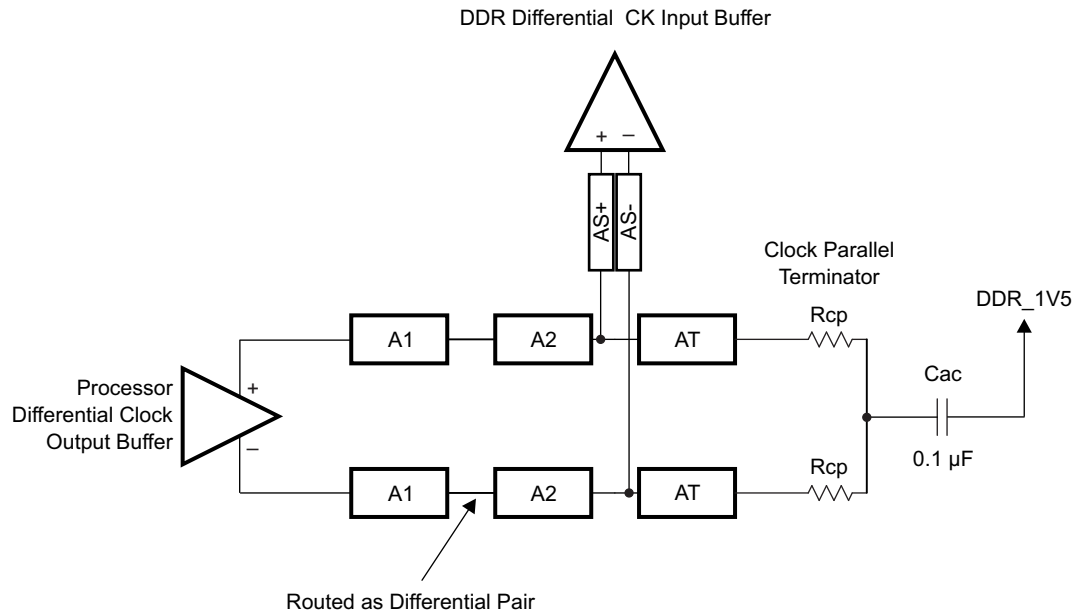
**7-46. ADDR\_CTRL Routing for Two Mirrored DDR3 Devices**

### 7.8.2.13.3 One DDR3 Device

A single DDR3 device is supported on the DDR EMIF consisting of one x16 DDR3 device arranged as one bank (CS), 16 bits wide.

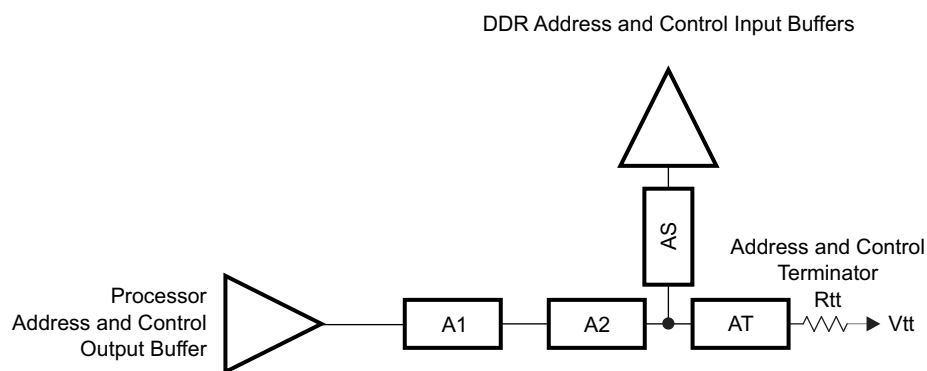
#### 7.8.2.13.3.1 CK and ADDR\_CTRL Topologies, One DDR3 Device

7-47 shows the topology of the CK net classes and 7-48 shows the topology for the corresponding ADDR\_CTRL net classes.



SPRS91v\_PCB\_DDR3\_18

✎ 7-47. CK Topology for One DDR3 Device

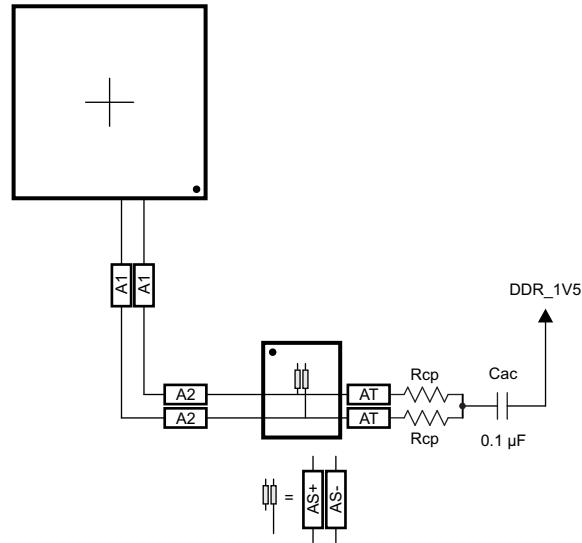


SPRS91v\_PCB\_DDR3\_19

✎ 7-48. ADDR\_CTRL Topology for One DDR3 Device

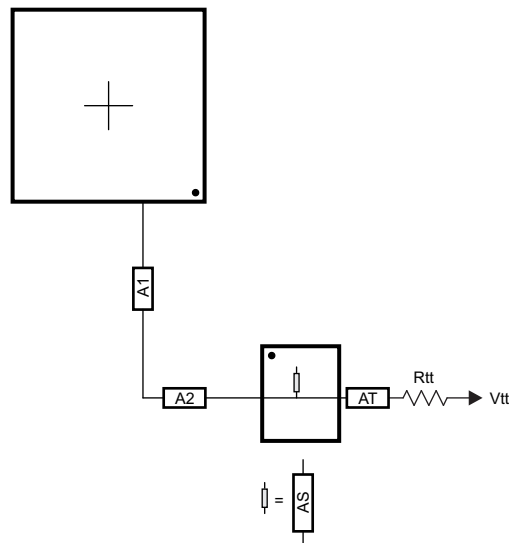
### 7.8.2.13.3.2 CK and ADDR/CTRL Routing, One DDR3 Device

✎ 7-49 shows the CK routing for one DDR3 device placed on the same side of the PCB. ✎ 7-50 shows the corresponding ADDR\_CTRL routing.



SPRS91v\_PCB\_DDR3\_20

7-49. CK Routing for One DDR3 Device



SPRS91v\_PCB\_DDR3\_21

7-50. ADDR\_CTRL Routing for One DDR3 Device

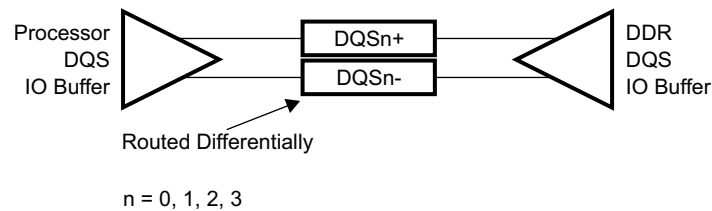
#### 7.8.2.14 Data Topologies and Routing Definition

No matter the number of DDR3 devices used, the data line topology is always point to point, so its definition is simple.

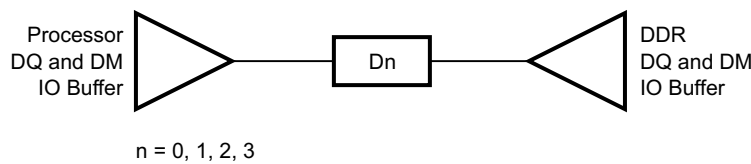
Care should be taken to minimize layer transitions during routing. If a layer transition is necessary, it is better to transition to a layer using the same reference plane. If this cannot be accommodated, ensure there are nearby ground vias to allow the return currents to transition between reference planes if both reference planes are ground or vdds\_ddr. Ensure there are nearby bypass capacitors to allow the return currents to transition between reference planes if one of the reference planes is ground. The goal is to minimize the size of the return current loops.

#### 7.8.2.14.1 DQS and DQ/DM Topologies, Any Number of Allowed DDR3 Devices

DQS lines are point-to-point differential, and DQ/DM lines are point-to-point singled ended. [Figure 7-51](#) and [Figure 7-52](#) show these topologies.



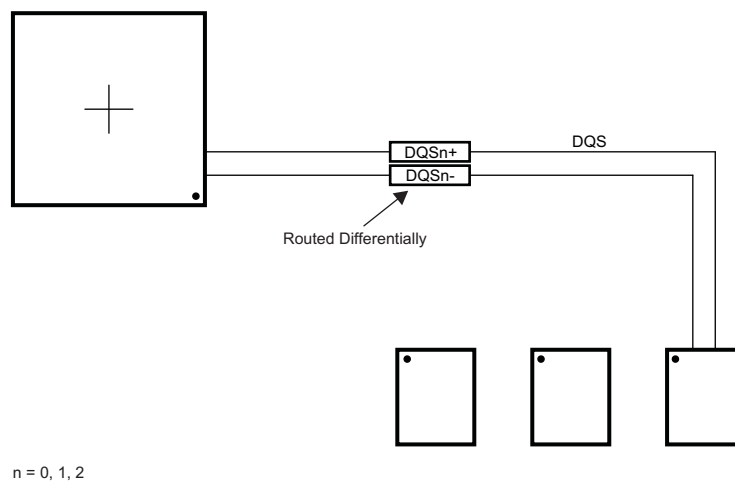
**Figure 7-51. DQS Topology**



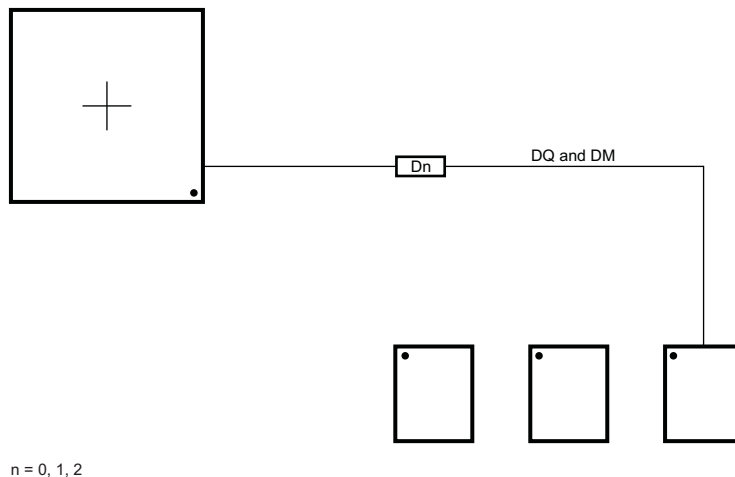
**Figure 7-52. DQ/DM Topology**

#### 7.8.2.14.2 DQS and DQ/DM Routing, Any Number of Allowed DDR3 Devices

[Figure 7-53](#) and [Figure 7-54](#) show the DQS and DQ/DM routing.



**Figure 7-53. DQS Routing With Any Number of Allowed DDR3 Devices**



SPRS91v\_PCB\_DDR3\_25

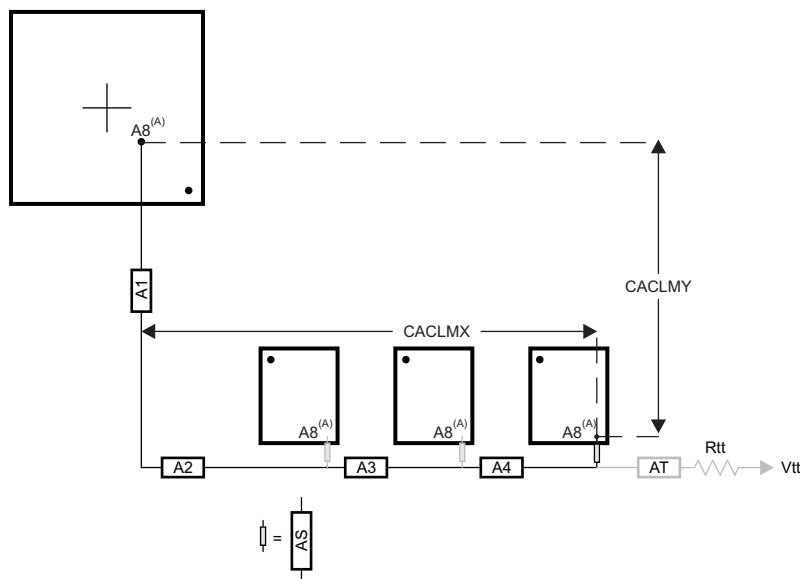
7-54. DQ/DM Routing With Any Number of Allowed DDR3 Devices

### 7.8.2.15 Routing Specification

#### 7.8.2.15.1 CK and ADDR\_CTRL Routing Specification

Skew within the CK and ADDR\_CTRL net classes directly reduces setup and hold margin and, thus, this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. A metric to establish this maximum length is Manhattan distance. The Manhattan distance between two points on a PCB is the length between the points when connecting them only with horizontal or vertical segments. A reasonable trace route length is to within a percentage of its Manhattan distance. CACLM is defined as Clock Address Control Longest Manhattan distance.

Given the clock and address pin locations on the processor and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. 7-55 and 7-56 show this distance for three loads and two loads, respectively. It is from this distance that the specifications on the lengths of the transmission lines for the address bus are determined. CACLM is determined similarly for other address bus configurations; that is, it is based on the longest net of the CK/ADDR\_CTRL net class. For CK and ADDR\_CTRL routing, these specifications are contained in 表 7-32.



SPRS91v\_PCB\_DDR3\_26

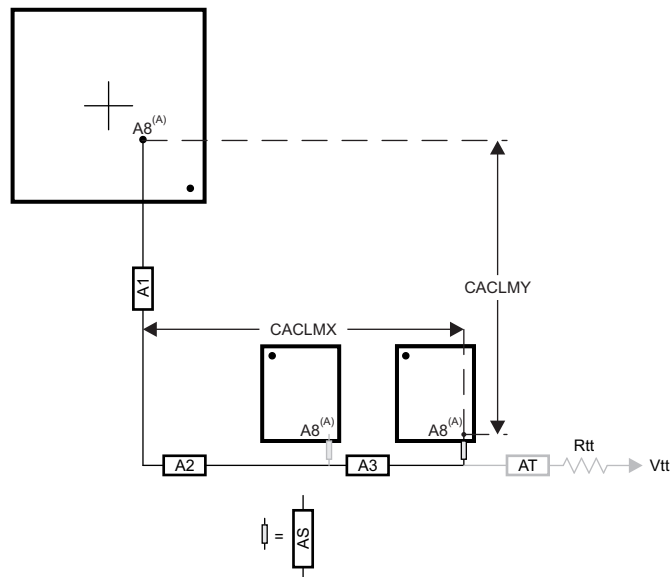
- A. It is very likely that the longest CK/ADDR\_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK/ADDR\_CTRL skew matching and length control.

The length of shorter CK/ADDR\_CTRL stubs as well as the length of the terminator stub are not included in this length calculation. Non-included lengths are grayed out in the figure.

Assuming A8 is the longest, CALM = CACLMY + CACLMX + 300 mils.

The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

#### 7-55. CACLM for Three Address Loads on One Side of PCB



SPRS91v\_PCB\_DDR3\_27

- A. It is very likely that the longest CK/ADDR\_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK/ADDR\_CTRL skew matching and length control.

The length of shorter CK/ADDR\_CTRL stubs as well as the length of the terminator stub are not included in this length calculation. Non-included lengths are grayed out in the figure.

Assuming A8 is the longest, CALM = CACLMY + CACLMX + 300 mils.

The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

**图 7-56. CACLM for Two Address Loads on One Side of PCB**

**表 7-32. CK and ADDR\_CTRL Routing Specification<sup>(2)(3)</sup>**

| NO.     | PARAMETER                                                                  | MIN | TYP | MAX                | UNIT |
|---------|----------------------------------------------------------------------------|-----|-----|--------------------|------|
| CARS31  | A1+A2 length                                                               |     |     | 500 <sup>(1)</sup> | ps   |
| CARS32  | A1+A2 skew                                                                 |     |     | 29                 | ps   |
| CARS33  | A3 length                                                                  |     |     | 125                | ps   |
| CARS34  | A3 skew <sup>(4)</sup>                                                     |     |     | 6                  | ps   |
| CARS35  | A3 skew <sup>(5)</sup>                                                     |     |     | 6                  | ps   |
| CARS36  | A4 length                                                                  |     |     | 125                | ps   |
| CARS37  | A4 skew                                                                    |     |     | 6                  | ps   |
| CARS38  | AS length                                                                  |     | 5   | 17 <sup>(1)</sup>  | ps   |
| CARS39  | AS skew                                                                    |     | 1.3 | 14 <sup>(1)</sup>  | ps   |
| CARS310 | AS+/AS- length                                                             |     | 5   | 12                 | ps   |
| CARS311 | AS+/AS- skew                                                               |     |     | 1                  | ps   |
| CARS312 | AT length <sup>(6)</sup>                                                   |     | 75  |                    | ps   |
| CARS313 | AT skew <sup>(7)</sup>                                                     |     | 14  |                    | ps   |
| CARS314 | AT skew <sup>(8)</sup>                                                     |     |     | 1                  | ps   |
| CARS315 | CK/ADDR_CTRL trace length                                                  |     |     | 1020               | ps   |
| CARS316 | Vias per trace                                                             |     |     | 3 <sup>(1)</sup>   | vias |
| CARS317 | Via count difference                                                       |     |     | 1 <sup>(15)</sup>  | vias |
| CARS318 | Center-to-center CK to other DDR3 trace spacing <sup>(9)</sup>             | 4w  |     |                    |      |
| CARS319 | Center-to-center ADDR_CTRL to other DDR3 trace spacing <sup>(9)(10)</sup>  | 4w  |     |                    |      |
| CARS320 | Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing <sup>(9)</sup> | 3w  |     |                    |      |

表 7-32. CK and ADDR\_CTRL Routing Specification<sup>(2)(3)</sup> (continued)

| NO.     | PARAMETER                                       | MIN  | TYP | MAX  | UNIT |
|---------|-------------------------------------------------|------|-----|------|------|
| CARS321 | CK center-to-center spacing <sup>(11)(12)</sup> |      |     |      |      |
| CARS322 | CK spacing to other net <sup>(9)</sup>          | 4w   |     |      |      |
| CARS323 | Rcp <sup>(13)</sup>                             | Z0-1 | Z0  | Z0+1 | Ω    |
| CARS324 | Rtt <sup>(13)(14)</sup>                         | Z0-5 | Z0  | Z0+5 | Ω    |

- (1) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.
- (2) The use of vias should be minimized.
- (3) Additional bypass capacitors are required when using the DDR\_1V5 plane as the reference plane to allow the return current to jump between the DDR\_1V5 plane and the ground plane when the net class switches layers at a via.
- (4) Non-mirrored configuration (all DDR3 memories on same side of PCB).
- (5) Mirrored configuration (one DDR3 device on top of the board and one DDR3 device on the bottom).
- (6) While this length can be increased for convenience, its length should be minimized.
- (7) ADDR\_CTRL net class only (not CK net class). Minimizing this skew is recommended, but not required.
- (8) CK net class only.
- (9) Center-to-center spacing is allowed to fall to minimum (2w) for up to 1250 mils of routed length.
- (10) The ADDR\_CTRL net class of the other DDR EMIF is considered *other DDR3 trace spacing*.
- (11) CK spacing set to ensure proper differential impedance.
- (12) The most important thing to do is control the impedance so inadvertent impedance mismatches are not created. Generally speaking, center-to-center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the singleended impedance, Z0.
- (13) Source termination (series resistor at driver) is specifically not allowed.
- (14) Termination values should be uniform across the net class.
- (15) Via count difference may increase by 1 only if accurate 3-D modeling of the signal flight times – including accurately modeled signal propagation through vias – has been applied to ensure all segment skew maximums are not exceeded.

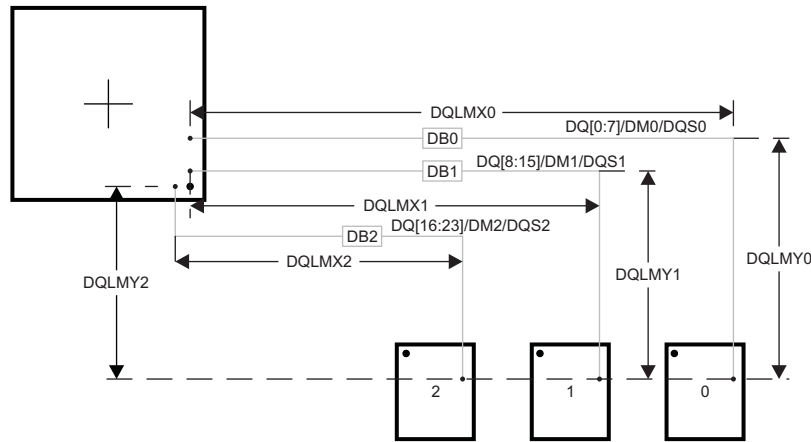
#### 7.8.2.15.2 DQS and DQ Routing Specification

Skew within the DQS and DQ/DM net classes directly reduces setup and hold margin and thus this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. As with CK and ADDR\_CTRL, a reasonable trace route length is to within a percentage of its Manhattan distance. DQLMn is defined as DQ Longest Manhattan distance n, where n is the byte number. For a 32-bit interface, there are three DQLMs, DQLM0-DQLM2. Likewise, for a 16-bit interface, there are two DQLMs, DQLM0-DQLM1.

#### 注

It is not required, nor is it recommended, to match the lengths across all bytes. Length matching is only required within each byte.

Given the DQS and DQ/DM pin locations on the processor and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. [图 7-57](#) shows this distance for four loads. It is from this distance that the specifications on the lengths of the transmission lines for the data bus are determined. For DQS and DQ/DM routing, these specifications are contained in [表 7-33](#).



DB0 - DB2 represent data bytes 0 - 2.

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There are three DQLMs, one for each byte (32-bit interface). Each DQLM is the longest Manhattan distance of the byte; therefore:

$$DQLM0 = DQLMX0 + DQLMY0$$

$$DQLM1 = DQLMX1 + DQLMY1$$

$$DQLM2 = DQLMX2 + DQLMY2$$

**图 7-57. DQLM for Any Number of Allowed DDR3 Devices**

**表 7-33. Data Routing Specification<sup>(2)</sup>**

| NO.    | PARAMETER                                                       | MIN | TYP | MAX               | UNIT             |
|--------|-----------------------------------------------------------------|-----|-----|-------------------|------------------|
| DRS31  | DB0 length                                                      |     |     | 340               | ps               |
| DRS32  | DB1 length                                                      |     |     | 340               | ps               |
| DRS33  | DB2 length                                                      |     |     | 340               | ps               |
| DRS35  | DBn skew <sup>(3)</sup>                                         |     |     | 5                 | ps               |
| DRS36  | DQSn+ to DQSn- skew                                             |     |     | 1                 | ps               |
| DRS37  | DQSn to DBn skew <sup>(3)(4)</sup>                              |     |     | 5 <sup>(10)</sup> | ps               |
| DRS38  | Vias per trace                                                  |     |     | 2 <sup>(1)</sup>  | vias             |
| DRS39  | Via count difference                                            |     |     | 0 <sup>(10)</sup> | vias             |
| DRS310 | Center-to-center DBn to other DDR3 trace spacing <sup>(6)</sup> | 4   |     |                   | w <sup>(5)</sup> |
| DRS311 | Center-to-center DBn to other DBn trace spacing <sup>(7)</sup>  | 3   |     |                   | w <sup>(5)</sup> |
| DRS312 | DQSn center-to-center spacing <sup>(8)(9)</sup>                 |     |     |                   |                  |
| DRS313 | DQSn center-to-center spacing to other net                      | 4   |     |                   | w <sup>(5)</sup> |

(1) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.

(2) External termination disallowed. Data termination should use built-in ODT functionality.

(3) Length matching is only done within a byte. Length matching across bytes is neither required nor recommended.

(4) Each DQS pair is length matched to its associated byte.

(5) Center-to-center spacing is allowed to fall to minimum (2w) for up to 1250 mils of routed length.

(6) Other DDR3 trace spacing means other DDR3 net classes not within the byte.

(7) This applies to spacing within the net classes of a byte.

(8) DQS pair spacing is set to ensure proper differential impedance.

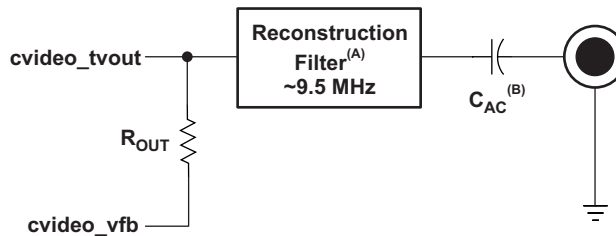
(9) The most important thing to do is control the impedance so inadvertent impedance mismatches are not created. Generally speaking, center-to-center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the singleended impedance, Zo.

(10) Via count difference may increase by 1 only if accurate 3-D modeling of the signal flight times – including accurately modeled signal propagation through vias – has been applied to ensure DBn skew and DQSn to DBn skew maximums are not exceeded.

## 7.9 CVIDEO/SD-DAC Guidelines and Electrical Data/Timing

The device's analog video CVIDEO/SD-DAC TV analog composite output can be operate in one of two modes: Normal mode and TVOUT Bypass mode. In Normal mode, the device's internal video amplifier is used. In TVOUT Bypass mode, the internal video amplifier is bypassed and an external amplifier is required.

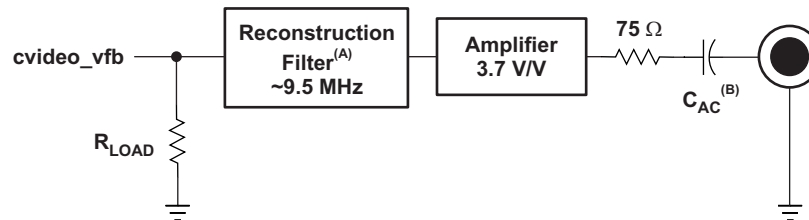
☒ 7-58 shows a typical circuit that permits connecting the analog video output from the device to standard 75-Ω impedance video systems in Normal mode.



- A. Reconstruction Filter (optional)  
B. AC coupling capacitor (optional)

☒ 7-58. TV Output (Normal Mode)

☒ 7-59 shows a typical circuit that permits connecting the analog video output from the device to standard 75-Ω impedance video systems in TVOUT Bypass mode.



- A. Reconstruction Filter (optional). Note: An amplifier with an integrated reconstruction filter can alternatively be used instead of a discrete reconstruction filter.  
B. AC coupling capacitor (optional)

☒ 7-59. TV Output (TVOUT Bypass Mode)

During board design, the onboard traces and parasitics must be matched for the channel. The video DAC output pins (cvideo\_tvout / cvideo\_vfb) are very high-frequency analog signals and must be routed with extreme care. As a result, the paths of these signals must be as short as possible, and as isolated as possible from other interfering signals. In TVOUT Bypass mode, the load resistor and amplifier/buffer should be placed as close as possible to the cvideo\_vfb pin. Other layout guidelines include:

- Take special care to bypass the vdda\_dac power supply pin with a capacitor.
- In **TVOUT Bypass mode**, place the  $R_{LOAD}$  resistor as close as possible to the Reconstruction Filter and Amplifier. In addition, place the 75-Ω resistor as close as possible (< 0.5 inch) to the Amplifier/buffer output pin. To maintain a high-quality video signal, the onboard traces after the 75-Ω resistor should have a characteristic impedance of 75 Ω ( $\pm 20\%$ ).
- In **Normal mode**, cvideo\_vfb is the most sensitive pin in the TV out system. The  $R_{OUT}$  resistor should be placed as close as possible to the device pins. To maintain a high-quality video signal, the onboard traces leading to the cvideo\_tvout pin should have a characteristic impedance of 75 Ω ( $\pm 20\%$ ) starting from the closest possible place to the device pin output.
- Minimize input trace lengths to the device to reduce parasitic capacitance.
- Include solid ground return paths.
- Match trace lengths as close as possible within a video format group.

表 7-34 和 表 7-35 present the Static and Dynamic CVIDEO / SD-DAC TV analog composite output specifications

**表 7-34. Static CVIDEO/SD-DAC Specifications**

| PARAMETER                                                              | TEST CONDITIONS                                | MIN                                  | TYP   | MAX   | UNIT     |
|------------------------------------------------------------------------|------------------------------------------------|--------------------------------------|-------|-------|----------|
| Reference Current Setting Resistor ( $R_{SET}$ )                       | Normal Mode                                    | 4653                                 | 4700  | 4747  | $\Omega$ |
|                                                                        | TVOUT Bypass Mode                              | 9900                                 | 10000 | 10100 | $\Omega$ |
| Output resistor between cvideo_tvout and cvideo_vfb pins ( $R_{OUT}$ ) | Normal Mode                                    | 2673                                 | 2700  | 2727  | $\Omega$ |
|                                                                        | TVOUT Bypass Mode                              | N/A                                  |       |       |          |
| Load Resistor ( $R_{LOAD}$ )                                           | Normal Mode                                    | 75- $\Omega$ Inside the Display      |       |       |          |
|                                                                        | TVOUT Bypass Mode                              | 1485                                 | 1500  | 1515  | $\Omega$ |
| AC-Coupling Capacitor (Optional) [ $C_{AC}$ ]                          | Normal Mode                                    | 220                                  |       |       | $\mu F$  |
|                                                                        | TVOUT Bypass Mode                              | See External Amplifier Specification |       |       |          |
| Total Capacitance from cvideo_tvout to vssa_dac                        | Normal Mode                                    |                                      |       | 300   | pF       |
|                                                                        | TVOUT Bypass Mode                              | N/A                                  |       |       |          |
| Resolution                                                             |                                                |                                      | 10    |       | Bits     |
| Integral Non-Linearity (INL), Best Fit                                 | Normal Mode                                    | -4                                   |       | 4     | LSB      |
|                                                                        | TVOUT Bypass Mode                              | -1                                   |       | 1     | LSB      |
| Differential Non-Linearity (DNL)                                       | Normal Mode                                    | -2.5                                 |       | 2.5   | LSB      |
|                                                                        | TVOUT Bypass Mode                              | -1                                   |       | 1     | LSB      |
| Full-Scale Output Voltage                                              | Normal Mode ( $R_{LOAD} = 75 \Omega$ )         |                                      | 1.3   |       | V        |
|                                                                        | TVOUT Bypass Mode ( $R_{LOAD} = 1.5 k\Omega$ ) |                                      | 0.7   |       | V        |
| Full-Scale Output Current                                              | Normal Mode                                    | N/A                                  |       |       |          |
|                                                                        | TVOUT Bypass Mode                              |                                      | 470   |       | $\mu A$  |
| Gain Error                                                             | Normal Mode (Composite) and TVOUT Bypass Mode  | -10                                  |       | 10    | %FS      |
|                                                                        | Normal Mode (S-Video)                          | -20                                  |       | 20    | %FS      |
| Gain Mismatch (Luma-to-Chroma)                                         | Normal Mode (Composite)                        | N/A                                  |       |       |          |
|                                                                        | Normal Mode (S-Video)                          | -10                                  |       | 10    | %        |
| Output Impedance                                                       | Looking into cvideo_tvout nodes                |                                      | 75    |       | $\Omega$ |

**表 7-35. Dynamic CVIDEO/SD-DAC Specifications**

| PARAMETER                                           | TEST CONDITIONS                                        | MIN | TYP | MAX | UNIT |
|-----------------------------------------------------|--------------------------------------------------------|-----|-----|-----|------|
| Output Update Rate ( $F_{CLK}$ )                    |                                                        |     | 54  | 60  | MHz  |
| Signal Bandwidth                                    | 3 dB                                                   |     | 6   |     | MHz  |
| Spurious-Free Dynamic Range (SFDR) within bandwidth | $F_{CLK} = 54 \text{ MHz}$ , $F_{OUT} = 1 \text{ MHz}$ |     | 50  |     | dBc  |
| Signal-to-Noise Ratio (SNR)                         | $F_{CLK} = 54 \text{ MHz}$ , $F_{OUT} = 1 \text{ MHz}$ |     | 54  |     | dB   |
| Power Supply Rejection (PSR)                        | Normal Mode, 100 mVpp @ 6 MHz on vdda_dac              |     | 6   |     | dB   |
|                                                     | TVOUT Bypass Mode, 100 mVpp @ 6 MHz on vdda_dac        |     | 20  |     |      |

## 8 Device and Documentation Support

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules are listed below.

### 8.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, DRA78x). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

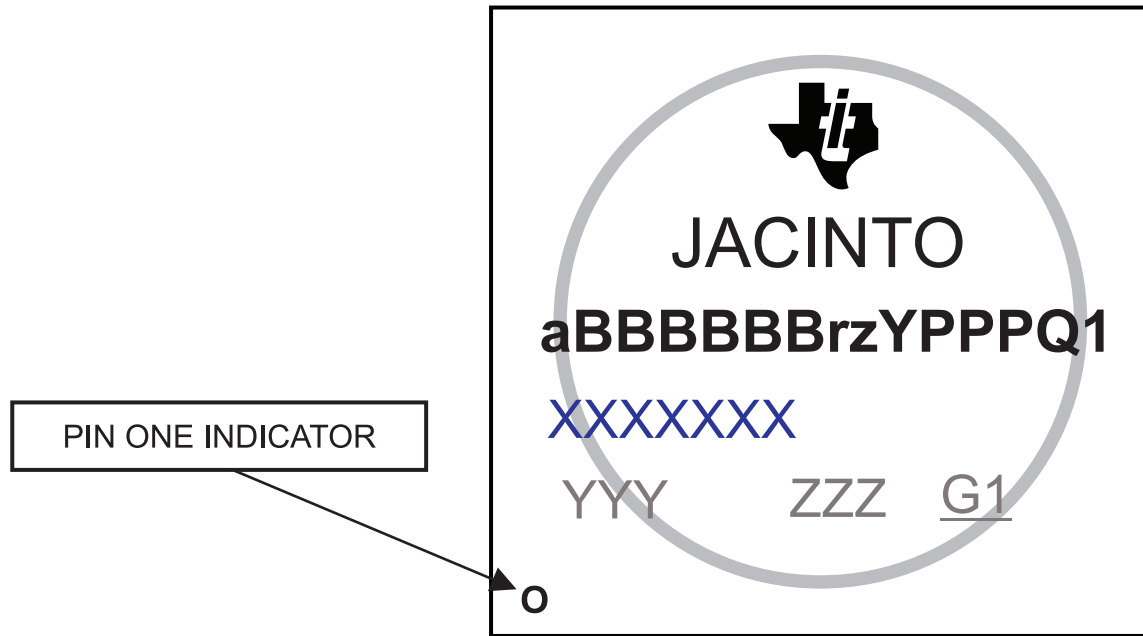
For orderable part numbers of DRA78x devices in the ABF package type, see the Package Option Addendum of this document, the TI website ([www.ti.com](http://www.ti.com)), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the [DRA78x SoC for Automotive Infotainment Silicon Revision 2.0](#).

#### 8.1.1 Standard Package Symbolization

##### 注

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.



SPRS975\_PACK\_01

图 8-1. Printed Device Reference

## 8.1.2 Device Naming Convention

表 8-1. Nomenclature Description

| FIELD PARAMETER       | FIELD DESCRIPTION                     | VALUE  | DESCRIPTION                                                                                                                     |
|-----------------------|---------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------|
| a                     | Device evolution stage <sup>(1)</sup> | X      | Prototype                                                                                                                       |
|                       |                                       | P      | Preproduction (production test flow, no reliability data)                                                                       |
|                       |                                       | BLANK  | Production                                                                                                                      |
| BBBBBB <sup>(2)</sup> | Base production part number           | DRA780 | Indicates base production part number. For more information see 表 3-1, <i>Device Comparison Table</i> .                         |
|                       |                                       | DRA781 |                                                                                                                                 |
|                       |                                       | DRA782 |                                                                                                                                 |
|                       |                                       | DRA783 |                                                                                                                                 |
|                       |                                       | DRA784 |                                                                                                                                 |
|                       |                                       | DRA785 |                                                                                                                                 |
|                       |                                       | DRA786 |                                                                                                                                 |
|                       |                                       | DRA787 |                                                                                                                                 |
|                       |                                       | DRA788 |                                                                                                                                 |
| r                     | Device revision                       | BLANK  | SR 1.0                                                                                                                          |
|                       |                                       | A      | SR 1.0A                                                                                                                         |
|                       |                                       | B      | SR 2.0                                                                                                                          |
| z                     | Device Speed                          | D      | Indicates the speed grade for each of the cores in the device. For more information see 表 3-1, <i>Device Comparison Table</i> . |
|                       |                                       | R      |                                                                                                                                 |
|                       |                                       | S      |                                                                                                                                 |
|                       |                                       | OTHER  |                                                                                                                                 |
| Y                     | Device type                           | G      | General purpose (Prototype and Production)                                                                                      |
|                       |                                       | E      | Emulation (E) devices                                                                                                           |
|                       |                                       | D      | High security prototype devices with TI Development keys (D)                                                                    |
|                       |                                       | Yn     | Letter followed by number indicates HS device with customer key                                                                 |
| PPP                   | Package designator                    | ABF    | ABF FCBGA-N367 (15mm x 15mm) Package                                                                                            |

表 8-1. Nomenclature Description (continued)

| FIELD PARAMETER | FIELD DESCRIPTION                | VALUE | DESCRIPTION                                                         |
|-----------------|----------------------------------|-------|---------------------------------------------------------------------|
| Q1              | Automotive Designator            | BLANK | Not meeting automotive qualification                                |
|                 |                                  | Q1    | Meeting Q100 equal requirements, with exceptions as specified in DM |
| XXXXXXX         | Lot Trace Code                   |       |                                                                     |
| YYY             | Production Code, For TI use only |       |                                                                     |
| ZZZ             | Production Code, For TI use only |       |                                                                     |
| O               | Pin one designator               |       |                                                                     |
| G1              | ECAT—Green package designator    |       |                                                                     |

- (1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices. Prototype devices are shipped against the following disclaimer:  
"This product is still in development and is intended for internal evaluation purposes."  
Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.
- (2) XTDA3SX is the base part number for the superset device. Software should constrain the features used to match the intended production device.

注

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

## 8.2 Tools and Software

The following products support development for DRA78x platforms:

### Design Kits and Evaluation Modules

#### DRA78X Evaluation Module

The Jacinto™ DRA78x evaluation module (EVM) is an evaluation platform designed to speed up development efforts and reduce time-to-market for Radio Signal Processor (RSP) applications. The EVM also integrates a host of peripherals including multicamera interfaces (both parallel and serial) displays, CAN, and GigB Ethernet AVB. The EVM also integrates key peripherals such as Ethernet, FPD-Link and HDMI.

### Software

#### Processor Software Development Kit for DRA7x Jacinto™ Processors – Linux, Android, and RTOS

Processor SDK Linux Automotive is the foundational software development platform for TI's Jacinto™ DRAx family of Infotainment SoCs. The software framework allows users to develop feature-rich Infotainment solutions such as reconfigurable digital instrument cluster, integrated cockpit, in-vehicle infotainment, telematics, rear seat entertainment, etc for next generation automobiles. The SDK is based on common Processor SDK platform.

### Development Tools

#### Clock Tree Tool for Sitara, Automotive, Vision Analytics, & Digital Signal Processors

The Clock Tree Tool (CTT) for Sitara™ ARM®, Automotive, and Digital Signal Processors is an interactive clock tree configuration software that provides information about the clocks and modules in these TI devices. It allows the user to: Visualize the device clock tree. Interact with clock tree elements and view the effect on PRCM registers. Interact with the PRCM registers and view the effect on the device clock tree. View a trace of all the device registers affected by the user interaction with clock tree.

### Models

**DRA78X BSDL Model** BSDL Model

**DRA78X IBIS Model** IBIS Model

**DRA78x Thermal Model** Thermal Model

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at [www.ti.com](http://www.ti.com). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

### 8.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the DRA78x devices.

#### Technical Reference Manual

##### **DRA78x SoC for Automotive Infotainment Silicon Revision 2.0**

Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the DRA78x family of devices.

#### Errata

##### **DRA78x SoC for Automotive Infotainment Silicon Revision 2.0**

Describes the known exceptions to the functional specifications for the device.

### 8.4 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**表 8-2. Related Links**

| PARTS  | PRODUCT FOLDER             | ORDER NOW                  | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|--------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| DRA780 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DRA781 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DRA782 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DRA783 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DRA784 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DRA785 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DRA786 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DRA787 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DRA788 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 8.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**TI Embedded Processors Wiki** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

### 8.6 商標

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JTAG is a registered trademark of JTAG Technologies, Inc.  
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MMC is a trademark of MultiMediaCard Association.  
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HD Radio is a trademark of iBiquity Digital Corporation.  
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## 8.9 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

## 9 Mechanical, Packaging, and Orderable Information

### 9.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                         |
|-----------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------------------------------|
| DRA780BDGABFQ1        | Active        | Production           | FCBGA (ABF)   367 | 90   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 125   | DRA780BDGABFQ1<br>JACINTO<br>775<br>775 ABF |
| DRA780BDGABFRQ1       | Active        | Production           | FCBGA (ABF)   367 | 750   LARGE T&R       | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 125   | DRA780BDGABFQ1<br>JACINTO<br>775<br>775 ABF |
| DRA781BRGABFQ1        | Active        | Production           | FCBGA (ABF)   367 | 90   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 125   | DRA781BRGABFQ1<br>JACINTO<br>775<br>775 ABF |
| DRA781BRGABFRQ1       | Active        | Production           | FCBGA (ABF)   367 | 750   LARGE T&R       | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 125   | DRA781BRGABFQ1<br>JACINTO<br>775<br>775 ABF |
| DRA782BDGABFQ1        | Active        | Production           | FCBGA (ABF)   367 | 90   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 125   | DRA782BDGABFQ1<br>775<br>775 ABF            |
| DRA782BDGABFRQ1       | Active        | Production           | FCBGA (ABF)   367 | 750   LARGE T&R       | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 125   | DRA782BDGABFQ1<br>775<br>775 ABF            |
| DRA783BRGABFQ1        | Active        | Production           | FCBGA (ABF)   367 | 90   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 125   | DRA783BRGABFQ1<br>JACINTO<br>775<br>775 ABF |
| DRA786BDGABFQ1        | Active        | Production           | FCBGA (ABF)   367 | 90   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 125   | DRA786BDGABFQ1<br>JACINTO<br>775<br>775 ABF |
| DRA786BDGABFRQ1       | Active        | Production           | FCBGA (ABF)   367 | 750   LARGE T&R       | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 125   | DRA786BDGABFQ1<br>JACINTO<br>775<br>775 ABF |

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                         |
|-----------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------------------------------|
| DRA787BRGABFQ1        | Active        | Production           | FCBGA (ABF)   367 | 90   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 125   | DRA787BRGABFQ1<br>JACINTO<br>775<br>775 ABF |
| DRA787BRGABFRQ1       | Active        | Production           | FCBGA (ABF)   367 | 750   LARGE T&R       | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 125   | DRA787BRGABFQ1<br>JACINTO<br>775<br>775 ABF |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

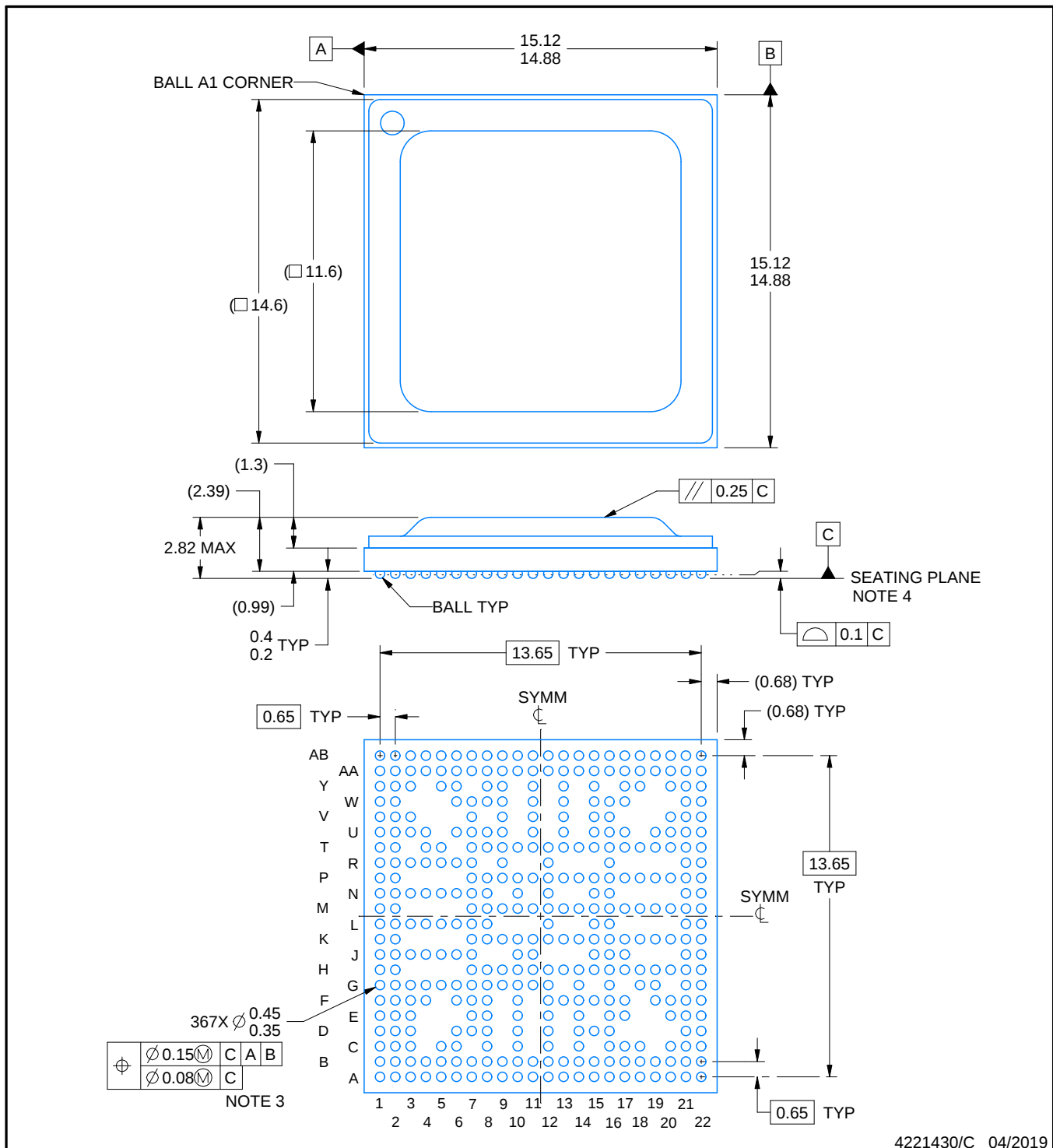
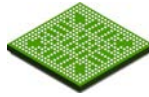
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## NOTES:

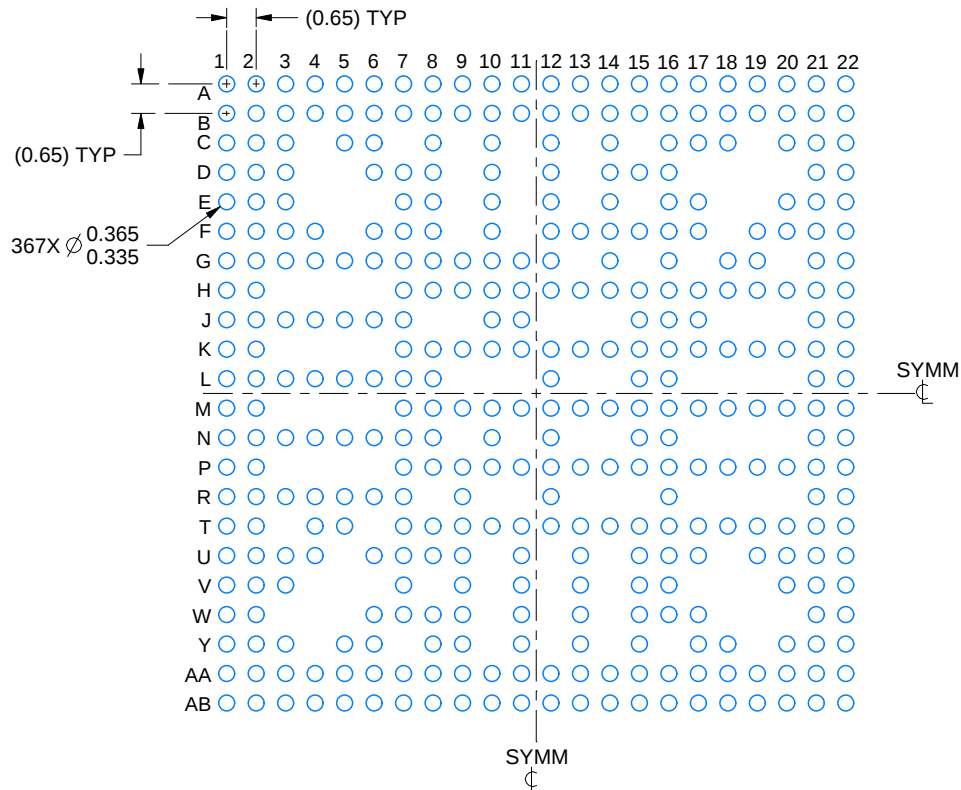
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crown of the solder balls.

# EXAMPLE BOARD LAYOUT

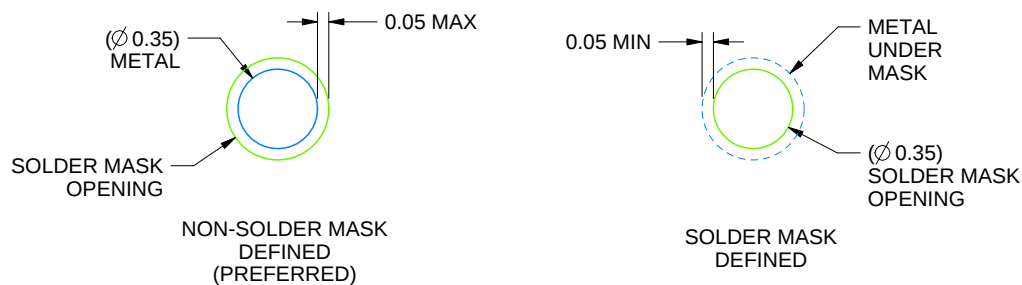
ABF0367A

FCBGA - 2.82 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS  
NOT TO SCALE

4221430/C 04/2019

NOTES: (continued)

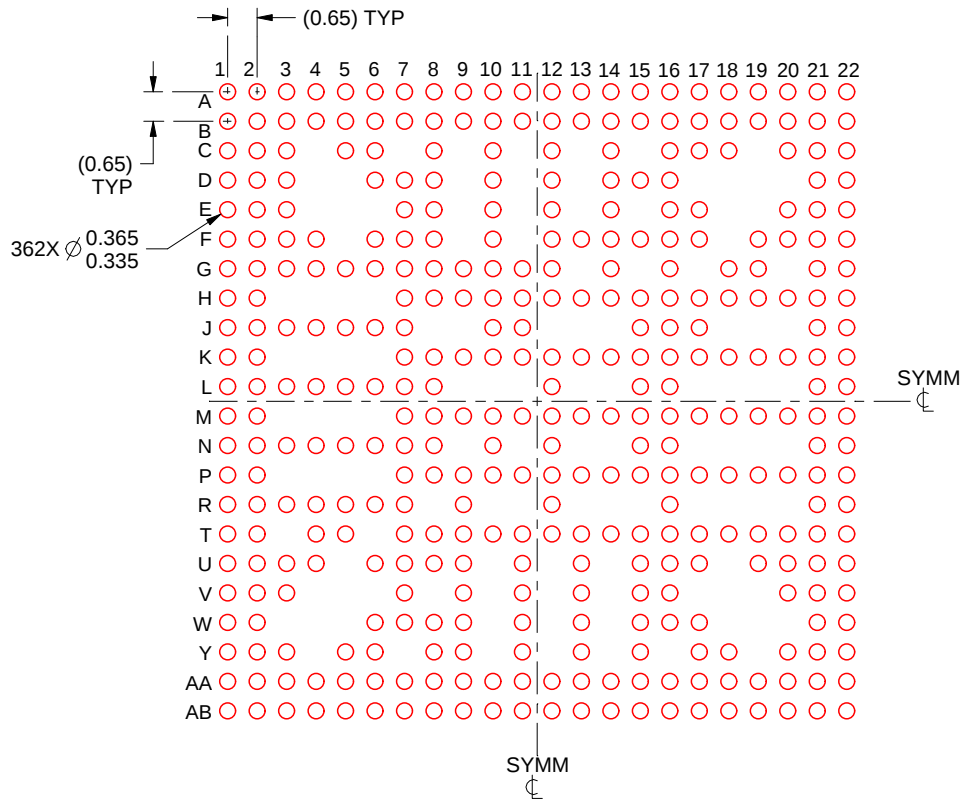
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

ABF0367A

FCBGA - 2.82 mm max height

BALL GRID ARRAY



4221430/C 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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