DLPC900 高度な照明制御向けデジタル・コントローラ

1 特長

- DLP500YX、DLP5500、DLP6500、DLP670S、DLP9000 デジタル マイクロミラー デバイス (DMD) をサポートする、高分解能の産業用およびディスプレイ アプリケーション向けのスケーラブルなコントローラ
- 複数の高速パターン速度をサポート:
  - 最大 16129Hz (DLP500YX、1 ビットの保存済みパターン モード)
  - 最大 2016Hz (DLP500YX、照明変調による 8 ビットの保存済みパターン モード)
  - 最大 1008Hz (DLP500YX、照明変調による 16 ビットの保存済みパターン モード)
- 内蔵 DRAM:128 メガバイト
- 外部フラッシュ機能:128MB の外部フラッシュ機能
- マイクロミラーへの 1 対 1 の入力マッピング
- カメラやセンサと簡単に同期
  - 2 つの構成可能な入力および出力トリガ
- GPIO および PWM 信号を完全にプログラム可能
- 複数の制御インターフェイス
  - 1 つの USB 1.1 ターゲット ポートと 3 つの I^2C ポート
  - LED イネーブルおよび PWM ジェネレータ
- ビデオ モード
  - 最高 120Hz の デュアル 24 ビット RGB 入力
  - YUV、YCrCb、RGB データ形式
  - XGA から WQXGA までの標準ビデオ
  - DLP9000 (WQXGA)、DLP500YX (2048 × 1200)、DLP670S (2716 × 1600) には 2 つの DLPC900 コントローラが必要

2 アプリケーション

- 3D マシン ビジョンおよび光学検査
- 3D プリントおよび積層造形
- 眼科用
- 四肢および皮膚測定用の 3D スキャナ
- インテリジェントおよび適応型照明
- 3D 画像処理顕微鏡

3 概要

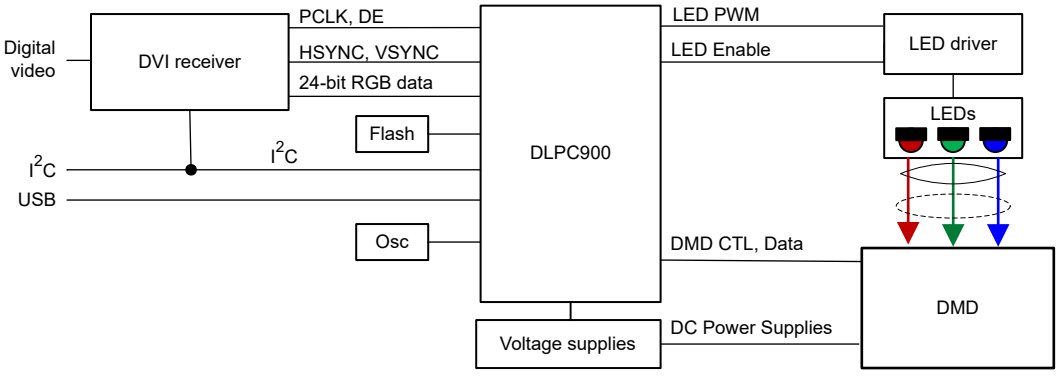
DLP® DLPC900 は、スケーラブルなデジタル マイクロミラー デバイス (DMD) コントローラであり、DLP500YX、DLP5500、DLP6500、DLP670S、および DLP9000 の DMD の高信頼性動作をサポートします。この高性能 DMD コントローラにより、特に産業用アプリケーションでの高度な光制御において、プログラム可能な高いパターン速度を実現できます。DLPC900 のパターン速度によって、高速で正確な 3D スキャンや 3D プリンティングが可能になり、高解像度でインテリジェントなイメージング アプリケーションにも対応できます。DLPC900 は 128 メガバイトの DRAM を内蔵しており、DMD に応じて 400 ～ 1024 個の 1 ビット パターンを使いやすくバッファリングできます。入力および出力トリガにより、各種のカメラ、センサ、他のペリフェラルと簡単に接続および同期できます。

開発を始める方法については、TI DLP® 光制御テクノロジーのページをご覧ください。DLP® の高度な光制御リソースには、評価基板、リファレンス デザイン、光学モジュール メーカー、DLP® デザイン ネットワーク パートナーなどが含まれています。

製品情報

部品番号	パッケージ(1)	パッケージ サイズ
DLPC900	BGA (516)	27.00mm × 27.00mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。



アプリケーション概略図

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Pin Configuration and Functions ... 3
5 Specifications ... 19
5.1 Absolute Maximum Ratings ... 19
5.2 ESD Ratings ... 20
5.3 Recommended Operating Conditions ... 20
5.4 Thermal Information ... 21
5.5 Electrical Characteristics ... 21
5.6 System Oscillators Timing Requirements (1) ... 24
5.7 Power-Up and Power-Down Timing Requirements ... 25
5.8 JTAG Interface: I/O Boundary Scan Application Timing Requirements ... 28
5.9 JTAG Interface: I/O Boundary Scan Application Switching Characteristics ... 28
5.10 Programmable Output Clocks Switching Characteristics ... 29
5.11 Port 1 and 2 Input Pixel Interface Timing Requirements ... 29
5.12 Two Pixels Per Clock (48-Bit Bus) Timing Requirements ... 30
5.13 Synchronous Serial Port (SSP) Switching Characteristics ... 31
5.14 DMD Interface Switching Characteristics ... 33
5.15 DMD LVDS Interface Switching Characteristics ... 34
5.16 Source Input Blanking Requirements ... 35
6 Detailed Description ... 36
6.1 Overview ... 36
6.2 Functional Block Diagram ... 36
6.3 Feature Description ... 37
6.4 Device Functional Modes ... 47
7 Application and Implementation ... 50
7.1 Application Information ... 50
7.2 Typical Applications ... 50
8 Power Supply Recommendations ... 59
8.1 System Power Regulation ... 59
8.2 System Environment and Defaults ... 60
8.3 System Power-Up Sequence ... 60
8.4 System Reset Operation ... 62
9 Layout ... 63
9.1 Layout Guidelines ... 63
9.2 Layout Example ... 74
9.3 Thermal Considerations ... 75
10 Device and Documentation Support ... 77
10.1 Device Support ... 77
10.2 Documentation Support ... 78
10.3 ドキュメントの更新通知を受け取る方法 ... 79
10.4 サポート・リソース ... 79
10.5 Trademarks ... 79
10.6 静電気放電に関する注意事項 ... 79
10.7 用語集 ... 79
11 Revision History ... 80
12 Mechanical, Packaging, and Orderable Information ... 81

4 Pin Configuration and Functions

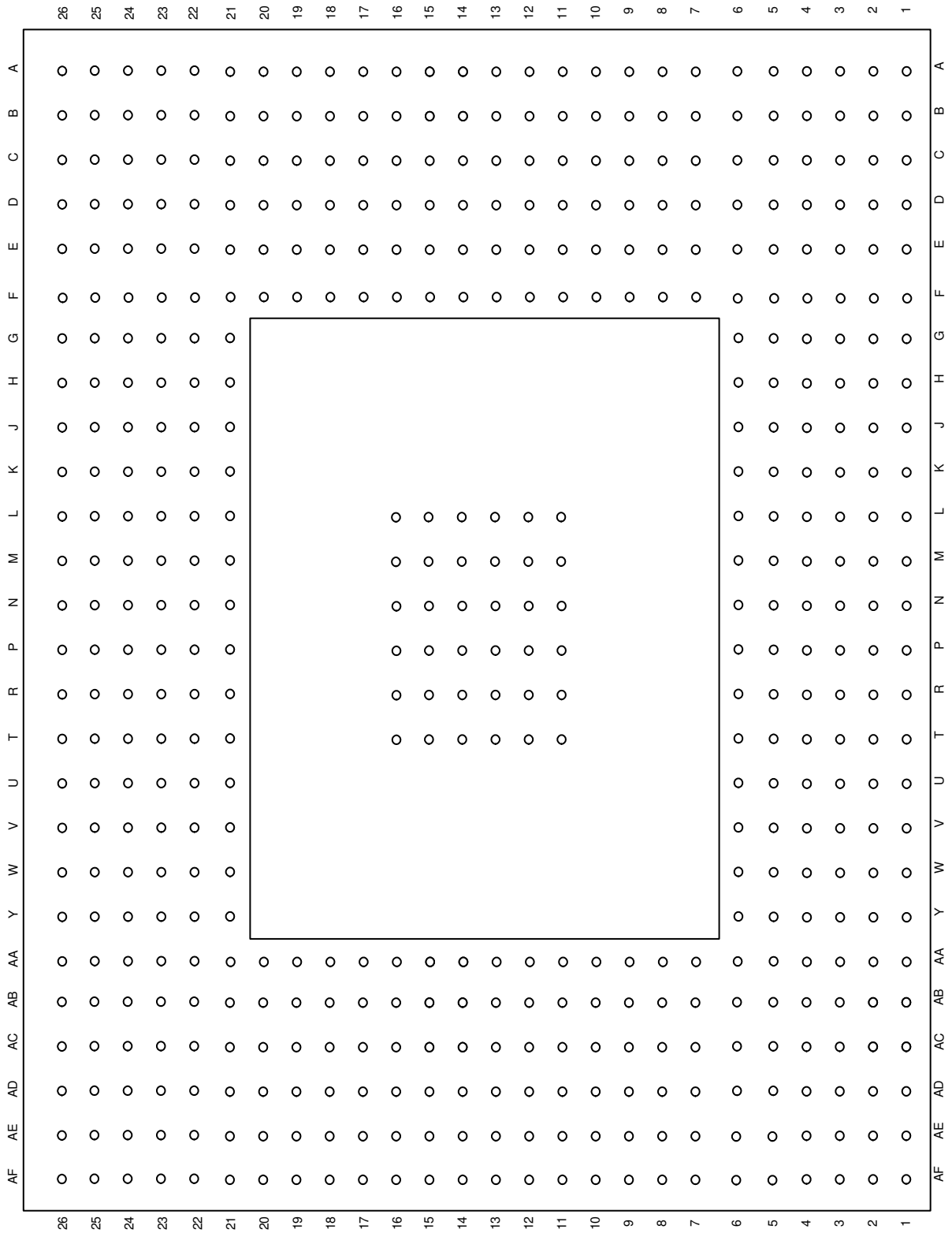


図 4-1. ZPC Package 516-Pin BGA Bottom View

表 4-1. Initialization Pin Functions

PIN		I/O POWER	I/O TYPE(1)	CLK SYSTEM	DESCRIPTION(2)
NAME	NUMBER				
POSENSE	P22	VDD33	I_4 H	Async	Power-on sense is an active high signal with hysteresis, generated from an external voltage monitor circuit. This signal is driven active high when all the controller supply voltages have reached 90% of their specified minimum voltage. This signal is driven inactive low after the falling edge of PWRGOOD as shown in 図 5-4 and 図 5-5. Refer to セクション 5.7 for more details.
PWRGOOD	T26	VDD33	I_4 H	Async	Power Good is an active high signal with hysteresis that is provided from an external voltage monitor circuit. A high value indicates all power is within operating voltage specifications and the system is safe to exit its RESET state. Refer to セクション 5.7 for more details.
EXT_ARSTZ	T24	VDD33	O_2	Async	General purpose active low reset output signal. This output is driven low immediately after POSENSE is externally driven low, placing the system in RESET and remains low while POSENSE remains low. EXT_ARSTZ will continue to be held low after POSENSE is driven high and released by the controller firmware. EXT_ARSTZ is also driven low approximately 5µs after the detection of a PWRGOOD or any internally generated reset. In all cases, it will remain active for a minimum of 2ms.
CTRL_ARSTZ	T25	VDD33	O_2	Async	Controller active low reset output signal. This output is driven low immediately after POSENSE is externally driven low and remains low while POSENSE remains low. CTRL_ARSTZ will continue to be held low after POSENSE is driven high and released by the controller firmware. CTRL_ARSTZ is also optionally asserted low approximately 5µs after the detection of a PWRGOOD or any internally generated reset. In all cases it will remain active for a minimum of 2ms.
AFE_ARSTZ	AC12	VDD33	O_2	Async	Analog Front End active low reset output signal. This output is driven low immediately upon asserting power-up reset (POSENSE) low and remains low while POSENSE remains low. AFE_ARSTZ continues to be held low after the release of power-up reset (that is, POSENSE set high) until released by software. AFE_ARSTZ is also asserted low approximately 5µs after the detection of a PWRGOOD or any internally generated reset. In all cases, it remains active for a minimum of 2ms after the reset condition is released by software. Note that the ASIC contains a software register that can be used to independently drive this output. This pin requires an external 4.7kΩ pullup resistor.
AFE_IRQ	AB13	VDD33	I_4	Async	Analog Front End interrupt active high signal. This signal includes an internal pulldown and uses hysteresis.

(1) Refer to I/O Type and Subscript Definition (表 4-15).
(2) Refer to the セクション 7.2.2 and the セクション 7.2.1 for a description between a one controller and a two controller configuration.

表 4-2. DMD Control Pin Functions

PIN		I/O POWER	I/O TYPE(1)	CLK SYSTEM	DESCRIPTION(2)
NAME	NUMBER				
DADOEZ	AE7	VDD33	O_5	Async	DMD output-enable (active low). This signal does not apply to the secondary controller in a two-controller system configuration. On the secondary controller, this pin is reserved and must be left unconnected.
DADADDR_3 DADADDR_2 DADADDR_1 DADADDR_0	AD6 AE5 AF4 AB8	VDD33	O_5	Async	DMD address. This signal does not apply to the secondary controller in a two-controller system configuration. On the secondary controller, this pin is reserved and must be left unconnected.

表 4-2. DMD Control Pin Functions (続き)

PIN		I/O POWER	I/O TYPE[1]	CLK SYSTEM	DESCRIPTION[2]
NAME	NUMBER				
DADMODE_1 DADMODE_0	AD7 AE6	VDD33	O_5	Async	DMD mode. This signal does not apply to the secondary controller in a two-controller system configuration. On the secondary controller, this pin is reserved and must be left unconnected.
DADSEL_1 DADSEL_0	AE4 AC7	VDD33	O_5	Async	DMD select. This signal does not apply to the secondary controller in a two-controller system configuration. On the secondary controller, this pin is reserved and must be left unconnected.
DADSTRB	AF5	VDD33	O_5	Async	DMD strobe. This signal does not apply to the secondary controller in a two-controller system configuration. On the secondary controller, this pin is reserved and must be left unconnected.
DAD_INTZ	AC8	VDD33	I_4 H	Async	DMD interrupt (active low). Requires an external 1kΩ pullup resistor

(1) Refer to I/O Type and Subscript Definition (表 4-15).
(2) Refer to the セクション 7.2.2 and the セクション 7.2.1 for a description between a one controller and a two controller configuration.

表 4-3. DMD LVDS Interface Pin Functions

PIN[3] [4]		I/O POWER	I/O TYPE[1]	CLK SYSTEM	DESCRIPTION[2]
NAME	NUMBER				
DCKA_P DCKA_N	V4 V3	VDD18	O_7	DCKA_P DCKA_N	DMD, LVDS interface channel A, differential clock
SCA_P SCA_N	V2 V1	VDD18	O_7	DCKA_P DCKA_N	DMD, LVDS interface channel A, differential serial control
DDA_P_15 DDA_N_15 DDA_P_14 DDA_N_14 DDA_P_13 DDA_N_13 DDA_P_12 DDA_N_12 DDA_P_11 DDA_N_11 DDA_P_10 DDA_N_10 DDA_P_9 DDA_N_9 DDA_P_8 DDA_N_8	P4 P3 P2 P1 R4 R3 R2 R1 T4 T3 T2 T1 U4 U3 U2 U1	VDD18	O_7	DCKA_P DCKA_N	DMD, LVDS interface channel A, differential serial data
DDA_P_7 DDA_N_7 DDA_P_6 DDA_N_6 DDA_P_5 DDA_N_5 DDA_P_4 DDA_N_4 DDA_P_3 DDA_N_3 DDA_P_2 DDA_N_2 DDA_P_1 DDA_N_1 DDA_P_0 DDA_N_0	W4 W3 W2 W1 Y2 Y1 Y4 Y3 AA2 AA1 AA4 AA3 AB2 AB1 AC2 AC1				
DCKB_P DCKB_N	J3 J4	VDD18	O_7	DCKB_P DCKB_N	DMD, LVDS interface channel B, differential clock

表 4-3. DMD LVDS Interface Pin Functions (続き)

PIN[3] [4]		I/O POWER	I/O TYPE[1]	CLK SYSTEM	DESCRIPTION[2]
NAME	NUMBER				
SCB_P SCB_N	J1 J2	VDD18	O_7	DCKB_P DCKB_N	DMD, LVDS interface channel B, differential serial control
DDB_P_15 DDB_N_15 DDB_P_14 DDB_N_14 DDB_P_13 DDB_N_13 DDB_P_12 DDB_N_12 DDB_P_11 DDB_N_11 DDB_P_10 DDB_N_10 DDB_P_9 DDB_N_9 DDB_P_8 DDB_N_8	N1 N2 N3 N4 M2 M1 M3 M4 L1 L2 L3 L4 K1 K2 K3 K4	VDD18	O_7	DCKB_P DCKB_N	DMD, LVDS interface channel B, differential serial data
DDB_P_7 DDB_N_7 DDB_P_6 DDB_N_6 DDB_P_5 DDB_N_5 DDB_P_4 DDB_N_4 DDB_P_3 DDB_N_3 DDB_P_2 DDB_N_2 DDB_P_1 DDB_N_1 DDB_P_0 DDB_N_0	H1 H2 H3 H4 G1 G2 G3 G4 F1 F2 F3 F4 E1 E2 D1 D2				

(1) Refer to I/O Type and Subscript Definition (表 4-15).
(2) Refer to the セクション 7.2.2 and the セクション 7.2.1 for a description between a one controller and a two controller configuration.
(3) Several options allow reconfiguration of the DMD interface in order to better optimize board layout. The DLPC900 can swap channel A with channel B. The DLPC900 can also swap the data bit order within each channel independent of swapping the A and B channels.
(4) The DLPC900 is a full-bus DMD signaling interface. 図 6-4 shows the controller connections for this configuration.

表 4-4. Program Memory Flash Interface Pin Functions

PIN[3]		I/O POWER	I/O TYPE[1]	CLK SYSTEM	DESCRIPTION		
NAME	NUMBER				CHIP SELECT 0 (ADDITIONAL FLASH)	CHIP SELECT 1 (BOOT FLASH ONLY) [2] [3]	CHIP SELECT 2 (ADDITIONAL FLASH)
PM_CSZ_0 [4]	D13	VDD33	O_5	Async	Chip select (active low)	N/A	N/A
PM_CSZ_1 [4]	E12	VDD33	O_5	Async	N/A	Boot flash chip select (active low)	N/A
PM_CSZ_2 [4]	A13	VDD33	O_5	Async	N/A	N/A	Chip select (active low)
PM_ADDR_22 [5]	A12	VDD33	B_5	Async	Address bit (MSB)	Address bit (MSB)	Address bit (MSB)
PM_ADDR_21 [5]	E11	VDD33	B_5	Async	Address bit	Address bit	Address bit
PM_ADDR_20	D12	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_19	C12	VDD33	O_5	Async	Address bit	Address bit	Address bit

表 4-4. Program Memory Flash Interface Pin Functions (続き)

PIN[3]		I/O POWER	I/O TYPE[1]	CLK SYSTEM	DESCRIPTION		
NAME	NUMBER				CHIP SELECT 0 (ADDITIONAL FLASH)	CHIP SELECT 1 (BOOT FLASH ONLY) [2] [3]	CHIP SELECT 2 (ADDITIONAL FLASH)
PM_ADDR_18	B11	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_17	A11	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_16	D11	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_15	C11	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_14	E10	VDD33	O5	Async	Address bit	Address bit	Address bit
PM_ADDR_13	D10	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_12	C10	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_11	B9	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_10	A9	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_9	E9	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_8	D9	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_7	C9	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_6	B8	VDD33	O5	Async	Address bit	Address bit	Address bit
PM_ADDR_5	A8	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_4	D8	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_3	C8	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_2	B7	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_1	A7	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_0	C7	VDD33	O_5	Async	Address bit (LSB)	Address bit (LSB)	Address bit (LSB)
PM_WEZ	B12	VDD33	O_5	Async	Write-enable (active low)	Write-enable (active low)	Write-enable (active low)
PM_OEZ	C13	VDD33	O_5	Async	Output-enable (active low)	Output-enable (active low)	Output-enable (active low)
PM_BLSZ_1	B6	VDD33	O_5	Async	UpperByte(15:8) enable (active low)	N/A	UpperByte(15:8) Enable (active low)
PM_BLSZ_0	A6	VDD33	O_5	Async	LowerByte(7:0) enable (active low)	N/A	LowerByte(7:0) Enable (active low)
PM_DATA_15	C17	VDD33	B_5	Async	Data bit (15)	Data bit (15)	Data bit (15)
PM_DATA_14	B16	VDD33	B_5	Async	Data bit (14)	Data bit (14)	Data bit (14)
PM_DATA_13	A16	VDD33	B_5	Async	Data bit (13)	Data bit (13)	Data bit (13)
PM_DATA_12	A15	VDD33	B_5	Async	Data bit (12)	Data bit (12)	Data bit (12)
PM_DATA_11	B15	VDD33	B_5	Async	Data bit (11)	Data bit (11)	Data bit (11)
PM_DATA_10	D16	VDD33	B_5	Async	Data bit (10)	Data bit (10)	Data bit (10)
PM_DATA_9	C16	VDD33	B_5	Async	Data bit (9)	Data bit (9)	Data bit (9)
PM_DATA_8	E14	VDD33	B_5	Async	Data bit (8)	Data bit (8)	Data bit (8)
PM_DATA_7	D15	VDD33	B_5	Async	Data bit (7)	Data bit (7)	Data bit (7)
PM_DATA_6	C15	VDD33	B_5	Async	Data bit (6)	Data bit (6)	Data bit (6)
PM_DATA_5	B14	VDD33	B_5	Async	Data bit (5)	Data bit (5)	Data bit (5)
PM_DATA_4	A14	VDD33	B_5	Async	Data bit (4)	Data bit (4)	Data bit (4)
PM_DATA_3	E13	VDD33	B_5	Async	Data bit (3)	Data bit (3)	Data bit (3)
PM_DATA_2	D14	VDD33	B_5	Async	Data bit (2)	Data bit (2)	Data bit (2)
PM_DATA_1	C14	VDD33	B_5	Async	Data bit (1)	Data bit (1)	Data bit (1)

表 4-4. Program Memory Flash Interface Pin Functions (続き)

PIN(3)		I/O POWER	I/O TYPE(1)	CLK SYSTEM	DESCRIPTION		
NAME	NUMBER				CHIP SELECT 0 (ADDITIONAL FLASH)	CHIP SELECT 1 (BOOT FLASH ONLY) (2) (3)	CHIP SELECT 2 (ADDITIONAL FLASH)
PM_DATA_0	B13	VDD33	B_5	Async	Data bit (0)	Data bit (0)	Data bit (0)

(1) Refer to I/O Type and Subscript Definition (表 4-15).
(2) The default wait-state is set for a flash device of 120ns access time. Therefore, the slowest flash access time supported is 120ns. Refer to the セクション 7.2.1.2.1.4.2 on how to program new wait-state values.
(3) Refer to the 図 7-2 for the memory layout of the boot flash.
(4) Requires an external 10kΩ pullup resistor
(5) Requires an external 10kΩ pulldown resistor

表 4-5. Port 1 and Port 2 Channel Data and Control Pin Functions

PIN (3) (4) (5)		I/O POWER	I/O TYPE(1)	CLK SYSTEM	DESCRIPTION(2)
NAME	NUMBER				
P_CLK1	AE22	VDD33	I_4 D	N/A	Input port data pixel write clock (selectable as rising or falling edge triggered, and with which port it is associated [Port 1 or Port 2 or [Port 1 and Port 2]]).
P_CLK2	W25	VDD33	I_4 D	N/A	Input port data pixel write clock (selectable as rising or falling edge triggered, and with which port it is associated [Port 1 or Port 2 or [Port 1 and Port 2]]).
P_CLK3	AF23	VDD33	I_4 D	N/A	Input port data pixel write clock (selectable as rising or falling edge triggered, and with which port it is associated [Port 1 or Port 2 or [Port 1 and Port 2]]).
P_DATAEN1	AF22	VDD33	I_4 D	P_CLK1, P_CLK2, or P_CLK3	Active high data enable. Selectable as to which port it is associated with (Port 1 or Port 2 or [Port 1 and Port 2]).
P_DATAEN2	W24	VDD33	I_4 D	P_CLK1, P_CLK2, or P_CLK3	Active high data enable. Selectable as to which port it is associated with (Port 1 or Port 2 or [Port 1 and Port 2]).
P1_A9 P1_A8 P1_A7 P1_A6 P1_A5 P1_A4 P1_A3 P1_A2 P1_A1 (3) P1_A0 (3)	AD15 AE15 AE14 AE13 AD13 AC13 AF14 AF13 AF12 AE12	VDD33	I_4 D	P_CLK1, P_CLK2, or P_CLK3	Port 1 A channel input pixel data (bit weight 128) Port 1 A channel input pixel data (bit weight 64) Port 1 A channel input pixel data (bit weight 32) Port 1 A channel input pixel data (bit weight 16) Port 1 A channel input pixel data (bit weight 8) Port 1 A channel input pixel data (bit weight 4) Port 1 A channel input pixel data (bit weight 2) Port 1 A channel input pixel data (bit weight 1) Unused, tie to 0 Unused, tie to 0.
P1_B9 P1_B8 P1_B7 P1_B6 P1_B5 P1_B4 P1_B3 P1_B2 P1_B1 (3) P1_B0 (3)	AF18 AB18 AC15 AC16 AD16 AE16 AF16 AF15 AC14 AD14	VDD33	I_4 D	P_CLK1, P_CLK2, or P_CLK3	Port 1 B channel input pixel data (bit weight 128) Port 1 B channel input pixel data (bit weight 64) Port 1 B channel input pixel data (bit weight 32) Port 1 B channel input pixel data (bit weight 16) Port 1 B channel input pixel data (bit weight 8) Port 1 B channel input pixel data (bit weight 4) Port 1 B channel input pixel data (bit weight 2) Port 1 B channel input pixel data (bit weight 1) Unused, tie to 0 Unused, tie to 0.

表 4-5. Port 1 and Port 2 Channel Data and Control Pin Functions (続き)

PIN (3) (4) (5)		I/O POWER	I/O TYPE(1)	CLK SYSTEM	DESCRIPTION(2)
NAME	NUMBER				
P1_C9 P1_C8 P1_C7 P1_C6 P1_C5 P1_C4 P1_C3 P1_C2 P1_C1 (3) P1_C0 (3)	AD20 AE20 AE21 AF21 AD19 AE19 AF19 AF20 AC19 AE18	VDD33	I_4 D	P_CLK1, P_CLK2, or P_CLK3	Port 1 C channel input pixel data (bit weight 128) Port 1 C channel input pixel data (bit weight 64) Port 1 C channel input pixel data (bit weight 32) Port 1 C channel input pixel data (bit weight 16) Port 1 C channel input pixel data (bit weight 8) Port 1 C channel input pixel data (bit weight 4) Port 1 C channel input pixel data (bit weight 2) Port 1 C channel input pixel data (bit weight 1) Unused, tie to 0 Unused, tie to 0.
P1_VSYNC	AC20	VDD33	B_2 D	P_CLK1, P_CLK2, or P_CLK3	Port 1 vertical sync. While intended to be associated with port 1, it can be programmed for use with port 2.
P1_HSYNC	AD21	VDD33	B_2 D	P_CLK1, P_CLK2, or P_CLK3	Port 1 horizontal sync. While intended to be associated with port 1, it can be programmed for use with port 2.
P2_A9 P2_A8 P2_A7 P2_A6 P2_A5 P2_A4 P2_A3 P2_A2 P2_A1 (3) P2_A0 (3)	AD26 AD25 AB21 AC22 AD23 AB20 AC21 AD22 AE23 AB19	VDD33	I_4 D	P_CLK1, P_CLK2, or P_CLK3	Port 2 A channel input pixel data (bit weight 128) Port 2 A channel input pixel data (bit weight 64) Port 2 A channel input pixel data (bit weight 32) Port 2 A channel input pixel data (bit weight 16) Port 2 A channel input pixel data (bit weight 8) Port 2 A channel input pixel data (bit weight 4) Port 2 A channel input pixel data (bit weight 2) Port 2 A channel input pixel data (bit weight 1) Unused, tie to 0 Unused, tie to 0.
P2_B9 P2_B8 P2_B7 P2_B6 P2_B5 P2_B4 P2_B3 P2_B2 P2_B1 (3) P2_B0 (3)	Y22 AB26 AA23 AB25 AA22 AB24 AC26 AB23 AC25 AC24	VDD33	I_4 D	P_CLK1, P_CLK2, or P_CLK3	Port 2 B channel input pixel data (bit weight 128) Port 2 B channel input pixel data (bit weight 64) Port 2 B channel input pixel data (bit weight 32) Port 2 B channel input pixel data (bit weight 16) Port 2 B channel input pixel data (bit weight 8) Port 2 B channel input pixel data (bit weight 4) Port 2 B channel input pixel data (bit weight 2) Port 2 B channel input pixel data (bit weight 1) Unused, tie to 0 Unused, tie to 0.
P2_C9 P2_C8 P2_C7 P2_C6 P2_C5 P2_C4 P2_C3 P2_C2 P2_C1 (3) P2_C0 (3)	W23 V22 Y26 Y25 Y24 Y23 W22 AA26 AA25 AA24	VDD33	I_4 D	P_CLK1, P_CLK2, or P_CLK3	Port 2 C channel input pixel data (bit weight 128) Port 2 C channel input pixel data (bit weight 64) Port 2 C channel input pixel data (bit weight 32) Port 2 C channel input pixel data (bit weight 16) Port 2 C channel input pixel data (bit weight 8) Port 2 C channel input pixel data (bit weight 4) Port 2 C channel input pixel data (bit weight 2) Port 2 C channel input pixel data (bit weight 1) Unused, tie to 0 Unused, tie to 0.
P2_VSYNC	U22	VDD33	B_2 D	P_CLK1, P_CLK2, or P_CLK3	Port 2 vertical sync. While intended to be associated with port 2, it can be programmed for use with port 1.
P2_HSYNC	W26	VDD33	B_2 D	P_CLK1, P_CLK2, or P_CLK3	Port 2 horizontal sync. While intended to be associated with port 2, it can be programmed for use with port 1.
RESERVED_H23	H23	VDD33	B_2	N/A	Connects to BUS_SELECT signal on Primary Controller, must be left unconnected for Secondary Controller
RESERVED_G23	G23	VDD33	B_2	N/A	Connects to HDMI_CEC signal on Primary Controller, must be left unconnected for Secondary Controller

(1) Refer to I/O Type and Subscript Definition (表 4-15).
(2) Refer to the セクション 7.2.2 and the セクション 7.2.1 for a description between a one controller and a two controller configuration.

(3) Port 1 and Port 2 are capable of 24 bits each. A maximum of 8-bits is available in each of the A, B, and C channels. The 8-bit color inputs are connected to bits [9:2] of the corresponding A, B, C input channels. Sources feeding 8 bits or less per color component channel are MSB justified when connected to the DLPC900, and the LSBs tied to ground along with the data lines 0 and 1 from every channel. Three port clocks options (1, 2, and 3) are provided to improve the signal integrity.
(4) Ports 1 and 2 can be used separately as two 24-bit ports, or can be combined into one 48-bit port (typically, for high data rate sources) for transmission of two pixels per clock.
(5) The A, B, C input data channels of ports 1 and 2 can be internally reconfigured or remapped for optimum board layout. Specifically, each channel can individually remapped to the internal GBR channels. For example, G data can be connected to channel A, B, or C and remapped to be appropriate channel internally. Port configuration and channel multiplexing is handled in the API software.

表 4-6. Clock and PLL Support Pin Functions

PIN		I/O POWER	I/O TYPE(1)	CLK SYSTEM	DESCRIPTION(2)
NAME	NUMBER				
MOSC	M26	VDD33	I_{10}	N/A	System clock oscillator input (3.3V LVTTL). MOSC must be stable a maximum of 25ms after POSENSE transitions from low to high.
MOSCN	N26	VDD33	O_{10}	N/A	MOSC crystal return
OCLKA (3)	AF6	VDD33	O_5	Async	General-purpose output clock A. The frequency is software programmable. Power-up default is 787kHz and the output frequency is maintained through all operations, except power loss and reset.

(1) Refer to I/O Type and Subscript Definition (表 4-15).
(2) Refer to the セクション 7.2.2 and the セクション 7.2.1 for a description between a one controller and a two controller configuration.
(3) This signal does not apply to the secondary controller in a two controller system configuration. On the secondary controller, this pin is reserved and Must be left unconnected Refer to the セクション 7.2.2 and the セクション 7.2.1 for a description between a one controller and a two controller configuration.

表 4-7. Board-Level Test and Debug Pin Functions

PIN (3)		I/O POWER	I/O TYPE(1)	CLK SYSTEM	DESCRIPTION(2)
NAME	NUMBER				
TDI	N25	VDD33	I_4 U	TCK	JTAG serial data in. Used in both Boundary Scan and ICE modes
TCK	N24	VDD33	I_4 D	N/A	JTAG serial data clock. Used in both Boundary Scan and ICE modes
TMS1	P25	VDD33	I_4 U	TCK	JTAG test mode select. Used in Boundary Scan mode
TMS2	P26	VDD33	I_4 U	TCK	JTAG-ICE test mode select. Used in ICE mode
TDO1	N23	VDD33	O_5	TCK	JTAG serial data out. Used in Boundary Scan mode
TDO2	N22	VDD33	O_5	TCK	JTAG-ICE serial data out. Used in ICE mode
TRSTZ	M23	VDD33	I_4 H U	Async	JTAG Reset. Used in both Boundary Scan and ICE modes. This pin is pulled high (or left unconnected) when the JTAG interface is in use for boundary scan or debug. Connect this to ground otherwise. Failure to tie this pin low during standard operation causes startup and initialization problems.
RTCK	E4	VDD33	O_2	N/A	JTAG return clock. Used in ICE mode.
ICTSEN	M24	VDD33	I_4 H D	Async	IC tri-state enable (active high). Asserting high will tri-state all outputs except the JTAG interface. Requires an external 4.7kΩ pulldown resistor
RESERVED_E8	E8	VDD33	B_2 D	N/A	Connects to signal TSTPT7
RESERVED_B4	B4	VDD33	B_2 D	N/A	Connects to signal TSTPT6
RESERVED_C4	C4	VDD33	B_2 D	N/A	Connects to signal TSTPT5
RESERVED_E7	E7	VDD33	B_2 D	N/A	Connects to signal TSTPT4

表 4-7. Board-Level Test and Debug Pin Functions (続き)

PIN [3]		I/O POWER	I/O TYPE[1]	CLK SYSTEM	DESCRIPTION[2]
NAME	NUMBER				
RESERVED_D5	D5	VDD33	B_2 D	N/A	Connects to signal TSTPT3
RESERVED_E6	E6	VDD33	B_2 D	N/A	Connects to signal TSTPT2
RESERVED_D3	D3	VDD33	B_2 D	N/A	Connects to signal TSTPT1
RESERVED_C2	C2	VDD33	B_2 D	N/A	Connects to signal TSTPT0
RESERVED_A4	A4	VDD33	B_2 D	N/A	Connects to signal PIPESTAT2
RESERVED_B5	B5	VDD33	B_2 D	N/A	Connects to signal PIPESTAT1
RESERVED_C6	C6	VDD33	B_2 D	N/A	Connects to signal PIPESTAT0
RESERVED_A5	A5	VDD33	B_2 D	N/A	Connects to signal TRACESYNC
RESERVED_D7	D7	VDD33	B_2 D	N/A	Connects to signal TRACECLK

(1) Refer to I/O Type and Subscript Definition (表 4-15).
(2) Refer to the セクション 7.2.2 and the セクション 7.2.1 for a description between a one controller and a two controller configuration.
(3) All JTAG signals are LVTTL compatible.

表 4-8. Device Test Pin Functions

PIN		I/O POWER	I/O TYPE[1]	CLK SYSTEM	DESCRIPTION[2]
NAME	NUMBER				
HW_TEST_EN	M25	VDD33	I_4 H D	N/A	Device manufacturing test enable. This signal must be connected to an external ground for standard operation.

(1) Refer to I/O Type and Subscript Definition (表 4-15).
(2) Refer to the セクション 7.2.2 and the セクション 7.2.1 for a description between a one controller and a two controller configuration.

表 4-9. Peripheral Interface Pin Functions

PIN		I/O POWER	I/O TYPE[1]	CLK SYSTEM	DESCRIPTION[2]
NAME	NUMBER				
I2C0_SCL	A10	VDD33	B_8	N/A	I^2C bus 0, clock. This bus supports 400kHz, fast mode operation. This input is not 5V tolerant. This pin requires an external pullup resistor to 3.3V. The minimum acceptable pullup value is 1kΩ resistor.
I2C0_SDA	B10	VDD33	B_8	I2C0_SCL	I^2C bus 0, data. This bus supports 400kHz, fast mode operation. This input is not 5-V tolerant. This pin requires an external pullup resistor to 3.3V. The minimum acceptable pullup value is 1kΩ resistor.
I2C1_SDA [3]	E19	VDD33	B_2	I2C1_SCL	I^2C bus 1, data. This bus supports 400kHz, fast mode operation. This input is not 5V tolerant. This pin requires an external pullup resistor to 3.3V. The minimum acceptable pullup value is 1kΩ resistor.
I2C1_SCL [3]	D20	VDD33	B_2	N/A	I^2C bus 1, clock. This bus supports 400kHz, fast mode operation. This input is not 5V tolerant. This pin requires an external pullup resistor to 3.3V. The minimum acceptable pullup value is 1kΩ resistor.

表 4-9. Peripheral Interface Pin Functions (続き)

PIN		I/O POWER	I/O TYPE[1]	CLK SYSTEM	DESCRIPTION[2]
NAME	NUMBER				
I2C2_SDA [3]	C21	VDD33	B_2	I2C2_SCL	I^2C bus 2, data. This bus supports 400kHz, fast mode operation. This input is not 5V tolerant. This pin requires an external pullup resistor to 3.3V. The minimum acceptable pullup value is 1kΩ resistor.
I2C2_SCL [3]	B22	VDD33	B_2	N/A	I^2C bus 2, clock. This bus supports 400kHz, fast mode operation. This input is not 5-V tolerant. This pin requires an external pullup resistor to 3.3V. The minimum acceptable pullup value is 1kΩ resistor.
RESERVED_AE8	AE8	VDD33	I_4	N/A	PMD Interrupt. This pin requires an external 10kΩ pullup resistor.
RESERVED_AD8	AD8	VDD33	O_5	N/A	Color wheel control PWM output
SSP0_CLK	AD4	VDD33	B_5	N/A	Synchronous serial port 0, clock
SSP0_RXD	AD5	VDD33	I_4	SSP0_CLK	Synchronous serial port 0, receive data in
SSP0_TXD	AB7	VDD33	O_5	SSP0_CLK	Synchronous serial port 0, transmit data out
SSP0_CSZ_0 [3]	AC5	VDD33	B_5	SSP0_CLK	Synchronous serial port 0, chip select 0 (active low)
SSP0_CSZ_1 [3]	AB6	VDD33	B_5	SSP0_CLK	Synchronous serial port 0, chip select 1 (active low) This signal connects to the DMD SCP_ENZ input
SSP0_CSZ_2 [3]	AC3	VDD33	B_5	SSP0_CLK	Synchronous serial port 0, chip select 2 (active low)
UART0_TXD	AB3	VDD33	O_5	Async	UART0, UART transmit data output. The firmware only outputs debug messages on this port.
UART0_RXD	AD1	VDD33	I_4	Async	UART0, UART receive data input. The firmware does not support receiving data on this port.
UART0_RTSZ	AD2	VDD33	O_5	Async	UART0, UART ready to send hardware flow control output (active low)
UART0_CTSZ	AE2	VDD33	I_4	Async	UART0, UART clear to send hardware flow control input (active low). This pin requires an external 10kΩ pulldown resistor.
USB_DAT_N [3] USB_DAT_P	C5 D6	VDD33	B_9	Async	USB D– I/O USB D+ I/O
HOLD_BOOTZ	F24	VDD33	B_2	Async	Boot mode. When this pin is held low, the firmware boots-up in bootload mode. When pin is held high, the firmware boots-up in default operating mode. This pin requires an external 1kΩ pullup resistor.
USB_ENZ [3]	E25	VDD33	B_2	Async	The firmware will use this pin to enable an external buffer on the USB data lines after it has completed initialization.
FAULT_STATUS	AC11	VDD33	O_2	Async	This signal toggles or held high to indicate status faults. This pin requires an external 10kΩ pulldown resistor.
HEARTBEAT	AB12	VDD33	O_2	Async	This signal toggles to indicate the system is operational. Period is approximately 1 second.
RESERVED_AF8	AF8	VDD33	I_4	N/A	Lamp status pin. This pin requires an external 10kΩ pulldown resistor.
SEQ_INT2	H26	VDD33	I_2	Async	This signal serves as an interrupt for pattern sequencing and must be connected to SEQ_AUX6.
SEQ_INT1	G26	VDD33	I_2	Async	This signal serves as an interrupt for pattern sequencing and must be connected to SEQ_AUX7.
SEQ_AUX7	F26	VDD33	O_2	Async	This signal serves as an interrupt for pattern sequencing and must be connected to SEQ_INT1.
SEQ_AUX6	E26	VDD33	O_2	Async	This signal serves as an interrupt for pattern sequencing and must be connected to SEQ_INT2.
TEST_FUNC_5 [3]	K22	VDD33	B_2	Async	In a dual DLPC900 configuration, this pin connects to the FPGA and could serve as a configuration pin. Otherwise, this pin can be left unconnected.

表 4-9. Peripheral Interface Pin Functions (続き)

PIN		I/O POWER	I/O TYPE[1]	CLK SYSTEM	DESCRIPTION[2]
NAME	NUMBER				
TEST_FUNC_4 [3]	J26	VDD33	B_2	Async	In a dual DLPC900 configuration, this pin connects to the FPGA and could serve as a configuration pin. Otherwise, this pin can be left unconnected.
TEST_FUNC_3 [3]	J25	VDD33	B_2	Async	In a dual DLPC900 configuration, this pin connects to the FPGA and serves as a configuration pin. This function configures the 24-bit parallel data output of the FPGA to be split between the primary and the secondary controllers. The firmware sets this pin high by default.
TEST_FUNC_2 [3]	J24	VDD33	B_2	Async	In a dual DLPC900 configuration, this pin connects to the FPGA and could serve as a configuration pin. Otherwise, this pin can be left unconnected.
TEST_FUNC_1 [3]	J23	VDD33	B_2	Async	In a dual DLPC900 configuration, this pin connects to the FPGA and could serve as a configuration pin. Otherwise, this pin can be left unconnected.
GPIO_60	H22	VDD33	B_2	N/A	Used for Flash memory address extension ADDR_26. Pull down to GND with a 10kΩ resistor.
GPIO_46	T22	VDD33	B_2	N/A	Used for Flash memory address extension ADDR_25. Pull down to GND with a 10kΩ resistor.
GPIO_45	U23	VDD33	B_2	N/A	Used for Flash memory address extension ADDR_24. Pull down to GND with a 10kΩ resistor.
GPIO_08 [3]	E21	VDD33	B_2	Async	This pin can be configured as GPIO 8. An external pullup resistor is required when this pin is configured as open-drain. [4]
GPIO_07 [3]	V23	VDD33	B_2	Async	This pin can be configured as GPIO 7. An external pullup resistor is required when this pin is configured as open-drain.[4]
GPIO_06 [3]	V24	VDD33	B_2	Async	This pin can be configured as GPIO 6. An external pullup resistor is required when this pin is configured as open-drain.[4]
GPIO_05 [3]	U24	VDD33	B_2	Async	This pin can be configured as GPIO 5. An external pullup resistor is required when this pin is configured as open-drain.[4]
GPIO_04 [3]	U25	VDD33	B_2	Async	This pin can be configured as GPIO 4. An external pullup resistor is required when this pin is configured as open-drain.[4]
GPIO_PWM_03 [3]	A23	VDD33	B_2	Async	This pin can be configured as GPIO 3 or PWM 3. An external pullup resistor is required when this pin is configured as open-drain. [4]
GPIO_PWM_02 [3]	A22	VDD33	B_2	Async	This pin can be configured as GPIO 2 or PWM 2. An external pullup resistor is required when this pin is configured as open-drain.[4]
GPIO_PWM_01 [3]	B21	VDD33	B_2	Async	This pin can be configured as GPIO 1 or PWM 1. An external pullup resistor is required when this pin is configured as open-drain. [4]
GPIO_PWM_00 [3]	A21	VDD33	B_2	Async	This pin can be configured as GPIO 0 or PWM 0. An external pullup resistor is required when this pin is configured as open-drain.[4]
RESERVED_AF9	AF9	VDD33	B_2	N/A	This pin connects to signal 3DLR_GPIO78.
RESERVED_G24	G24	VDD33	B_2	N/A	This pin connects to signal IIC_BUSY (I2C_BUSY).
RESERVED_F23	F23	VDD33	B_2	N/A	This pin connects to signal SSP1_CSZ_1 of the primary controller in a dual controller configuration. Otherwise, leave unconnected.
RESERVED_D26	D26	VDD33	B_2	N/A	This pin connects to signal SSP1_CSZ_0 of the primary controller in a dual controller configuration. Otherwise, leave unconnected.

表 4-9. Peripheral Interface Pin Functions (続き)

PIN		I/O POWER	I/O TYPE(1)	CLK SYSTEM	DESCRIPTION(2)
NAME	NUMBER				
RESERVED_E24	E24	VDD33	B_2	N/A	This pin connects to signal SSP1_DO of the primary controller in a dual controller configuration. Otherwise, leave unconnected.
RESERVED_F22	F22	VDD33	B_2	N/A	This pin connects to signal SSP1_DIN of the primary controller in a dual controller configuration. Otherwise, leave unconnected.
RESERVED_D25	D25	VDD33	B_2	N/A	This pin connects to signal SSP1_CLK of the primary controller in a dual controller configuration. Otherwise, leave unconnected.

(1) Refer to I/O Type and Subscript Definition (表 4-15).
(2) Refer to the セクション 7.2.2 and the セクション 7.2.1 for a description between a one controller and a two controller configuration.
(3) This signal does not apply to the secondary controller in a two controller system configuration. On the secondary controller, this pin is reserved and must be left unconnected. Refer to セクション 7.2.2 and セクション 7.2.1 for a description between a one controller and a two controller configuration.
(4) GPIO signals must be configured through software for input, output, bidirectional, or open-drain. Some GPIO have one or more alternative use modes, which are also software-configurable. The reset default for all GPIO signals is as an input signal. Refer to the *DLPC900 Programmer's Guide*.

表 4-10. Trigger Control Pin Functions

PIN		I/O POWER	I/O TYPE(1)	CLK SYSTEM	DESCRIPTION(2)
NAME	NUMBER				
TRIG_IN_1(3)	AF7	VDD33	I_4	Async	In video pattern mode, this signal is used for advancing the pattern display.
TRIG_IN_2(3)	H25	VDD33	I_2	Async	In video pattern mode, the rising edge of this signal is used for starting the pattern display and the falling edge is used for stopping the pattern display. It works along with the software start stop command.
TRIG_OUT_1	E20	VDD33	O_2	Async	Active high trigger output signal during pattern exposure
TRIG_OUT_2	D22	VDD33	O_2	Async	Active high trigger output to indicate first pattern display

(1) Refer to I/O Type and Subscript Definition (表 4-15).
(2) Refer to the セクション 7.2.2 and the セクション 7.2.1 for a description between a one controller and a two controller configuration.
(3) These signals do not apply to the secondary controller in a two controller system configuration. On the secondary controller, these pins are reserved and are acceptable to be left unconnected. Refer to the セクション 7.2.2 and the セクション 7.2.1 for a description between a one controller and a two controller configuration.

表 4-11. LED Control Pin Functions

PIN (3)		I/O POWER	I/O TYPE(1)	CLK SYSTEM	DESCRIPTION(2)
NAME	NUMBER				
BLU_LED_PWM	C20	VDD33	O_2	Async	Blue LED PWM current control signal
GRN_LED_PWM	B20	VDD33	O_2	Async	Green LED PWM current control signal
RED_LED_PWM	B19	VDD33	O_2	Async	Red LED PWM current control signal
BLU_LED_EN	D24	VDD33	O_2	Async	Blue LED enable signal
GRN_LED_EN	C25	VDD33	O_2	Async	Green LED enable signal
RED_LED_EN	B26	VDD33	O_2	Async	Red LED enable signal

(1) Refer to I/O Type and Subscript Definition (表 4-15).
(2) Refer to the セクション 7.2.2 and the セクション 7.2.1 for a description between a one controller and a two controller configuration.
(3) These signals do not apply to the secondary controller in a two controller system configuration. On the secondary controller, these pins are reserved and Must be left unconnected Refer to the セクション 7.2.2 and the セクション 7.2.1 for a description between a one controller and a two controller configuration.

表 4-12. Two Controller Support Pin Functions

PIN		I/O POWER	I/O TYPE(1)	CLK SYSTEM	DESCRIPTION(2)
NAME	NUMBER				
SEQ_SYNC	AB9	VDD33	B_3	Async	Sequence sync. This signal must be connected between the primary and secondary controller in a two controller configuration. Do not leave unconnected. This pin requires an external 10kΩ pullup resistor.
SSP0_CSZ4_SLV	U26	VDD33	B_2	SSP0_CLK	This signal is used by the primary controller to communicate with the secondary controller over the SSP interface. This pin requires an external 4.7kΩ pullup resistor.
FSD12_OUTPUT	T23	VDD33	B_2	Async	This pin must be connected to DA_SYNC_INPUT (3).
DA_SYNC_INPUT	R22	VDD33	B_2	Async	This pin must be connected to FSD12_OUTPUT (4).
SLV_CTRL_PRST	V25	VDD33	B_2	Async	This signal must be connected between the primary and secondary controller in a two controller configuration. The secondary controller will pull this signal high to inform the primary controller that it is present and ready. This pin requires an external 10kΩ pulldown resistor. Do not leave unconnected.
CTRL_MODE_CFG	V26	VDD33	B_2	Async	When this pin is high, the controller operates as the primary controller. When this pin is low the controller operates as the secondary controller. Use an external 4.7kΩ pullup or pulldown resistor to identify the controller. Do not leave unconnected.

(1) Refer to I/O Type and Subscript Definition (表 4-15).
(2) Refer to the セクション 7.2.2 and the セクション 7.2.1 for a description between a one controller and a two controller configuration.
(3) The FSD12_OUTPUT of the secondary controller Must be left unconnected
(4) The DA_SYNC_INPUT of the secondary controller must be connected to the FSD12_OUTPUT of the primary controller.

表 4-13. Reserved Pin Functions

PIN		I/O POWER	I/O TYPE(1)	CLK SYSTEM	DESCRIPTION(2)
NAME	NUMBER				
RESERVED_AD12	AD12	VDD33	O_6	N/A	Reserved. Must be left unconnected
RESERVED_AF11	AF11	VDD33	I_4	N/A	Reserved. Must be left unconnected
RESERVED_AD11	AD11	VDD33	I_4	N/A	Reserved. Must be left unconnected
RESERVED_AE11	AE11	VDD33	I_4	N/A	Reserved. Must be left unconnected
RESERVED_AC9	AC9	VDD33	O_5	N/A	Reserved. Must be left unconnected
RESERVED_E3	E3	VDD33	B_5	N/A	Reserved. Must be left unconnected
RESERVED_AB10	AB10	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_AD9	AD9	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_AE9	AE9	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_AB11	AB11	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_AC10	AC10	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_AD10	AD10	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_AE10	AE10	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_AF10	AF10	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_K24	K24	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_K23	K23	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_J22	J22	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_H24	H24	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_G25	G25	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_F25	F25	VDD33	B_2	N/A	Reserved. Must be left unconnected

表 4-13. Reserved Pin Functions (続き)

PIN		I/O POWER	I/O TYPE(1)	CLK SYSTEM	DESCRIPTION(2)
NAME	NUMBER				
RESERVED_G22	G22	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_E23	E23	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_C26	C26	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_AB4	AB4	VDD33	B_5	N/A	Reserved. Must be left unconnected
RESERVED_C23	C23	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_D21	D21	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_B24	B24	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_C22	C22	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_B23	B23	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_A20	A20	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_A19	A19	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_E18	E18	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_D19	D19	VDD33	B_2	N/A	Reserved. Must be left unconnected
RESERVED_C19	C19	VDD33	B_2	N/A	Reserved. Must be left unconnected

(1) Refer to I/O Type and Subscript Definition (表 4-15).
(2) Refer to the セクション 7.2.2 and the セクション 7.2.1 for a description between a one controller and a two controller configuration.

表 4-14. Power and Ground Pin Functions

PIN(3)		I/O TYPE(1)	DESCRIPTION(2)
NAME	NUMBER		
VDD33	F20, F17, F11, F8, L21, R21, Y21, AA19, AA16, AA10, AA7	PWR	3.3V I/O power
VDD18	C1, F5, G6, K6, M5, P5, T5, W6, AA5, AE1, H5, N6, T6, AA13, U21, P21, H21, F14	PWR	1.8V internal DRAMVDD and LVDSAVD I/O power (To shut this power down in a system low-power mode, see the セクション 8.3.)
VDDC	F19, F16, F13, F10, F7, H6, L6, P6, U6, Y6, AA8, AA11, AA14, AA17, AA20, W21, T21, N21, K21, G21, L11, T11, T16, L16	PWR	1.15V core power
PLLD_VDD	L22	PWR	1.15V DMD clock generator PLL Digital power
PLLD_VSS	L23	GND	1.15V DMD clock generator PLL Digital GND
PLLD_VAD	K25	PWR	1.8V DMD clock generator PLL Analog power
PLLD_VAS	K26	GND	1.8V DMD clock generator PLL Analog GND
PLLM1_VDD	L26	PWR	1.15V primary-LS clock generator PLL Digital power
PLLM1_VSS	M22	GND	1.15V primary-LS clock generator PLL Digital GND
PLLM1_VAD	L24	PWR	1.8V primary-LS clock generator PLL Analog power
PLLM1_VAS	L25	GND	1.8V primary-LS clock generator PLL Analog GND
PLLM2_VDD	P23	PWR	1.15V primary-HS clock generator PLL Digital power

表 4-14. Power and Ground Pin Functions (続き)

PIN[3]		I/O TYPE[1]	DESCRIPTION[2]
NAME	NUMBER		
PLLM2_VSS	P24	GND	1.15V primary-HS clock generator PLL Digital GND
PLLM2_VAD	R25	PWR	1.8V primary-HS clock generator PLL Analog power
PLLM2_VAS	R26	GND	1.8V primary-HS clock generator PLL Analog GND
PLLS_VAD	R23	PWR	1.15V video-2X clock generator PLL Analog power
PLLS_VAS	R24	GND	1.15V video-2X clock generator PLL Analog GND
L_VDQPAD_[7:0], R_VDQPAD_[7:0]	B18, D18, B17, E17, A18, C18, A17, D17, AE17, AC17, AF17, AC18, AB16, AD17, AB17, AD18	RES	DRAM direct test pins (for manufacturing use only). These pins must be tied directly to ground when in operation.
CFO_VDD33	AE26	RES	DRAM direct test control pin (for manufacturing use only). This pin must be tied directly to 3.3 I/O power (VDD33) when in operation.
VTEST1, VTEST2, VTEST3, VTEST4	AB14, AB15, E15, E16	RES	DRAM direct test control pins (for manufacturing use only). These pins must be tied directly to ground when in operation.
LVDS_AVS1, LVDS_AVS2	V5, K5	PWR	Dedicated ground for LVDS bandgap reference. These pins must be tied directly to ground when in operation.
VPGM	AC6	PWR	Fuse programming pin (for manufacturing use only). This pin must be tied directly to ground when in operation.
GND	A26, A25, A24, B25, C24, D23, E22, F21, F18, F15, F12, F9, F6, E5, D4, C3, B3, A3, B2, A2, B1, A1, G5, J5, J6, L5, M6, N5, R5, R6, U5, V6, W5, Y5, AA6, AB5, AC4, AD3, AE3, AF3, AF2, AF1, AA9, AA12, AA15, AA18, AA21, AB22, AC23, AD24, AE24, AF24, AE25, AF25, AF26, V21, M21, J21, L15, L14, L13, L12, M16, M15, M14, M13, M12, M11, N16, N15, N14, N13, N12, N11, P16, P15, P14, P13, P12, P11, R16, R15, R14, R13, R12, R11, T15, T14, T13, T12	GND	Common ground

表 4-15. I/O Type and Subscript Definition

I/O		ESD STRUCTURE
(SUBSCRIPT) (3)	DESCRIPTION	
1	N/A	N/A
2	3.3 LVTTL I/O buffer, with 8mA drive	ESD diode to VDD33 and GND
3	3.3 LVTTL I/O buffer, with 12mA drive	
4	3.3 LVTTL receiver	
5	3.3 LVTTL I/O buffer, with 8mA drive, with slew rate control	
6	3.3 LVTTL I/O buffer, with programmable 4mA, 8mA, or 12mA drive	
7	1.8V LVDS (DMD interface)	
8	3.3V I^2C with 3mA sink	
9	USB-compatible (3.3V)	
10	OSC 3.3V I/O compatible LVTTL	
(TYPE)		N/A
I	Input	
O	Output	
B	Bidirectional	
H	Hysteresis	
U	Includes an internal termination pullup resistor	
D	Includes an internal termination pulldown resistor	

(1) Refer to I/O Type and Subscript Definition (表 4-15).
(2) Refer to the セクション 7.2.2 and the セクション 7.2.1 for a description between a one controller and a two controller configuration.
(3) Refer to the セクション 9.1.7 for instructions on handling unused pins.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (see(1))

			MIN	MAX	UNIT
	Supply voltage (2) (3)	VDDC (core)	–0.3	1.6	V
		VDD18 (LVDSAVD I/O and internal DRAMVDD)	–0.3	2.5	
		VDD33 (I/O)	–0.3	3.9	
		PLLD_VDD (1.15V DMD clock generator – digital)	–0.3	1.6	
		PLLM1_VDD (1.15V primary-LS clock generator – digital)	–0.3	1.6	
		PLLM2_VDD (1.15V primary-HS clock generator – digital)	–0.3	1.6	
		PLLD_VAD (1.8V DMD clock generator – analog)	–0.3	2.5	
		PLLM1_VAD (1.8V primary-LS clock generator – analog)	–0.3	2.5	
		PLLM2_VAD (1.8V primary-HS clock generator – analog)	–0.3	2.5	
		PLLS_VAD (1.15V video-2X – analog)	–0.5	1.4	
V_I	Input voltage (4)	USB	–1	5.25	V
		OSC	–0.3	VDD33 + 0.3 V	
		3.3 LVTTL	–0.3	3.6	
		3.3 I^2C	–0.5	3.8	
V_O	Output voltage	USB	–1	5.25	V
		1.8 LVDS	–0.3	2.2	
		3.3 LVTTL	–0.3	3.6	
		3.3 I^2C	–0.5	3.8	
T_J	Operating junction temperature		0	111	°C
T_{stg}	Storage temperature		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in セクション 5.3. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) All voltage values are with respect to GND.
(3) All of the 3.3V, 1.8V, and 1.15V power must be applied and removed per the procedure defined in セクション 8.3. Overlap currents, if allowed to continue flowing unchecked not only increase total power dissipation in a circuit, but degrade the circuit reliability, thus shortening its usual operating life.
(4) Applies to external input and bidirectional buffers

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	DLPC900	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
			Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±300	
		DLPC900A	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) (4)	±1000	
			Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) (3)	+500 / –300	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
(3) CDM passes to –500V on all digital pins, however the PLL pins pass only to –300V, failing at –350V.
(4) HBM includes power supply combinations only. Non-supply pin to non-supply pin combinations not performed in accordance with qualification plan.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

		I/O (1)	MIN	NOM	MAX	UNIT
$V_{DD}33$	3.3V supply voltage, I/O		3.135	3.3	3.465	V
$V_{DD}18$	1.8V supply voltage, LVDSAVD and DRAMVDD		1.71	1.8	1.89	
VDDC	1.15V supply voltage, Core logic		1.100	1.15	1.200	
PLLD_V_{DD}	1.8V supply voltage, PLL analog		1.71	1.8	1.89	
PLLM1_V_{DD}	1.8V supply voltage, PLL analog		1.71	1.8	1.89	
PLLM2_V_{DD}	1.8V supply voltage, PLL analog		1.71	1.8	1.89	
PLLS_V_{DD}	1.15V supply voltage, PLL analog		1.090	1.15	1.200	
PLLD_V_{DD}	1.15V supply voltage, PLL digital		1.090	1.15	1.200	
PLLM1_V_{DD}	1.15V supply voltage, PLL digital		1.090	1.15	1.200	
PLLM2_V_{DD}	1.15V supply voltage, PLL digital		1.090	1.15	1.200	
V_I	Input voltage	USB (9)	0		VDD33	V
		OSC (10)	0		VDD33	
		3.3V LVTTL (1, 2, 3, 4)	0		VDD33	
		3.3V I^2C (8)	0		VDD33	
V_O	Output voltage	USB (8)	0		VDD33	V
		3.3V LVTTL (1, 2, 3, 4)	0		VDD33	
		3.3V I^2C (8)	0		VDD33	
		1.8V LVDS (7)	0		VDD18	
T_A	Operating ambient temperature range	See (2) and (3)	0		55	°C
T_C	Operating top-center case temperature	See (3) and (4)	0		109.16	°C
T_J	Operating junction temperature		0		111	°C

(1) The number inside the parentheses for the I/O refers to the I/O type defined in 表 4-15.
(2) Assumes minimum 1m/s airflow.
(3) Maximum thermal values assume max power of 4.76W (total for controller).
(4) Assume φ_{JT} equals 0.4°C/W.

5.4 Thermal Information

THERMAL METRIC		DLPC900 ZPC (BGA) 516 PINS	UNIT
$R_{\theta JC}$ (1)	Junction-to-case thermal resistance	4.4	°C/W
$R_{\theta JA}$ at 0 m/s of forced airflow (2)	Junction-to-air thermal resistance	14.4	°C/W
$R_{\theta JA}$ at 1 m/s of forced airflow (2)	Junction-to-air thermal resistance	9.5	°C/W
$R_{\theta JA}$ at 2 m/s of forced airflow (2)	Junction-to-air thermal resistance	9.0	°C/W
φ_{JT} (3)	Temperature variance from junction to package top center temperature, per unit power dissipation	0.4	°C/W

(1) $R_{\theta JC}$ analysis assumptions: The heat generated in the chip flows into overmold (top side) and also into the package laminate (bottom side) and then into PCB via package solder balls. Used for heat sink analysis only.
(2) Thermal coefficients abide by JEDEC Standard 51. $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC900 PCB and thus the reported thermal resistance can be inaccurate in the actual product application. Although the actual thermal resistance can be different, it is the best information available during the design phase to estimate thermal performance.
(3) Example: (3.2 W) × (0.4 C/W) ≈ 1.28°C temperature rise.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER (1)			TEST CONDITIONS (4)	MIN	TYP	MAX	UNIT
V_{IH}	High-level input threshold voltage	USB (9)		2			V
		OSC (10)		2			
		3.3V LVTTL (1, 2, 3, 4)		2			
		3.3V I^2C (8)		2.4		VDD33 + 0.5	
V_{IL}	Low-level input threshold voltage	USB (9)				0.8	V
		OSC (10)				0.8	
		3.3V LVTTL (1, 2, 3, 4)				0.8	
		3.3V I^2C (8)		–0.5		1	
V_{DIS}	Differential input sensitivity (Differential input voltage)	USB (9)		200			mV
V_{ICM}	Input common mode range (Differential cross point voltage)	USB (9)		0.8		2.5	V
V_{OH}	High-level output voltage	USB (9)		2.8			V
		1.8V LVDS (7)		1.52			
		3.3V LVTTL (1, 2, 3)	I_{OH} = Max rated	2.7			
V_{OL}	Low-level output voltage	USB (9)		0		0.3	V
		1.8V LVDS (7)				0.88	
		3.3V LVTTL (1, 2, 3)	I_{OL} = Max rated			0.4	
		3.3V I^2C (8)	I_{OL} = 3mA sink			0.4	
V_{OD}	Output differential voltage	1.8V LVDS (7)		0.065		0.44	V

5.5 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER [1]			TEST CONDITIONS [4]	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	USB (9)				200	µA
		OSC (10)		–10		10	
		3.3V LVTTL (1 to 4) (without internal pulldown)	V_{IH} = VDD33	–10		10	
		3.3V LVTTL (1 to 4) (with internal pulldown)	V_{IH} = VDD33	10		200	
		3.3V I^2C (8)	V_{IH} = VDD33			10	
I_{IL}	Low-level input current	USB (9)		–10		10	µA
		OSC (10)		–10		10	
		3.3V LVTTL (1 to 4) (without internal pullup)	V_{OH} = VDD33	–10		10	
		3.3V LVTTL (1 to 4) (with internal pullup)	V_{OH} = VDD33	–10		–200	
		3.3V I^2C (8)	V_{OH} = VDD33			–10	
I_{OH}	High-level output current [2]	USB (9)		–18.4			mA
		1.8V LVDS (7) (V_{OD} = 300 mV)	VO = 1.4 V	–6.5			
		3.3V LVTTL (1)	VO = 2.4V	–4			
		3.3V LVTTL (2)	VO = 2.4V	–8			
		3.3V LVTTL (3)	VO = 2.4V	–12			
I_{OL}	Low-level output current [3]	USB (9)		19.1			mA
		1.8V LVDS (7) (V_{OD} = 300 mV)	VO = 1V	6.5			
		3.3V LVTTL (1)	VO = 0.4V	4			
		3.3V LVTTL (2)	VO = 0.4V	8			
		3.3V LVTTL (3)	VO = 0.4V	12			
		3.3V I^2C (8)		3			
I_{OZ}	High-impedance leakage current	USB (9)		–10		10	µA
		LVDS (7)		–10		10	
		3.3V LVTTL (1, 2, 3)		–10		10	
		3.3V I^2C (8)		–10		10	
C_I	Input capacitance (including package)	USB (9)		11.84		17.07	pF
		3.3V LVTTL (1)		3.75		5.52	
		3.3V LVTTL (2)		3.75		5.52	
		3.3V LVTTL (4)		3.75		5.52	
		3.3V I^2C (8)		5.26		6.54	

5.5 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER (1)		TEST CONDITIONS (4)	MIN	TYP	MAX	UNIT
I_{CC11}	Supply voltage, 1.15V core power	Normal mode			2368	mA
I_{CC18}	Supply voltage, 1.8V power (LVDS I/O and internal DRAM)	Normal mode			1005	mA
I_{CC33}	Supply voltage, 3.3V I/O power	Normal mode			33	mA
I_{CC11_PLLD}	Supply voltage, DMD PLL digital power (1.15V)	Normal mode		4.4	6.2	mA
I_{CC11_PLLM1}	Supply voltage, primary-LS clock generator PLL digital power (1.15V)	Normal mode		4.4	6.2	mA
I_{CC11_PLLM2}	Supply voltage, primary-HS clock generator PLL digital power (1.15V)	Normal mode		4.4	6.2	mA
I_{CC18_PLLD}	Supply voltage, DMD PLL analog power (1.8V)	Normal mode		8	10.2	mA
I_{CC18_PLLM1}	Supply voltage, primary-LS clock generator PLL analog power (1.8V)	Normal mode		8	10.2	mA
I_{CC18_PLLM2}	Supply voltage, primary-HS clock generator PLL analog power (1.8V)	Normal mode		8	10.2	mA
I_{CC11_PLLS}	Supply voltage, video-2X PLL analog power (1.15V)	Normal mode			2.9	mA
Total Power in Normal Mode					4.76	W

(1) The number inside the parentheses for the I/O refers to the I/O type defined in 表 4-15.
(2) VDDQ = 1.7V; VOUT = 1420mV. (VOUT – VDDQ) / I_{OH} must be < 21Ω for values of VOUT between VDDQ and VDDQ – 280mV.
(3) VDDQ = 1.7V; VOUT = 280mV. VOUT / I_{OL} must be < 21Ω for values of VOUT between 0 V and 280mV.
(4) Normal mode refers to DLPC900 operation during full functionality. Typical values correspond to power dissipated on nominal process devices operating at nominal voltage and 70°C junction temperature (approximately 25°C ambient) displaying typical video-graphics content from a high-frequency source. Max values correspond to power dissipated on fast-process devices operating at high voltage and 105°C junction temperature (approximately 55°C ambient) displaying typical video-graphics content from a high-frequency source. The increased power dissipation observed on fast-process devices operated at max recommended temperature is primarily a result of increased leakage current.

5.6 System Oscillators Timing Requirements (1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, MOSC1 Stability and Tolerance. Crystal frequency 20MHz(2)		19.998 100	20.002 100	MHz ppm
t_c	Cycle time, MOSC1		49.995	50.005	ns
$t_{w(H)}$	Pulse duration2, MOSC, high	50% to 50% reference points (signal)	20		ns
$t_{w(L)}$	Pulse duration2, MOSC, low	50% to 50% reference points (signal)	20		ns
t_t	Transition time2, MOSC, $t_t = t_f / t_r$	20% to 80% reference points (signal)		12	ns
t_{jp}	Period jitter2, MOSC (The deviation in period from ideal period due solely to high-frequency jitter – not spread spectrum clocking)			18	ps

(1) Applies only when driven through an external digital oscillator. The MOSC input cannot support spread spectrum clock spreading.
(2) Including impact to accuracy due to aging, temperature, and trim sensitivity.

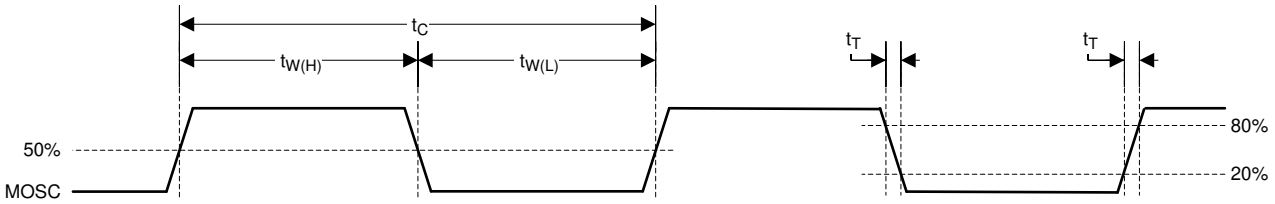


図 5-1. System Oscillators

5.7 Power-Up and Power-Down Timing Requirements

All DMDs supported by the DLPC900 controller require Firmware Version 4.0.0 or later.

表 5-1. Power-Up and Power-Down Timing Requirements

			MIN	MAX	UNIT
$t_{w1(L)}$	Pulse duration, inactive low, PWRGOOD	50% to 50% reference points (signal)	4		µs
$t_{w1(L)}$	Pulse duration with 1.8 V on, inactive low, PWRGOOD	50% to 50% reference points (signal)		1000	ms
	Pulse duration with 1.8 V off, inactive low, PWRGOOD			indefinite	ms
t_{t1}	Transition time, PWRGOOD, $t_{t1} = t_f / t_r$	20% to 80% reference points (signal)		625	µs
$t_{w2(L)}$	Pulse duration, inactive low, POSENSE	50% to 50% reference points (signal)	500		µs
$t_{w2(L)}$	Pulse duration with 1.8 V on, inactive low, POSENSE	50% to 50% reference points (signal)		1000	ms
	Pulse duration with 1.8 V off, inactive low, POSENSE			indefinite	ms
t_{t2}	Transition time, POSENSE, $t_{t2} = t_f / t_r$	20% to 80% reference points (signal)		25 (1)	µs
t_{PH}	Power hold time, POSENSE remains active after PWGOOD is deasserted.	20% to 80% reference points (signal)	500		µs
t_{ePH}	Extended power hold time for revision "B" and later DMDs		20		ms
t_{SB}	Total standby and power down time		123		s
$t_{w1(L)} + t_{w2(L)}$	The sum of PWRGOOD and POSENSE inactive time with 1.8 V on			1050	ms
	The sum of PWRGOOD and POSENSE inactive time with 1.8 V off			indefinite	ms

(1) As long as noise on this signal is below the hysteresis threshold.

5.7.1 Power-Up

POSENSE and PWRGOOD are active high signals that are generated by an external voltage monitor circuit. POSENSE must only be driven active high when all the controller and DMD supply voltages have reached 90% of their specified minimum voltage. The DLPC900 is safe to exit its RESET state once PWRGOOD is driven high. PWRGOOD has no impact on operation for 60 ms after rising edge of POSENSE.

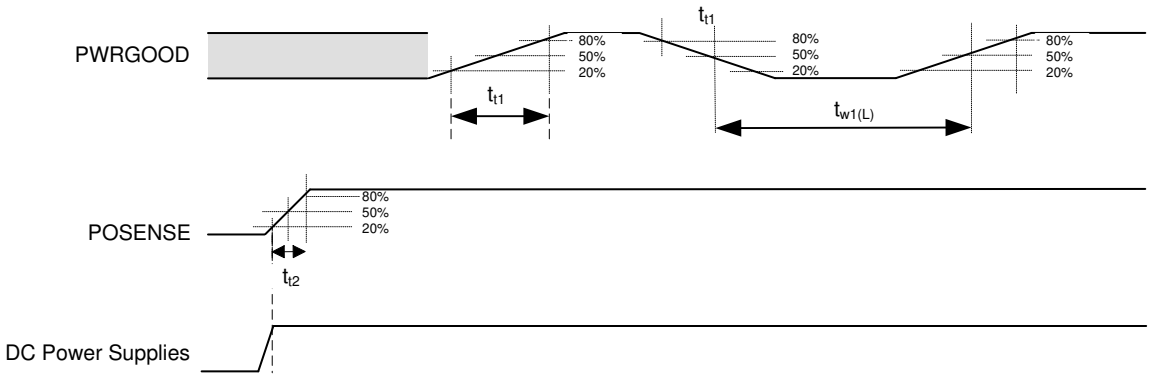


図 5-2. Power Up Timing Diagram

5.7.2 Power-Down

PWRGOOD cannot be used as an early warning signal for an anticipated power down. DMDs require an enhanced power down where the DLPC900 performs a sequence of memory loads to the DMD followed by the mirror park instruction so that the mirrors end up in an un-landed state. Issue the power-down command before unplugging the power cord from the system.

There are two scenarios to consider when powering down DMDs supported by the DLPC900. 図 5-3 shows a power distribution layout for a typical system, which provides the mechanisms for both scenarios:

1. An anticipated power down, which is during a typical power down of the system. Anticipated Power Down Timing Diagram shows a timing diagram where an external host sends a power-down command to the microprocessor (µP). **The µP must send a *Power Mode = 1 "Standby"* command to the DLPC900**. The DLPC900 then performs the necessary power down sequence on the DMD. The power can be safely removed once the minimum t_{SB} is met.
2. An unanticipated power loss. In this case, a power loss detection circuit must provide a means of triggering a power loss. 図 5-5 shows a timing diagram where the Voltage Monitor detects a power loss and deasserts PWRGOOD. **Power Regulation must maintain the DC Power Supplies until the minimum t_{ePH} is met.** During t_{ePH} the DLPC900 performs the necessary power-down sequence on the DMD. The power supplies can be allowed to drop below their specifications once the minimum t_{ePH} is met.

Refer to the *DLPC900 Programmer's Guide* for a description of the *Power Mode = 1 "Standby"* command.

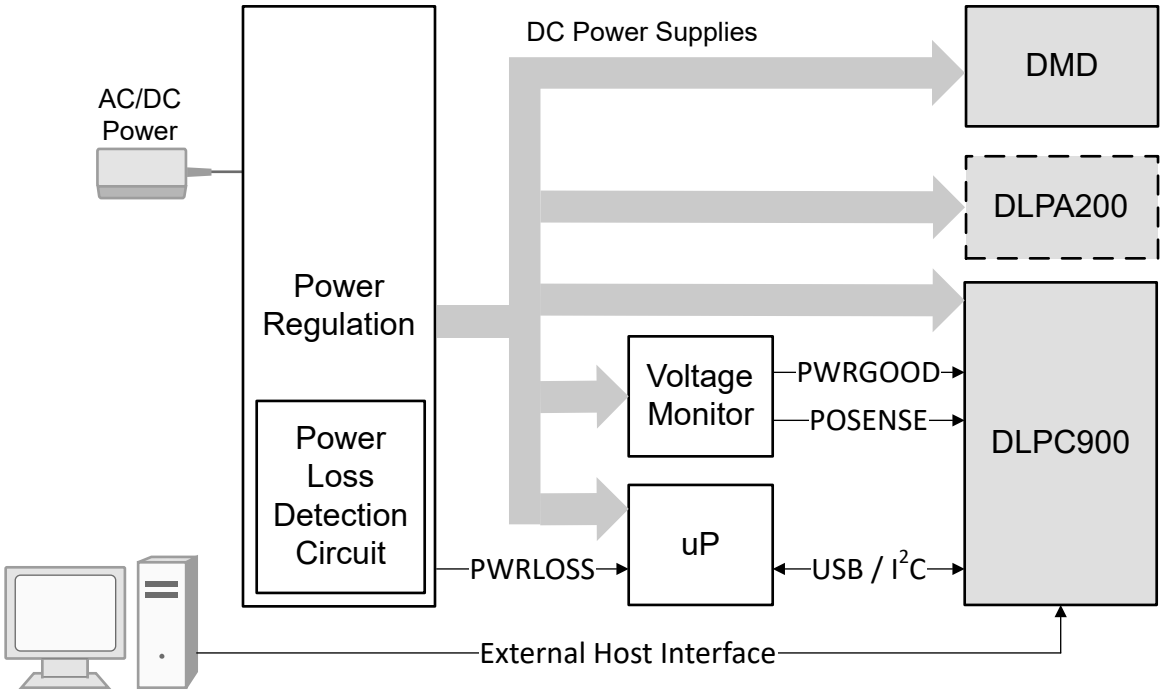


図 5-3. Power Distribution Layout Example

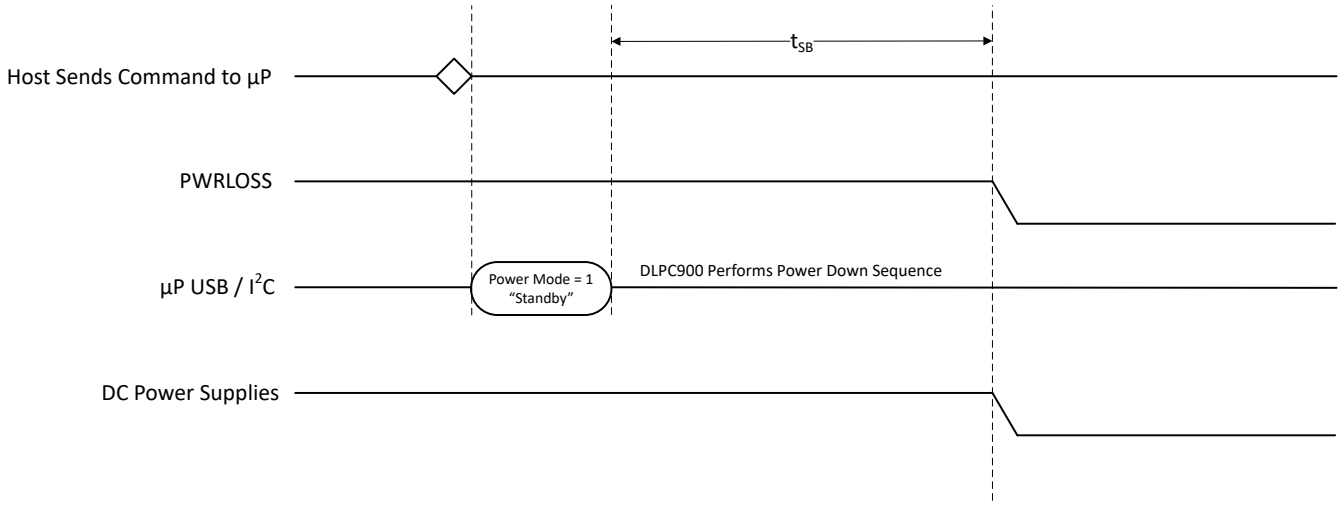


図 5-4. Anticipated Power Down Timing Diagram

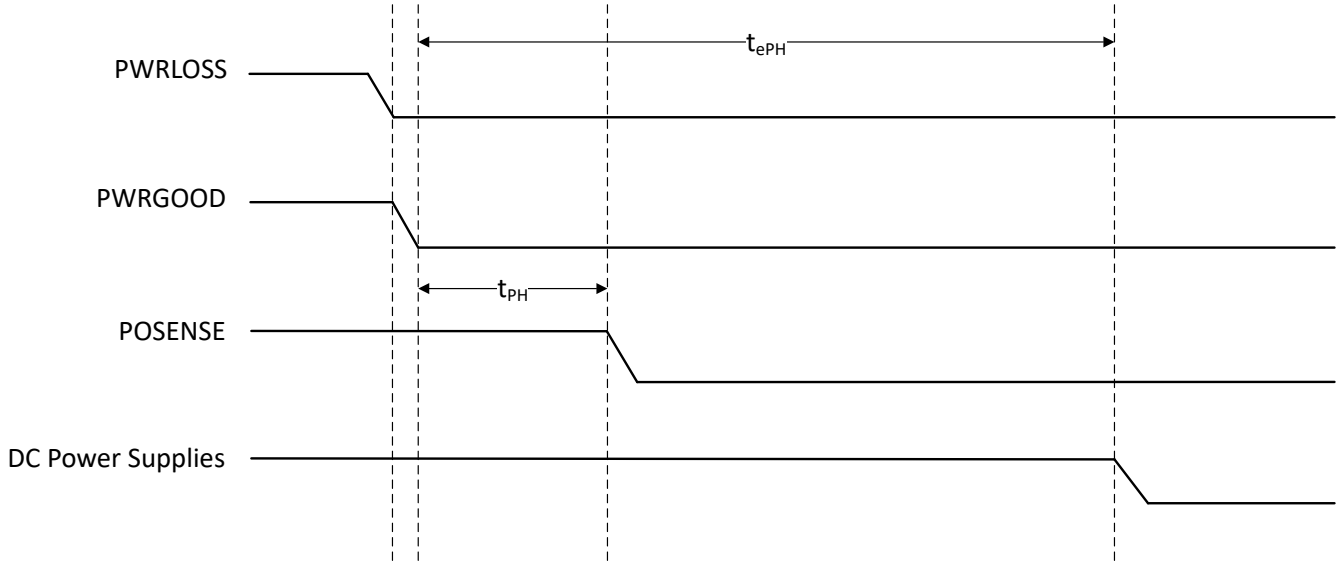


図 5-5. Unanticipated Power Loss Timing Diagram

5.8 JTAG Interface: I/O Boundary Scan Application Timing Requirements

			MIN	MAX	UNIT
f_{clock}	Clock frequency, TCK			10	MHz
t_c	Cycle time, TCK		100		ns
$t_{w(H)}$	Pulse duration, high	50% to 50% reference points (signal)	40		ns
$t_{w(L)}$	Pulse duration, low	50% to 50% reference points (signal)	40		ns
t_t	Transition time, $t_t = t_f / t_r$	20% to 80% reference points (signal)		5	ns
t_{su}	Setup time, TDI valid before TCK ↑		8		ns
t_h	Hold time, TDI valid after TCK ↑		2		ns
t_{su}	Setup time, TMS1 valid before TCK ↑		8		ns
t_h	Hold time, TMS1 valid after TCK ↑		2		ns

5.9 JTAG Interface: I/O Boundary Scan Application Switching Characteristics

Switching characteristics over recommended operating conditions, C_L (min timing) = 5pF, C_L (max timing) = 85pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}	Output propagation, clock to Q	TCK ↑	TDO1	3	12	ns

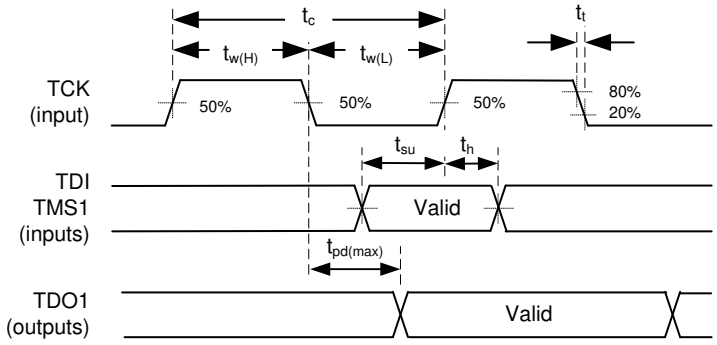


図 5-6. I/O Boundary Scan

5.10 Programmable Output Clocks Switching Characteristics

Switching characteristics over recommended operating conditions, C_L (min timing) = 5pF, C_L (max timing) = 50pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{clock}	Clock frequency, OCLKA (1)	N/A	OCLKA	0.787	50.00	MHz
t_c	Cycle time, OCLKA	N/A	OCLKA	20.00	1270.6	ns
$t_{w(H)}$	Pulse duration, high (2) 50% to 50% reference points (signal)	N/A	OCLKA	(t_c / 2) – 2		ns
$t_{w(L)}$	Pulse duration, low (2) 50% to 50% reference points (signal)	N/A	OCLKA	(t_c / 2) – 2		ns
	Jitter	N/A	OCLKA		350	ps

(1) The frequency of OCLKA is programmable.
(2) The duty cycle of OCLKA will be within ±2ns of 50%.

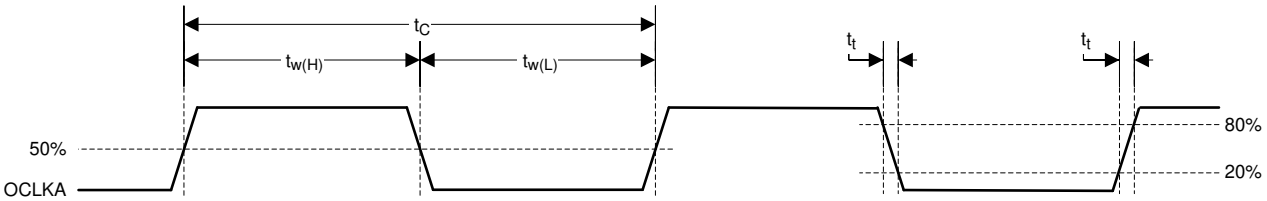


図 5-7. Programmable Output Clocks

5.11 Port 1 and 2 Input Pixel Interface Timing Requirements

			MIN	MAX	UNIT
f_{clock}	Clock frequency, P_CLK1, P_CLK2, P_CLK3 (24-bit bus セクション 6.3.5.6)		12	175	MHz
f_{clock}	Clock frequency, P_CLK1, P_CLK2, P_CLK3 (48-bit bus セクション 6.3.5.6) See セクション 5.12.		12	141	MHz
t_c	Cycle time, P_CLK1, P_CLK2, P_CLK3		5.714	83.33	ns
$t_{w(H)}$	Pulse duration, high	50% to 50% reference points (signal)	2.3		ns
$t_{w(L)}$	Pulse duration, low	50% to 50% reference points (signal)	2.3		ns
t_{jp}	Clock period jitter P_CLK1, P_CLK2, P_CLK3 (that is, the deviation in period from ideal period)	Max f_{clock}		See (1)	ps
t_t	Transition time, $t_t = t_f$ / t_r, P_CLK1, P_CLK2, P_CLK3	20% to 80% reference points (signal)	0.6	2.0	ns
t_t	Transition time, $t_t = t_f$ / t_r, P1_A(9:0), P1_B(9:0) , P1_C(9:0), P1_HSYNC, P1_VSYNC, P1_DATEN	20% to 80% reference points (signal)	0.6	3.0	ns
t_t	Transition time, $t_t = t_f$ / t_r	20% to 80% reference points (signal)	0.6	3.0	ns
t_{su}	Setup time, P1_A(9:0), valid before P_CLK1, P_CLK2, or P_CLK3		0.8		ns
t_h	Hold time, P1_A(9:0), valid after P_CLK1, P_CLK2, or P_CLK3		0.8		ns
t_{su}	Setup time, P1_B(9:0), valid before P_CLK1, P_CLK2, or P_CLK3		0.8		ns
t_h	Hold time, P1_B(9:0), valid after P_CLK1, P_CLK2, or P_CLK3		0.8		ns
t_{su}	Setup time, P1_C(9:0), valid before P_CLK1, P_CLK2, or P_CLK3		0.8		ns
t_h	Hold time, P1_C(9:0), valid after P_CLK1, P_CLK2, or P_CLK3		0.8		ns
t_{su}	Setup time, P1_VSYNC, valid before P_CLK1, P_CLK2, or P_CLK3		0.8		ns
t_h	Hold time, P1_VSYNC, valid after P_CLK1, P_CLK2, or P_CLK3		0.8		ns
t_{su}	Setup time, P1_HSYNC, valid before P_CLK1, P_CLK2, or P_CLK3		0.8		ns

5.11 Port 1 and 2 Input Pixel Interface Timing Requirements (続き)

		MIN	MAX	UNIT
t_h	Hold time, P1_HSYNC, valid after P_CLK1, P_CLK2, or P_CLK3	0.8		ns
t_{su}	Setup time, P2_A(9:0), valid before P_CLK1, P_CLK2, or P_CLK3	0.8		ns
t_h	Hold time, P2_A(9:0), valid after P_CLK1, P_CLK2, or P_CLK3	0.8		ns
t_{su}	Setup time, P2_B(9:0), valid before P_CLK1, P_CLK2, or P_CLK3	0.8		ns
t_h	Hold time, P2_B(9:0), valid after P_CLK1, P_CLK2, or P_CLK3	0.8		ns
t_{su}	Setup time, P2_C(9:0), valid before P_CLK1, P_CLK2, or P_CLK3	0.8		ns
t_h	Hold time, P2_C(9:0), valid after P_CLK1, P_CLK2, or P_CLK3	0.8		ns
t_{su}	Setup time, P2_VSYNC, valid before P_CLK1, P_CLK2, or P_CLK3	0.8		ns
t_h	Hold time, P2_VSYNC, valid after P_CLK1, P_CLK2, or P_CLK3	0.8		ns
t_{su}	Setup time, P2_HSYNC, valid before P_CLK1, P_CLK2, or P_CLK3	0.8		ns
t_h	Hold time, P2_HSYNC, valid after P_CLK1, P_CLK2, or P_CLK3	0.8		ns
t_{su}	Setup time, P_DATEN1, valid before P_CLK1, P_CLK2, or P_CLK3	0.8		ns
t_h	Hold time, P_DATEN1, valid after P_CLK1, P_CLK2, or P_CLK3	0.8		ns
t_{su}	Setup time, P_DATEN2, valid before P_CLK1, P_CLK2, or P_CLK3	0.8		ns
t_h	Hold time, P_DATEN2, valid after P_CLK1, P_CLK2, or P_CLK3	0.8		ns
t_w(A)	VSYNC active pulse duration	1		Video line
t_w(A)	HSYNC active pulse duration	16		Pixel clocks

(1) For frequencies (f_{clock}) less than 175MHz, use the following formula to obtain the jitter: Max clock jitter = ± [(1 / f_{clock}) – 5414ps].

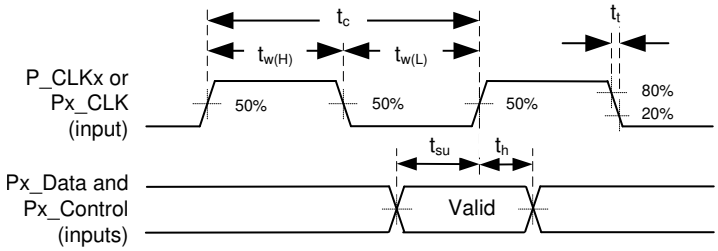


図 5-8. Input Port 1 and 2 Interface

5.12 Two Pixels Per Clock (48-Bit Bus) Timing Requirements

When operating in two pixels per clock mode, the pixel clock must be maintained below 141MHz. A typical video source requiring two pixels per clock is shown in the following table and must have reduced blanking to stay below the maximum pixel clock.

SOURCE	RATE (Hz)	TOTAL PIXELS PER LINE (1)	TOTAL LINES PER FRAME (1)	PIXEL CLOCK ACHIEVED (MHz)
1080p	120	2060	1120	138.4

(1) Values chosen for front and back porches must meet the timing requirements in セクション 5.16.

5.13 Synchronous Serial Port (SSP) Switching Characteristics

Switching characteristics over recommended operating conditions, C_L (min timing) = 5pF, C_L (max timing) = 50pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{clock}	Clock frequency, SSPx_CLK	N/A	SSPx_CLK	73.00	25000	kHz
t_c	Cycle time, SSPx_CLK	N/A	SSPx_CLK	0.040	13.6	µs
$t_w(H)$	Pulse duration, high 50% to 50% reference points (signal)	N/A	SSPx_CLK	40%		
$t_w(L)$	Pulse duration, low 50% to 50% reference points (signal)	N/A	SSPx_CLK	40%		
SSP MASTER						
t_{pd}	Output propagation, clock to Q, SSPx_DO	SSPx_CLK ↓ (1) (2)	SSPx_DO (1) (2)	–5	5	ns
		SSPx_CLK ↑ (1) (3)	SSPx_DO (1) (3)	–5	5	ns
SSP SLAVE						
t_{pd}	Output propagation, clock to Q, SSPx_DO	SSPx_CLK ↓ (1) (2)	SSPx_DO (1) (2)	0	34	ns
		SSPx_CLK ↑ (1) (3)	SSPx_DO (1) (3)	0	34	ns

(1) The SSP is configured into four different modes of operation by the controller firmware. These modes are shown in 表 5-2, 図 5-10, and 図 5-11.
(2) SPI Modes 0 and 3
(3) SPI Modes 1 and 2

表 5-2. SSP Clock Operational Modes

SPI CLOCKING MODE	SPI CLOCK POLARITY (CPOL)	SPI CLOCK PHASE (CPHA)
0	0	0
1	0	1
2	1	0
3	1	1

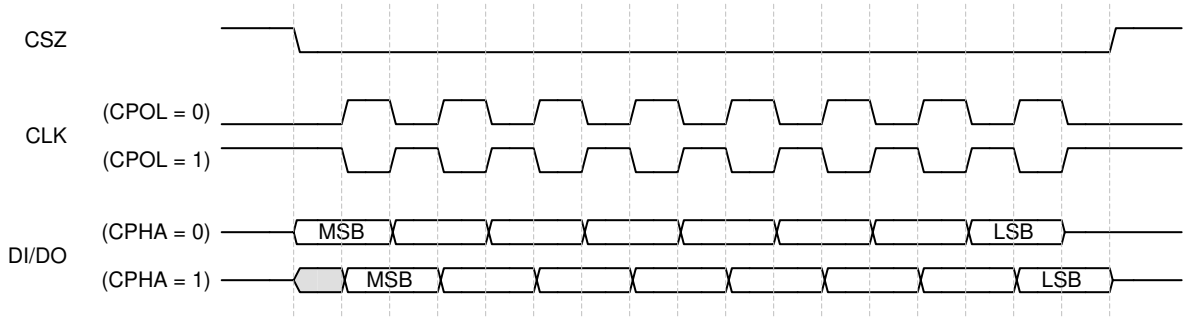


図 5-9. SSP Clock Mode Timing Diagram

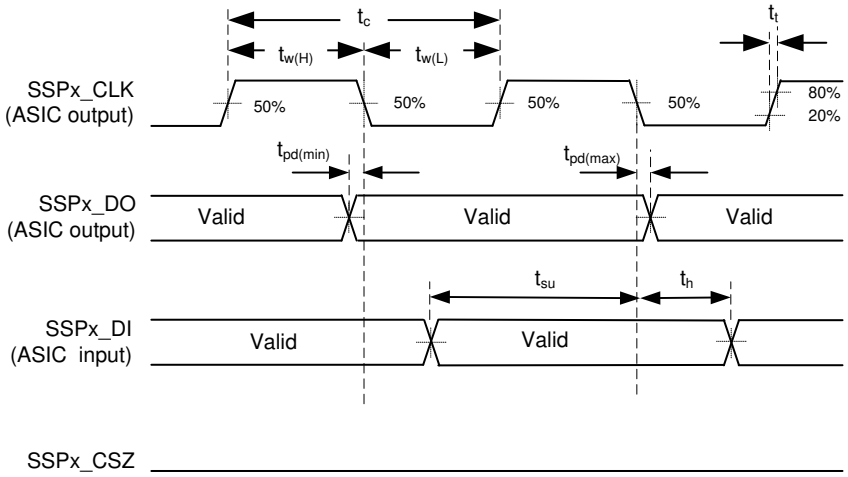


図 5-10. Synchronous Serial Port Interface—Master (Modes 0/3)

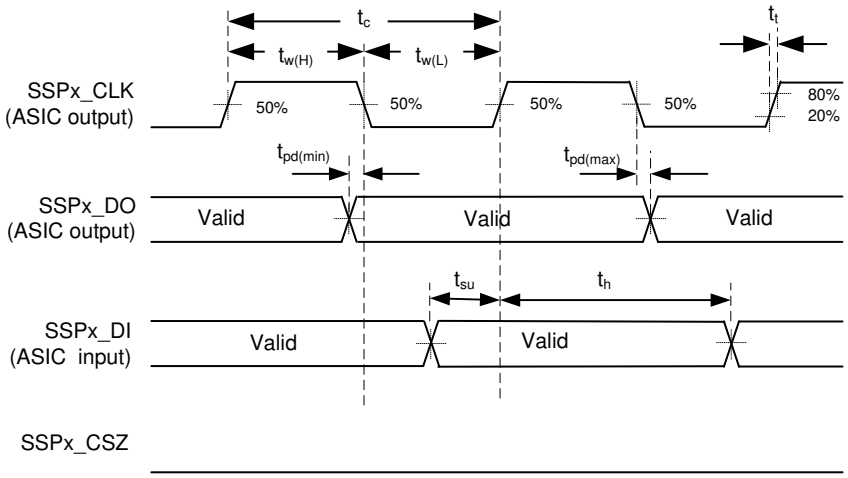


図 5-11. Synchronous Serial Port Interface—Slave (Modes 0/3)

5.14 DMD Interface Switching Characteristics

over recommended operating conditions, C_L (min timing) = 5pF, C_L (max timing) = 50pF (unless otherwise noted)

PARAMETER[1]		FROM	TO	MIN	MAX	UNIT
DMD TIMING MODE 0 [2]						
$t_{w(H)}$	DMD strobe high pulse duration	N/A	DADSTRB	29		ns
$t_{w(L)}$	DMD strobe low pulse duration	N/A	DADSTRB	29		ns
$T_{odv\text{-}min}$	Output data valid window, DADADDR_(3:0), DADMODE_(1:0), DADSEL_(1:0) with respect to DADSTRB	DADADDR_(3:0) DADMODE_(1:0) DADSEL_(1:0)	DADSTRB ↑ (1)	–27		ns
$T_{odv\text{-}max}$	Output data valid window, DADADDR_(3:0), DADMODE_(1:0), DADSEL_(1:0) with respect to DADSTRB	DADADDR_(3:0) DADMODE_(1:0) DADSEL_(1:0)	DADSTRB ↑ (1)	27		ns
DMD TIMING MODE 1 [2]						
t_w(H)	DMD strobe pulse duration	N/A	DADSTRB	14		ns
t_w(L)	DMD strobe low pulse duration	N/A	DADSTRB	14		ns
$T_{odv\text{-}min}$	Output data valid window, DADADDR_(3:0), DADMODE_(1:0), DADSEL_(1:0) with respect to DADSTRB	DADADDR_(3:0) DADMODE_(1:0) DADSEL_(1:0)	DADSTRB ↑ (1)	–12		ns
$T_{odv\text{-}max}$	Output data valid window, DADADDR_(3:0), DADMODE_(1:0), DADSEL_(1:0) with respect to DADSTRB	DADADDR_(3:0) DADMODE_(1:0) DADSEL_(1:0)	DADSTRB ↑ (1)	12		ns

(1) DMD control signals are captured on the rising edge of DADSTRB within the DMD.
(2) The DMD timing mode is controlled by the controller firmware.

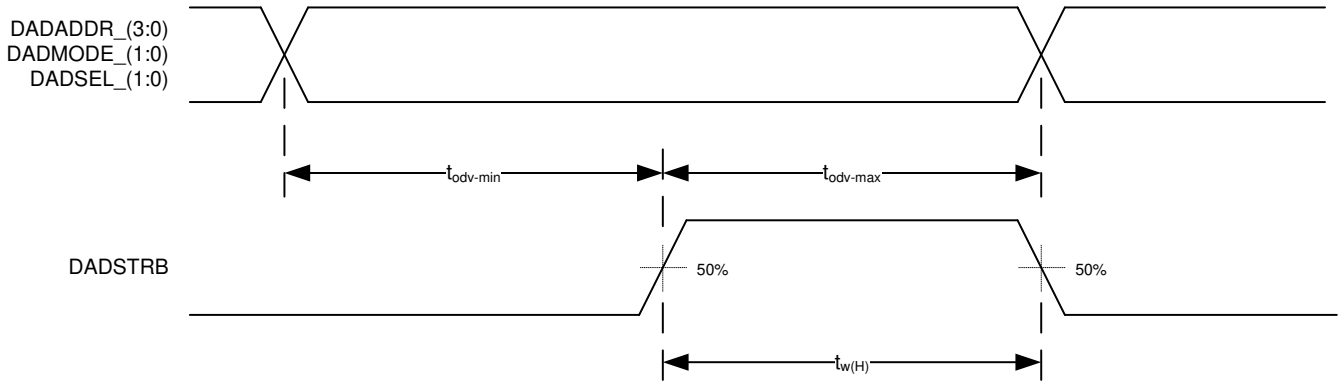


図 5-12. DMD Interface Timing

5.15 DMD LVDS Interface Switching Characteristics

Switching characteristics over recommended operating conditions (1) (2) (3) (4) (5) (6)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{clock}	Clock frequency, DCK_A	N/A	DCK_A	100	400	MHz
t_c	Cycle time, DCK_A1	N/A	DCK_A	2475.3		ps
$t_{w(H)}$	Pulse duration, high 5 (50% to 50% reference points)	N/A	DCK_A	1093		ps
$t_{w(L)}$	Pulse duration, low 5 (50% to 50% reference points)	N/A	DCK_A	1093		ps
t_t	Transition time, $t_t = t_f$ / t_r (20% to 80% reference points)	N/A	DCK_A	100	400	ps
t_{osu}	Output setup time at max clock rate3	DCK_A ↑ ↓	SCA, DDA(15:0)	438		ps
t_{oh}	Output hold time at max clock rate3	DCK_A ↑ ↓	SCA, DDA(15:0)	438		ps
f_{clock}	Clock frequency, DCK_B	N/A	DCK_B	100	400	MHz
t_c	Cycle time, DCK_B1	N/A	DCK_B	2475.3		ps
$t_{w(H)}$	Pulse duration, high 5 (50% to 50% reference points)	N/A	DCK_B	1093		ps
$t_{w(L)}$	Pulse duration, low 5 (50% to 50% reference points)	N/A	DCK_B	1093		ps
t_t	Transition time, $t_t = t_f$ / t_r (20% to 80% reference points)	N/A	DCK_B	100	400	ps
t_{osu}	Output setup time at max clock rate3	DCK_B ↑ ↓	SCB, DDB(15:0)	438		ps
t_{oh}	Output hold time at max clock rate3	DCK_B ↑ ↓	SCB, DDB(15:0)	438		ps
t_{sk}	Output skew, channel A to channel B	DCK_A ↑	DCK_B ↑		250	ps

(1) The minimum cycle time (t_c) for DCK_A and DCK_B includes 1.0% spread spectrum modulation.
(2) The DMD LVDS interface uses a double data rate (DDR) clock, thus both rising and falling edges of DCK_A and DCK_B are used to clock data into the DMD. As a result, the minimum $t_{w(H)}$ and $t_{w(L)}$ parameters determine the worse-case DDR clock cycle time.
(3) Output setup and hold times for DMD clock frequencies below the maximum can be calculated as follows: $t_{osu}(f_{clock}) = t_{osu}(f_{max}) + 250000 \times (1 / f_{clock} - 1 / 400)$ and $t_{oh}(f_{clock}) = t_{oh}(f_{max}) + 250000 \times (1 / f_{clock} - 1 / 400)$ where f_{clock} is in MHz.
(4) The DLPC900 is a full-bus DMD signaling interface. 図 6-4 shows the controller connections for this configuration.
(5) The pulse duration minimum for any clock rate can be calculated using the following formulas.
    a. Pulse duration minimum when using spread spectrum
        i. Duty cycle % = 49.06 – [0.01335 × clock frequency (MHz)]
        ii. Minimum pulse duration = 1 / clock frequency × DC%
            1. Example: At 400MHz: DC% = 49.06 – [0.01335 × 400] = 43.72%
            2. MPW = 1 / 400MHz × 0.4372 = 1093.0ps
    b. Pulse duration minimum when not using spread spectrum
        i. Duty cycle % = 49.00 – [0.01055 × clock frequency (MHz)]
        ii. Minimum pulse duration = 1 / clock frequency × DC%
            1. Example: At 400MHz: DC% = 49.00 – [0.01055 × 400] = 44.78%
            2. MPW = 1 / 400MHz × 0.448 = 1119.5ps
(6) A duty cycle specification is not provided because the key limiting factor to clock frequency is the minimum pulse duration (that is, if the other half of the clock period is larger than the minimum, it is not limiting the clock frequency).

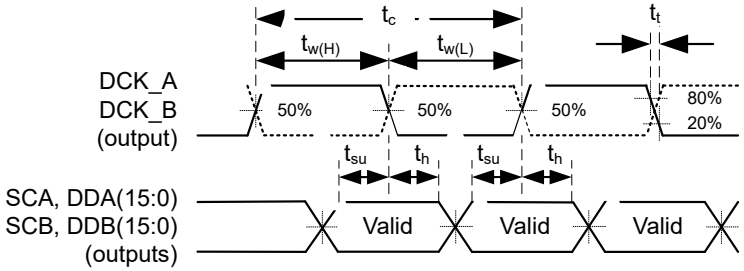


図 5-13. DMD LVDS Interface

5.16 Source Input Blanking Requirements

PORT	PARAMETER (1)	MINIMUM BLANKING
Port 1 Vertical Blanking	VBP	370µs
	VFP	1 Line
	Total vertical blanking	370µs + 2 lines
Port 2 Vertical Blanking	VBP	370µs
	VFP	1 line
	Total vertical blanking	370µs + 2 lines
Port 1 and 2 Horizontal Blanking	HBP	10 pixels
	HFP	0 pixels
	Total horizontal blanking	80 pixels

(1) Refer to セクション 10.1.3.

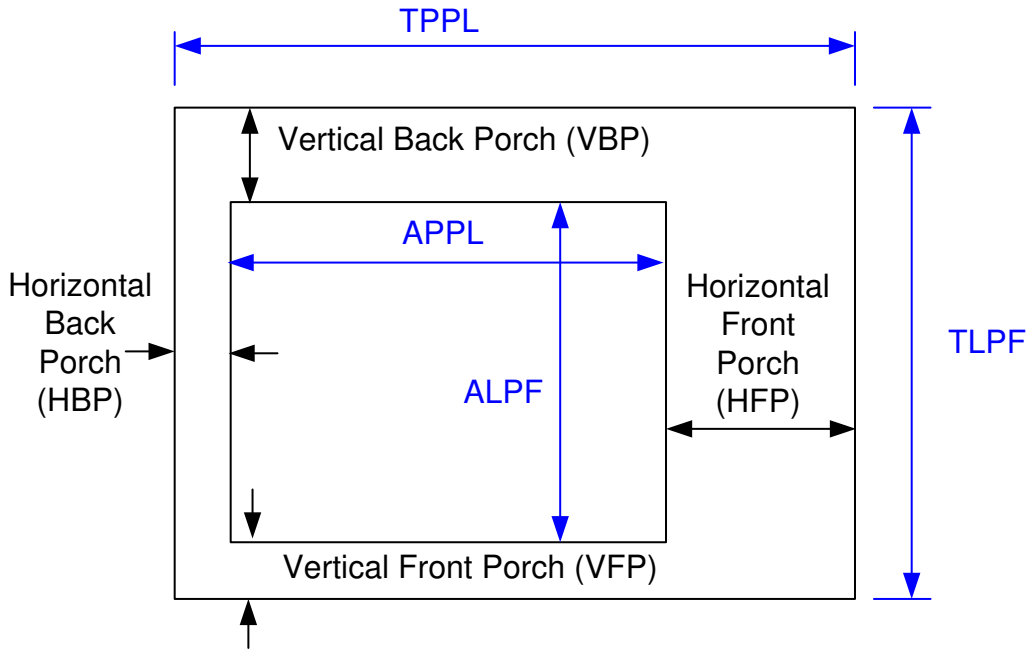


図 5-14. Video Timing Parameters

6 Detailed Description

6.1 Overview

The DLPC900 controller processes the digital input image and converts the data into the digital format needed by the DLP500YX, DLP670S, DLP9000, DLP5500, or DLP6500. The DLP500YX, DLP670S, DLP9000, DLP5500, and DLP6500 reflect light using binary pulse-width-modulation (PWM) for each micromirror. For further details, refer to the DLP500YX, DLP670S, DLP9000, DLP5500, or DLP6500 data sheets.

A single DLPC900 controller combined with a DLP5500 or DLP6500 supports a wide variety of resolutions from XGA to 1080p. When accurate pattern display is needed, a native 1080p resolution source is used for a one-to-one association with the corresponding micromirror on the DLP6500. A native XGA resolution is used for a one-to-one association with the corresponding micromirror on the DLP5500.

Two DLPC900 controllers combined with a DLP500YX, DLP670S, or DLP9000 support only native resolution for a one-to-one association with the corresponding micromirror on the DMD. All combinations are well-suited for structured light, additive manufacturing, or digital exposure applications.

6.2 Functional Block Diagram

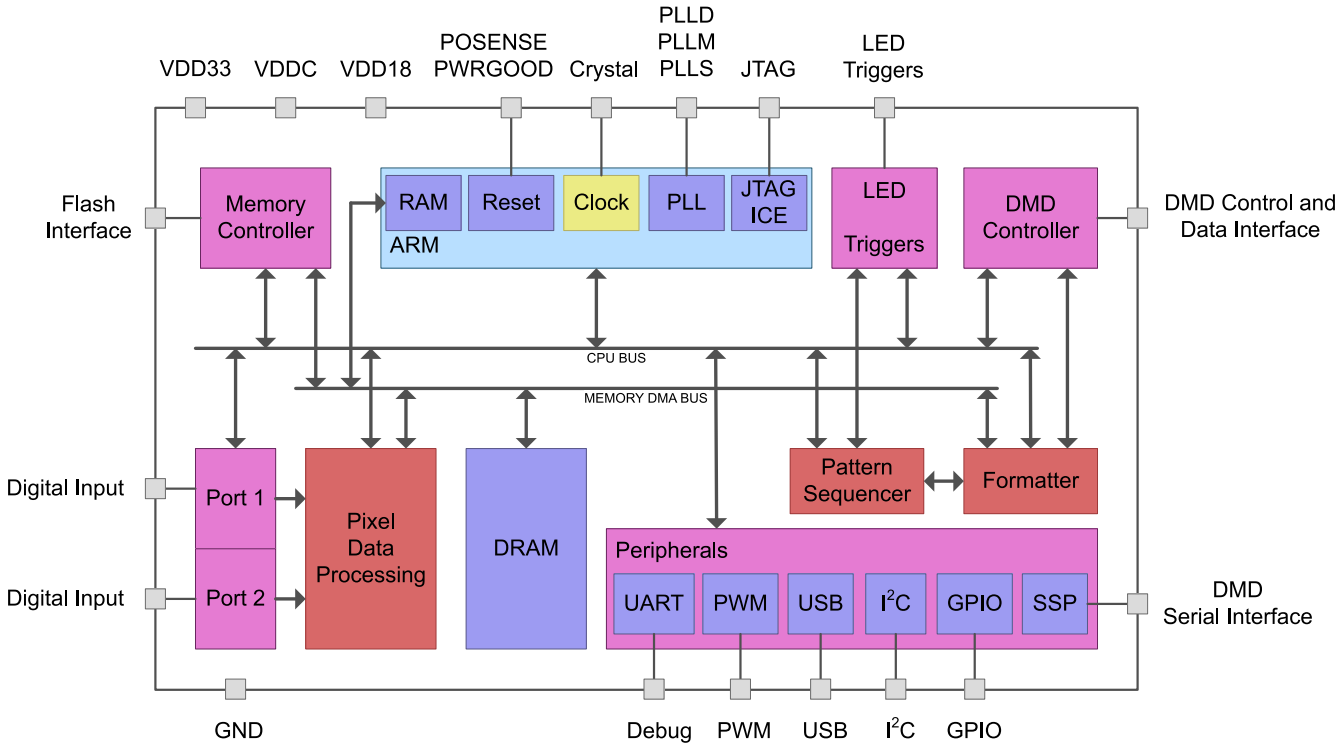


図 6-1. Functional Block Diagram

6.3 Feature Description

The DLPC900 controller takes as input 16-, 20-, or 24-bit RGB data at up to 120Hz frame rate. For example, a 120Hz 24-bit frame is composed of three colors (red, green, and blue) with each color equally divided in the 120Hz frame rate. Thus, each color has a 2.78ms time slot allocated. Because each color has an 8-bit depth, each color time slot is further divided into bit-planes. A bit-plane is the 2-dimensional arrangement of one-bit extracted from all the pixels in the full-color 2D image to implement dynamic depth (see 図 6-2).

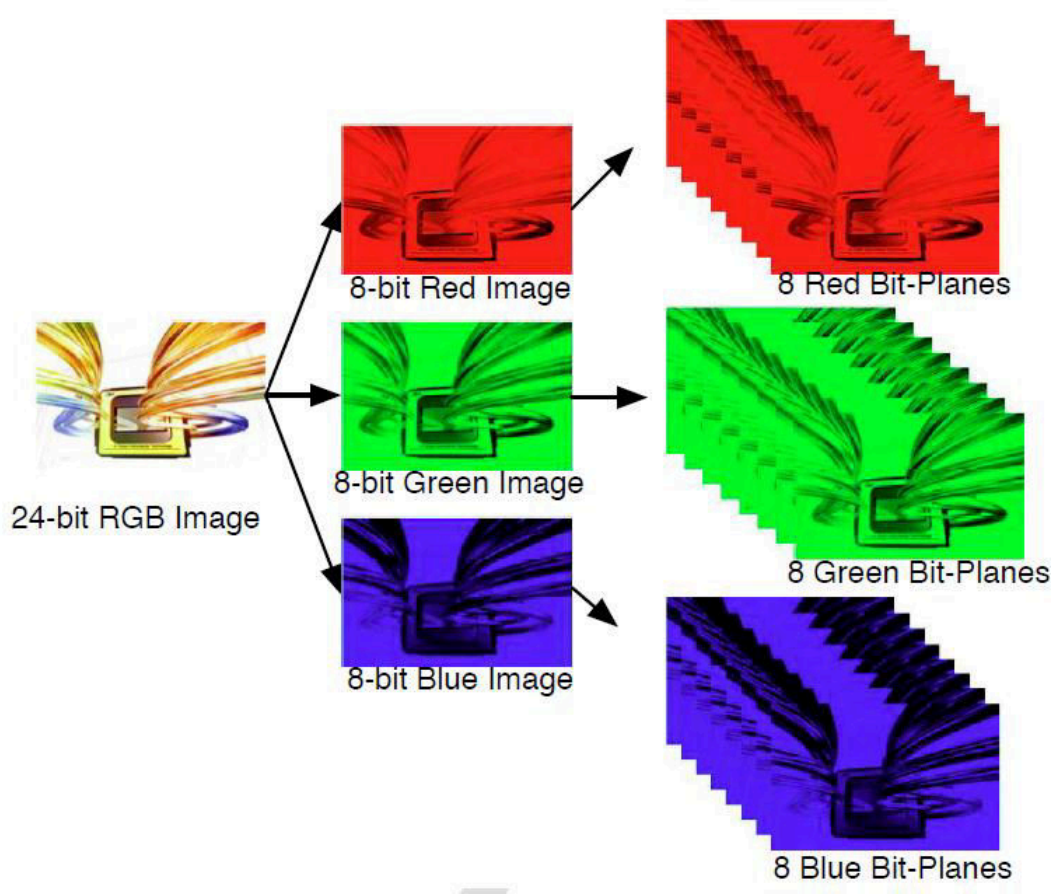


図 6-2. Bit Slices

The length of each bit-plane in the time slot is weighted by the corresponding power of two of its binary representations. This provides a binary pulse-width modulation of the image. For example, a 24-bit RGB input has three colors (R, G, and B) with 8-bit depth each. Each color time slot is then divided into eight bit-planes, with the sum of the weight of all bit planes in the time slot equal to 256. 図 6-3 illustrates the time partition of the bits in one 8-bit color time slot within a 24-bit RGB frame.

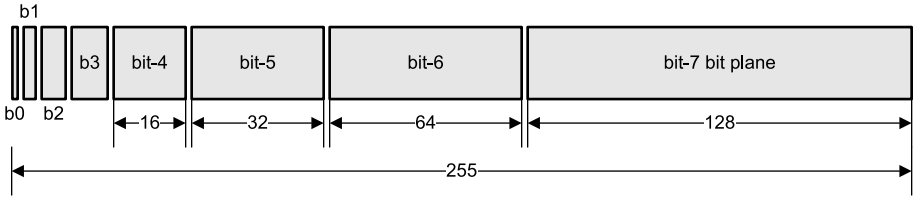


図 6-3. 24-Bit RGB Frame Bit Partition

Therefore, a single video frame is composed of a series of bit-planes. Because the DMD mirrors can be either on or off, an image is created by turning on the mirrors corresponding to the bit set in a bit-plane. With binary pulse-width modulation, the intensity level of the color is reproduced by controlling the amount of time the mirror is on. For a 24-bit RGB frame image inputted to the DLPC900 controller, the DLPC900 controller creates 24 bit-planes, stores them in internal embedded DRAM, and sends them to the DMD, one bit-plane at a time. The bit weight controls the amount of time the mirror is on. To improve image quality in video frames, these bit-planes, time slots, and color frames are shuffled and interleaved within the pixel processing functions of the DLPC900 controller.

6.3.1 DMD Configurations

図 6-4 shows the controller connections for full-bus default or swapped. Refer to the Firmware section of the *DLP® LightCrafter™ Single DLPC900 Evaluation Module (EVM) User's Guide* (DLPU101) or *DLP® LightCrafter ™ Dual DLPC900 Evaluation Module (EVM) User's Guide* (DLPU102) for details on how to select the bus swap settings to match the board layout connections.

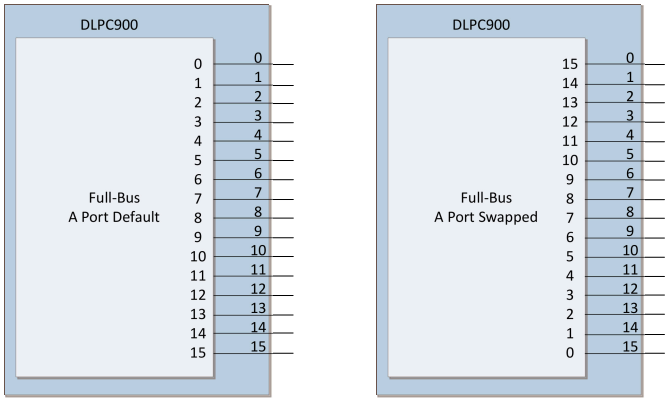


図 6-4. Controller to DMD Full-Bus Connections

6.3.2 Video Timing Input Blanking Specification

The DLPC900 controller requires a minimum horizontal and vertical blanking for both Port 1 and Port 2, as shown in セクション 5.16. These parameters indicate the time allocated to retrace the signal at the end of each line and field of a display. Refer to セクション 10.1.3.

6.3.3 Board-Level Test Support

The In-Circuit Tristate Enable signal (ICTSEN) is a board-level test control signal. By driving ICTSEN to a logic high state, all controller outputs (except TDO1 and TDO2) will be configured as tristate outputs.

The DLPC900 also provides JTAG boundary scan support on all I/O except non-digital I/O and a few special signals. 表 6-1 lists these exceptions.

表 6-1. DLPC900 – Signals Not Covered by JTAG (1)

SIGNAL NAME	PACKAGE BALL
HW_TEST_EN	M25
MOSC	M26
MOSCN	N26
USB_DAT_N	C5
USB_DAT_P	D6
TCK	N24
TDI	N25
TRSTZ	M23
TDO1	N23
TDO2	N22
TMS1	P25
TMS2	P26

(1) There is no JTAG connection to power or no-connect pins.

6.3.4 Two Controller Considerations

When two DLPC900 controllers drive a single DLP500YX, DLP670S, or DLP9000 DMD, each controller is used to drive half of the DMD, as shown in Two Controllers Connected to DLP9000 DMD. Each controller must operate in two pixels per clock, and the pixel clock must be maintained below the maximum two pixel per clock frequency. Only native resolution is supported when two DLPC900 controllers are matched with a DLP500YX, DLP670S, or DLP9000 DMD.

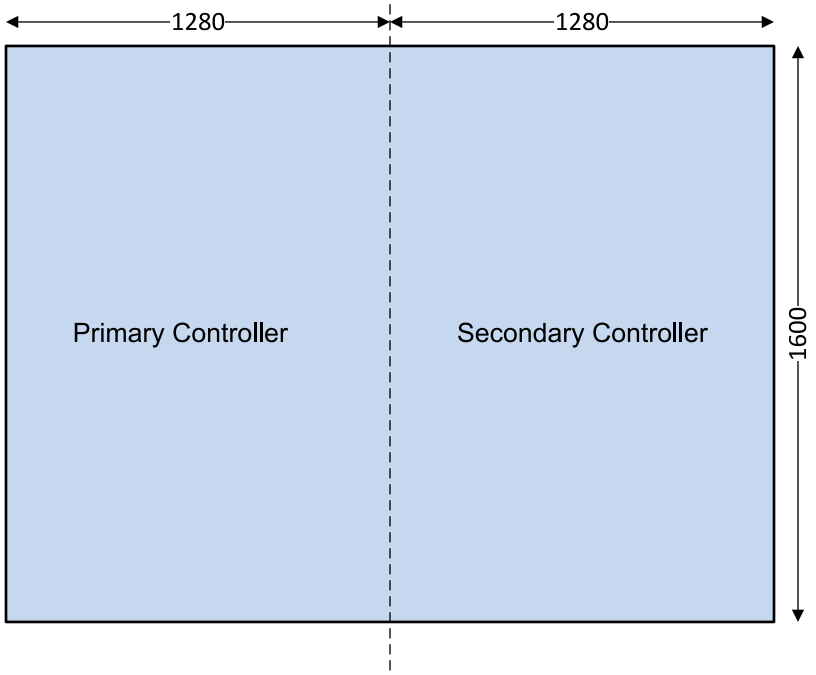


図 6-5. Two Controllers Connected to DLP9000 DMD

6.3.5 Memory Design Considerations

6.3.5.1 Flash Memory Optimization

The DLPC900 memory configuration can be optimized for different applications. The operating mode chosen and the application implementation will determine how much optimization can be performed.

6.3.5.2 Operating Modes

The DLPC900 firmware offers four operating modes which can be selected when designing a product for a particular application.

1. Video Mode: streamed over parallel RGB interface
2. Video Pattern Mode: streamed over parallel RGB interface
3. Pre-Stored Pattern Mode: patterns loaded from stored memory
4. Pattern On-The-Fly Mode: patterns loaded over USB or I^2C interface

Depending on the application design requirements, the memory required for each operating mode can be optimized for both performance and cost. This includes reducing the number of flash memory components, which reduces PCB size and lowers overall product cost. In addition, having fewer components reduces the power supply requirements hence lowering total power consumption.

6.3.5.3 DLPC900 External Memory Space

The external memory space of the DLPC900 consists of three chip-selects:

1. CS0
2. CS1—Power-up boot chip select
3. CS2

The DLPC900 is capable of accessing up to 16 megabytes of memory on each chip-select plus two optional GPIOs for extended external memory access (GPIO_45, GPIO_46). CS1 contains the firmware, and it is the power-up boot chip-select.

The memory space shown in 図 6-6 displays how the DLPC900 accesses the memory when memory is present on all three chip selects. Although the chip-selects are numbered 0, 1, and 2, the way the DLPC900 accesses the memory is not in this order. Note that the boot flash is located on chip select CS1.

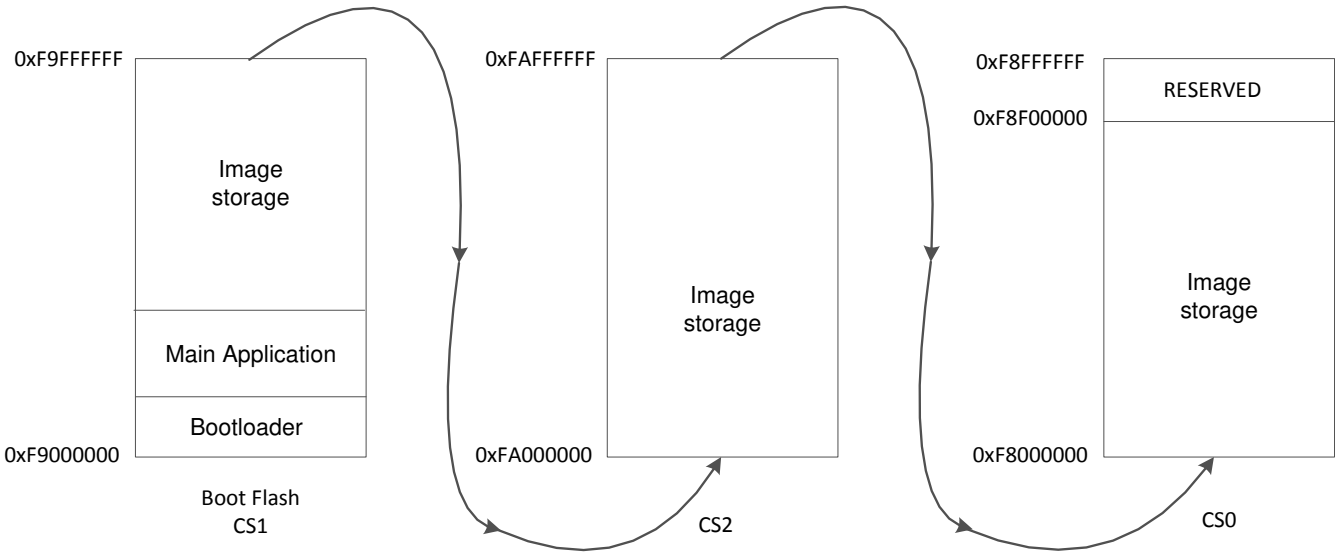


図 6-6. DLPC900 Memory Space

During the power-up initialization, the DLPC900 firmware performs a query on each chip-select to determine whether there is memory present. If there is no memory present on CS1, then the DLPC900 will not boot up; therefore, flash memory and the firmware must exist on CS1.

Note that the addresses from CS2 to CS0 are not ascending linearly in 図 6-6; therefore, an image cannot span across CS2 and CS0. If an image cannot entirely fit in CS2, then the entire image must be moved and stored in CS0.

If more memory space is required, the DLPC900 memory space can also be organized into a single flash memory device larger than 48 megabytes. By using the architecture shown in 図 6-7, a flash memory device up to 128 megabytes can be attached to the DLPC900. 表 6-2 describes the memory space layout of a 128-megabyte flash device. Similar to memories attached directly to chip selects, an image also cannot span across memory blocks when using a single large flash memory with the DLPC900.

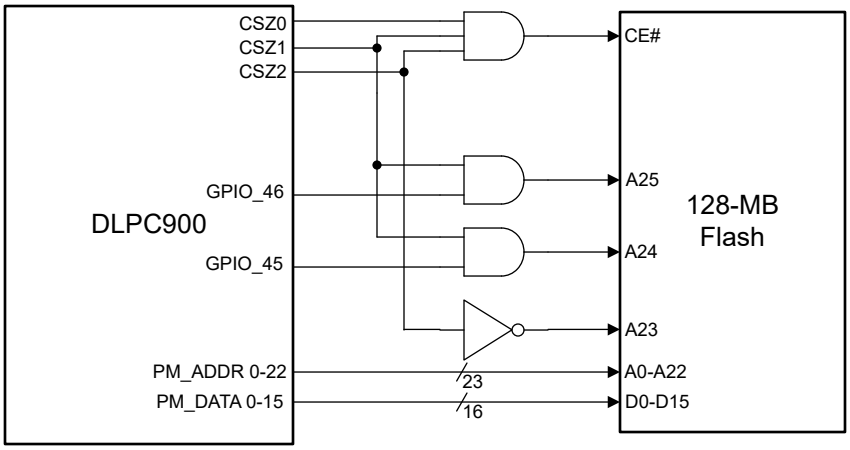


図 6-7. One 128-Megabyte Flash Device

表 6-2. Flash Device Layout

MEMORY BLOCK	ADDRESS SPACE (START AND END)	SINGLE FLASH MEMORY ADDRESSED	MEGABYTES	CONTENTS
0	0xF9000000 – 0xF901FFFF	0x00000000 – 0x0001FFFF	0 – 0.128	Bootloader
	0xF9020000 – 0xF913FFFF	0x00020000 – 0x0013FFFF	0.128 – 1.15	Application binary, Sequences / Patterns
	0xF9140000 – 0xF923FFFF	0x00140000 – 0x0023FFFF	1.15 – 2.15	Reserved space
	0xF9240000 – 0xF9FFFFFF	0x00240000 – 0x00FFFFFF	2.15 – 15	Patterns only
1	0xFA000000 – 0xFAFFFFFF	0x01000000 – 0x01FFFFFF	16 – 31	Patterns only
2	0xF8000000 – 0xF8FFFFFF	0x02000000 – 0x02FFFFFF	32 – 47	Patterns only
3	0x03000000 – 0x03FFFFFF	0x03000000 – 0x03FFFFFF	48 – 63	Patterns only
4	0x04000000 – 0x04FFFFFF	0x04000000 – 0x04FFFFFF	64 – 79	Patterns only
5	0x05000000 – 0x05FFFFFF	0x05000000 – 0x05FFFFFF	80 – 95	Patterns only
6	0x06000000 – 0x06FFFFFF	0x06000000 – 0x06FFFFFF	96 – 111	Patterns only
7	0x07000000 – 0x07FFFFFF	0x07000000 – 0x07FFFFFF	112 – 127	Patterns only

The design for a single 128-megabyte flash device for storing the firmware consists of the bootloader, the main application, sequences/images stored in flash (optional), and 1 megabyte of reserved space. The bootloader is located at the beginning of the flash memory block 0. The size of the bootloader is 128 kilobytes, beginning at address 0xF9000000. The bootloader is necessary for operation. If the bootloader becomes corrupted in some way it can render the device inoperable. The bootloader is followed by the main application and then sequence/image data. As mentioned above, **patterns must not span memory block boundaries**. If a pattern does not fit

in a given block, the entire 24-bit image (or composite image) must be moved in the next block. Additionally, the 1 megabyte of reserved space in memory block 0 from 0xF9140000 to 0xF923FFFF is necessary for operation and must not be overwritten.

6.3.5.4 Minimizing Memory Space

Depending on the application design requirements of the product, the amount of memory can be reduced. This can include reducing the number of flash memory components or the memory size of the flash memory component.

As depicted in 図 6-8, the firmware resides in CS1, and the amount of memory the firmware occupies is usually less than 128 kilobytes. With this in mind, the design engineer can conclude that memory is only required to be present on CS1 if no images are needed for the design.

For example, if the application design only requires the DLPC900 to operate in *Video Mode*, then the flash memory components on CS0 and CS2 are not required and can be left out. Moreover, since the firmware only occupies about 128 kilobytes of memory, then a smaller density flash memory component can be used such as a 4-megabyte rather than a 16-megabyte component. One 4-Megabyte Flash Memory shows the memory space for this example.

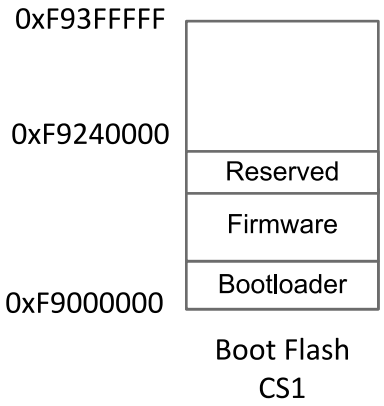


図 6-8. One 4-Megabyte Flash Memory

The same memory space shown in One 4-Megabyte Flash Memory also applies to *Video Pattern Mode*. In this mode, the images are streamed from an external video source directly in to the internal memory of the DLPC900. Another operating mode that can use this same memory configuration is *Pattern On-The-Fly Mode* because the images are streamed over the USB or I^2C interfaces directly into the internal memory of the DLPC900. These three operating modes are excellent opportunities for minimizing flash memory because they don't require images to be stored in flash memory.

However, there exists one mode that can require additional memory because this mode requires images to be stored in flash memory. When the DLPC900 is operating in *Pre-Stored Pattern Mode*, the DLPC900 reads all the required images from flash memory into its internal memory when the pattern sequence is started. The amount of flash memory depends on the needs of the application.

For example, if the application design requires only a few images, and the images and firmware can fit in one 4-megabyte flash component, then the memory space in One 4-Megabyte Flash Memory can be used. However, if more memory is needed, then one 8-megabyte or one 16-megabyte flash component can be used, as shown in One 8-Megabyte Flash Memory and One 16-Megabyte Flash Memory.

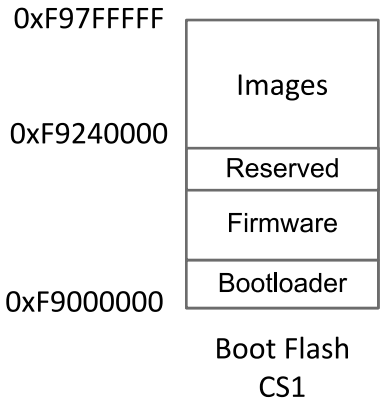


図 6-9. One 8-Megabyte Flash Memory

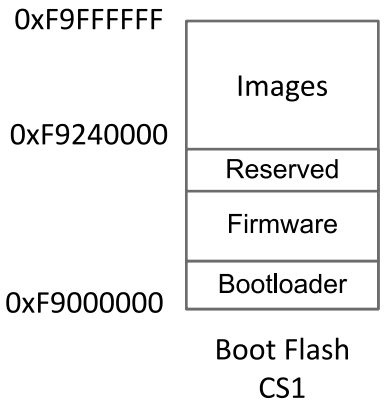


図 6-10. One 16-Megabyte Flash Memory

When the memory requirement is greater than 16 megabytes but less than 32 megabytes, then two 16-megabyte flash components can be used as shown in Two 16-Megabyte Flash Memory Components. Use CS1 and CS2 when using only two flash components.

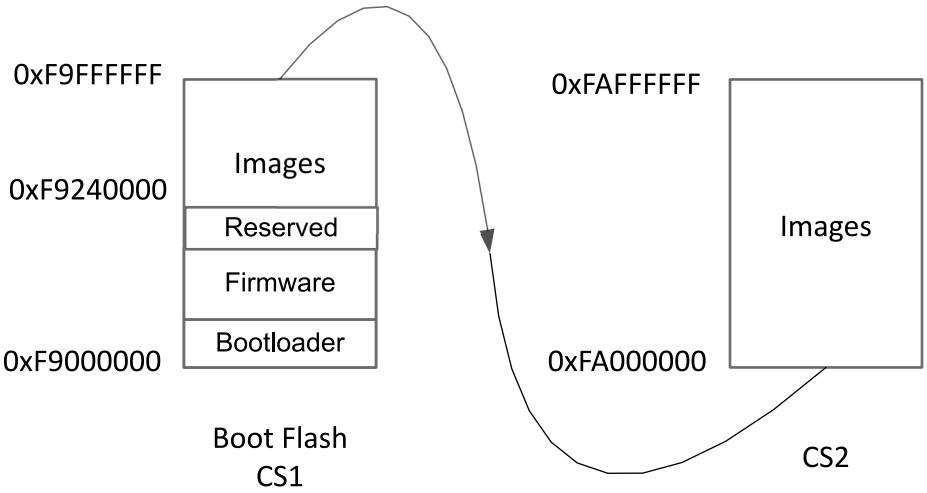


図 6-11. Two 16-Megabyte Flash Memory Components

When the memory requirement exceeds 32 megabytes, use the flash memory space shown in 図 6-11 or use a single large flash device as described in セクション 6.3.5.5.2. Notice that in all examples, there is a 1-megabyte

space reserved at the end of the Firmware space. The default and maximum size of this reserved space is 1 megabyte; however, depending on the operating mode, the reserved space is customizable and can be reduced by the design engineer when configuring the firmware. Whatever size is chosen, this reserved area must be taken into consideration when calculating the required amount of memory.

6.3.5.5 Minimizing Board Size

Reducing the number of flash components saves valuable board area and reduces the cost of the PCB. There are two additional ways to reduce cost: package selection and using larger density flash.

6.3.5.5.1 Package Selection

The first way is to use a smaller package type for the flash memory. Most of the flash memory components that can be used with the DLPC900 also come in alternate packages. For example, selecting a BGA package can be more than 50% smaller compared to a TSOP package.

6.3.5.5.2 Large Density Flash

The second way is to use a larger density flash memory component to combine two or all three flash memory components into one flash component. However, using this method requires some additional low cost external logic gates to combine the chip-selects and create and invert signals for the extra address lines. **The other requirement is the flash memory component must contain uniform sectors where each sector is 128-kilobytes in size.**

6.3.5.5.2.1 Combining Two Chip-Selects with One 32-Megabyte Flash

One use case is when the memory requirement for a design is greater than 16-megabytes but less than 32-megabytes. In this case, rather than using two 16-megabyte flash components, use only one 32-megabyte component. One 32-Megabyte Flash Component shows a block diagram describing how to combine CS1 and CS2 with external logic gates, as well as the connections between the DLPC900 and the flash component.

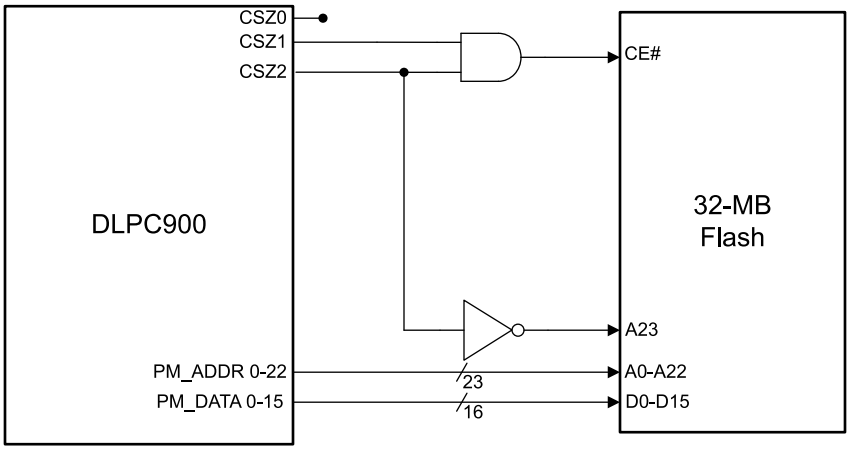


図 6-12. One 32-Megabyte Flash Component

6.3.5.5.2.2 Combining Three Chip-Selects with One 64-Megabyte Flash

Another use case is when the memory requirement exceeds 32 megabytes but is less than 64 megabytes. In this case, a single flash device up to 64 megabytes can be used. 図 6-13 shows a block diagram describing how to combine CS0, CS1, CS2, and GPIO_45 with external logic gates, as well as the connections between the DLPC900 and the flash component.

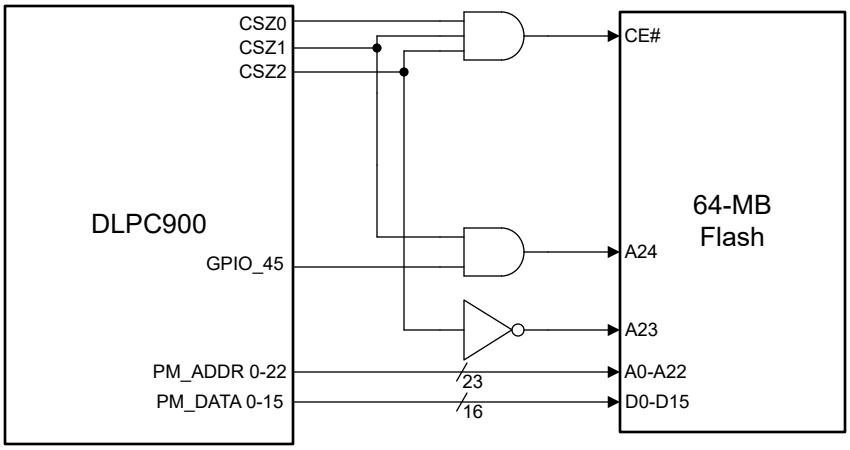


図 6-13. One 64-Megabyte Flash Component

6.3.5.5.2.3 Combining Three Chip-Selects with One 128-Megabyte Flash

The other use case is when the memory requirement exceeds 64 megabytes. In this case, a single flash device up to 128 megabytes can be used. 図 6-14 shows a block diagram describing how to combine CS0, CS1, CS2, GPIO_45, and GPIO_46 with the required external logic gates and the connections between the DLPC900 and the flash component.

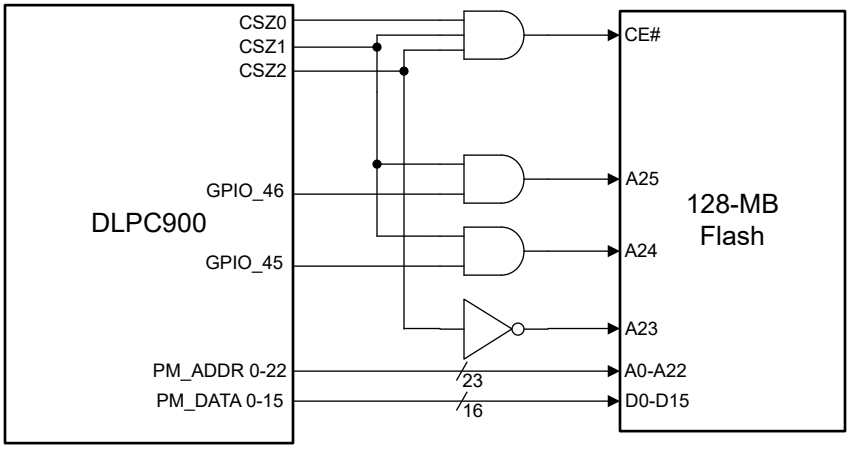


図 6-14. One 128-Megabyte Flash Component

注

Flash devices that are larger than 128 megabytes can also be used with the DLPC900, but the DLPC900 is only capable of accessing 128 megabytes. The other sectors within the flash device will go unused.

注

GPIO_45, GPIO_46, and GPIO_60 are exclusively used by the DLPC900 as extended flash address lines. These GPIO are not to be used for any other purpose.

6.3.5.6 Minimizing Board Space

図 6-15 shows how to minimize board space by selecting the next larger density of flash memory. For example, if two 4-megabyte flash components are needed, then selecting one 8-megabyte flash component can be considered. This will save board space because only one component takes up space on the board rather than two components.

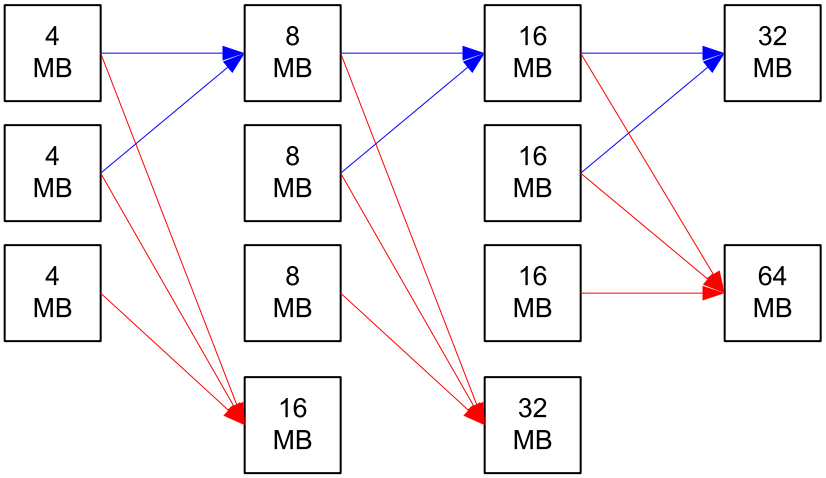


図 6-15. Selecting Next Larger Density for Board Space Savings

When calculating the appropriate amount of memory to use**, do not mix densities to come up with the exact amount of memory that is calculated**. Always use the same densities of flash memory even if it exceeds the amount of memory that is calculated.

6.3.5.7 Flash Memory

Flash changes will require a change to the flash parameters file. This file must be changed to match the flash device info for the selected device including the sector mapping of the device.

Refer to the appropriate BOM for a list of flash memory that was used and tested on the DLP®LightCrafter™ Single DLPC900 Evaluation Module and DLP®LightCrafter™ Dual DLPC900 Evaluation Module. The reader can also refer to the data sheets for alternate package types for each of the components listed. If substituting other flash memory, the user must consult the data sheets to ensure compatibility.

6.4 Device Functional Modes

6.4.1 Structured Light Application

For structured light applications, the DLPC900 can be commanded to enter the following high speed sequential pattern modes.

1. Video Pattern Mode
2. Pre-Stored Pattern Mode
3. Pattern On-The-Fly Mode

In each mode a specific set of patterns are selected with a maximum of 24 bits per pixel. The bit-depth of the patterns are then allocated into the corresponding time slots. Furthermore, an output trigger signal is also synchronized with these time slots to indicate when the image is displayed.

These pattern modes provide the capability to display a set of patterns and signal a camera to capture these patterns overlaid on an object. The DLPC900 controller is capable of preloading up to 480 1-bit binary patterns or 1024 1-bit binary patterns for the DLP5500 into internal memory from the external flash memory or from the USB or I^2C interfaces. These preloaded binary patterns are then streamed to the DMD at high speed.

注

When using Pre-Stored Pattern Mode, the number of patterns that can be stored in External Flash depends on the size of the external flash and level of compression achievable. The 1-bit pre-stored patterns for each DMD describe the controller memory, **not** flash memory.

表 6-3. Number of 1-Bit Pre-Stored Patterns for Each DMD

DMD	NUMBER OF PATTERNS
DLP5500	1024
DLP500YX	800
DLP6500	400
DLP670S	400
DLP9000	480

The DLPC900 controller is capable of synchronizing a camera to the displayed patterns. In video pattern mode, the vertical sync is used as trigger input. In pre-stored pattern mode and pattern on-the-fly mode, an internal user configurable trigger or a TRIG_IN_1 pulse indicates to the DLPC900 controller to advance to the next pattern, while TRIG_IN_2 starts and stops the pattern sequence. In all pattern modes, TRIG_OUT_1 frames the exposure time of the pattern, while TRIG_OUT_2 indicates the start of the pattern sequence.

図 6-16 shows an example timing diagram of video pattern mode. The VSYNC starts the pattern sequence display. The pattern sequence consists of a series of four patterns followed by a series of three patterns and then repeats. The first pattern sequence consists of P1, P2, P3, and P4. The second pattern sequence consists of P5, P6, and P7. TRIG_OUT_1 frames each pattern exposed, while TRIG_OUT_2 indicates the start of each pattern in the sequence. If the pattern sequence is configured without dark time between patterns, then the TRIG_OUT_1 output would be high for the entire pattern sequence.

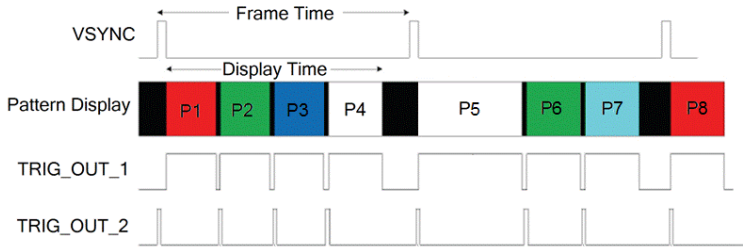


図 6-16. Video Pattern Mode Timing Diagram

図 6-17 shows an example of a pre-stored pattern mode timing diagram. Pattern sequences of four are displayed. TRIG_OUT_1 frames each pattern exposed, while TRIG_OUT_2 indicates the start of each pattern in the sequence. If the pattern sequence is configured without dark time between patterns, then the TRIG_OUT_1 output would be high for the entire pattern sequence.

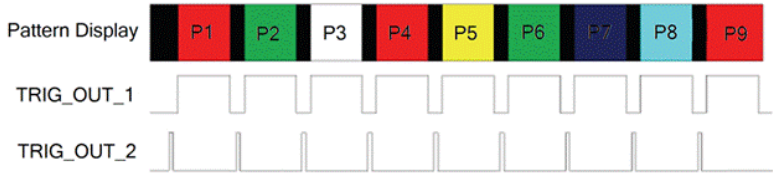


図 6-17. Pre-Stored Pattern Mode Timing Diagram

Another example of a pre-stored pattern mode timing diagram is shown in 図 6-18, where pattern sequences of three are displayed. TRIG_OUT_1 frames each pattern displayed, while TRIG_OUT_2 indicates the start of each pattern. TRIG_IN_2 serves as a start and stop signal. When high, the pattern sequence starts or continues. Note, in the middle of displaying the P4 pattern, TRIG_IN_2 is low, so the sequence stops displaying P4. When TRIG_IN_2 is raised, the pattern sequence continues where it stopped by re-displaying P4.

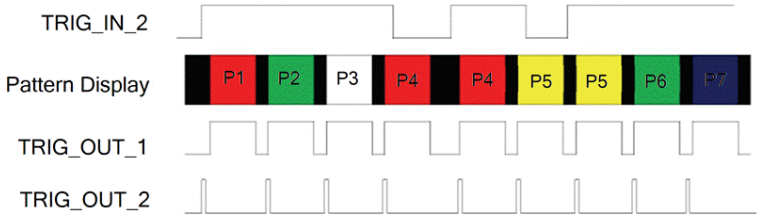


図 6-18. Pre-Stored Pattern Mode Timing Diagram for 3-Patterns

表 6-4 shows the allowed pattern combinations in relation to the bit depth of the pattern. If the pattern sequence is configured without dark time between patterns, then the TRIG_OUT_1 output would be high for the entire pattern sequence.

表 6-4. Minimum Pattern Time in Any Pattern Mode

BIT DEPTH	DLP5500 (µs)	DLP6500 (µs)	DLP9000 (µs)	DLP500YX (µs)	DLP670S (µs)
1	94	105	105	62	100
2	275	304	304	184	343
3	356	394	380	269	438
4	444	823	733	458	768
5	972	1215	1215	682	1299
6	1517	1487	1487	807	1488
7	1877	1998	1998	1083	2000
8	3753	4046	4046	2263	4046
10	NA	NA	NA	10363	NA
12	NA	NA	NA	41452	NA
14	NA	NA	NA	165807	NA
16	NA	NA	NA	663225	NA

For faster 8-bit pattern speeds, the illumination source can be modulated to shorten the smallest bits, and thus shorten the pattern speed. This method will introduce dark time into the pattern and affect the brightness, but it is capable of 8-bit pattern speeds up to four times faster than patterns without illumination modulation. More information on illumination modulation can be found in the *DLP® LightCrafter™ Single DLPC900 Evaluation Module (EVM) User's Guide* or *DLP® LightCrafter™ Dual DLPC900 Evaluation Module (EVM) User's Guide*. Examples of possible pattern speeds is shown in 表 6-5

表 6-5. Faster Pattern Speed Examples

BIT DEPTH	DLP5500 (µs)	DLP6500 (µs)	DLP9000 (µs)	DLP500YX (µs)	DLP670S (µs)
8 @ 500Hz	1950	1944	1944	1534	100
8 @ 750Hz	1283	1444	1444		343
8 @ 1000Hz(1)	916	969	944	1034	944
16 @ 4Hz	NA	NA	NA	255943	NA

(1) Minimum achievable exposure using smallest allowed Minimum LED Pulse Width

表 6-6 shows the minimum pattern time for a 1-bit pattern in relation to the number of active DMD blocks.

表 6-6. Minimum Exposures for Number of Active DMD Blocks

ACTIVE BLOCKS	DLP5500 (µs)	DLP6500 (µs)	DLP9000 (µs)	DLP670S (µs)	DLP500YX (µs)
1	25 (1)	24	24	27	30
2	30 (1)	45	42	27	30
3	35 (1)	45	42	27	30
4	28	45	42	33	30
5	33	48	45	38	34
6	38	54	51	44	38
7	43	60	56	49	42
8	48	66	61	55	46
9	53	72	67	61	50
10	58	78	72	66	54
11	63	84	77	72	58
12	68	90	83	77	62
13	73	96	88	83	-
14	78	101	93	89	
15	83	105	99	94	
16	94	-	105	100	

(1) To accommodate the 20µs trigger pulse and 5.2µs block reset time, minimum exposure times for active blocks 1, 2, and 3 are calculated differently than the following active blocks.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The DLPC900 controller is required to be coupled with the DLP500YX, DLP5500, DLP6500, DLP670S, or DLP9000 DMD to provide a reliable display solution for video display and structure light applications. The DLPC900 converts the digital input data into the digital format needed by the DLP500YX, DLP5500, DLP6500, DLP670S, or DLP9000 DMDs. The DMDs consist of an array of micromirrors which reflect incoming light to one of two directions by using binary pulse-width-modulation (PWM) for each micromirror, with the primary direction being into a projection or collection optics. Applications of interest include 3D machine vision, 3D printing, direct imaging lithography, and intelligent lighting.

7.2 Typical Applications

7.2.1 Typical Two Controller Chipset

A typical embedded system application using the DLPC900 controller and DLP9000, DLP500YX, or DLP670S DMD is shown in 図 7-1. This configuration requires two DLPC900 controllers to drive a DLP9000, DLP500YX, or DLP670S DMD and supports a 24-bit parallel RGB input, typical of LCD interfaces, from an external source or processor. In this configuration, the 24-bit parallel RGB input data is split between the primary and the secondary controller as described in セクション 6.3.4 using an FPGA or some other mechanism.

This system supports both still and motion video sources with the input resolution native to the DLP9000, DLP500YX, or DLP670S DMD. However, the controller supports only sources with periodic synchronization pulses. This support is ideal for motion video sources, but can also be used for still images by maintaining periodic syncs and sending a new frame of data only when needed. The still image must be fully contained within a single video frame and meet the frame timing constraints. The DLPC900 controller refreshes the displayed image at the source frame rate and repeats the last active frame for intervals in which no new frame has been received.

This configuration also supports the high-speed sequential pattern modes mentioned in the セクション 6.4.1. The patterns can be from the video source, from the USB or I^2C interface, or pre-stored in external flash, and have a maximum of 24 bits per pixel. The patterns are preloaded into the internal embedded DRAM and then streamed to the DLP9000, DLP500YX, or DLP670S DMD at high speeds.

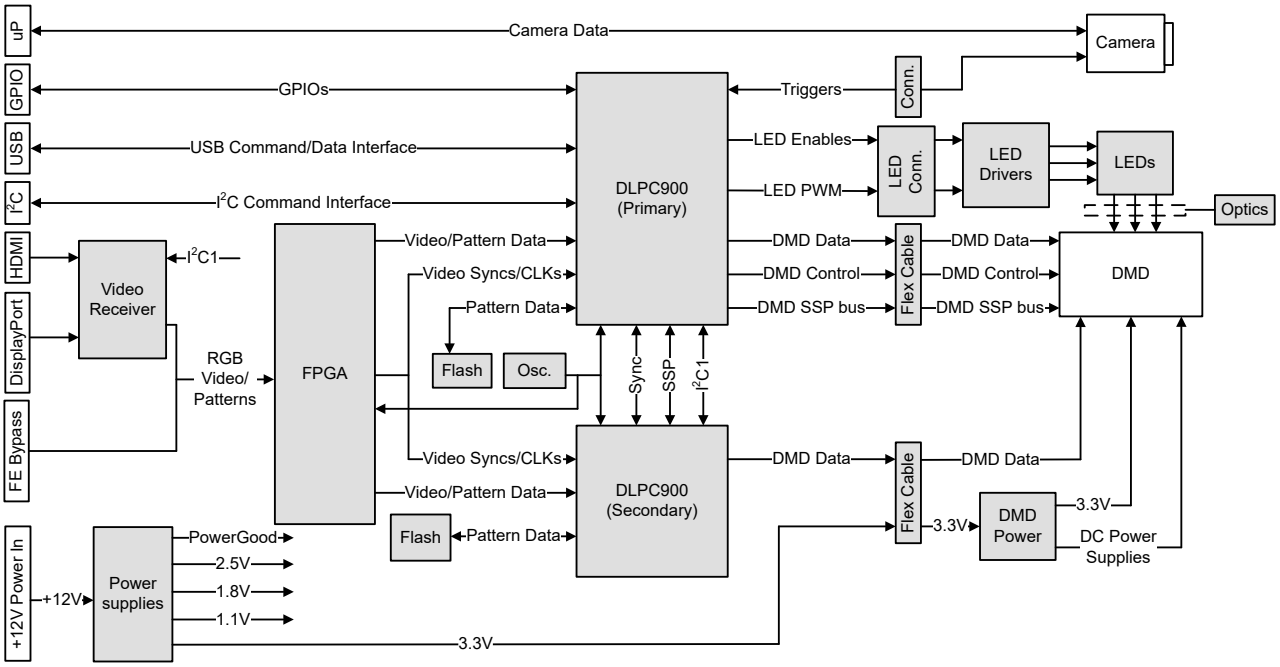


図 7-1. Typical Application Schematic for DLP9000, DLP500YX, or DLP670S

表 7-1. DLPC900 LVDS Channel (A/B) to DMD Data Bus Mapping (A, B, C, D)

DMD	DLPC900 Primary		DLPC900 Secondary	
	LVDS Channel A	LVDS Channel B	LVDS Channel A	LVDS Channel B
DLP5500	DMD Data Bus A	DMD Data Bus B	N/A	N/A
DLP6500	DMD Data Bus A	DMD Data Bus B	N/A	N/A
DLP500YX	DMD Data Bus C	DMD Data Bus D	DMD Data Bus A	DMD Data Bus B
DLP670S	DMD Data Bus C	DMD Data Bus D	DMD Data Bus A	DMD Data Bus B
DLP9000	DMD Data Bus C	DMD Data Bus D	DMD Data Bus A	DMD Data Bus B

注

DLPC900 has the capability to swap Data Bus A and B or Data Bus C and D. DLPC900 can also reverse the bit order to assist PCB layout. See 表 4-3 for further details.

7.2.1.1 Design Requirements

All applications require both the controller and DMD components for reliable operation. The system uses an external parallel flash memory device loaded with the DLPC900 configuration and support firmware. The external boot flash must contain a minimum of two sectors, where the first sector starts at address 0xF9000000 which is the power-up reset start address. The first 128 kilobytes is reserved for the bootloader image and must be in its own sector and can be made up of several smaller contiguous sectors that add up to 128 kilobytes as shown in 図 7-2. The remaining sectors contains the rest of the firmware. The default wait-states is set for a flash device of 120ns access time. For a faster flash access time, refer to the セクション 7.2.1.2.1.4.2 on how to program new wait-state values.

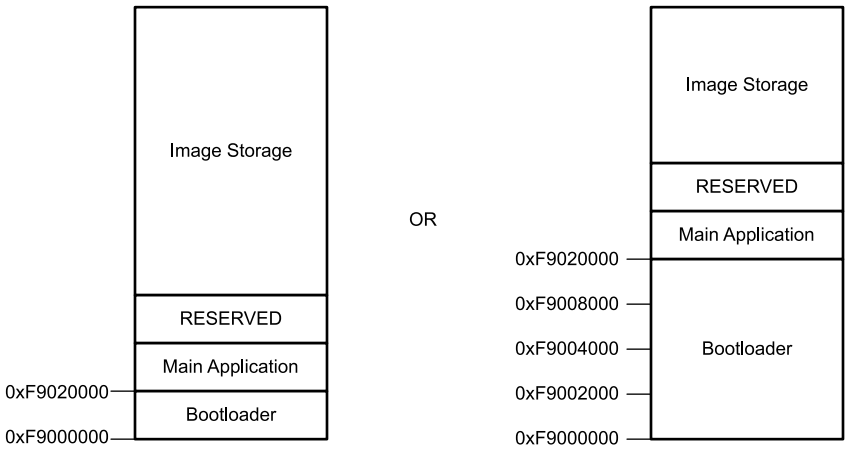


図 7-2. Boot Flash Memory Layout

注

The bootloader, the main application, and any images stored in flash (if present) are considered the firmware.

The chipset has the following interfaces and support circuitry:

- DLPC900 System Interfaces
  - Control Interfaces
  - Trigger Interface
  - Input Data Interfaces
  - Illumination Interface
- DLPC900 Support Circuitry and Interfaces
  - Reference Clock
  - PLL
  - Program Memory Flash Interface
- DMD Interface
  - DLPC900 to DLP6500/DLP9000/DLP500YX/DLP5500/DLP670S Digital Data
  - DLPC900 to DLP6500/DLP9000/DLP500YX/DLP5500/DLP670S Control and Clock Interface
  - DLPC900 to DLP6500/DLP9000/DLP500YX/DLP5500/DLP670S Serial Communication Interface
  - DLPC900 to DLP5500 and DLPA200 Interfaces

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 DLPC900 System Interfaces

The DLPC900 chipset supports a 24-bit parallel RGB interface for image data transfers from another device and a 24-bit interface for video data transfers. The system input requires proper generation of the PWRGOOD and POSENSE inputs to ensure reliable operation. There are two primary output interfaces: illumination driver control interface and sync outputs.

7.2.1.2.1.1 Control Interface

The DLPC900 chipset supports I^2C or USB commands through the control interface. The control interface allows another primary processor to send commands to the DLPC900 controller to query system status or perform real-time operations, such as, LED driver current settings. The DLPC900 allows the user to set a different I^2C slave address for the host port. Refer to the *DLPC900 Programmer's Guide* to set a different I^2C master and slave addresses.

表 7-2. Active Signals – I^2C Interfaces

SIGNAL NAME	DESCRIPTION
I2C2_SCL	I^2C clock. Bidirectional open-drain signal. I^2C master clock to external devices.
I2C2_SDA	I^2C data. Bidirectional open-drain signal. I^2C master to transfer data to external devices.
I2C1_SCL	I^2C clock. Bidirectional open-drain signal. I^2C master clock to external devices.
I2C1_SDA	I^2C data. Bidirectional open-drain signal. I^2C master to transfer data to external devices.
I2C0_SCL (1)	I^2C clock. Bidirectional open-drain signal. I^2C slave clock input from the external processor.
I2C0_SDA (1)	I^2C data. Bidirectional open-drain signal. I^2C slave to accept commands or transfer data to and from the external processor.

(1) This interface is the host port.

7.2.1.2.1.2 Input Data Interfaces

The data interface has a parallel RGB input port and has a nominal I/O voltage of 3.3V. Maximum and minimum input timing specifications for both components are provided in the Interface Timing Requirements. Each parallel RGB port can support up to 24 bits in Video Mode.

表 7-3. Active Signals – Data Interface

SIGNAL NAME	DESCRIPTION
RGB Parallel Interface Port 1	
P1_(A, B, C)_[0:9] (1)	24-bit data inputs, 8 bits for each of the red, green, and blue channels. When interfacing to a system with 8 bits per color or less, connect the bus of the red, green, and blue channels to the upper bits of the DLPC900 10-bit bus.
P_CLK1	Pixel clock. All input signals on data interface are synchronized with this clock.
P1_VSYNC	Vertical sync
P1_HSYNC	Horizontal sync
P_DATAEN1	Input data valid
RGB Parallel Interface Port 2	
P2_(A, B, C)_[0:9] (1)	24-bit data inputs, 8 bits for each of the red, green, and blue channels. When interfacing to a system with 8 bits per color or less, connect the bus of the red, green, and blue channels to the upper bits of the DLPC900 10-bit bus.
P_CLK2	Pixel clock. All input signals on data interface are synchronized with this clock.
P2_VSYNC	Vertical sync
P2_HSYNC	Horizontal sync
P_DATAEN2	Input data valid
Optional Pixel Clock 3	
P_CLK3	Pixel clock. All input signals on data interface are synchronized with this clock.

(1) The A, B, and C input data channels of Port 1 and 2 can be internally swapped for optimum board layout. Refer to the DLPC900 Programmers Guide for details on how to configuring the port settings to match the board layout connections.

7.2.1.2.1.3 DLPC900 System Output Interfaces

DLPC900 system output interfaces include the illumination interface as well as the trigger and sync interface.

7.2.1.2.1.3.1 Illumination Interface

An illumination interface is provided that supports up to a three (3) channel LED driver. The illumination interface provides signals that support: LED driver enable, LED enable, LED enable select, and PWM signals to control the LED current.

表 7-4. Active Signals - Illumination Interface

SIGNAL NAME	DESCRIPTION
HEARTBEAT	Signal toggles continuously to indicate system is running fine.
FAULT_STATUS	Signal toggles or held high indicating system faults
RED_LED_EN	Red LED enable
GRN_LED_EN	Green LED enable
BLU_LED_EN	Blue LED enable
RED_LED_PWM	Red LED PWM signal used to control the LED current
GRN_LED_PWM	Green LED PWM signal used to control the LED current
BLU_LED_PWM	Blue LED PWM signal used to control the LED current

7.2.1.2.1.3.2 Trigger and Sync Interface

The DLPC900 outputs a trigger signal for synchronizing displayed patterns with a camera, sensor, or other peripherals. The sync output supporting signals are: horizontal sync, vertical sync, two input triggers, and two output triggers. Depending on the application, these signals control how the pattern is displayed.

表 7-5. Active Signals - Trigger and Sync Interface

SIGNAL NAME	DESCRIPTION
P1_HSYNC	Horizontal Sync
P1_VSYNC	Vertical Sync
TRIG_IN_1	Depending on the mode, advances the pattern display.
TRIG_IN_2	Depending on the mode, starts or stops the pattern display.
TRIG_OUT_1	Active high during pattern exposure
TRIG_OUT_2	Active high pulse to indicate first pattern display

7.2.1.2.1.4 DLPC900 System Support Interfaces

7.2.1.2.1.4.1 Reference Clock and PLL

The DLPC900 controller requires a 20MHz 3.3V external input from an oscillator. This signal serves as the DLPC900 chipset reference clock from which the majority of the interfaces derive their timing. This includes DMD interfaces and serial interfaces.

Refer to セクション 9.1.2 on PLL guidelines.

7.2.1.2.1.4.2 Program Memory Flash Interface

The DLPC900 provides three external program memory chip selects for standard NOR-type flash plus two optional GPIOs for extended external memory access (GPIO_45, GPIO_46):

- PM_CSZ_0 – flash device (≤ 16 megabytes)
- PM_CSZ_1 – dedicated CS for boot flash device (≤ 16 megabytes). Refer to the 図 7-2 for the memory layout of the boot flash.
- PM_CSZ_2 – flash device (≤ 16 megabytes)

Flash access timing is programmable up to 19 wait-states. 表 7-6 contains the formulas to calculate the required wait-states for each of the parameters shown in 図 7-3 for a typical flash device. Refer to the DLPC900 Programmers Guide for details on how to set new wait-state values.

表 7-6. Flash Wait-States

PARAMETER	FORMULA (1)	DEFAULT
T_{CS} (CSZ low to WEZ low)	= Roundup((T_{CS}+ 5ns) / 6.7ns)	2
T_{WP} (WEZ low to WEZ high)	= Roundup((T_{WP}+ 5ns) / 6.7ns)	11
T_{CH} (WEZ high to CSZ high)	= Roundup((T_{CH}+ 5ns) / 6.7ns)	2
T_{ACC} (CSZ low to Output Valid) (2)	= Roundup((T_{ACC}+ 5ns) / 6.7ns)	19
Maximum supported wait-states	19 (120ns) (3)	

(1) Assumes a maximum single direction trace length of 75mm
(2) In some flash device data sheets, the read access time can also be represented as T_{OE}, T_E, T_{RC}, or T_{CE}. Use the largest of these values to calculate the wait-states for the read access time.
(3) For each parameter

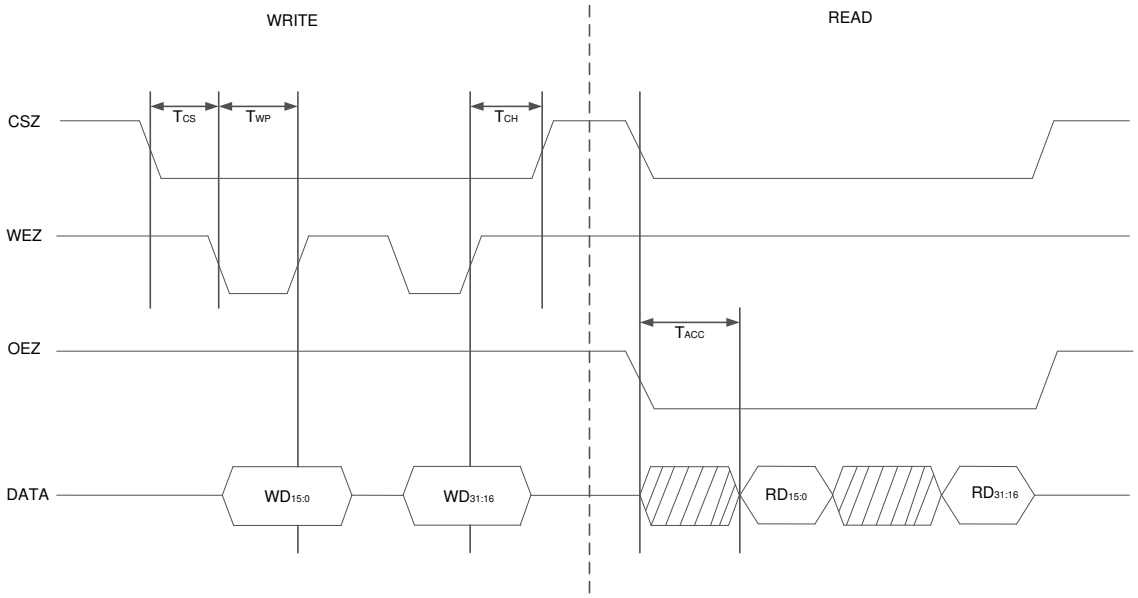


図 7-3. Flash Interface Timing Diagram

7.2.1.2.1.4.3 DMD Interface

The DLPC900 controller provides the pattern data to the DMD over a double data rate (DDR) interface. 表 7-7 describes the signals used for this interface.

表 7-7. Active Signals—DLPC900 to DMD Digital Data Interface

SIGNAL NAME	DESCRIPTION
DDA(15:0)	DMD, LVDS interface channel A, differential serial data
DDB(15:0)	DMD, LVDS interface channel B, differential serial data
DCKA	DMD, LVDS interface channel A, differential clock
DCKB	DMD, LVDS interface channel B, differential clock
SCA	DMD, LVDS interface channel A, differential serial control
SCB	DMD, LVDS interface channel B, differential serial control

The DLPC900 controls the micromirror clock pulses in a manner to ensure proper and reliable operation of the DMD.

表 7-8. Active Signals—DLPC900 to DMD Control Interface

SIGNAL NAME	DESCRIPTION
DADOEZ	DMD output-enable (active low)
DADADDR(3:0)	DMD address
DADMODE(1:0)	DMD mode
DADSEL(1:0)	DMD select
DADSTRB	DMD strobe
DAD_INTZ	DMD interrupt (active low). This signal requires an external 1KΩ pullup and uses hysteresis.

The DLPC900 controls the micromirror control interface signals in a manner to ensure proper and reliable operation of the DMD.

7.2.2 Typical Single Controller Chipset

A typical embedded system application using the DLPC900 controller and DLP6500 is shown in 図 7-4. This configuration uses one DLPC900 controller to operate with a DLP6500 or DLP5500 (with the DLPA200) and supports a 24-bit parallel RGB input, typical of LCD interfaces, from an external source or processor.

This system supports both still and motion video sources. However, the controller only supports sources with periodic synchronization pulses. This is ideal for motion video sources, but can also be used for still images by maintaining periodic syncs and only sending a new frame of data when needed. The still image must be fully contained within a single video frame and meet the frame timing constraints. The DLPC900 controller refreshes the displayed image at the source frame rate and repeats the last active frame for intervals in which no new frame has been received.

This configuration also supports the high speed sequential pattern modes mentioned in the セクション 6.4.1. The patterns can be from the video source, from the USB or I^{2}C interface, or pre-stored in external flash, and have a maximum of 24 bits per pixel. The patterns are preloaded into the internal embedded DRAM and then streamed to the DLP5500 or DLP6500 at high speeds.

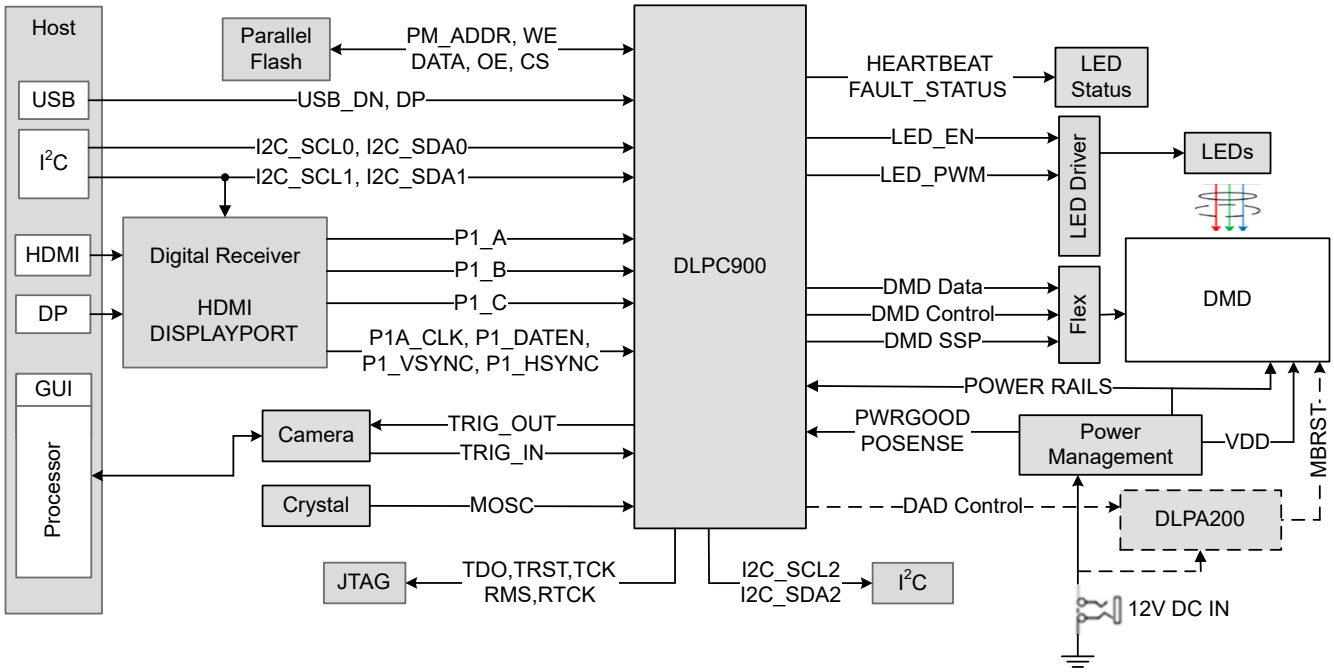


図 7-4. Typical Application Schematic for DLP5500 or DLP6500

8 Power Supply Recommendations

8.1 System Power Regulation

The PLLD_VAD, PLLM1_VAD, and PLLM2_VAD power feeding internal PLLs must be derived from an isolated linear regulator with filter as recommended in セクション 9.1.2 to minimize the AC noise component.

It is acceptable to derive PLLD_VDD, PLLM1_VDD, PLLM2_VDD, and PLLS_VAD from the same regulator as the core VDDC, but they must be filtered as recommended in the セクション 9.1.2.

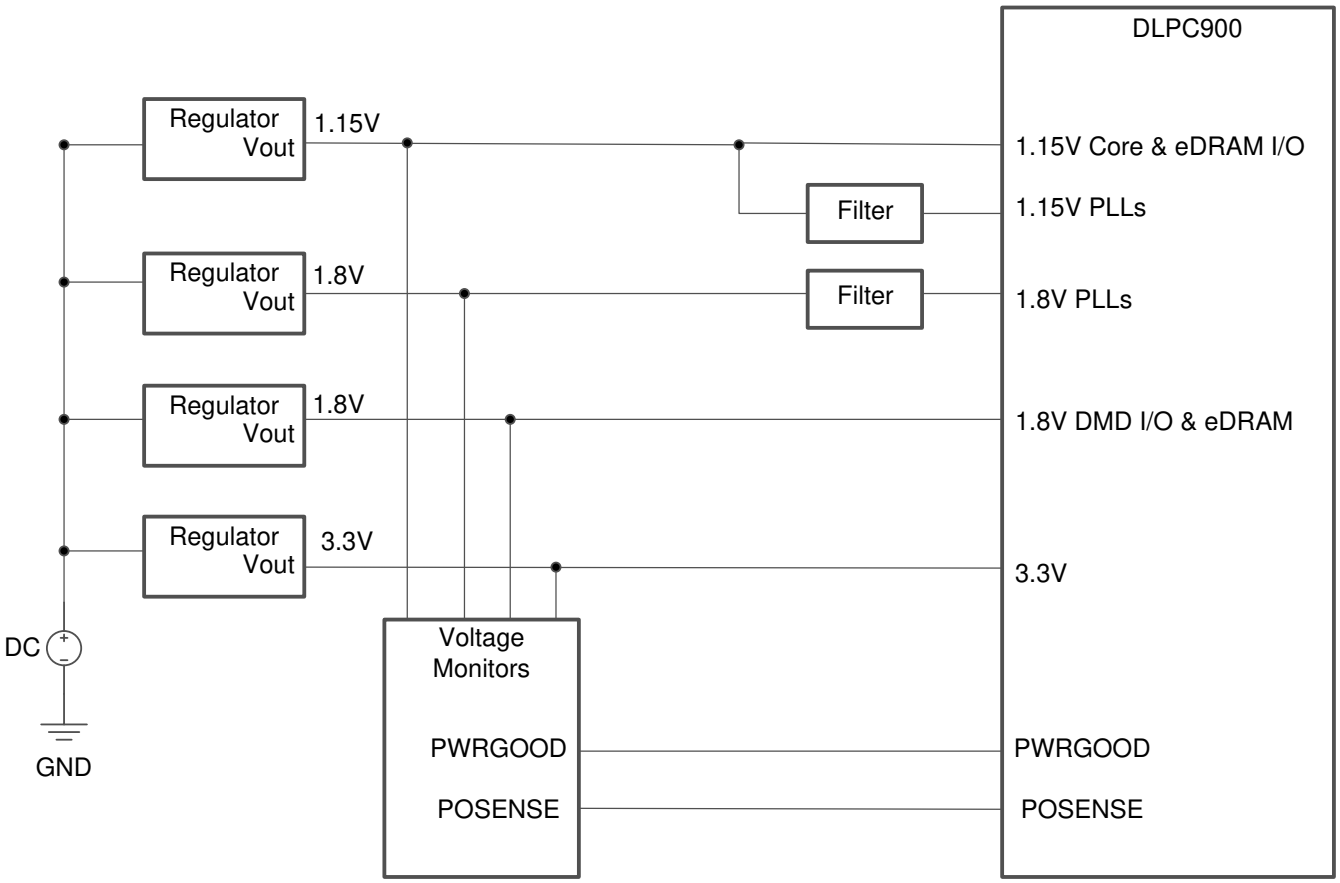


図 8-1. Power Regulation

8.1.1 Power Distribution System

8.1.1.1 1.15V System Power

The DLPC900 can support a low-cost power delivery system with a single 1.15V power source derived from a switching regulator. The main core can receive 1.15V power directly from the regulator output, and the internal DLPC900 PLLs (PLLD_VDD, PLLM1_VDD, PLLM2_VDD, and PLLS_VAD) must receive individually filtered versions of this 1.15V power. For specific filter recommendations, refer to the セクション 9.1.2.

8.1.1.2 1.8V System Power

The DLPC900 power delivery system provides two independent 1.8V power sources. One of the 1.8V power sources is used to supply 1.8V power to the DLPC900 LVDS I/O and internal DRAM. Power for these functions must always be fed from a common source, which is recommended as a linear regulator. The second 1.8V power source is used (along with appropriate filtering as discussed in the セクション 9.1.2) to supply all of the DLPC900 internal PLLs (PLLD_VAD, PLLM1_VAD, and PLLM2_VAD). To keep this power as clean as possible, a dedicated linear regulator is highly recommended for the 1.8V power to the PLLs.

8.1.1.3 3.3-V System Power

The DLPC900 can support a low-cost power delivery system with a single 3.3V power source derived from a switching regulator. This 3.3V power will supply all LVTTL I/O and the crystal oscillator cell. The 3.3V power must remain active in all power modes for which 1.15V core power is applied.

8.2 System Environment and Defaults

8.2.1 DLPC900 System Power-Up and Reset Default Conditions

Following system power-up, the DLPC900 performs a power-up initialization routine that defaults the controller to its normal operation power mode in which all blocks are powered, all processor clocks are enabled at their full rate, and associated resets are released. Most other clocks default to disabled with associated resets asserted until released by the processor. These same defaults are also applied as part of all system reset events that occur without removing or cycling power. The 1.8V power must be applied prior to releasing the reset so that the LVDS I/O and the internal embedded DRAM are enabled before the DLPC900 begins executing its system initialization routines.

8.3 System Power-Up Sequence

Although the DLPC900 requires an array of power supply voltages, for example, 1.15V, 1.8V, and 3.3V, there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the DLPC900, as long as the system is held in reset during power supply sequencing. This is true for both power-up (reset controlled by POSENSE) and power-down (reset controlled by PWRGOOD) scenarios. Similarly, there is no minimum time between powering-up or powering-down the different supplies feeding the DLPC900. However, power-sequencing requirements are common for the devices that share the supplies with the DLPC900.

Power-sequencing recommendations to ensure proper operation are:

- 1.15V core power must be applied whenever any I/O power is applied. This ensures the state of the associated I/O that are powered are set to a known state. Thus, applying core power first is recommended.
- All DLPC900 power must be applied before POSENSE is asserted to ensure proper power-up initialization is performed.

It is assumed that all DLPC900 power-up sequencing is handled by external hardware. It is also assumed that an external power monitor will hold the DLPC900 in system reset during power-up (that is, POSENSE = 0). During this time, all controller I/Os are tristated. The primary PLL (PLLM1) will be released from reset upon the low-to-high transition of POSENSE, but the DLPC900 will be kept in reset for an additional 60ms to allow the PLL to lock and stabilize its outputs. After this delay the DLPC900 internal resets will be deasserted, thus causing the processor to begin its boot-up routine.

図 8-2 shows the recommended DLPC900 system power-up sequence of the regulators:

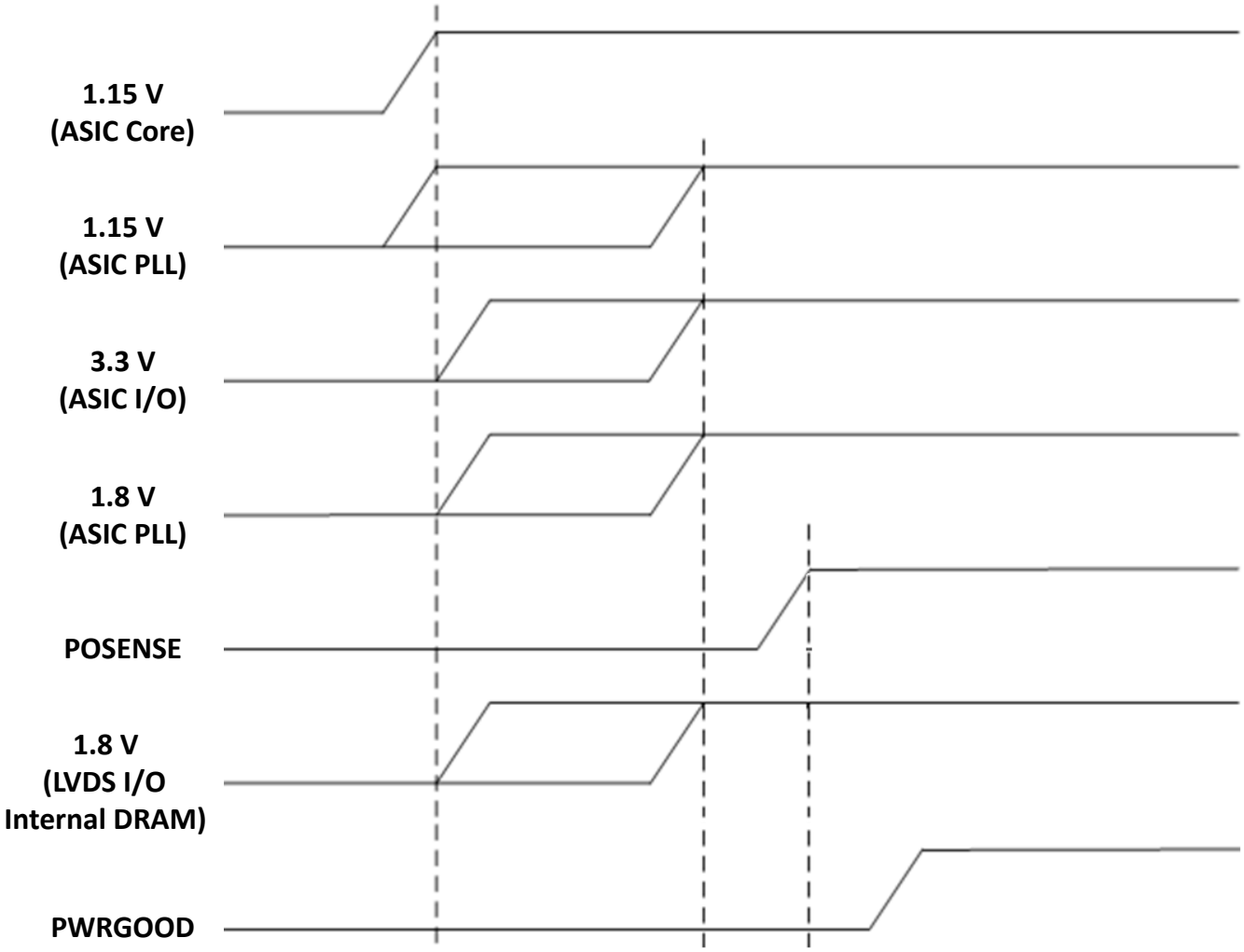


図 8-2. Power Sequencing

8.3.1 Power-On Sense (POSENSE) Support

It is difficult to set up a power monitor to trip exactly on the controller minimum supply voltage specification. Thus for practical reasons, the external power monitor generating POSENSE must target its threshold to 90% of the minimum supply voltage specifications and ensure that POSENSE remains low a sufficient amount of time for all supply voltages to reach minimum DLPC900 and DMD requirements and stabilize. The trip voltage for detecting the loss of power, as well as the reaction time to respond to a low voltage condition is critical for powering down the DMD. Refer to セクション 5.7 for details on powering up and powering down the DLPC900 and the DMD.

8.3.2 Power Good (PWRGOOD) Support

The PWRGOOD signal is defined as an early warning signal that alerts the DLPC900 of the DC supply voltages will drop below specifications. This warning lets the DLPC900 park the DMD mirrors and place the system into reset. For revision "B" DMDs and later, PWRGOOD can no longer be used as an early warning signal, and must follow the power-down requirements in セクション 5.7.

8.3.3 5V Tolerant Support

With the exception of USB_DAT, the DLPC900 does not support any other 5V tolerant I/O. However, I^2C typically have 5V requirements and special measures must be taken to support them. It is recommended that a 5V to 3.3V level shifter be used.

It is strongly recommended that a 0.5W external series resistance (of 22Ω) to limit the potential impact of a continuous short circuit between either USB D+ or USB D– to either V_{BUS}, GND, the other data line, or the cable. For additional protection, also add an optional 200mA Schottky diode from USB_DAT to VDD33.

8.4 System Reset Operation

8.4.1 Power-Up Reset Operation

Immediately after a power-up event, DLPC900 hardware will automatically bring up the primary PLL and place the controller in normal power mode. It will then follow the standard system reset procedure (see セクション 8.4.2).

8.4.2 System Reset Operation

Immediately after any type of system reset (power-up reset, PWRGOOD reset, watchdog timer time-out, and so forth), the DLPC900 automatically returns to normal power mode and returns to the following state:

- All GPIO will tristate.
- The primary PLL will remain active (it is only reset on a power-up reset) and most of the derived clocks will be active. However, only those resets associated with the DLPC900 processor and its peripherals will be released. (The DLPC900 firmware is responsible for releasing all other resets).
- The DLPC900 associated clocks will default to their full clock rates (boot-up is at full speed).
- The PLL feeding the LVDS DMD interface (PLLD) will default to its power-down mode and all derived clocks will be inactive with corresponding resets asserted. (The DLPC900 firmware is responsible for enabling these clocks and releasing associated resets).
- LVDS I/O will default to its power-down mode with tristated outputs.
- All resets output by the DLPC900 will remain asserted until released by the firmware (after boot-up).
- The DLPC900 processor will boot up from external flash.

Once the DLPC900 processor boots up, the DLPC900 firmware does the following:

- Configure the programmable DDR clock generator (DCG) clock rates (that is, the DMD LVDS interface rate)
- Enable the DCG PLL (PLLD) while holding divider logic in reset
- After the DCG PLL locks, the processor software will set DMD clock rates
- API software will then release DCG divider logic resets, which in turn, will enable all derived DCG clocks
- Release external resets

The LVDS I/O is reset by a system reset event and remains in reset until released by the DLPC900 firmware. Thus, the software is responsible for waiting until power is restored to these components before releasing reset.

9 Layout

9.1 Layout Guidelines

9.1.1 General PCB Recommendations

Two-ounce copper planes are recommended in the PCB design in order to achieve needed thermal connectivity.

9.1.2 PCB Layout Guidelines for Internal Controller PLL Power

The following are guidelines to achieve desired controller performance relative to internal PLLs:

The DLPC900 contains four PLLs (PLLM1, PLLM2, PLLD, and PLLS), each of which have a dedicated 1.15V digital supply; three of these PLLs (PLLM1, PLLM2, and PLLD) have a dedicated 1.8V analog supply. It is important to have filtering on the supply pins that covers a broad frequency range. Each 1.15V PLL supply pin must have individual high frequency filtering in the form of a ferrite bead and a 0.1µF ceramic capacitor. These components must be located very close to the individual PLL supply balls. The impedance of the ferrite bead should far exceed that of the capacitor at frequencies above 10MHz. The 1.15V to the PLL supply pins must also have low frequency filtering in the form of an RC filter. This filter can be common to all the PLLs. The voltage drop across the resistor is limited by the 1.15V regulator tolerance and the DLPC900 voltage tolerance. A resistance of 0.36Ω and a 100µF ceramic are recommended. 図 9-1 shows the recommended filter topology.

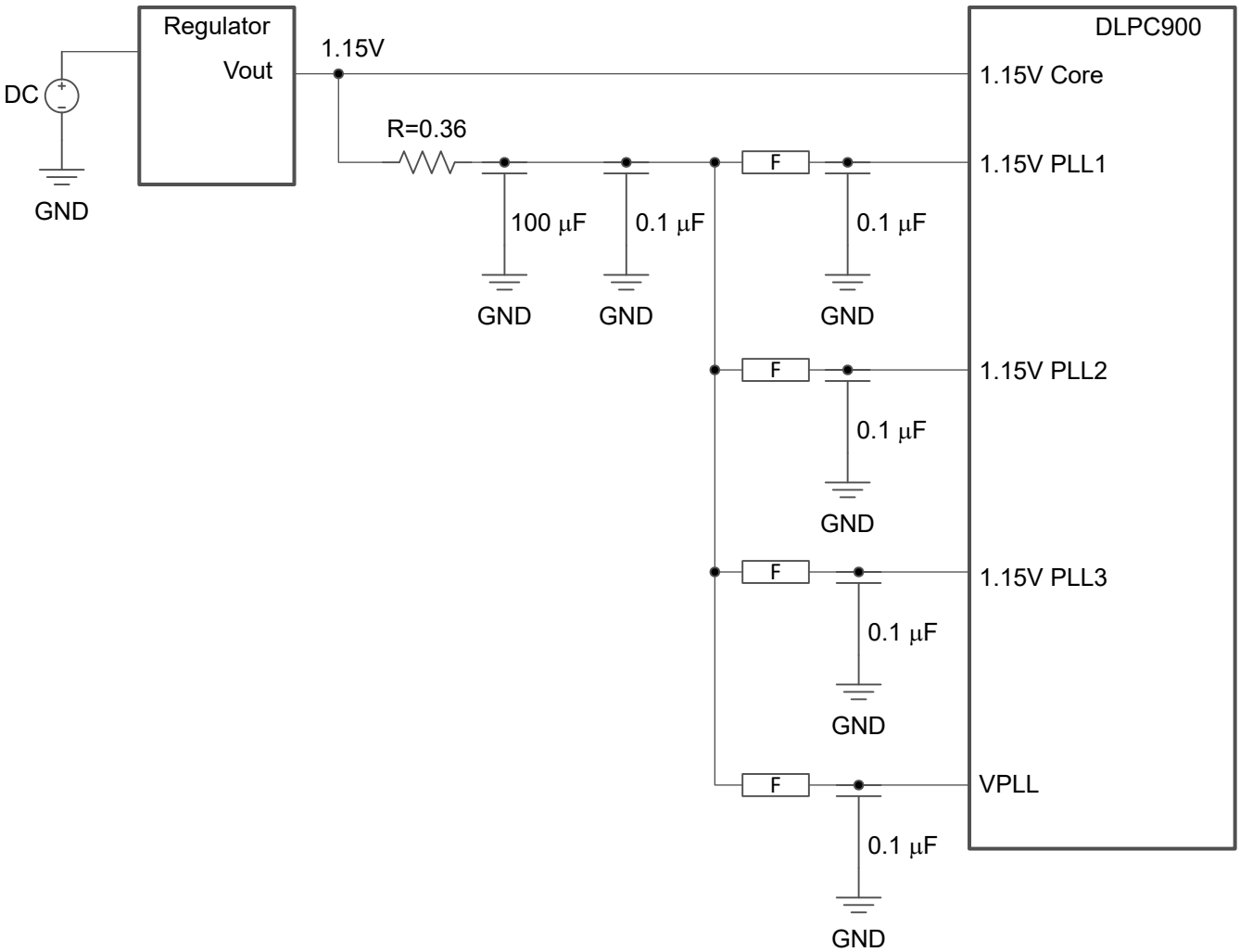


図 9-1. Recommended Filter Topology for PLL 1.15V Supplies

The analog 1.8V PLL power pins must have a similar filter topology as the 1.15V. In addition, it is recommended that a dedicated linear regulator generates the 1.8V. 図 9-2 shows the recommended filtering topology.

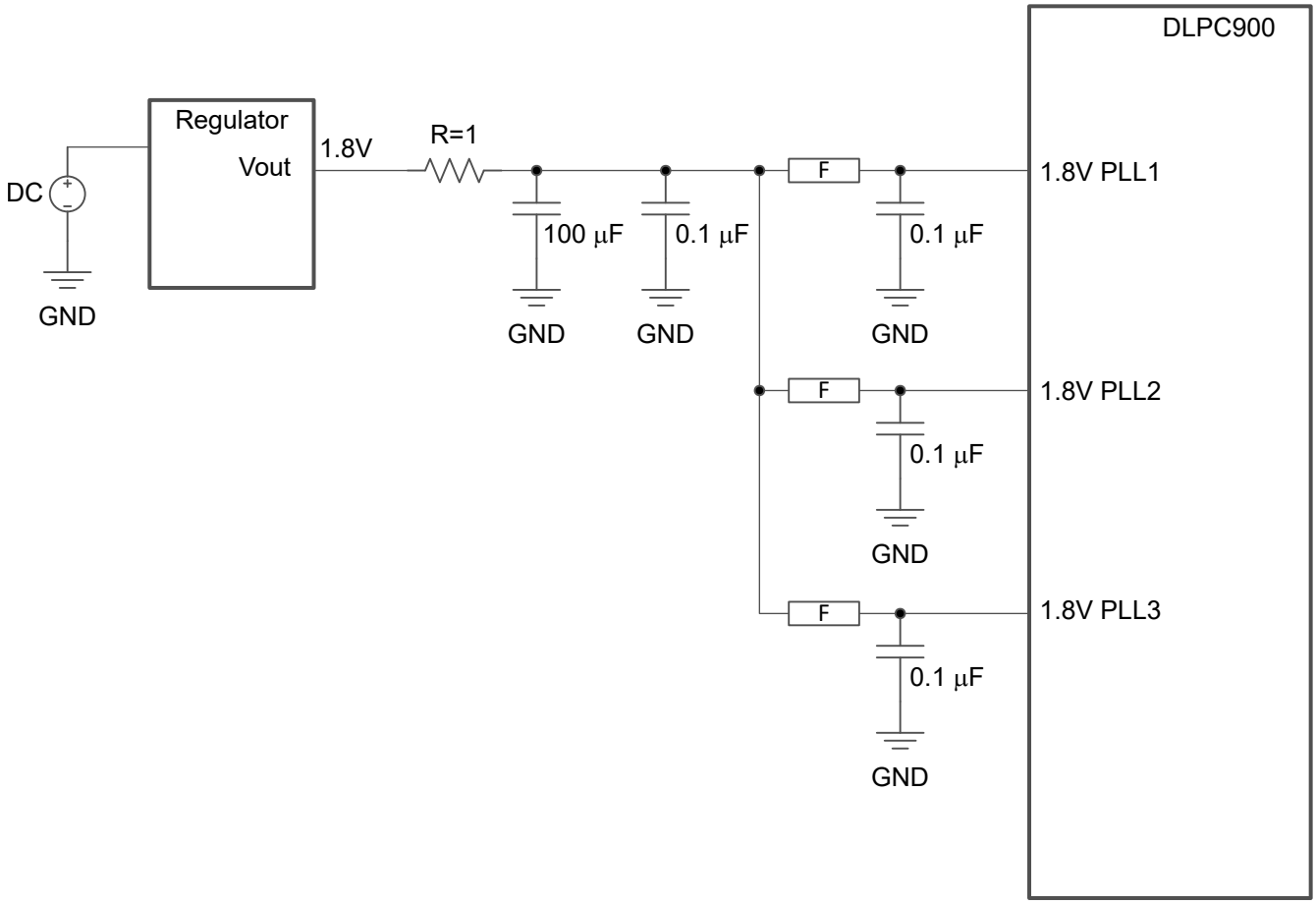


図 9-2. Recommended Filter Topology for PLL 1.8V Supplies

When designing the overall supply filter network, care must be taken to ensure no resonance occurs. Specific care is required around the 1MHz to 2MHz band, as this coincides with the PLL natural loop frequency.

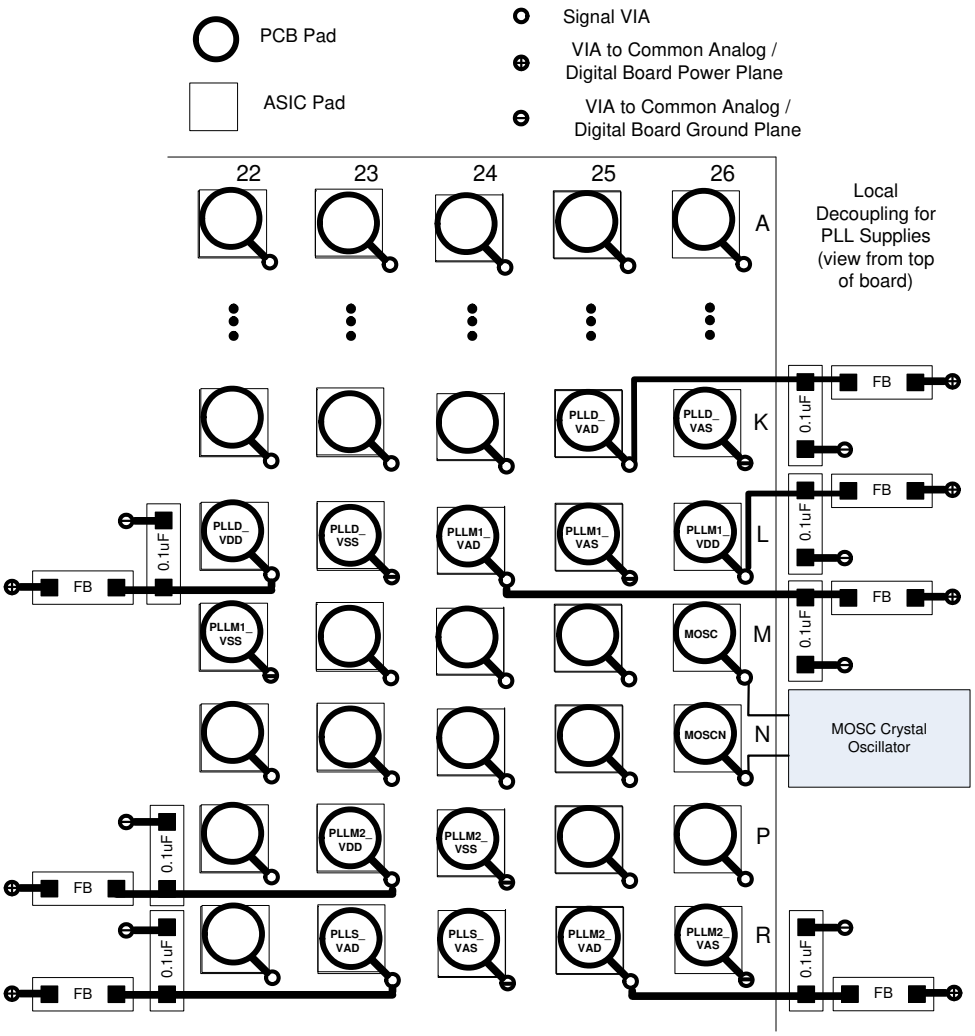


図 9-3. High Frequency Decoupling

High-frequency decoupling is required for 1.15V and 1.8V PLL supplies and must be provided as close as possible to each of the PLL supply package pins as shown in 図 9-3. Placing decoupling capacitors under the package on the opposite side of the board is recommended. High-quality, low-ESR, monolithic, surface-mount capacitors are recommended for use. Typically, 0.1µF for each PLL supply should be sufficient. The length of a connecting trace increases the parasitic inductance of the mounting, and thus, where possible, there can be no trace, allowing the via to butt up against the land. Additionally, the connecting trace must be made as wide as possible. Further improvement can be made by placing vias to the side of the capacitor lands or doubling the number of vias.

The location of bulk decoupling depends on the system design.

9.1.3 PCB Layout Guidelines for Quality Video Performance

One of the most important factors to gain good performance is designing the PCB with the highest quality signal integrity possible. Here are a few recommendations:

1. Minimize the trace lengths between the video digital receiver and the DLPC900 port inputs.
2. Analog power must not be shared with the digital power directly.
3. Try to keep the trace lengths of the RGB as equal as possible.
4. Impedance matching between the digital receiver and the DLPC900 is important.

9.1.4 Recommended MOSC Crystal Oscillator Configuration

図 9-4 shows a recommended crystal oscillator configuration.

It is assumed that the external crystal oscillator will stabilize within 50ms after stable power is applied.

表 9-1. Crystal Port Characteristics

PARAMETER	NOMINAL	UNIT
MOSC-to-GND capacitance	1.5	pF
MOSCZ-to-GND capacitance	1.5	pF

表 9-2. Recommended Crystal Configuration (1)

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	20	MHz
Crystal temperature stability	± 30	PPM
Crystal frequency tolerance (including accuracy, temperature, aging, and trim sensitivity)	± 100	PPM
Crystal equivalent series resistance (ESR)	50 max	Ω
Crystal load	20	pF
Crystal shunt load	7 max	pF
R_S drive resistor (nominal)	100	Ω
R_{FB} feedback resistor (nominal)	1	MΩ
C_{L1} external crystal load capacitor (MOSC)	See 式 1	pF
C_{L2} external crystal load capacitor (MOSCN)	See 式 2	pF
PCB layout	A ground isolation ring around the crystal is recommended	

(1) Typical drive level with the XSA020000FK1H-OCX crystal (ESR_{max} = 40Ω) = 50µW

$$C_{L1} = 2 \times (C_L - C_{Stray\text{-}MOSC}) \quad (1)$$

$$C_{L2} = 2 \times (C_L - C_{Stray\text{-}MOSCN} \quad (2)$$

(3)

where

- C_L = Crystal load capacitance (Farads)
- $C_{Stray\text{-}MOSC}$ = Sum of package and PCB capacitance at the crystal pin associated with controller signal MOSC.
- $C_{Stray\text{-}MOSCN}$ = Sum of package and PCB capacitance at the crystal pin associated with controller signal MOSCN.

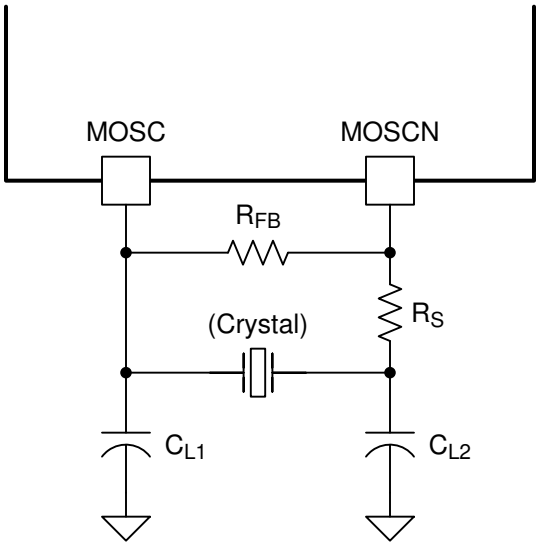


図 9-4. Crystal Oscillator Configuration

9.1.5 Spread Spectrum Clock Generator Support

DLPC900 supports limited, internally controlled, spread spectrum clock spreading on the DMD interface. The purpose is to frequency-spread all signals on this high-speed external interface to reduce EMI emissions. Clock spreading is limited to triangular waveforms. The DLPC900 provides modulation options of 0%, ±0.5%, and ±1.0% (center-spread modulation).

9.1.6 GPIO Interface

The DLPC900 provides nine software-programmable, general-purpose I/O pins. Each GPIO pin is individually configurable as either input or output. In addition, each GPIO output can be either configured as push-pull or open-drain. Some GPIO have one or more alternative use modes, which are also software configurable. The reset default for all GPIO is as an input signal. However, any alternative function connected to these GPIO pins, with the exception of general-purpose clocks and PWM generation, will be reset. When configured as open-drain, the outputs must be externally pulled up (to the 3.3V supply). External pullup or pulldown resistors can be required to ensure stable operation before software can configure these ports.

9.1.7 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, it is recommended tying unused controller input pins through a pullup resistor to its associated power supply or through a pulldown to ground unless noted in the Pin Functions. For controller inputs with an internal pullup or pulldown resistor, it is unnecessary to add an external pullup or pulldown unless specifically recommended. Internal pullup and pulldown resistors are weak and must not be expected to drive the external line.

Unused output-only pins can be left open.

When possible, it is recommended to configure unused bidirectional I/O pins to their output state such that the pin can be left open. If this control is not available and the pins become an input, then they must be pulled-up (or pulled-down) using an appropriate resistor unless noted in the Pin Functions.

9.1.8 DMD Interface Considerations

High-speed interface waveform quality and timing on the DLPC900 controller (that is, the LVDS DMD interface) is dependent on the following factors:

- Total length of the interconnect system
- Spacing between traces
- Characteristic impedance
- Etch losses
- How well matched the lengths are across the interface

Thus, ensuring positive timing margin requires attention to many factors.

As an example, DMD interface system timing margin can be calculated as follows:

Setup Margin = (controller output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation) (4)

Hold-time Margin = (controller output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation) (5)

The PCB SI degradation is the signal integrity degradation due to PCB affects which includes such things as simultaneously switching output (SSO) noise, crosstalk, and intersymbol interference (ISI) noise.

DLPC900 I/O timing parameters, as well as DMD I/O timing parameters, can be easily found in their corresponding data sheets. Similarly, PCB routing mismatch can be easily budgeted and met via controlled PCB routing. However, PCB SI degradation is not as easy-to-determine.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines provide a reference of an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Deviation from these recommendations can work, but must be confirmed with PCB signal integrity analysis or lab measurements.

PCB design: Refer to the 図 9-5.

Configuration:	Asymmetric dual stripline
Etch thickness (T):	1.0oz copper (1.2mil)
Flex etch thickness (T):	0.5oz copper (0.6mil)
Single-ended signal impedance:	50Ω (±10%)
Differential signal impedance:	100Ω (±10%)

PCB stackup: Refer to the 図 9-5.

Reference plane 1 is assumed to be a ground plane for proper return path.

Reference plane 2 is assumed to be the I/O power plane or ground.

Dielectric FR4, (Er):	4.2 (nominal)
Signal trace distance to reference plane 1 (H1):	5.0mil (nominal)
Signal trace distance to reference plane 2 (H2):	34.2mil (nominal)

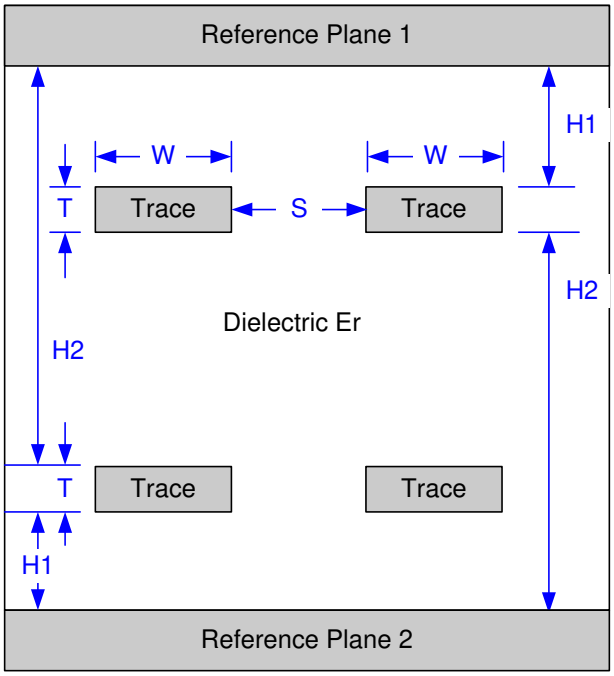


図 9-5. PCB Stackup Geometries

表 9-3. General PCB Routing (Applies to All Corresponding PCB Signals (Refer to 図 9-5.)

PARAMETER	APPLICATION	SINGLE-ENDED SIGNALS	DIFFERENTIAL PAIRS	UNIT
Line width (W)	Escape routing in ball field	4 (0.1)	4 (0.1)	mil (mm)
	PCB etch data or control	7 (0.18)	4.25 (0.11)	mil (mm)
	PCB etch clocks	7 (0.18)	4.25 (0.11)	mil (mm)
Differential signal pair spacing (S)	PCB etch data or control	N/A	5.75 (1) (0.15)	mil (mm)
	PCB etch clocks	N/A	5.75 (1) (0.15)	mil (mm)
Minimum differential pair-to-pair spacing (S)	PCB etch data or control	N/A	20 (0.51)	mil (mm)
	PCB etch clocks	N/A	20 (0.51)	mil (mm)
Minimum line spacing to other signals (S)	Escape routing in ball field	4 (0.1)	4 (0.1)	mil (mm)
	PCB etch data or control	10 (0.25)	20 (0.51)	mil (mm)
	PCB etch clocks	20 (0.51)	20 (0.51)	mil (mm)
Maximum differential pair P-to-N length mismatch	Total data	N/A	12 (0.3)	mil (mm)
	Total clock	N/A	12 (0.3)	mil (mm)

(1) Spacing can vary to maintain differential impedance requirements.

表 9-4. DMD Interface Specific PCB Routing

SIGNAL GROUP LENGTH MATCHING				
INTERFACE	**SIGNAL GROUP**	**REFERENCE SIGNAL**	**MAX MISMATCH**	**UNIT**
DMD (LVDS)	SCA_P/ SCA_N DDA_P_(15:0)/ DDA_N_(15:0)	DCKA_P/ DCKA_N	± 150 (± 3.81)	mil (mm)
DMD (LVDS)	SCB_P/ SCB_N DDB_P_(15:0)/ DDB_N_(15:0)	DCKB_P/ DCKB_N	± 150 (± 3.81)	mil (mm)

When routing the DMD Interface signals it is recommended to:

- Minimize the number of layer changes for single-ended signals.
- Individual differential pairs can be routed on different layers but the signals of a given pair must not change layers.

表 9-5. DMD Signal Routing Length(1)

BUS	MIN	MAX	UNIT
DMD (LVDS)	50	375	mm

(1) Max signal routing length includes escape routing.

Stubs: Avoid stubs.

Termination Requirements: DMD interface: None – The DMD receiver is differentially terminated to 100Ω internally.

Connector (DMD-LVDS interface bus only):

High-speed connectors that meet the following requirements can be used:

- Differential crosstalk: < 5%
- Differential impedance: 75Ω to 125Ω

Routing requirements for right-angle connectors: When using right-angle connectors, P-N pairs must be routed in the same row to minimize delay mismatch. When using right-angle connectors, propagation delay difference for each row must be accounted for on associated PCB etch lengths.

These guidelines will produce a maximum PCB routing mismatch of 4.41mm (0.174 inch) or approximately 30.4ps, assuming 175ps/inch FR4 propagation delay.

These PCB routing guidelines will result in approximately 25ps system setup margin and 25ps system hold margin for the DMD interface after accounting for signal integrity degradation as well as routing mismatch.

Both the DLPC900 output timing parameters and the DMD input timing parameters include timing budget to account for their respective internal package routing skew.

9.1.8.1 Flex Connector Plating

Plate all the pad area on top layer of flex connection with a minimum of 35 and maximum 50 micro-inches of electrolytic hard gold over a minimum of 100 micro-inches of electrolytic nickel.

9.1.9 PCB Design Standards

PCB designed and built in accordance with the following industry specifications:

表 9-6. Industry Design Specification

INDUSTRY SPECIFICATION	APPLICABLE TO
IPC-2221 and IPC2222, Type 3, Class X, at Level B producibility	Board Design
IPC-6011 and IPC-6012, Class 2	PWB Fabrication
IPC-SM-840, Class 3, Color Green	Finished PWB Solder mask
UL94V-0 Flammability Rating and Marking	Finished PWB
UL796 Rating and Marking	Finished PWB

9.1.10 Signal Layers

The PCB signal layers must follow typical good practice guidelines including:

- Layer changes must be minimized for single-ended signals.
- Individual differential pairs can be routed on different layers, but the signals of a given pair must not change layers.
- Stubs are to be avoided.
- Only voltage or low-frequency signals can be routed on the outer layers, except as noted previously in this document.
- Double data rate signals must be routed first.
- Pin swapping on components is not allowed.

The PCB must have a solder mask on the top and bottom layers. The mask must not cover the vias.

- Except for fine pitch devices (pitch ≤ 0.032 inches), the copper pads and the solder mask cutout are to be of the same size.
- Solder mask between pads of fine pitch devices must be removed.
- In the BGA package, the copper pads and the solder mask cutout must be of the same size.

9.1.11 Trace Widths and Minimum Spacing

BGA escape routing can be routed with 4mils width and 4mils spacing, as long as the escape nets are less than 1 inch long, to allow two traces to fit between vias. After signals escape the BGA field, trace widths can be widened to achieve the desired impedance and spacing.

All single-ended 50Ω signal must have a minimum spacing of 10-mils relative to other signals. Other special trace spacing requirements are listed in 表 9-7.

表 9-7. Traces Widths and Minimum Spacing

SIGNAL ON PIN	MINIMUM WIDTH	MINIMUM SPACE
VDDC, VDD18, VDD33	0.020	0.015
GND	0.015 (1)	0.005
PLLS_VAD, PLLM2_VDD, PLLD_VDD, PLLM1_VDD, PLLM1_VAD, PLLM2_VAD, PLLD_VAD	0.012 (keep length less than 260mils)	0.015
MOSCP, OCLKA		0.020 (2)
SCA_(P,N), DDA_(P,N)_(15:00), SCB_(P,N), DDB_(P,N)_(15:00), DCKA_(P,N), DCKB_(P,N)		0.030 (2)
USB_DAT_(P,N)		0.030 (2)

(1) Make width of GND trace as wide as the pin it is connected to, when possible.
(2) Trace spacing of these signals/signal-pairs relative to other signals.

9.1.12 Trace Impedance and Routing Priority

For the best performance, it is recommended that the trace impedance for differential signals as in 表 9-8.

All signals must be 50Ω controlled impedance unless otherwise noted in 表 9-8.

表 9-8. Trace Impedance

SIGNAL ON PIN	DIFFERENTIAL IMPEDANCE
DCKA_(P,N)	100Ω ±10%
SCA_(P,N)	
DDA_(P,N)_(15:00)	
DCKB_(P,N)	100Ω ±10%
SCB_(P,N)	
DDB_(P,N)_(15:00)	
USB_DAT_(P,N)	90Ω ±10%
USB_(P,N)	
All other Differential Signals	100Ω ±10%

表 9-9 lists the signals' routing priority assignment.

表 9-9. Routing Priority

SIGNAL ON PIN	PRIORITY
DCKA_(P,N) SCA_(P,N) DDA_(P,N)_(15:00) DCKB_(P,N) SCB_(P,N) DDB_(P,N)_(15:00)	1(1) (2) (3)
USB_(P,N) USB_DAT_(P,N)	2(1)
P1(A,B,C)(9:2), P2(A,B,C)(9:2), P_CLK1, P_CLK2, P_CLK3, P_DATEN1, P_DATEN2, P1_VSYNC, P2_VSYNC, P1_HSYNC, P2_HSYNC	3(1) (2) (3)
OCLKA, MOSCP	4(4)

(1) Refer to Trace Impedance for length matching requirement.
(2) Switching layers must not be done except at the beginning and end of the trace.
(3) Maximum routing length of 2 inches for each signal/pair, includes escape routing.
(4) Keep routing length under 0.35 inches.

9.1.13 Power and Ground Planes

For best performance, the following are recommended:

- Solid ground planes between each signal routing layer
- Two solid power planes for voltages
- Power and ground pins must be connected to these planes through a via for each pin.
- All device pin and via connections to these planes must use a thermal relief with a minimum of four spokes.
- Trace lengths for the component power and ground pins must be minimized to 0.03 inches or less.
- Vias should be spaced out to avoid forming slots on the power planes.
- High-speed signals must not cross over a slot in the adjacent power planes.
- Vias connecting all the digital layers are recommended for placement around the edge of the rigid PCB regions 0.03 inches from the board edges with 0.1-inch spacing prior to routing.
- Placing extra vias is not required if there are sufficient ground vias due to standard ground connections of devices.
- All signal routing and signal vias must be inside the perimeter ring of ground vias.

9.1.14 Power Vias

Power and Ground pins of each component must be connected to the power and ground planes with a via for each pin. Avoid sharing vias to the power plane among multiple power pins, where possible. Trace lengths for component power and ground pins must be minimized (ideally, less than 0.100"). Unused or spare device pins

that are connected to power or ground can be connected together with a single via to power or ground. The minimum spacing between vias shall be 0.050” to prevent slots from being developed on the ground plane.

9.1.15 Decoupling

Decoupling capacitors must be located as near as possible to the DLPC900 voltage supply pins. Capacitors must not share vias. The DLPC900 power pins can be connected directly to the decoupling capacitor (no via) if the trace is less than 0.03”. Otherwise the component must be tied to the voltage or ground plane through a separate via. All capacitors must be connected to the power planes with trace lengths less than 0.05”. Mount decoupling capacitors connecting to power rail VDDC (1.15V) using “via on sides” geometry as shown below in 図 9-6. If “2 via on sides” is not possible, 1.15V decoupling capacitors can be mounted using “via at ends” method, providing traces between the vias and decoupling capacitors’ pads be as short and wide (at least 15mils wide) as possible.

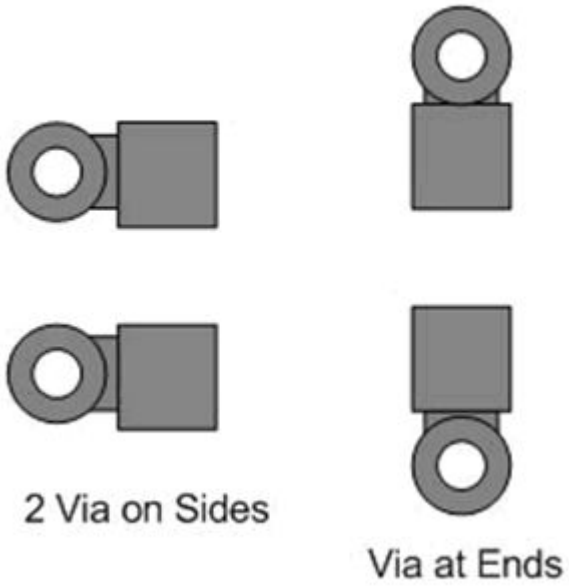


図 9-6. Decoupling Via Placement

9.1.16 Fiducials

Fiducials for automatic component insertion are placed on the board according to the following guidelines or on recommendation from manufacturer:

- Fiducials for optical auto insertion alignment shall be placed on three corners of both sides of the PCB.
- Fiducials shall be 0.050” copper with 0.100” cutout (antipad).

9.2 Layout Example

The DLP® LightCrafter™ Dual DLPC900 Evaluation Module (EVM) PCB is targeted at 14 layers with layer stack up shown in 図 9-7. The PCB layer stack can vary depending on the system design. However, careful attention is required to meet design considerations. Layers 1 and 14 consist of the component layers. Layers 2, 4, 6, 9, 11, and 13 consist of solid ground planes. Layers 7 and 8 consist of solid power planes. Layers 1, 3, 5, 10, 12, and 14 are used as the primary routing layers. Routing on external layers must be less than 0.25 inches for priority one and two signals. Refer to the 表 9-9 for signal priority groups. Board material must be FR-370HR or similar. PCB must be designed for lead-free assembly with the stack-up geometry shown in 図 9-7 and 図 9-8.

Layer	Calc Thickness	Primary Stack	Description
	0.0005		Taiyo 4000-BN
Layer - 1	0.0020		**1/2oz Sig (Std Plt)**
	0.0046	2116	370H
Layer - 2	0.0006		**1/2oz P/G**
	0.0060	0.0060 (1-1652)	370H
Layer - 3	0.0006		**1/2oz Sig**
	0.0074	2113 2113	370H
Layer - 4	0.0006		**1/2oz P/G**
	0.0060	0.0060 (1-1652)	370H
Layer - 5	0.0006		**1/2oz Sig**
	0.0074	2113 2113	370H
Layer - 6	0.0006		**1/2oz P/G**
	0.0021	0.0020 (1-106)	370H
Layer - 7	0.0006		**1/2oz P/G**
	0.0115	2113 2113 2113	370H
Layer - 8	0.0006		**1/2oz P/G**
	0.0021	0.0020 (1-106)	370H
Layer - 9	0.0006		**1/2oz P/G**
	0.0074	2113 2113	370H
Layer - 10	0.0006		**1/2oz Sig**
	0.0060	0.0060 (1-1652)	370H
Layer - 11	0.0006		**1/2oz P/G**
	0.0074	2113 2113	370H
Layer - 12	0.0006		**1/2oz Sig**
	0.0060	0.0060 (1-1652)	370H
Layer - 13	0.0006		**1/2oz P/G**
	0.0046	2116	370H
Layer - 14	0.0020		**1/2oz Sig (Std Plt)**
	0.0005		Taiyo 4000-BN

Materials: Isola 370H High-Tg FR4

Requirement	Req. Thickness	Tol +	Tol -	Calc Thick
Incl. Plating & Mask	0.0900	0.0090	0.0090	0.0907
Incl. Mask over Laminate	0.0860	0.0086	0.0086	0.0867
Incl. Plating	0.0890	0.0089	0.0089	0.0897
After Lamination	0.0862	0.0043	0.0043	0.0869
Over Laminate	0.0850	0.0085	0.0085	0.0857

図 9-7. Board Layer Stack

	Impedance Type	Layer	Design	Actual	Pitch	Plane	Target	Tol (ohms)	Predict
1	Surface MS	L1	-	0.0068	-	-	50	5.0	50.20
		-	-	-	-	L2			
2	EC Microstrip	L1	-	0.0055	0.0110	-	90	9.0	89.55
		-	-	0.0055	-	L2			
3	EC Microstrip	L1	0.00475	0.00475	0.0120	-	100	10.0	100.27
		-	0.00475	0.00475	-	L2			
4	Stripline	L3	-	0.0057	-	L2	50	5.0	49.34
		-	-	-	-	L4			
5	EC Stripline	L3	-	0.0054	0.0110	L2	90	9.0	89.75
		-	-	0.0054	-	L4			
6	EC Stripline	L3	0.00475	0.00475	0.0120	L2	100	10.0	99.03
		-	0.00475	0.00475	-	L4			
7	Stripline	L5	-	0.0057	-	L4	50	5.0	49.34
		-	-	-	-	L6			
8	EC Stripline	L5	-	0.0054	0.0110	L4	90	9.0	89.75
		-	-	0.0054	-	L6			
9	EC Stripline	L5	0.00475	0.00475	0.0120	L4	100	10.0	99.03
		-	0.00475	0.00475	-	L6			
10	Stripline	L10	-	0.0057	-	L9	50	5.0	49.34
		-	-	-	-	L11			
11	EC Stripline	L10	-	0.0054	0.0110	L9	90	9.0	89.75
		-	-	0.0054	-	L11			
12	EC Stripline	L10	0.00475	0.00475	0.0120	L9	100	10.0	99.03
		-	0.00475	0.00475	-	L11			
13	Stripline	L12	-	0.0057	-	L11	50	5.0	49.34
		-	-	-	-	L13			
14	EC Stripline	L12	-	0.0054	0.0110	L11	90	9.0	89.75
		-	-	0.0054	-	L13			
15	EC Stripline	L12	0.00475	0.00475	0.0120	L11	100	10.0	99.03
		-	0.00475	0.00475	-	L13			
16	Surface MS	L14	-	0.0068	-	L13	50	5.0	50.20
		-	-	-	-	-			

図 9-8. Board Trace Geometry

Refer to セクション 9.2 for a complete set of documentation for the DLP® LightCrafter™ Dual DLPC900 Evaluation Module (EVM) reference design.

9.3 Thermal Considerations

The thermal limitation for the DLPC900 is that the maximum operating junction temperature (T_J) must not be exceeded (this is defined in セクション 5.3). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC900, and power dissipation of surrounding components. The DLPC900 device package is designed

primarily to extract heat through the power and ground planes of the PCB, thus copper content and airflow over the PCB are important factors.

The recommended maximum operating ambient temperature (T_A) is provided primarily as a design target and is based on maximum DLPC900 power dissipation and $R_{\theta JA}$ at 1m/s of forced airflow, where $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC-defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC900 PCB, and thus the reported thermal resistance can be inaccurate in the actual product application. Although the actual thermal resistance can be different, it is the best information available during the design phase to estimate thermal performance. However after the PCB is designed and the product is built, it is highly recommended thermal performance be measured and validated.

To do this, the top-center case temperature must be measured under the worst-case product scenario (max power dissipation, max voltage, max ambient temp) and validated not to exceed the maximum recommended case temperature (T_C). This specification is based on the measured φ_{JT} for the DLPC900 package and provides a relatively accurate correlation to junction temperature. Care must be taken when measuring this case temperature to prevent accidental cooling of the package surface. It is recommended to use a small (approximately 40 gauges) thermocouple. The bead and the thermocouple wire must be covered with a minimal amount of thermally conductive epoxy and contact the top of the package. The wires are routed closely along the package and the board surface to avoid cooling the bead through the wires.

10 Device and Documentation Support

10.1 Device Support

10.1.1 Device Nomenclature

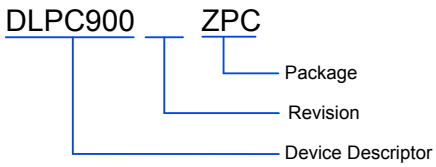
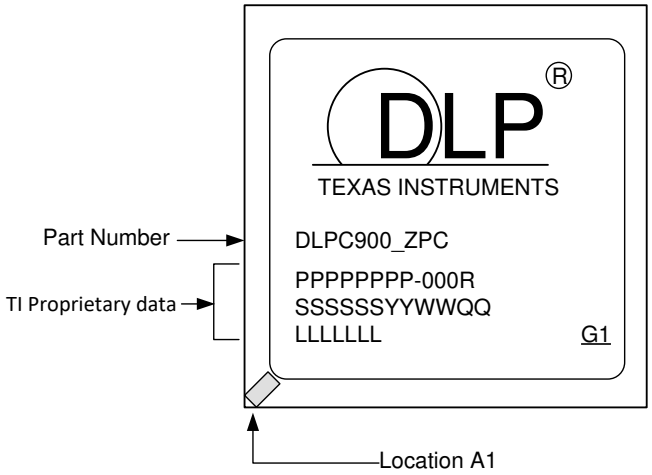


図 10-1. Device Number Description

10.1.2 Device Markings



10.1.3 DEFINITIONS—Video Timing Parameters

Active Lines Per Frame (ALPF)	Defines the number of lines in a frame containing displayable data: ALPF is a subset of the TLPF.
Active Pixels Per Line (APPL)	Defines the number of pixel clocks in a line containing displayable data: APPL is a subset of the TPPL.
Horizontal Back Porch (HBP) Blanking	Number of blank pixel clocks after horizontal sync but before the first active pixel. Note: HBP times are reference to the leading (active) edge of the respective sync signal.
Horizontal Front Porch (HFP) Blanking	Number of blank pixel clocks after the last active pixel but before Horizontal Sync.
Horizontal Sync (HS)	Timing reference point that defines the start of each horizontal interval (line). The absolute reference point is defined by the active edge of the HS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all horizontal blanking parameters are measured.
Total Lines Per Frame (TLPF)	Defines the vertical period (or frame time) in lines: TLPF = Total number of lines per frame (active and inactive).
Total Pixel Per Line (TPPL)	Defines the horizontal line period in pixel clocks: TPPL = Total number of pixel clocks per line (active and inactive).
Vertical Back Porch (VBP) Blanking	Number of blank lines after vertical sync but before the first active line.
Vertical Front Porch (VFP) Blanking	Number of blank lines after the last active line but before vertical sync.
Vertical Sync (VS)	Timing reference point that defines the start of the vertical interval (frame). The absolute reference point is defined by the active edge of the VS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all vertical blanking parameters are measured.

10.2 Documentation Support

10.2.1 Related Documentation

The following documents contain additional information related to the use of the DLPC900 device.

表 10-1. Related Documents

DOCUMENT	DOCUMENT LINK
DLP6500FLQ DMD Data Sheet	DLPS040
DLP6500FYE DMD Data Sheet	DLPS053
DLP9000 DMD Data Sheet	DLPS036
DLP500YX DMD Data Sheet	DLPS193
DLP670S DMD Data Sheet	DLPS194
DLP5500 DMD Data Sheet	DLPS013
DLPA200 DMD Micromirror Driver	DLPS015
DLPC900 Programmer's Guide	DLPU018
DLP® LightCrafter™ Single DLPC900 Evaluation Module (EVM) User's Guide	DLPU101
DLP® LightCrafter™ Dual DLPC900 Evaluation Module (EVM) User's Guide	DLPU102
Reference Design Documentation	DLPLCRC900EVM DLPLCRC900DEVM DLPLCR65EVM DLPLCR50XEVM DLPLCR55EVM DLPLCR67EVM DLPLCR90EVM

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.4 サポート・リソース

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すべての商標は、それぞれの所有者に帰属します。

10.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

Changes from Revision G (November 2023) to Revision H (June 2024) **Page**

- DRAM メモリに保存できる 1 ビット パターンの数を更新 ... 1
- Updated the number of 1-bit pre-stored patterns for each DMD in 表 6-3 ... 47
- Updated the DLP5500 DMD minimum pattern time for bit depth 3 and 6 in 表 6-4 ... 47
- Added pattern speed examples with dark time in 表 6-5 ... 47
- Added mimimum exposure time for active block 16 (DLP5500) and active block 6 (DLP670S) in 表 6-6 ... 47

Changes from Revision F (June 2021) to Revision G (November 2023) **Page**

- 一覧を再編成し、サポート対象デバイスの一覧に DLP5500 DMD を追加 ... 1
- 高速パターン速度の表現を編集し、DLP500YX に関する明確な情報を追加 ... 1
- フラッシュ メモリで保持できるパターンの数を削除 ... 1
- 「ビデオ モード」セクションの SVGA を XGA に訂正 ... 1
- DLPC900 コントローラでサポートされるデバイスのリストに DLP5500 DMD を追加 ... 1
- TI.com に掲載されなくなったページへのリンクを削除 ... 1
- アプリケーション概略図からファン ブロックを削除 ... 1
- DLP5500500 と他のすべての DMD で利用可能な 1 ビット パターンの数を列挙 ... 1
- Moved placement of footnote 3 in the Trigger Control Pin Function table ... 3
- Moved pins H23 and G23 from the Reserved Pin Functions table to Port1 and Port2 Channel Data and Control Pin Functions table ... 3
- Moved pins E8, B4, C4, E7, D5, E6, D3, C2, A4, B5, C6, A5, and D7 from Reserved Pin Functions table to Board-Level Test and Debug Pin Functions table ... 3
- Moved pins AD8, AE8, AF9, G24, D26, F23, F22, E24, and D25 from the Reserved Pin Functions table to the Peripheral Interface Pin Functions table ... 3
- Removed extraneous YCbCr reference ... 3
- Added the t_{SB} parameter to 表 5-1 table ... 25
- Removed t_{EW} from 表 5-1 table - duplicates t_{PH} ... 25
- Added DLPA200 to 図 5-3 ... 26
- PWRGOOD cannot be uses as an early warning signal for an anticipated power down ... 26
- Changed Power Mode = 1 "Standby" instructions for anticipated power down ... 26
- Changed Anticipated Power Down Sequence and Unanticipated Power Down Sequence diagrams to match the behavior of the DLPC900 controller ... 26
- Added DLP5500 DMD to list of supported devices ... 36
- Added XGA resolution to single DLPC900 controller systems for the DLP5500 ... 36
- Changed phrasing from 'normal' to 'default' ... 38
- Changed the section name from DLPC900 Memory Space to DLPC900 External Memory Space ... 40
- Updated GPIO signal names ... 44
- Updated GPIO signal names ... 45
- Removed lists of flash memory components and added links to the appropriate BOMs on TI.com ... 46
- Added information about the number of 1-bit patterns the DLP5500 can pre-load and corrected the 1-bit depth of the DLP670S DMD ... 47
- Added information to the tables about minimum exposure times for the DLP5500 ... 47
- Added table listing the number of 1-bit pre-stored patterns for each DMD ... 47
- Updated Section to include DLP5500 DMD and reordered the DMD names ... 50
- Updated block diagram and added 表 7-1 ... 50
- Updated DMD interface lists to include support for the DLP5500 ... 52
- Corrected P1_ bits to [0:9] ... 54

- Added information about optional GPIOs for extended external memory access..... 56
- Updated the schematic to reflect the DLP5500..... 58
- Updated Related Documents Table (added DLPLCR55EVM)..... 78

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC900AZPC	ACTIVE	BGA	ZPC	516	1	TBD	Call TI	Call TI	0 to 55		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

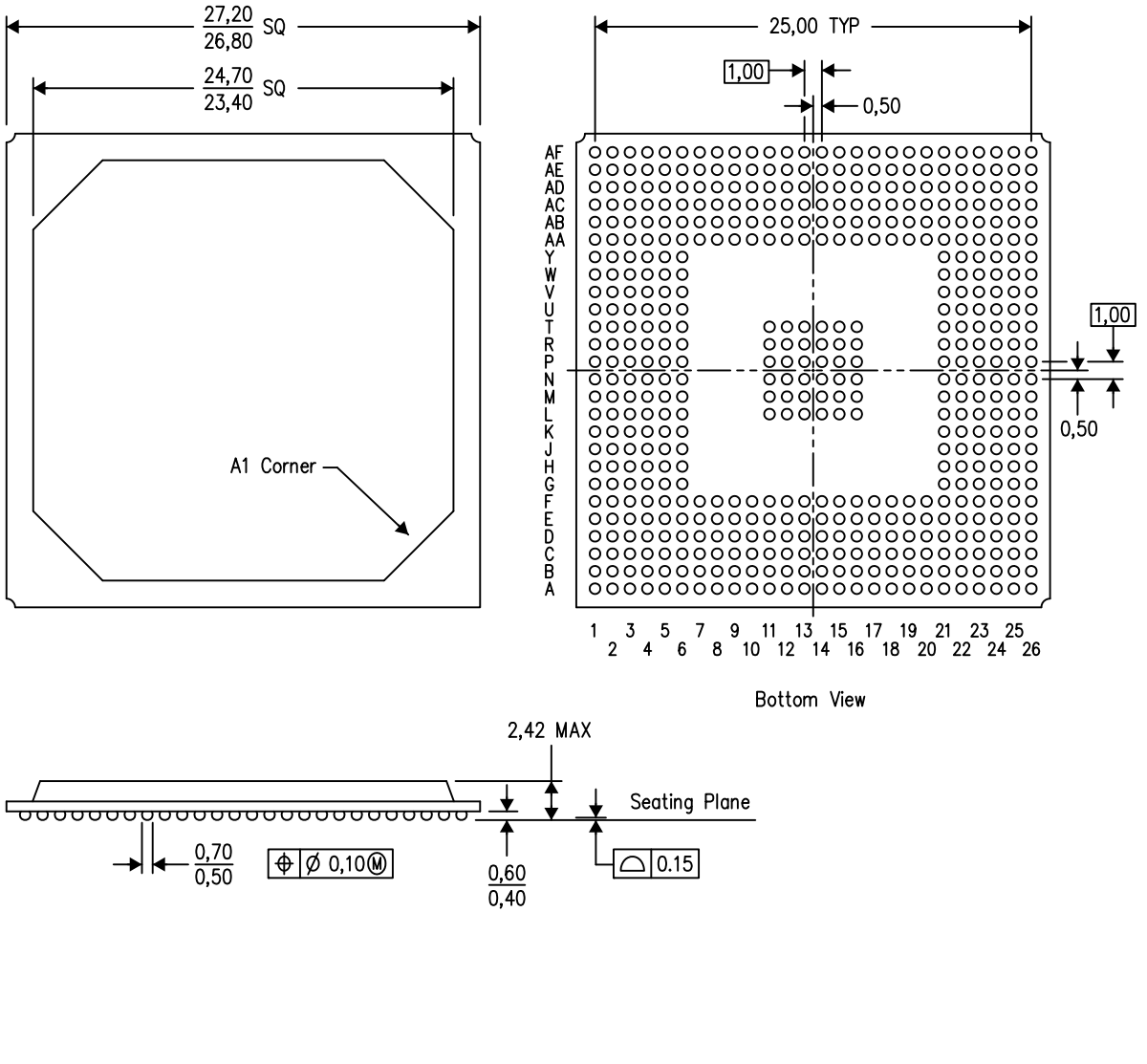
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

ZPC (S–PBGA–N516) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is Pb–free.

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