DLPC2607 低消費電力の DLP® ディスプレイ・コントローラ

1 特長

- 0.2nHD、0.24VGA、0.3WVGA DMDの信頼性の高い動作をサポート
- マルチモードの24ビット入力ピクセル・インターフェイス
  - パラレルまたはBT656バス・プロトコルに対応
  - QVGA～WVGAの入力サイズに対応
  - 1～60Hzのフレーム・レートに対応
  - 最高33.5MHzのピクセル・クロックに対応
  - 横方向/縦方向に対応
  - 8/16/18/24ビットのバス・オプションに対応
  - 3つの入力色(ビット)深度オプションに対応
    - RGB888、YCrCb888
    - RGB666、YCrCb666
    - RGB565、4:2:2 YCrCb
- ピクセル・データ処理
  - 画像リサイズ(スケーリング)
  - フレーム・レート変換
  - カラー・コーディネート調整
  - 自動ゲイン制御
  - プログラミング可能な逆ガンマ補正
  - 時空間多重(ディザリング)
  - ビデオ処理に対応
    - 色空間の変換
    - 4:2:2～4:4:4の色差補間
    - フィールド・スケーリング・デインターレース
- 176ピン、0.4mmピッチのVFBGAパッケージ
- 外部メモリに対応
  - 166MHzモバイルDDR SDRAM
  - 33.3MHzシリアル・フラッシュ
- WVGA、VGA、nHD DMDディスプレイに対応
  - DMDビットプレーンの生成およびフォーマット
  - プログラマブル・ビットプレーン・ディスプレイ・シーケンサ(LEDイネーブルおよびDMDロードを制御)
  - 76.2MHzのダブル・データ・レート(DDR) DMD I/F
  - ミラー用パルス幅変調(PWM)
    - 電源オフ時の自動DMDパーキング
    - DMDで24ビットのビット深度
- システム制御
  - デバイス構成のI^2C制御
  - プログラミング可能なスプラッシュ・スクリーン
  - プログラミング可能なLED電流制御
  - DMD電源およびミラー・ドライバ制御
  - DMD表示画像の左右/上下反転
  - 表示画像の回転
  - フラッシュを使用した構成バッチ・ファイル
  - I/Fスリープ静止画省電力モード
- テストのサポート
  - テスト・パターン生成機能を内蔵
  - JTAGバウンダリ・スキャン・テストに対応

2 アプリケーション

- 組み込みモバイル・プロジェクション
  - スマートフォン
  - タブレット
  - カメラ
  - ノートPC
- モバイル・アクセサリ
- ウェアラブル(ニアアイ)ディスプレイ
- バッテリ動作のプロジェクター

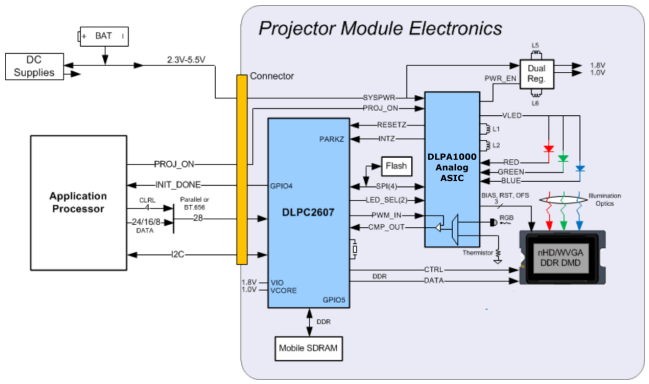
3 概要

DLPC2607はバッテリ駆動ディスプレイ機器向けの低消費電力 DLP™デジタル・コントローラであり、0.3WVGA、0.24VGA、0.2nHD DMDの信頼性の高い動作をサポートします。DLPC2607コントローラは、システム電子機器とDMDの間を接続する便利な多機能インターフェイスを提供し、小型で低消費電力のディスプレイを実現します。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
DLPC2607	VFBGA (176)	7.00mm×7.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (May 2017) から Revision E に変更 **Page**

- タイトルを「DLPC2607 DLP PICO プロセッサ 2607 ASIC」から「DLPC2607 低消費電力の DLP® ディスプレイ・コントローラ」に 変更 ... 1
- Added ZVB Package Bottom View ... 5
- Changed to "Add external pullup or pulldown resistors as needed to these signals to avoid floating inputs" ... 5
- Changed PAD1000 to DLPA1000 ... 5
- Changed to "Establish this setting" ... 5
- Changed "low a minimum" to "low to a minimum" ... 5
- Changed "Should be pulled up to" to "Pull up to" ... 5
- Changed "Unused inputs should be pulled down" to "Pull unused inputs" ... 6
- Added DMD INTERFACE pin descriptions ... 7
- Added SDRAM INTERFACE pin descriptions ... 8
- Changed "It should be connected" to "Connect". ... 9
- Changed globally "Should be left open or unconnected for typical use." to "Leave open or unconnected for typical use." ... 10
- Changed globally "An external pullup should not be applied to this pin..." to "Do not apply an external pullup to this pin..." ... 10
- Swapped all values under I_{OH} and I_{OL} ... 14
- Changed "that should be applied" to "can safely be applied" ... 14
- Changed "that should be applied" to "can safely be applied" ... 14
- Changed "$_{OH}$and $_{OL}$" to VOH and VOL to clarify meaning ... 14
- Changed "VCCIO =" to "VCCIO (V)" ... 14

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改訂履歴 (continued)

- Changed "MAX Supported" to "Maximum Parallel Interface" 16
- Changed Changed "BT.565" to "BT.656" 17
- Added link to ITU-R BT.656 specification 17
- Changed "NOTE:" to "The table below" 17
- Deleted "Note that" 17
- Changed f_{clock} min 18
- Changed t_{p_clkper} min and max 18
- Changed "should support" to "supports" 25
- Changed "Thus, those pins should be tied" to "Tie these pins" 26
- Changed "1.8-, 2.5-, or 3.3-V" to "1.8 V, 2.5 V, or 3.3 V" 26
- Changed "the ASIC only supports periodic sources" to "the ASIC supports periodic sources only" 27
- Changed "multi media" to "multimedia" 27
- Changed Device Functional Modes to System Functional Modes and moved to correct position 27
- Added Reference to TSTPT_6 for Crystal nominal frequency 28
- Changed "ASIC, and the PLL_REFCLK_O pins hould be left unconnected" to "ASIC. Leave the PLL_REFCLK_O pins unconnected" 29
- Changed "The benefit of an oscillator is that it can be made to provide a spread-spectrum clock that reduces EMI." to "An oscillator that provides a spread-spectrum clock reduces EMI." 29
- Changed "can only accept" to "accepts" 29
- Added kHz 29
- Changed several items in Table 7 29
- Changed " the ODM's own risk" to "the risk of the ODM" 29
- Changed " Layout guidelines should be followed" to "Follow the layout guidelines" 29
- Changed "To complete DLP system . . . is requiered" to "The DLP system requires" 29
- Changed "The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors." to "An optical OEM that specializes in designing optics for DLP projectors typically supplies the optical engine that has the LED packages and the DMD mounted to it." 29
- Deleted "Note that" 30
- Changed "this allows these inputs to be driven high" to "This protection allows the device to drive these inputs high" 30
- Changed 30
- Changed "All I/O power should remain" to "Ensure that all I/O power remains" 32
- Changed "is defined" to "operates as" 35
- Changed "should alert" to "alerts" 35
- Changed "Note that the reference clock should continue to run and RESET should remain" to "The reference clock continues to run. RESET remains" 35
- Changed "At a minimum, VDD_PLL power and VSS_PLL ground pins should be isolated" to "Isolate VDD_PLL power and VSS_PLL ground pins" 36
- Changed "It is important that the quiet ground and power are treated like analog signals" to "The ground and power domains are analog signals, and should be treated as such to achieve minimum noise." 36
- Changed "The power and ground traces should be as short as possible" to "Ensure that the power and ground traces are as short as possible" 36
- Changed "and should not be expected" to "so do not expect them" 37
- Changed "they should be" to "ensure they are" 37
- Changed "should be split" to "Split the" 37
- Changed "In addition, the SPICLK trace . . . should be" to "Make the SPICLK trace" 37
- Changed "should be split" to "Split the" 37

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改訂履歴 (continued)

- Changed "In addition, the SPIDOUT trace . . . should be" to "Make the SPIDOUT trace" 37
- Changed "The SPIDIN .... should be split" to "Make the SPDIN" 37
- Changed "on their way back" to "on the return" 37
- Changed "They should then share" to "Make sure they share" 37
- Changed "Variation from these recommendations may also work, but should be confirmed with PCB signal integrity analysis or lab measurements" to "Make sure to confirm any variation from these recommendations with PCB signal integrity analysis or lab measurements" 37
- Changed PCB Design table to itemized list 38
- Changed "should take" to "takes" 40
- Changed "should take" to "takes" 40
- Changed "should" to "must" 40
- Changed "The pair should also be terminated" to "Terminate the pair" 41
- Changed "Specifically ... should be terminated" to "Terminate" 41
- Changed "Specifically ... should be terminated" to "Terminate" 41
- Changed "kept" to "maintained to a length of" 41
- Changed "should" to "does" 41

Revision C (November 2015) から Revision D に変更 **Page**

- Removed table 'Compatible SPI Serial Flash Devices' from *Serial Flash Interface* since listed devices are end of life. Replaced with new suggested devices as well as Table 4 which lists minimum performance specifications to determine flash device compatibility 26
- MSLピーク温度を*パッケージ情報*に追加 45

Revision B (January 2014) から Revision C に変更 **Page**

- 「*ESD定格*」の表、「*熱に関する情報*」の表、「*機能説明*」セクション、「*デバイスの機能モード*」、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 1

Revision A (December 2013) から Revision B に変更 **Page**

- 製品プレビュー・バナーを削除 1

2013年12月発行のものから更新 **Page**

- Corrected columns for I_{OH} and I_{OL} in *I/O Characteristics* 14
- Updated B38 I/O Type value for V_{OH} (min) in *I/O Characteristics* 14
- Added additional table notes to *I/O Characteristics* 14
- Added table note to *Internal Pullup and Pulldown Characteristics* 14
- Corrected device reference to DLPC2607 in the notes for *mDDR Memory Interface Timing Requirements* 19

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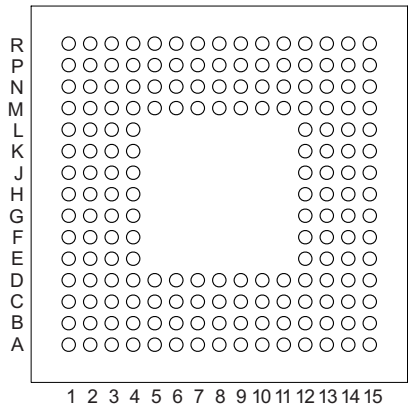
5 Pin Configuration and Functions

ZVB Package
176-Pin NFBGA
Bottom View



Pin Functions (1)

PIN		I/O		CLOCK SYSTEM	DESCRIPTION
NAME	NO.	POWER	TYPE		
DEVICE INITIALIZATION AND REFERENCE CLOCK (1)					
RESETZ	J14	VCC18	I1	Async	DLPC2607 power-on reset. Self-configuration starts when a low-to-high transition is detected on this pin. All ASIC power and clocks must be stable before this reset is de-asserted (hysteresis buffer). Note that the following seven signals tri-state while RESET is asserted: DMD_PWR_EN, LEDDVR_ON, LED_SEL_0,LED_SEL_1, SPICLK, SPIDOUT, SPICSZ0 Add external pullup or pulldown resistors as needed to these signals to avoid floating inputs.
PLL_REFCLK_I	K15	VCC18 (filter)	I4	N/A	Reference clock crystal input. If an external oscillator is used in place of a crystal, then use this pin as the oscillator Input.
PLL_REFCLK_O	J15		O14	N/A	Reference clock crystal return. If an external oscillator is used in place of a crystal, then leave this pin unconnected (floating).
FLASH INTERFACE (2)					
SPICLK	A4	VCC_ FLSH	O24	N/A	Clock for the external SPI device or devices
SPIDIN	B4		I2	SPICLK	Serial data input from the external SPI device or devices
SPICSZ0	A5		O24	SPICLK	Chip select 0 output for the external SPI flash device. Active low
SPICSZ1	C6		O24	SPICLK	Chip select 1 output for the external SPI DLPA1000 device. Active low
SPIDOUT	C5		O24	SPICLK	Serial data output to the external SPI device or devices. This pin sends address and control information as well as data when programming
MAIN VIDEO DATA AND CONTROL					
PARK	B8	VCC_ INTF	I3	Async	DMD park control (active low) is set high to enable typical operation. Establish this setting prior to releasing RESET, or within 500 µs after releasing RESET. It should be set low to a minimum of 500 µs before any power is to be removed from the DLPC2607 (hysteresis buffer).
LED_ENABLE	A11	VCC_ INTF	I3	Async	LED enable (active high input). A logic low on this signal forces LEDDRV_ON low and LED_SEL(1:0) = b00. These signals are enabled 100 ms after LED_ENABLE transitions from low to high (hysteresis buffer).
DBIC_CSZ	B10	VCC_ INTF	I3	SCL	Unused/reserved: Pull up to VCC_INTF.
SCL	A10	VCC_ INTF	B38	N/A	I^2C clock (hysteresis buffer) bidirectional, open-drain signal. An external pullup is required. No I^2C activity is permitted for a minimum of 100 ms after PARK and RESET are set high.
SDA	C10	VCC_ INTF	B38	SCL	I^2C data (hysteresis buffer) bidirectional, open-drain signal. An external pullup is required.

(1) Each device connected to the serial peripheral interface (SPI) bus must be operated off VCC_FLSH
(2) Each device connected to the SPI bus must be operated off VCC_FLSH

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Pin Functions [1] (continued)

PIN		I/O		CLOCK SYSTEM	DESCRIPTION	
NAME	NO.	POWER	TYPE			
GPIO4_INTF	C9	VCC_ INTF	B34	Async	General purpose I/O 4 (hysteresis buffer). Primary usage is to indicate when auto-initialization is complete (also referred to as INIT-DONE, which is when GPIO4 transitions high then low following release of $\overline{\text{RESET}}$) and to flag a detected error condition in the form of a logic high, pulsed Interrupt flag subsequent to INIT-DONE.	
GPIO5_INTF	B9	VCC_ INTF	B34	Async	General purpose I/O 5 (hysteresis buffer). For applications that use focus motor control with a sensor, this pin is an input that is connected to the motor position sensor. For applications that use non-focus motor control with a sensor, configure this pin with an output at logic 0 and left unconnected.	
MAIN VIDEO DATA AND CONTROL					**PARALLEL RGB MODE**	**BT.656 I/F MODE**
PCLK (Hysteresis)	D13	VCC_ INTF	I3	N/A	Pixel clock [3]	Pixel clock [3]
PDM_CVS_TE	H15	VCC_ INTF	B34	ASYNC	Parallel data mask [4]	Unused [5]
VSYNC_WE	H14	VCC_ INTF	I3	ASYNC	Vsync [6]	Unused[5]
HSYNC_CS	H13	VCC_ INTF	I3	PCLK	Hsync [6]	Unused [5]
DATEN_CMD	G15	VCC_ INTF	I3	PCLK	Data valid [6]	Unused [5]
PDATA[0]	G14	VCC_ INTF	I3	PCLK	Data [7]	Data0 [7]
PDATA[1]	G13	VCC_ INTF	I3	PCLK	Data [7]	Data1 [7]
PDATA[2]	F15	VCC_ INTF	I3	PCLK	Data [7]	Data2 [7]
PDATA[3]	F14	VCC_ INTF	I3	PCLK	Data [7]	Data3 [7]
PDATA[4]	F13	VCC_ INTF	I3	PCLK	Data [7]	Data4 [7]
PDATA[5]	E15	VCC_ INTF	I3	PCLK	Data [7]	Data5 [7]
PDATA[6]	E14	VCC_ INTF	I3	PCLK	Data [7]	Data6 [7]
PDATA[7]	E13	VCC_ INTF	I3	PCLK	Data [7]	Data7 [7]
PDATA[8]	D15	VCC_ INTF	I3	PCLK	Data [7]	Unused [5]
PDATA[9]	D14	VCC_ INTF	I3	PCLK	Data [7]	Unused [5]
PDATA[10]	C15	VCC_ INTF	I3	PCLK	Data [7]	Unused [5]
PDATA[11]	C14	VCC_ INTF	I3	PCLK	Data [7]	Unused [5]
PDATA[12]	C13	VCC_ INTF	I3	PCLK	Data [7]	Unused [5]
PDATA[13]	B15	VCC_ INTF	I3	PCLK	Data [7]	Unused [5]
PDATA[14]	B14	VCC_ INTF	I3	PCLK	Data [7]	Unused [5]
PDATA[15]	A15	VCC_ INTF	I3	PCLK	Data [7]	Unused [5]
PDATA[16]	A14	VCC_ INTF	I3	PCLK	Data [7]	Unused [5]
PDATA[17]	B13	VCC_ INTF	I3	PCLK	Data [7]	Unused [5]
PDATA[18]	A13	VCC_ INTF	I3	PCLK	Data [7]	Unused [5]
PDATA[19]	C12	VCC_ INTF	I3	PCLK	Data [7]	Unused [5]
PDATA[20]	B12	VCC_ INTF	I3	PCLK	Data [7]	Unused [5]
PDATA[21]	A12	VCC_ INTF	I3	PCLK	Data [7]	Unused [5]
PDATA[22]	C11	VCC_ INTF	I3	PCLK	Data [7]	Unused[5]
PDATA[23]	B11	VCC_ INTF	I3	PCLK	Data [7]	Unused [5]

(3) Pixel clock capture edge is software programmable.
(4) Data mask is optional for parallel bus operation. If unused, pull to ground through a resistor.
(5) Pull unused inputs to ground through an external resistor.
(6) VSYNC, HSYNC, and data valid polarity is software programmable.
(7) PDATA(23:0) bus mapping is pixel format and source mode dependent.

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Pin Functions [1] (continued)

PIN		I/O		CLOCK SYSTEM	DESCRIPTION
NAME	NO.	POWER	TYPE		
DMD INTERFACE					
DMD_D0	M15	VCC18	O58	DMD_DCLK	DMD Data Pins. DMD Data pins are double data rate (DDR) signals that are clocked on both edges of DMD_DCLK. All 15 DMD data signals are use to interface to the WVGA and VGA DMDs; however, only 12 of the 15 are used to interface to an nHD DMD. The standard nHD interconnect is to utilize pins DMD_D(11:0). However, DMD_D(14:3) must be used to interface to the nHD DMD when the I^2C programmable option to reverse the bit-order of the DMD interface pins is selected (DMD Bus Swap Control, I^2C: 0xA7).
DMD_D1	N14				
DMD_D2	M14				
DMD_D3	N15				
DMD_D4	P13				
DMD_D5	P14				
DMD_D6	P15				
DMD_D7	R15				
DMD_D8	R12				
DMD_D9	N11				
DMD_D10	P11				
DMD_D11	R11				
DMD_D12	N10				
DMD_D13	P10				
DMD_D14	R10				
DMD_DCLK	N13			N/A	DMD Data Clock (DDR)
DMD_LOADB	R13			DMD_DCLK	DMD Data Load Signal (active low). This signal requires an external pullup to VCC18.
DMD_SCTRL	R14			DMD_DCLK	DMD Data Serial Control Signal
DMD_TRC	P12			DMD_DCLK	DMD Data Toggle Rate Control
DMD_DAD_BUS	L13			DMD_SAC_CLK	DMD DAD Bus Data
DMD_DAD_STRB	K13			DMD_SAC_CLK	DMD DAD Bus Strobe
DMD_DAD_OEZ	M13			Async	DMD Reset Driver Output Enable (active low). To properly park the DMD, this signal requires a 30-kΩ to 100-kΩ external pullup resistor connected to VCC18.
DMD_SAC_BUS	L15			DMD_SAC_CLK	DMD SAC Bus Data
DMD_SAC_CLK	L14			N/A	DMD SAC Bus Clock

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Pin Functions [1] (continued)

PIN		I/O		CLOCK SYSTEM	DESCRIPTION
NAME	NO.	POWER	TYPE		
SDRAM INTERFACE					
MEM0_CLK_P	D1	VCC18	O74	N/A	mDDR memory, Differential Memory Clock
MEM0_CLK_N	E1		O74		
MEM0_A0	P1		O64	MEM_CLK	mDDR memory, Multiplexed Row, and Column Address
MEM0_A1	R3				
MEM0_A2	R1				
MEM0_A3	R2				
MEM0_A4	A1				
MEM0_A5	B1				
MEM0_A6	A2				
MEM0_A7	B2				
MEM0_A8	D2				
MEM0_A9	A3				
MEM0_A10	P2				
MEM0_A11	B3				
MEM0_A12	D3				
MEM0_BA0	M3				mDDR memory, Bank Select
MEM0_BA1	P3				
MEM0_RASZ	P4				mDDR memory, Row Address Strobe (active low)
MEM0_CASZ	R4				mDDR memory, Column Address Strobe (active low)
MEM0_WEZ	R5				mDDR memory, Write Enable (active low)
MEM0_CSZ	J3				mDDR memory, Chip Select (active low)
MEM0_CKE	C1				mDDR memory, Clock Enable (active high)
MEM0_LDQS	J2		B64	N/A	mDDR memory, Lower Byte, R/W Data Strobe
MEM0_LDM	J1		O64	MEM0_LDQS	mDDR memory, Lower Byte, Write Data Mask
MEM0_DQ0	N1		B64	MEM0_LDQS	mDDR memory, Lower Byte, Bidirectional R/W Data
MEM0_DQ1	M2				
MEM0_DQ2	M1				
MEM0_DQ3	L3				
MEM0_DQ4	L2				
MEM0_DQ5	K2				
MEM0_DQ6	L1				
MEM0_DQ7	K1				
MEM0_UDQS	G1		B64	N/A	mDDR memory, Upper Byte, R/W Data Strobe
MEM0_UDM	H1		O64	MEM0_UDQS	mDDR memory, Upper Byte, Write Data Mask
MEM0_DQ8	H2		B64	MEM0_UDQS	mDDR memory, Upper Byte, Bidirectional R/W Data
MEM0_DQ9	G2				
MEM0_DQ10	H3				
MEM0_DQ11	F3				
MEM0_DQ12	F1				
MEM0_DQ13	E2				
MEM0_DQ14	F2				
MEM0_DQ15	E3				

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Pin Functions [1] (continued)

PIN		I/O		CLOCK SYSTEM	DESCRIPTION
NAME	NO.	POWER	TYPE		
LED DRIVER INTERFACE					
GPIO1_RPWM	N8	VCC18	O14	Async	General-purpose I/O 1 (output only). If the DLPA1000 is not used, then this output must be used as the red LED PWM signal used to control the LED current.[8] If the DLPA1000 is used, then this output can be used as a general purpose output controlled by the WPC processor.
GPIO2_GPWM	P9		O14	Async	General-purpose I/O 2 (output only). If the DLPA1000 is not used, then this output must be used as the green LED PWM signal used to control the LED current.[8] If the DLPA1000 is used, then this output can be used as a general purpose output controlled by the WPC processor.
GPIO3_BPWM	R8		O14	Async	General-purpose I/O 3 (output only). If the DLPA1000 is not used, then this output must be used as the blue LED PWM signal used to control the LED current.[8] If the DLPA1000 is used, then this output can be used as a general-purpose output controlled by the WPC processor.
LED_SEL_0	R6		O14	Async	LED enable SELECT. Controlled by programmable DMD sequence timing (hysteresis buffer).
LED_SEL_1	N6		O14	Async	**LED_SEL(1:0)** / **Selected LED**: 00 – None; 01 – Red; 10 – Green; 11 – Blue. These outputs should be input directly to the DLPA1000 if used. If the DLPA1000 is not used, then a decode circuit is required to decode the selected LED enable.
LEDDRV_ON	P7		O14	Async	LED driver enable. Active-high output control to external LED driver logic (master enable). It is driven high 100 ms after LED_ENABLE is driven high and driven low immediately when either LED_ENABLE or $\overline{PARK}$ is driven low.
DMD_PWR_EN	K14		O14	Async	DMD power regulator enable (active high). This is an active-high output that should be used to control DMD V_{OFFSET}, V_{BIAS}, and V_{RESET} voltages. DMD_PWR_EN is driven high when the $\overline{PARK}$ input signal is set high. However, DMD_PWR_EN is held high for 500 µs after the $\overline{PARK}$ input signal is set low before it is driven low. TI recommends a weak external pulldown resistor to keep this signal at a known state during power-up reset.
WHITE POINT CORRECTION LIGHT SENSOR I/F					
CMP_OUT	A6	VCC_ 18	I1	Async	Successive approximation ADC comparator output (DLPC2607 input). Assumes a successive approximation ADC is implemented with either a light sensor or thermocouple or both feeding one input of an external comparator and the other side of the comparator driven from the CMP_PWM pin of the ASIC. If this function is not used, pull it down to ground (hysteresis buffer).
CMP_PWM	B7		O14	Async	Successive approximation comparator pulse-width modulation input. Supplies a PWM signal to drive the successive approximation ADC Comparator used in light-to-voltage light sensor applications. If this function is not used, leave it unconnected.
GPIO0_CMPPWR	P5		B14	Async	Power control signal for the WPC light sensor and other analog support circuits using the DLPC2607 ADC. Alternately, it provides general purpose I/O to the WPC microprocessor internal to the DLPC2607 device. If not used, leave it unconnected (hysteresis buffer).
HWTEST_EN	A9	VCC _INTF	I3	N/A	Manufacturing test enable signal. Connect directly to ground on the PCB for typical operation. Includes weak internal pulldown.
JTAGTDI	P6	VCC _18	I1	JTAGTCK	JTAG, serial data in. Includes weak internal pullup. (When JTAGRSTZ is held low, this input can be used as ICP/ WPC debug port RXD.)
JTAGTCK	N5			N/A	JTAG, serial data clock. Includes weak internal pullup.
JTAGTMS	N7			JTAGTCK	JTAG, test mode select. Includes weak internal pullup.
JTAGTDO	R7		O14	JTAGTCK	JTAG, serial data out
JTAGRSTZ	P8		I1	ASYNC	JTAG, RESET (active low). Includes weak internal pullup. This signal must be tied to ground, through an external ≤15-kΩ resistor, for typical operation.

(8) The DLPA1000 is not available for initial DLPC2607 design applications. When the DLPA1000 is not used, all LED PWM signals are forced high when LEDDRV_ON = 0, software LED control is disabled, or the sequence stops.

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Pin Functions [1] (continued)

PIN		I/O		CLOCK SYSTEM	DESCRIPTION
NAME	NO.	POWER	TYPE		
TEST AND DEBUG INTERFACES					
TSTPT_0	B6	VCC18	B18	Async	Test pin 0 – Sampled as an input test mode selection control upon release of RESET, and then driven as an output. Includes weak internal pulldown.[9] Normal use: Reserved for test output (ICP/ WPC debug port TXD). Leave open or unconnected for typical use. Alternative use: If focus motor control is used, use this pin as the motor driver chip enable. Do not apply an external pullup to this pin to avoid putting the DLPC2607 device in a test mode.
TSTPT_1	A8	VCC18	B18	Async	Test pin 1 – Sampled as an input test mode selection control upon release of RESET, and then driven as an output. Includes weak internal pulldown.[9] Normal use: Reserved for test output. Leave open or unconnected for typical use. Alternative use: If focus motor control is used, use this pin as the motor driver data bit1 (LSB). Do not apply an external pullup to this pin to avoid putting the DLPC2607 device in a test mode.
TSTPT_2	C7	VCC18	B18	Async	Test pin 2 – Sampled as an input test mode selection control upon release of RESET, and then driven as an output. Includes weak internal pulldown.[9] Normal use: Reserved for test output. Leave open or unconnected for typical use. Alternative use: If focus motor control is used, use this pin as the motor driver data bit2. Do not apply an external pullup to this pin to avoid putting the DLPC2607 device in a test mode.
TSTPT_3	B5	VCC18	B18	Async	Test Pin 3 – Sampled as an input test mode selection control upon release of RESET, and then driven as an output. Includes weak internal pulldown.[9] Normal use: Reserved for test output. Leave open or unconnected for typical use. Alternative use: If focus motor control is used, use this pin as the motor driver motor driver data bit3. Do not apply an external pullup to this pin to avoid putting the DLPC2607 device in a test mode.
TSTPT_4	A7	VCC18	B18	Async	Test pin 4 – Sampled as an input test mode selection control upon release of RESET, and then driven as an output. Includes weak internal pulldown.[9] Normal use: Reserved for test output. Leave open or unconnected for typical use. Alternative use: If focus motor control is used, use this pin as the motor driver data bit4 (MSB). Do not apply an external pullup to this pin to avoid putting the DLPC2607 device in a test mode. **Without External Pullup** [9] / **With External Pullup** [10] Enables auto-initialization from flash / Disables auto-initialization and facilitates flash programming via I^2C of a blank flash
TSTPT_5	C8	VCC18	B18	Async	Test pin 5 – Sampled as an input test mode selection control upon release of RESET and then driven as an output. Includes weak internal pulldown.[9] Normal use: Reserved for test output. Leave open or unconnected for typical use. Alternative use: Not yet defined. Do not apply an external pullup to this pin to avoid putting the DLPC2607 device in a test mode.
TSTPT_6	N9	VCC18	B18	Async	Test pin 6 and PLL REFCLK frequency selection – Sampled as an input test mode selection control upon release of RESET and then driven as an output. Includes a weak internal pulldown.[9] Normal use: Reserved for test output. Leave open or unconnected for typical use. Alternative use: Not yet defined. This pin is sampled upon de-assertion of RESTZ to determine REFCLK frequency selection. DLPC2607 I^2C address is set corresponding to the sampled input value as follows: **Without External Pullup** [9] / **With External Pullup** [10] PLL assumes REFCLK = 16.67 MHz / PLL assumes REFCLK = 8.33 MHz

(9) If operation does not call for an external pullup and there is no external logic that might overcome the weak internal pulldown resistor, then this I/O can be left open or unconnected for typical operation. If operation does not call for an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then TI recommends an external pulldown resistor to ensure a logic low.
(10) External pullup resistor must be 15 kΩ or less.

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Pin Functions (1) (continued)

PIN		I/O		CLOCK SYSTEM	DESCRIPTION	
NAME	NO.	POWER	TYPE			
TSTPT_7	R9	VCC18	B18	Async	Test pin 7 and I^2C address selection – Sampled as an input test mode selection control upon release of $\overline{RESET}$, and then driven as an output. Includes weak internal pulldown. Normal use: Reserved for test output. Leave open or unconnected for typical use. Alternative use: Not yet defined. This pin is sampled upon deassertion of $\overline{RESET}$ to determine I^2C address selection. DLPC2607 I^2C address is set corresponding to the sampled input value as follows:	
					Without External Pullup (9)	**With External Pullup** (10)
					I^2C slave Write Address = x36 I^2C slave Read Address = x37	I^2C slave Write Address = x3A I^2C slave Read Address = x3B
POWER AND GROUND (11)						
VDD10	D5, D9, F4, F12, J4, J12, M6, M8, M11				1-V core logic power supply	
VDD_PLL	H12				1-V power supply for the internal PLL	
VCC18	C4, D8, E4, G3, K3, K12, L4, M5, M9, M12, N4, N12				1.8-V power supply for all I/O other than the host, video interface, and SPI flash buses	
VCC_FLSH	D6				1.8-V, 2.5-V, or 3.3-V power supply for SPI flash bus I/O	
VCC_INTF	D11, E12				1.8-V, 2.5-V, or 3.3-V power supply for all I/Os on the host or video interface (includes I^2C, PDATA, video syncs, $\overline{PARK}$, and LED_ENABLE pins)	
GND	D4, D7, D10, D12, G4, G12, H4, K4, L12, M4, M7, M10				Common ground	
RTN_PLL	J13				Analog ground return for the PLL (This must be connected to the common ground GND through a ferrite.)	
Reserved	C2, C3, N2, N3				No connects. Other signals can be routed through the ball on these pins (versus going around them) to ease routing if desired	

(11) 134 total signal I/O pins, 38 total power or ground pins, and 4 total reserved pins

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage[2]	V_{DD10}	–0.5	1.32	V
	VDD_PLL	–0.5	1.32	
	V_{CC18}	–0.5	2.75	
	VCC_FLSH	–0.5	3.6	
	V_{CC_INTF}	–0.5	3.6	
	V_I 1.8 V, 2.5 V, 3.3 V [3]	–0.5	3.6	
T_J	Operating junction temperature	–30	105	ºC
T_A	Operating ambient temperature [4] [5]	–30	85	ºC
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND and are at the device not at the power supply.
(3) Applies to external input and bidirectional buffers.
(4) TI strongly recommends I/O simulations (using IBIS models) for operation near the extremes of the supported ambient operating temperature range to ensure that the PCB design provides acceptable signal integrity.
(5) The operating ambient temperature range assumes zero forced air flow, a JEDEC JESD51 junction-to-ambient thermal resistance value at zero forced air flow ($R_{\theta JA}$ at 0 m/s), a JEDEC JESD51 standard test card and environment, along with minimum and maximum estimated power dissipation across process, voltage, and temperature. Thermal conditions vary by application, which impacts $R_{\theta JA}$. Thus, maximum operating ambient temperature varies by application.
(a) $T_{A_min} = T_{J_min} – (P_{D_min} \times R_{\theta JA}) = –30°C – (0.0\ W \times 64.96°C/W) = –30°C$
(b) $T_{A_min} = T_{J_min} – (P_{D_min} \times R_{\theta JA}) = 105°C – (0.3\ W \times 64.96°C/W) = 85°C$

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VDD10	1-V supply voltage, core logic		0.95	1	1.05	V
VDD_PLL	Analog voltage for PLL		0.95	1	1.05	V
VCC18	1.8-V supply voltage (for all non-flash and host interface signals)		1.71	1.8	1.89	V
VCC_FLSH	Configuration and control I/O supply voltage (variable)	1.8-V LVCMOS	1.71	1.8	1.89	V
		2.5-V LVCMOS	2.375	2.5	2.625	V
		3.3-V LVCMOS	3.135	3.3	3.465	V
VCC_INTF	Pixel interface supply voltage (variable)	1.8-V LVCMOS	1.71	1.8	1.89	V
		2.5-V LVCMOS	2.375	2.5	2.625	V
		3.3-V LVCMOS	3.135	3.3	3.465	V
V_I	Input voltage		–0.3		VCCIO[1] + 0.3	V
V_O	Output voltage		0		VCCIO[1]	V
t_{RAMP}	Power supply ramp time		10			µs

(1) VCCIO represents the actual supply voltage applied to the corresponding I/O.

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6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC[1]		DLPC2607 ZVB (NFBGA) 176 PINS	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance	19.52	ºC/W
$R_{\theta JA}$	Junction-to-air thermal resistance (with no forced airflow)	64.96	ºC/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Typical Current and Power Dissipation

over operating free-air temperature range (unless otherwise noted)

SUPPLY	TYPICAL VOLTAGE (V)	WVGA APPLICATIONS		nHD APPLICATIONS	
		TYPICAL CURRENT (mA)	TYPICAL POWER (mW)	TYPICAL CURRENT (mA)	TYPICAL POWER (mW)
I/F Sleep Mode Disabled [1] [2] [3]					
VCC_INTF	1.8	0	0.1	0	0.1
VCC_FLSH[4]	2.5	0	0	0	0
VCC18	1.8	28.2	50.8	22.7	40.9
VDD_PLL	1	2.8	2.8	2.8	2.8
VDD10	1	39	39.0	37.7	37.7
Total			92.7		81.5
I/F Sleep Mode Enabled [1] [2] [3]					
VCC_INTF	1.8	0	0.1	0	0.1
VCC_FLSH	2.5	0	0	0	0
VCC18[4]	1.8	27	48.6	22.5	40.4
VDD_PLL	1	2.8	2.8	2.8	2.8
VDD10	1	30.6	30.6	29.3	29.3
Total			82.1		72.6

(1) I/F sleep is a programmable parameter that can be set to save power in free-run, sequencer mode when displaying still images on the DMD. When I/F sleep is enabled, any images applied to the input bus to the DLPC2607 device are ignored.
(2) Power for both I/F sleep mode disabled and I/F sleep mode enabled was measured while transferring a full 864 × 480 landscape image at periodic 30 frames per second. The image was a 12 × 6 color checkerboard.
(3) All measurements were taken on a TI internal reference design board at 25°C ambient.
(4) VCC_FLSH power was 0 at the time of the measurement because flash accesses are limited when the ASIC is being configured.

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6.6 I/O Characteristics

Voltage and current characteristics for each I/O type signal listed previously in the DLPC2607 table are summarized in *I/O Characteristics*. All inputs and outputs are LVCMOS.(1)

I/O TYPE	DESCRIPTION	VCCIO (NOM) (V)	V_{IL} (2) (min) (V)	V_{IL} (MAX) (V)	V_{IH} (MIN) (V)	V_{IH} (3) (MAX) (V)	I_{IN} (4) (MAX) (µA)	V_{OH} (5) (MIN) (V)	V_{OL} (6) (MAX) (V)	I_{OH} (7) (MIN) (mA)	I_{OL} (8) (MIN) (mA)	ITS (9) (MAX) (µA)
I1	Input (STD)	1.8	–0.3	0.5	1.2	3	±10					
I2	Input (FLSH)	1.8	–0.3	0.5	1.2	3	±10					
		2.5	–0.3	0.7	1.7	3.6	±10					
		3.3	–0.3	0.8	2	3.6	±10					
I3	Input (INTF)	1.8	–0.3	0.5	1.2	3	±10					
		2.5	–0.3	0.7	1.7	3.6	±10					
		3.3	–0.3	0.8	2	3.6	±10					
I4	Input (REFCLK)	1.8	–0.3	0.5	1.2	3	±10					
O14	1× output (STD/ REFCLK)	1.8						1.25	0.4	2.58	2.89	±10
O24	1× output (FLSH)	1.8						1.25	0.4	2.58	2.89	±10
		2.5						1.7	0.7	6.2	6.3	±10
		3.3						2.4	0.4	5.29	9.38	±10
O58	2× output (DMD)	1.8						1.25	0.4	6.41	5.78	±10
O64(10)	1× output (MEM)	1.8						1.53	0.19	4	4	±10
O74(10)	1× output (MEM DIFF)(11)	1.8						1.53	0.19	4	4	±10
B14	1× bidirectional (STD) output	1.8	–0.3	0.5	1.2	3	±10	1.25	0.4	2.58	2.89	±10
B18(12)	2× bidirectional (STD) output	1.8	–0.3	0.5	1.2	3	±10	1.25	0.4	5.15	5.72	±10
B34	1× bidirectional (INTF) output	1.8	–0.3	0.5	1.2	3	±10	1.25	0.4	2.58	2.89	±10
		2.5	–0.3	0.7	1.7	3.6	±10	1.7	0.7	6.2	6.3	±10
		3.3	–0.3	0.8	2	3.6	±10	2.4	0.4	5.29	9.38	±10
B38	2× bidirectional (INTF) output	1.8	–0.3	0.5	1.2	3	±10	2.4	0.4	5.15	5.72	±10
		2.5	–0.3	0.7	1.7	3.6	±10	1.7	0.7	12.4	12.7	±10
		3.3	–0.3	0.8	2.0	3.6	±10	1.25	0.4	10.57	18.68	±10
B64(10)	1× bidirectional (MEM) output	1.8	–0.3	0.57	1.19	2.2	±10	1.53	0.19	4	4	±10

(1) Pin PLL_REFCLK_I is a crystal oscillator input pin and is not tested during VIH/VIL testing.
(2) VIL(min) is the absolute minimum voltage that can safely be applied to each corresponding pin.
(3) VOH(max) is the maximum voltage that can safely be applied to each corresponding pin.
(4) Input leakage current with no internal pullup or pulldown. V_{IN} = 0 or V_{IN} = VCCIO where VCCIO = I/O supply voltage
(5) I_{OH} = – rated current
(6) I_{OL} = + rated current
(7) V_{OH} = VOH(max)
(8) V_{OL} = VOL(max)
(9) Tri-state output leakage current. V_{IN} = 0 or V_{IN} = VCCIO where VCCIO = I/O supply voltage
(10) O64, O74, and B64 buffers are tested to only 100 µA for IOH/IOL due to tester limitations.
(11) The O74 mDDR differential clock (CK) output is simply a pair of single-ended drivers driven by a true and complementary signal.
(12) B18 buffers are not tested for I_{IH}.

6.7 Internal Pullup and Pulldown Characteristics

The resistance depends on the supply voltage level applied to the I/O.(1) (2)

	VCCIO (V)	MIN	MAX	UNIT
Weak pullup resistance	3.3	N/A	N/A	kΩ
	2.5	33	89	
	1.8	50.3	157.3	
Weak pulldown resistance	3.3	17.8	79.6	kΩ
	2.5	37	109	
	1.8	51.8	184.1	

(1) The description column of identifies whether the corresponding signal includes an internal pullup or pulldown resistor.
(2) Due to tester limitations, only the 1.8-V pullup resistors are measured and no pulldown resistors are measured.

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6.8 Parallel I/F Frame Timing Requirements

			MIN	MAX	UNIT
t_{p_vsw}	Pulse duration – VSYNC_WE high	50% reference points	1		lines
t_{p_vbp}	Vertical back porch – Time from the leading edge of VSYNC_WE to the leading edge HSYNC_CS for the first active line.(1)	50% reference points	2		lines
t_{p_vfp}	Vertical front porch – Time from the leading edge of the HSYNC_CS following the last active line in a frame to the leading edge of VSYNC_WE.(1)	50% reference points	1		lines
t_{p_tvb}	Total vertical blanking – Time from the leading edge of HSYNC_CS following the last active line of one frame to the leading edge of HSYNC_CS for the first active line in the next frame. This is equal to the sum of Vertical back porch (t_{p_vbp}) + Vertical front porch (t_{p_vfp}).	50% reference points	12		lines
t_{p_hsw}	Pulse duration – HSYNC_CS high	50% reference points	4	128	PCLKs
t_{p_hbp}	Horizontal back porch – Time from rising edge of HSYNC_CS to rising edge of DATAEN_CMD.	50% reference points	4		PCLKs
t_{p_hfp}	Horizontal front porch – Time from falling edge of DATAEN_CMD to rising edge of HSYNC_CS.	50% reference points	8		PCLKs
t_{p_thh}	Total horizontal blanking – Sum of horizontal front and back porches	50% reference points			(2)PCLKs

(1) The programmable parameter vertical sync line delay (I^2C: 0x23) must be set such that:
6 – Vertical front porch (t_{p_vfp})' (min 0) ≤ Vertical sync line delay ≤ Vertical back porch ($tp_{_vbp}$) – 2 (max 15). The default value for vertical sync line delay is set to 5; thus, only a vertical back porch less than 7 requires potential action.

(2) Total horizontal blanking is driven by the max line rate for a given source, which is a function of resolution and orientation. See *Parallel I/F Maximum Parallel Interface Horizontal Line Rate* for max line rate for each source and display combination. t_{p_thb} = Roundup [(1000 x f_{clock})/ LR] – APPL where f_{clock} = Pixel clock rate in MHz, LR = Line rate in kHz, and the number of active pixels per (horizontal) line is APPL. If t_{p_thb} is calculated to be less than t_{p_hbp} + t_{p_hfp}, then the pixel clock rate is too low, or the line rate is too high, and one or both must be adjusted.

6.9 Parallel I/F General Timing Requirements

			MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK		1	33.5	MHz
t_{p_clkper}	Clock period, PCLK	50% reference points	29.85	1000	ns
t_{p_clkjit}	Clock jitter, PCLK	Max f_{clock}	(1)	(1)	
t_{p_wh}	Pulse-duration low, PCLK	50% reference points	10		ns
t_{p_wl}	Pulse-duration high, PCLK	50% reference points	10		ns
t_{p_su}	Setup time – HSYNC_CS, DATEN_CMD, PDATA (23:0) valid before the active edge of PCLK (2)	50% reference points	3		ns
t_{p_h}	Hold time – HSYNC_CS, DATEN_CMD, PDATA (23:0) valid after the active edge of PCLK (2)	50% reference points	3		ns
t_t	Transition time – All signals	20% to 80% reference points	0.2	4	ns

(1) Clock jitter (in ns) should be calculated using this formula: Jitter = (1 / f_{clock} – 28.35 ns). Setup and hold times must be met during clock jitter.

(2) See Figure 2.

6.10 Parallel I/F Maximum Parallel Interface Horizontal Line Rate

DMD	PARALLEL BUS SOURCE	LANDSCAPE FORMAT		PORTRAIT FORMAT	
		RESOLUTION (H×V)	MAX LINE RATE (kHz)	RESOLUTION (HxV)	MAX LINE RATE (kHz)
0.3 WVGA and 0.24 VGA diamond	NSTC (1)	720 × 240 (2)	17	Not supported	N/A
	PAL (1)	720 × 288 (2)	20	Not supported	N/A
	QVGA	320 × 240 (2)	17	240 × 320 (2)	22
	QWVGA	427 × 240 (2)	17	240 × 427 (2)	27
	nHD	640 × 360 (2)	25	360 × 640 (2)	42
	3:2 VGA	640 × 430 (2)	30	430 × 640 (2)	45
	4:3 VGA	640 × 480 (2)	34	480 × 640 (2)	45
	WVGA-720	720 × 480 (2)	34	480 × 720 (2)	51
	WVGA-752	752 × 480 (2)	34	480 × 752 (2)	53
	WVGA-800	800 × 480 (2)	34	480 × 800 (2)	56
	WVGA-852	852 × 480 (2)	34	480 × 852 (2)	56
	WVGA-853	853 × 480 (2)	34	480 × 853 (2)	56
	WVGA-854	854 × 480 (2)	34	480 × 854 (2)	56
	WVGA-864	864 × 480 (2)	34	480 × 864 (2)	56
0.2 nHD Manhattan	NSTC (1)	720 × 240 (2)	32	Not supported	N/A
	PAL (1)	720 × 288 (2)	39	Not supported	N/A
	QVGA	320 × 240	32	240 × 320 (2)	42
	QWVGA	427 × 240	32	240 × 427 (2)	52
	nHD	640 × 360	48	360 × 640 (2)	79
	3:2 VGA	640 × 430 (2)	50	430 × 640 (2)	74
	4:3 VGA	640 × 480 (2)	50	480 × 640 (2)	66
	WVGA-720	720 × 480 (2)	44	480 × 720 (2)	66
	WVGA-752	752 × 480 (2)	42	480 × 752 (2)	66
	WVGA-800	800 × 480 (2)	40	480 × 800 (2)	66
	WVGA-852	852 × 480 (2)	37	480 × 852 (2)	66
	WVGA-853	853 × 480 (2)	37	480 × 853 (2)	66
	WVGA-854	854 × 480 (2)	37	480 × 854 (2)	66
	WVGA-864	864 × 480 (2)	37	480 × 864 (2)	66

(1) NTSC and PAL are assumed to be interlaced sources
(2) Not supported for 100- to 120-Hz operation

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6.11 BT.656 I/F General Timing Requirements

The DLPC2607 ASIC input interface supports the industry standard BT.656 parallel video interface. See the appropriate ITU-R BT.656 specification for detailed interface timing requirements. Map the BT.656 data bits to the DLPC2607 PDATA bus as shown in Figure 3. (1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK		1	33.5	MHz
t_{p_clkper}	Clock period, PCLK	50% reference points	29.85	1000	ns
t_{p_clkjit}	Clock jitter, PCLK (2)	Maximum f_{clock}	(2)	(2)	
t_{p_wh}	Pulse duration low, PCLK	50% reference points	10		ns
t_{p_wl}	Pulse duration high, PCLK	50% reference points	10		ns
t_{p_su}	Setup time – HSYNC, DATEN, PDATA(23:0) valid before the active edge of PCLK	50% reference points	3		ns
t_{p_h}	Hold time – HSYNC, DATEN, PDATA(23:0) valid after the active edge of PCLK	50% reference points	3		ns
t_t	Transition time – All signals	20% to 80% reference points	0.2	4	ns

(1) The BT.656 I/F accepts 8-bit per color, 4:2:2 YCb/Cr data encoded per the industry standard though PDATA(7:0) on the active edge of PCLK (that is, programmable) as shown in Figure 2.
(2) Clock jitter should be calculated using this formula: Jitter = (1 / f_{clock} – 28.35 ns). Setup and hold times must be met during clock jitter.

6.12 100- to 120-Hz Operational Limitations

The table below assumes that a front-end device ahead of the DLPC2607 device converts all 3-D sources to the 3-D format defined previously and provides any needed left-eye or right-eye selection control directly to the 3-D glasses (that is, the DLPC2607 device does not control the glasses). The DLPC2607 device includes a double buffer frame memory, which causes the displayed image to be delayed one frame relative to its input. This requires left or right eye-frame shutter control to be inverted prior to being sent to the glasses.

SOURCE	RESOLUTION (APPL x ALPF)	MIN FRAME RATE (Hz)	NOM FRAME RATE (Hz)	MAX FRAME RATE (Hz)	MIN TVB (tp_tvb) (LINES)	MAX LINE RATE (kHz)	MIN LINE RATE (kHz)	MIN CLOCK RATE (MHz)
nHD	640 × 360	99	100	101	12	48	(1)	(2)
WQVGA	427 × 240	99	100	101	12	32	(1)	(2)
QVGA	320 × 240	99	100	101	12	32	(1)	(2)
nHD	640 × 360	118.8	120	121.2	12	48	(1)	(2)
WQVGA	427 × 240	118.8	120	121.2	12	32	(1)	(2)
QVGA	320 × 240	118.8	120	121.2	12	32	(1)	(2)

(1) Use the following equation to determine the minimum line rate for a given application. The application cannot be supported if the calculated minimum line rate exceeds the maximum line rate defined elsewhere in this table;
Line_Rate_min (kHz) = Frame_Rate_max (Hz) × [ALPF + TVB] /1000
Where: TVB = Total vertical blanking (in lines)
ALPF = Active lines per frame
Frame_Rate_max = Max frame rate including all expected wander
(2) The following equation should be used to determine the minimum pixel clock rate for a given application. The application cannot be supported if the calculated minimum pixel clock rate exceeds the max pixel clock rate defined in *Parallel I/F General Timing Requirements*.
Pixel_Clock_min (MHz) = Line_Rate_max (kHz) × (APPL + 12) / 1000
Where: APPL = Active pixels per line
Line_Rate_max = Max line rate including all expected wander

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6.13 Flash Interface Timing Requirements

The DLPC2607 ASIC flash memory interface consists of a SPI flash serial interface at 33.3 MHz (nominal). (1) (2)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, SPI_CLK (3)		33.3266	33.34	MHz
t_{p_clkper}	Clock period, SPI_CLK	50% reference points	29.994	30.006	ns
t_{p_wh}	Pulse duration low, SPI_CLK	50% reference points	10		ns
t_{p_wl}	Pulse duration high, SPI_CLK	50% reference points	10		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	4	ns
t_{p_su}	Setup time – SPI_DIN valid before SPI_CLK falling edge	50% reference points	10		ns
t_{p_h}	Hold time – SPI_DIN valid after SPI_CLK falling edge	50% reference points	0		ns
t_{p_clqv}	SP_ICLK clock low to output valid time – SPIDOUT and SPI_CSZ	50% reference points		1	ns
t_{p_clqx}	SPI_CLK clock low output hold time – SPI_DOUT and SPI_CSZ	50% reference points	–1		ns

(1) Standard SPI protocol is to transmit data on the falling edge of SPI_CLK and capture data on the rising edge. The DLPC2607 device does transmit data on the falling edge, but it captures data on the falling edge rather than the rising edge. This provides support for SPI devices with long clock-to-Q timing. The DLPC2607 device hold capture timing is set to facilitate reliable operation with standard external SPI protocol devices.
(2) With the above output timing, the DLPC2607 device provides the external SPI device 14-ns input set-up and 14-ns input hold relative to the rising edge of SPI_CLK.
(3) This range includes the 200 ppm of the external oscillator (but no jitter).

6.14 DMD Interface Timing Requirements

The DLPC2607 ASIC DMD interface consists of a 76.19-MHz (nominal) DDR output-only interface with LVCMOS signaling. (see (1))

			MIN	MAX	UNIT
f_{clock}	Clock frequency, DMD_DCLK and DMD_SAC_CLK (2)		76.175	76.206	MHz
t_{p_clkper}	Clock period, DMD_DCLK and DMD_SAC_CLK	50% reference points	13.122	13.128	ns
t_{p_wh}	Pulse duration low, DMD_DCLK and DMD_SAC_CLK	50% reference points	6.2		ns
t_{p_wl}	Pulse duration high, DMD_DCLK and DMD_SAC_CLK	50% reference points	6.2		ns
t_t	Transition time – all signals	20% to 80% reference points	0.3	2	ns
t_{p_su}	Output setup time – DMD_D(14:0), DMD_SCTRL, DMD_LOADB and DMD_TRC relative to both rising and falling edges of DMD_DCLK (3) (4)	50% reference points		1.5	ns
t_{p_h}	Output hold time – DMD_D(14:0), DMD_SCTRL,DMD_LOADB and DMD_TRC signals relative to both rising and falling edges of DMD_DCLK (3) (4)	50% reference points		1.5	ns
$t_{p_d1_skew}$	DMD data skew – DMD_D(14:0), DMD_SCTRL, DMD_LOADB, and DMD_TRC signals relative to each other (5)	50% reference points		0.2	ns
$t_{p_clk_skew}$	Clock skew – DMD_DCLK and DMD_SAC_CLK relative to each other	50% reference points		0.2	ns
$t_{p_d2_skew}$	DAD/SAC data skew - DMD_SAC_BUS, DMD_DRC_OEZ (6), DMD_DRC_BUS, and DMD_DRC_STRB signals relative to DMD_SAC_CLK	50% reference points		0.2	ns

(1) Assumes a 30-Ω series termination for all DMD interface signals (except DAD_DMD_OEZ)
(2) This range includes the 200 ppm of the external oscillator (but no jitter).
(3) Assumes minimum DMD setup time = 1 ns and minimum DMD hold time = 1 ns
(4) Output setup and hold numbers already account for controller clock jitter. Only routing skew and DMD setup/hold must be considered in system timing analysis.
(5) Assumes DMD data routing skew = 0.1 ns max
(6) DMD_DAD_OEZ requires a 30- to 100-kΩ external pullup resistor connected to VCC18 to achieve proper timing.

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6.15 mDDR Memory Interface Timing Requirements

The DLPC2607 controller mDDR memory interface consists of a 16-bit wide, mDDR interface (that is, LVCMOS signaling) operated at 133.33 MHz (nominal). (see (1) (2) (3))

		MIN	MAX	UNIT
t_{CYCLE}	Cycle-time reference	7500		ps
t_{CH}	CK high pulse width(4)	2700		ps
t_{CL}	CK low pulse width(4)	2700		ps
t_{DQSH}	DQS high pulse width(4)	2700		ps
t_{DQSL}	DQS low pulse width(4)	2700		ps
t_{WAC}	CK to address and control outputs active	–2870	2870	ps
t_{QAC}	CK to DQS output active		200	ps
t_{DAC}	DQS to DQ and DM output active	–1225	1225	ps
t_{DQSRS}	Input (read) DQS and DQ skew(5)		1000	ps

(1) This includes the 200 ppm of the external oscillator (but no jitter).
(2) Output setup and hold numbers already account for controller clock jitter. Only routing skew and memory setup/hold must be considered in system timing analysis.
(3) Assumes a 30-Ω series termination on all signal lines.
(4) CK and DQS pulse duration specifications for the DLPC2607 assume it is interfacing to a 166-MHz mDDR device. Even though these memories are only operated at 133.33 MHz, according to memory vendors, the rated t_{CK} specification (that is 6 ns) can be applied to determine minimum CK and DQS pulse duration requirements to the memory.
(5) Note that DQS must be within the t_{DQSRS} read data-skew window, but need not be centered.

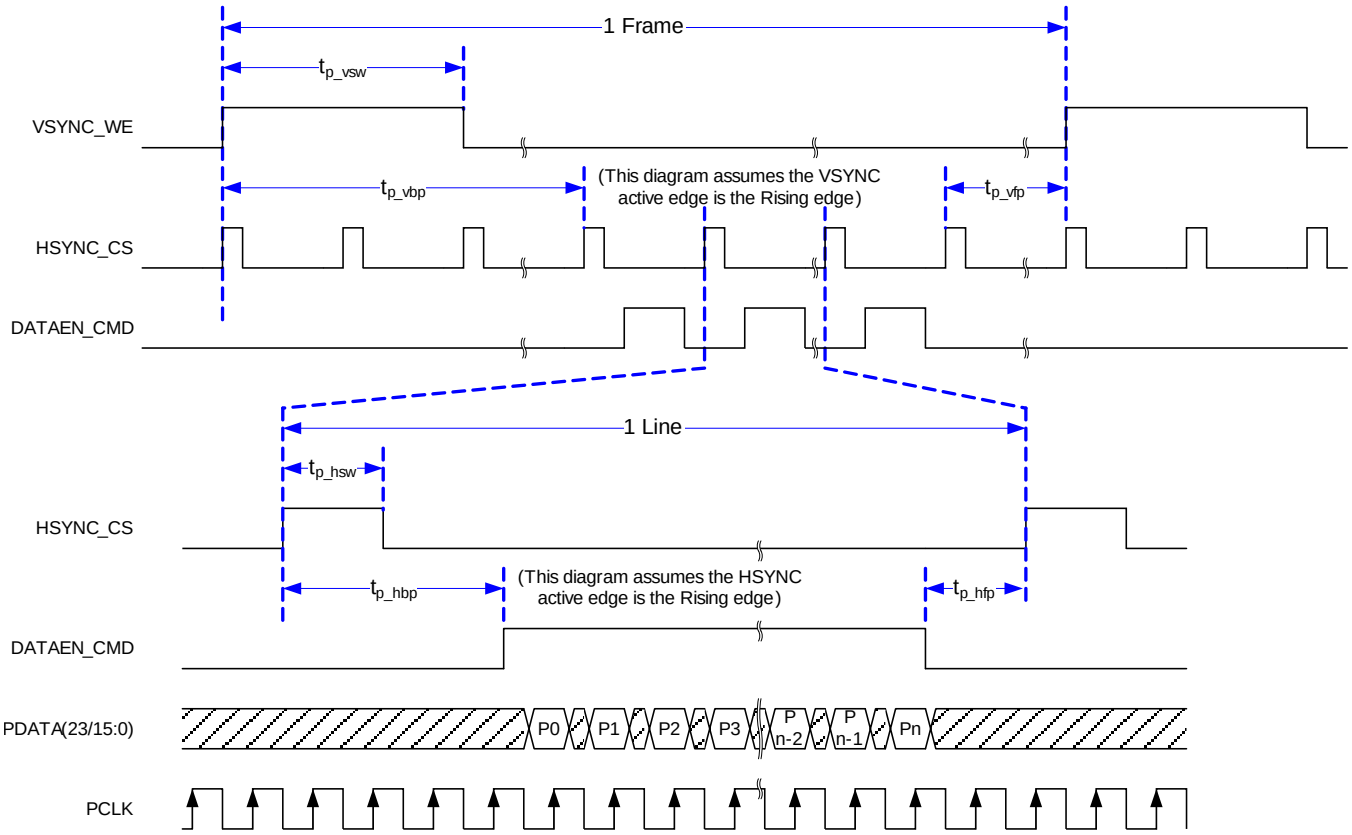

Figure 1. Parallel I/F Frame Timing

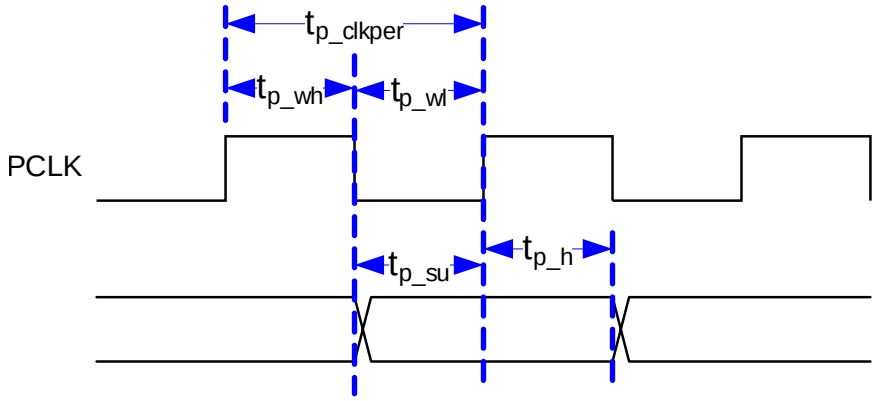

Figure 2. Parallel and BT.656 I/F General Timing

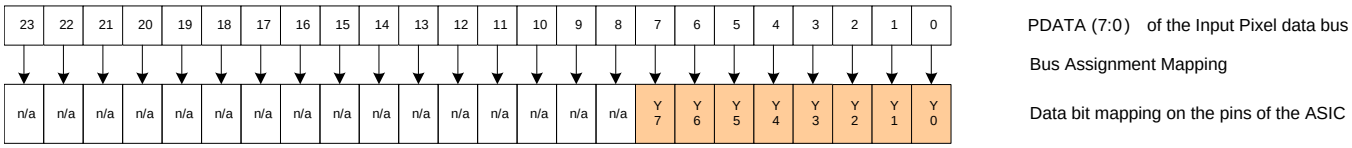

Figure 3. DLPC2607 PDATA Bus – BT.656 I/F Mode Bit Mapping (YCrCb 4:2:2 Source)

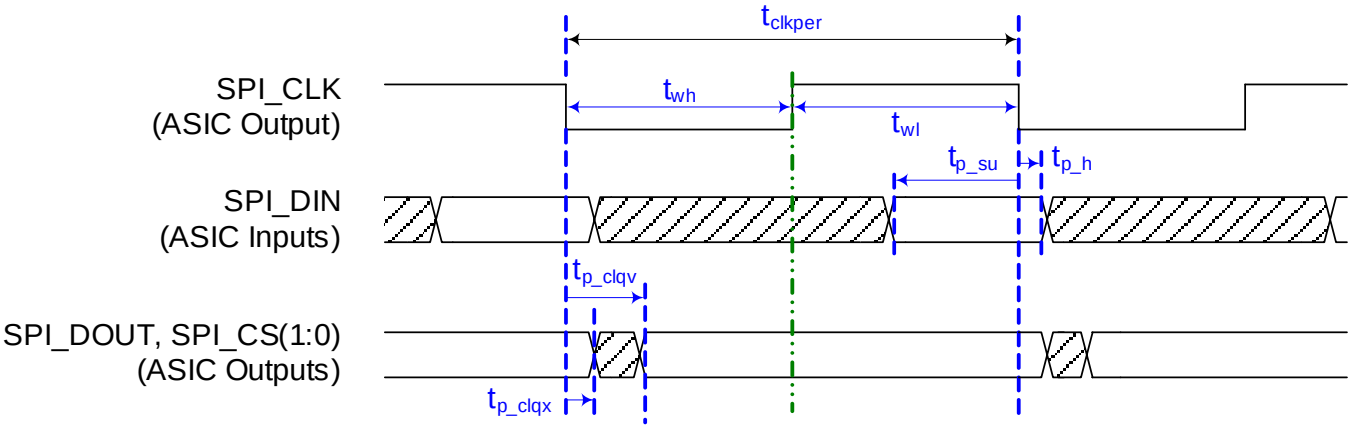

Figure 4. Flash I/F Timing

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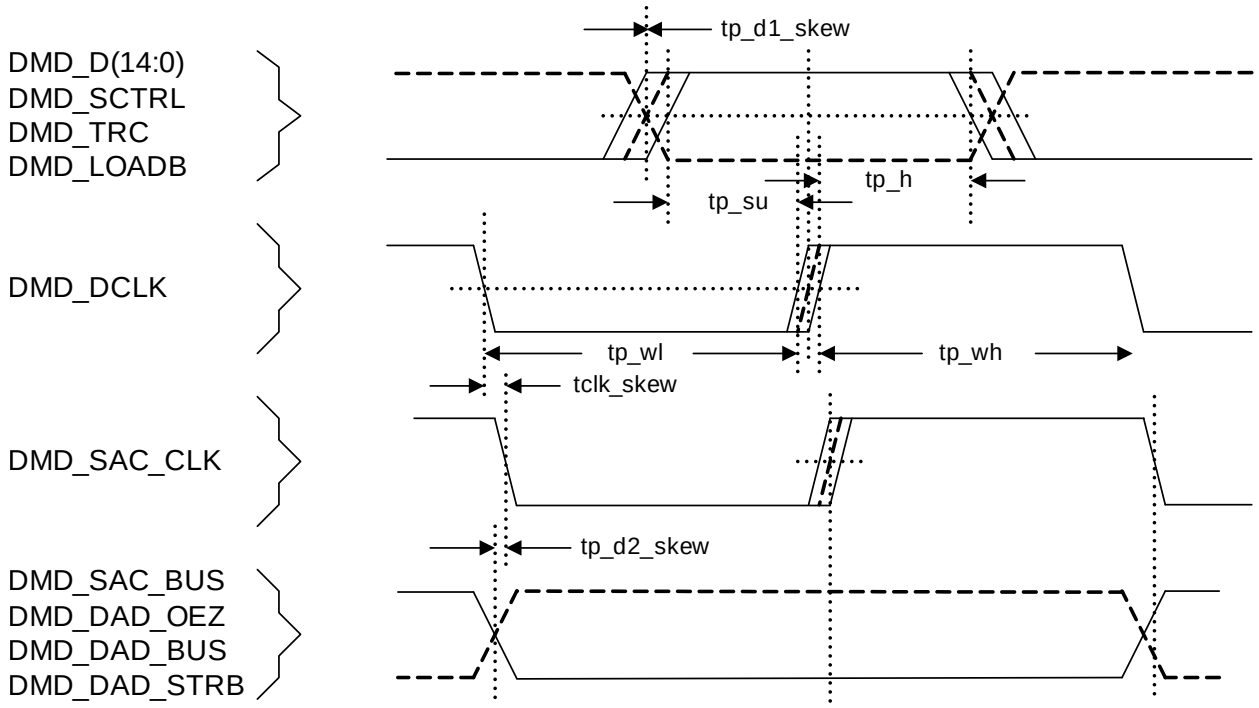

Figure 5. DMD I/F Timing

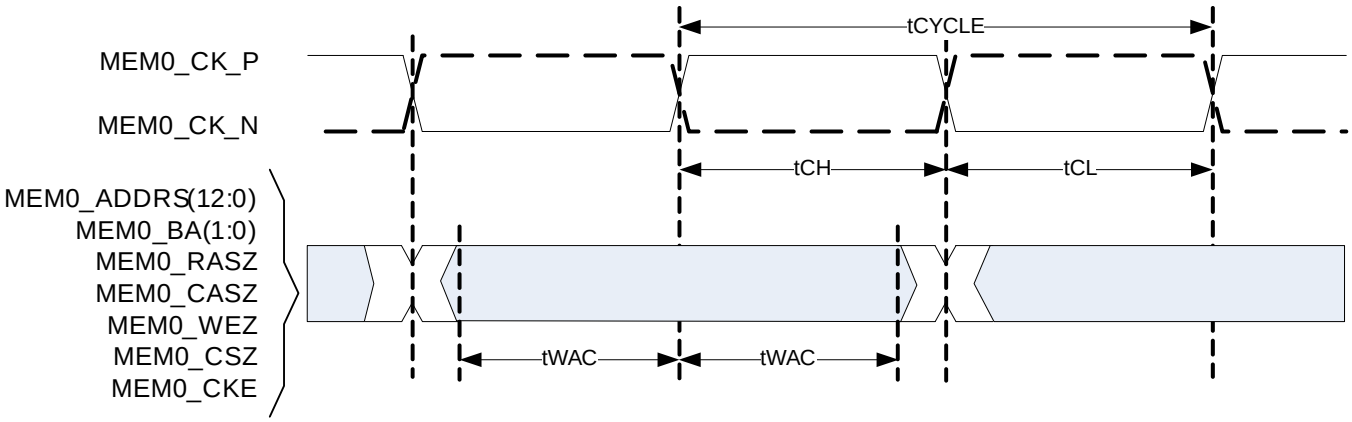

Figure 6. mDRR Memory Address and Control Timing

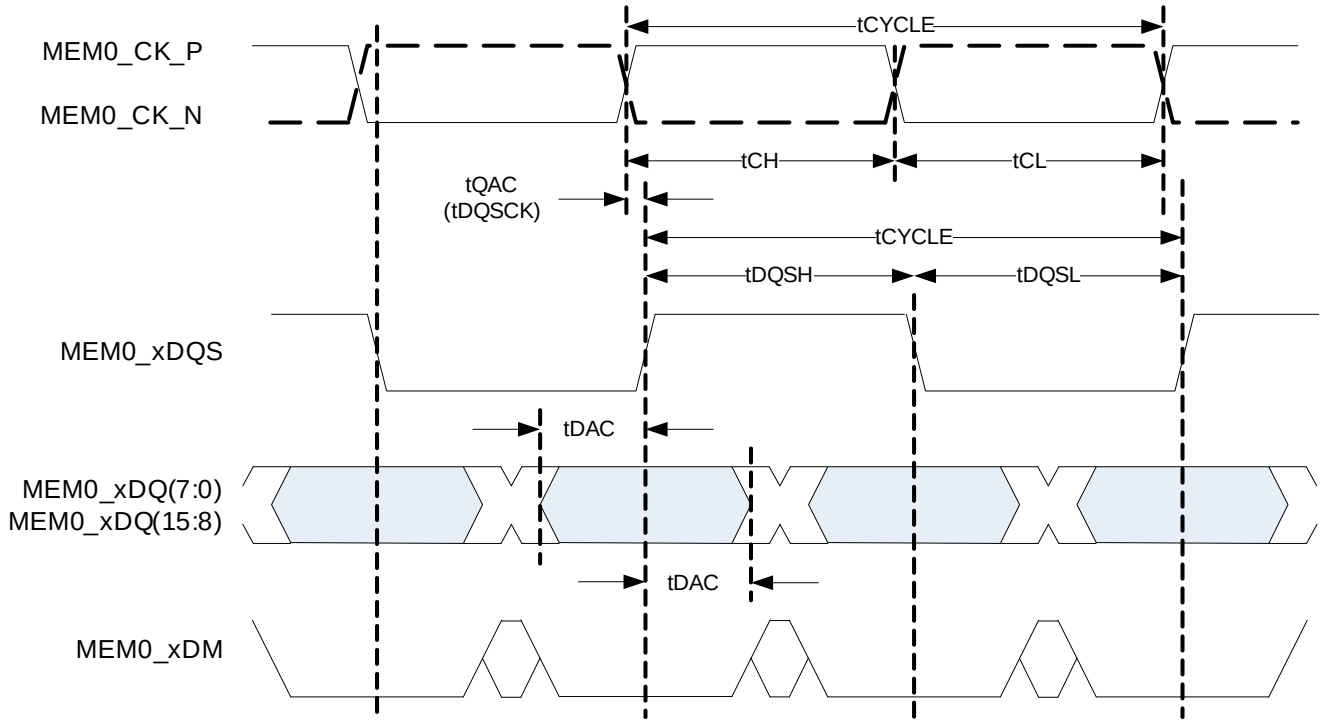

Figure 7. mDRR Memory Write Dtat Timing

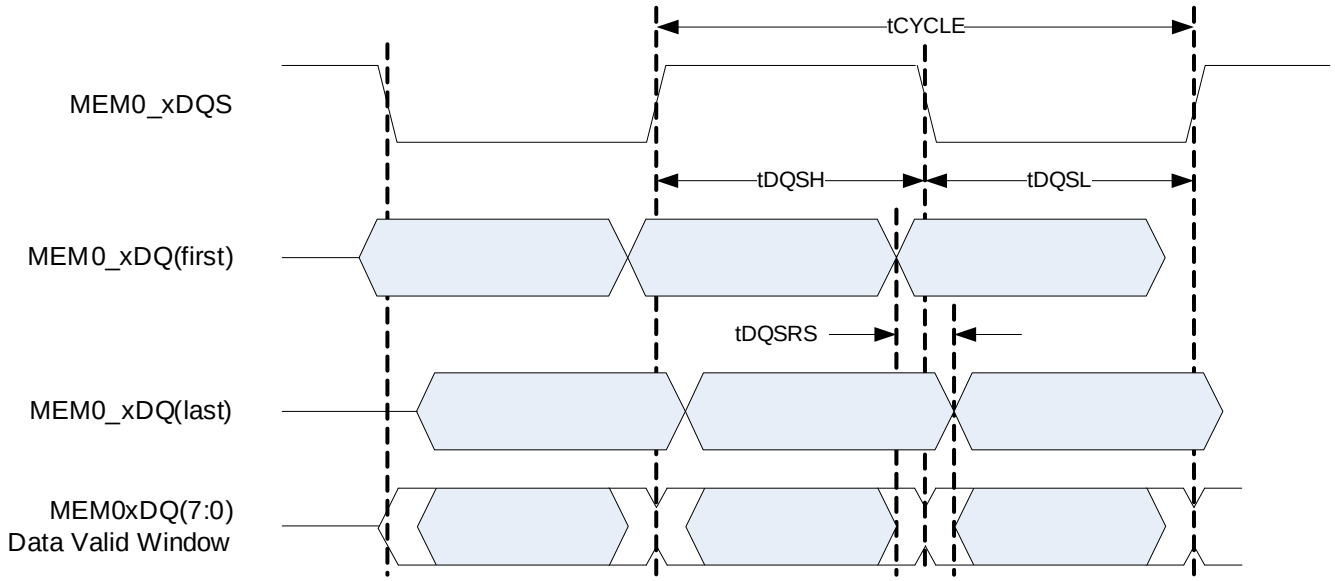

Figure 8. mDDR Memory Read Data Timing

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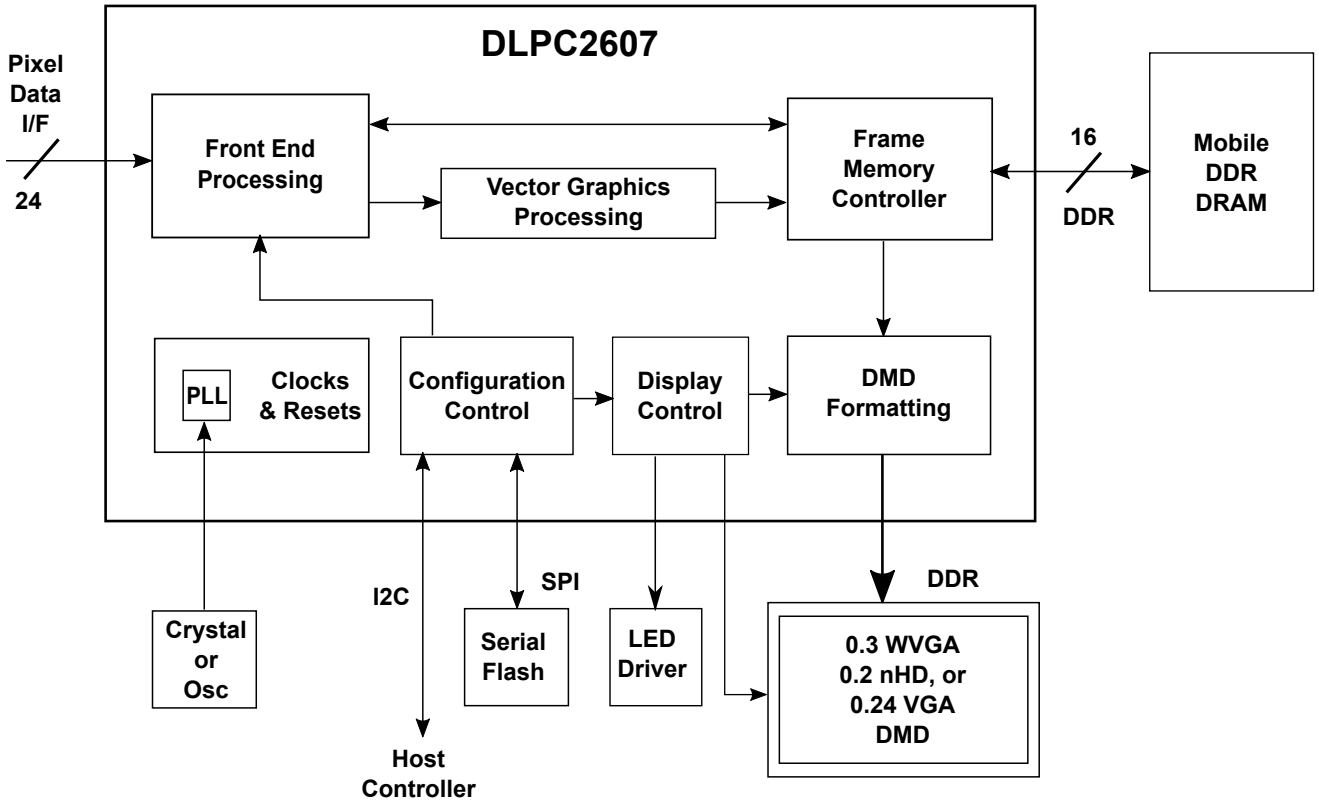
7 Detailed Description

7.1 Overview

The DLPC2607 is the display controller for the 0.3-WVGA, 0.24-VGA and 0.2-nHD DMDs. Both the controller and the DMD must be used in conjunction with each other for reliable operation of the DMD. The DLPC2607 display controller provides interfaces and data/image processing functions that are optimized for small form factor and low power display applications. Applications include pico projectors, smart projectors, screen less display, interactive display, wearable displays and many more. In typical systems a separate applications processor is used to provide various multimedia functionality (such as video decoder, HDMI receiver, VGA, SD card, or USB I/F chip).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Parallel Bus Interface

The parallel bus interface complies with standard graphics interface protocol, which includes a vertical sync signal (VSYNC_WE), horizontal sync signal (HSYNC_CS), optional data valid signal (DATAEN_CMD), a 24-bit data bus (PDATA), and a pixel clock (PCLK). The user can program the polarity of both syncs and the active edge of the clock. Figure 1 shows the relationship of these signals. The data valid signal (DATAEN_CMD) is optional in that the DLPC2607 device provides auto-framing parameters that can be programmed to define the data valid window based on pixel and line counting relative to the horizontal and vertical syncs.

Feature Description (continued)

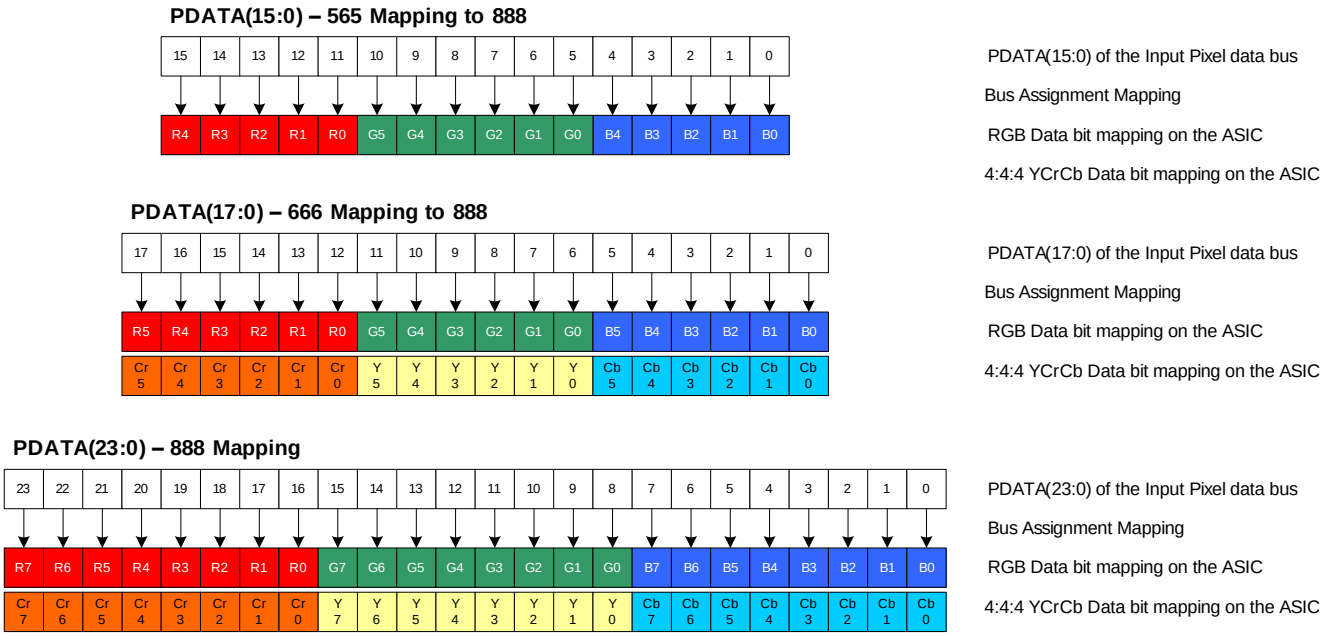
In addition to these standard signals, an optional side-band signal (PDM_CVS_TE) is available, which allows the user to stop the periodic frame updates without losing the displayed image. When PDM_CVS_TE is active, it acts as a data mask and does not allow the source image to be propagated to the display. A programmable PDM polarity parameter determines if it is active high or active low. This parameter defaults to make PDM_CVS_TE active high. Therefore, if this function is not desired, tie it to a logic low on the PCB. PDM_CVS_TE is restricted to change only during vertical blanking. Note that VSYNC_WE must remain active at all times (in Lock-to-VSYNC mode) or the display sequencer stops and causes the LEDs to be shut off.

The parallel bus interface supports six data transfer formats:

- 16-bit RGB565
- 18-bit RGB666
- 18-bit 4:4:4 YCrCb666
- 24-bit RGB888
- 24-bit 4:4:4 YCrCb888
- 16-bit 4:2:2 YCrCb (standard sampling assumed to be Y0Cb0, Y1Cr0, Y2Cb2, Y3Cr2, Y4Cb4, Y5Cr4, …)

Figure 9 shows the required PDATA(23:0) bus mapping for these six data transfer formats.

Parallel Bus Mode – 4:4:4 RGB and YCrCb Sources



Parallel Bus Mode - 16-bit YCrCb 4:2:2 Source

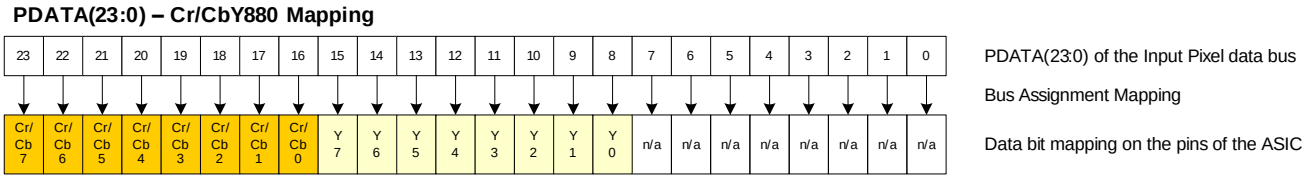


Figure 9. PDATA Bus – Parallel I/F Mode Bit Mapping

7.3.2 100- to 120-Hz 3-D Display Operation

The DLPC2607 device supports 100- to 120-Hz 3-D display operation, but is limited to a narrow set of configurations. 3-D operation is limited to:

- 0.2-nHD DMDs only

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Feature Description (continued)

- nHD, WQVGA and QVGA source resolutions
- Parallel bus interface only (all pixel formats are supported)
- Landscape source and display orientation only
- Non-interlaced video-graphics only
- 100-Hz ±1% or 120-Hz ±1% source frame rates
- Unpacked, full resolution, frame sequential, 3-D format (that is each 100- or 120-Hz source frame contains a single, full resolution, eye frame separated by VSYNCs, where an eye frame contains image data for a single left or right eye; not both)
- Minimum line rates that satisfy the high frame rates

To support 3-D operation, run the DLPC2607 device in Lock-to-VSYNC mode with 1× frame rate multiplication (that is, no frame rate multiplication). Each DMD frame is displayed at the source frame rate in the order it is received.

Because of the high frame rate of the source, the source line rate must be much higher than typical, but still cannot exceed the rates defined in *Parallel I/F Maximum Parallel Interface Horizontal Line Rate*. The minimum line rate is limited by the maximum frame rate and minimum total vertical blanking (TVB). *100- to 120-Hz Operational Limitations* provides a summary of the line rate range assuming the minimum TVB.

7.4 Programming

7.4.1 Serial Flash Interface

The DLPC2607 device uses an external SPI serial flash memory device for configuration support. The minimum required size depends on the desired minimum number of sequences, CMT tables, and splash options while the maximum supported is 16 Mb. Table 1 provides the list of the configuration options.

Table 1. Serial Flash Support Features by Density(1)

TARGET FLASH DENSITY (Mb)	QUANTITY OF FEATURES THAT CAN BE SUPPORTED						
	OPTICAL TEST SPLASH SCREENS	STANDARD SPLASH SCREENS	SERIES DATA SECTOR	UNIT DATA SECTOR	ODM DATA SECTOR	DLP DISPLAY SEQUENCES (2)	CMT TABLES PER SEQUENCE (3)
4 Mb	0	1	1	1	1	16	7
8 Mb	0	3	1	1	1	16	7
16 Mb	1	4	1	1	1	16	7

(1) All rows in this table have passed DVT at TI.
(2) Assumes individual DLP display sequences are limited to 5 KB each
(3) An equal number of CMT tables are required for each sequence (CMT tables define the DeGamma Curve). The DLPC2607 device uses a single SPI, employing SPI mode 0 protocol, operating at a frequency of 33.3 MHz. It supports two independent SPI chip selects. However, the primary flash must be connected to SPI chip select 0 (SPICS0) because the auto-initialization routine is always executed from the device connected to this chip select. The auto-initialization routine executed from flash consists of the following:
(a) The DLPC2607 device first uploads the size and location of the auto-initialization routine from address range 0x0000 through 0x0007 of the serial flash memory connected to SPICS0.
(b) The DLPC2607 device then uploads the actual auto-initialization routine to its ICP program memory from the serial flash memory connected to SPICS0.
(c) The DLPC2607 device then executes an auto-init routine, which includes uploading default control parameter values, uploading mailbox memory contents, turning on the sequence and LEDs, and then enabling the display.
(d) Upon completion of the auto-initialization routine, the DLPC2607 signals INIT DONE with GPIO4_INTF.

The DLPC2607 device supports any flash device that is compatible with these modes of operation. However, the DLPC2607 device does not support the Normal (slow) Read Opcode, and thus cannot automatically adapt protocol and clock rate based on the flash's electronic signature ID. The flash instead uses a fixed SPI clock and assumes certain attributes of the flash have been ensured by PCB design. The DLPC2607 device also assumes the flash supports address auto-incrementing for all read operations. Table 2 and Table 3 list the specific instruction OpCode and timing compatibility requirements for a DLPC2607 device compatible flash.

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Table 2. SPI Flash Instruction OpCode and Timing Compatibility Requirements

SPI FLASH COMMAND	OPCODE (hex)	ADDRESS BYTES	DUMMY BYTES	MIN CLOCK RATE
Fast READ (single output)	0x0B	3	1	33.3 MHz
All others	Can vary	Can vary	Can vary	33.3 MHz

Table 3. SPI Flash Key Timing Parameter Compatibility Requirements

	MIN	MAX	UNIT
Minimum chip select high time		300	ns
Minimum output hold time	0		ns
Maximum output valid time		9	ns
Minimum data in setup time		5	ns
Minimum data in hold time		5	ns

The DLPC2607 device does not have any specific page, block, or sector size requirements, except that programming with the I^2C interface requires the use of page mode programming. However, if the user would like to use a portion of the serial flash for storing external data (such as calibration data) with the I^2C interface, then the minimum sector size must be considered as it drives minimum erase size. Note that use of serial flash for storing external data may impact the number of features that can be supported.

NOTE

The DLPC2607 device does not drive the $\overline{\text{HOLD}}$ (active low hold) or $\overline{\text{WP}}$ (active low write protect) pins on the flash device. Tie these pins to a logic high on the PCB with an external pullup.

The DLPC2607 device supports 1.8 V, 2.5 V, or 3.3 V serial flash devices. Some suggested devices would include the W25Q16DWSSIG or MX25U4035. If a different flash device is used, Table 4 lists the minimum performance specifications necessary.

Table 4. Specifications of Compatible SPI Serial Flash Devices

SPI Flash Timing Parameter	MIN	MAX
Minimum Chip Select High Time		300ns
Minimum Output Hold Time	0ns	
Maximum Output Valid Time		9ns
Minimum Data in Setup Time		5ns
Minimum Data in Hold Time		5ns
Minimum Clock Rate	33.3MHz	

7.4.2 Serial Flash Programming

The flash can be programmed through the DLPC2607 device over I^2C (for directions, see the *DLPC2607 Software Programmer's Guide*, DLPU013) or by driving the SPI pins of the flash directly while the DLPC2607 device I/O are tri-stated. SPICLK, SPIDOUT, and SPICZ0 I/O can be tri-stated by holding $\overline{\text{RESET}}$ in a logic-low state while power is applied. Note that SPICSZ1 is not tri-stated by this same action.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DLPC2607 controller supports reliable operation of .3-WVGA, .24-VGA and .2-nHD DMDs and must be always used with the DMD to provide a reliable display solution for various data and video display applications. The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC2607. Applications of interest include accessory projectors, projectors embedded in display devices like notebooks, laptops, tablets, and set top box. Other applications include wearable (near-eye or head mounted) displays, interactive display and low latency gaming display.

8.2 Typical Application

Figure 10 shows a typical accessory projector application. For this application, the DLPC2607 device is controlled by a separate control processor (typically a MSP430) and the image data is received from a TVP5151 video decoder device. For this application, the ASIC supports periodic sources only. A common application when using DLPC2607 controller is for creating an accessory Pico projector for a smartphone, tablets or any other display source. The DLPC2607 in the accessory Pico projector typically receives images from a host processor or a multimedia processor.

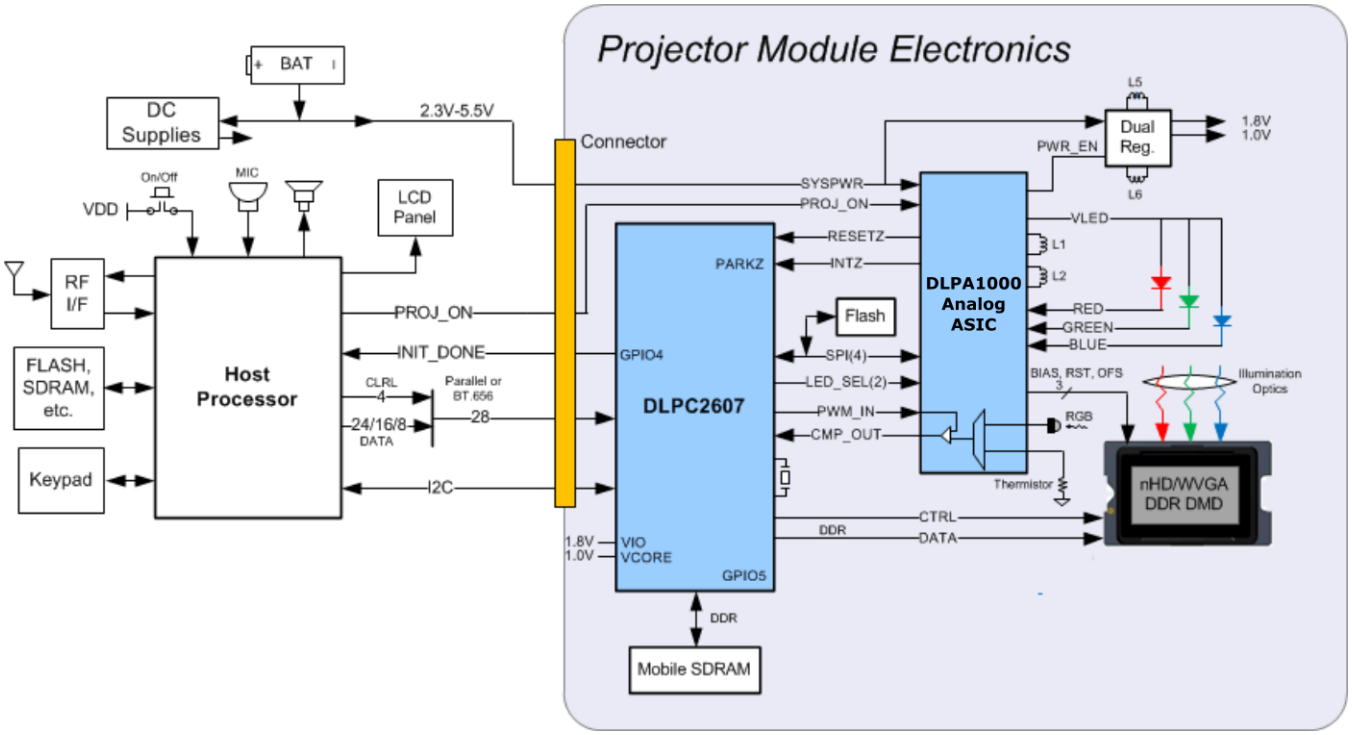

Figure 10. Typical Standalone Projector System Block Diagram

8.2.1 System Functional Modes

The application system has two functional modes (ON/OFF) controlled by a single pin PROJ_ON:

- When pin PROJ_ON is set high, the projector automatically powers up and an image is projected from the

Typical Application (continued)

DMD.

- When pin PROJ_ON is set low, the projector automatically powers down to save power.

8.2.2 Design Requirements

8.2.2.1 Reference Clock

The device requires an external reference clock to feed its internal PLL. This reference may be supplied by a crystal or oscillator. For flexibility, the DLPC2607 device accepts either of two reference clock frequencies (see Table 5), but both must have a maximum frequency variation of 200 ppm (including aging, temperature, and trim component variation). When a crystal is used, the configuration requires several discrete components, as shown in Figure 11.

CL = Crystal load capacitance (Farads)

CL1 = 2 x (CL - Cstray_pll_refclk_i)

CL2 = 2 x (CL - Cstray_pll_refclk_o)

Where:

Cstray_pll_refclk_i = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin pll_refclk_i.

Cstray_pll_refclk_o = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin pll_refclk_o.

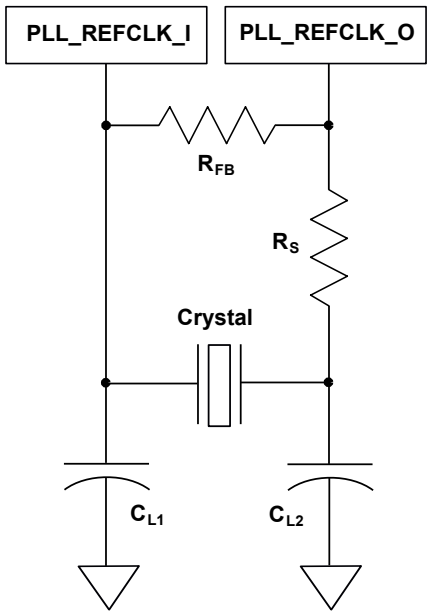

Figure 11. Recommended Crystal Oscillator Configuration

Table 5. Crystal Port Characteristics

PARAMETER	NOM	UNIT
PLL_REFCLK_I TO GND capacitance	4.5	pF
PLL_REFCLK_O TO GND capacitance	4.5	pF

Table 6. Recommended Crystal Configuration

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency (See TSTPT_6 in the Pin Functions table)	16.667 or 8.333	MHz
Crystal frequency tolerance (including accuracy, temperature, aging, and trim sensitivity)	±200	PPM
Crystal drive level	100 max	µW
Crystal equivalent series resistance (ESR)	80 max	Ω
Crystal load	12	pF
R_S drive resistor (nominal)	100	Ω
R_{FB} feedback resistor (nominal)	1	MΩ

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Table 6. Recommended Crystal Configuration (continued)

PARAMETER	RECOMMENDED	UNIT
C_{L1} external crystal load capacitor	See Figure 11	pF
C_{L2} external crystal load capacitor	See Figure 11	pF
PCB layout	TI recommends a ground isolation ring around the crystal	

If an external oscillator is used, then the oscillator output must drive the PLL_REFCLK_I pin on the DLPC2607 ASIC. Leave the PLL_REFCLK_O pins unconnected. An oscillator that provides a spread-spectrum clock reduces EMI.

NOTE

The DLPC2607 device accepts between 0% to –2% spreading (that is, down spreading only) with a modulation frequency between 20 kHz and 65 kHz and a triangular waveform.

Similar to the crystal option, the oscillator input frequency is limited to 16.667 or 8.333 MHz. To configure the DLPC2607 device to accept the 8.333-MHz reference clock option, an external pullup resistor to VCC18 must be applied to the TSTPT (6) pin. To configure the DLPC2607 device to accept the 16.667-MHz reference clock option, leave the TSTPT (6) pin unconnected.

It is assumed that the external crystal or oscillator stabilizes within 50 ms after stable power is applied.

8.2.2.2 mDDR DRAM Compatibility

The following are the basic SDRAM compatibility requirements for the DLPC2607 SDRAM:

- SDRAM memory type: mDDR
- Size: 128 Mb minimum
- Organization: N × 16-bits wide × 4 banks
- Speed grade t_{CK}: 6-ns max
- CAS latency (C_L), t_{RCD}, t_{RP} parameters (clocks): 3, 3, 3
- Burst length options to include: Burst of 4
- Refresh period (full device): ≥64 ms

The following mDDR DRAM devices are recommended for use with the DLPC2607 device:

Table 7. Compatible mDDR DRAM Device Options (1) (2)

DVT (3)	VENDOR	PART NUMBER	SIZE (Mb)	ORGANIZATION	SPEED GRADE t_{CK} (4) (ns)	C_L, t_{RCD}, t_{RP} (Clocks)
No	Elpida	EDK1216CFBJ-60-F (5)	128	8 M × 16	6	(3)
Yes	Elpida	EDD25163HBH-6ELS-F	256	16 M × 16	6	(3)
No	Samsung	K4X56163PL-FGC6 (6)	256	16 M × 16	6	(3)
Yes	Samsung	K4X56163PN-FGC6	256	16 M × 16	6	(3)
Yes	Micron	MT46H16M16LFBF-6IT:H	256	16 M × 16	6	(3)
Yes	Hynix	H5MS2562JFR-J3M	256	16 M × 16	6	(3)

(1) The DLPC2607 device does not use partial array self-refresh or temperature-compensated self-refresh options.
(2) These part numbers reflect Pb-free package.
(3) All these SDRAM devices appear compatible with the DLPC2607 device, but only those marked with 'yes' in the DVT column have been validated on a TI internal reference design board. Those marked with 'no' can be used at the risk of the ODM.
(4) A 6-ns speed grade corresponds to a 166-MHz mDDR device.
(5) These devices are EOL and no replacement with the same footprint. Do not use these in new designs.
(6) The manufacturer has issued an upcoming end of life notice on this device.

8.2.3 Detailed Design Procedure

For connecting together the DLPC2607 controller and the DMD, see the reference design schematic. Follow the layout guidelines to achieve a reliable projector. The DLP system requires an optical module or light engine. An optical OEM that specializes in designing optics for DLP projectors typically supplies the optical engine that has the LED packages and the DMD mounted to it.

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8.2.3.1 Hot-Plug Usage

The DLPC2607 device provides fail-safe I/O on all host interface signals (signals powered by VCC_INTF). This protection allows the device to drive these inputs high even when no I/O power is applied.

Under this condition, the DLPC2607 device does not load the input signal, nor draw excessive current that could degrade ASIC reliability. For example, the I^2C bus from the host to other components would not be affected by powering off VCC_INTF to the DLPC2607 device. Note that TI recommends weak pullups or pulldowns on signals feeding back to the host to avoid floating inputs.

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8.2.3.2 Maximum Signal Transition Time

Unless otherwise noted, the maximum recommended 20% to 80% rise and fall time to avoid input buffer oscillation is 10 ns. This applies to all DLPC2607 device input signals.

NOTE

The $\overline{\text{PARK}}$ input signal includes an additional small digital filter that ignores any input-buffer transitions caused by a slower rise and fall time for up to 150 ns.

8.2.3.3 Configuration Control

The primary configuration control mechanism for the DLPC2607 device is the I^2C interface. See the *DLPC2607 Software Programmer's Guide*, DLPU004, for details on how to configure and control the DLPC2607.

8.2.3.4 White Point Correction Light Sensor

With the addition of a light-to-voltage light sensor (such as a phototransistor) and a voltage comparator circuit, the DLPC2607 device supports automatic white point correction and power control.

8.2.4 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is shown in Figure 12. For the LED currents shown, it is assumed that the same current amplitude is applied to the red, green, and blue LEDs.

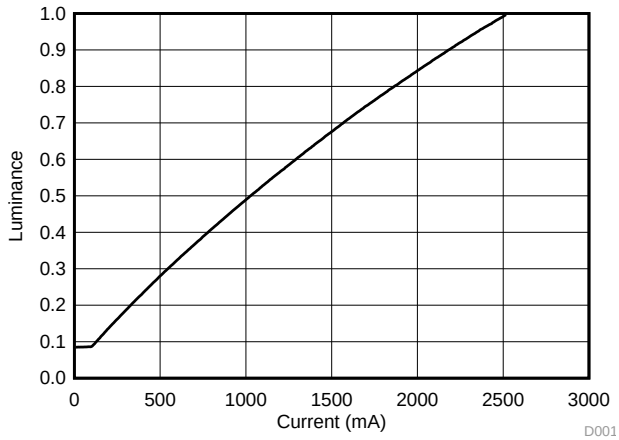

Figure 12. Luminance vs Current

As with prior DLP electronics solutions, image data is 100% digital from the DLPC2607 device input port to the image projected on to the display screen. The image stays in digital form and is never converted into an analog signal. The DLPC2607 device processes the digital input image and converts the data into bit-plane format as needed by the DMD. The DMD then reflects light to the screen using binary pulse-width modulation (PWM) for each pixel mirror. The viewer's eyes integrate this light to form brilliant, crisp images.

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9 Power Supply Recommendations

9.1 System Power Considerations

Table 8 provides a summary of the required power delivery requirements for DLPC2607 for various VCC_FLSH and VCC_INTF power options.

Table 8. Configuration Based Power Supply Requirements

ASIC POWER RAIL	USAGE	NOMINAL VOLTAGE (V)	TOTAL SUPPLY MARGIN (1)
VCC_INTF (2)	Video interface I/O	1.8, 2.5, or 3.3	±5%
VCC_FLSH (3)	Flash I/O	1.8, 2.5, or 3.3	±5%
VDD_PLL (4)	Internal PLL	1	±5%
VCC18	mDDR and DMD I/O	1.8	±5%
VDD10	ASIC core	1	±5%

(1) Total supply margin = DC offset budget + AC noise budget
(2) VCC_INTF is independent of all other supplies.
(3) VCC_FLSH is independent of all other supplies.
(4) When possible, TI recommends to use a tighter supply tolerance (±3%) for the power to the PLL in order to improve system noise immunity.

9.2 System Power-Up and Power-Down Sequence

Although the DLPC2607 device requires an array of power supply voltages, (that is, VDD, VDD_PLL, VCC_18, VCC_FLSH, and VCC_INTF), there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the DLPC2607 device. This is true for both power-up and power-down scenarios. Similarly there is no minimum time between powering-up or powering-down the different supplies feeding the DLPC2607 device.

NOTE

Often, there are power sequencing requirements for devices that share the supplies with the DLPC2607 device.

From a functional standpoint, there is one specific power-sequencing recommendation to ensure proper operation. In particular, apply all ASIC power and allow it to reach the minimum specified voltage levels before RESET is deasserted to ensure proper power-up initialization is performed. Ensure that all I/O power remains applied as long as 1-V core power is applied and RESET is de-asserted.

NOTE

When VDD10 core power is applied but I/O power is not applied, additional leakage current may be drawn.

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System Power-Up and Power-Down Sequence (continued)

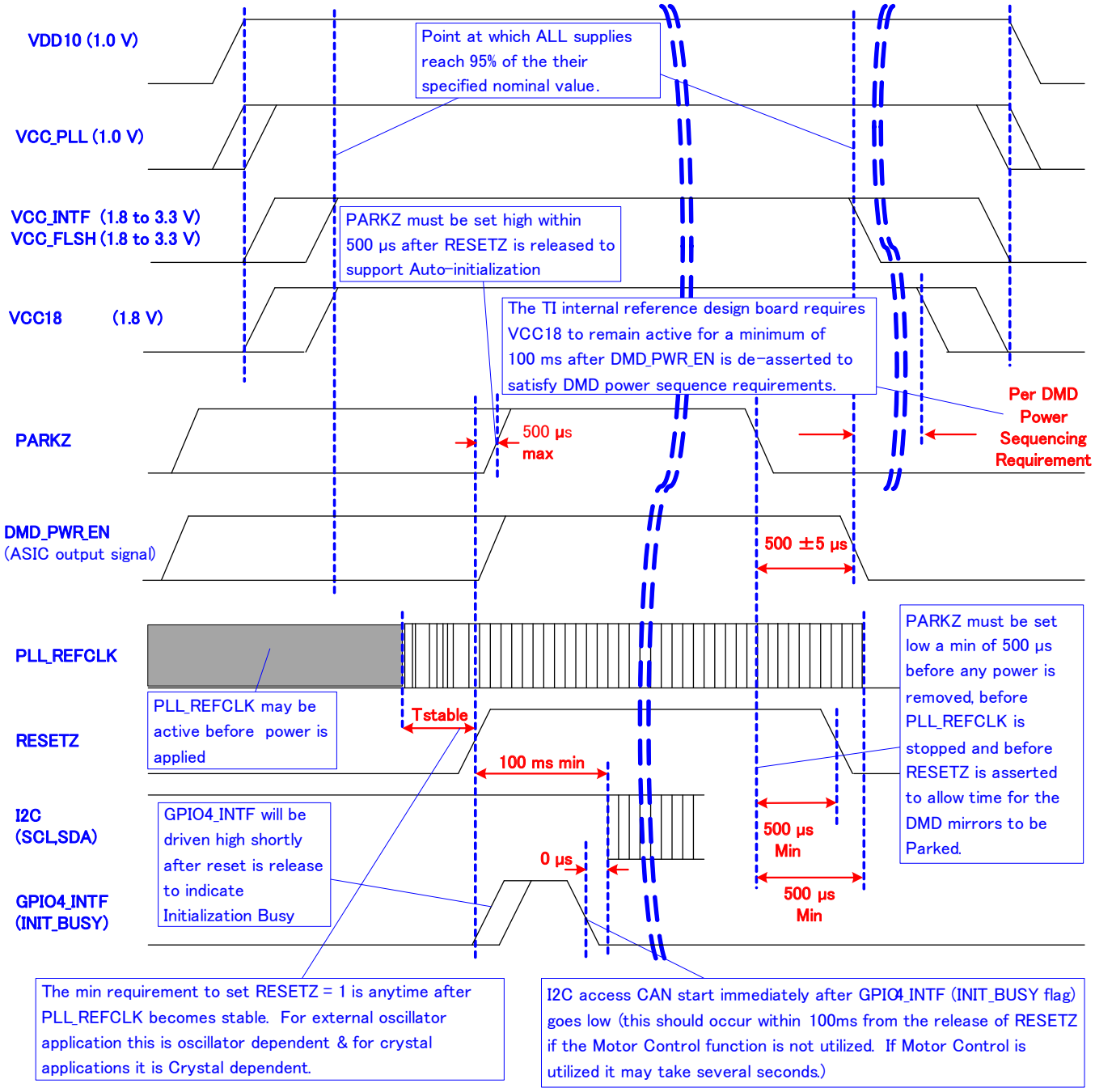

Figure 13. Power-Up and Power-Down Timing

9.3 System Power I/O State Considerations

Note that:

- If VCC18 I/O power is applied when VDD10 core power is not applied, then all mDDR (non-fail-safe) and non-mDDR (fail-safe) output signals associated with the VCC18 supply are in a high-impedance state.
- If VCC_INTF or VCC_FLSH I/O power is applied when VDD10 core power is not applied, then all output signals associated with these inactive I/O supplies are in a high-impedance state.
- If VDD10 core power is applied but VCC_INTF or VCC_FLSH I/O power is not applied, then all output signals associated with these inactive I/O supplies are in a high-impedance state.
- If VDD10 core power is applied but VCC18 I/O power is not applied, then all mDDR (non-fail-safe) and non-mDDR (fail-safe) output signals associated with the VCC18 I/O supply are in a high-impedance state. However, if driven high externally, only the non-mDDR (fail-safe) output signals remain in a high-impedance state, and the mDDR (non fail-safe) signals are shorted to ground through clamping diodes.

9.4 Power-Up Initialization Sequence

It is assumed that an external power monitor holds the DLPC2607 device in system reset during power-up. It must do this by driving RESET to a logic low state. It should continue to assert system reset until all ASIC voltages have reached minimum specified voltage levels, PARK is asserted high, and input clocks are stable. During this time, most ASIC outputs are driven to an inactive state and all bidirectional signals are configured as inputs to avoid contention. ASIC outputs that are not driven to an inactive state are tri-stated, which includes DMD_PWR_EN, LEDDVR_ON, LED_SEL_0, LED_SEL_1, SPICLK, SPIDOUT, and SPICSZ0. After power is stable and the PLL_REFCLK clock input to the DLPC2607 device is stable, then RESET should be deactivated (set to a logic high). The DLPC2607 device then performs a power-up initialization routine that first locks its PLL, followed by loading self configuration data from the external flash. Upon release of RESET, all DLPC2607 device I/Os become active. Immediately following the release of RESET, the GPIO4_INTF signal is driven high to indicate that the auto-initialization routine is in progress. Upon completion of the auto-initialization routine, the DLPC2607 device drives GPIO4_INTF low to signal INITIALIZATION DONE (also known as INIT DONE).

NOTE

The host processor can start sending standard I^2C commands after GPIO4 (INIT_DONE) goes low, or a 100-ms timer expires in the host processor, whichever is earlier, irrespective of whether the motor is enabled or not. However, before sending any compound I^2C commands at power-up, the host processor must wait until GPIO4 (INIT_DONE) goes low, irrespective of whether the motor control function is enabled or not. Due to motor movement, the worst-case time to wait for GPIO4 to go low is when the motor control function is enabled and system dependent; it may take several seconds.

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Power-Up Initialization Sequence (continued)

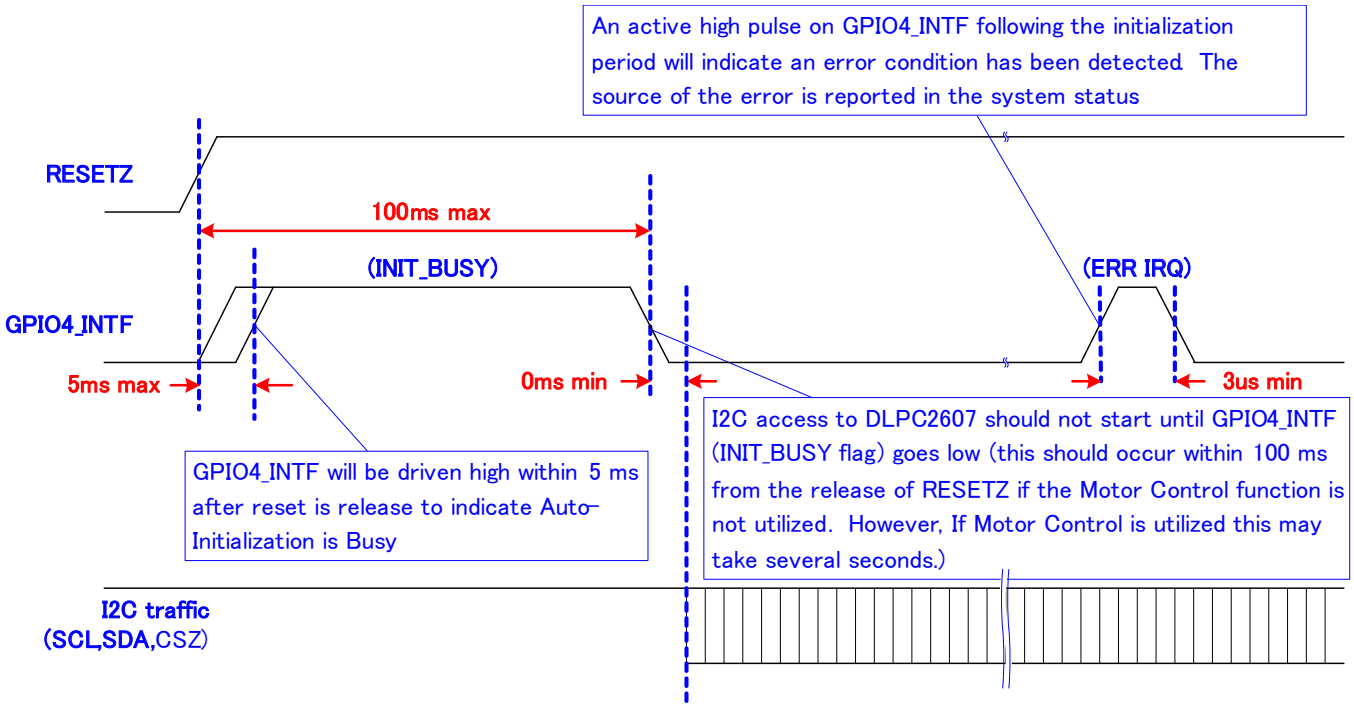

Figure 14. Initialization Timeline

9.5 Power-Good ($\overline{\text{PARK}}$) Support

The $\overline{\text{PARK}}$ signal operates as an early warning signal that alerts the controller 500 µs before DC supply voltages have dropped below specifications. This allows the controller time to park the DMD, ensuring the integrity of future operation. The reference clock continues to run. $\overline{\text{RESET}}$ remains deactivated for at least 500 µs after $\overline{\text{PARK}}$ has been deactivated (set to a logic low) to allow the park operation to complete.

10 Layout

10.1 Layout Guidelines

10.1.1 Internal ASIC PLL Power

TI recommends the following guidelines to achieve desired ASIC performance relative to the internal PLL. The DLPC2607 device contains one internal PLL, which has a dedicated analog supply (VDD_PLL and VSS_PLL). Isolate VDD_PLL power and VSS_PLL ground pins using an RC-filter consisting of two 50-Ω series ferrites and two shunt capacitors (to widen the spectrum of noise absorption). TI recommends one 0.1-µF capacitor and that the other is a 0.01-µF capacitor. Place all four components as close to the ASIC as possible; it is especially important to keep the leads of the high-frequency capacitors as short as possible. Note that the user should connect both capacitors across VDD_PLL and VSS_PLL on the ASIC side of the ferrites.

The PCB layout is critical to PLL performance. The ground and power domains are analog signals, and should be treated as such to achieve minimum noise. Therefore, VDD_PLL must be a single trace from the DLPC2607 device to both capacitors, and then through the series ferrites to the power source. Ensure that the power and ground traces are as short as possible, parallel to each other, and as close as possible to each other.

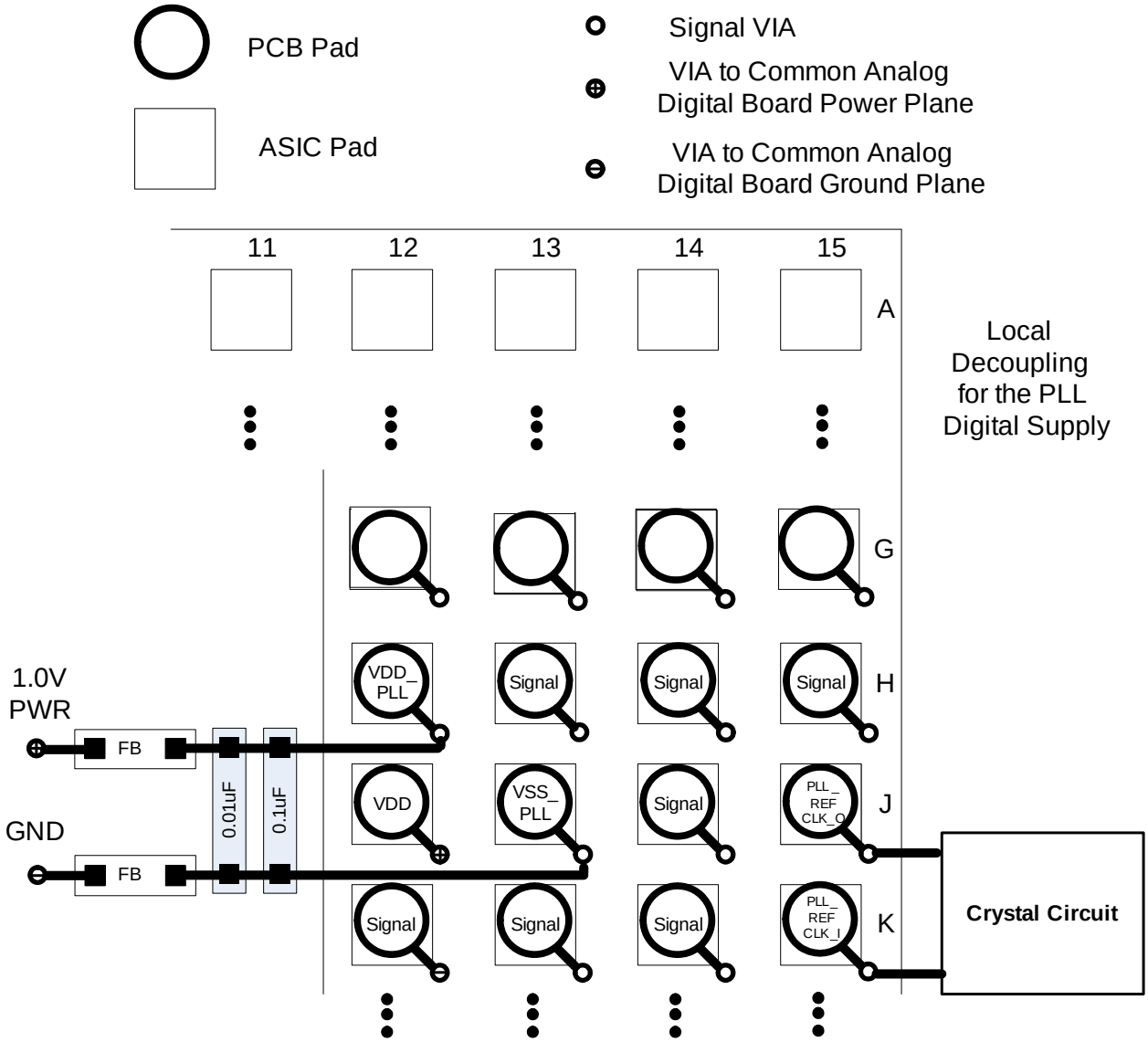

Figure 15. PLL Filter Layout

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Layout Guidelines (continued)

10.1.2 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends to tie unused ASIC input pins through a pullup resistor to their associated power supply or a pulldown to ground. For ASIC inputs with internal pullup or pulldown resistors, it is unnecessary to add an external pullup or pulldown unless specifically recommended.

NOTE

Internal pullup and pulldown resistors are weak so do not expect them to drive the external line. The DLPC2607 device implements very few internal resistors and these are noted in the pin list.

Never tie unused output-only pins directly to power or ground. These pins can be left open.

When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then ensure they are pulled-up (or pulled-down) using an appropriate, dedicated resistor.

10.1.3 SPI Signal Routing

The DLPC2607 device is designed to support two SPI slave devices, specifically, a serial flash and the PMD1000. Given this requires routing associated SPI signals to two locations while attempting to operate at 33.3 MHz, ensure that reflections do not compromise signal integrity. TI recommends the following:

- Split the SPICLK PCB signal trace from the DLPC2607 source to each slave device into separate routes as close to the DLPC2607 device as possible. Make the SPICLK trace length to each device equal in total length.
- Split the SPIDOUT PCB signal trace from the DLPC2607 source to each slave device into separate routes as close to the DLPC2607 device as possible. Make the SPIDOUT trace length to each device equal in total length (that is, use the same strategy as SPICLK).
- Make the SPIDIN PCB signal trace from each slave device to the point where they intersect on the return to the DLPC2607 device equal in length and as short as possible. Make sure they share a common trace back to the DLPC2607 device.
- SPICSZ0 and SPICSZ1 do not require special treatment because they are dedicated signals which drive only one device.

10.1.4 mDDR Memory and DMD Interface Considerations

High-speed interface waveform quality and timing on the DLPC2607 ASIC (that is, the mDDR memory I/F and the DMD interface) depend on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

As an example, the DMD interface system timing margin can be calculated as follows:

Setup margin = (DLPC2607 output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation) (1)

Hold-time margin = (DLPC2607 output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

where

- PCB SI degradation is signal integrity degradation due to PCB effects. This includes things such as simultaneously switching output (SSO) noise, crosstalk, and inter-symbol interference (ISI) noise. (2)

The DLPC2607 device I/O timing parameters, as well as mDDR and DMD I/O timing parameters, can be found in their corresponding data sheets. Similarly, PCB routing mismatch can be easily budgeted and met by controlled PCB routing. However, PCB SI degradation is not so straight forward.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided as a reference of an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Make sure to confirm any variation from these recommendations with PCB signal integrity analysis or lab measurements.

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Layout Guidelines (continued)

10.1.5 PCB Design

- Configuration: Asymmetric dual stripline
- Etch thickness (T): 0.5 oz copper
- Single-ended signal impedance: 50 Ω (±10%)
- Single-ended signal impedance: 100-Ω differential (±10%)

- Reference plane 1 is assumed to be a ground plane for proper return path.
- Reference plane 2 is assumed to be the I/O power plane or ground.
- Dielectric FR4, (Er): 4.2 (nominal)
- Signal trace distance to reference plane 1 (H1): 5 mil (nominal)
- Signal trace distance to reference plane 2 (H2): 34.2 mil (nominal)

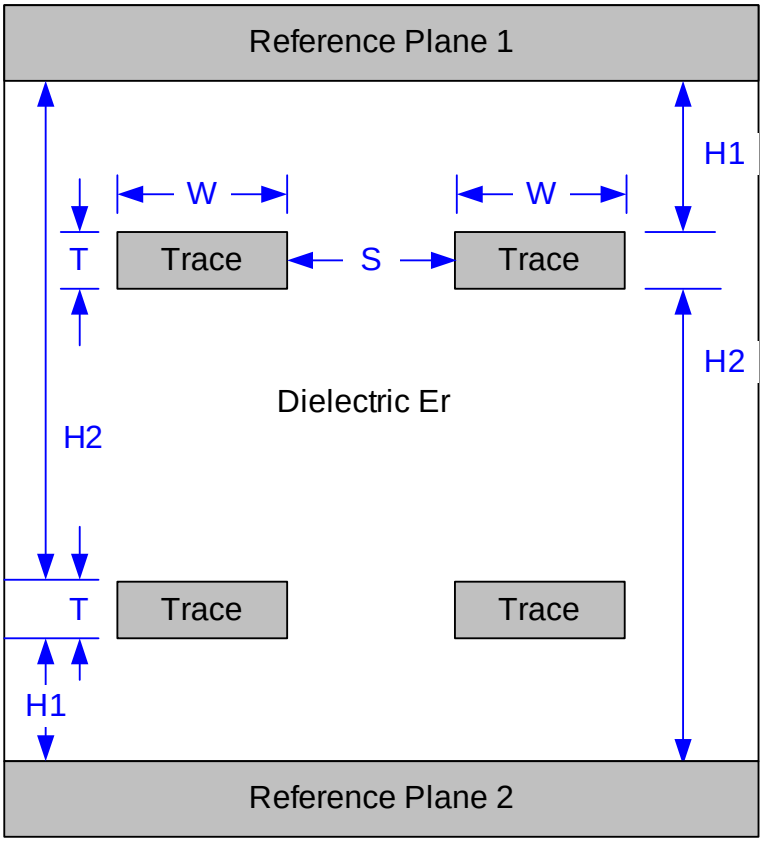

Figure 16. PCB Stacking Geometries

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Layout Guidelines (continued)

10.1.6 General PCB Routing (Applies to All Corresponding PCB Signals)

Table 9. PCB Line and Spacing Recommendations(1) (2) (3)

PARAMETER	APPLICATION	SINGLE-ENDED SIGNALS	DIFFERENTIAL PAIRS	UNIT
Line width (W)	Escape routing in ball field	3 (0.762)	3 (0.762)	mil (mm)
	PCB etch – Outer layer data or control	7.25 (0.184)	4.5 (0.114)	mil (mm)
	PCB etch - Inner layer data or control	4.5 (0.114)	4.5 (0.114)	mil (mm)
	PCB etch clocks	4.5 (0.114)	4.5 (0.114)	mil (mm)
Differential signal pair spacing (S)	PCB etch data or control	N/A	7.75 [1] (0.305)	mil (mm)
	PCB etch clocks	N/A	7.75 [1] (0.305)	mil (mm)
Minimum line spacing to other signals (S)	Escape routing in ball field	3 (0.762)	3 (0.762)	mil (mm)
	PCB etch – Outer layer data or control	7.25 (0.184)	4.5 (0.114)	mil (mm)
	PCB etch - Inner layer data or control	4.5 (0.114)	4.5 (0.114)	mil (mm)
	PCB etch clocks	11 (0.279)	11 (0.279)	mil (mm)
Maximum differential pair P-to-N length mismatch	Total clock	N/A	25 (0.635)	mil (mm)

(1) Spacing may vary to maintain differential impedance requirements.
(2) The DLPC2607 device only includes one differential signal pair – MEM0_CK_P and MEM0_CK_N.
(3) These values are merely recommendations to achieve good signal integrity. The OEM is free to apply their own rules as long as they maintain good signal integrity.

These PCB design guidelines are purposefully conservative to minimize potential signal integrity issues. Given this device is targeted for low-cost, handheld application, there is a need to be more aggressive with these best practices. TI highly recommends to perform a full-board-level signal integrity analysis, if these guidelines cannot be followed. The DLPC2607 IBIS models are available for such analysis.

10.1.7 Maximum, Pin-to-Pin, PCB Interconnects Etch Lengths

Table 10. Max Pin-to-Pin PCB Interconnect Recommendations(1) (2)

BUS	SIGNAL INTERCONNECT TOPOLOGY		UNIT
	SINGLE BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD			
DMD_D(14:0), DMD_DCLK, DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_OEZ DMD_DAD_STRB, DMD_DAD_BUS, DMD_SAC_CLK and DMD_SAC_BUS	4 max (101.5 max)	3.5 max (88.91 max)	inch (mm)
mDDR			
MEM0_DQ(15:8), MEM0_UDM and MEM0_UDQS	1.5 max 38.1 max	NA	inch (mm)
mDDR			
MEM0_DQ(7:0), MEM0_LDM and MEM0_LDQS	1.5 max (38.1 max)	NA	inch (mm)
mDDR			

(1) Max signal routing length includes escape routing.
(2) Multi-board DMD routing length is more restricted due to the impact of the connector.

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Table 10. Max Pin-to-Pin PCB Interconnect Recommendations(1) (2) (continued)

BUS	SIGNAL INTERCONNECT TOPOLOGY		UNIT
	SINGLE BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
MEM0_CK_P, MEM0_CK_N, MEM0_A(12:0), MEM0_BA(1:0), MEM0_CKE, MEM0_CSZ, MEM0_RASZ, MEM0_CASZ and MEM0_WEZ	2.5 max (63.5 max)	N/A	inch (mm)

10.1.8 I/F Specific PCB Routing

Table 11. High-Speed PCB Signal Routing Matching Requirements(1) (2) (3)

SIGNAL INTERCONNECT TOPOLOGY				
IF	SINGLE GROUP	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD	DMD_D(14:0), DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_OEZ	DMD_DCLK	±500 (±12.7)	mil (mm)
	DMD_DAD_STRB, DMD_DAD_BUS	DMD_DCLK	±750 (±19.05)	mil (mm)
	DMD_SAC_BUS	DMD_SAC_CLK	±750 (±19.05)	mil (mm)
	DMD_SAC_CLK	DMD_DCLK	±500 (±12.7)	mil (mm)
mDDR:	MEM0_CLK_P	MEM0_CLK_N	±150 (±3.81)	mil (mm)
	Read/ Write Data Lower Byte: MEM0_LDM and MEM0_DQ(7:0) 38.1 max	MEM0_LDQS	±300 (±7.62)	mil (mm)
	Read/ Write Data Upper Byte: MEM0_UDM and MEM0_DQ(15:8)	MEM0_UDQS	±300 (±7.62)	mil (mm)
	Address and control: MEM0_A(12:0), MEM0_BA(1:0), MEM0_RASZ , MEM0_CASZ, MEM0_WEZ, MEM0_CSZ, MEM0_CKE	MEM0_CLK_P/ MEM0_CLK_N	±1000 (±25.4)	mil (mm)
	Data strobes: MEM0_LDQS and MEM0_UDQS	MEM0_CLK_P/ MEM0_CLK_N	±300 (±7.62)	mil (mm)

(1) These values apply to PCB routing only. They do not include any internal package routing mismatch associated with the DLPC2607 device, DMD, or mDDR memory.
(2) DMD data and control lines are DDR, whereas DMD_SAC and DMD_DAD lines are single data rate. Matching the DDR lines is more critical and takes precedence over matching single data rate lines.
(3) mDDR data, mask, and strobe lines are DDR, whereas address and control are single data rate. Matching the DDR lines is more critical and takes precedence over matching single data rate lines.

10.1.9 Number of Layer Changes

- Single-ended signals: Minimize the number of layer changes.
- Differential signals: Individual differential pairs can be routed on different layers, but the signals of a given pair must not change layers.

10.1.10 Stubs

Avoid stubs.

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10.1.11 Termination Requirements:

DMD I/F	Terminate all DMD I/F signals, with the exception of DMD_OEZ (specifically DMD_D(14:0), DMD_DCLK, DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_DAD_STRB, DMD_DAD_BUS, DMD_SAC_CLK, and DMD_SAC_BUS), at the source with a 10- to 30-Ω series resistor. TI recommends a 30-Ω series resistor for most applications because this minimizes overshoot, undershoot, and reduces EMI; however, for systems that must operate below –20°C, it may be necessary to reduce this series resistance to avoid narrowing the data eye too much under worse-case PVT conditions. TI recommends IBIS simulations for this worse-case scenario.
mDDR memory I/F	
mDDR differential clock	Terminate each line, specifically MEM0_CK(P:N), at the source with a 30-Ω series resistor. Terminate the pair with an external 100-Ω differential termination across the two signals as close to the DRAM as possible. (It may be possible to use a 200-Ω differential termination at the DRAM to save power while still providing sufficient signal integrity, but this has not been validated.)
mDDR data, strobe, and mask	Terminate MEM0_DQ(15:0), MEM0_LDM, MEM0_UDM, MEM0_LDQS, and MEM0_UDQS with a 30-Ω series resistor located midway between the two devices.
mDDR address and control	Terminate MEM0_A(12:0), MEM0_BA(1:0), MEM0_CKE, MEM0_CSZ, MEM0_RASZ, MEM0_CASZ, and MEM0_WEZ at the source with a 30-Ω series resistor.

For applications where the routed distance of the mDDR or DMD signal can be maintained to a length of less than 0.75 inches, this signal is short enough not be considered a transmission line and does not need a series terminating resistor.

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10.2 Layout Example

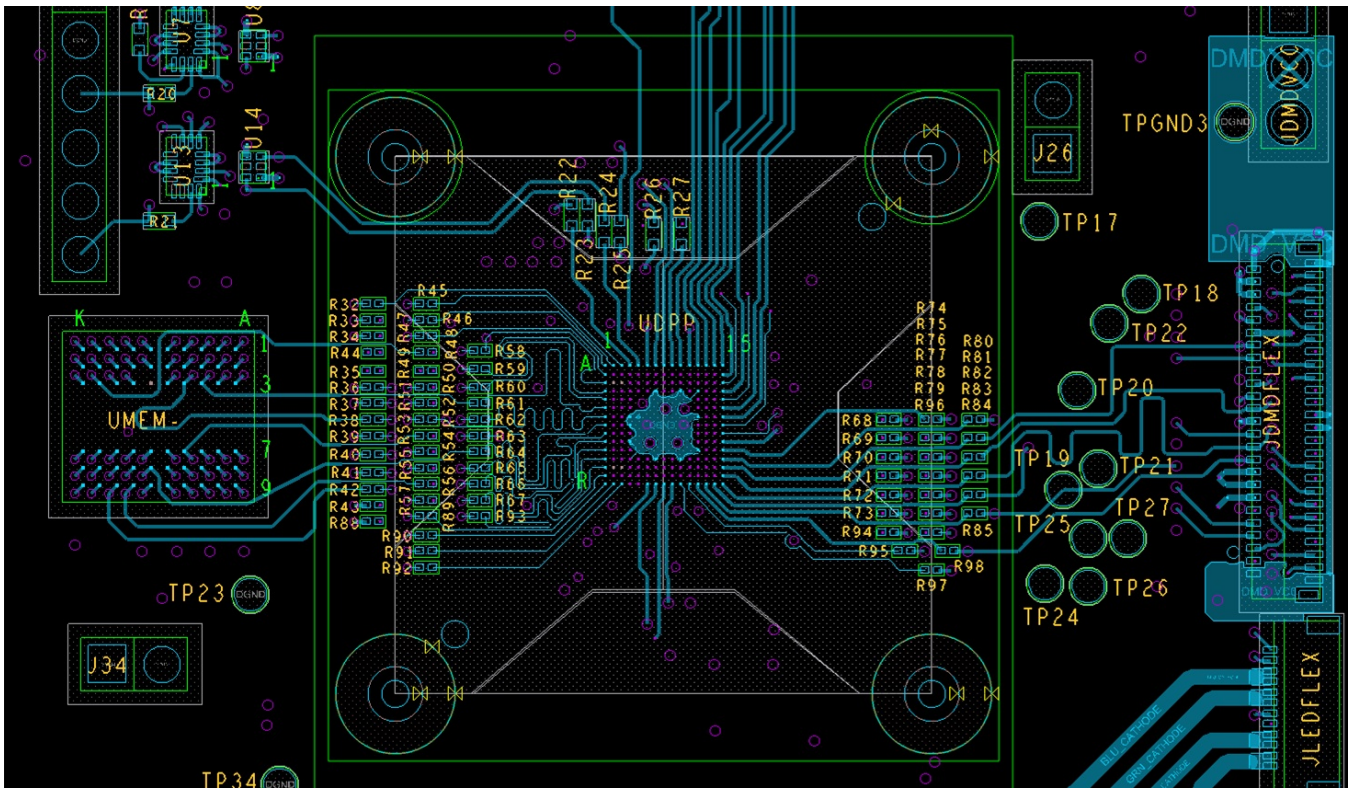

Figure 17. PCB Layout Example

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11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

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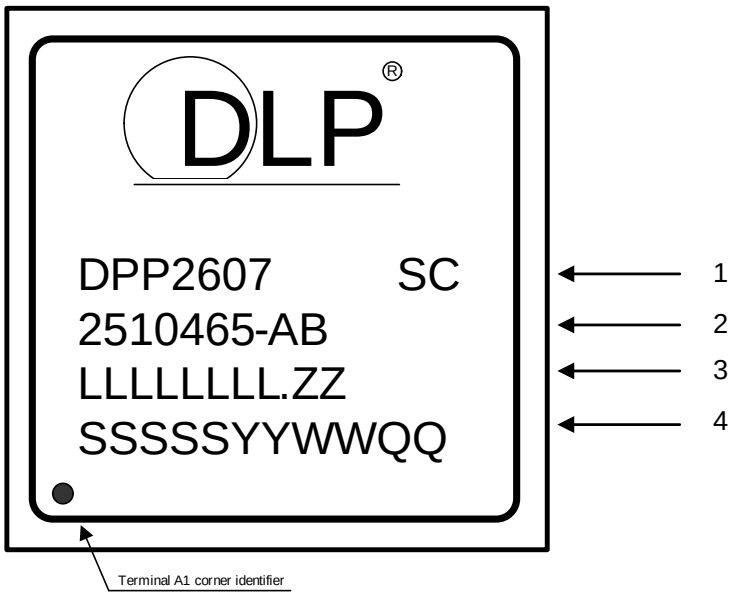
11.1.2 デバイスの項目表記

11.1.2.1 デバイス・マーキング



マーキングの定義:

1. DLPデバイス名

   SC: 半田ボール組成

   e1: SnAgCuからなる鉛フリー・半田ボールを示しています。

   G8: 錫・銀・銅(SnAgCu)からなり、銀の含有量が1.5%以下で、モールド化合物がTIのグリーン規定を満たしている鉛フリー半田ボールを示しています。

2. TI型番

   AB (1つまたは2つの英数字)＝「**A**」はTIデバイス・ダッシュ番号です。「**B**」は未認定デバイス・マーキング用です。プロトタイプやスキュー・ロット・サンプルなどの未認定デバイスには、いずれも「**B**」のマーキング位置に(TI型番に続けて)「**X**」を記したラベルが貼付されます。認定済みデバイスは「**B**」が空欄のままです。

3. LLLLLLLL.ZZは半導体ウエハーの工場ロット・コードと鉛フリー半田ボール・マーキングです。

   LLLLLLLL: 製造ロット・コード

   ZZ: ロット枝番号

4. SSSSSYYWWQQ: パッケージ組み立て情報

   SSSSS: 製造サイト

   YYWW: 日付コード(YY＝年、WW＝週)

   QQ: 認定レベル・オプション — エンジニアリング・サンプルの場合は、このフィールドの末尾に**ES**が付きます。

   例えば、KOREA0914ESは2009年第14週に韓国で製造されたエンジニアリング・サンプルです。

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商標

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11.4 静電気放電に関する注意事項

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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12.1 付録: パッケージ･オプション

12.1.1 パッケージ情報

発注可能なデバイス	供給状況 (1)	パッケージの種類	パッケージ図	ピン数	パッケージの数量	エコ・プラン (2)	リード/ボール仕上げ	MSL ピーク温度 (3)	動作温度(°C)	デバイス・マーキング(4)(5)
DLPC2607ZVB	供給中	NFBGA	ZVB	176	260	未定	TIサポートにお電話ください	Level-3-260C-168 HRS	－30～85	

(1) 供給状況値は次のように定義されています。
供給中:製品デバイスは新規設計用に推奨されています。
最終受注中:TI によりデバイスの生産中止予定が発表され、ライフタイム購入期間が有効です。
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生産前 未発表デバイス、生産していない、市販されていない、またはウェブでも発表されておらず、サンプルは提供されていません。
開発中製品:デバイスは発表済みですが、まだ生産が開始されていません。サンプルが提供される場合と提供されない場合があります。
生産中止品: TI はデバイスの生産を終了しました。

(2) エコプラン - 環境に配慮した製品分類プランであり、鉛フリー(RoHS)、鉛フリー(RoHS 免除)、またはグリーン(RoHS 準拠、Sb/Br 非含有)があります。最新情報および製品内容の詳細については、http://www.ti.com/productcontent でご確認ください。
TBD:鉛フリー/グリーン変換プランが策定されていません。
鉛フリー(RoHS): TI における「Lead-Free」または「Pb-Free」(鉛フリー)は、6 つの物質すべてに対して現在のRoHS 要件を満たしている半導体製品を意味します。これには、同種の材質内で鉛の重量が 0.1% を超えないという要件も含まれます。高温で半田付けするように設計されている場合、TIの鉛フリー製品は指定された鉛フリー・プロセスでの使用に適しています。
鉛フリー(RoHS 免除):この部品は、1)ダイとパッケージの間に鉛ベース・フリップ・チップの半田バンプ使用、または 2)ダイとリード・フレーム間に鉛ベースの接着剤を使用、が除外されています。それ以外の点では、上記の定義のPb-Free(RoHS準拠)の条件を満たしています。
グリーン(RoHS 準拠、Sb/Br 非含有):TI における「グリーン」は、鉛フリー(RoHS 互換)に加えて、臭素(Br)およびアンチモン(Sb)をベースとした難燃材を含まない(均質な材質中の Br または Sb 重量が 0.1% を超えない)ことを意味しています。

(3) MSL、ピーク温度-- JEDEC 業界標準分類に従った耐湿性レベル、およびピーク半田温度です。

(4) ロゴ、ロット・トレース・コード情報、または環境カテゴリに関する追加マークがデバイスに表示されることがあります

(5) 複数のデバイス・マーキングが、括弧書きされています。「～」で区切られた括弧書きデバイス専用マークだけがデバイスに表示されます。改行すると前行の続きになります。2 行が結合されている場合、そのデバイスの全デバイス・マークとなります。

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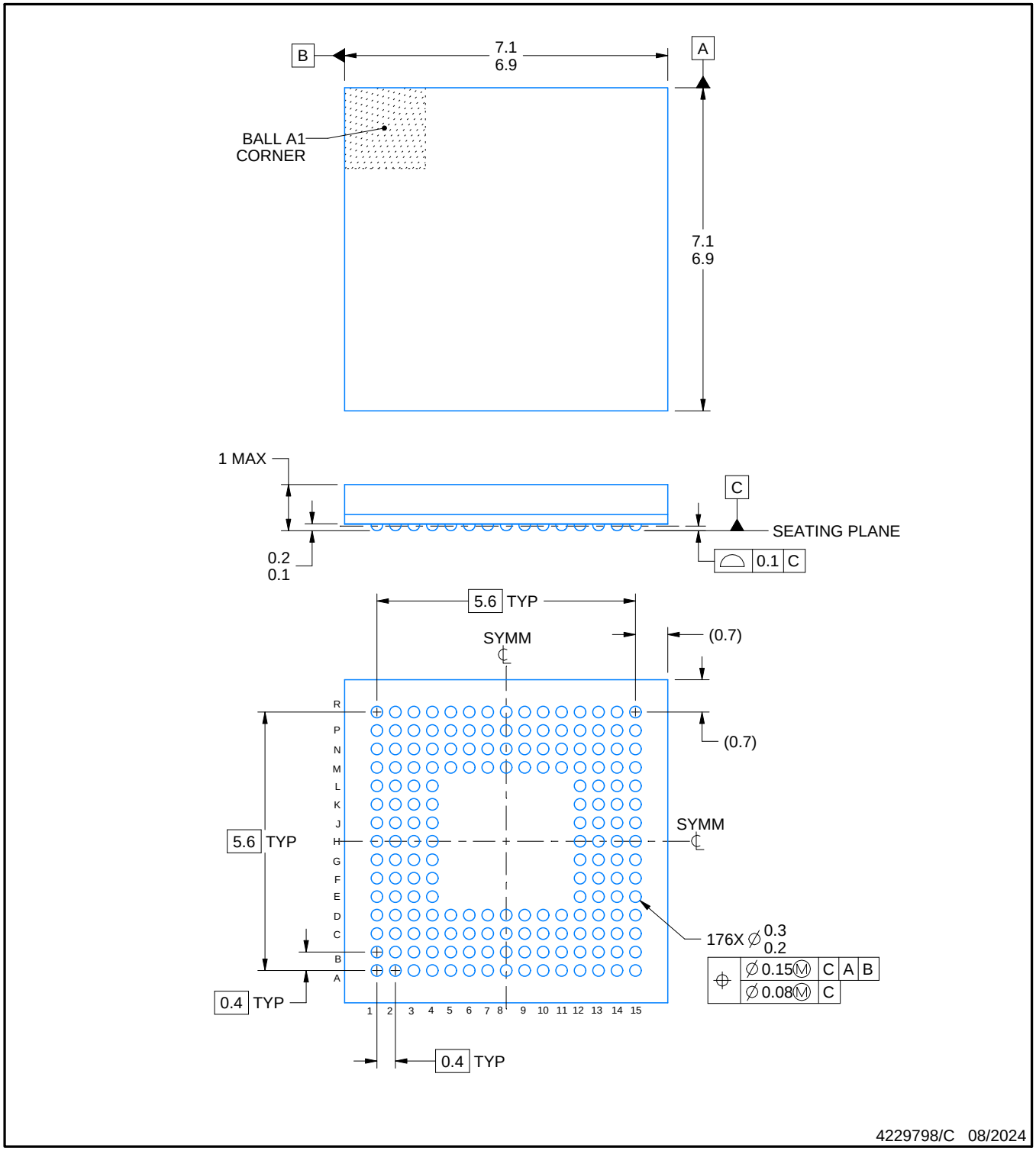
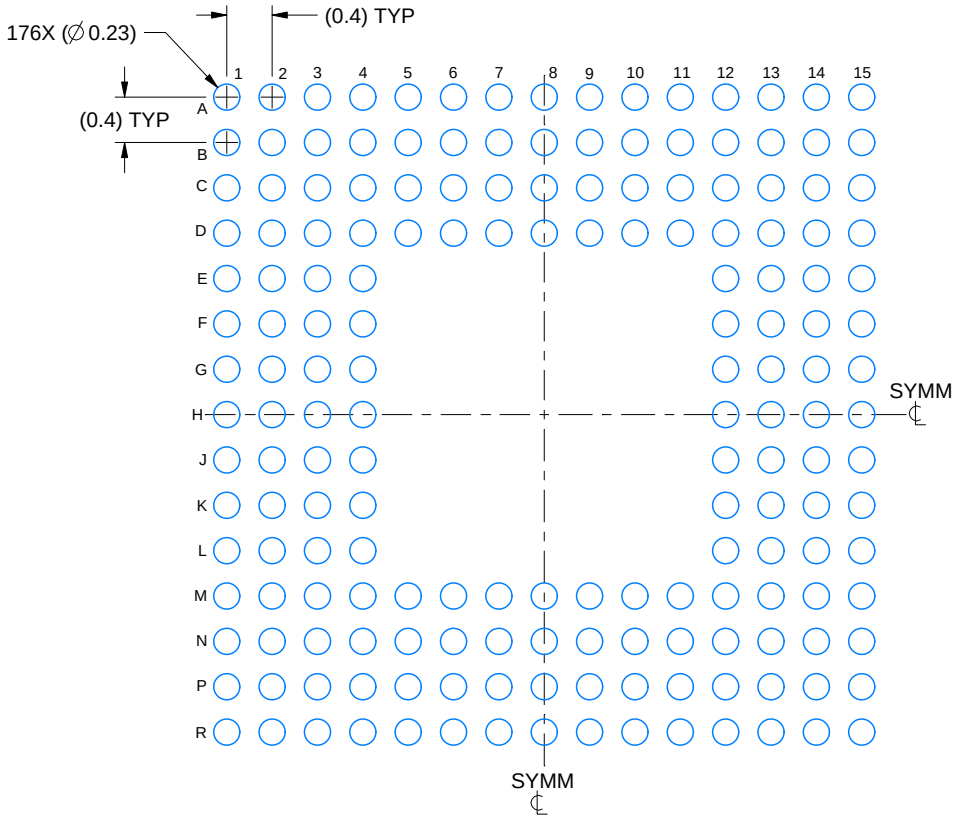
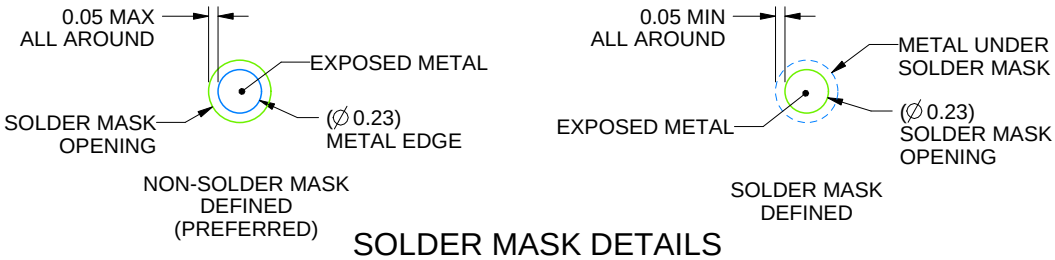


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS
NOT TO SCALE

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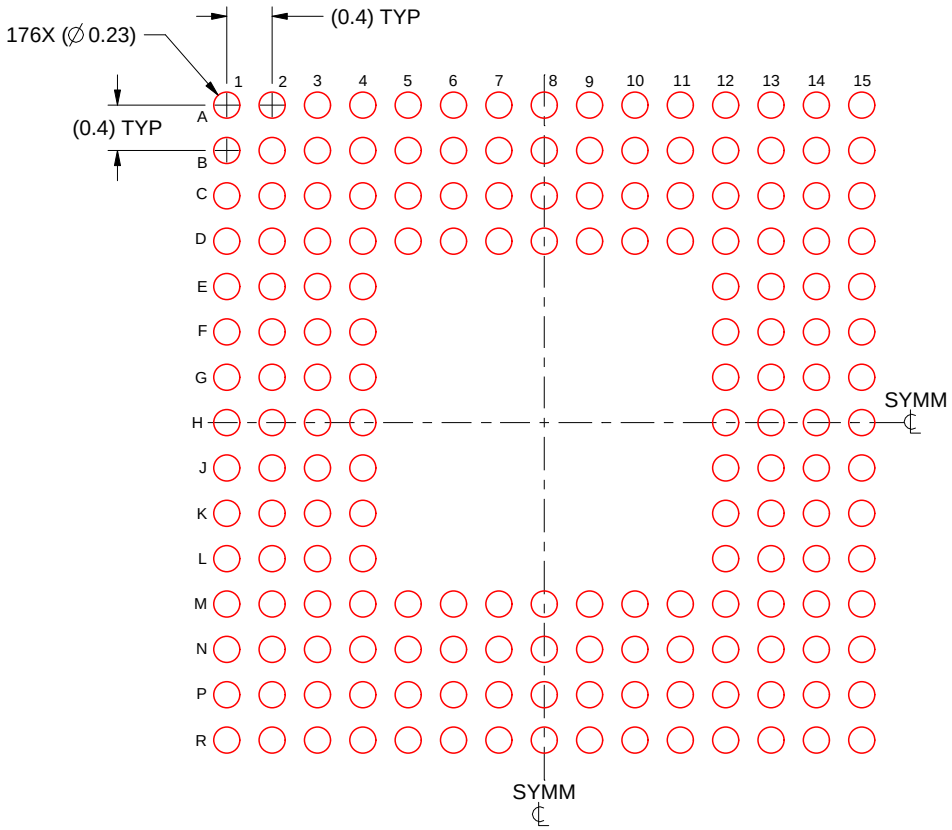
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 15X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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