DLP9000XUV 0.9 UV WQXGA Type A DMD

1 Features

- High resolution 2560 × 1600 (WQXGA) Array
  - > 4 Million micromirrors
  - 7.56-µm micromirror pitch
  - 0.9-Inch micromirror array diagonal
  - ±12° micromirror tilt angle
  - Designed for corner illumination
  - Integrated micromirror driver circuitry
- DLP9000XUV with the DLPC910 controller
  - 480-MHz input data clock rate
  - Streams up to 61 gigapixels per second
  - 1-Bit binary patterns up to 14,989 Hz
  - 8-Bit gray patterns up to 1,873 Hz (coupled with Illumination Modulation)
- Designed to steer UV wavelengths from 355 to 420 nm
  - Window transmission 98% (per window pass)
  - Micromirror reflectivity 88% (nominal)
  - Array diffraction efficiency 85% (nominal)
  - Array fill factor 92% (nominal)

2 Applications

- Industrial
  - Direct imaging lithography
  - Laser marking and repair systems
  - Computer to plate printers
  - 3D printers
- Medical
  - Ophthalmology
  - Photo therapy

3 Description

Featuring over 4 million micromirrors, the DLP9000XUV digital micromirror device (DMD) enables high resolution and high performance spatial light modulation of UV wavelengths from 355 nm to 420 nm. The DLP9000XUV is designed with a special UV optimized window to support numerous applications in the industrial and medical markets. Reliable operation of the DLP9000XUV chipset requires the DMD be driven by the DLPC910 Controller. The DLP9000XUV chipset's architecture enables continuous data streaming for very high speed lithographic applications. The 4.1 megapixel resolution of the DMD enables large 3D print build sizes and results in fine detail for Digital Lithography.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP9000XUV	FLS (355)	42.20 mm x 42.20 mm x 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Schematic

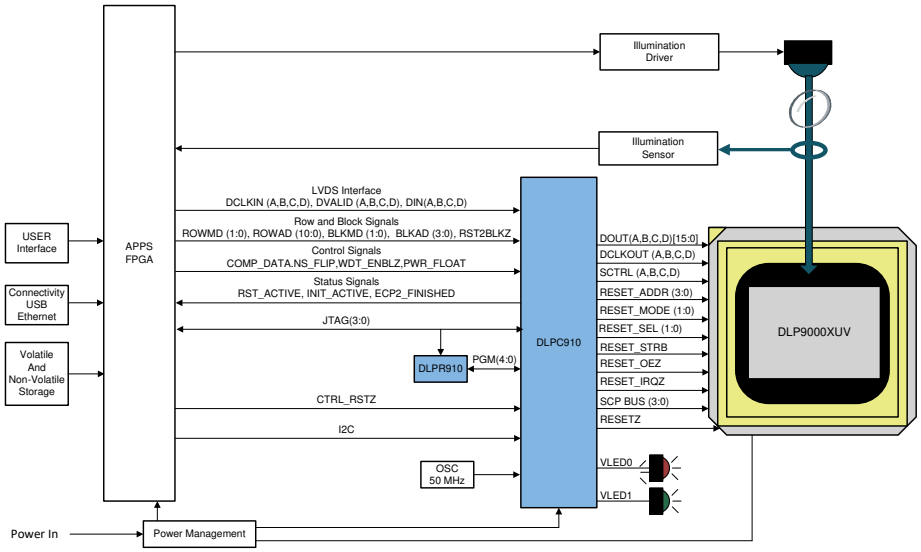


Table of Contents

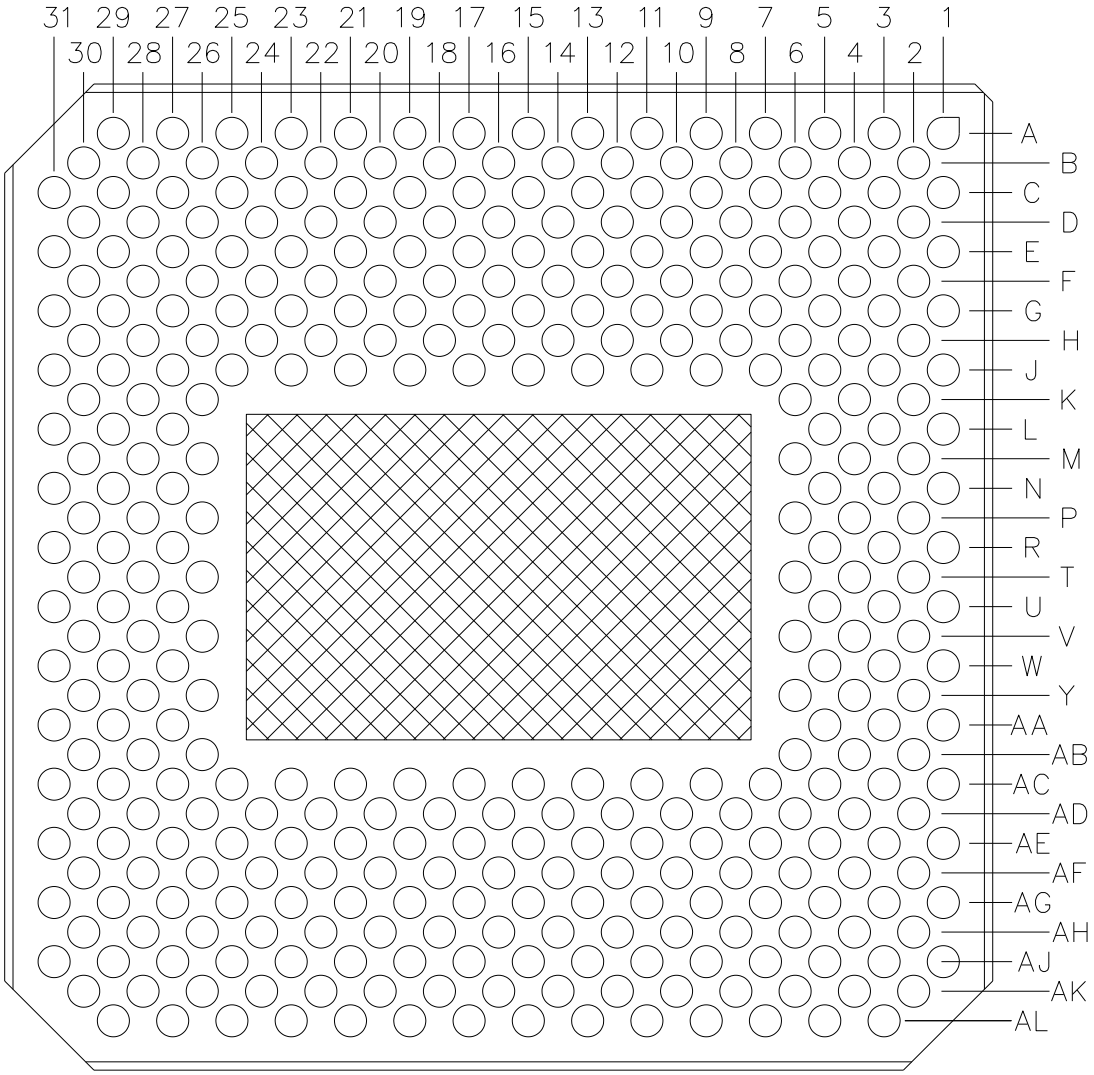
1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 10
6.1 Absolute Maximum Ratings ... 10
6.2 Storage Conditions ... 10
6.3 ESD Ratings ... 11
6.4 Recommended Operating Conditions ... 11
6.5 Thermal Information ... 13
6.6 Electrical Characteristics ... 13
6.7 Timing Requirements ... 14
6.8 Capacitance at Recommended Operating Conditions ... 18
6.9 Typical Characteristics ... 18
6.10 System Mounting Interface Loads ... 19
6.11 Micromirror Array Physical Characteristics ... 20
6.12 Micromirror Array Optical Characteristics ... 21
6.13 Optical and System Image Quality ... 22
6.14 Window Characteristics ... 22
6.15 Chipset Component Usage Specification ... 22
7 Parameter Measurement Information ... 23
8 Detailed Description ... 24
8.1 Overview ... 24
8.2 Functional Block Diagram ... 25
8.3 Feature Description ... 26
8.4 Device Functional Modes ... 29
8.5 Window Characteristics and Optics ... 29
8.6 Micromirror Array Temperature Calculation ... 30
8.7 Micromirror Landed-On/Landed-Off Duty Cycle ... 31
9 Application and Implementation ... 33
9.1 Application Information ... 33
9.2 Typical Applications ... 34
10 Power Supply Requirements ... 36
10.1 DMD Power Supply Requirements ... 36
10.2 DMD Power Supply Power-Up Procedure ... 36
10.3 DMD Mirror Park Sequence (Power_Float) Requirements ... 37
10.4 DMD Power Supply Power-Down Procedure ... 37
11 Layout ... 40
11.1 Layout Guidelines ... 40
11.2 Layout Example ... 42
12 Device and Documentation Support ... 45
12.1 Device Support ... 45
12.2 Documentation Support ... 46
12.3 Support Resources ... 46
12.4 Trademarks ... 46
12.5 Electrostatic Discharge Caution ... 46
12.6 Glossary ... 46
13 Mechanical, Packaging, and Orderable Information ... 46
13.1 Thermal Characteristics ... 46
13.2 Package Thermal Resistance ... 46
13.3 Case Temperature ... 46
13.4 Package Option Addendum ... 47

4 Revision History

DATE	REVISION	NOTES
December 2019	*	Initial Release.

5 Pin Configuration and Functions

FLS Package Connector Terminals
355-Pin CLGA
Bottom View



Pin Functions

PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	DESCRIPTION	TRACE (mils) (4)
NAME	NO.						
DATA BUS A							
D_AN(0)	H10	Input	LVDS	DDR	Differential	Data, negative	737
D_AN(1)	G3	Input	LVDS	DDR	Differential	Data, negative	737
D_AN(2)	G9	Input	LVDS	DDR	Differential	Data, negative	737
D_AN(3)	F4	Input	LVDS	DDR	Differential	Data, negative	738
D_AN(4)	F10	Input	LVDS	DDR	Differential	Data, negative	739
D_AN(5)	E3	Input	LVDS	DDR	Differential	Data, negative	739
D_AN(6)	E9	Input	LVDS	DDR	Differential	Data, negative	737
D_AN(7)	D2	Input	LVDS	DDR	Differential	Data, negative	737
D_AN(8)	J5	Input	LVDS	DDR	Differential	Data, negative	739
D_AN(9)	C9	Input	LVDS	DDR	Differential	Data, negative	736
D_AN(10)	F14	Input	LVDS	DDR	Differential	Data, negative	743
D_AN(11)	B8	Input	LVDS	DDR	Differential	Data, negative	737
D_AN(12)	G15	Input	LVDS	DDR	Differential	Data, negative	739
D_AN(13)	B14	Input	LVDS	DDR	Differential	Data, negative	740
D_AN(14)	H16	Input	LVDS	DDR	Differential	Data, negative	737
D_AN(15)	D16	Input	LVDS	DDR	Differential	Data, negative	737
D_AP(0)	H8	Input	LVDS	DDR	Differential	Data, positive	737
D_AP(1)	G5	Input	LVDS	DDR	Differential	Data, positive	738
D_AP(2)	G11	Input	LVDS	DDR	Differential	Data, positive	737
D_AP(3)	F2	Input	LVDS	DDR	Differential	Data, positive	736
D_AP(4)	F8	Input	LVDS	DDR	Differential	Data, positive	739
D_AP(5)	E5	Input	LVDS	DDR	Differential	Data, positive	738
D_AP(6)	E11	Input	LVDS	DDR	Differential	Data, positive	737
D_AP(7)	D4	Input	LVDS	DDR	Differential	Data, positive	737
D_AP(8)	J3	Input	LVDS	DDR	Differential	Data, positive	739
D_AP(9)	C11	Input	LVDS	DDR	Differential	Data, positive	737
D_AP(10)	F16	Input	LVDS	DDR	Differential	Data, positive	741
D_AP(11)	B10	Input	LVDS	DDR	Differential	Data, positive	737
D_AP(12)	H14	Input	LVDS	DDR	Differential	Data, positive	739
D_AP(13)	B16	Input	LVDS	DDR	Differential	Data, positive	739
D_AP(14)	G17	Input	LVDS	DDR	Differential	Data, positive	737
D_AP(15)	D14	Input	LVDS	DDR	Differential	Data, positive	737
DATA BUS B							
D_BN(0)	AD8	Input	LVDS	DDR	Differential	Data, negative	739
D_BN(1)	AE3	Input	LVDS	DDR	Differential	Data, negative	737
D_BN(2)	AF8	Input	LVDS	DDR	Differential	Data, negative	736
D_BN(3)	AF2	Input	LVDS	DDR	Differential	Data, negative	739
D_BN(4)	AG5	Input	LVDS	DDR	Differential	Data, negative	737
D_BN(5)	AH8	Input	LVDS	DDR	Differential	Data, negative	737
D_BN(6)	AG9	Input	LVDS	DDR	Differential	Data, negative	737
D_BN(7)	AH2	Input	LVDS	DDR	Differential	Data, negative	739

(1) The following power supplies are required to operate the DMD: V_{CC}, V_{CCI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. V_{SS} must also be connected.
(2) DDR = Double data rate.
SDR = Single data rate.
Refer to the *Timing Requirements* regarding specifications and relationships.
(3) Internal term = CMOS level internal termination. Refer to *Recommended Operating Conditions* regarding differential termination specification.
(4) Dielectric constant for the DMD type A ceramic package is approximately 9.6.
For the package trace lengths shown:
Propagation speed = 11.8 / sqrt(9.6) = 3.808 in/ns.
Propagation delay = 0.262 ns/in = 262 ps/in = 10.315 ps/mm.

Pin Functions (continued)

PIN [1]		TYPE (I/O/P)	SIGNAL	DATA RATE [2]	INTERNAL TERM [3]	DESCRIPTION	TRACE (mils) [4]
NAME	NO.						
D_BN(8)	AL9	Input	LVDS	DDR	Differential	Data, negative	737
D_BN(9)	AJ11	Input	LVDS	DDR	Differential	Data, negative	738
D_BN(10)	AF14	Input	LVDS	DDR	Differential	Data, negative	736
D_BN(11)	AE11	Input	LVDS	DDR	Differential	Data, negative	737
D_BN(12)	AH16	Input	LVDS	DDR	Differential	Data, negative	740
D_BN(13)	AD14	Input	LVDS	DDR	Differential	Data, negative	737
D_BN(14)	AG17	Input	LVDS	DDR	Differential	Data, negative	738
D_BN(15)	AD16	Input	LVDS	DDR	Differential	Data, negative	738
D_BP(0)	AD10	Input	LVDS	DDR	Differential	Data, positive	738
D_BP(1)	AE5	Input	LVDS	DDR	Differential	Data, positive	737
D_BP(2)	AF10	Input	LVDS	DDR	Differential	Data, positive	737
D_BP(3)	AF4	Input	LVDS	DDR	Differential	Data, positive	738
D_BP(4)	AG3	Input	LVDS	DDR	Differential	Data, positive	737
D_BP(5)	AH10	Input	LVDS	DDR	Differential	Data, positive	737
D_BP(6)	AG11	Input	LVDS	DDR	Differential	Data, positive	737
D_BP(7)	AH4	Input	LVDS	DDR	Differential	Data, positive	740
D_BP(8)	AL11	Input	LVDS	DDR	Differential	Data, positive	736
D_BP(9)	AJ9	Input	LVDS	DDR	Differential	Data, positive	739
D_BP(10)	AF16	Input	LVDS	DDR	Differential	Data, positive	737
D_BP(11)	AE9	Input	LVDS	DDR	Differential	Data, positive	737
D_BP(12)	AH14	Input	LVDS	DDR	Differential	Data, positive	737
D_BP(13)	AE15	Input	LVDS	DDR	Differential	Data, positive	737
D_BP(14)	AG15	Input	LVDS	DDR	Differential	Data, positive	740
D_BP(15)	AE17	Input	LVDS	DDR	Differential	Data, positive	739
DATA BUS C							
D_CN(0)	C15	Input	LVDS	DDR	Differential	Data, negative	737
D_CN(1)	E15	Input	LVDS	DDR	Differential	Data, negative	737
D_CN(2)	A17	Input	LVDS	DDR	Differential	Data, negative	736
D_CN(3)	F20	Input	LVDS	DDR	Differential	Data, negative	737
D_CN(4)	B20	Input	LVDS	DDR	Differential	Data, negative	738
D_CN(5)	G21	Input	LVDS	DDR	Differential	Data, negative	737
D_CN(6)	D22	Input	LVDS	DDR	Differential	Data, negative	737
D_CN(7)	E23	Input	LVDS	DDR	Differential	Data, negative	737
D_CN(8)	B26	Input	LVDS	DDR	Differential	Data, negative	739
D_CN(9)	F28	Input	LVDS	DDR	Differential	Data, negative	737
D_CN(10)	C27	Input	LVDS	DDR	Differential	Data, negative	737
D_CN(11)	J29	Input	LVDS	DDR	Differential	Data, negative	737
D_CN(12)	D26	Input	LVDS	DDR	Differential	Data, negative	737
D_CN(13)	H26	Input	LVDS	DDR	Differential	Data, negative	739
D_CN(14)	E29	Input	LVDS	DDR	Differential	Data, negative	736
D_CN(15)	G29	Input	LVDS	DDR	Differential	Data, negative	737
D_CP(0)	C17	Input	LVDS	DDR	Differential	Data, positive	738
D_CP(1)	E17	Input	LVDS	DDR	Differential	Data, positive	737
D_CP(2)	A15	Input	LVDS	DDR	Differential	Data, positive	735
D_CP(3)	F22	Input	LVDS	DDR	Differential	Data, positive	737
D_CP(4)	B22	Input	LVDS	DDR	Differential	Data, positive	737
D_CP(5)	H20	Input	LVDS	DDR	Differential	Data, positive	737
D_CP(6)	D20	Input	LVDS	DDR	Differential	Data, positive	737
D_CP(7)	E21	Input	LVDS	DDR	Differential	Data, positive	737
D_CP(8)	B28	Input	LVDS	DDR	Differential	Data, positive	739

Pin Functions (continued)

PIN [1]		TYPE (I/O/P)	SIGNAL	DATA RATE [2]	INTERNAL TERM [3]	DESCRIPTION	TRACE (mils) [4]
NAME	NO.						
D_CP(9)	F26	Input	LVDS	DDR	Differential	Data, positive	735
D_CP(10)	C29	Input	LVDS	DDR	Differential	Data, positive	737
D_CP(11)	J27	Input	LVDS	DDR	Differential	Data, positive	737
D_CP(12)	D28	Input	LVDS	DDR	Differential	Data, positive	736
D_CP(13)	H28	Input	LVDS	DDR	Differential	Data, positive	739
D_CP(14)	E27	Input	LVDS	DDR	Differential	Data, positive	736
D_CP(15)	G27	Input	LVDS	DDR	Differential	Data, positive	737
DATA BUS D							
D_DN(0)	AJ15	Input	LVDS	DDR	Differential	Data, negative	737
D_DN(1)	AC27	Input	LVDS	DDR	Differential	Data, negative	737
D_DN(2)	AK16	Input	LVDS	DDR	Differential	Data, negative	738
D_DN(3)	AE29	Input	LVDS	DDR	Differential	Data, negative	738
D_DN(4)	AE21	Input	LVDS	DDR	Differential	Data, negative	737
D_DN(5)	AF20	Input	LVDS	DDR	Differential	Data, negative	738
D_DN(6)	AL15	Input	LVDS	DDR	Differential	Data, negative	737
D_DN(7)	AG29	Input	LVDS	DDR	Differential	Data, negative	738
D_DN(8)	AD22	Input	LVDS	DDR	Differential	Data, negative	739
D_DN(9)	AG21	Input	LVDS	DDR	Differential	Data, negative	738
D_DN(10)	AJ23	Input	LVDS	DDR	Differential	Data, negative	736
D_DN(11)	AJ29	Input	LVDS	DDR	Differential	Data, negative	737
D_DN(12)	AF28	Input	LVDS	DDR	Differential	Data, negative	737
D_DN(13)	AK22	Input	LVDS	DDR	Differential	Data, negative	741
D_DN(14)	AD28	Input	LVDS	DDR	Differential	Data, negative	739
D_DN(15)	AK28	Input	LVDS	DDR	Differential	Data, negative	739
D_DP(0)	AJ17	Input	LVDS	DDR	Differential	Data, positive	737
D_DP(1)	AC29	Input	LVDS	DDR	Differential	Data, positive	737
D_DP(2)	AK14	Input	LVDS	DDR	Differential	Data, positive	738
D_DP(3)	AE27	Input	LVDS	DDR	Differential	Data, positive	737
D_DP(4)	AD20	Input	LVDS	DDR	Differential	Data, positive	737
D_DP(5)	AF22	Input	LVDS	DDR	Differential	Data, positive	738
D_DP(6)	AL17	Input	LVDS	DDR	Differential	Data, positive	737
D_DP(7)	AG27	Input	LVDS	DDR	Differential	Data, positive	738
D_DP(8)	AE23	Input	LVDS	DDR	Differential	Data, positive	739
D_DP(9)	AG23	Input	LVDS	DDR	Differential	Data, positive	738
D_DP(10)	AJ21	Input	LVDS	DDR	Differential	Data, positive	736
D_DP(11)	AJ27	Input	LVDS	DDR	Differential	Data, positive	737
D_DP(12)	AF26	Input	LVDS	DDR	Differential	Data, positive	737
D_DP(13)	AK20	Input	LVDS	DDR	Differential	Data, positive	740
D_DP(14)	AD26	Input	LVDS	DDR	Differential	Data, positive	739
D_DP(15)	AK26	Input	LVDS	DDR	Differential	Data, positive	739
SERIAL CONTROL							
SCTRL_AN	D8	Input	LVDS	DDR	Differential	Serial control, negative	736
SCTRL_BN	AK8	Input	LVDS	DDR	Differential	Serial control, negative	739
SCTRL_CN	G23	Input	LVDS	DDR	Differential	Serial control, negative	737
SCTRL_DN	AH28	Input	LVDS	DDR	Differential	Serial control, negative	739
SCTRL_AP	D10	Input	LVDS	DDR	Differential	Serial control, positive	736
SCTRL_BP	AK10	Input	LVDS	DDR	Differential	Serial control, positive	739
SCTRL_CP	H22	Input	LVDS	DDR	Differential	Serial control, positive	739
SCTRL_DP	AH26	Input	LVDS	DDR	Differential	Serial control, positive	739

Pin Functions (continued)

PIN [1]		TYPE (I/O/P)	SIGNAL	DATA RATE [2]	INTERNAL TERM [3]	DESCRIPTION	TRACE (mils) [4]
NAME	NO.						
CLOCKS							
DCLK_AN	H2	Input	LVDS		Differential	Clock, negative	740
DCLK_BN	AJ5	Input	LVDS		Differential	Clock, negative	740
DCLK_CN	C23	Input	LVDS		Differential	Clock, negative	736
DCLK_DN	AH22	Input	LVDS		Differential	Clock, negative	736
DCLK_AP	H4	Input	LVDS		Differential	Clock, positive	740
DCLK_BP	AJ3	Input	LVDS		Differential	Clock, positive	740
DCLK_CP	C21	Input	LVDS		Differential	Clock, positive	736
DCLK_DP	AH20	Input	LVDS		Differential	Clock, positive	738
SERIAL COMMUNICATIONS PORT (SCP)							
SCP_DO	AC3	Output	LVCMOS	SDR		Serial communications port output	
SCP_DI	AD2	Input	LVCMOS	SDR	Pull-Down	Serial communications port data input	
SCP_CLK	AE1	Input	LVCMOS		Pull-Down	Serial communications port clock	
SCP_ENZ	AD4	Input	LVCMOS		Pull-Down	Active-low serial communications port enable	
MICROMIRROR RESET CONTROL							
RESET_ADDR(0)	H12	Input	LVCMOS		Pull-Down	Reset driver address select	
RESET_ADDR(1)	C5	Input	LVCMOS		Pull-Down	Reset driver address select	
RESET_ADDR(2)	B6	Input	LVCMOS		Pull-Down	Reset driver address select	
RESET_ADDR(3)	A19	Input	LVCMOS		Pull-Down	Reset driver address select	
RESET_MODE(0)	J1	Input	LVCMOS		Pull-Down	Reset driver mode select	
RESET_MODE(1)	G1	Input	LVCMOS		Pull-Down	Reset driver mode select	
RESET_SEL(0)	AK4	Input	LVCMOS		Pull-Down	Reset driver level select	
RESET_SEL(1)	AL13	Input	LVCMOS		Pull-Down	Reset driver level select	
RESET_STROBE	H6	Input	LVCMOS		Pull-Down	Reset address, mode, and level latched on rising-edge	
ENABLES AND INTERRUPTS							
PWRDNZ	B4	Input	LVCMOS			Active-low device reset	
RESET_OEZ	AK24	Input	LVCMOS		Pull-Down	Active-low output enable for DMD reset driver circuits	
RESETZ	AL19	Input	LVCMOS		Pull-Down	Active-low sets reset circuits in known V_{OFFSET} state	
RESET_IRQZ	C3	Output	LVCMOS			Active-low, output interrupt to ASIC	
VOLTAGE REGULATOR MONITORING							
PG_BIAS	J19	Input	LVCMOS		Pull-Up	Active-low fault from external V_{BIAS} regulator	
PG_OFFSET	A13	Input	LVCMOS		Pull-Up	Active-low fault from external V_{OFFSET} regulator	
PG_RESET	AC19	Input	LVCMOS		Pull-Up	Active-low fault from external V_{RESET} regulator	
EN_BIAS	J15	Output	LVCMOS			Active-high enable for external V_{BIAS} regulator	
EN_OFFSET	H30	Output	LVCMOS			Active-high enable for external V_{OFFSET} regulator	
EN_RESET	J17	Output	LVCMOS			Active-high enable for external V_{RESET} regulator	
LEAVE PIN UNCONNECTED							
MBRST(0)	L5	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(1)	M28	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(2)	P4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(3)	P30	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(4)	L3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(5)	P28	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(6)	P2	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(7)	T28	Output	Analog		Pull-Down	For proper DMD operation, do not connect	

Pin Functions (continued)

PIN [1]		TYPE (I/O/P)	SIGNAL	DATA RATE [2]	INTERNAL TERM [3]	DESCRIPTION	TRACE (mils) [4]
NAME	NO.						
MBRST(8)	M4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(9)	L29	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(10)	T4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(11)	N29	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(12)	N3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(13)	L27	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(14)	R3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(15)	V28	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(16)	V4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(17)	R29	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(18)	Y4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(19)	AA27	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(20)	W3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(21)	W27	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(22)	AA3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(23)	W29	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(24)	U5	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(25)	U29	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(26)	Y2	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(27)	AA29	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(28)	U3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(29)	Y30	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(30)	AA5	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(31)	R27	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
LEAVE PIN UNCONNECTED							
RESERVED_PFE	J11	Input	LVCMOS		Pull-Down	For proper DMD operation, do not connect	
RESERVED_TM	AC7	Input	LVCMOS		Pull-Down	For proper DMD operation, do not connect	
RESERVED_XI0	AC25	Input	LVCMOS		Pull-Down	For proper DMD operation, do not connect	
RESERVED_XI1	AC23	Input	LVCMOS		Pull-Down	For proper DMD operation, do not connect	
RESERVED_XI2	J23	Input	LVCMOS		Pull-Down	For proper DMD operation, do not connect	
RESERVED_TP0	AC9	Input	Analog			For proper DMD operation, do not connect	
RESERVED_TP1	AC11	Input	Analog			For proper DMD operation, do not connect	
RESERVED_TP2	AC13	Input	Analog			For proper DMD operation, do not connect	
LEAVE PIN UNCONNECTED							
RESERVED_BA	AC15	Output	LVCMOS			For proper DMD operation, do not connect	
RESERVED_BB	J13	Output	LVCMOS			For proper DMD operation, do not connect	
RESERVED_BC	AC21	Output	LVCMOS			For proper DMD operation, do not connect	
RESERVED_BD	J21	Output	LVCMOS			For proper DMD operation, do not connect	
RESERVED_TS	AC17	Output	LVCMOS			For proper DMD operation, do not connect	
LEAVE PIN UNCONNECTED							
NO CONNECT	J7					For proper DMD operation, do not connect	
NO CONNECT	J9					For proper DMD operation, do not connect	
NO CONNECT	J25					For proper DMD operation, do not connect	

Pin Functions

PIN		TYPE (I/O/P)	SIGNAL	DESCRIPTION
NAME (1)	NO.			
V_{BIAS}	A3, A9, A5, A11, A7, B2	Power	Analog	Supply voltage for positive bias level of micromirror reset signal.
V_{OFFSET}	L1, N1, R1	Power	Analog	Supply voltage for HVCMOS logic.
	U1, W1	Power	Analog	Supply voltage for stepped high voltage at micromirror address electrodes.
	AC1, AA1	Power	Analog	Supply voltage for offset level of MBRST(31:0).
V_{RESET}	L31, N31, R31, U31, W31, AA31	Power	Analog	Supply voltage for negative reset level of micromirror reset signal.
V_{CC}	A21, A23, A25, A27, A29, C1, C31, E31, G31, J31, K2, AC31, AE31, AG1, AG31, AJ31, AK2, AK30, AL3, AL5, AL7, AL21, AL23, AL25, AL27	Power	Analog	Supply voltage for LVCMOS core logic. Supply voltage for normal high level at micromirror address electrodes.
V_{CCI}	H18, H24, M6, M26, P6, P26, T6, T26, V6, V26, Y6, Y26, AD6, AD12, AD18, AD24	Power	Analog	Supply voltage for LVDS receivers.
V_{SS}	A1, B12, B18, B24, B30, C7, C13, C19, C25, D6, D12, D18, D24, D30, E1, E7, E13, E19, E25, F6, F12, F18, F24, F30, G7, G13, G19, G25, K4, K6, K26, K28, K30, M2, M30, N5, N27, R5, T2, T30, U27, V2, V30, W5, Y28, AB2, AB4, AB6, AB26, AB28, AB30, AC5, AD30, AE7, AE13, AE19, AE25, AF6, AF12, AF18, AF24, AF30, AG7, AG13, AG19, AG25, AH6, AH12, AH18, AH24, AH30, AJ1, AJ7, AJ13, AJ19, AJ25, AK6, AK12, AK18, AL29	Power	Analog	Device ground. Common return for all power.

(1) The following power supplies are required to operate the DMD: V_{CC}, V_{CCI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. V_{SS} must also be connected.

6 Specifications

6.1 Absolute Maximum Ratings

See (1).

		MIN	MAX	UNIT
SUPPLY VOLTAGES				
V_{CC}	Supply voltage for LVCMOS core logic (2)	–0.5	4	V
V_{CCI}	Supply voltage for LVDS receivers (2)	–0.5	4	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode (2) (3)	–0.5	9	V
V_{BIAS}	Supply voltage for micromirror electrode (2)	–0.5	17	V
V_{RESET}	Supply voltage for micromirror electrode (2)	–11	0.5	V
$\lvert V_{CC} - V_{CCI} \rvert$	Supply voltage delta (absolute value) (4)		0.3	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta (absolute value) (5)		8.75	V
INPUT VOLTAGES				
	Input voltage for all other LVCMOS input pins (2)	–0.5	V_{CC} + 0.3	V
	Input voltage for all other LVDS input pins (2) (6)	–0.5	V_{CCI} + 0.3	V
$\lvert V_{ID} \rvert$	Input differential voltage (absolute value) (7)		700	mV
I_{ID}	Input differential current (7)		7	mA
CLOCKS				
f_{clock}	Clock frequency for LVDS interface, DCLK_A		500	MHz
	Clock frequency for LVDS interface, DCLK_B		500	
	Clock frequency for LVDS interface, DCLK_C		500	
	Clock frequency for LVDS interface, DCLK_D		500	
ENVIRONMENTAL				
T_{ARRAY}	Array temperature: Operational (8)	20	30	ºC
	Array temperature: Non–operational (8)	–40	90	
T_{WINDOW}	Window temperature: Operational	20	30	ºC
	Window temperature: Non–operational	–40	90	
$\lvert T_{DELTA} \rvert$	Absolute temperature delta between the window test points and the ceramic test point TP1 (9)		10	ºC
R_H	Relative humidity, operating and non–operating		95	%

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure above *Recommended Operating Conditions* for extended periods may affect device reliability.
(2) All voltages are referenced to common ground V_{SS}. Supply voltages V_{CC}, V_{CCI}, V_{OFFSET}, V_{BIAS}, and V_{RESET} are all required for proper DMD operation. V_{SS} must also be connected.
(3) V_{OFFSET} supply transients must fall within specified voltages.
(4) To prevent excess current, the supply voltage delta $\lvert V_{CCI} - V_{CC} \rvert$ must be less than specified limit.
(5) To prevent excess current, the supply voltage delta $\lvert V_{BIAS} - V_{OFFSET} \rvert$ must be less than specified limit. Refer to *Power Supply Requirements* for additional information.
(6) This maximum LVDS input voltage rating applies when each input of a differential pair is at the same voltage potential.
(7) LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(8) The highest temperature of the active array as calculated by the *Micromirror Array Temperature Calculation* using ceramic test point 1 (TP1) in Figure 15.
(9) Temperature delta is the highest difference between the ceramic test point TP1 and window test points TP2 and TP3 in Figure 15.

6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	80	°C
R_H	Relative humidity, (non-condensing)		95	%

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGES (2)					
V_{CC}	Supply voltage for LVCMOS core logic	3.3	3.45	3.6	V
V_{CCI}	Supply voltage for LVDS receivers	3.3	3.45	3.6	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrodes (3)	8.25	8.5	8.75	V
V_{BIAS}	Supply voltage for micromirror electrodes	15.5	16	16.5	V
V_{RESET}		–9.5	–10	–10.5	V
$\lvert V_{CCI}–V_{CC}\rvert$	Supply voltage delta (absolute value) (4)			0.3	V
$\lvert V_{BIAS}–V_{OFFSET}\rvert$	Supply voltage delta (absolute value) (5)			8.75	V
LVCMOS PINS					
V_{IH}	High level Input voltage (6)	1.7	2.5	VCC + 0.3	V
V_{IL}	Low level Input voltage (6)	–0.3		0.7	V
I_{OH}	High level output current at V_{OH} = 2.4 V			–20	mA
I_{OL}	Low level output current at V_{OL} = 0.4 V			15	mA
T_{PWRDNZ}	PWRDNZ pulse width (7)	10			ns
SCP INTERFACE					
f_{clock}	SCP clock frequency (8)			500	kHz
t_{SCP_SKEW}	Time between valid SCPDI and rising edge of SCPCLK (9)	–800		800	ns
t_{SCP_DELAY}	Time between valid SCPDO and rising edge of SCPCLK (9)			700	ns
$t_{SCP\_BYTE\_INTERVAL}$	Time between consecutive bytes	1			µs
$t_{SCP\_NEG\_ENZ}$	Time between falling edge of SCPENZ and the first rising edge of SCPCLK	30			ns
$t_{SCP\_PW\_ENZ}$	SCPENZ inactive pulse width (high level)	1			µs
$t_{SCP\_OUT\_EN}$	Time required for SCP output buffer to recover after SCPENZ (from tri-state)			1.5	ns
f_{clock}	SCP circuit clock oscillator frequency (10)	9.6		11.1	MHz

(1) The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.
(2) Supply voltages V_{CC}, V_{CCI}, V_{OFFSET}, V_{BIAS}, and V_{RESET} are all required for proper DMD operation. V_{SS} must also be connected. All voltages are referenced to common ground V_{SS}.
(3) V_{OFFSET} supply transients must fall within specified max voltages.
(4) To prevent excess current, the supply voltage delta $|V_{CCI} – V_{CC}|$ must be less than the specified limit.
(5) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit. Refer to *Power Supply Requirements* for additional information.
(6) Tester conditions for V_{IH} and V_{IL}:
Frequency = 60 MHz. Maximum rise time = 2.5 ns at (20% to 80%)
Frequency = 60 MHz. Maximum fall time = 2.5 ns at (80% to 20%)
(7) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tri-states the SCPDO output pin.
(8) The SCP clock is a gated clock. Duty cycle shall be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
(9) Refer to Figure 1.
(10) SCP internal oscillator is specified to operate all SCP registers. For all SCP operations, DCLK is required.

Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
LVDS INTERFACE						
f_{clock}	Clock frequency DCLK (11)		400	400 or 480	480	MHz
$\|V_{ID}\|$	Input differential voltage (absolute value) (12)		100	400	600	mV
V_{CM}	Common mode (12)			1200		mV
V_{LVDS}	LVDS voltage (12)		0		2000	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ				10	ns
Z_{IN}	Internal differential termination resistance		95		105	Ω
Z_{LINE}	Line differential impedance (PWB/trace)		90	100	110	Ω
ENVIRONMENTAL(13)						
ILL_{PD} and ILL_{TP}	Illumination power density and illumination total power on the array(14)	Total combined <353 nm(15)			10	mW/cm^2
		Max per single wavelength(16) 355 nm to 365 nm			2.5	W/cm^2
					5.8	W
		Total Combined 355 nm to 365 nm			2.5	W/cm^2
					5.8	W
		Max per single wavelength(16) 365 nm to 400 nm			5	W/cm^2
					11.6	W
		Total Combined 365 nm to 400 nm			10	W/cm^2
					23.3	W
		Max per single wavelength(16) 400 nm to 420 nm			15	W/cm^2
					34.8	W
		Total Combined 400 nm to 420 nm			15	W/cm^2
					34.8	W
		Total Combined 355 nm to 420 nm			15	W/cm^2
					34.8	W
		Total Combined >420 nm(17)			Thermally Limited	W/cm^2
T_{ARRAY}	Array temperature(18) (19)		20		30	°C
T_{WINDOW}	Window temperature measured at test points TP2 and TP3		20		30	°C
$\|T_{DELTA}\|$	Absolute temperature delta between the window test points (TP2, TP3) and the ceramic test point TP1.(20)				10	°C
RH	Relative Humidity (non-condensing)				95	%
	Operating Landed Duty Cycle(21)			50		%

(11) The DLP9000XUV DMD, coupled with the DLPC910, is designed for operation at 2 specific DCLK frequencies only: 400 MHz or 480 MHz, but not random values in between.
(12) Refer to Figure 2, Figure 3, and Figure 4.
(13) Optimal, long-term performance and optical efficiency of the digital micromirror device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty-cycle, ambient temperature (storage and operating), DMD temperature, ambient humidity (storage and operating), and power on or off duty cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle.
(14) This is the illumination power density and illumination total power input to the DMD micromirror array and does not include illumination overfill of the DMD device outside the active array.
(15) Any 355 nm or higher illumination source must use a cutoff filter to be at or below this power level by 353 nm. Illumination power from 355 nm down to 353 nm is expected to be diminishing such that the maximum power limit at 353 nm can be achieved.
(16) Integrated power in any single 3 nm band.
(17) Limited by the resulting micromirror array temperature. Refer to T_{ARRAY}, $|T_{DELTA}|$, and Micromirror Array Temperature Calculation for information related to verifying the DMD temperature meets its requirements.
(18) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in Figure 15 and the package thermal resistance in *Thermal Information* using *Micromirror Array Temperature Calculation*.
(19) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination will reduce device lifetime.
(20) Temperature delta is the highest difference between the ceramic test point (TP1) and window test points (TP2) and (TP3) in Figure 15.
(21) Landed duty cycle refers to the percentage of time an individual micromirror spends landed in one state (12° or –12°) versus the opposite state (–12° or 12°). 50% equates to a 50/50 duty cycle where the mirror has been landed 50% in the On-state and 50% in the Off-state. See Micromirror Landed-On/Landed-Off Duty Cycle for more information on Landed Duty Cycle.

6.5 Thermal Information

THERMAL METRIC (1)	DLP9000XUV FLS (CLGA) 355 PINS	UNIT
Thermal resistance, active area to test point 1 (TP1)	0.5	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 3.0 V, I_{OH} = –20 mA	2.4			V
V_{OL}	Low level output voltage	V_{CC} = 3.6 V, I_{OL} = 15 mA			0.4	V
I_{IH}	High–level input current (2) (3)	V_{CC} = 3.6 V, V_I = VCC			250	µA
IIL	Low level input current	V_{CC} = 3.6 V, V_I = 0	–250			µA
I_{OZ}	High–impedance output current	V_{CC} = 3.6 V			10	µA
CURRENT						
I_{CC}	Supply current (4)	V_{CC} = 3.6 V, DCLK = 480 MHz			1850	mA
I_{CCI}		V_{CCI} = 3.6 V, DCLK = 480 MHz			1100	
I_{OFFSET}	Supply current (5)	V_{OFFSET} = 8.75 V			25	mA
I_{BIAS}		V_{BIAS} = 16.5 V			14	
I_{RESET}	Supply current	V_{RESET} = –10.5 V			11	mA
I_{TOTAL}		DLP9000XUV Total Sum			3000	
POWER						
P_{CC}	Supply power dissipation	V_{CC} = 3.6 V			6660	mW
P_{CCI}		V_{CCI} = 3.6 V			3960	mW
P_{OFFSET}		V_{OFFSET} = 8.75 V			219	mW
P_{BIAS}		V_{BIAS} = 16.5 V			231	mW
P_{RESET}		V_{RESET} = –10.5 V			115	mW
P_{TOTAL}	Supply power dissipation	Total sum, DCLK = 480 MHz			11185	mW
CAPACITANCE						
C_I	Input capacitance	f = 1 MHz			10	pF
C_O	Output capacitance	f = 1 MHz			10	pF
	Reset group capacitance MBRST(31:0)	f = 1 MHz; 2560 × 50 micromirrors	230		290	pF

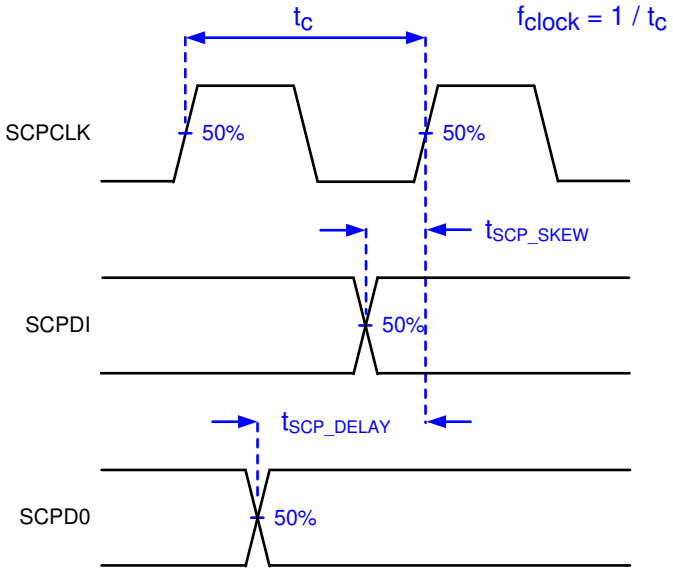
(1) All voltages are referenced to common ground V_{SS}. Supply voltages V_{CC}, V_{CCI}, V_{OFFSET}, V_{BIAS}, and V_{RESET} are all required for proper DMD operation. V_{SS} must also be connected.
(2) Applies to LVCMOS input pins only. Does not apply to LVDS pins and MBRST pins.
(3) LVCMOS input pins utilize an internal 18000 Ω passive resistor for pull-up and pull-down configurations. Refer to *Pin Configuration and Functions* to determine pull-up or pull-down configuration used.
(4) To prevent excess current, the supply voltage delta $|V_{CCI} – V_{CC}|$ must be less than the specified limit.
(5) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit.

6.7 Timing Requirements

Over *Recommended Operating Conditions* (unless otherwise noted) (1)

			MIN	NOM	MAX	UNIT
SCP INTERFACE (2)						
t_r	Rise time	20% to 80%			200	ns
t_f	Fall time	80% to 20%			200	ns
LVDS INTERFACE (2)						
t_r	Rise time	20% to 80%	100		400	ps
t_f	Fall time	80% to 20%	100		400	ps
LVDS CLOCKS (3)						
t_c	Cycle time	DCLK_A, 50% to 50%	2.083			ns
		DCLK_B, 50% to 50%	2.083			
		DCLK_C, 50% to 50%	2.083			
		DCLK_D, 50% to 50%	2.083			
t_w	Pulse duration	DCLK_A, 50% to 50%	1.031	1.042		ns
		DCLK_B, 50% to 50%	1.031	1.042		
		DCLK_C, 50% to 50%	1.031	1.042		
		DCLK_D, 50% to 50%	1.031	1.042		
LVDS INTERFACE (3)						
t_{su}	Setup time	D_A(15:0) before rising or falling edge of DCLK_A	0.2			ns
		D_B(15:0) before rising or falling edge of DCLK_B	0.2			
		D_C(15:0) before rising or falling edge of DCLK_C	0.2			
		D_D(15:0) before rising or falling edge of DCLK_D	0.2			
t_h	Hold time	D_A(15:0) after rising or falling edge of DCLK_A	0.4			ns
		D_B(15:0) after rising or falling edge of DCLK_B	0.4			
		D_C(15:0) after rising or falling edge of DCLK_C	0.4			
		D_D(15:0) after rising or falling edge of DCLK_D	0.4			
LVDS INTERFACE (3)						
t_{skew}	Skew time	Channel A includes the following LVDS pairs: DCLK_AP and DCLK_AN SCTRL_AP and SCTRL_AN D_AP(15:0) and D_AN(15:0)	–1.04		1.04	ns
		Channel B includes the following LVDS pairs: DCLK_BP and DCLK_BN SCTRL_BP and SCTRL_BN D_BP(15:0) and D_BN(15:0)				
		Channel C includes the following LVDS pairs: DCLK_CP and DCLK_CN SCTRL_CP and SCTRL_CN D_CP(15:0) and D_CN(15:0)	–1.04		1.04	ns
		Channel D includes the following LVDS pairs: DCLK_DP and DCLK_DN SCTRL_DP and SCTRL_DN D_DP(15:0) and D_DN(15:0)				

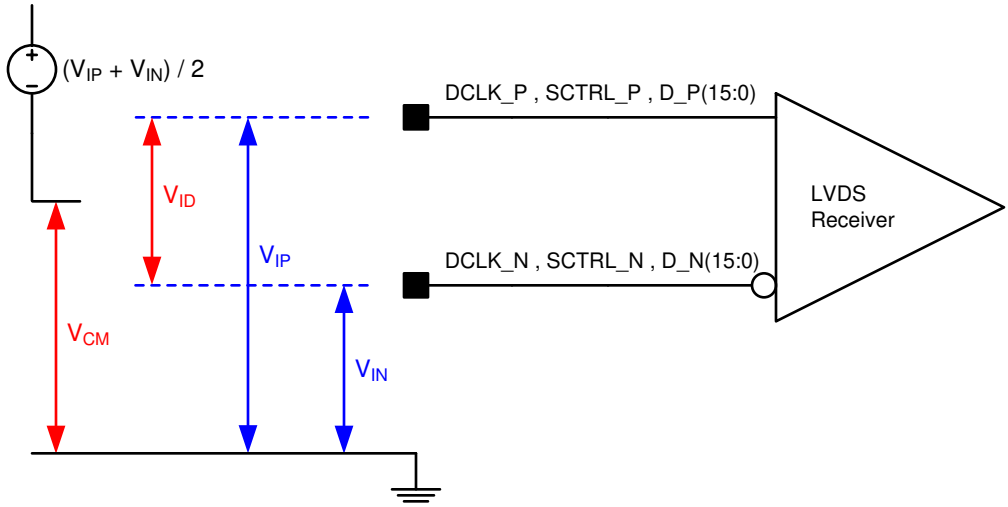
(1) Refer to *Pin Configuration and Functions* for pin details.
(2) Refer to Figure 5.
(3) Refer to Figure 6.



Not to scale.

Refer to SCP Interface section of the *Recommended Operating Conditions*.

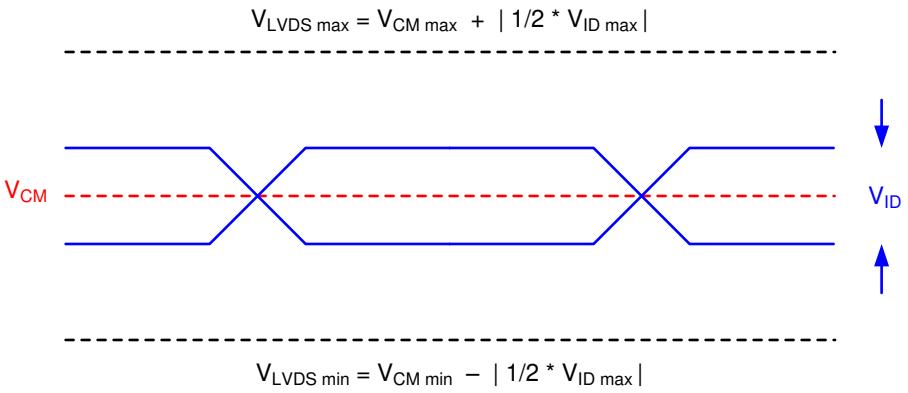
Figure 1. SCP Timing Parameters



Refer to LVDS Interface section of the *Recommended Operating Conditions* table.

Refer to *Pin Configuration and Functions* for a list of LVDS pins.

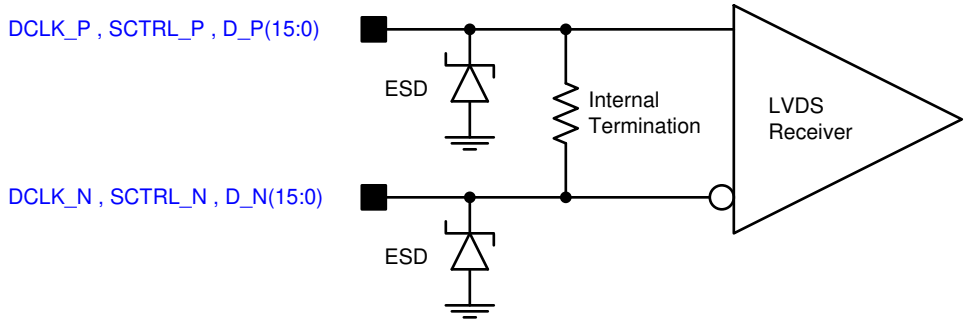
Figure 2. LVDS Voltage Definitions (References)



Not to scale.

Refer to LVDS Interface section of the *Recommended Operating Conditions* table.

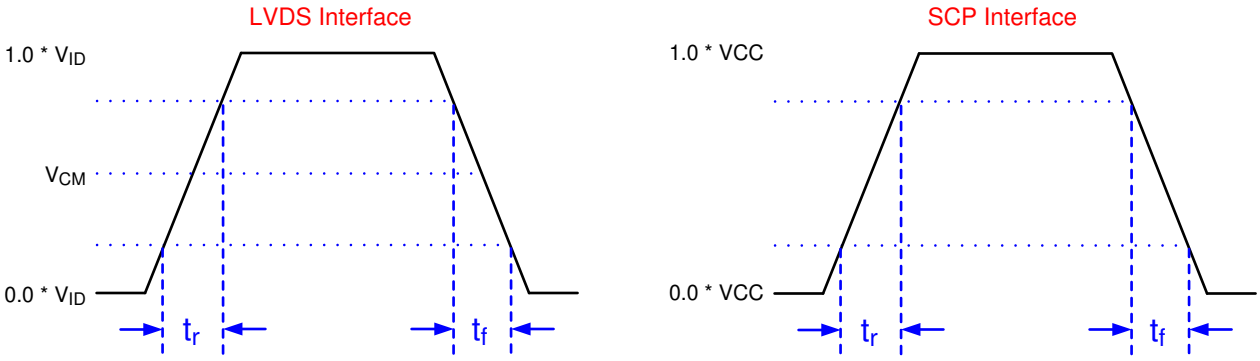
Figure 3. LVDS Voltage Parameters



Refer to LVDS Interface section of the *Recommended Operating Conditions* table.

Refer to *Pin Configuration and Functions* for list of LVDS pins.

Figure 4. LVDS Equivalent Input Circuit

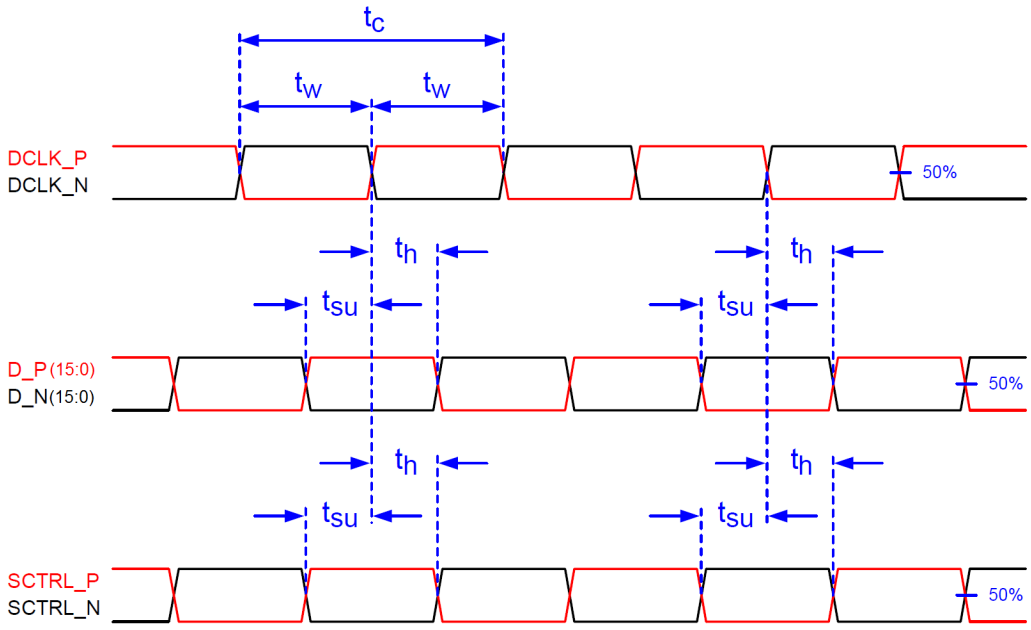


Not to scale.

Refer to the Timing Requirements in *Timing Requirements*.

Refer to *Pin Configuration and Functions* for a list of LVDS pins and SCP pins.

Figure 5. Rise Time and Fall Time



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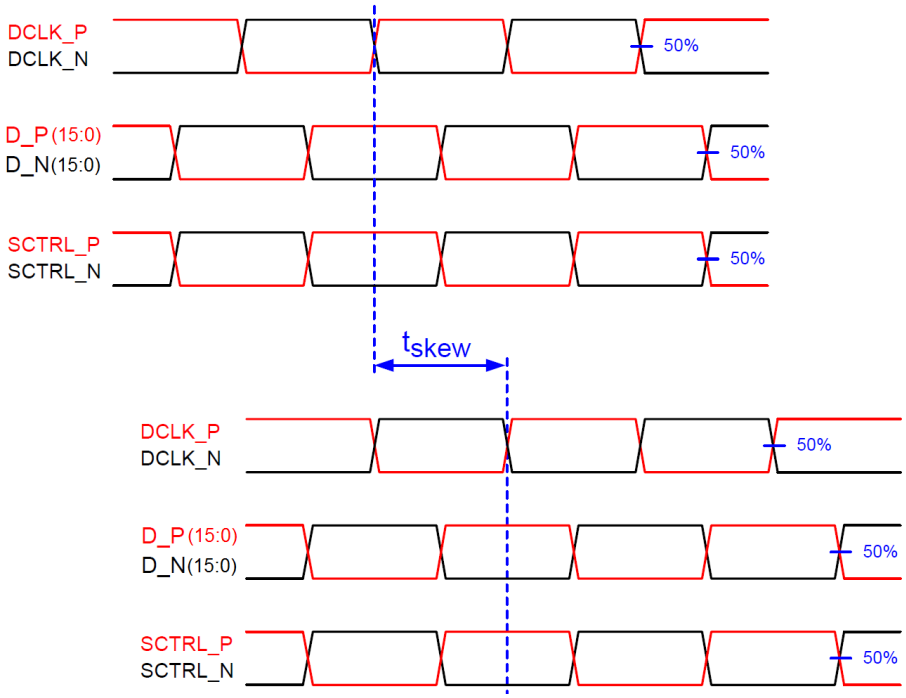
Refer to LVDS INTERFACE section in the *Timing Requirements* table.

Figure 6. Timing Requirement Parameter Definitions



Not to scale.

Refer to LVDS INTERFACE section in the *Timing Requirements* table.

Figure 7. LVDS Interface Channel Skew Definition

6.8 Capacitance at Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C_I	Input capacitance	f = 1 MHz		10	pF
C_O	Output capacitance	f = 1 MHz		10	pF
C_{IM}	MBRST(31:0) input capacitance	f = 1 MHz. All inputs interconnected.	230	290	pF

6.9 Typical Characteristics

When the DLP9000XUV DMD is controlled by the DLPC910 controller, the digital controller offers streaming 1-bit binary patterns to the DMD at speeds greater than 61 Gigabits per second (Gbps). The patterns are streamed from a customer designed applications processor into the DLPC910 input LVDS data interface. Table 1 shows the pattern rates for the different DMD reset modes.

Table 1. DLPC910 with DLP9000XUV DMD Pattern Rates versus Reset Mode

RESET MODE (1)	MAX PIXEL DATA RATE (Gbps) (2)	MAX PATTERN RATE (Hz) (3)
Global	53.42	13043
Single	56.46	13783 (4)
Dual	59.89	14624 (4)
Quad	61.39	14989 (4)

(1) Refer to the DLPC910 data sheet in *Related Documentation* for a description of the reset modes.
(2) Pixel data rates are based on continuous streaming.
(3) Increasing exposure periods may be necessary for a desired application but may decrease pattern rate.
(4) This reset mode typically requires pulsed illumination such as a laser or LED.

6.10 System Mounting Interface Loads

PARAMETER		MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:	Thermal interface area (See Figure 8) (1)(2)			156	N
	Electrical interface area (1)(2)			1334	N
	Datum *A* interface area (1)(2)			712	N

(1) Refer to the DMD Mounting Concepts guide in *Related Documentation* for more DMD mounting information.
(2) Combined loads of the thermal and electrical interface areas in excess of Datum "A" load shall be evenly distributed outside the Datum *A* area (1334 + 156 – Datum *A*).

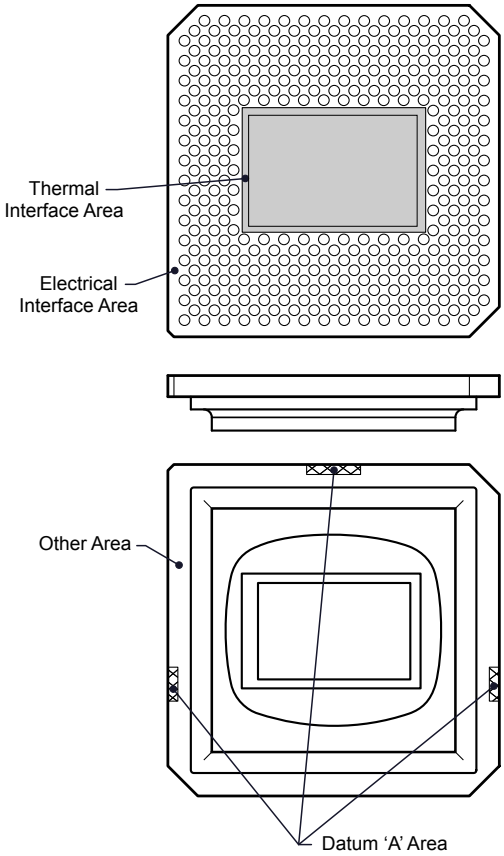
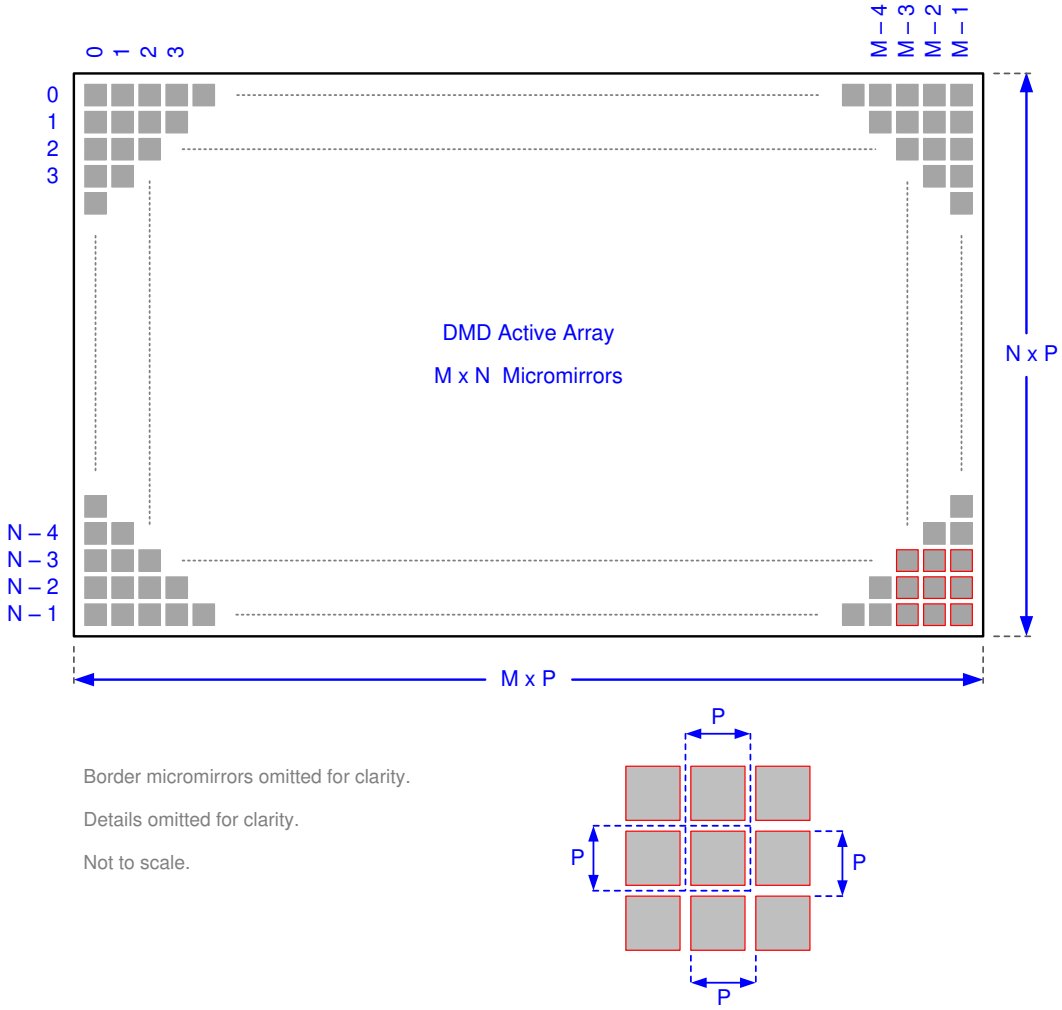


Figure 8. System Mounting Interface Loads

6.11 Micromirror Array Physical Characteristics

				VALUE	UNIT
M	Number of active columns		See Figure 9	2560	micromirrors
N	Number of active rows			1600	micromirrors
P	Micromirror (pixel) pitch			7.56	µm
	Micromirror active array width	M × P		19.3536	mm
	Micromirror active array height	N × P		12.096	mm
	Micromirror active border	Pond of micromirror (POM) (1)		14	micromirrors/side
	Micromirror total area	P^2 × M × N (converted to cm)		2.341	cm^2

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.



Refer to section *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

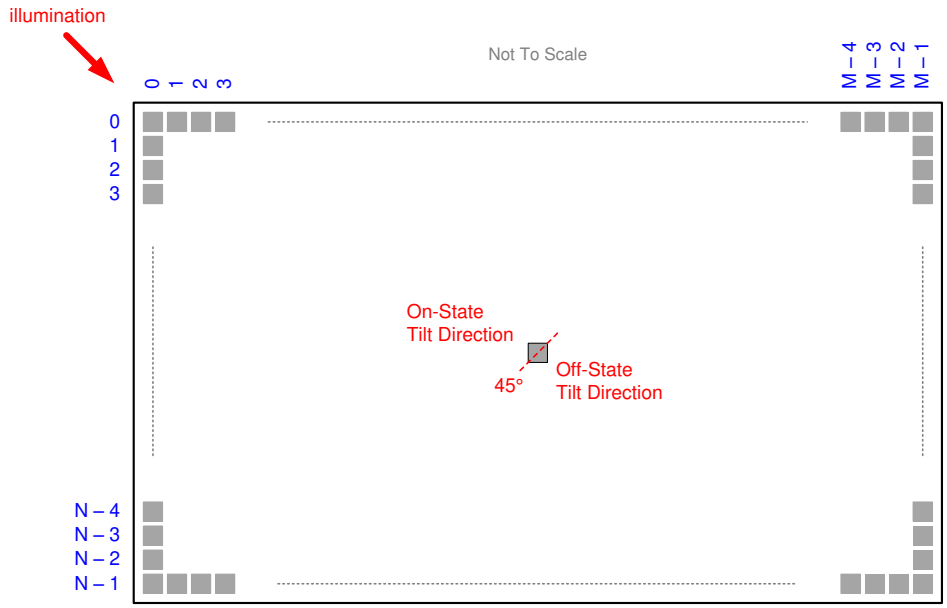
Figure 9. Micromirror Array Physical Characteristics

6.12 Micromirror Array Optical Characteristics

Refer to *Optical Interface and System Image Quality* for important information.

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
α Micromirror tilt angle (1)	Micromirror Landed State (2)		12		degree
β Micromirror tilt angle range tolerance (1)(2) (3) (4) (5) (6)		-1		1	degree
Micromirror Hinge Axis Orientation (7)	See Figure 10 and Figure 13	44	45	46	degree
Number of out-of-specification micromirrors (8)	Adjacent micromirrors			0	micromirrors
	Non-adjacent micromirrors			10	
Micromirror crossover time (9) (10)	Typical performance		2.5		µs
DMD efficiency within the wavelength range 355 nm to 420 nm (11)			68%		

(1) α and β are an average of 5 measured locations on the DMD.
(2) Measured relative to the plane formed by the overall micromirror array.
(3) Additional variation exists between the micromirror array and the package datums.
(4) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(5) Represents the positive tilt angle variation that can occur between any two individual micromirrors, located on the same device.
(6) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
(7) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction.
(8) An out-of-specification micromirror is defined as a micromirror that is unable to transition between the two landed states within the specified micromirror switching time.
(9) Micromirror crossover time is primarily a function of the natural response time of the micromirrors.
(10) Performance as measured at the start of life.
(11) Efficiency numbers assume 24-degree illumination angle, F/2.4 illumination and collection cones, uniform source spectrum, and uniform pupil illumination. Efficiency numbers assume 100% electronic mirror duty cycle and do not include optical overfill loss. Note that this number is specified under conditions described above and deviations from the specified conditions could result in decreased efficiency.



Refer to section *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

Figure 10. Micromirror Landed Orientation and Tilt

6.13 Optical and System Image Quality

Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, optical performance is contingent on compliance to the optical system operating conditions described in a) through c) below:

a. **Numerical Aperture and Stray Light Control:** The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, artifacts could occur in the projected image of the DMD border region and/or active area.

b. **Pupil Match:** TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within two degrees of the entrance pupil of the projection optics. Misalignment of pupils can create artifacts in the projection of the DMD border region and/or active area which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

c. **Illumination Overfill:** Overfill light illuminating the DMD area far enough outside the active array may strike mechanical features that surround the active array or other surface anomalies resulting in scattered or reflected light which may impact the projected image performance in certain customer applications. The illumination optical system should be designed to limit these artifacts by minimizing the amount of light incident outside the active array to the point where the image performance is in line with the expected application image performance. The design also needs to take into account the particular system's optical architecture and light engine assembly tolerances.

NOTE

TI ASSUMES NO RESPONSIBILITY FOR IMAGE QUALITY ARTIFACTS OR DMD FAILURES CAUSED BY OPTICAL SYSTEM OPERATING CONDITIONS EXCEEDING LIMITS DESCRIBED ABOVE.

6.14 Window Characteristics

PARAMETER (1)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Window material designation			Corning 7056		
Window refractive index	At wavelength 589 nm		1.487		
Window aperture	See (2)				
Illumination overfill	Refer to *Illumination Overfill*				
Window Artifact Size	Area within the window aperture only.			400	µm
Window transmittance, single–pass through both surfaces and glass (3)	Minimum within the wavelength range 355 nm to 420 nm. Applies to all angles 0° to 30° AOI.	97%			

(1) Refer to *Window Characteristics and Optics* for more information.
(2) For details regarding the size and location of the window aperture, refer to the package mechanical characteristics listed in the Mechanical ICD in the Mechanical, Packaging, and Orderable Information section.
(3) Refer to the TI application report DLPA031, *Wavelength Transmittance Considerations for DLP DMD Window*.

6.15 Chipset Component Usage Specification

The DMD is a component of one or more DLP® chipsets. Reliable function and operation of the DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices for operating or controlling a DMD.

7 Parameter Measurement Information

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. Figure 11 shows an equivalent test load circuit for the output under test. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Refer to the *Application and Implementation* section.

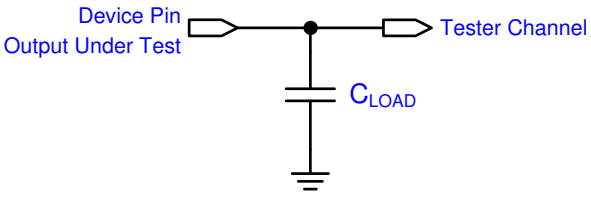


Figure 11. Test Load Circuit

8 Detailed Description

8.1 Overview

The DMD is a 0.9 inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. Pixel array size and square grid pixel arrangement are shown in Figure 9.

The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is Low Voltage Differential Signaling (LVDS), Double Data Rate (DDR).

The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of *M* memory cell columns by *N* memory cell rows. Refer to the *Functional Block Diagram*.

The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

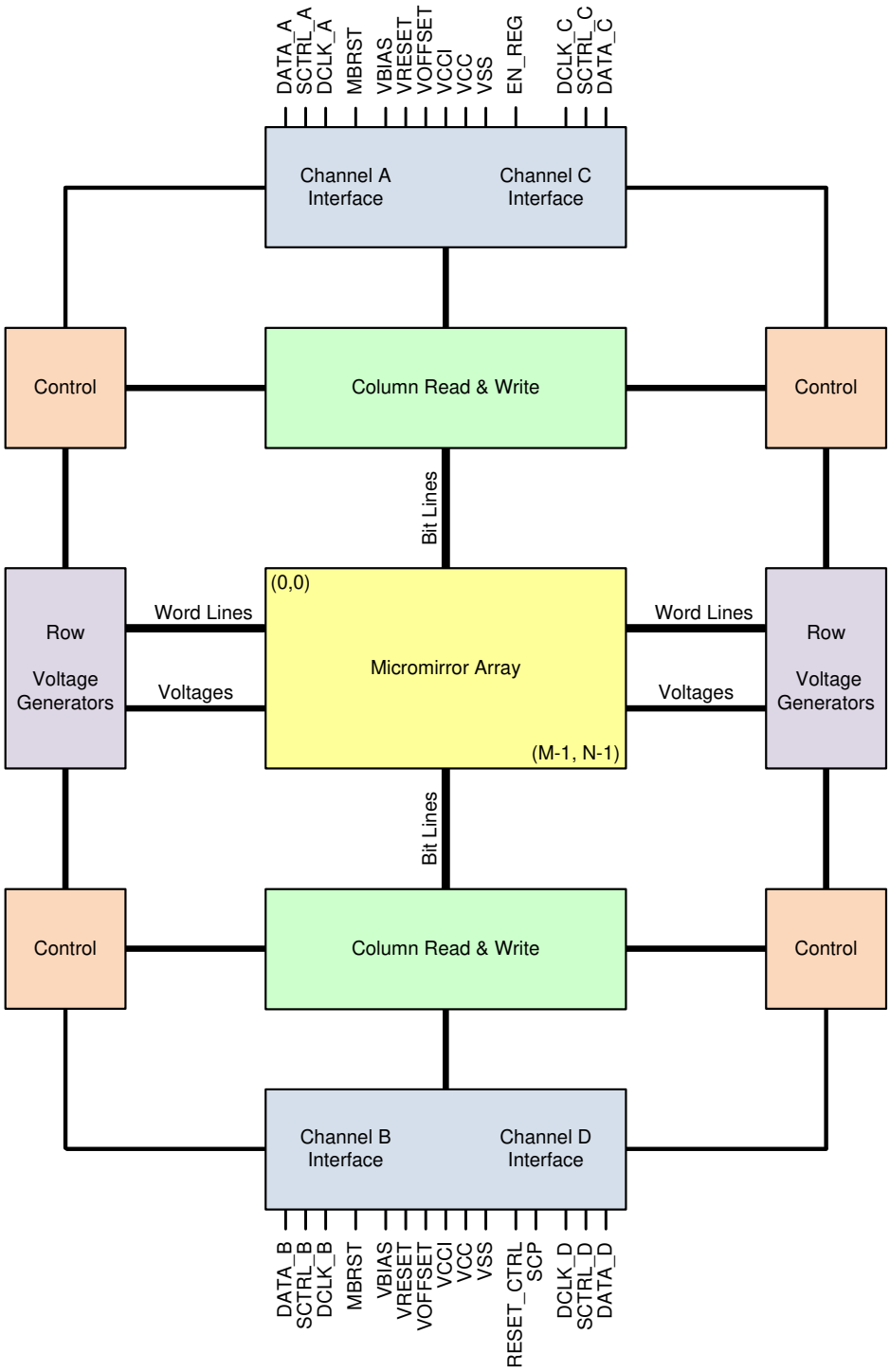
Each cell of the *M* × *N* memory array drives its true and complement ('Q' and 'QB') data to two electrodes underlying one micromirror, one electrode on each side of the diagonal axis of rotation. Refer to *Micromirror Array Optical Characteristics*. The micromirrors are electrically tied to the micromirror reset signals (MBRST) and the micromirror array is divided into reset groups.

Electrostatic potentials between a micromirror and its memory data electrodes cause the micromirror to tilt toward the illumination source in a DLP projection system or away from it, thus reflecting its incident light into or out of an optical collection aperture. The positive (+) tilt angle state corresponds to an 'on' pixel, and the negative (–) tilt angle state corresponds to an 'off' pixel.

Refer to *Micromirror Array Optical Characteristics* for the ± tilt angle specifications. Refer to *Pin Configuration and Functions* for more information on micromirror reset control.

8.2 Functional Block Diagram

Not to Scale. Details Omitted for Clarity. See Accompanying Notes in this Section.



For pin details on Channels A, B, C, and D, refer to *Pin Configuration and Functions* and LVDS Interface section of *Timing Requirements*.

Figure 12. Functional Block Diagram

8.3 Feature Description

The DMD consists of 4096000 highly reflective, digitally switchable, micrometer-sized mirrors (micromirrors) organized in a two-dimensional orthogonal pixel array. Refer to Figure 9 and Figure 13.

Each aluminum micromirror is switchable between two discrete angular positions, –α and +α. The angular positions are measured relative to the micromirror array plane, which is parallel to the silicon substrate. Refer to *Micromirror Array Optical Characteristics* and Figure 14.

The parked position of the DMD micromirrors is not an operational mode which is electrostatically driven. Therefore, the DMD micromirrors are not driven to a known landed position and the individual micromirror flat-state angular positions may vary from the DMD array plane. Tilt direction of the micromirror is perpendicular to the hinge-axis. The on-state landed position is directed toward the left-top edge of the package, as shown in Figure 13.

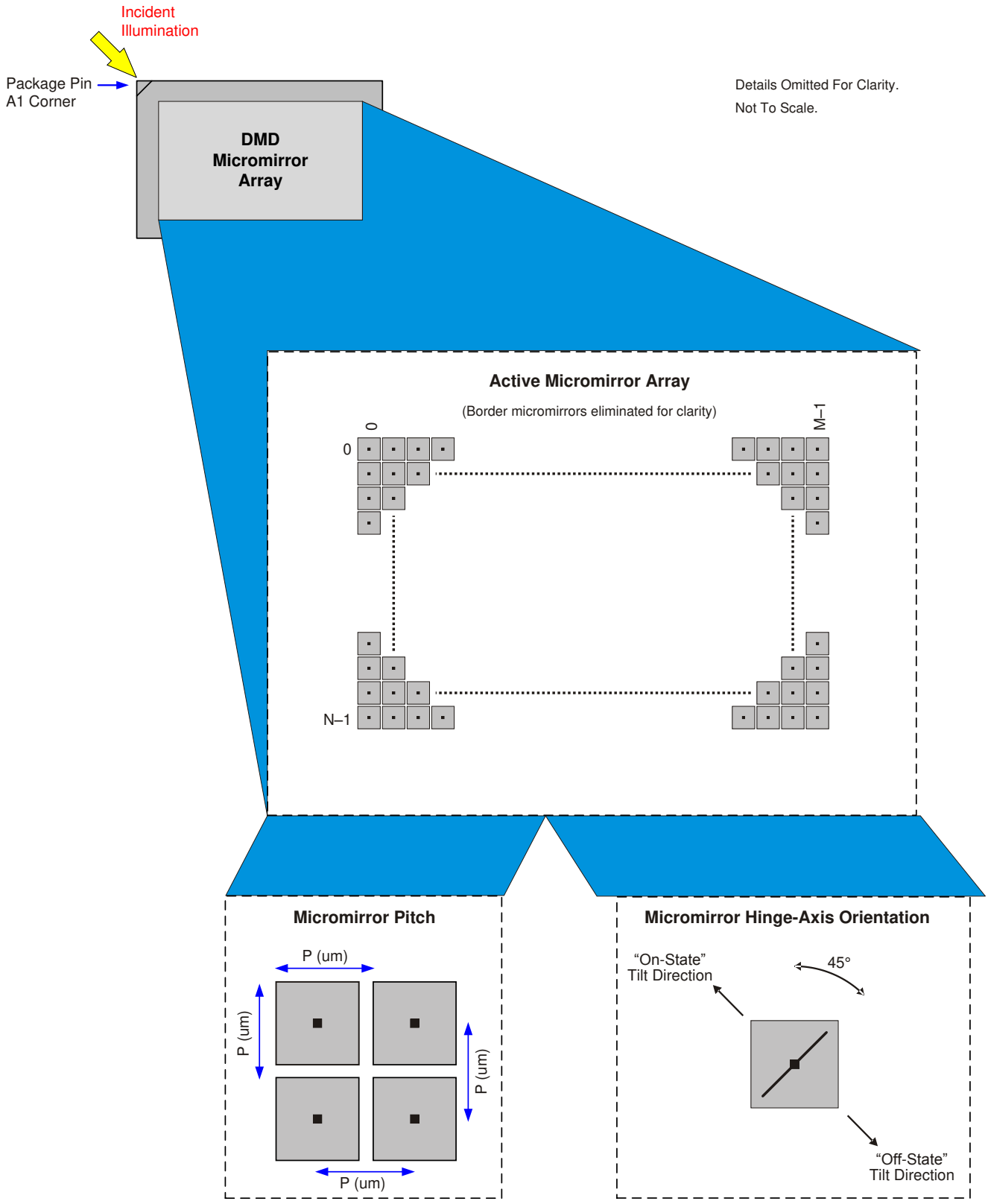
Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents, after the mirror clocking pulse is applied. The angular position (–α and +α) of the individual micromirrors changes synchronously with a micromirror clocking pulse, rather than being coincident with the CMOS memory cell data update.

Writing logic 1 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a +α position. Writing logic 0 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a – α position.

Updating the angular position of the micromirror array consists of two steps. First, update the contents of the CMOS memory. Second, apply a micromirror reset (also referred as Mirror Clocking Pulse) to all or a portion of the micromirror array (depending upon the configuration of the system). Micromirror reset pulses are generated internally by the DMD, with application of the pulses being coordinated by the DLPC910 digital controller.

For more information, refer to the TI application report DLPA008, *DMD101: Introduction to Digital Micromirror Device (DMD) Technology*.

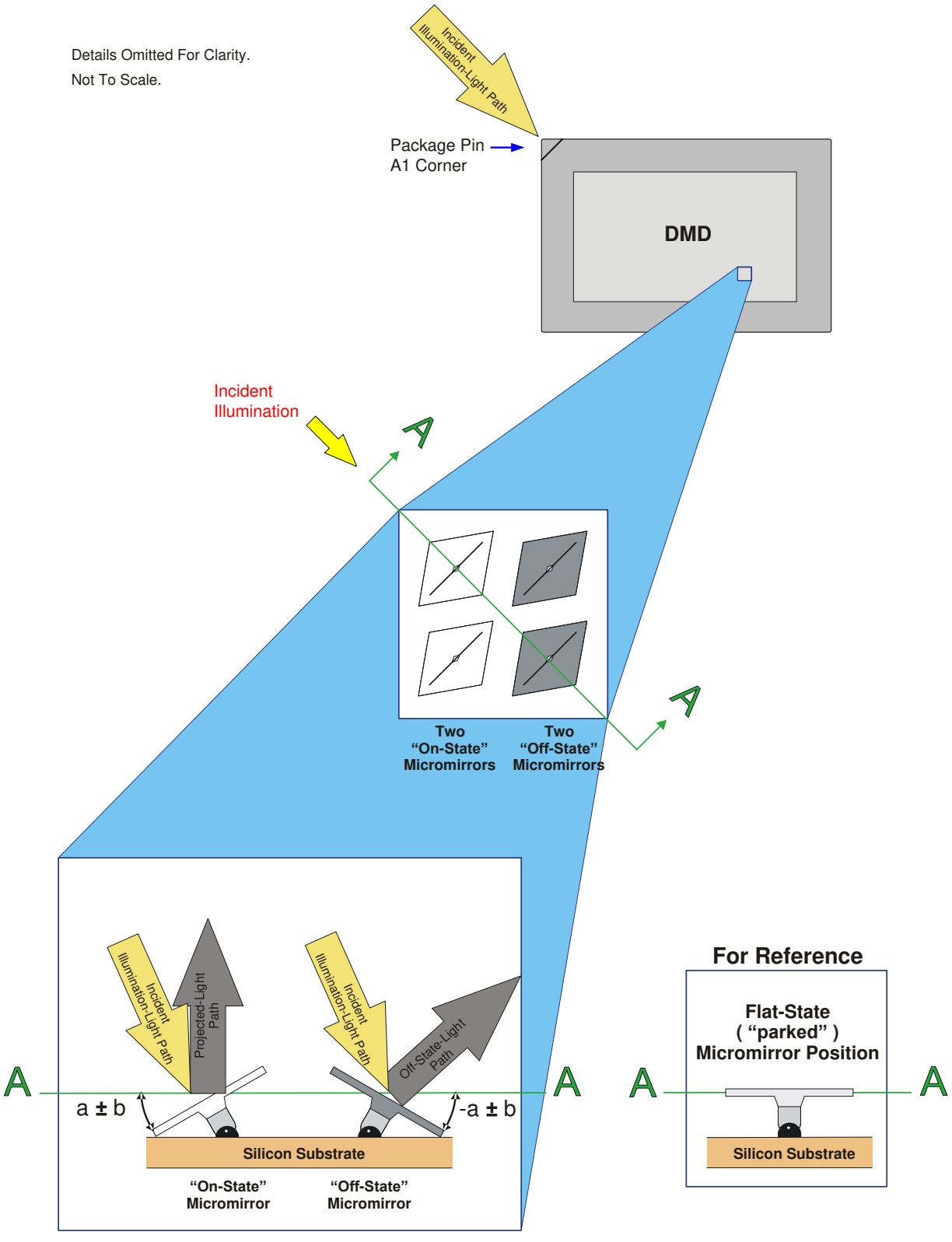
Feature Description (continued)



Refer to *Micromirror Array Physical Characteristics*, Figure 9, and Figure 10.

Figure 13. Micromirror Array, Pitch, Hinge Axis Orientation

Feature Description (continued)



Micromirror States: On, Off, Flat

Figure 14. Micromirror States: On, Off, Flat

8.4 Device Functional Modes

The DLP9000XUV DMD is controlled by one DLPC910 digital controller. The digital controller offers high speed streaming mode where 1-bit binary patterns are accepted at the LVDS interface input, and then streamed to the DMD. To ensure reliable operation, the DLP9000XUV DMD must always be used with the DLPC910 controller. For more information, refer to the DLPC910 data sheet listed under *Related Documentation*.

8.5 Window Characteristics and Optics

NOTE

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

8.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

8.5.2 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

8.5.3 Pupil Match

TI's optical specifications assume that the exit pupil of the illumination optics is nominally centered within 2° (two degrees) of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

8.5.4 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

8.6 Micromirror Array Temperature Calculation

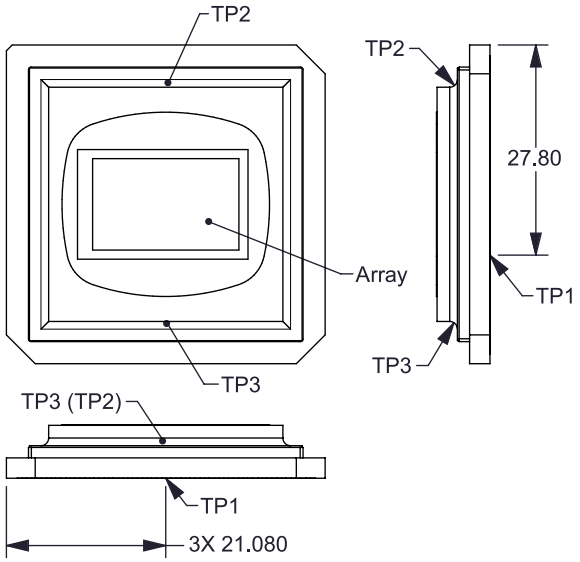


Figure 15. DMD Thermal Test Points

Micromirror array temperature can be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between micromirror array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION})$$

where:

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of DMD package from array to ceramic TP1 (°C/W)
- Q_{ARRAY} = Total DMD power (electrical and absorbed) on the array (Watts)
- $Q_{ELECTRICAL}$ = Nominal electrical power (Watts)
- $Q_{INCIDENT}$ = Incident Illumination optical power (W)
- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity x $Q_{INCIDENT}$) (W)
- DMD average thermal absorptivity = 0.39

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and pattern rates of the DMD within the intended application. For the example array temperature calculation shown below, the maximum value of 11.2 W is used for the electrical power dissipation. Since the electrical power dissipation of the DMD is application dependent, customers will want to test and use their own application dependent power values in their array temperature calculation. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for each DMD chip in a system. The absorption factor of 0.39 assumes the array is fully illuminated with an illumination distribution of 90% on the active array and 10% overfill on the array border. It is strongly recommended to minimize illumination overfill as much as possible which will, in turn, maximize the active array illumination, increase overall system efficiency, and reduce DMD thermal heating.

The following is a sample Calculation for each DMD in a system with a measured illumination power density:

- $T_{Ceramic}$ = 15°C (measured)
- $ILL_{DENSITY}$ = 15 Watts per cm^2 (optical power on DMD per unit area) (measured)
- Overfill = 10% (optical design)
- $Q_{ELECTRICAL}$ = 11.2 Watts
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = 0.5 °C/W

Micromirror Array Temperature Calculation (continued)

- Area of array = (1.9354 cm x 1.2096 cm) = 2.34 cm^2
- ILL_{AREA} = 2.34 cm^2 / (90%) = 2.6 cm^2
- $Q_{INCIDENT}$ =15 W/cm^2 x 2.6 cm^2 = 39.0 W
- Q_{ARRAY} = 11.2 W + (0.39 x 39.0 W) = 26.4 W
- **T_{ARRAY}** =15°C + (26.4 W x 0.5 °C) **= 28.2 °C**

8.7 Micromirror Landed-On/Landed-Off Duty Cycle

8.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On–state versus the amount of time the same micromirror is landed in the Off–state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On-state 100% of the time (and in the Off-state 0% of the time); whereas 0/100 would indicate that the pixel is in the Off-state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

8.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

Individual DMD mirror duty cycles vary by application as well as the mirror location on the DMD within any specific application. DMD mirror useful life are maximized when every individual mirror within a DMD approaches 50/50 (or 1/1) duty cycle. For the DLPC910 and DLP9000XUV chipset, it is recommended the controlling applications processor provide a 50/50 pattern sequence to the DLPC910 for display on the DLP9000XUV DMD as often as possible. The pattern provides a 50/50 duty cycle across the entire DMD mirror array, where the mirrors are continuously flipped between the on and off states.

8.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life.

8.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in Table 2.

Micromirror Landed-On/Landed-Off Duty Cycle (continued)

Table 2. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DLP9000XUV DMD is controlled by the DLPC910 controller, where the DLPC910 is configured by the program content in the DLPR910. This chipset offers streaming 1-bit binary patterns to the DMD at speeds greater than 61 Gigabits per second (Gbps). The patterns are streamed from a customer designed processor into the LVDS input data interface of the DLPC910 Controller.

The DLP9000XUV chipset provides solutions for many varied applications including structured light, 3D printing, video projection, and high speed lithography. The DMD is a spatial light modulator, which reflects incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data being used.

9.1.1 DMD Reflectivity Characteristics

Under long term UVA illumination, many elements of optical systems can experience degradation, including illuminators, lenses, etc. TI assumes no responsibility for DMD reflectivity performance which affects end-equipment performance over time. Achieving the desired end-equipment reflectivity performance involves making trade-offs between numerous component and system design parameters and validating the performance for the end equipment prior to production. DMD reflectivity includes both micromirror surface reflectivity and DMD window transmission. DMD reflectivity was characterized over time using 365 nm, 385 nm, and 405 nm high power LEDs directly illuminating the DMD at various DMD array temperatures. Nominal DMD Reflectivity characteristics over Total UV Exposure Times at maximum power densities for given wavelengths are represented in the following figures. (Contact your local Texas Instruments representative for additional information about power density measurements.)

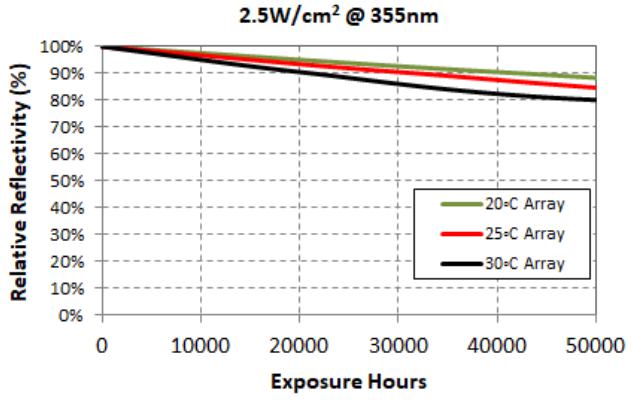


Figure 16. Relative Reflectivity @ 355nm

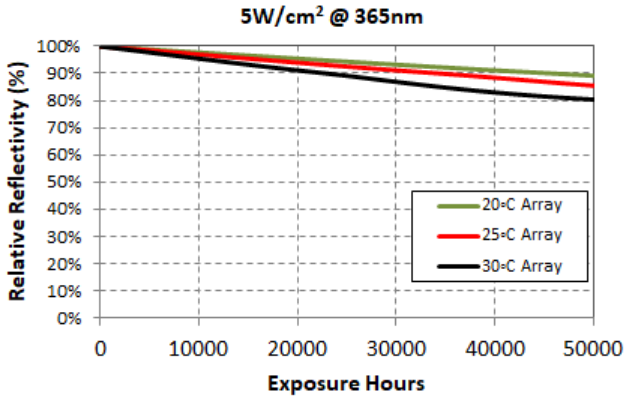


Figure 17. Relative Reflectivity @ 365nm

Application Information (continued)

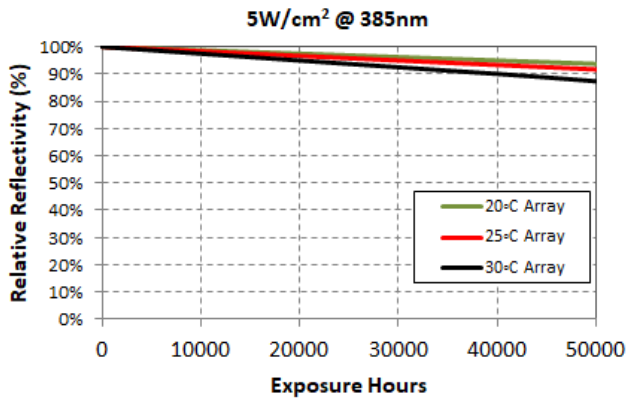


Figure 18. Relative Reflectivity @ 385nm

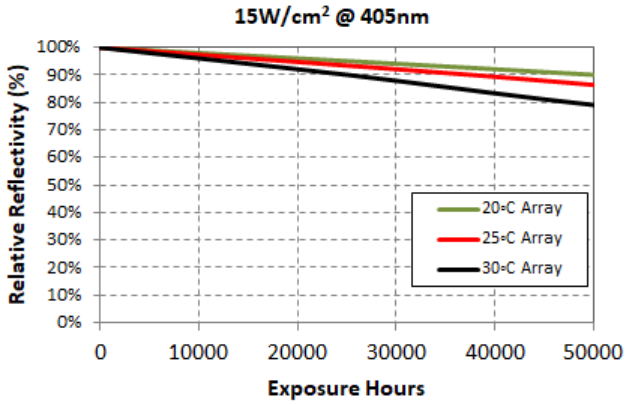


Figure 19. Relative Reflectivity @ 405nm

9.1.1.1 Design Considerations Influencing DMD Reflectivity

Optimal, long-term performance of the digital micromirror device (DMD) can be affected by various customer selected application and design parameters. The following list identifies some of these parameters and includes high level design recommendations that may help extend relative DMD reflectivity from time zero:

- Illumination spectrum – use longer wavelengths for the application whenever possible while filtering or preventing shorter wavelengths from striking the DMD
- Illumination power density – use the lowest illumination power density possible for the application
- DMD temperature – always operate the DMD within its array temperature specification and toward the lower end when at all possible
- Cumulative incident illumination – minimize the total hours of UV illumination exposure. In the application, when the DMD is not actively required to steer UV light, disable the solid-state illumination or shutter the illumination.
- Micromirror landed duty cycles – during periods of system inactivity, turn off the illuminators and rapidly apply repeating 50/50 duty cycle patterns to the DMD.

9.2 Typical Applications

High-end lithography is benefitting from the conversion from mask-based imaging to digital mask-less imaging. Instead of stopping the lithography process to change out expensive masks, mask-less lithography offers a continuous run of printing by changing the imaged patterns digitally without stopping the imaging process. The programmable nature of the DMD supports real-time correction of optical and imaged surface distortions. Figure 20 shows a system where a DLPC910 digital controller is coupled with the DLP9000XUV DMD. These components enable a high speed digital imaging system that takes in digital images at 2560 × 1600 in resolution at speeds of more than 61 Gbps and projects them at pattern rates nearing 15 kHz. For more information, refer to the DLPC910 digital controller data sheet listed under *Related Documentation*.

9.2.1 Design Requirements

Detailed design requirements are located in the DLPC910 digital controller data sheets. Refer to the data sheets listed under *Related Documentation*.

9.2.2 Detailed Design Procedure

TIDA-00570 is a TI reference design which provides detailed information to assist customers in implementing a DLPC910 based system using the DLP9000X DMD. The reference design is also applicable to using the DLPC910 with the DLP9000XUV DMD instead of the DLP9000X DMD. This reference material includes reference board schematics, PCB layouts, and Bills of Materials. Layout guidelines for boards utilizing these controllers and DMDs can also be found in the DLPC910 Controller and DLP9000X(UV) data sheets. For more information, please refer to the individual data sheets listed under *Related Documentation*.

Typical Applications (continued)

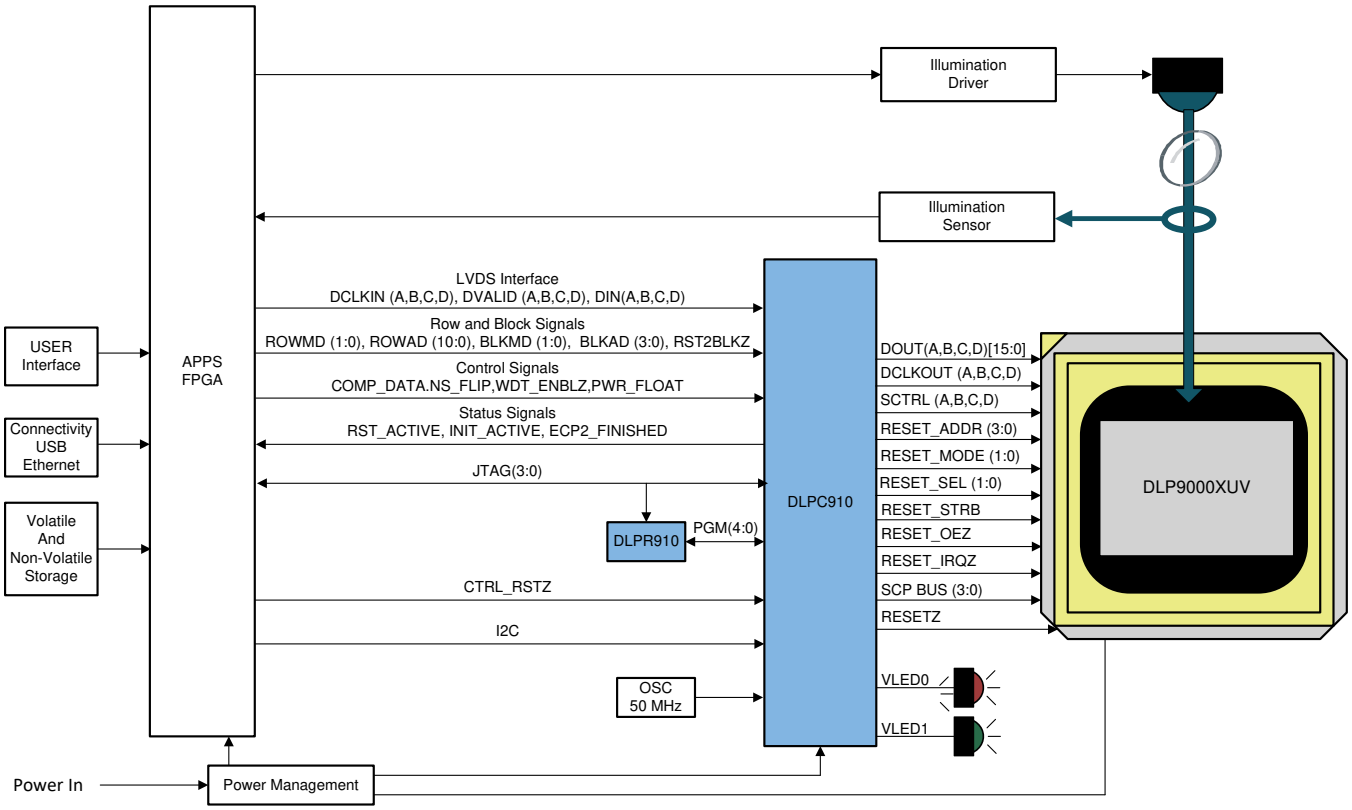


Figure 20. DLP9000XUV DMD - Typical Application Schematic

10 Power Supply Requirements

10.1 DMD Power Supply Requirements

The following power supplies are all required to operate the DMD: V_{CC}, V_{CCI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. V_{SS} must also be connected. DMD power-up and power-down sequencing is strictly controlled by the DLPC910 Controllers within their associated reference designs.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. V_{CC}, V_{CCI}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supplies have to be coordinated during power-up and power-down operations. V_{SS} must also be connected. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. Refer to Figure 21.

10.2 DMD Power Supply Power-Up Procedure

- During power-up, V_{CC} and V_{CCI} must always start and settle before V_{OFFSET}, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in *Recommended Operating Conditions*. *During power-up, V_{BIAS} does not have to start after V_{OFFSET}.*
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{OFFSET} and V_{BIAS}.
- Power supply slew rates requirements during power-up are flexible, provided that the transient voltage levels follow the requirements listed in *Absolute Maximum Ratings*, in *Recommended Operating Conditions*, and in Figure 21.
- During power-up, LVCMOS input pins shall not be driven high until after V_{CC} and V_{CCI} have settled at operating voltages listed in *Recommended Operating Conditions*.

10.3 DMD Mirror Park Sequence (Power_Float) Requirements

For correct power down operation of the DLP9000XUV DMD, the following power down procedure must be executed.

Prior to an anticipated power removal, assert the PWR_FLOAT signal to the DLPC910 for a minimum of 500 μs to allow the DLPC910 to complete the power down procedure. This procedure will assure the DMD mirrors are in the unbiased parked state. Following this procedure, the power can be safely removed.

In the event of an unanticipated power loss, the power management system must detect the input power loss, immediately assert PWR_FLOAT to the DLPC910, and maintain all operating power levels of the DLPC910 and the DLP9000XUV DMD for a minimum of 500 μs to allow the DLPC910 to complete the power down procedure. Refer to the DLPC910 datasheet for more details on power down requirements.

To restart the DLPC910 and DLP9000XUV after assertion of PWR_FLOAT, the DLPC910 must be reset by setting CTRL_RSTZ low (logic 0) for 50 ms and then back to high (logic 1), or the power to the DLPC910 must be cycled.

10.4 DMD Power Supply Power-Down Procedure

- During power-down, V_{CC} and V_{CCI} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within the specified limit of ground. Refer to Table 3.
- During power-down, it is a strict requirement that the delta between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in *Recommended Operating Conditions*. During power-down, it is not mandatory to stop driving V_{BIAS} prior to V_{OFFSET}.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{OFFSET} and V_{BIAS}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed in *Absolute Maximum Ratings*, in *Recommended Operating Conditions*, and in Figure 21.
- During power-down, LVCMOS input pins must be less than specified in *Recommended Operating Conditions*.

DMD Power Supply Power-Down Procedure (continued)

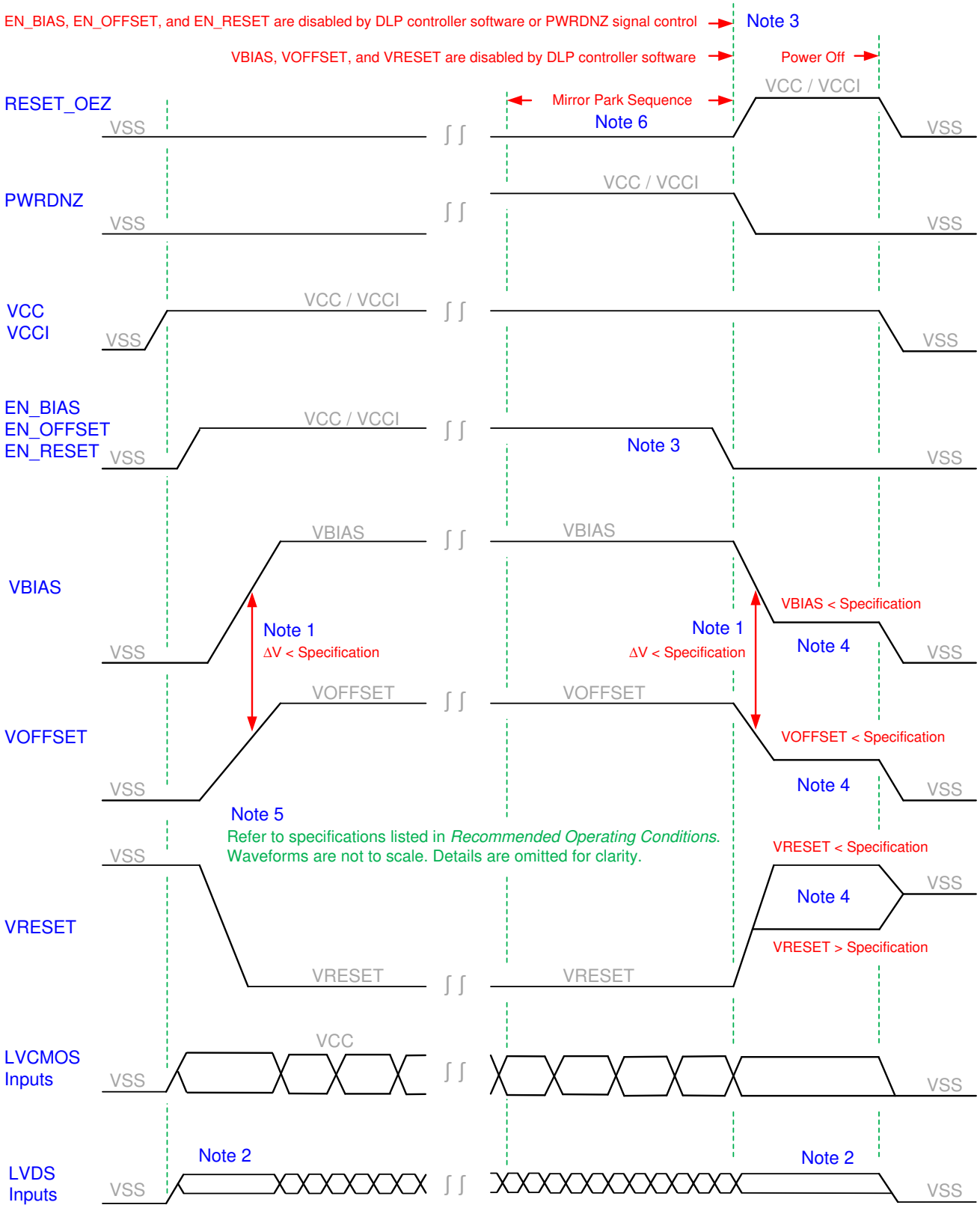


Figure 21. DMD Power Supply Sequencing Requirements

DMD Power Supply Power-Down Procedure (continued)

1. To prevent excess current, the supply voltage delta $|V_{BIAS} - V_{OFFSET}|$ must be less than specified in *Recommended Operating Conditions*. *OEMs may find that the most reliable way to ensure this is to power V_{OFFSET} prior to V_{BIAS} during power-up and to remove V_{BIAS} prior to V_{OFFSET} during power-down.*
2. During power-up, the LVDS signals are less than the input differential voltage (V_{ID}) maximum specified in *Recommended Operating Conditions*. During power-down, LVDS signals are less than the high level input voltage (V_{IH}) maximum specified in *Recommended Operating Conditions*.
3. When system power is interrupted, the DLPC910 controllers initiate a hardware power-down that activates PWRDNZ and disables V_{BIAS}, V_{RESET} and V_{OFFSET} after the micromirror park sequence. Software power-down disables V_{BIAS}, V_{RESET}, and V_{OFFSET} after the micromirror park sequence through software control. For either case, enable signals EN_BIAS, EN_OFFSET, and EN_RESET are used to disable V_{BIAS}, V_{OFFSET}, and V_{RESET}, respectively.
4. Refer to Table 3.
5. Figure not to scale. Details have been omitted for clarity. Refer to *Recommended Operating Conditions*.
6. Refer to *DMD Mirror Park Sequence (Power_Float) Requirements* for details on powering down the DMD.

Table 3. DMD Power-Down Sequence Requirements

PARAMETER		MIN	MAX	UNIT
V_{BIAS}	Supply voltage level during power–down sequence		4.0	V
V_{OFFSET}			4.0	V
V_{RESET}		–4.0	0.5	V

11 Layout

11.1 Layout Guidelines

Each chipset provides a solution for many applications including digital lithography and 3D printing. This section provides layout guidelines for the DMD.

11.1.1 General PCB Recommendations

The PCB shall be designed to IPC2221 and IPC2222, Class 2, Type Z, at level B producibility and built to IPC6011 and IPC6012, class 2. The PCB board thickness to be 0.062 inches ±10%, using a dielectric material with a low loss-tangent, for example: Hitachi 679gs or equivalent.

Two-ounce copper planes are recommended in the PCB design in order to achieve needed thermal connectivity. Refer to the digital controller data sheets listed under *Related Documentation* regarding DMD Interface Considerations.

High-speed interface waveform quality and timing on the digital controllers (that is, the LVDS DMD interface) is dependent on the following factors:

- Total length of the interconnect system
- Spacing between traces
- Characteristic impedance
- Etch losses
- How well matched the lengths are across the interface

Thus, ensuring positive timing margin requires attention to many factors.

As an example, DMD interface system timing margin can be calculated as follows:

- Setup Margin = (controller output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation)
- Hold-time Margin = (controller output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

The PCB SI degradation is the signal integrity degradation due to PCB effects which includes simultaneously switching output (SSO) noise, crosstalk, and inter-symbol-interference (ISI) noise.

DLPC910 I/O timing parameters can be found in their respective data sheets. Similarly, PCB routing mismatch can be easily budgeted and met via controlled PCB routing. However, PCB SI degradation is not as easy to determine.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines provide a reference of an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Deviation from these recommendations should be confirmed with PCB signal integrity analysis or lab measurements.

11.1.2 Power Planes

Signal routing is NOT allowed on the power and ground planes. All device pin and via connections to this plane shall use a thermal relief with a minimum of four spokes. The power plane shall clear the edge of the PCB by 0.2".

Prior to routing, vias connecting all digital ground layers (GND) should be placed around the edge of the rigid PWB regions 0.025” from the board edges with a 0.100” spacing. It is also desirable to have all internal digital ground (GND) planes connected together in as many places as possible. If possible, all internal ground planes should be connected together with a minimum distance between connections of 0.5". Extra vias are not required if there are sufficient ground vias due to normal ground connections of devices. NOTE: All signal routing and signal vias should be inside the perimeter ring of ground vias.

Power and Ground pins of each component shall be connected to the power and ground planes with one via for each pin. Trace lengths for component power and ground pins should be minimized (ideally, less than 0.100”). Unused or spare device pins that are connected to power or ground may be connected together with a single via to power or ground. Ground plane slots are NOT allowed.

Route V_{OFFSET}, V_{BIAS}, and V_{RESET} as a wide trace >20 mils (wider if space allows) with 20 mils spacing.

Layout Guidelines (continued)

11.1.3 LVDS Signals

The LVDS signals shall be first. Each pair of differential signals must be routed together at a constant separation such that constant differential impedance (as in section *Board Stack and Impedance Requirements*) is maintained throughout the length. Avoid sharp turns and layer switching while keeping lengths to a minimum. The distance from one pair of differential signals to another shall be at least 2 times the distance within the pair.

11.1.4 Critical Signals

The critical signals on the board must be hand routed in the order specified below. In case of length matching requirements, the longer signals should be routed in a serpentine fashion, keeping the number of turns to a minimum and the turn angles no sharper than 45 degrees. Avoid routing long trace all around the PCB.

Table 4. Timing Critical Signals

GROUP	SIGNAL	CONSTRAINTS	ROUTING LAYERS
1	D_AP(0:15), D_AN(0:15), DCLK_AP, DCLK_AN, SCTRL_AN, SCTRL_AP, D_BP(0:15), D_BN(0:15), DCLK_BP, DCLK_BN, SCTRL_BN, SCTRL_BP, D_CP(0:15), D_CN(0:15), DCLK_CP, DCLK_CN, SCTRL_CN, SCTRL_CP, D_DP(0:15), D_DN(0:15), DCLK_DP, DCLK_DN, SCTRL_DN, SCTRL_DP.	Refer to Table 5 and Table 6	Internal signal layers. Avoid layer switching when routing these signals.
2	RESET_ADDR_(0:3), RESET_MODE_(0:1), RESET_OEZ, RESET_SEL_(0:1) RESET_STROBE, RESET_IRQZ.		Internal signal layers. Top and bottom as required.
3	SCP_CLK, SCP_DO, SCP_DI, SCP_DMD_CSZ.		Any
4	Others	No matching/length requirement	Any

11.1.5 Flex Connector Plating

Plate all the of pad area on the top layer of the flex connection with a minimum of 35 and of maximum 50 micro-inches of electrolytic hard gold over a minimum of 150 micro-inches of electrolytic nickel.

11.1.6 Device Placement

Unless otherwise specified, all major components should be placed on the top layer. Small components such as ceramic, non-polarized capacitors, resistors, and resistor networks can be placed on the bottom layer. All high frequency de-coupling capacitors for the ICs shall be placed near the parts. Distribute the capacitors evenly around the IC and place them as close to the device's power pins as possible (preferably with no vias). In the case where an IC has multiple de-coupling capacitors with different values, alternate the values of those that are side by side as much as possible and place the smaller value capacitor closer to the device.

11.1.7 Device Orientation

It is desirable to have all polarized capacitors oriented with their positive terminals in the same direction. If polarized capacitors are oriented both horizontally and vertically, then all horizontal capacitors should be oriented with the "+" terminal facing the same direction and likewise for the vertically oriented ones.

11.2 Layout Example

11.2.1 Board Stack and Impedance Requirements

Refer to Figure 22 regarding guidance on the parameters.

PCB design:

Configuration:	Asymmetric dual stripline
Etch thickness (T):	1.0-oz copper (1.2 mil)
Flex etch thickness (T):	0.5-oz copper (0.6 mil)
Single-ended signal impedance:	50 Ω (±10%)
Differential signal impedance:	100 Ω (±10%)

PCB stack-up:

Reference plane 1 is assumed to be a ground plane for the proper return path.

Reference plane 2 is assumed to be the I/O power plane or ground.

Dielectric material with a low loss-tangent, for example: Hitachi 679gs or equivalent.	(Er): 3.8 (nominal)
Signal trace distance to reference plane 1 (H1):	5.0 mil (nominal)
Signal trace distance to reference plane 2 (H2):	34.2 mil (nominal)

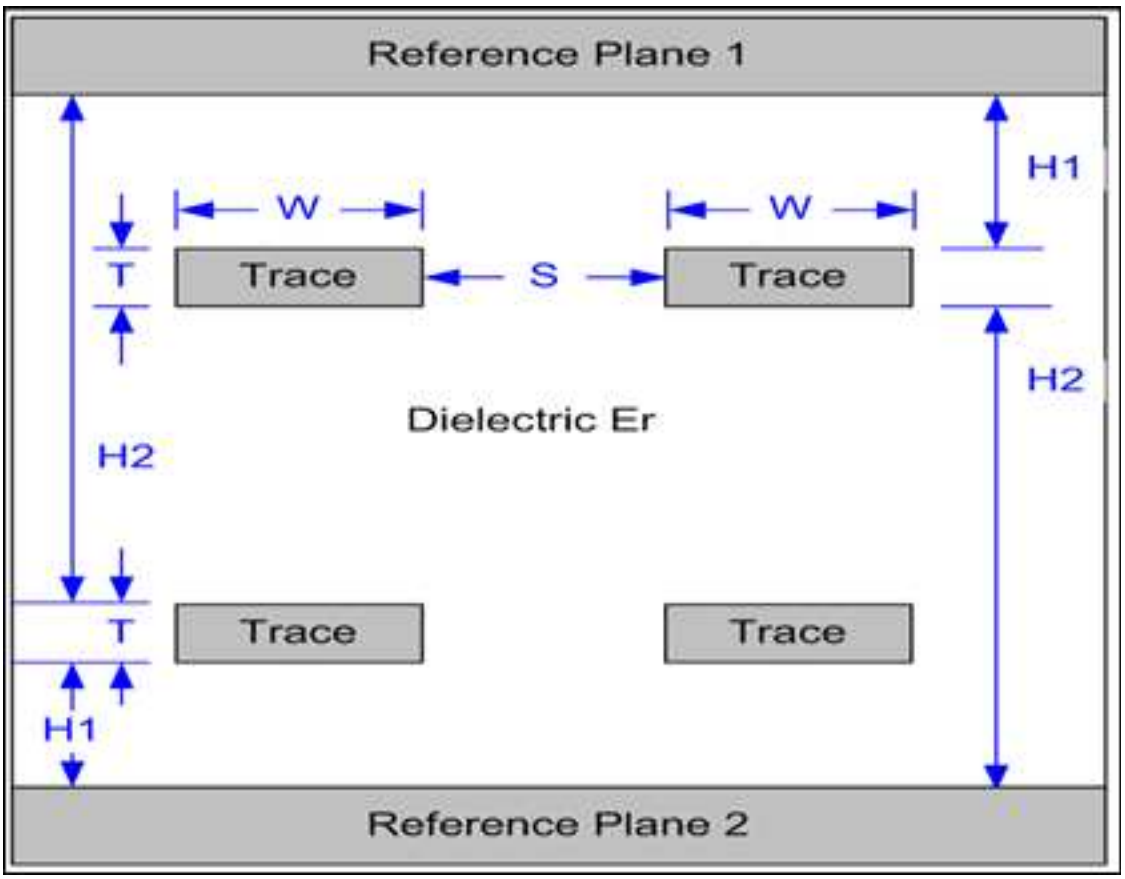


Figure 22. PCB Stack Geometries

Layout Example (continued)

Table 5. General PCB Routing (Applies to All Corresponding PCB Signals)

PARAMETER	APPLICATION	SINGLE-ENDED SIGNALS	DIFFERENTIAL PAIRS	UNIT
Line width (W)	Escape routing in ball field	4 .4 (0.1)	4 .3 (0.1)	mil (mm)
	PCB etch data or control	7 (0.18)	4.25 (0.11)	mil (mm)
	PCB etch clocks	7 (0.18)	4.25 (0.11)	mil (mm)
Differential signal pair spacing (S)	PCB etch data or control	N/A	5.75 (1) –0.15	mil (mm)
	PCB etch clocks	N/A	5.75 (1) –0.15	mil (mm)
Minimum differential pair-to-pair spacing (S)	PCB etch data or control	N/A	20 (0.51)	mil (mm)
	PCB etch clocks	N/A	20 (0.51)	mil (mm)
	Escape routing in ball field	4 (0.1)	4 (0.1)	mil (mm)
Minimum line spacing to other signals (S)	PCB etch data or control	10 (0.25)	20 (0.51)	mil (mm)
	PCB etch clocks	20 (0.51)	20 (0.51)	mil (mm)
Maximum differential pair P-to-N length mismatch	Total data	N/A	10 –0.25	mil (mm)
	Total data	N/A	10 –0.25	mil (mm)

(1) Spacing may vary to maintain differential impedance requirements.

Table 6. DMD Interface Specific Routing

SIGNAL GROUP LENGTH MATCHING				
INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD (LVDS)	SCTRL_AN / SCTRL_AP D_AP(15:0)/ D_AN(15:0)	DCLK_AP/ DCLK_AN	± 50 (± 1.3)	mil (mm)
DMD (LVDS)	SCTRL_BN/ SCTRL_BP D_BP(15:0)/ D_BN(15:0)	DCLK_BP/ DCLK_BN	± 50 (± 1.3)	mil (mm)
DMD (LVDS)	SCTRL_CN/ SCTRL_CP D_CP(15:0)/ D_CN(15:0)	DCLK_CP/ DCLK_CN	± 50 (± 1.3)	mil (mm)
DMD (LVDS)	SCTRL_DN/ SCTRL_DP D_DP(15:0)/ D_DN(15:0)	DCLK_DP/ DCLK_DN	± 50 (± 1.3)	mil (mm)

Number of layer changes:

- Single-ended signals: Minimize.
- Differential signals: Individual differential pairs can be routed on different layers but the signals of a given pair should not change layers.

Table 7. DMD Signal Routing Length (1)

BUS	MIN	MAX	UNIT
DMD (LVDS)	50	375	mm

(1) Max signal routing length includes escape routing.

Stubs: Stubs should be avoided.

Termination Requirements (DMD interface): None – The DMD receiver is differentially terminated to 100 Ω internally.

Connector (DMD-LVDS interface bus only):

High-speed connectors that meet the following requirements should be used:

- Differential crosstalk: <5%
- Differential impedance: 75 to 125 Ω

Routing requirements for right-angle connectors: When using right-angle connectors, P-N pairs should be routed in the same row to minimize delay mismatch. When using right-angle connectors, propagation delay difference for each row should be accounted for on associated PCB etch lengths. Voltage or low frequency signals should be routed on the outer layers. Signal trace corners shall be no sharper than 45 degrees. Adjacent signal layers shall have the predominant traces routed orthogonal to each other.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

Figure 23 provides a legend for reading the complete device name for any DLP device.

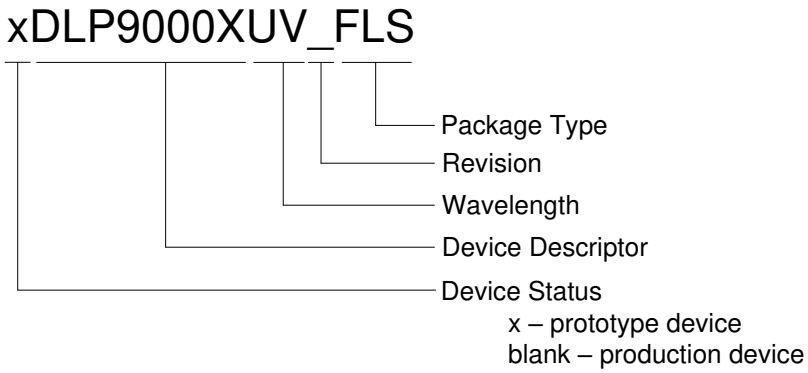


Figure 23. Device Nomenclature

12.1.2 Device Markings

The device marking will include both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 24. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, Part 1 of Serial Number, and Part 2 of Serial Number. The first character of the DMD Serial Number (part 1) is the manufacturing year. The second character of the DMD Serial Number (part 1) is the manufacturing month.

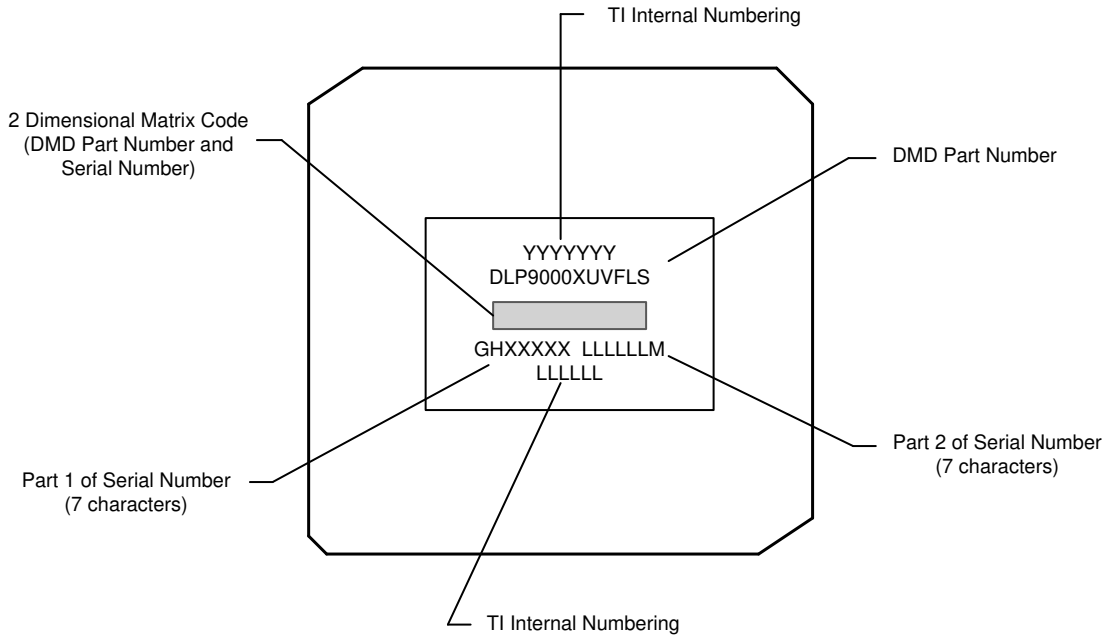


Figure 24. DMD Markings

12.2 Documentation Support

12.2.1 Related Documentation

The following documents contain additional information related to the use of the DLP9000XUV:

- DLPC910 Digital Controller Data Sheet (DLPS064)
- DLPR910 Configuration PROM Data Sheet (DLPS065)
- DLP9000 DLP9500 Type A Mounting Concept (DLPR014)

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
DLP is a registered trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Thermal Characteristics

Achieving optimal DMD performance requires proper management of the maximum DMD case temperature, the maximum temperature of any individual micromirror in the active array and the temperature gradient between any two points on or within the package.

Refer to *Absolute Maximum Ratings* and *Recommended Operating Conditions* regarding applicable temperature limits.

13.2 Package Thermal Resistance

The DMD is designed to conduct the absorbed and dissipated heat back to the series FLS package where it can be removed by an appropriate thermal management system. The thermal management system must be capable of maintaining the package within the specified operational temperatures at the thermal test point locations (refer to Figure 15 or *Micromirror Array Temperature Calculation*). The total heat load on the DMD is typically driven by the incident light absorbed by the active area; although other contributions can include light energy absorbed by the window aperture, electrical power dissipation of the array, and parasitic heating. For the thermal resistance, refer to *Thermal Information*.

13.3 Case Temperature

The temperature of the DMD case can be measured directly. For consistency, a thermal test point location is defined as shown in Figure 15 and *Micromirror Array Temperature Calculation*.

13.4 Package Option Addendum

13.4.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4) (5)
xDLP9000XUVFLS	PREVIEW	CLGA	FLS	355	1	RoHS & Green	NI-PD-AU	N / A for Pkg Type	20°C to 30°C	See Data Sheet
DLP9000XUVFLS	PREVIEW	CLGA	FLS	355	1	RoHS & Green	NI-PD-AU	N / A for Pkg Type	20°C to 30°C	See Data Sheet

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP9000XUVFLS	Active	Production	CLGA (FLS) | 355	12 | TRAY NON-STD	Yes	NIPDAU	N/A for Pkg Type	20 to 30	
DLP9000XUVFLS.B	Active	Production	CLGA (FLS) | 355	12 | TRAY NON-STD	Yes	NIPDAU	N/A for Pkg Type	20 to 30	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

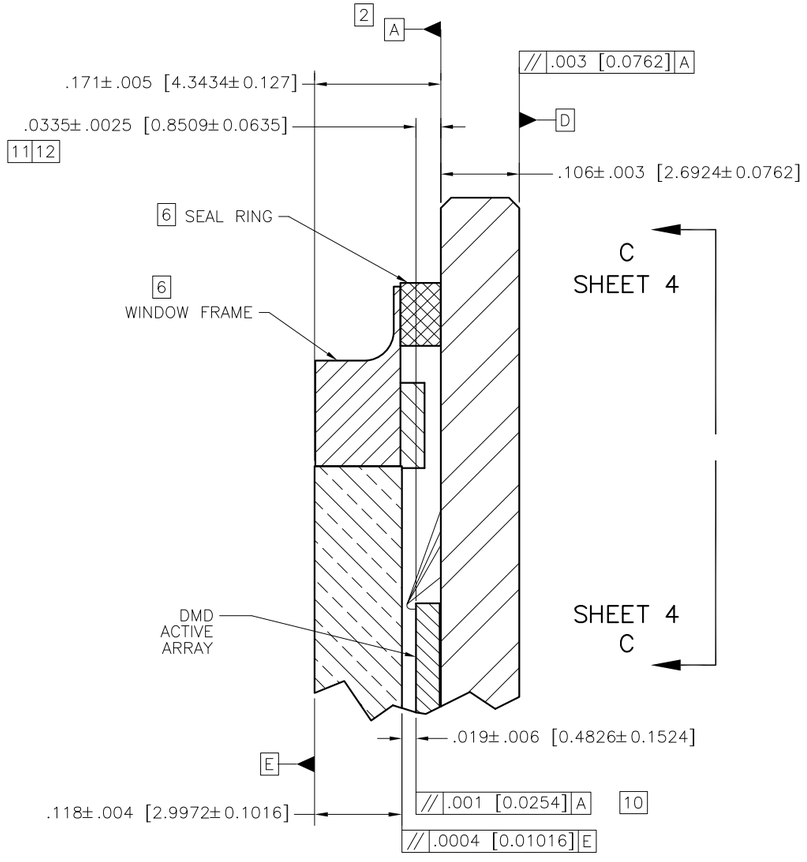
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

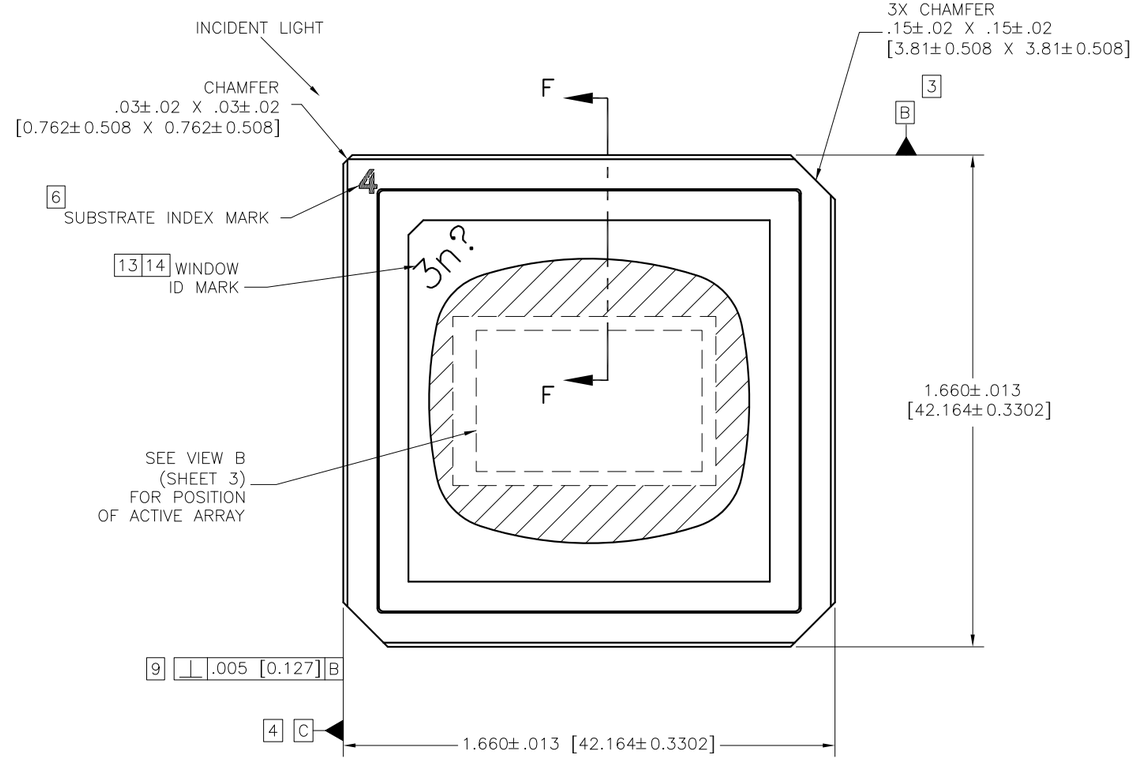
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2098262, INITIAL RELEASE	4/16/09	M. AVERY
B	ECO 2099196, CHANGE DESIGN TO OVAL WINDOW	5/22/09	M. AVERY
C	ECO 2150560, ADD NOTE 15.	05/12/15	M. AVERY
D	ECO 2179202, CHG WINDOW MARK TO INCLUDE UV	1/22/19	B. HASKETT
E	ECO 2179654, DELETE NOTE 7	2/15/19	B. HASKETT

NOTES: UNLESS OTHERWISE SPECIFIED:

1. INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M–1994.
2. DATUM A (SYSTEM INTERFACE PLANE) ESTABLISHED BY THREE DATUM AREAS SHOWN IN VIEW A (SHEET 2).
3. DATUM B ESTABLISHED BY TWO DATUM AREAS SHOWN IN VIEW A (SHEET 2).
4. DATUM C ESTABLISHED BY DATUM AREA SHOWN IN VIEW A (SHEET 2).
5. LOCALIZED BACKSIDE SURFACE FLATNESS APPLIES TO ENTIRE SURFACE.
6. SUBSTRATE INDEX MARK, BACK INDEX PAD, SYMBOLIZATION PAD, SEAL RING, AND WINDOW FRAME TO BE ELECTRICALLY CONNECTED TO VSS PLANE IN SUBSTRATE.
7. (DELETED)
8. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND IS THE MAXIMUM VALUE ALLOWED.
9. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE.
10. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
11. DIE HEIGHT TOLERANCE APPLIES TO CENTER OF DMD ACTIVE ARRAY ONLY.
12. DMD ACTIVE ARRAY ROTATION AND LOCATION DIMENSIONS ARE RELATED TO DATUM A (PRIMARY), DATUM B (SECONDARY), AND DATUM C (TERTIARY).
13. WINDOW SHALL BE ORIENTED SUCH THAT I.D. MARK ALIGNS WITH SUBSTRATE INDEX MARK AS SHOWN.
14. n AND ? ARE WILD CARD CHARACTERS. n=4 FOR STANDARD VISIBLE WINDOWS; n=7 FOR UV-TRANSMISSIVE WINDOWS. ? CAN BE ANY LETTER.
15. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE SYMBOLIZATION PAD, AS SHOWN. SUBSTRATES WITH Ni/Pd/Au SHALL HAVE THE SAME MARKING, BUT ROTATED UPSIDE-DOWN.



SECTION F–F
SCALE 10/1



PARTS LIST

–1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES[MILLIMETERS]
- TOLERANCES: ANGLES ± 1°
  3 PLACE DECIMALS ±.005[0.127]
  2 PLACE DECIMALS ±.01[0.254]
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIM
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

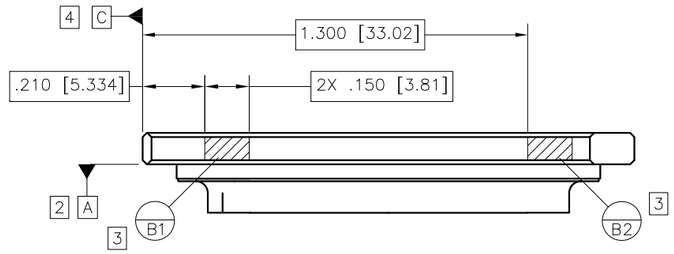
.013 THRU .125 ± .004 / ± .001	.126 THRU .250 ± .005 / ± .001	.251 THRU .500 ± .006 / ± .001
.501 THRU .750 ± .008 / ± .001	.751 THRU 1.000 ± .010 / ± .001	1.001 THRU 2.000 ± .012 / ± .001

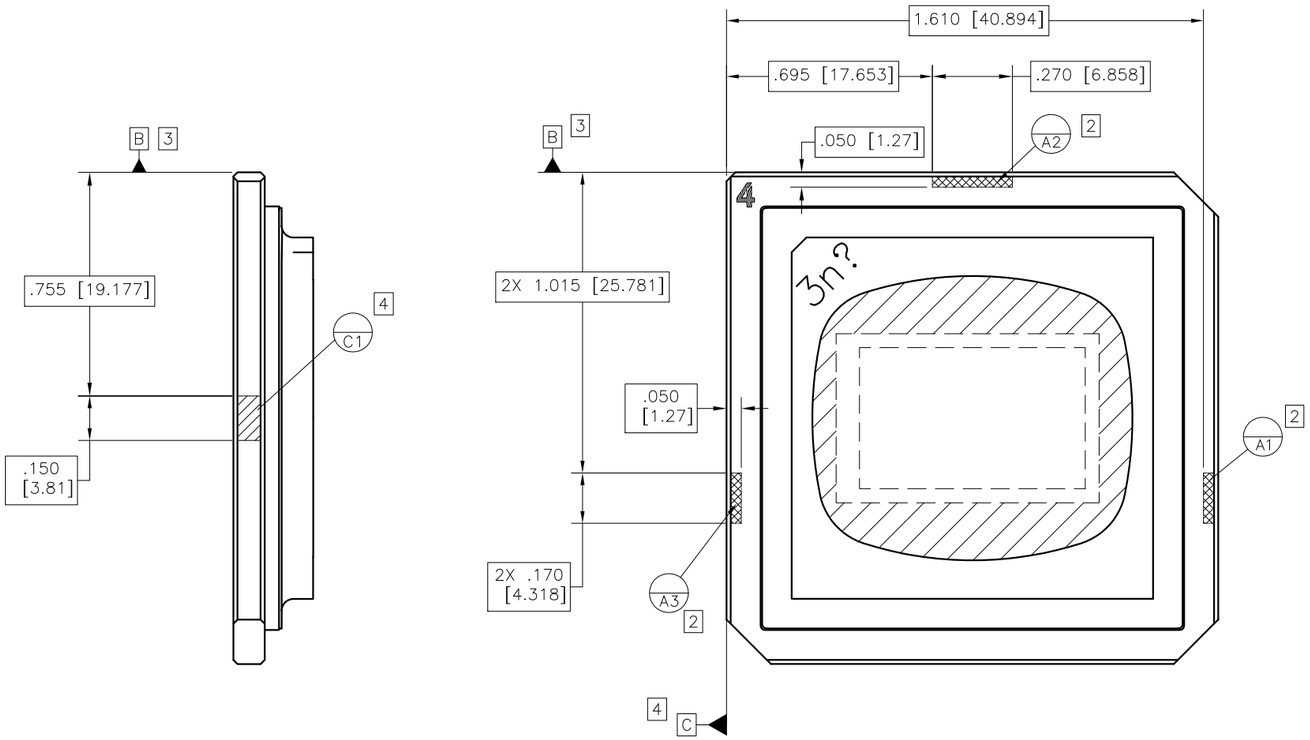
THIRD ANGLE PROJECTION

NEXT ASSY	USED ON
NONE	0314DA
APPLICATION	

DWN M. AVERY	DATE 4/02/09	TEXAS INSTRUMENTS Dallas, Texas
ENGR M. AVERY	4/02/09	ICD, MECHANICAL, DMD .9" WQXGA 2XLVDS TYPE A (FLS PACKAGE)
QA		
APVD		SIZE D · DRAWING NO 2510425 · REV E · SCALE 4/1 · SHEET 1 OF 4

ACED1g

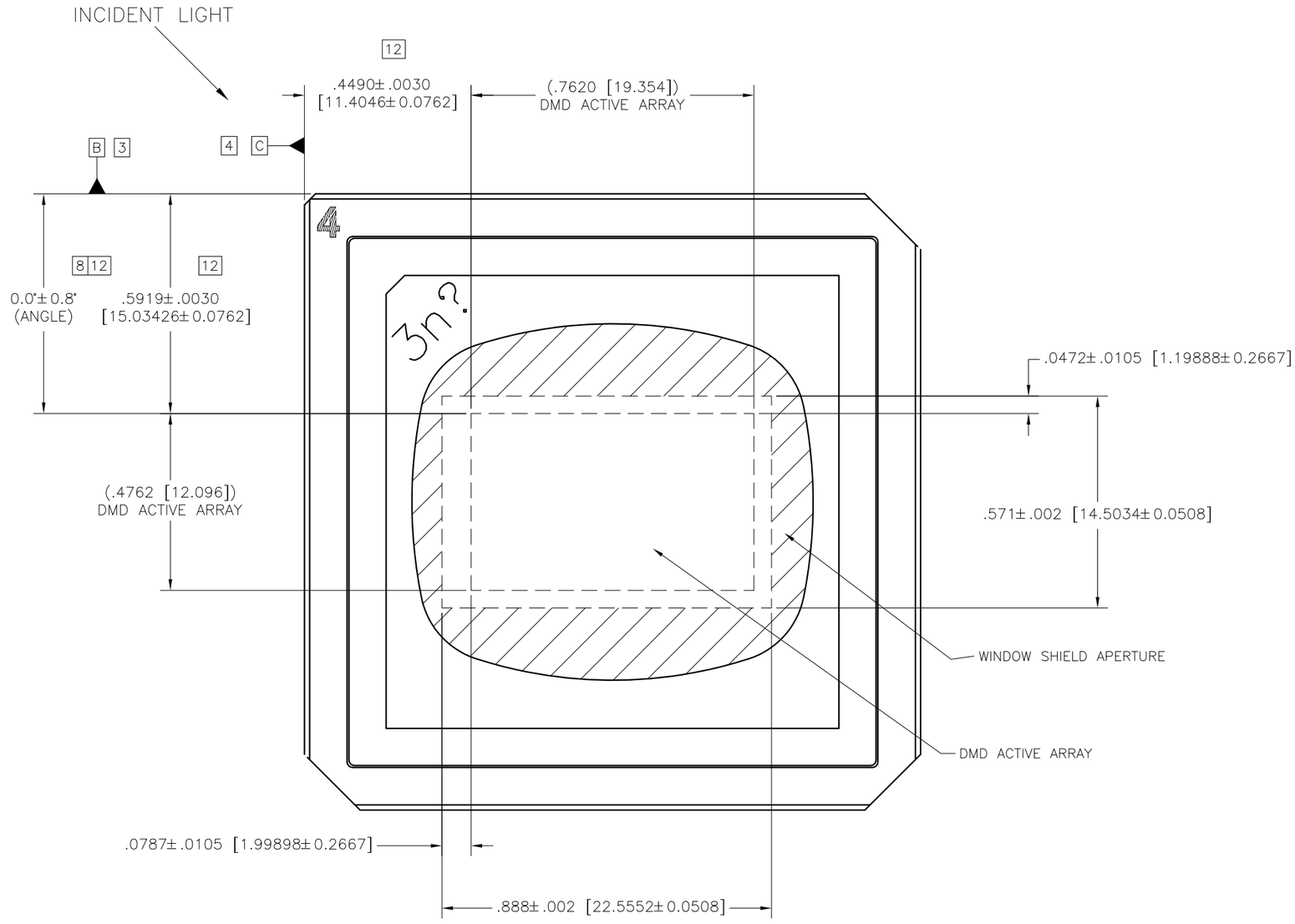




VIEW A (SHEET 1 NOTES)
DATUM A, B AND C DETAILS

Texas Instruments, Dallas, Texas	DWN DATE	SIZE D	DRAWING NO 2510425	REV E
	ISSUE DATE	SCALE 4/1	SHEET 2	

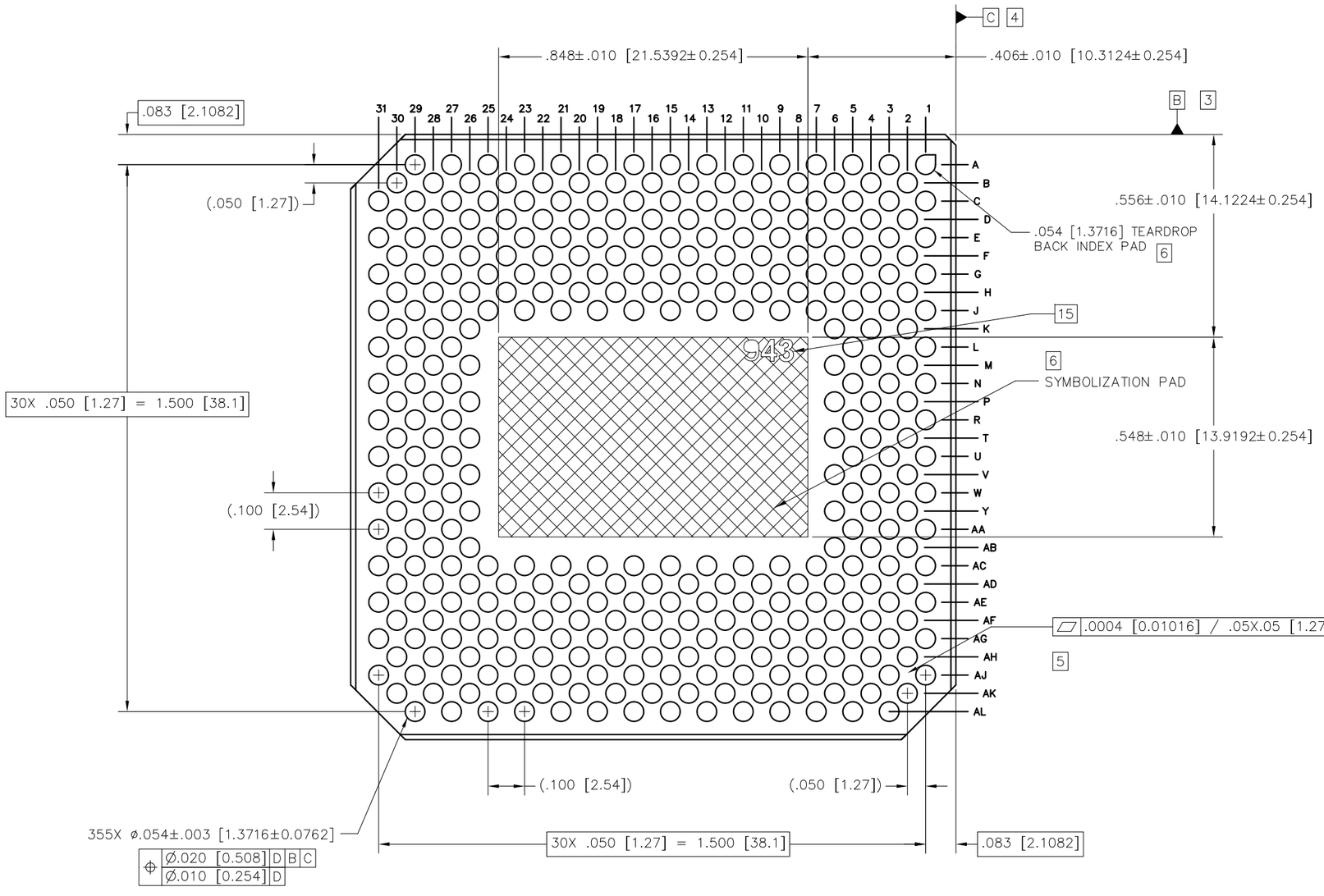
ACED2c



VIEW B (SHEET 1)
POSITION OF ACTIVE ARRAY
SCALE 6/1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE / ISSUE DATE	SIZE D	DRAWING NO 2510425	REV E
		SCALE 4/1	SHEET 3	

ACED2c



VIEW C–C (SHEET 1)
BACK PADS
SCALE 6/1

Texas Instruments, Dallas, Texas	DWN DATE / ISSUE DATE	SIZE D	DRAWING NO 2510425	REV E
		SCALE 4/1	SHEET 4	

ACED2c

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