

DLP780NE 0.78 インチ 1080P デジタル マイクロミラー デバイス

1 特長

- 対角 0.78 インチのマイクロミラー アレイ
 - フル HD (1920 × 1080) ディスプレイ解像度
 - マイクロミラー ピッチ: 9.0μm
 - マイクロミラー傾斜角: ±14.5°
 - コーナー照明
- 2 個の LVDS 入力データ バス
- フル HD~120Hz をサポート
- DLPC4430 ディスプレイ コントローラ、DLPA100 パワー マネージメント / モーター ドライバ IC によってサポートされた LED、レーザー 蛍光、RGB レーザー

2 アプリケーション

- レーザー TV
- スマート・プロジェクタ
- 企業向けプロジェクタ
- デジタル・サイネージ

3 概要

DLP780NE デジタル マイクロミラー デバイス (DMD) は、高輝度 フル HD 固体照明ディスプレイ システムを可能にするデジタル制御型 MEMS (Micro-ElectroMechanical System) 空間光変調器 (SLM) です。テキサス・インスツルメンツの DLP® 0.78 インチ フル HD チップセットは、DMD、DLPC4430 ディスプレイ コントローラ、DLPA300 マイクロミラー ドライバ、DLPA100 パワー / モーター ドライバで構成されています。このコンパクトなチップセットは、半導体照明を使った小型の フル HD ディスプレイを実現する完全なシステムを提供します。

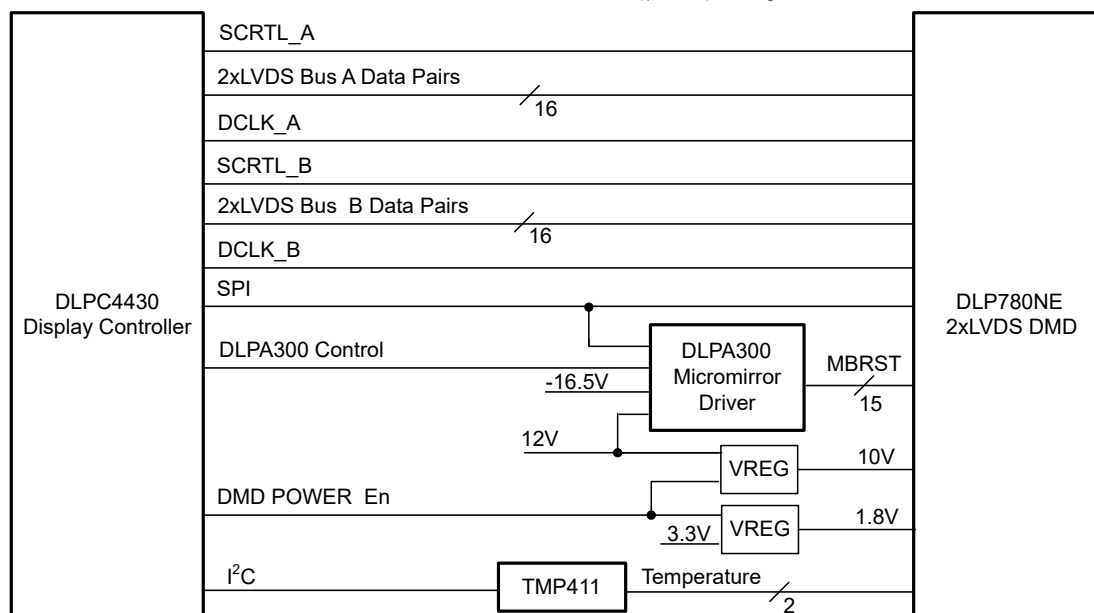
設計期間の短縮に役立つように、この DMD エコシステムは定評あるリソースで構成されており、これには、[すぐに購入可能な光モジュール](#)、[光モジュール メーカー](#)、[デザインハウス](#)などが含まれます。

DMD を使用して設計を始める方法の詳細については、「[テキサス・インスツルメンツの DLP ディスプレイテクノロジーを使用した設計の開始](#)」のページをご覧ください。

製品情報

| 部品番号 (1) | パッケージ | 本体サイズ (公称) |
|----------|-----------|-----------------|
| DLP780NE | FYU (350) | 35.0mm × 32.2mm |

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。



アプリケーション概略図



Table of Contents

| | | | |
|---|-----------|--|-----------|
| 1 特長 | 1 | 6.8 Window Aperture Illumination Overfill Calculation.... | 27 |
| 2 アプリケーション | 1 | 6.9 Micromirror Landed-On/Landed-Off Duty Cycle..... | 28 |
| 3 概要 | 1 | 7 Application and Implementation | 31 |
| 4 Pin Configuration and Functions | 3 | 7.1 Application Information..... | 31 |
| 5 Specifications | 8 | 7.2 Typical Application..... | 31 |
| 5.1 Absolute Maximum Ratings..... | 8 | 7.3 Temperature Sensor Diode..... | 34 |
| 5.2 Storage Conditions..... | 8 | 8 Power Supply Recommendations | 35 |
| 5.3 ESD Ratings..... | 8 | 8.1 DMD Power Supply Requirements..... | 35 |
| 5.4 Recommended Operating Conditions..... | 9 | 8.2 DMD Power Supply Power-Up Procedure..... | 35 |
| 5.5 Thermal Information..... | 11 | 8.3 DMD Power Supply Power-Down Procedure..... | 35 |
| 5.6 Electrical Characteristics..... | 11 | 9 Layout | 37 |
| 5.7 Timing Requirements..... | 12 | 9.1 Layout Guidelines..... | 37 |
| 5.8 System Mounting Interface Loads..... | 16 | 9.2 Layout Example..... | 37 |
| 5.9 Micromirror Array Physical Characteristics..... | 18 | 10 Device and Documentation Support | 39 |
| 5.10 Micromirror Array Optical Characteristics..... | 19 | 10.1 サード・パーティ製品に関する免責事項..... | 39 |
| 5.11 Window Characteristics..... | 20 | 10.2 Device Support..... | 39 |
| 5.12 Chipset Component Usage Specification..... | 21 | 10.3 Device Markings..... | 39 |
| 6 Detailed Description | 22 | 10.4 Documentation Support..... | 40 |
| 6.1 Overview..... | 22 | 10.5 ドキュメントの更新通知を受け取る方法..... | 40 |
| 6.2 Functional Block Diagram..... | 22 | 10.6 サポート・リソース..... | 40 |
| 6.3 Feature Description..... | 23 | 10.7 Trademarks..... | 40 |
| 6.4 Device Functional Modes..... | 23 | 10.8 静電気放電に関する注意事項..... | 40 |
| 6.5 Optical Interface and System Image Quality Considerations..... | 23 | 10.9 用語集..... | 40 |
| 6.6 Micromirror Array Temperature Calculation..... | 24 | 11 Revision History | 40 |
| 6.7 Micromirror Power Density Calculation..... | 25 | 12 Mechanical, Packaging, and Orderable Information | 41 |

4 Pin Configuration and Functions

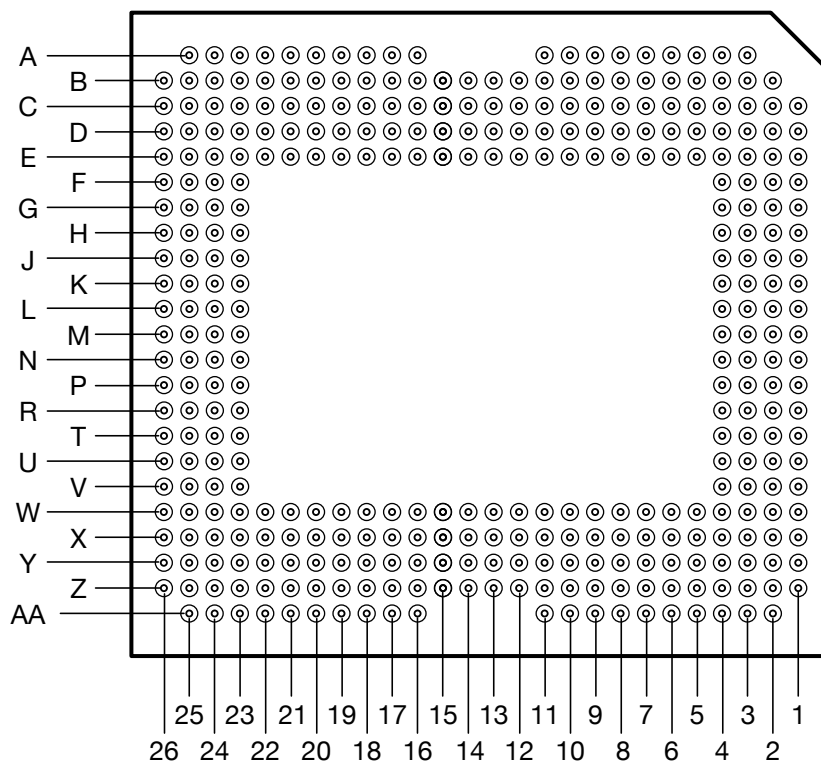


図 4-1. FYU Package (350-Pin) Bottom View

表 4-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | PIN DESCRIPTION | SIGNAL TYPE | TERMINATION |
|------------|---------|---------------------|------------------------------|-------------|-------------------|
| SIGNAL | PGA_PAD | | | | |
| LVDS BUS C | | | | | |
| D_CN(0) | B18 | I | High-speed differential pair | LVDS | Differential 100Ω |
| D_CP(0) | B19 | I | | | |
| D_CN(1) | H24 | I | High-speed differential pair | | Differential 100Ω |
| D_CP(1) | G24 | I | | | |
| D_CN(2) | L23 | I | High-speed differential pair | | Differential 100Ω |
| D_CP(2) | K23 | I | | | |
| D_CN(3) | C18 | I | High-speed differential pair | | Differential 100Ω |
| D_CP(3) | C19 | I | | | |
| D_CN(4) | A19 | I | High-speed differential pair | | Differential 100Ω |
| D_CP(4) | A20 | I | | | |
| D_CN(5) | E24 | I | High-speed differential pair | | Differential 100Ω |
| D_CP(5) | D24 | I | | | |
| D_CN(6) | K25 | I | High-speed differential pair | | Differential 100Ω |
| D_CP(6) | J25 | I | | | |
| D_CN(7) | C26 | I | High-speed differential pair | | Differential 100Ω |
| D_CP(7) | D26 | I | | | |
| D_CN(8) | C21 | I | High-speed differential pair | | Differential 100Ω |
| D_CP(8) | B21 | I | | | |
| D_CN(9) | G25 | I | High-speed differential pair | | Differential 100Ω |
| D_CP(9) | F25 | I | | | |
| D_CN(10) | A24 | I | High-speed differential pair | | Differential 100Ω |
| D_CP(10) | B24 | I | | | |
| D_CN(11) | J26 | I | High-speed differential pair | | Differential 100Ω |
| D_CP(11) | K26 | I | | | |
| D_CN(12) | D25 | I | High-speed differential pair | | Differential 100Ω |
| D_CP(12) | C25 | I | | | |
| D_CN(13) | E23 | I | High-speed differential pair | | Differential 100Ω |
| D_CP(13) | D23 | I | | | |
| D_CN(14) | B23 | I | High-speed differential pair | | Differential 100Ω |
| D_CP(14) | C23 | I | | | |
| D_CN(15) | K24 | I | High-speed differential pair | | Differential 100Ω |
| D_CP(15) | L24 | I | | | |
| DCLK_CN | H23 | I | High-speed differential pair | | Differential 100Ω |
| DCLK_CP | G23 | I | | | |
| SCTRL_CN | F26 | I | High-speed differential pair | | Differential 100Ω |
| SCTRL_CP | G26 | I | | | |
| LVDS BUS D | | | | | |

表 4-1. Pin Functions (続き)

| PIN | | TYPE ⁽¹⁾ | PIN DESCRIPTION | SIGNAL TYPE | TERMINATION |
|---------------|---------|---------------------|-----------------------------------|-------------|-------------------|
| SIGNAL | PGA_PAD | | | | |
| D_DN(0) | Z18 | I | High-speed differential pair | LVDS | Differential 100Ω |
| D_DP(0) | Z19 | I | | | |
| D_DN(1) | T24 | I | High-speed differential pair | | |
| D_DP(1) | U24 | I | | | |
| D_DN(2) | N23 | I | High-speed differential pair | | Differential 100Ω |
| D_DP(2) | P23 | I | | | |
| D_DN(3) | Y18 | I | High-speed differential pair | | Differential 100Ω |
| D_DP(3) | Y19 | I | | | |
| D_DN(4) | AA19 | I | High-speed differential pair | | Differential 100Ω |
| D_DP(4) | AA20 | I | | | |
| D_DN(5) | W24 | I | High-speed differential pair | | Differential 100Ω |
| D_DP(5) | X24 | I | | | |
| D_DN(6) | P25 | I | High-speed differential pair | | Differential 100Ω |
| D_DP(6) | R25 | I | | | |
| D_DN(7) | Y26 | I | High-speed differential pair | | Differential 100Ω |
| D_DP(7) | X26 | I | | | |
| D_DN(8) | Y21 | I | High-speed differential pair | | Differential 100Ω |
| D_DP(8) | Z21 | I | | | |
| D_DN(9) | U25 | I | High-speed differential pair | | Differential 100Ω |
| D_DP(9) | V25 | I | | | |
| D_DN(10) | AA24 | I | High-speed differential pair | | Differential 100Ω |
| D_DP(10) | Z24 | I | | | |
| D_DN(11) | R26 | I | High-speed differential pair | | Differential 100Ω |
| D_DP(11) | P26 | I | | | |
| D_DN(12) | X25 | I | High-speed differential pair | | Differential 100Ω |
| D_DP(12) | Y25 | I | | | |
| D_DN(13) | W23 | I | High-speed differential pair | | Differential 100Ω |
| D_DP(13) | X23 | I | | | |
| D_DN(14) | Z23 | I | High-speed differential pair | | Differential 100Ω |
| D_DP(14) | Y23 | I | | | |
| D_DN(15) | P24 | I | High-speed differential pair | | Differential 100Ω |
| D_DP(15) | N24 | I | | | |
| DCLK_DN | T23 | I | High-speed differential pair | | Differential 100Ω |
| DCLK_DP | U23 | I | | | |
| SCTRL_DN | V26 | I | High-speed differential pair | | Differential 100Ω |
| SCTRL_DP | U26 | I | | | |
| SCP INTERFACE | | | | | |
| SCPCLK | U2 | I | Serial Communications Port CLK | LVC MOS | Internal pulldown |
| SCPDI | T3 | I | Serial Communications Data In | LVC MOS | Internal pulldown |
| SCPENZ | U4 | I | Serial Communications Port Enable | LVC MOS | Internal pulldown |
| SCPDO | U3 | O | Serial Communications Port Output | LVC MOS | Internal pulldown |
| OTHER SIGNALS | | | | | |
| DMD_PWRDNZ | G4 | I | Chip-Level ResetZ | LVC MOS | Internal pulldown |

表 4-1. Pin Functions (続き)

| PIN | | TYPE ⁽¹⁾ | PIN DESCRIPTION | SIGNAL TYPE | TERMINATION |
|--------------------------------------|--|---------------------|-------------------------|-------------|-------------|
| SIGNAL | PGA_PAD | | | | |
| N/C | G1, H1, J1, J3, J4, K3, P3, R1, R3, R4, T1, U1, V3, D17, X17, K4, P4, F3, G2, H3, W18, G3, W6, W5, Y5, Y4, W15, X15, Z16, Z15, Y16, Y17, Z13, Z12, Y14, Y13, AA10, AA9, Z10, Y10, Z5, Z6, Z9, Z8, W3, X3, X6, Y6, X7, X8, Y8, Y7, X4, W4, Y3, Z3, W11, W10, D4, E4, C3, B3, E15, D15, B16, B15, C16, C17, B13, B12, C14, C13, A10, A9, B10, C10, B5, B6, B9, B8, C4, C5, E5, E6, D7, D8, C8, C7, D3, E3, C6, D6, E11, E10, X16 | No Connect | | | |
| TEMP_N | W16 | I/O | | | |
| TEMP_P | W17 | I/O | | | |
| MICROMIRROR BIAS RESET INPUTS | | | | | |
| MBRST(0) | E14 | I | Mirror actuation signal | | |
| MBRST(1) | D13 | I | Mirror actuation signal | | |
| MBRST(2) | E13 | I | Mirror actuation signal | | |
| MBRST(3) | C12 | I | Mirror actuation signal | | |
| MBRST(4) | E12 | I | Mirror actuation signal | | |
| MBRST(5) | C11 | I | Mirror actuation signal | | |
| MBRST(6) | D16 | I | Mirror actuation signal | | |
| MBRST(7) | C15 | I | Mirror actuation signal | | |
| MBRST(8) | W14 | I | Mirror actuation signal | | |
| MBRST(9) | X13 | I | Mirror actuation signal | | |
| MBRST(10) | W13 | I | Mirror actuation signal | | |
| MBRST(11) | Y12 | I | Mirror actuation signal | | |
| MBRST(12) | W12 | I | Mirror actuation signal | | |
| MBRST(13) | Y11 | I | Mirror actuation signal | | |
| MBRST(14) | Y15 | I | Mirror actuation signal | | |
| POWERS AND GROUNDS | | | | | |

表 4-1. Pin Functions (続き)

| PIN | | TYPE ⁽¹⁾ | PIN DESCRIPTION | SIGNAL TYPE | TERMINATION |
|--------|---|---------------------|---------------------------------|-------------|-------------|
| SIGNAL | PGA_PAD | | | | |
| VDD | A5, A6, B2, C1, D10, D12, D19, D22, E8, E19, E20, E21, E22, F1, F2, J2, K1, L1, L25, M3, M4, M25, N1, N25, P1, R2, V1, V2, W8, W19, W20, W21, W22, X10, X12, X19, X22, Y1, Z1, Z2, AA2, AA5, AA6 | P | Low-voltage CMOS core supply | | |
| VDDI | A7, A8, A11, A16, A17, A18, A21, A22, A23, AA7, AA8, AA11, AA16, AA17, AA18, AA21, AA22, AA23 | P | I/O supply | | |
| VCC2 | A3, A4, A25, B26, L26, M26, N26, Z26, AA3, AA4, AA25 | P | Memory array stepped-up voltage | | |
| VSS | B4, B7, B11, B14, B17, B20, B22, B25, C2, C9, C20, C22, C24, D1, D2, D5, D9, D11, D14, D18, D20, D21, E1, E2, E7, E9, E16, E17, E18, E25, E26, F4, F23, F24, H2, H4, H25, H26, J23, J24, K2, L2, L3, L4, M1, M2, M23, M24, N2, N3, N4, P2, R23, R24, T2, T4, T25, T26, V4, V23, V24, W1, W2, W7, W9, W25, W26, X1, X2, X5, X9, X11, X14, X18, X20, X21, Y2, Y9, Y20, Y22, Y24, Z4, Z7, Z11, Z14, Z17, Z20, Z22, Z25 | G | Global ground | | |

(1) I = Input, O = Output, P = Power, G = Ground, NC = No Connect

5 Specifications

5.1 Absolute Maximum Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

| | | MIN | MAX | UNIT |
|------------------------|--|-------|-----------------|------|
| SUPPLY VOLTAGES | | | | |
| V_{DD} | Supply voltage for LVCMOS core logic ⁽¹⁾ | −0.5 | 2.3 | V |
| V_{DDI} | Supply voltage for LVDS Interface ⁽¹⁾ | −0.5 | 2.3 | V |
| V_{CC2} | Micromirror Electrode and HVCMOS voltage ^{(1) (2)} | −0.5 | 11 | V |
| V_{MBRST} | Input voltage for MBRST pins ⁽¹⁾ | −17.5 | 22.5 | V |
| $ V_{DDI} - V_{DD} $ | Supply voltage delta (absolute value) ⁽³⁾ | | 0.3 | V |
| INPUT VOLTAGES | | | | |
| $ V_{ID} $ | Input differential voltage for LVDS pins (absolute value) | | 500 | mV |
| V_{LVCMOS} | Input voltage for all other input pins ⁽¹⁾ | −0.3 | $V_{DDI} + 0.3$ | V |
| ENVIRONMENTAL | | | | |
| T_{ARRAY} | Temperature, operating ⁽⁴⁾ | 0 | 90 | °C |
| | Temperature, nonoperating ⁽⁴⁾ | −40 | 90 | °C |
| T_{DP} | Dew point temperature, operating and non-operating (noncondensing) | | 81 | °C |

- (1) All voltages are referenced to common ground V_{SS} . V_{DD} , V_{DDI} , and V_{CC2} power supplies are all required for all DMD operating modes.
(2) V_{CC2} supply transients must fall within specified voltages.
(3) Exceeding the recommended allowable voltage difference between V_{DD} and V_{DDI} may result in excessive current draw.
(4) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1), shown in [Figure 6-1](#) using the [Micromirror Array Temperature Calculation](#).

5.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system

| | | MIN | MAX | UNIT |
|--------------|---|-----|-----|--------|
| T_{DMD} | DMD storage temperature | −40 | 80 | °C |
| T_{DP-AVG} | Average dew point temperature (noncondensing) ⁽¹⁾ | | 28 | °C |
| T_{DP-ELR} | Elevated dew point temperature range (noncondensing) ⁽²⁾ | 28 | 36 | °C |
| CT_{ELR} | Cumulative time in elevated dew point temperature range | | 24 | months |

- (1) This is the average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation must be limited to less than a total cumulative time of CT_{ELR} .

5.3 ESD Ratings

| SYMBOL | PARAMETER | DESCRIPTION | VALUE | UNIT |
|-------------|--------------------------------------|---|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | ±500 | V |
| $V_{(ESD)}$ | Electrostatic discharge (MBRST PINS) | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 | ±150 | V |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

| | | MIN | NOM | MAX | UNIT |
|------------------------------------|---|-----------------------|------|--------------------------|--------------------|
| VOLTAGE SUPPLY | | | | | |
| V _{DD} | Supply voltage for LVCMOS core logic ⁽¹⁾ | 1.65 | 1.8 | 1.95 | V |
| V _{DDI} | Supply voltage for LVDS Interface ⁽¹⁾ | 1.65 | 1.8 | 1.95 | V |
| V _{CC2} | Micromirror Electrode and HVCMOS voltage ^{(1) (2)} | 9.5 | 10 | 10.5 | V |
| V _{MBRST} | Micromirror Bias / Reset Voltage ⁽¹⁾ | –17 | | 21.5 | V |
| V _{DD} – V _{DDI} | Supply voltage delta (absolute value) ⁽³⁾ | | 0 | 0.3 | V |
| LVCMOS | | | | | |
| V _{IH(DC)} | Input High Voltage | 0.7 × V _{DD} | | V _{DD} + 0.3 | V |
| V _{IL(DC)} | Input Low Voltage | –0.3 | | 0.3 × V _{DD} | V |
| V _{IH(AC)} | Input High Voltage | 0.8 × V _{DD} | | V _{DD} + 0.3 | V |
| V _{IL(AC)} | Input Low Voltage | –0.3 | | 0.2 × V _{DD} | V |
| I _{OH} | High-level Output Current | | | 2 | mA |
| I _{OL} | Low-level Output Current | –2 | | | mA |
| t _{PWRDNZ} | PWRDNZ pulse width ⁽⁴⁾ | 10 | | | ns |
| SCP INTERFACE | | | | | |
| F _{SCPCLK} | SCP clock frequency | 50 | | 500 | kHz |
| SCPCLK _{DCDIN} | SCP Clk Input duty cycle | 40% | | 60% | |
| LVDS INTERFACE | | | | | |
| F _{CLOCK} | Clock frequency for LVDS interface (all channels), DCLK ⁽⁵⁾ | | | 400 | MHz |
| DCD _{IN} | Input CLK Duty Cycle Distortion tolerance | 44% | | 56% | |
| V _{ID} | Input differential voltage (absolute value) ⁽⁶⁾ | 150 | 300 | 440 | mV |
| V _{CM} | Common mode voltage ⁽⁶⁾ | 1100 | 1200 | 1300 | mV |
| V _{LVDS} | LVDS voltage ⁽⁶⁾ | 880 | | 1520 | mV |
| t _{LVDS_RSTZ} | Time required for LVDS receivers to recover from PWRDNZ | 2 | | | μs |
| Z _{IN} | Internal differential termination resistance | 80 | 100 | 120 | Ω |
| Z _{LINE} | Line differential impedance (PWB/trace) | 90 | 100 | 110 | Ω |
| ENVIRONMENTAL | | | | | |
| T _{ARRAY} | Array temperature, long-term operational ^{(7) (8) (9)} | 10 | | 40 to 70 ⁽¹⁰⁾ | °C |
| | Array temperature, short-term operational, 500 hour max ^{(8) (11)} | 0 | | 10 | °C |
| T _{DP-AVG} | Average dew point average temperature (non-condensing) ⁽¹²⁾ | | | 28 | °C |
| T _{DP-ELR} | Elevated dew point temperature range (non-condensing) ⁽¹³⁾ | 28 | | 36 | °C |
| CT _{ELR} | Cumulative time in elevated dew point temperature range | | | 24 | Months |
| Q _{AP-ILL} | Window aperture illumination overfill ^{(14) (15) (16)} | | | 17 | W/cm ² |
| SOLID STATE ILLUMINATION | | | | | |
| ILL _{UV} | Illumination power at wavelengths < 410nm ^{(7) (18)} | | | 10 | mW/cm ² |
| ILL _{VIS} | Illumination power at wavelengths ≥ 410nm and ≤ 800nm ^{(17) (18)} | | | 22 | W/cm ² |
| ILL _{IR} | Illumination power at wavelengths > 800nm ⁽¹⁸⁾ | | | 10 | mW/cm ² |
| ILL _{BLU} | Illumination power at wavelengths ≥ 410nm and ≤ 475nm ^{(17) (18)} | | | 7.5 | W/cm ² |
| ILL _{BLU1} | Illumination power at wavelengths ≥ 410nm and ≤ 440nm ^{(17) (18)} | | | 1.1 | W/cm ² |

(1) All voltages are referenced to common ground V_{SS}. V_{DD}, V_{DDI}, and V_{CC2} power supplies are all required for proper DMD operation. V_{SS} must also be connected.

(2) V_{CC2} supply transients must fall within specified max voltages.

- (3) To prevent excess current, the supply voltage delta $|V_{DDI} - V_{DD}|$ must be less than the specified limit. See the [DMD Power Supply Requirements](#).
- (4) PWRDNZ input pin resets the SCP and disables the LVDS receivers. The PWRDNZ input pin overrides the SCPENZ input pin and tristates the SCPDO output pin.
- (5) See LVDS clock timing requirements in [Timing Requirements](#).
- (6) See [Figure 5-5](#) for the LVDS waveform requirements.
- (7) Simultaneous exposure of the DMD to the maximum [Recommend Operating Conditions](#) for temperature and UV illumination reduces device lifetime.
- (8) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1), shown in [Figure 6-1](#) using the [Micromirror Array Temperature Calculation](#).
- (9) Long-term is defined as the usable life of the device.
- (10) Per [Figure 5-1](#), the maximum operational array temperature is derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See [Micromirror Landed-on/Landed-off Duty Cycle](#) for a definition of micromirror landed duty cycle.
- (11) Short-term is the total cumulative time over the useful life of the device.
- (12) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
- (13) Exposure to dew point temperatures in the elevated range during storage and operation is limited to less than a total cumulative time of CT_{ELR} .
- (14) Applies to region defined in [Figure 5-2](#)
- (15) The active area of the DMD is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. Minimizing the light flux incident outside the active array is a design requirement of the illumination optical system. Depending on the particular optical architecture and assembly tolerances of the optical system, the amount of overfill light on the outside of the active array may cause system performance degradation.
- (16) To calculate see [Window Aperture Illumination Overfill Calculation](#).
- (17) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature (T_{ARRAY}).
- (18) To calculate see [Micromirror Power Density Calculation](#).

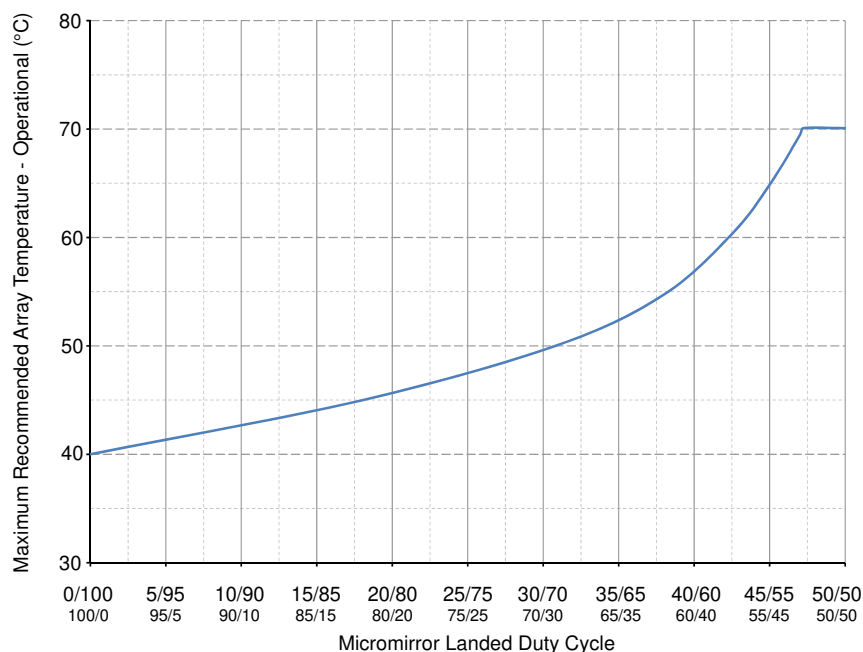


图 5-1. Maximum Recommended Array Temperature—Derating Curve

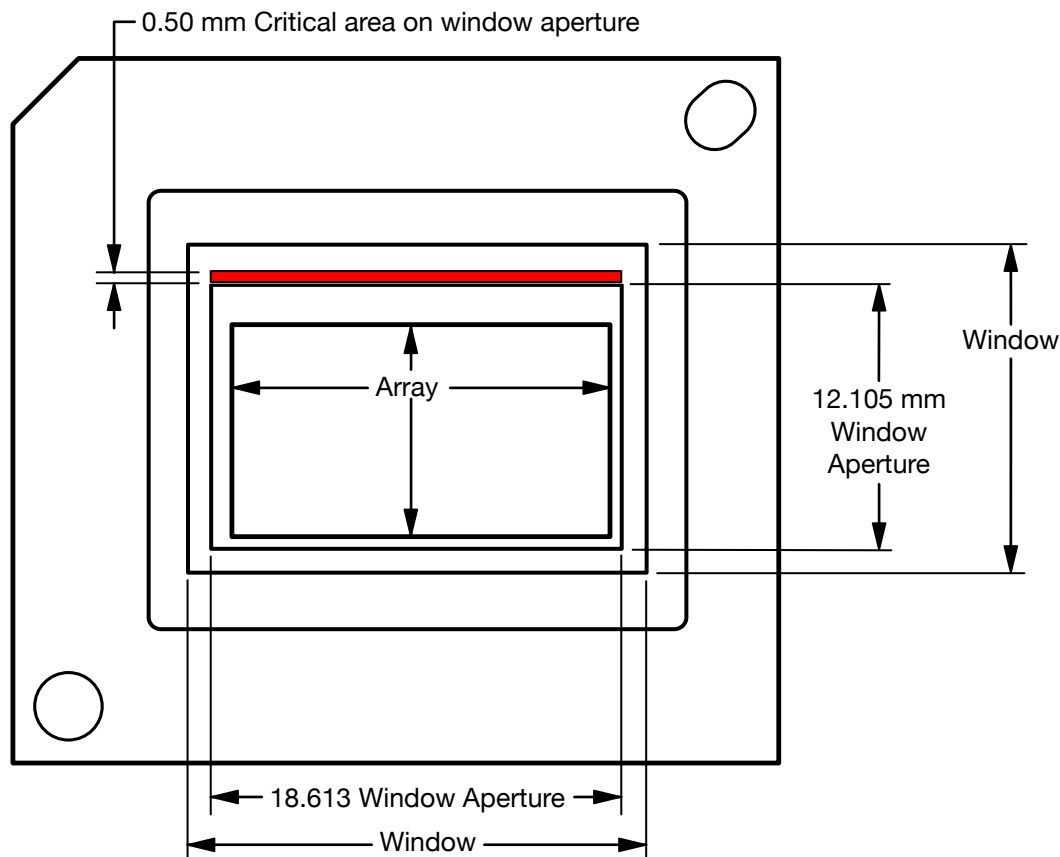


図 5-2. Illumination Overfill Diagram—Critical Area

5.5 Thermal Information

| THERMAL METRIC | DLP780NE | UNIT |
|--|----------|------|
| | FYU | |
| | 350 PINS | |
| Thermal resistance, active area to test point 1 (TP1) ⁽¹⁾ | 0.55 | °C/W |

- (1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the DMD within the temperature range specified in the [Recommended operating conditions](#). The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Minimizing the light energy falling outside the window clear aperture is a design requirement of the optical system because any additional thermal load in this area can significantly degrade the reliability of the device.

5.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|---|-----------------|-----|-----|------|------|
| Power Supply Information | | | | | | |
| I_{DD} | Supply current V_{DD} ⁽¹⁾ | | | | 800 | mA |
| I_{DDI} | Supply current V_{DDI} ⁽¹⁾ | | | | 170 | mA |
| I_{CC2} | Supply current V_{CC2} | | | | 40 | mA |
| P_{DD} | Supply power V_{DD} ⁽¹⁾ | | | | 1560 | mW |
| P_{DDI} | Supply power V_{DDI} ⁽¹⁾ | | | | 332 | mW |
| P_{CC2} | Supply power V_{CC2} ⁽¹⁾ | | | | 420 | mW |

5.6 Electrical Characteristics (続き)

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|---|--|-----|-----|-----|-------------------|
| LVCMOS | | | | | | |
| V _{OH} | High-level output voltage | I _{OH} = 2mA | 0.8 | | | × V _{DD} |
| V _{OL} | Low-level output voltage | I _{OL} = 2mA | | | 0.2 | × V _{DD} |
| I _{OZ} | High impedance output current | V _{DD} = 1.95V | | | 10 | μA |
| I _{IL} | Low-level input current | V _{DD} = 1.95V, V _{in} = 0V | –60 | | | μA |
| I _{IH} | High-level input current ⁽²⁾ | V _{DD} = 1.95V, V _{in} = V _{DD} | | | 200 | μA |
| Capacitances | | | | | | |
| C _I | Input capacitance: LVDS pins | f = 1MHz | | | 20 | pF |
| C _I | Input capacitance ⁽²⁾ | f = 1MHz | | | 15 | pF |
| C _O | Output capacitance ⁽²⁾ | f = 1MHz | | | 15 | pF |
| C _{IM} | Input capacitance for MBRST[0:14] pins | f = 75kHz | 360 | 410 | 520 | pF |

(1) To prevent excess current, the supply voltage delta |V_{DDI} – V_{DD}| must be less than the specified limit in [Absolute Maximum Ratings](#).

(2) Applies to LVCMOS pins only. Excludes LVDS pins and test pad pins

5.7 Timing Requirements

Over [Recommended Operating Conditions](#) (unless otherwise noted)

| PARAMETER DESCRIPTION | | MIN | NOM | MAX | UNIT |
|---------------------------|--|-------|-----|------|-------------------------|
| SCP | | | | | |
| t _{SCP_DS} | SCPDI clock setup time (before SCPCLK falling-edge) ⁽¹⁾ | 800 | | | ns |
| t _{SCP_DH} | SCPDI hold time (after SCPCLK falling-edge) ⁽¹⁾ | 900 | | | ns |
| t _{SCP_NEG_EN Z} | Time between falling edge of SCPENZ and the rising edge of SCPCLK ⁽¹⁾ | 1 | | | μs |
| t _{SCP_POS_EN Z} | Time between falling edge of SCPCLK and the rising edge of SCPENZ ⁽¹⁾ | 1 | | | μs |
| t _{SCP_OUT_EN} | Time required for SCP output buffer to recover after SCPENZ (from tri-state). ⁽¹⁾ | | | 960 | ns |
| t _{SCP_PW_ENZ} | SCPENZ inactive pulse width (high-level) | 1 | | | 1/F _{scpclock} |
| t _r | Rise time (20% to 80%). See ⁽²⁾ | | | 200 | ns |
| t _f | Fall time (80% to 20%). See ⁽²⁾ | | | 200 | ns |
| LVDS | | | | | |
| t _{R_LVDS} | Rise time (20% to 80%). See ⁽³⁾ | | | 500 | ps |
| t _{F_LVDS} | Fall time (80% to 20%). See ⁽³⁾ | | | 500 | ps |
| t _C | Clock Cycle Duration for DCLK_C and DCLK_D ⁽⁴⁾ | 2.5 | | | ns |
| t _W | Pulse Duration for DCLK_C/D ⁽⁴⁾ | 1.19 | | | ns |
| t _{SU_data} | Setup Time for High-speed data(15:0) before DCLK ⁽⁴⁾ | 350 | | | ps |
| t _{SU_sctrl} | Setup Time for SCTRL before DCLK ⁽⁴⁾ | 330 | | | ps |
| t _{H_data} | Hold time for High-speed data(15:0) after DCLK ⁽⁴⁾ | 150 | | | ps |
| t _{H_sctrl} | Hold Time for SCTRL after DCLK ⁽⁴⁾ | 170 | | | ps |
| t _{SKEW_C2D} | Skew tolerance between Channel C and Channel D ^{(5) (6) (7)} | –1.25 | | 1.25 | ns |

(1) See [Figure 5-3](#).

(2) See [Figure 5-4](#).

(3) See [Figure 5-6](#).

(4) See [Figure 5-7](#).

(5) See [Figure 5-8](#).

(6) Channel C (Bus C) includes the following LVDS pairs: DCLK_C, SCTRL_C, and D_C

(7) Channel D (Bus D) includes the following LVDS pairs: DCLK_D, SCTRL_D, and D_D.

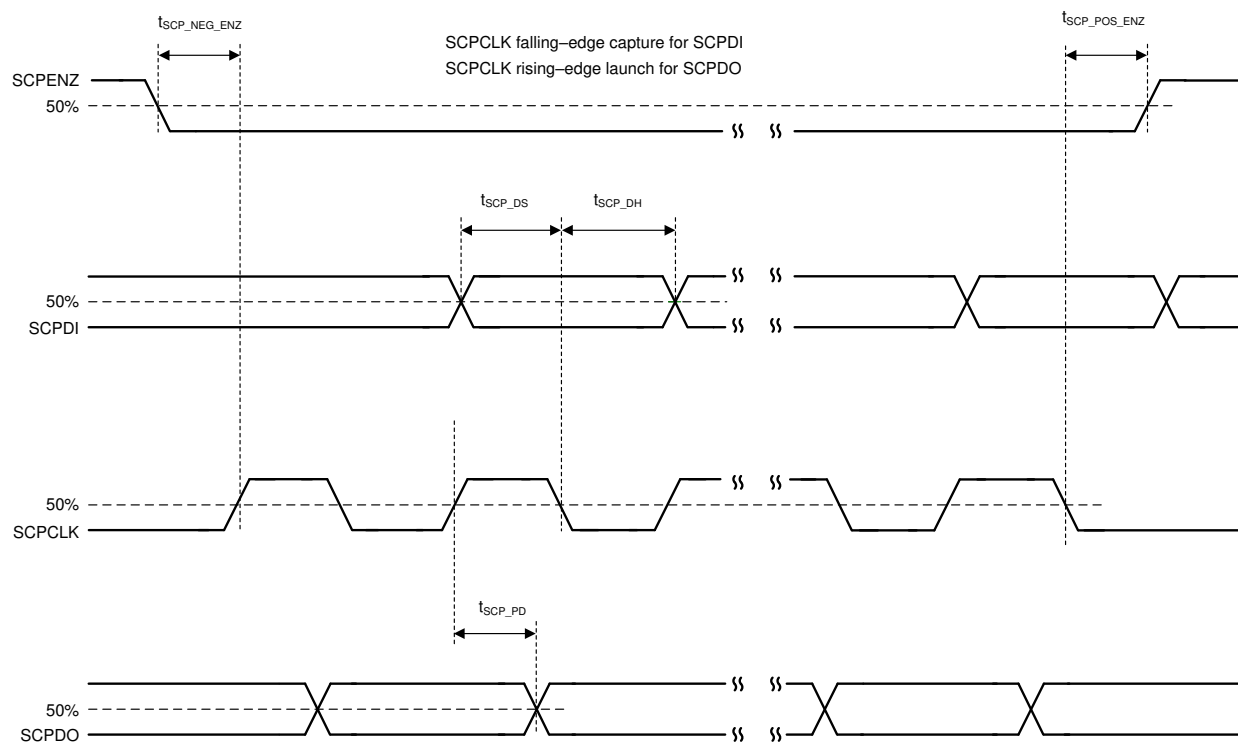


図 5-3. SCP Timing Parameters

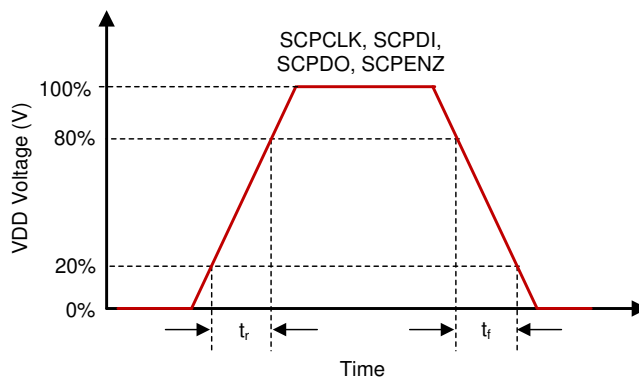
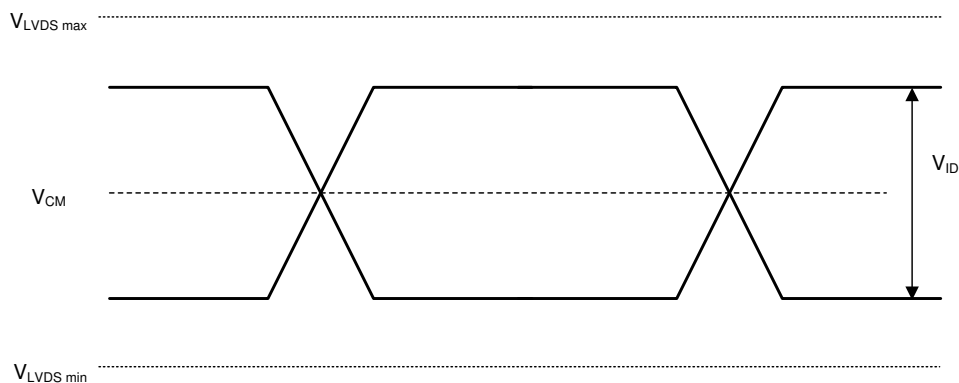
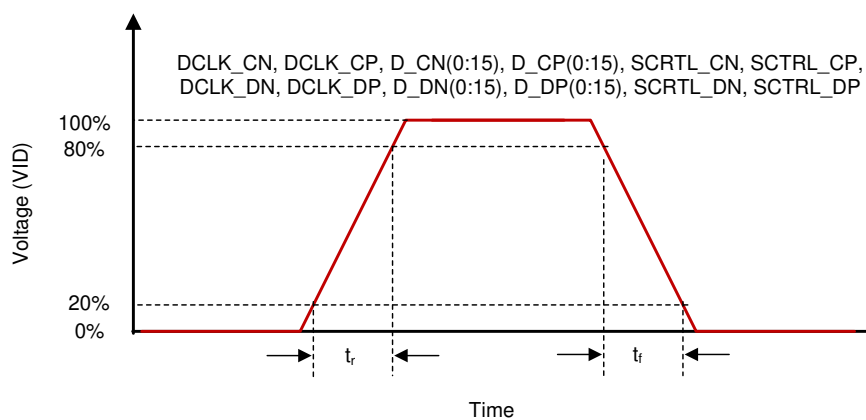


図 5-4. SCP Rise and Fall Times


 **5-5. LVDS Waveform Parameters**

 **5-6. LVDS Rise and Fall Times**

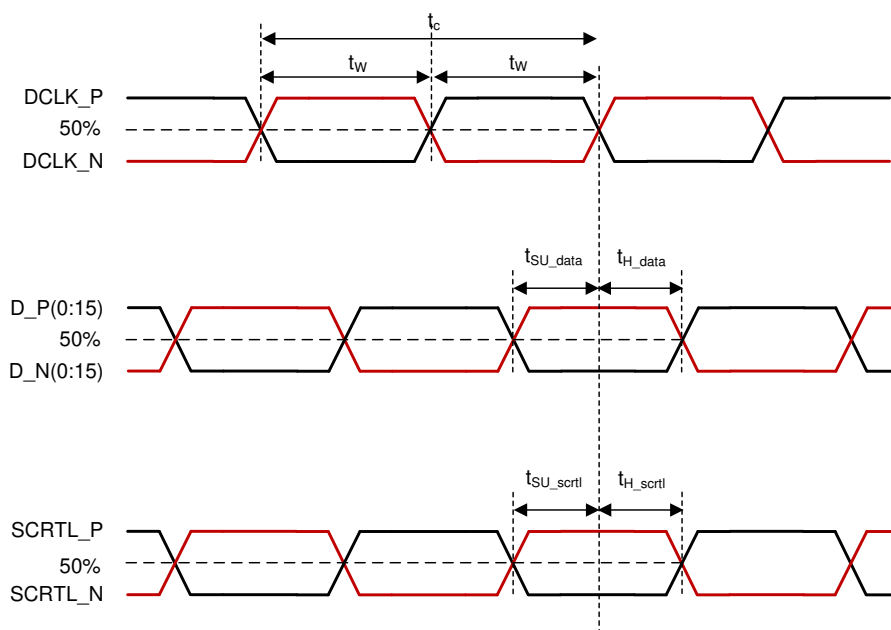


図 5-7. LVDS Timing Parameters

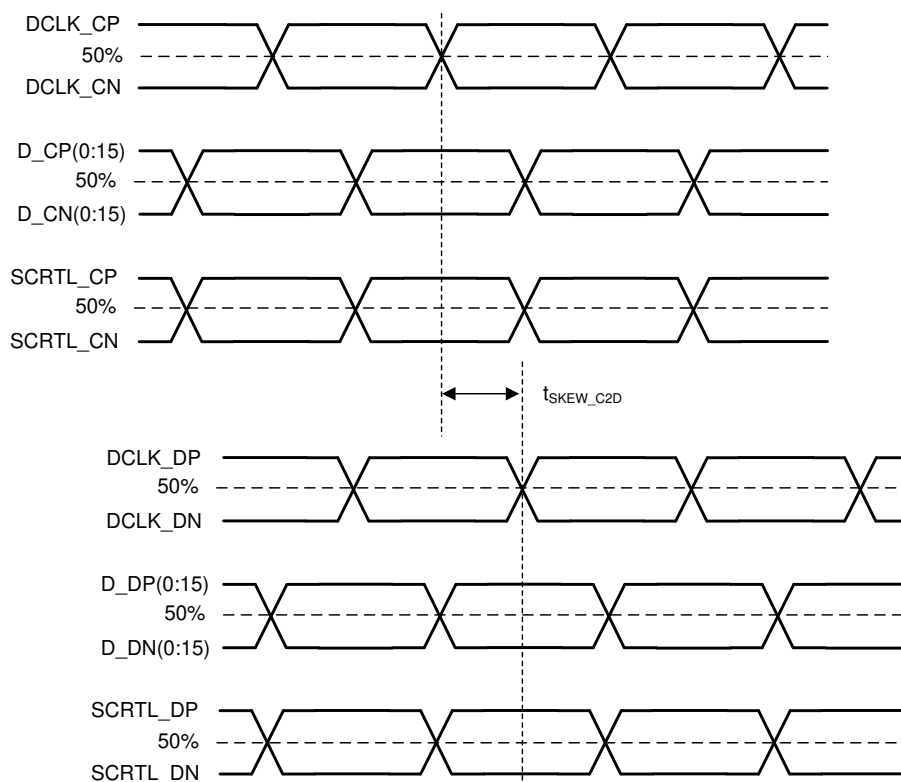


図 5-8. LVDS Skew Parameters

5.8 System Mounting Interface Loads

| PARAMETER | MIN | NOM | MAX | UNIT |
|--|-----|-----|-----|------|
| When loads are applied on both electrical and thermal interface areas | | | | |
| Maximum load to be applied to the electrical interface area ⁽¹⁾ | | | 111 | N |
| Maximum load to be applied to the thermal interface area ⁽¹⁾ | | | 111 | N |
| When load is applied on the electrical interface area only | | | | |
| Maximum load to be applied to the electrical interface area ⁽¹⁾ | | | 222 | N |
| Maximum load to be applied to the thermal interface area ⁽¹⁾ | | | 0 | N |

(1) The load must be uniformly applied in the corresponding areas shown in [Figure 5-9](#).

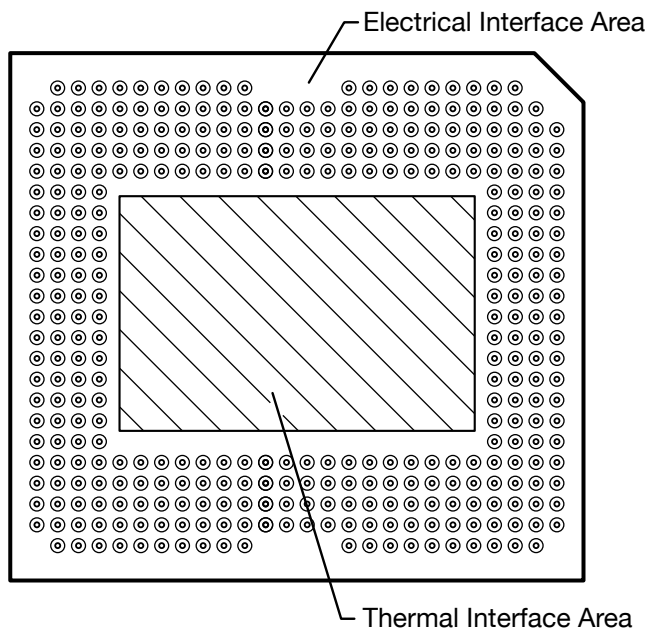


図 5-9. System Mounting Interface Loads

5.9 Micromirror Array Physical Characteristics

| PARAMETER DESCRIPTION | | VALUE | UNIT |
|---|--|--------|-------------------|
| M | Number of active columns ⁽¹⁾ | 1920 | micromirrors |
| N | Number of active rows ⁽¹⁾ | 1080 | micromirrors |
| P | Micromirror (pixel) pitch ⁽¹⁾ | 9.0 | μm |
| Micromirror active array width ⁽¹⁾ | Micromirror pitch x number of active columns | 17.280 | mm |
| Micromirror active array height ⁽¹⁾ | Micromirror pitch x number of active rows | 9.720 | mm |
| Micromirror active border (top and bottom) ⁽²⁾ | Pond of micromirror (POM) | 12 | micromirrors/side |
| Micromirror active border (right and left) ⁽²⁾ | Pond of micromirror (POM) | 12 | micromirrors/side |

(1) See Figure 5-10.

(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

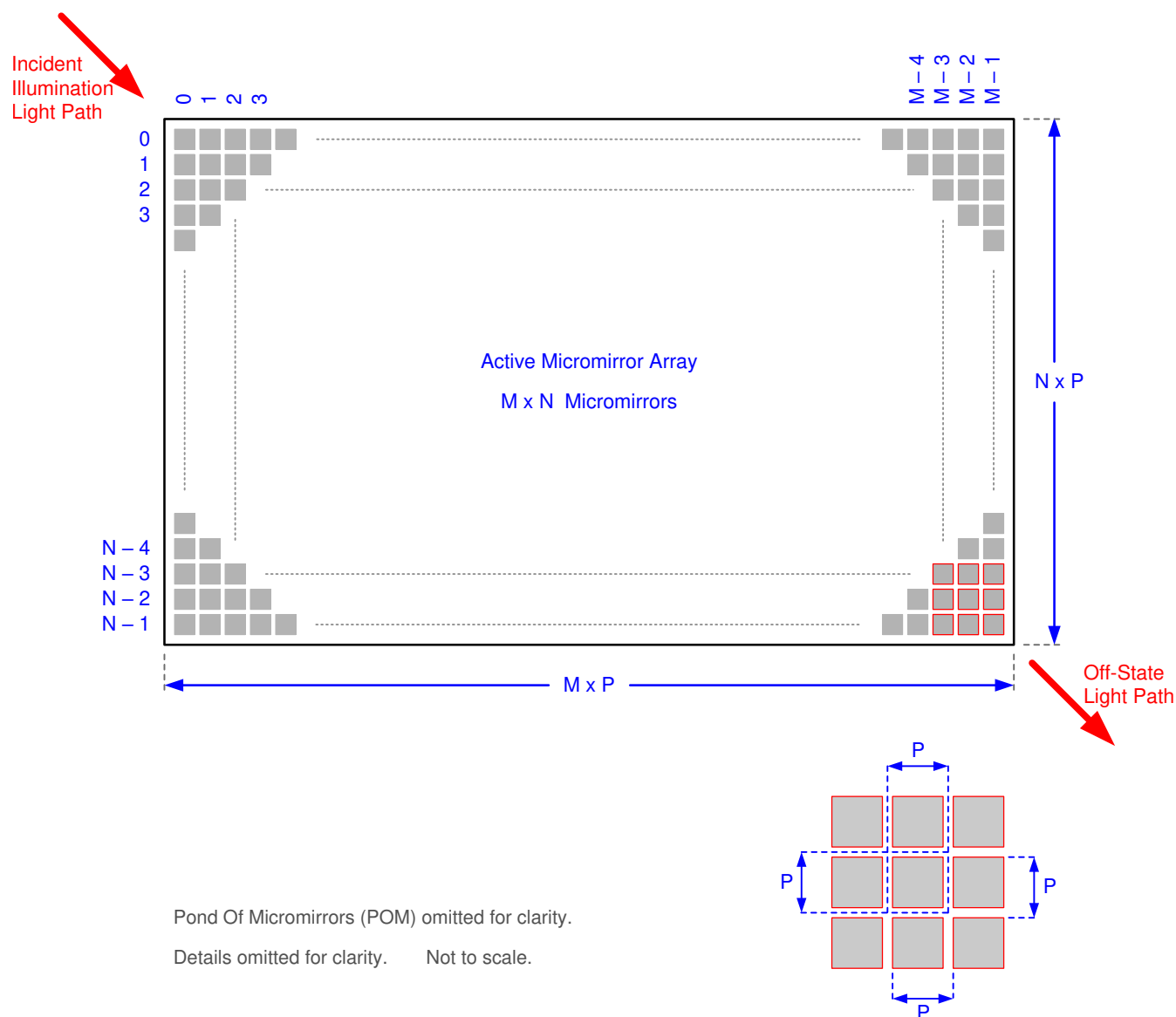


図 5-10. Micromirror Array Physical Characteristics

5.10 Micromirror Array Optical Characteristics

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|---|--------------------------------|------|------|------|--------------|
| | Micromirror tilt angle ^{(2) (3) (4) (5)} | Landed state ⁽¹⁾ | 13.5 | 14.5 | 15.5 | degrees |
| | Micromirror crossover time ⁽⁶⁾ | typical performance | | 3 | | μs |
| | Micromirror switching time ⁽⁷⁾ | typical performance | 10 | | | μs |
| Image performance ⁽⁸⁾ | Bright pixel(s) in active area ⁽⁹⁾ | Gray 10 screen ⁽¹²⁾ | | | 0 | micromirrors |
| | Bright pixel(s) in the POM ^{(9) (11)} | Gray 10 screen ⁽¹²⁾ | | | 1 | |
| | Dark pixel(s) in the active area ⁽¹⁰⁾ | White screen ⁽¹³⁾ | | | 4 | |
| | Adjacent pixel(s) ⁽¹⁴⁾ | Any screen | | | 0 | |
| | Unstable pixel(s) in active area ⁽¹⁵⁾ | Any screen | | | 0 | |

- (1) Measured relative to the plane formed by the overall micromirror array.
- (2) Additional variation exists between the micromirror array and the package datums.
- (3) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
- (4) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
- (5) Refer to [Figure 5-11](#).
- (6) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
- (7) The minimum time between successive transitions of a micromirror.
- (8) Conditions of Acceptance: all DMD image performance returns are evaluated using the following projected image test conditions:
 Test set degamma shall be linear.
 Test set brightness and contrast shall be set to nominal.
 The diagonal size of the projected image shall be a minimum of 60 inches.
 The projections screen shall be 1× gain.
 The projected image shall be inspected from an 8-foot minimum viewing distance.
 The image shall be in focus during all image performance tests.
- (9) Bright pixel definition: a single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
- (10) Dark pixel definition: a single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
- (11) POM definition: rectangular border of off-state mirrors surrounding the active area
- (12) Gray 10 screen definition: a full screen with RGB values set to R = 10/255, G = 10/255, B = 10/255
- (13) White screen definition: a full screen with RGB values set to R=255/255, G = 255/255, B = 255/255
- (14) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster.
- (15) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

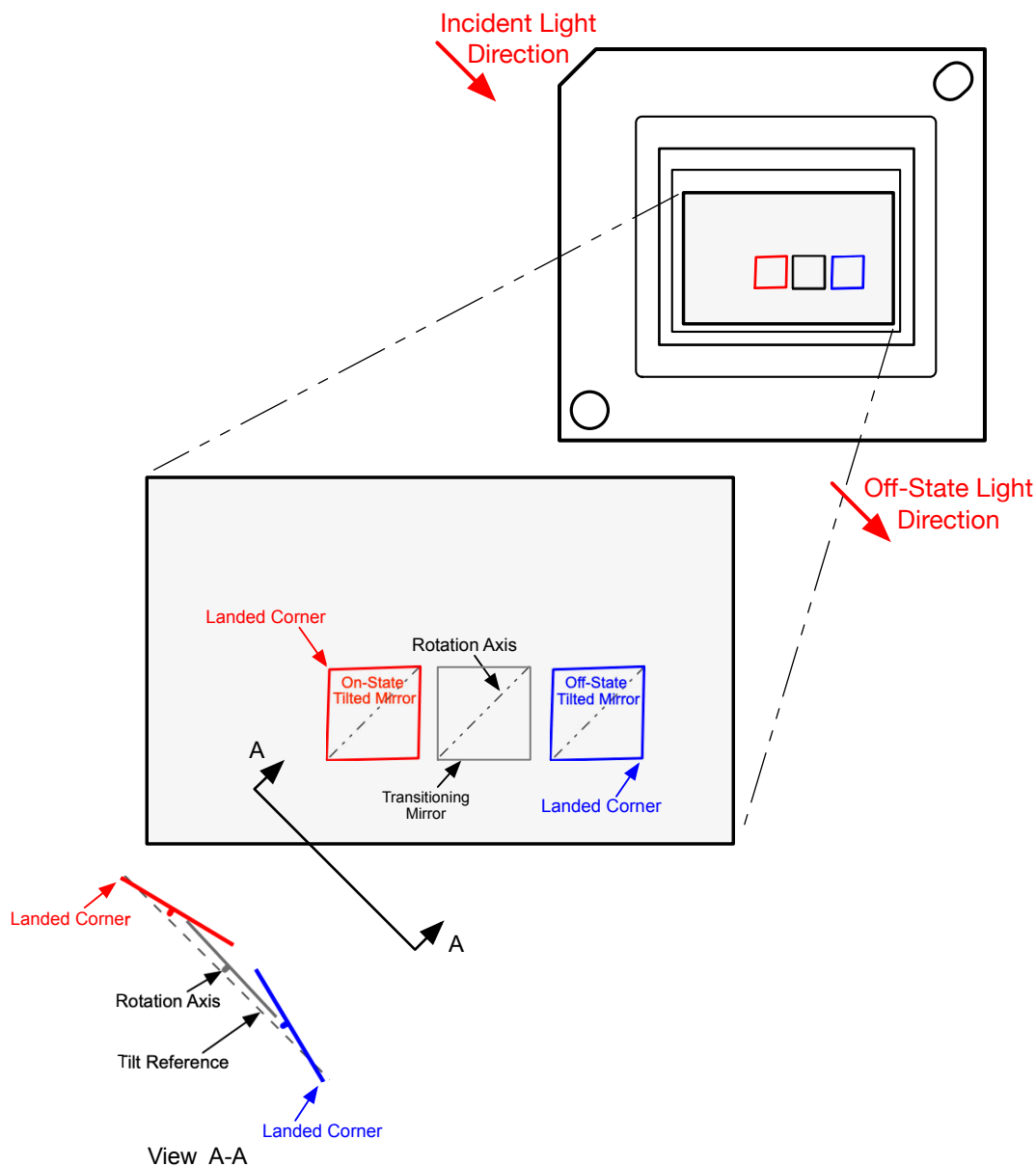


図 5-11. Micromirror Landed Orientation and Tilt

5.11 Window Characteristics

| PARAMETER DESCRIPTION | Test Conditions | MIN | NOM | MAX | UNIT |
|-------------------------|-----------------|-----------------|--------|-----|------|
| Window Material | | Corning EagleXG | | | |
| Window Refractive Index | 546.1nm | | 1.5119 | | |

5.12 Chipset Component Usage Specification

Reliable function and operation of the DLP780NE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

注

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

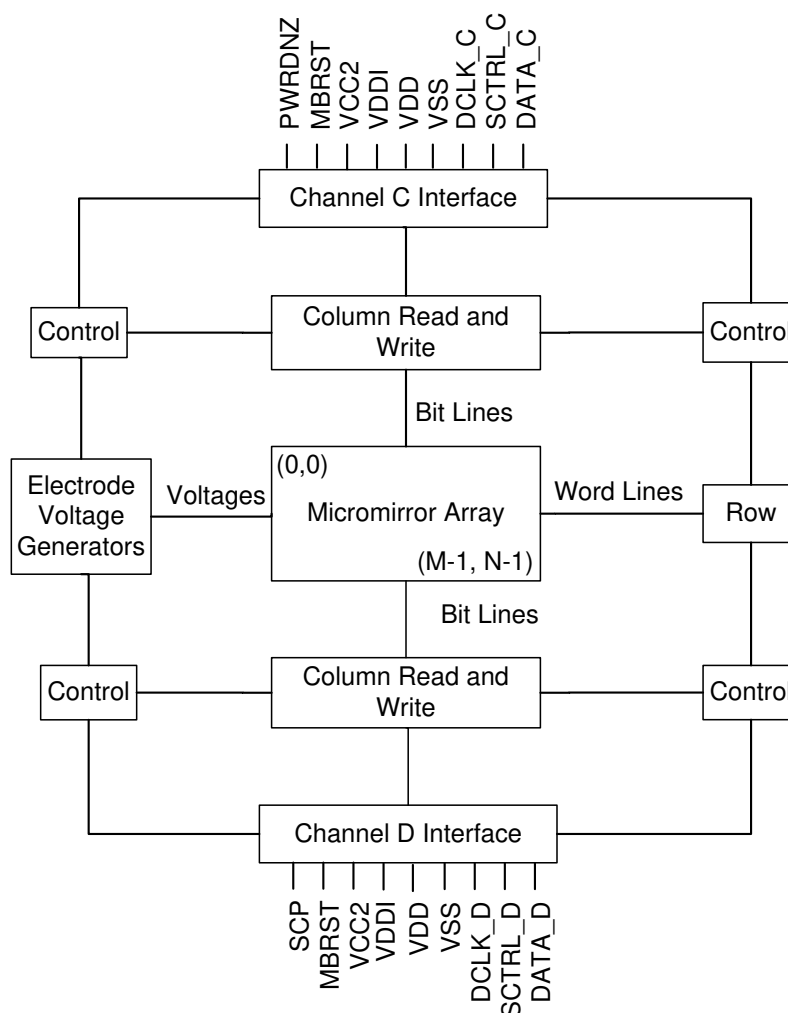
6 Detailed Description

6.1 Overview

The DMD is a 0.78-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-optical-electrical-mechanical system (MOEMS). The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables the micromirror array to display a full 1920 × 1080 pixel image at a 120Hz frame rate. The electrical interface is a low voltage differential signaling (LVDS) interface. The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the [セクション 6.2](#). The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP 0.78 インチ フル HD chipset is comprised of the DLP780NE DMD, DLPC4430 ディスプレイ コントローラ, the DLPA300 micromirror driver and the [DLPA100](#) power management and motor driver. For reliable operation, the DLP780NE DMD must always be used with the DLP display controller and the power and motor driver specified in the chipset.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Power Interface

The DMD requires two DC voltages: 1.8-V source for VDD and VDDI, and a 10-V supply for VCC2. In a typical configuration, 3.3V is created by the [DLPA100](#) power management and motor driver and is used on the DMD board to create the 1.8V. The [DLPA300](#) micromirror driver takes in 12V and creates the micromirror reset voltages.

6.3.2 Timing

The data sheet specifies timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Timing reference loads are not intended to be precise representations of any particular system environment or depiction of the actual load presented by a production test. TI recommends that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. Use the specified load capacitance value for characterization and measurement of AC timing signals only. This load capacitance value does not indicate the maximum load the device is capable of driving.

6.4 Device Functional Modes

DMD functional modes are controlled by the DLPC4430 ディスプレイ コントローラ. See the DLPC4430 ディスプレイ コントローラ data sheet or contact a TI applications engineer.

6.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

6.5.1 Numerical Aperture and Stray Light Control

TI recommends that the light cone angle defined by the numerical aperture of the illumination optics is the same as the light cone angle defined by the numerical aperture of the projection optics. This angle must not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and projection pupils to block out flat-state and stray light from the projection lens. The DLP780NE has a 14.5° tilt angle which corresponds to the f/2.0 numerical aperture. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than 2° larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border or active area are possible.

6.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

6.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the

average flux level in the active area. Depending on the particular system optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

6.6 Micromirror Array Temperature Calculation

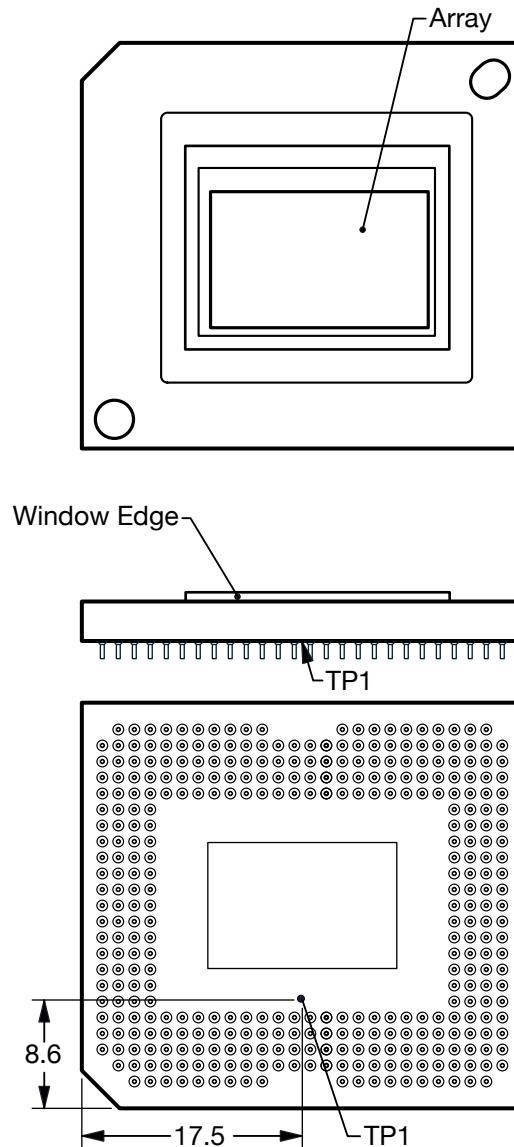


図 6-1. DMD Thermal Test Point

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from a measurement point on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The following equations show the relationship between array temperature and the reference ceramic temperature, thermal test TP1, shown above:

$$T_{\text{ARRAY}} = T_{\text{CERAMIC}} + (Q_{\text{ARRAY}} \times R_{\text{ARRAY-TO-CERAMIC}}) \quad (1)$$

$$Q_{\text{ARRAY}} = Q_{\text{ELECTRICAL}} + Q_{\text{ILLUMINATION}} \quad (2)$$

where

- T_{ARRAY} = Computed array temperature ($^{\circ}\text{C}$)
- T_{CERAMIC} = Measured ceramic temperature ($^{\circ}\text{C}$) (TP1 location)
- $R_{\text{ARRAY-TO-CERAMIC}}$ = Thermal resistance of package specified in セクション 5.5 from array to ceramic TP1 ($^{\circ}\text{C}/\text{Watt}$)
- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{\text{ELECTRICAL}}$ = Nominal electrical power (W)
- Q_{INCIDENT} = Incident illumination optical power (W)
- $Q_{\text{ILLUMINATION}}$ = (DMD average thermal absorptivity $\times Q_{\text{INCIDENT}}$) (W)
- DMD average thermal absorptivity = 0.55

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 1.0W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single chip or multichip DMD system. It assumes an illumination distribution of 83.7% on the active array, and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$$Q_{\text{INCIDENT}} = 40\text{W (measured)} \quad (3)$$

$$T_{\text{CERAMIC}} = 55.0^{\circ}\text{C (measured)} \quad (4)$$

$$Q_{\text{ELECTRICAL}} = 1.0\text{W} \quad (5)$$

$$Q_{\text{ARRAY}} = 1.0\text{W} + (0.55 \times 40\text{W}) = 23.00\text{W} \quad (6)$$

$$T_{\text{ARRAY}} = 55.0^{\circ}\text{C} + (23.00\text{W} \times 0.55^{\circ}\text{C/W}) = 67.7^{\circ}\text{C} \quad (7)$$

6.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{\text{UV}} = [OP_{\text{UV-RATIO}} \times Q_{\text{INCIDENT}}] \times 1000 \div A_{\text{ILL}}$ (mW/cm^2)
- $ILL_{\text{VIS}} = [OP_{\text{VIS-RATIO}} \times Q_{\text{INCIDENT}}] \div A_{\text{ILL}}$ (W/cm^2)
- $ILL_{\text{IR}} = [OP_{\text{IR-RATIO}} \times Q_{\text{INCIDENT}}] \times 1000 \div A_{\text{ILL}}$ (mW/cm^2)
- $ILL_{\text{BLU}} = [OP_{\text{BLU-RATIO}} \times Q_{\text{INCIDENT}}] \div A_{\text{ILL}}$ (W/cm^2)
- $ILL_{\text{BLU1}} = [OP_{\text{BLU1-RATIO}} \times Q_{\text{INCIDENT}}] \div A_{\text{ILL}}$ (W/cm^2)
- $A_{\text{ILL}} = A_{\text{ARRAY}} \div (1 - OV_{\text{ILL}})$ (cm^2)

where:

- ILL_{UV} = UV illumination power density on the DMD (mW/cm^2)
- ILL_{VIS} = VIS illumination power density on the DMD (W/cm^2)
- ILL_{IR} = IR illumination power density on the DMD (mW/cm^2)
- ILL_{BLU} = BLU illumination power density on the DMD (W/cm^2)
- ILL_{BLU1} = BLU1 illumination power density on the DMD (W/cm^2)
- A_{ILL} = illumination area on the DMD (cm^2)

- Q_{INCIDENT} = total incident optical power on DMD (W) (measured)
- A_{ARRAY} = area of the array (cm^2) (data sheet)
- OV_{ILL} = percent of total illumination on the DMD outside the array (%) (optical model)
- $OP_{\text{UV-RATIO}}$ = ratio of the optical power for wavelengths $<410\text{nm}$ to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{\text{VIS-RATIO}}$ = ratio of the optical power for wavelengths ≥ 410 and $\leq 800\text{nm}$ to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{\text{IR-RATIO}}$ = ratio of the optical power for wavelengths $>800\text{nm}$ to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{\text{BLU-RATIO}}$ = ratio of the optical power for wavelengths ≥ 410 and $\leq 475\text{nm}$ to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{\text{BLU1-RATIO}}$ = ratio of the optical power for wavelengths ≥ 410 and $\leq 440\text{nm}$ to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array (OV_{ILL}) and the percent of the total illumination that is on the active array. From these values the illumination area (A_{ILL}) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation:

$$Q_{\text{INCIDENT}} = 40\text{W (measured)} \quad (8)$$

$$A_{\text{ARRAY}} = (17.280\text{mm} \times 9.72\text{mm}) \div 100 = 1.6796\text{cm}^2 \text{ (data sheet)} \quad (9)$$

$$OV_{\text{ILL}} = 16.3\% \text{ (optical model)} \quad (10)$$

$$OP_{\text{UV-RATIO}} = 0.00017 \text{ (spectral measurement)} \quad (11)$$

$$OP_{\text{VIS-RATIO}} = 0.99977 \text{ (spectral measurement)} \quad (12)$$

$$OP_{\text{IR-RATIO}} = 0.00006 \text{ (spectral measurement)} \quad (13)$$

$$OP_{\text{BLU-RATIO}} = 0.28100 \text{ (spectral measurement)} \quad (14)$$

$$OP_{\text{BLU1-RATIO}} = 0.03200 \text{ (spectral measurement)} \quad (15)$$

$$A_{\text{ILL}} = 1.6796\text{cm}^2 \div (1 - 0.163) = 2.0067\text{cm}^2 \quad (16)$$

$$ILL_{\text{UV}} = [0.00017 \times 40\text{W}] \times 1000 \div 2.0067\text{cm}^2 = 3.39\text{mW/cm}^2 \quad (17)$$

$$ILL_{\text{VIS}} = [0.99977 \times 40\text{W}] \div 2.0067\text{cm}^2 = 19.93\text{W/cm}^2 \quad (18)$$

$$ILL_{\text{IR}} = [0.00006 \times 40\text{W}] \times 1000 \div 2.0067\text{cm}^2 = 1.20\text{mW/cm}^2 \quad (19)$$

$$ILL_{\text{BLU}} = [0.28100 \times 40\text{W}] \div 2.0067\text{cm}^2 = 5.60\text{W/cm}^2 \quad (20)$$

$$ILL_{\text{BLU1}} = [0.03200 \times 40\text{W}] \div 2.0067\text{cm}^2 = 0.64\text{W/cm}^2 \quad (21)$$

6.8 Window Aperture Illumination Overfill Calculation

The amount of optical overfill on the critical area of the window aperture cannot be measured directly. For systems with uniform illumination on the array the amount is determined using the total measured incident optical power on the DMD, and the ratio of the total optical power on the DMD that is on the defined critical area. The optical model is used to determine the percent of optical power on the window aperture critical area and estimate the size of the area.

$$Q_{AP-ILL} = [Q_{INCIDENT} \times OP_{AP_ILL_RATIO}] \div A_{AP_ILL} \text{ (W/cm}^2\text{)}$$

where:

- Q_{AP-ILL} = window aperture illumination overfill (W/cm²)
- $Q_{INCIDENT}$ = total incident optical power on the DMD (Watts) (measured)
- $OP_{AP_ILL_RATIO}$ = ratio of the optical power on the critical area of the window aperture to the total optical power on the DMD (optical model)
- A_{AP-ILL} = size of the window aperture critical area (cm²) (datasheet)
- OP_{CA_RATIO} = percent of the window aperture critical area with incident optical power (%) (optical model)

Sample calculation:

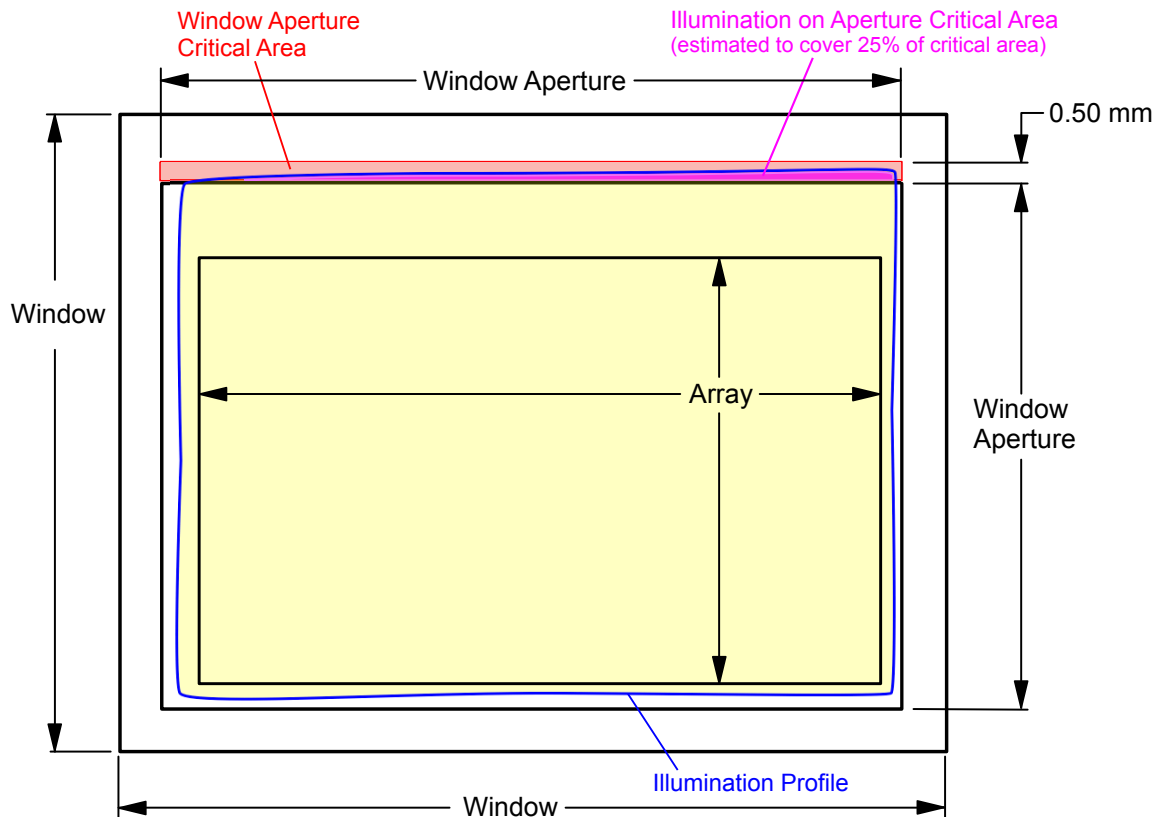


図 6-2. Window Aperture Overfill Example

See the figure for the length of the critical aperture.

$$Q_{INCIDENT} = 40W \text{ (measured)}$$

(22)

$$OP_{AP_ILL_RATIO} = 0.312\% \text{ (optical model)} \quad (23)$$

$$OV_{CA_RATIO} = 25\% \text{ (optical model)} \quad (24)$$

$$\text{Length of the window aperture for critical area} = 1.8613\text{cm} \text{ (data sheet)} \quad (25)$$

$$\text{Width of critical area} = 0.050\text{cm} \text{ (data sheet)} \quad (26)$$

$$A_{AP_ILL} = 1.8613\text{cm} \times 0.050\text{cm} = 0.093065 \text{ (cm}^2\text{)} \quad (27)$$

$$Q_{AP_ILL} = (40\text{W} \times 0.00312) \div (0.093065\text{cm}^2 \times 0.25) = 5.4 \text{ (W/cm}^2\text{)} \quad (28)$$

6.9 Micromirror Landed-On/Landed-Off Duty Cycle

6.9.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the percentage of time that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

For example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time); whereas 0/100 indicates that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

6.9.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD useful life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

6.9.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD useful life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD useful life. This is quantified in the derating curve shown in [Figure 5-1](#).

The importance of this curve is that:

- All points along this curve represent the same useful life.
- All points above this curve represent lower useful life (and the further away from the curve, the lower the useful life).
- All points below this curve represent higher useful life (and the further away from the curve, the higher the useful life).

In practice, this curve specifies the maximum operating DMD temperature for a given long-term average landed duty cycle.

6.9.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in 表 6-1.

表 6-1. Grayscale Value and Landed Duty Cycle

| GRAYSCALE VALUE | LANDED DUTY CYCLE |
|-----------------|-------------------|
| 0% | 0/100 |
| 10% | 10/90 |
| 20% | 20/80 |
| 30% | 30/70 |
| 40% | 40/60 |
| 50% | 50/50 |
| 60% | 60/40 |
| 70% | 70/30 |
| 80% | 80/20 |
| 90% | 90/10 |
| 100% | 100/0 |

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use 式 29 to calculate the landed duty cycle of a given pixel during a given time period.

$$\text{Landed Duty Cycle} = (\text{Red_Cycle_}\% \times \text{Red_Scale_Value}) + (\text{Green_Cycle_}\% \times \text{Green_Scale_Value}) + (\text{Blue_Cycle_}\% \times \text{Blue_Scale_Value}) \quad (29)$$

where

- Red_Cycle_% represents the percentage of the frame time that red is displayed to achieve the desired white point.
- Green_Cycle_% represents the percentage of the frame time that green is displayed to achieve the desired white point.
- Blue_Cycle_% represents the percentage of the frame time that blue is displayed to achieve the desired white point.

For example, assume that the red, green, and blue color cycle times are 30%, 50%, and 20% respectively (to achieve the desired white point), then the landed duty cycle for various combinations of red, green, blue color intensities are shown in 表 6-2 and 表 6-3.

表 6-2. Example Landed Duty Cycle for Full-Color, Color Percentage

| CYCLE PERCENTAGE | | |
|------------------|-------|------|
| RED | GREEN | BLUE |
| 30% | 50% | 20% |

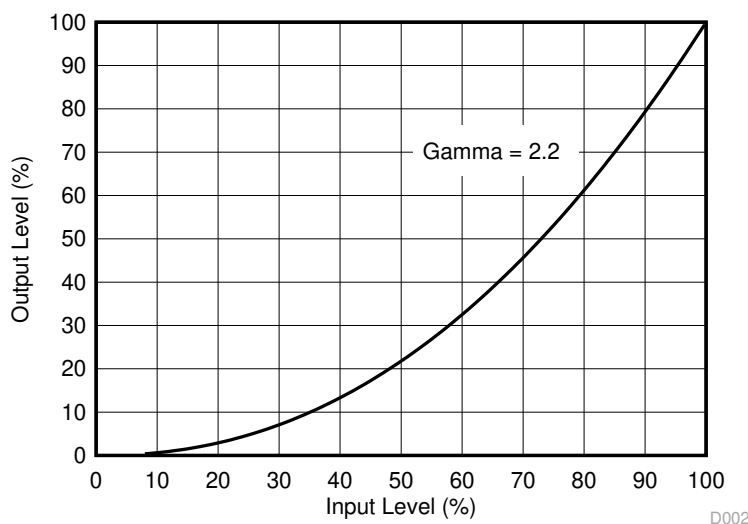
表 6-3. Example Landed Duty Cycle for Full-Color

| SCALE VALUE | | | LANDED DUTY CYCLE |
|-------------|-------|------|-------------------|
| RED | GREEN | BLUE | |
| 0% | 0% | 0% | 0/100 |
| 100% | 0% | 0% | 30/70 |
| 0% | 100% | 0% | 50/50 |
| 0% | 0% | 100% | 20/80 |
| 0% | 12% | 0% | 6/94 |
| 0% | 0% | 35% | 7/93 |
| 60% | 0% | 0% | 18/82 |
| 0% | 100% | 100% | 70/30 |
| 100% | 0% | 100% | 50/50 |
| 100% | 100% | 0% | 80/20 |
| 0% | 12% | 35% | 13/87 |
| 60% | 0% | 35% | 25/75 |
| 60% | 12% | 0% | 24/76 |
| 100% | 100% | 100% | 100/0 |

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the DLPC4430 ディスプレイ コントローラ, the gamma function affects the landed duty cycle.

Gamma is a power function of the form $\text{Output_Level} = A \times \text{Input_Level}^{\text{Gamma}}$, where A is a scaling factor that is typically set to 1.

In the DLPC4430 ディスプレイ コントローラ, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in 図 6-3.

**図 6-3. Example of Gamma = 2.2**

From 図 6-3, if the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value is 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

Consideration must also be given to any image processing that occurs before the DLPC4430 ディスプレイ コントローラ.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC4430 ディスプレイ コントローラ. Typical applications using the DLP780NE DMD include laserTV, smart projectors, enterprise projectors and digital signage.

DMD power-up and power-down sequencing is strictly controlled by the DLPC4430 ディスプレイ コントローラ through the DLPA300. Refer to [セクション 8.2](#) for power-up and power-down specifications. For reliable operation, the DLP780NE DMD must always be used with DLPC4430 ディスプレイ コントローラ, a [DLPA100](#) PMIC/Motor driver and a DLPA300 Micromirror Driver.

7.2 Typical Application

The DLP780NE DMD combined with DLPC4430 ディスプレイ コントローラ and a power management device provides フル HD resolution for bright, colorful display applications. A typical display system using LED illumination combines the DLP780NE DMD, DLPC4430 ディスプレイ コントローラ, DLPA300 micromirror driver and [DLPA100](#) PMIC and motor driver. [図 7-1](#) shows a system block diagram for this configuration of the DLP 0.78 インチ フル HD chipset and additional system components needed. See [図 7-2](#) for a block diagram showing the system components needed along with the laser phosphor of the DLP 0.78-inch Full HD chipset. The components include DLP780NE DMD, DLPC4430 ディスプレイ コントローラ and [DLPA100](#) PMIC and motor driver and a DLPA300 micromirror driver.

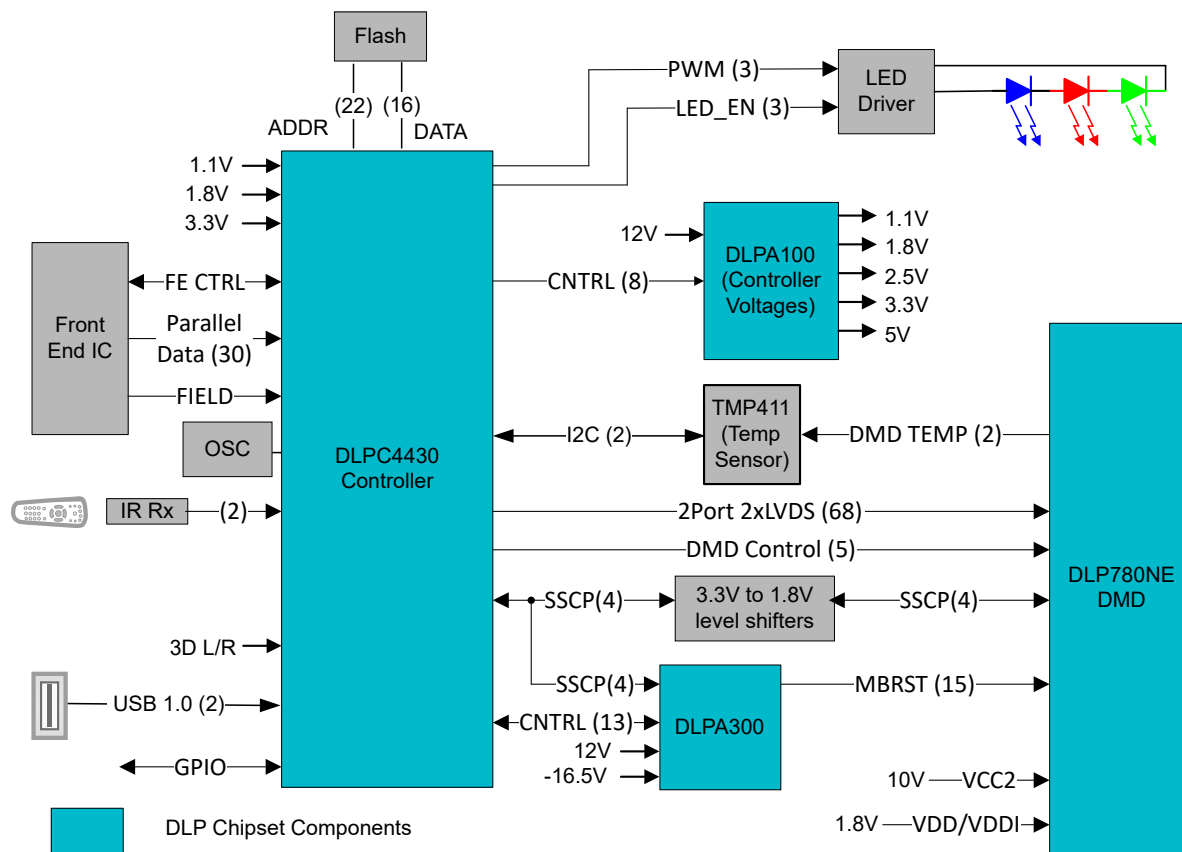


図 7-1. Typical Full HD LED Application

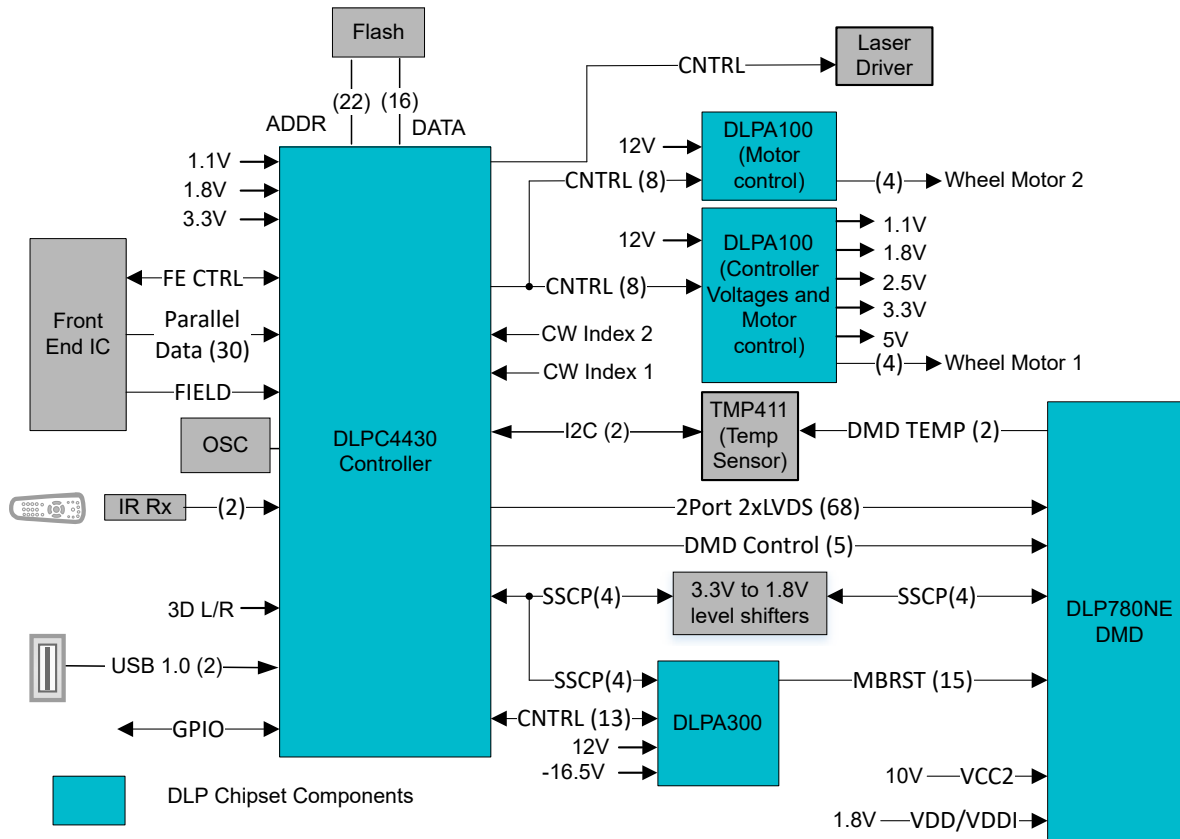


図 7-2. Typical Full HD Laser Phosphor Application

7.2.1 Design Requirements

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The type of illumination used and desired brightness has a major effect on the overall system design and size.

The display system uses the DLP780NE DMD as the core imaging device and contains a 0.78-inch array of micromirrors. The DLPC4430 ディスプレイ コントローラ is the digital interface between the DMD and the rest of the system, taking digital input from front end receiver and driving the DMD over a high-speed LVDS interface. The DLPA100 PMIC serves as a voltage regulator for the controller, and color filter wheel and phosphor wheel motor control. The DLPA300 provides the DMD reset control.

7.2.2 Detailed Design Procedure

For a complete DLP system, an optical module or light engine is required that contains the DLP780NE DMD, associated illumination sources, optical elements, and necessary mechanical components.

For reliable operation, the DMD must always be used with DLPC4430 ディスプレイ コントローラ, the DLPA300 micromirror driver and the DLPA100 PMIC and motor driver.

7.2.3 Application Curves

In a typical projector application, the luminous flux on the screen from the DMD depends on the optical design of the projector. The efficiency and total power of the illumination optical system and the projection optical system determines the overall light output of the projector. The DMD is inherently a linear spatial light modulator, so its efficiency just scales the light output. 図 7-3 describes the relationship of laser input optical power to light output for a laser-phosphor illumination system, where the phosphor is not at its thermal quenching limit.

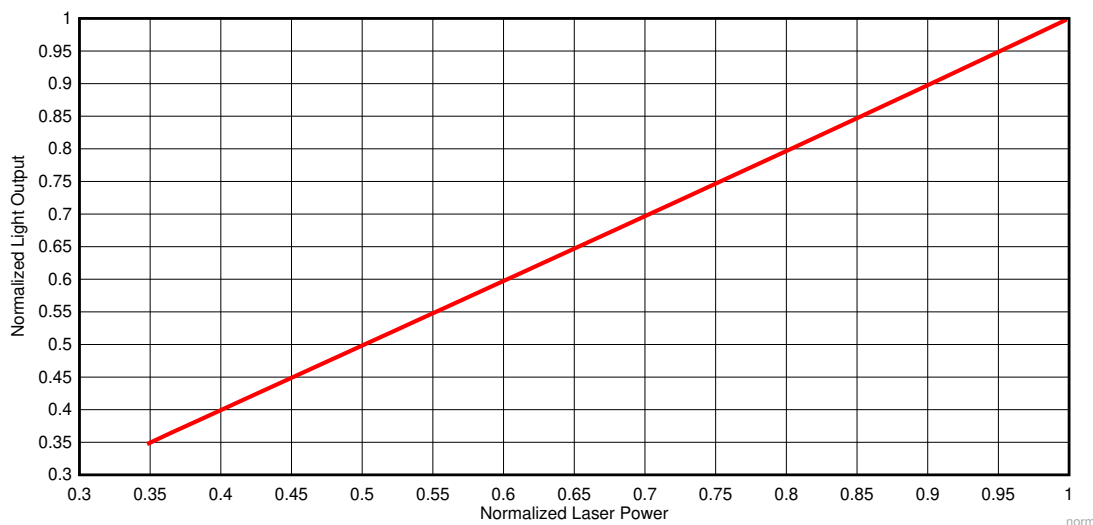
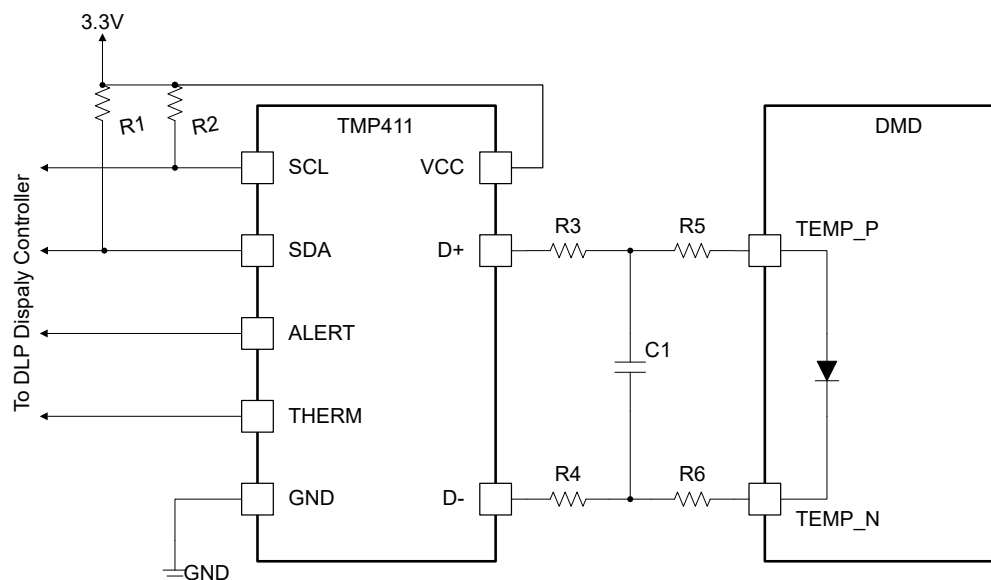


図 7-3. Normalized Light Output vs. Normalized Laser Power for Laser Phosphor Illumination

7.3 Temperature Sensor Diode

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The thermal diode can be interfaced with the TMP411 temperature sensor as shown in 図 7-4. The software application contains functions to configure the TMP411 to read the DLP780NE DMD temperature sensor diode. This data can be leveraged by the customer to incorporate additional functionality in the overall system design such as adjusting illumination, fan speeds, etc. All communication between the TMP411 and the DLPC4430 ディスプレイ コントローラ happens over the I²C interface. The TMP411 connects to the DMD through pins outlined in セクション 4.

Leave TEMP_N and TEMP_P pins unconnected (NC) if the temp sensor is not used.



- A. Details omitted for clarity.
- B. See the [TMP411](#) datasheet for system board layout recommendation.
- C. See the [TMP411](#) datasheet and the TI reference design for suggested component values for R1, R2, R3, R4, and C1.
- D. R5 = 0Ω. R6 = 0Ω. Place 0-Ω resistors close to the DMD package pins.

図 7-4. TMP411 Sample Schematic

8 Power Supply Recommendations

8.1 DMD Power Supply Requirements

The following power supplies are all required to operate the DMD: VDD, VDDI, and VCC2. VSS must also be connected. DMD power-up and power-down sequencing is strictly controlled by the DLPC4430 ディスプレイ コントローラ.

注意

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. VDD, VDDI and VCC2 power supplies have to be coordinated during power-up and power-down operations. VSS must also be connected. Failure to meet any of the below requirements results in a significant reduction in the reliability and lifetime of the DMD. Refer to [図 8-1](#).

8.2 DMD Power Supply Power-Up Procedure

- During power-up, VDD and VDDI must always start and settle before VCC2 is applied to the DMD.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed in [セクション 5.1](#) and in [セクション 5.4](#).
- During power-up, LVCMOS input pins must not be driven high until after VDD and VDDI have settled at operating voltages listed in [セクション 5.4](#) table.

8.3 DMD Power Supply Power-Down Procedure

- During power-down, VDD and VDDI must be supplied until after VCC2 is discharged to within the specified limit of ground. Refer to [セクション 5.4](#).
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed in [セクション 5.1](#) and in [セクション 5.4](#).
- During power-down, LVCMOS input pins must be less than specified in [セクション 5.4](#).

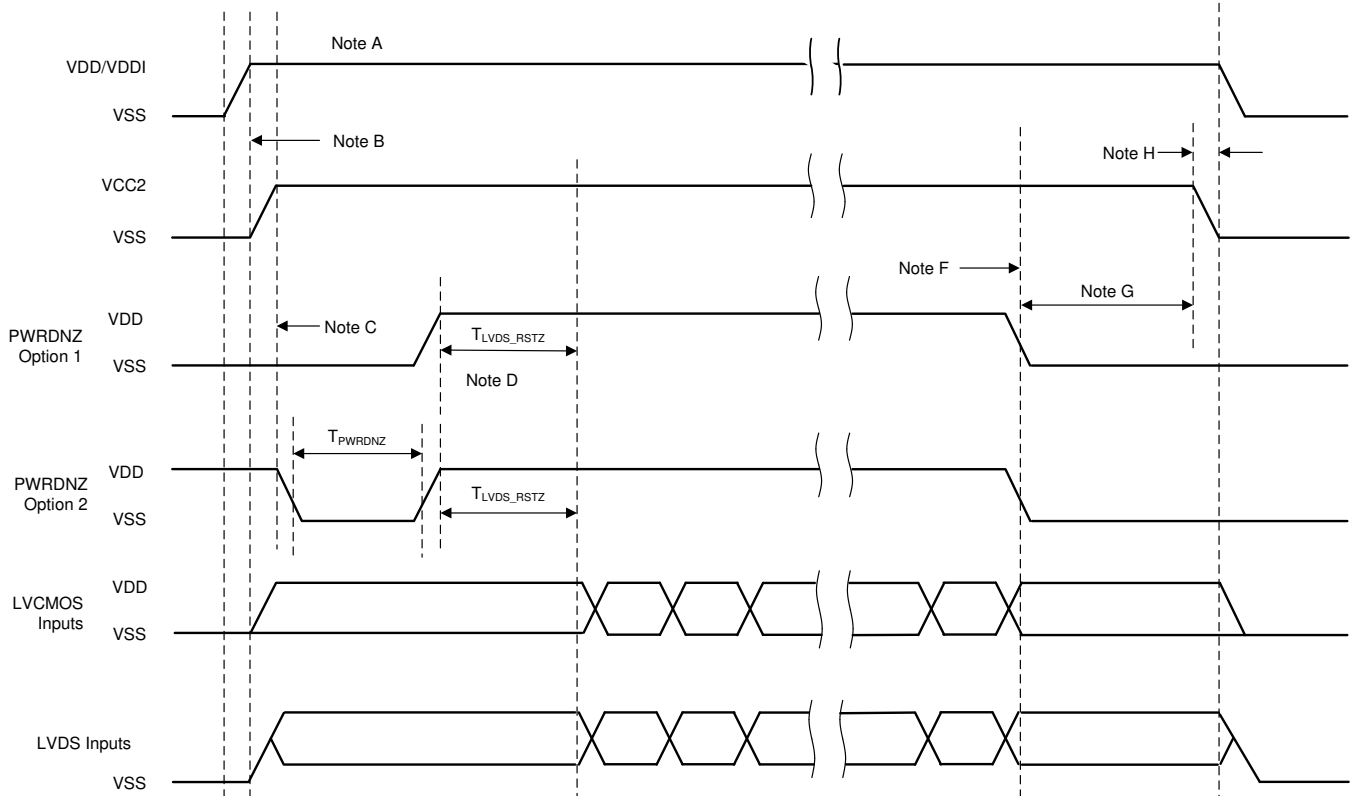


図 8-1. DMD Power Supply Sequencing Requirements

- A. See *Pin Configuration and Functions* for pin functions.
- B. VDD must be up and stable prior to VCC2 powering up.
- C. PWRDNZ has two turn on options. Option 1: PWRDNZ does not go high until VDD and VCC2 are up and stable, or Option 2: PWRDNZ must be pulsed low for a minimum of T_{PWRDNZ} , or 10ns after VDD and VCC2 are up and stable.
- D. There is a minimum of T_{LVDS_ARSTZ} , or 2 μ s, wait time from PWRDNZ going high for the LVDS receiver to recover.
- E. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates the PWRDNZ and disables VCC2.
- F. Under power-loss conditions, where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware, PWRDNZ goes low.
- G. VDD must remain high until after VCC2 goes low.
- H. To prevent excess current, the supply voltage delta $|VDDI - VDD|$ must be less than specified limit in [セクション 5.4](#).

9 Layout

9.1 Layout Guidelines

The DLP780NE DMD is part of a chipset that is controlled by the DLPC4430 ディスプレイ コントローラ in conjunction with the DLP300 micromirror driver and the DLPA100 power and motor driver. These guidelines are targeted at designing a PCB board with the DLP780NE DMD. The DLP780NE DMD board is a high-speed multi-layer PCB, with primarily high-speed digital logic utilizing dual edge clock rates up to 400MHz for DMD LVDS signals. The remaining traces are comprised of low speed digital LVTTTL signals. Solid planes are required for DMD_P1P8V and Ground. The target impedance for the PCB is $50\Omega \pm 10\%$ with the LVDS traces being $100\Omega \pm 10\%$ differential. TI recommends using an 8-layer stack-up as described in 表 9-1.

9.2 Layout Example

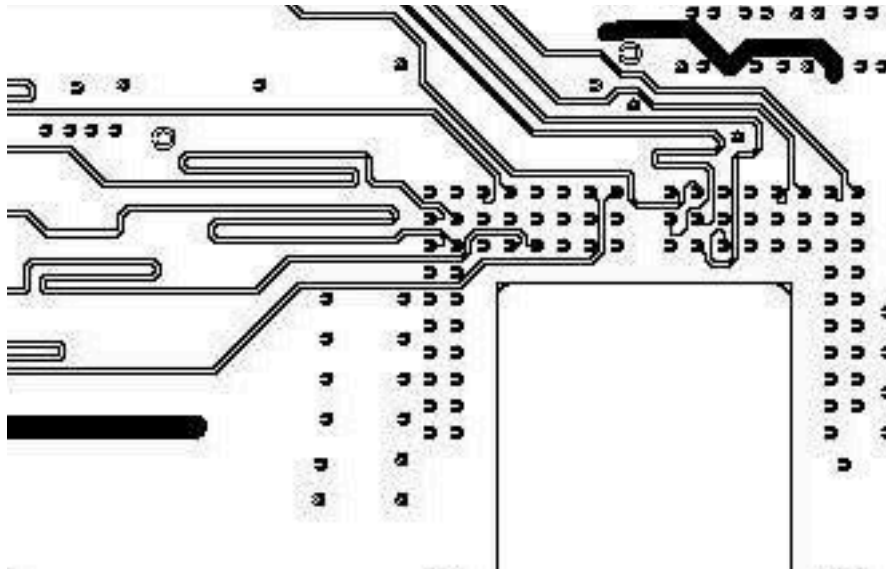


図 9-1. Typical example for matching LVDS signal lengths by serpentine sections

9.2.1 Layers

The layer stack-up and copper weight for each layer is shown in 表 9-1. Small subplanes are allowed on signal routing layers to connect components to major subplanes on top and bottom layers if necessary.

表 9-1. Layer Stack-Up

| LAYER NO. | LAYER NAME | COPPER WT. (oz.) | COMMENTS |
|-----------|-----------------------------|------------------|---|
| 1 | Side A—DMD only | 1.5 | DMD, escapes, low frequency signals, power subplanes |
| 2 | Ground | 1 | Solid ground plane (net GND) |
| 3 | Signal | 0.5 | 50Ω and 100Ω differential signals |
| 4 | Ground | 1 | Solid ground plane (net GND) |
| 5 | VDD and VDDI | 1 | +1.8V power plane |
| 6 | Signal | 0.5 | 50Ω and 100Ω differential signals |
| 7 | Ground | 1 | Solid ground plane (net GND) |
| 8 | Side B—All other Components | 1.5 | Discrete components, low frequency signals, power subplanes |

9.2.2 Impedance Requirements

TI recommends that the board has matched impedance of $50\Omega \pm 10\%$ for all signals. The exceptions are listed in [表 9-2](#).

表 9-2. Special Impedance Requirements

| SIGNAL TYPE | SIGNAL NAME | IMPEDANCE (Ω) |
|-----------------------------------|------------------------|--|
| C channel LVDS differential pairs | DDCP(0:15), DDCN(0:15) | 100 $\pm 10\%$ differential across each pair |
| | DCLKC_P, DCLKC_N | |
| | SCTRL_CP, SCTRL_CN | |
| D channel LVDS differential pairs | DDDP(0:15), DDDN(0:15) | 100 $\pm 10\%$ differential across each pair |
| | DCLKD_P, DCLKD_N | |
| | SCTRL_DP, SCTRL_DN | |

9.2.3 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005"/0.005" design rule. Minimum trace clearance from the ground ring around the PWB has a 0.1" minimum. An analysis of impedance and stack-up requirements determine the actual trace widths and clearances.

9.2.3.1 Voltage Signals

表 9-3. Special Trace Widths, Spacing Requirements

| SIGNAL NAME | MINIMUM TRACE WIDTH TO PINS (MIL) | LAYOUT REQUIREMENT |
|-------------------|-----------------------------------|---|
| GND | 15 | Maximize trace width to connecting pin |
| 3.3-V Supply Rail | 15 | Maximize trace width to connecting pin |
| VDD, VDDI | 15 | Maximize trace width to connecting pin |
| MBRST(0,14) | 15 | Use 10mil etch to connect all signals/voltages from DLPA300 to DLP780NE |
| VCC2 | 15 | Create mini plane from Voltage regulator to DLP780NE |

10 Device and Documentation Support

10.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

10.2 Device Support

10.2.1 Device Nomenclature

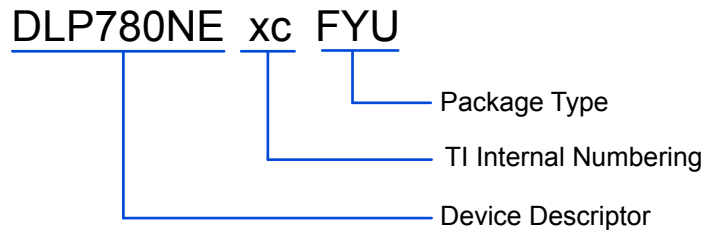


図 10-1. Part Number Description

10.3 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in 図 10-2. The 2-dimensional matrix code is an alpha-numeric string that contains the DMD part number, Part 1 and Part 2 of the serial number.

Example:

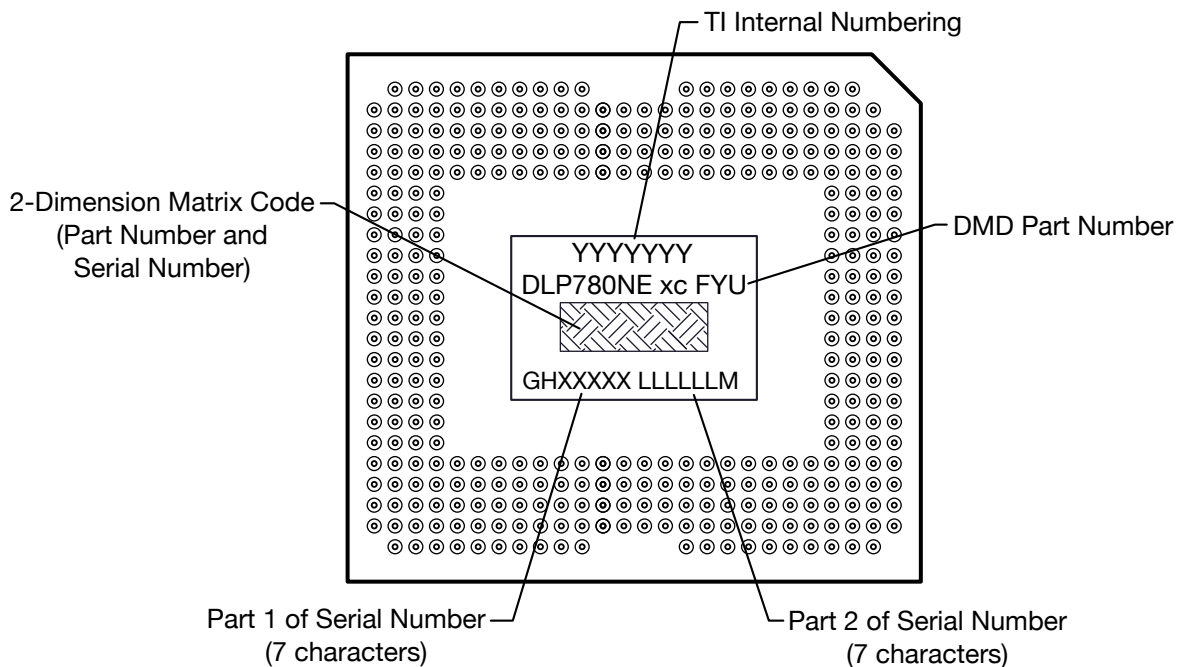


図 10-2. DMD Marking Locations

10.4 Documentation Support

10.4.1 Related Documentation

For related documentation, see the following:

- [DLPC4430 DLP Display Controller Data Sheet](#)
- [DLPA100 Power and Motor Driver Data Sheet](#)
- [DLPA300 DMD Micromirror Driver Data Sheet](#)

10.5 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.6 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

10.7 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

DLP® is a registered trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.8 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.9 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision A (September 2022) to Revision B (March 2024) | Page |
|--|------|
| • Updated ILL _{VIS} , ILL _{BLU} and ILL _{BLU1} in セクション 5.4 | 8 |
| • Added セクション 6.7 Micromirror Power Density Calculation | 25 |
| • Added セクション 6.8 Window Aperture Illumination Overfill Calculation | 27 |

| Changes from Revision * (September 2021) to Revision A (September 2022) | Page |
|--|------|
| • の本体 サイズを訂正 製品情報 | 1 |
| • Updated ILL _{VIS} , added ILL _{BLU} and ILL _{BLU1} in セクション 5.4 | 8 |

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| DLP780NEA0FYU | Active | Production | CPGA (FYU) 350 | 21 JEDEC TRAY (5+1) | Yes | Call TI | N/A for Pkg Type | 0 to 70 | |
| DLP780NEA0FYU.A | Active | Production | CPGA (FYU) 350 | 21 JEDEC TRAY (5+1) | Yes | Call TI | N/A for Pkg Type | 0 to 70 | |
| DLP780NEA0FYU.B | Active | Production | CPGA (FYU) 350 | 21 JEDEC TRAY (5+1) | - | Call TI | Call TI | 0 to 70 | |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

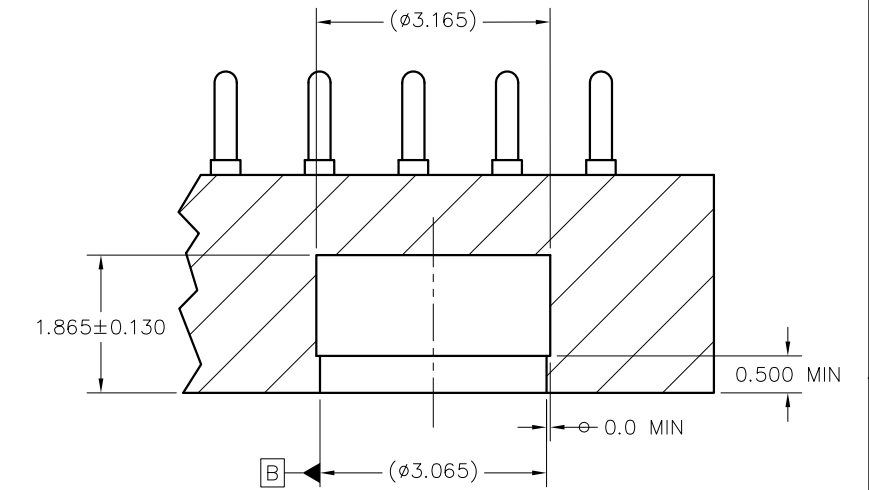
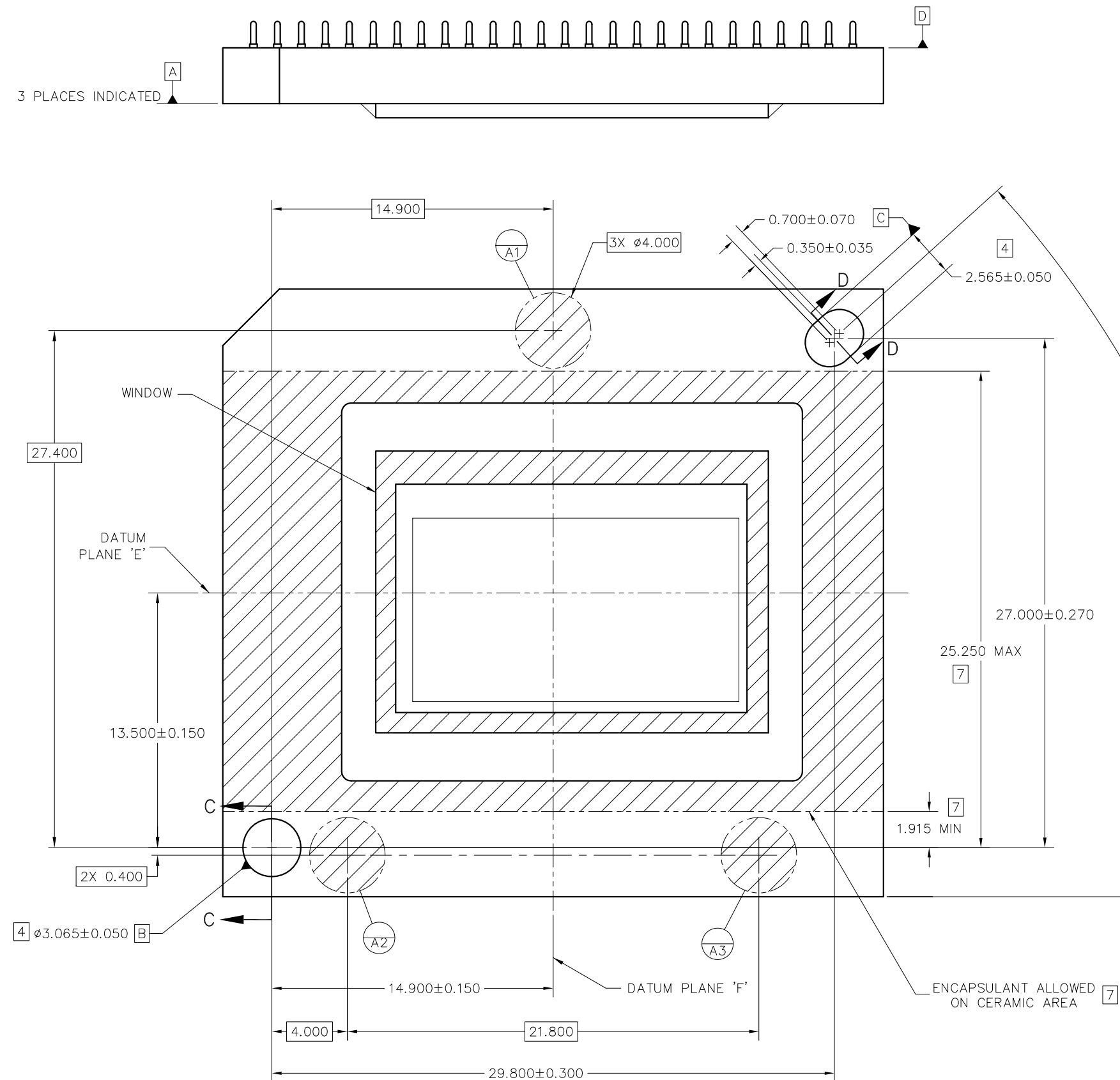
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

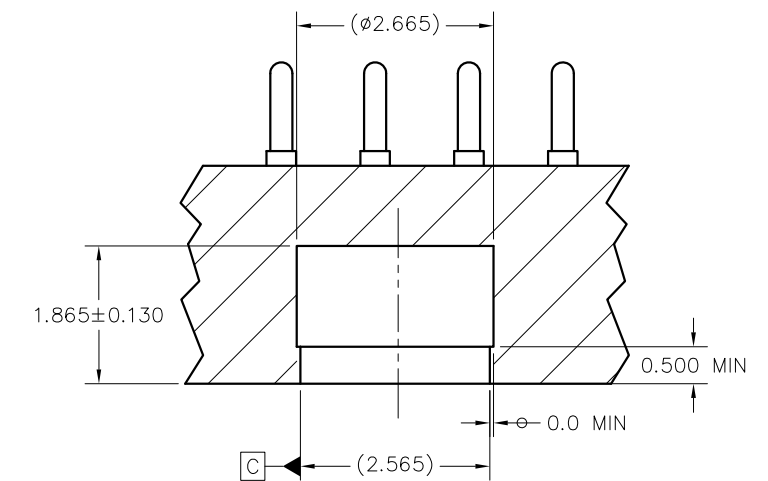
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

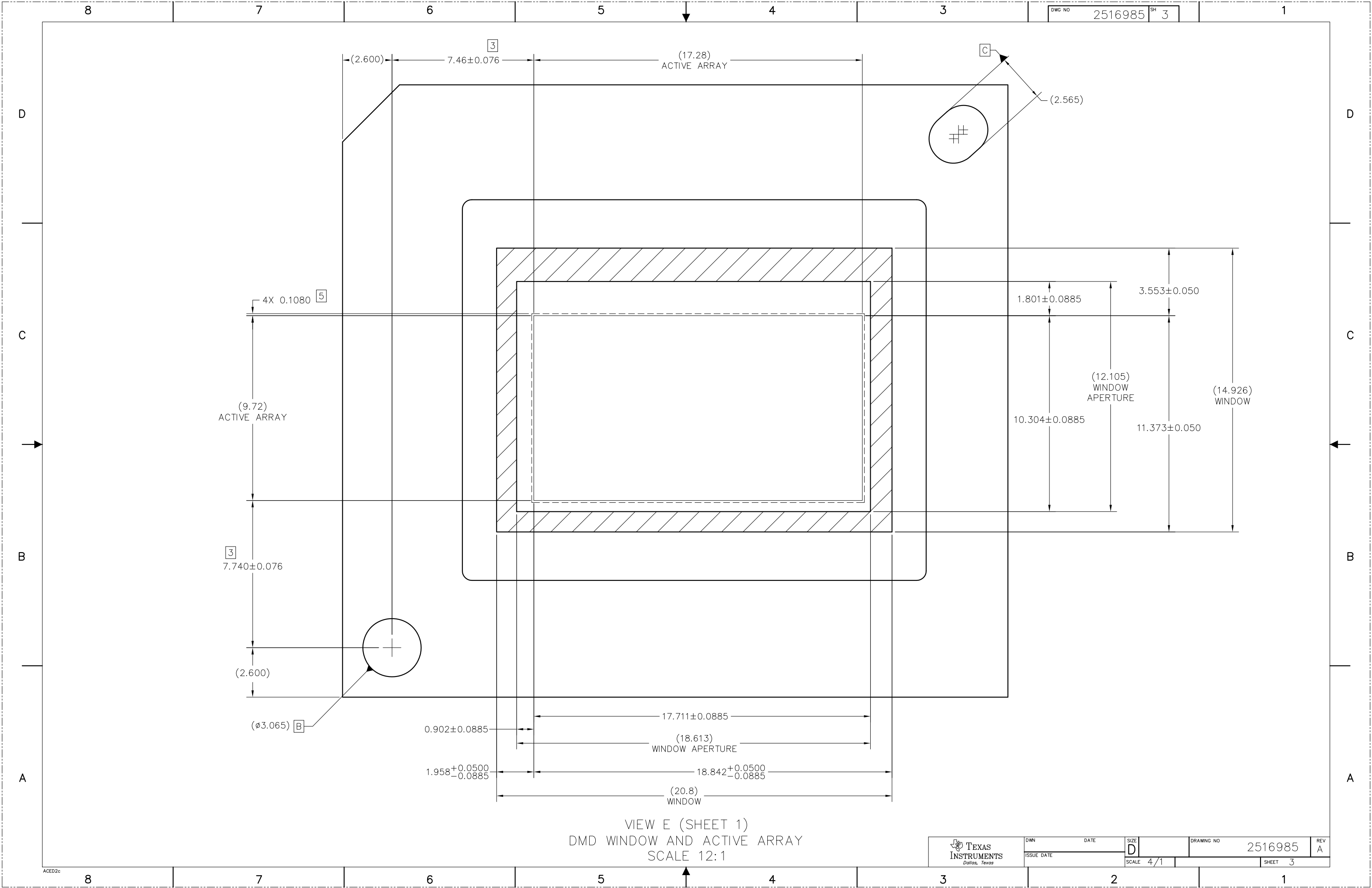


SECTION C-C
DATUM B
SCALE 16/1



SECTION D-D
DATUM C
SCALE 16/1

VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1



VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12:1

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated