DLP7000UV DLP® 0.7 UV XGA 2x LVDS タイプ A DMD

1 特長

- 対角 0.7 インチのマイクロミラー・アレイ
  - 1024 × 768 配列のマイクロメートル・サイズのアルミニウム・ミラー
  - マイクロミラー・ピッチ：13.68µm
  - マイクロミラー傾斜角：±12° (フラット状態に対して)
  - コーナー・イルミネーション (対角照射) 対応
- UV 光 (363～420nm) で使用するよう設計
  - ウィンドウ透過率 98% (シングル・パス、ウィンドウ表面を 2 回通過)
  - マイクロミラーの反射率 88%
  - アレイの回折効率 85%
  - アレイの充填率 92% (公称値)
- 2 つの 16 ビット、低電圧差動信号(LVDS)、ダブル・データ・レート (DDR) 入力データ・バス
- 最高 400MHz の入力データ・クロック速度
- 40.64mm × 31.75mm × 6.0mm のパッケージ・フットプリント
- 気密パッケージ

2 アプリケーション

- 産業用
  - ダイレクト・イメージング・リソグラフィー
  - レーザー・マーキングおよびリペア・システム
  - コンピュータ・トゥ・プレート・プリンタ
  - ラピッド・プロトタイプ・マシン
  - 3D プリンタ
- 医療用
  - 眼科用
  - 光線療法
  - ハイパースペクトル画像処理

3 概要

DLP7000UV は、デジタル制御のマイクロ電気機械システム (MEMS) 空間光変調器 (SLM) です。適切な光学系と組み合わせることで、DLP7000UV を使用して受信光の振幅、方向、位相を変調できます。

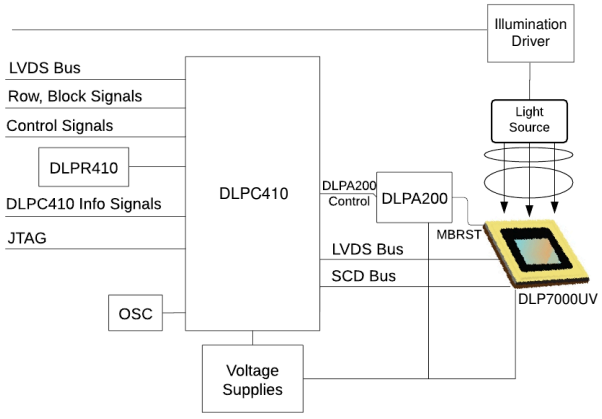
DLP7000UV デジタル・マイクロミラー・デバイス (DMD) は DLP® Discovery™ 4100 プラットフォームの追加製品であり、非常に高速なパターン・レートと、可視スペクトルを超えて UVA スペクトル (363nm～420nm) で動作する高性能空間光変調を実現します。DLP7000UV DMD には、UV の伝達に最適化された特殊な窓が設けられています。また、DLP Discovery 4100 プラットフォームでは、個別のマイクロミラーについて最高レベルの制御を実現でき、オプションとしてランダムな行アドレッシングも使用できます。気密パッケージと相まって、DLP7000UV が備える独自の能力と価値は、広範な産業用、医療用、および高度なディスプレイ・アプリケーションをサポートするのに最適です。

DLP7000UV DMD は気密パッケージとともに、32000Hz (1 ビット・バイナリ) および 1900Hz (8 ビット・グレー) を超える高いパターン速度を達成するための専用 DLPC410 コントローラ、1 つの DLPR410 (DLP Discovery 4100 構成 PROM)、1 つの DLPA200 (DMD マイクロミラー・ドライバ) とともに販売されています。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
DLP7000UV	LCCC (203)	40.64mm × 31.75mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



簡略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (May 2017) to Revision E (May 2017)	Page
• Changed Micromirror switching time typical value from 13 µs to 12.5 µs and removed 22 µs Max value.	20

Changes from Revision C (September 2015) to Revision D (May 2017)	Page
• Updated Pin Configuration and Functions diagram	4
• Changed $T_{GRADIENT}$ from 5 °C to 10 °C to accommodate increase in power density from 400 to 420 nm and added RH symbol for relative humidity in *セクション 7.1*	11
• Clarified $T_{GRADIENT}$ footnote in *セクション 7.1*	11
• Changed T_{stg} to T_{DMD} in *セクション 7.2*	11
• Changed 363 to 420 nm to 363 to 400 nm max for 2.5 W/cm^2 power density and 3.7 W max optical power in *セクション 7.4*	12
• Added 400 to 420 nm max power density of 11 W/cm^2 and max optical power of 16.2 W in *セクション 7.4*	12
• Added 363 to 420 nm total integrated max power density of 11 W/cm^2 and total integrated max optical power of 16.2 W in *セクション 7.4*	12
• Changed $T_{GRADIENT}$ from 5 °C to 10 °C to accommodate increase in power density from 400 to 420 nm *セクション 7.4*	12
• Changed Micromirror active border value from 10 to correct value of 6 in *セクション 7.11*	19
• Changed micromirror crossover to mean transition time and renamed previous crossover to micromirror switching time typical micromirror crossover time typo (16 µs to 13 µs) in *セクション 7.12*	20
• Added typical micromirror switching time - 13 µs in *セクション 7.12*	20
• Changed "Micromirror switching time" to "Array switching time" for clarity in *セクション 7.12*	20
• Added clarification to Micromirror switching time at 400 MHz with global reset in *セクション 7.12*	20

- Changed 図 8-11 drawing to current thermal test point numbering convention....34
- Added Related Links table....46

Changes from Revision B (July 2015) to Revision C (September 2015) **Page**

- デバイスのステータスを「製品プレビュー」から「量産データ」へ変更....1
- Added 3.7-W maximum value to illumination power (from 363 nm to 420 nm) in *セクション 7.4* 12
- Updated 図 9-1 38

Changes from Revision A (June 2015) to Revision B () **Page**

- データシート全体をリリース....1
- セクション 3 で、UVA スペクトルの最小値を 365nm から 363nm に訂正 1

Changes from Revision * (May 2015) to Revision A () **Page**

- デバイスの型番を訂正....1

5 概要 (続き)

DLP7000UV の機能と動作の信頼性を確保するには、チップセットの他の部品と組み合わせて使用する必要があります。専用のチップセットにより、開発者は DMD へ簡単にアクセスでき、マイクロミラーを高速に独立して制御できます。

DLP7000UV は、電気的には 1 ビット CMOS メモリ・セルの 2 次元配列から成り、1024 列 × 768 行の格子状に構成されています。この CMOS メモリ・アレイは、2 つの 16 ビット低電圧差動信号 (LVDS) ダブル・データ・レート (DDR) バスを使用して、行単位でアドレス指定します。アドレス指定は、シリアル制御バスを介して処理されます。特定の CMOS メモリ・アクセス・プロトコルは、DLPC410 デジタル・コントローラによって処理されます。

6 Pin Configuration and Functions

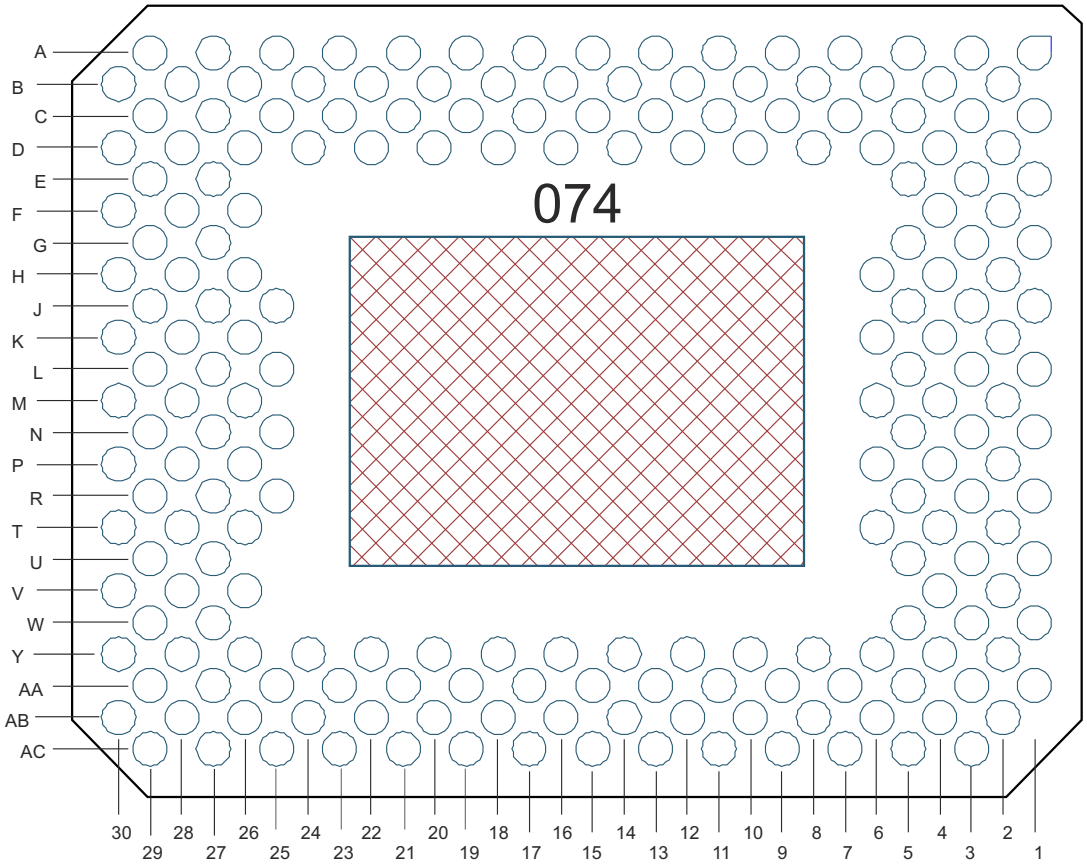


図 6-1. FLP Package 203-Pin LCCC Bottom View

表 6-1. Pin Functions

PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	CLOCK	DESCRIPTION	TRACE (MILS)
NAME	NO.							
DATA INPUT								
D_AN(0)	B10	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		368.72
D_AN(1)	A13	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		424.61
D_AN(2)	D16	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		433.87

表 6-1. Pin Functions (continued)

PIN [1]		TYPE (I/O/P)	SIGNAL	DATA RATE [2]	INTERNAL TERM [3]	CLOCK	DESCRIPTION	TRACE (MILS)
NAME	NO.							
D_AN(3)	C17	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A	Input data bus A (2x LVDS)	391.39
D_AN(4)	B18	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		438.57
D_AN(5)	A17	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		391.13
D_AN(6)	A25	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		563.26
D_AN(7)	D22	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		411.62
D_AN(8)	C29	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		595.11
D_AN(9)	D28	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		543.07
D_AN(10)	E27	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		455.98
D_AN(11)	F26	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		359.5
D_AN(12)	G29	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		542.67
D_AN(13)	H28	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		551.51
D_AN(14)	J27	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		528.04
D_AN(15)	K26	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		484.38
D_AP(0)	B12	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		366.99
D_AP(1)	A11	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		417.47
D_AP(2)	D14	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		434.89
D_AP(3)	C15	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		394.67
D_AP(4)	B16	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		437.3

表 6-1. Pin Functions (continued)

PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	CLOCK	DESCRIPTION	TRACE (MILS)
NAME	NO.							
D_AP(5)	A19	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A	Input data bus A (2x LVDS)	389.01
D_AP(6)	A23	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		562.92
D_AP(7)	D20	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		410.34
D_AP(8)	A29	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		594.61
D_AP(9)	B28	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		539.88
D_AP(10)	C27	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		456.78
D_AP(11)	D26	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		360.68
D_AP(12)	F30	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		543.97
D_AP(13)	H30	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		570.85
D_AP(14)	J29	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		527.18
D_AP(15)	K28	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		481.02
D_BN(0)	AB10	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		368.72
D_BN(1)	AC13	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		424.61
D_BN(2)	Y16	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		433.87
D_BN(3)	AA17	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		391.39
D_BN(4)	AB18	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		438.57
D_BN(5)	AC17	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		391.13
D_BN(6)	AC25	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		563.26

表 6-1. Pin Functions (continued)

PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	CLOCK	DESCRIPTION	TRACE (MILS)
NAME	NO.							
D_BN(7)	Y22	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		411.62
D_BN(8)	AA29	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		595.11
D_BN(9)	Y28	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		543.07
D_BN(10)	W27	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		455.98
D_BN(11)	V26	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		360.94
D_BN(12)	T30	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		575.85
D_BN(13)	R29	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		519.37
D_BN(14)	R27	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		532.59
D_BN(15)	N27	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		441.14
D_BP(0)	AB12	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B	Input data bus B (2x LVDS) Input data bus B (2x LVDS)	366.99
D_BP(1)	AC11	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		417.47
D_BP(2)	Y14	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		434.89
D_BP(3)	AA15	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		394.67
D_BP(4)	AB16	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		437.3
D_BP(5)	AC19	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		389.01
D_BP(6)	AC23	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		562.92
D_BP(7)	Y20	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		410.34
D_BP(8)	AC29	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		594.61

表 6-1. Pin Functions (continued)

PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	CLOCK	DESCRIPTION	TRACE (MILS)
NAME	NO.							
D_BP(9)	AB28	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B	Input data bus B (2x LVDS)	539.88
D_BP(10)	AA27	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		456.78
D_BP(11)	Y26	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		360.68
D_BP(12)	U29	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		578.46
D_BP(13)	T28	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		509.74
D_BP(14)	P28	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		534.59
D_BP(15)	P26	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		440
DATA CLOCK								
DCLK_AN	B22	Input	LVCMOS	–	Differential Terminated - 100 Ω	–		477.10
DCLK_AP	B24	Input	LVCMOS	–	Differential Terminated - 100 Ω	–		477.11
DCLK_BN	AB22	Input	LVCMOS	–	Differential Terminated - 100 Ω	–		477.10
DCLK_BP	AB24	Input	LVCMOS	–	Differential Terminated - 100 Ω	–		477.11
DATA CONTROL INPUTS								
SCTRL_AN	C21	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A	Serial control for data bus A (2x LVDS)	477.07
SCTRL_AP	C23	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_A		477.14
SCTRL_BN	AA21	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B	Serial control for data bus B (2x LVDS)	477.07
SCTRL_BP	AA23	Input	LVCMOS	DDR	Differential Terminated - 100 Ω	DCLK_B		477.14
SERIAL COMMUNICATION AND CONFIGURATION								
SCPCLK	E3	Input	LVCMOS	–	Pull-down	–	Serial port clock	379.29
SCPDO	B2	Output	LVCMOS	–	–	SCPCLK	Serial port output	480.91
SCPDI	F4	Input	LVCMOS	–	Pull-down	SCPCLK	Serial port input	323.56
SCPENZ	D4	Input	LVCMOS	–	Pull-down	SCPCLK	Serial port enable	326.99
PWRDNZ	C3	Input	LVCMOS	–	Pull-down	–	Device Reset	406.28

表 6-1. Pin Functions (continued)

PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	CLOCK	DESCRIPTION	TRACE (MILS)
NAME	NO.							
MODE_A	D8	Input	LVCMOS	–	Pull-down	–	Data bandwidth mode select	396.05
MODE_B	C11	Input	LVCMOS	–	Pull-down	–		208.86
MICROMIRROR BIAS CLOCKING PULSE								
MBRST(0)	P2	Input	Analog	–	–	–	Micromirror Bias Clocking Pulse *MBRST* signals *clock* micromirrors into state of LVCMOS memory cell associated with each mirror.	
MBRST(1)	AB4	Input	Analog	–	–	–		
MBRST(2)	AA7	Input	Analog	–	–	–		
MBRST(3)	N3	Input	Analog	–	–	–		
MBRST(4)	M4	Input	Analog	–	–	–		
MBRST(5)	AB6	Input	Analog	–	–	–		
MBRST(6)	AA5	Input	Analog	–	–	–		
MBRST(7)	L3	Input	Analog	–	–	–		
MBRST(8)	Y6	Input	Analog	–	–	–		
MBRST(9)	K4	Input	Analog	–	–	–		
MBRST(10)	L5	Input	Analog	–	–	–		
MBRST(11)	AC5	Input	Analog	–	–	–		
MBRST(12)	Y8	Input	Analog	–	–	–		
MBRST(13)	J5	Input	Analog	–	–	–		
MBRST(14)	K6	Input	Analog	–	–	–		
MBRST(15)	AC7	Input	Analog	–	–	–		
POWER								
VCC	A7, A15, C1, E1, U1, W1, AB2,AC9, AC15	Power	Analog	–	–	–	Power for LVCMOS Logic	–
VCC1	A21, A27, D30, M30, Y30, AC21, AC27	Power	Analog	–	–	–	Power supply for LVDS Interface	–
VCC2	G1, J1, L1, N1, R1	Power	Analog	–	–	–	Power for High Voltage CMOS Logic	–

表 6-1. Pin Functions (continued)

PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	CLOCK	DESCRIPTION	TRACE (MILS)
NAME	NO.							
VSS	A1, A3, A5, A9, B4, B8, B14, B20, B26, B30, C7, C13, C19, C25, D6, D12, D18, D24, E29, F2, F28, G3, G27, H2, H4, H26, J3, J25 ,K2, K30, L25, L27, L29, M2, M6, M26, M28, N5, N25, N29, P4, P30, R3, R5, R25, T2, T26, U27, V28, V30, W5, W29, Y4, Y12, Y18, Y24, AA3,AA9, AA13, AA19, AA25, AB8, AB14, AB20, AB26, AB30	Power	Analog	–	–	–	Common return for all power inputs	–
RESERVED SIGNALS (NOT FOR USE IN SYSTEM)								
RESERVED_AA1	AA1	Input	LVCMOS	–	Pull-down	–	Pins should be connected to VSS	–
RESERVED_B6	B6	Input	LVCMOS	–	Pull-down	–	–	–
RESERVED_T4	T4	Input	LVCMOS	–	Pull-down	–	–	–
RESERVED_U5	U5	Input	LVCMOS	–	Pull-down	–	–	–
NO_CONNECT	AA11, AC3, C5, C9, D10, D2, E5,G5, H6, P6, T6, U3, V2, V4, W3, Y10, Y2	–	–	–	–	–	DO NOT CONNECT	–

(1) The following power supplies are required to operate the DMD: VCC, VCC1, VCC2. VSS must also be connected.
(2) DDR = Double Data Rate. SDR = Single Data Rate. Refer to the *LVDS Timing Requirements* for specifications and relationships.
(3) Refer to *Electrical Characteristics* for differential termination specification.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
ELECTRICAL					
V_{CC}	Voltage applied to V_{CC} (2) (3)		–0.5	4	V
V_{CCI}	Voltage applied to V_{CCI} (2) (3)		–0.5	4	V
V_{CC2}	Voltage applied to V_{VCC2} (2) (3) (4)		–0.5	8	V
V_{MBRST}	Micromirror clocking pulse waveform voltage applied to MBRST[15:0] Input Pins (supplied by DLPA200)		–28	28	V
$\lvert V_{CC} - V_{CCI} \rvert$	Supply voltage delta (absolute value) (4)			0.3	V
	Voltage applied to all other input pins (2)		–0.5	V_{CC} + 0.3	V
$\lvert V_{ID} \rvert$	Maximum differential voltage, damage can occur to internal termination resistor if exceeded, see LVDS Waveform Requirements			700	mV
I_{OH}	Current required from a high-level output	V_{OH} = 2.4 V		–20	mA
I_{OL}	Current required from a low-level output	V_{OL} = 0.4 V		15	mA
ENVIRONMENTAL					
T_C	Case temperature – operational (5)		20	30	°C
	Case temperature – non-operational (5)		–40	80	°C
$T_{GRADIENT}$	Device temperature gradient – operational (6)			10	°C
RH	Relative humidity (non-condensing)			95	%RH

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS} (ground).
(3) Voltages V_{CC}, V_{CCI}, and V_{CC2} are required for proper DMD operation.
(4) Exceeding the recommended allowable absolute voltage difference between V_{CC} and V_{CCI} may result in excess current draw. The difference between V_{CC} and V_{CCI}, $\lvert V_{CC} - V_{CCI} \rvert$, should be less than the specified limit.
(5) DMD Temperature is the worst-case of any test point shown in *Case Temperature*, or the active array as calculated by the *Micromirror Array Temperature Calculation*.
(6) As either measured, predicted, or both between any two points -- measured on the exterior of the package, or as predicted at any point inside the micromirror array cavity. Refer to *Case Temperature* and *Micromirror Array Temperature Calculation*.

7.2 Storage Conditions

are applicable before the DMD is installed in the final product.

		MIN	MAX	UNIT
T_{DMD}	Storage temperature	–40	80	°C
RH	Relative humidity (non-condensing)		95	%RH

7.3 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	All pins except MBRST[0:15]	±2000	V
			MBRST[0:15] pins	<250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	NOM	MAX	UNIT
ELECTRICAL						
V_{CC}	Supply voltage for LVCMOS core logic (2) (3)		3.0	3.3	3.6	V
V_{CCI}	Supply voltage for LVDS receivers (2) (3)		3.0	3.3	3.6	V
V_{CC2}	Mirror electrode and HVCMOS supply voltage (2) (3)		7.25	7.5	7.75	V
V_{MBRST}	Clocking pulse waveform voltage applied to MBRST[15:0] input pins (supplied by DLPA200)		–27		26.5	V
$\lvert V_{CC} - V_{CCI} \rvert$	Supply voltage delta (absolute value) (3)				0.3	V
ENVIRONMENTAL						
	Illumination power density (4) (13)	< 363 nm (12)			2	mW/cm^2
		363 to 400 nm (11)			2.5	W/cm^2
					3.7	W
		400 to 420 nm (11)			11	W/cm^2
					16.2	W
		363 to 420 nm total (10) (11)			11	W/cm^2
					16.2	W
		> 420 nm		Thermally limited (11)		W/cm^2
T_C	Case/array temperature (8) (9)		20		30 (7)	°C
$T_{GRADIENT}$	Device temperature gradient – operational (6)				10	°C
RH	Relative humidity (non-condensing)				95	%RH
	Operating landed duty cycle (5)			25%		

(1) The functional performance of the device specified in this datasheet is achieved when operating the device within the limits defined by the *Recommended Operating Conditions*. No level of performance is implied when operating the device above or below the *Recommended Operating Conditions* limits.
(2) All voltages referenced to VSS (ground).
(3) Voltages V_{CC}, V_{CCI}, and V_{CC2}, are required for proper DMD operation.
(4) Various application parameters can affect optimal, long-term performance of the DMD, including illumination spectrum, illumination power density, micromirror landed duty cycle, ambient temperature (both storage and operating), case temperature, and power-on or power-off duty cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle.
(5) Landed duty cycle refers to the percentage of time an individual micromirror spends landed in one state (12° or –12°) versus the other state (–12° or 12°).
(6) As either measured, predicted, or both between any two points -- measured on the exterior of the package, or as predicted at any point inside the micromirror array cavity. Refer to Case Temperature and *セクション 8.6*.
(7) Refer to *セクション 8.6* for thermal test point locations, package thermal resistance, and device temperature calculation.
(8) Temperature is the highest measured value of any test point shown in Figure 17 or the active array as calculated by the *セクション 8.6*.
(9) In some applications, the total DMD heat load can be dominated by the amount of incident light energy absorbed. Refer to *セクション 8.6* for further details.
(10) The total integrated illumination power density from 363 to 420 nm shall not exceed 11 W/cm^2 (or 16.2 W evenly distributed on the active array area). Therefore if 2.5 W/cm^2 of illumination is used in the 363 to 400 nm range, then illumination in the 400 to 420 nm range must be limited to 8.5 W/cm^2.
(11) Also limited by the resulting micromirror array temperature. Refer to *セクション 8.6.2* and *セクション 8.6* for information related to calculating the micromirror array temperature.
(12) The maximum operating conditions for operating temperature and illumination power density for wavelengths < 363 nm should not be implemented simultaneously.
(13) Total integrated illumination power density, above or below the indicated wavelength threshold or in the indicated wavelength range.

7.5 Thermal Information

THERMAL METRIC (1) (2)	DLP7000UV FLP (LCCC) 203 PINS	UNIT
Active micromirror array resistance to TP1	0.9	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the temperature range specified in the セクション 7.4. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.6 Electrical Characteristics

over the range of recommended supply voltage and recommended case operating temperature (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage (1), See 図 8-4	V_{CC} = 3.0 V, I_{OH} = –20 mA	2.4			V
V_{OL}	Low-level output voltage (1), See 図 8-4	V_{CC} = 3.6 V, I_{OH} = 15 mA			0.4	V
V_{MBRST}	Clocking Pulse Waveform applied to MBRST[29:0] Input Pins (supplied by DLPA200)		-27		26.5	V
I_{OZ}	High impedance output current (1)	V_{CC} = 3.6 V			10	µA
I_{OH}	High-level output current(1)	V_{OH} = 2.4 V, V_{CC} ≥ 3 V			–20	mA
		V_{OH} = 1.7 V, V_{CC} ≥ 2.25 V			–15	
I_{OL}	Low-level output current(1)	V_{OL} = 0.4 V, V_{CC} ≥ 3 V			15	mA
		V_{OL} = 0.4 V, V_{CC} ≥ 2.25 V			14	
V_{IH}	High-level input voltage (1)		1.7		VCC + .3	V
V_{IL}	Low-level input voltage (1)		–0.3		0.7	V
I_{IL}	Low-level input current (1)	V_{CC} = 3.6 V, V_I = 0 V			–60	µA
I_{IH}	High-level input current (1)	V_{CC} = 3.6 V, V_I = V_{CC}			200	µA
I_{CC}	Current into V_{CC} pin	V_{CC} = 3.6 V			1475	mA
I_{CCI}	Current into V_{CCI} pin (2)	V_{CCI} = 3.6 V			450	mA
I_{CC2}	Current into V_{CC2} pin	V_{CC2} = 8.75 V			25	mA
P_D	Power dissipation			2.0		W
Z_{IN}	Internal differential impedance		95		105	Ω
Z_{LINE}	Line differential impedance (PWB, Trace)		90	100	110	Ω
C_I	Input capacitance (1)	f = 1 MHz			10	pF
C_O	Output capacitance (1)	f = 1 MHz			10	pF
C_{IM}	Input capacitance for MBRST[0:15] pins	f = 1 MHz	220		270	pF

(1) Applies to LVCMOS pins only.
(2) Exceeding the maximum allowable absolute voltage difference between V_{CC} and V_{CCI} may result in excess current draw. See *セクション 7.1* for details.

7.7 LVDS Timing Requirements

over operating free-air temperature range (unless otherwise noted); see 図 7-1

		MIN	NOM	MAX	UNIT
f_{DCLK_*}	DCLK_* clock frequency {where * = [A, or B]}	200		400	MHz
t_c	Clock cycle - DLCK_*	2.5			ns
t_w	Pulse width - DLCK_*		1.25		ns
t_s	Setup time - D_*[15:0] and SCTRL_* before DCLK_*	0.35			ns
t_h	Hold time, D_*[15:0] and SCTRL_* after DCLK_*	0.35			ns
t_{skew}	Skew between bus A and B	–1.25		1.25	ns

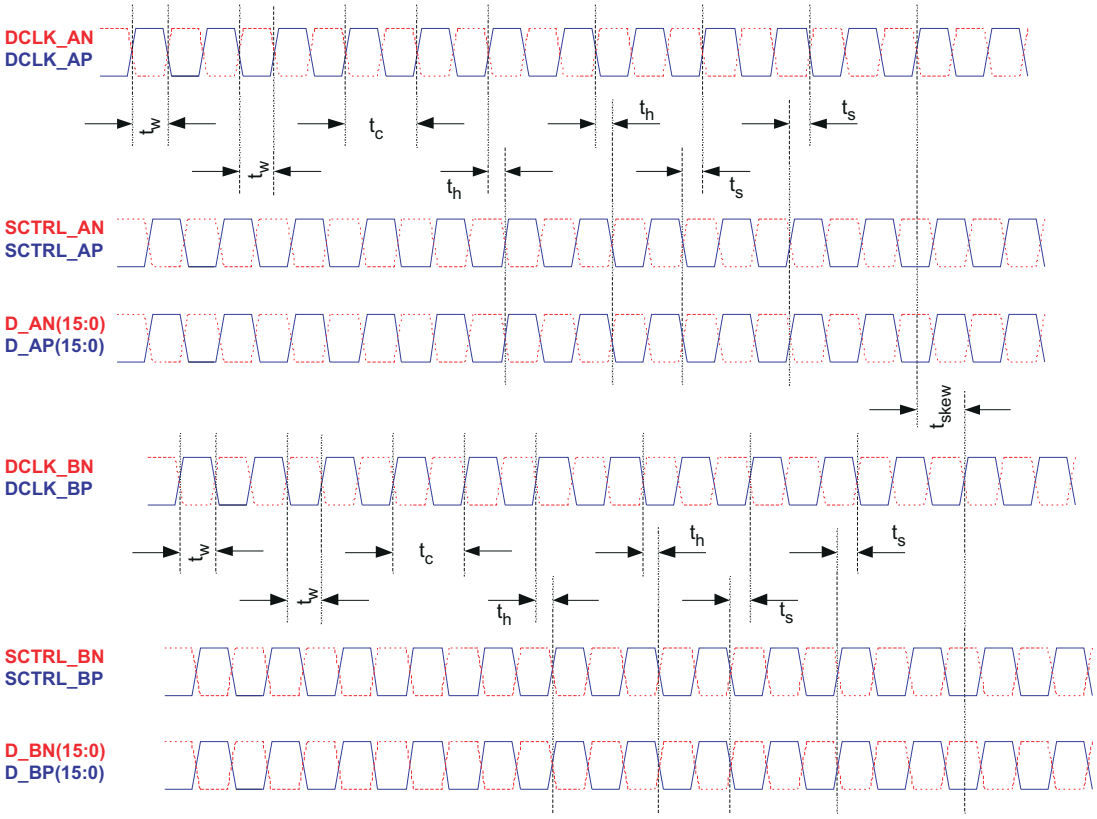


図 7-1. LVDS Timing Waveforms

7.8 LVDS Waveform Requirements

over operating free-air temperature range (unless otherwise noted); see 図 7-2

		MIN	NOM	MAX	UNIT
$\|V_{ID}\|$	Input differential voltage (absolute difference)	100	400	600	mV
V_{CM}	Common mode voltage		1200		mV
V_{LVDS}	LVDS voltage	0		2000	mV
t_r	Rise time (20% to 80%)	100		400	ps
t_r	Fall time (80% to 20%)	100		400	ps

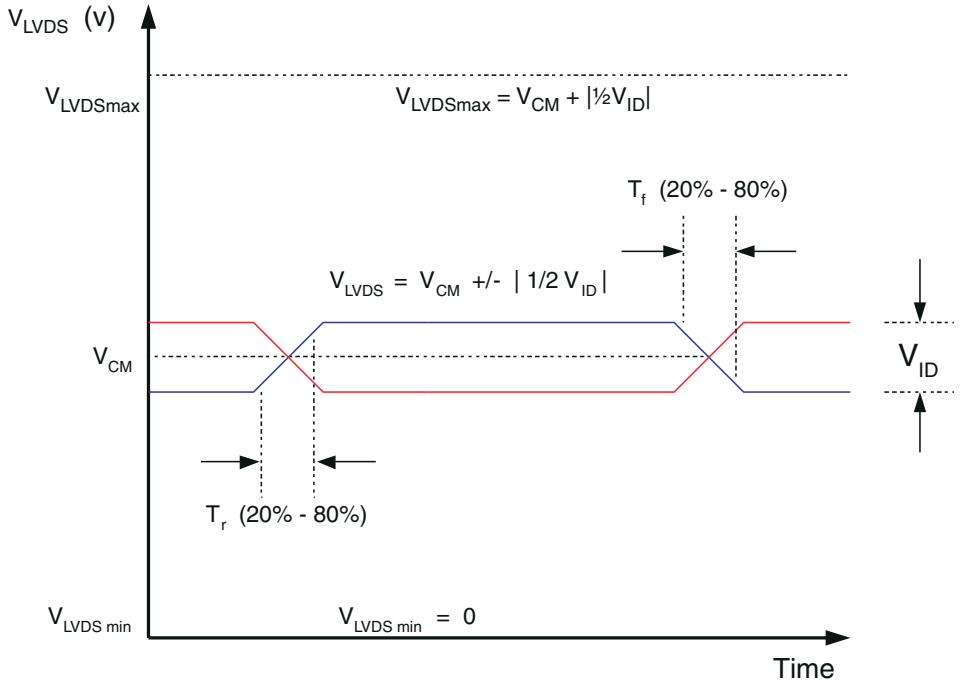


図 7-2. LVDS Waveform Requirements

7.9 Serial Control Bus Timing Requirements

over operating free-air temperature range (unless otherwise noted); see 図 7-3 and 図 7-4

		MIN	NOM	MAX	UNIT
f_{SCP_CLK}	SCP clock frequency	50		500	kHz
t_{SCP_SKEW}	Time between valid SCP_DI and rising edge of SCP_CLK	–300		300	ns
t_{SCP_DELAY}	Time between valid SCP_DO and rising edge of SCP_CLK			960	ns
$t_{\overline{SCP\_EN}}$	Time between falling edge of $\overline{SCP\_EN}$ and the first rising edge of SCP_CLK	30			ns
$t_{\_SCP}$	Rise time for SCP signals			200	ns
t_{f_SCP}	Fall time for SCP signals			200	ns

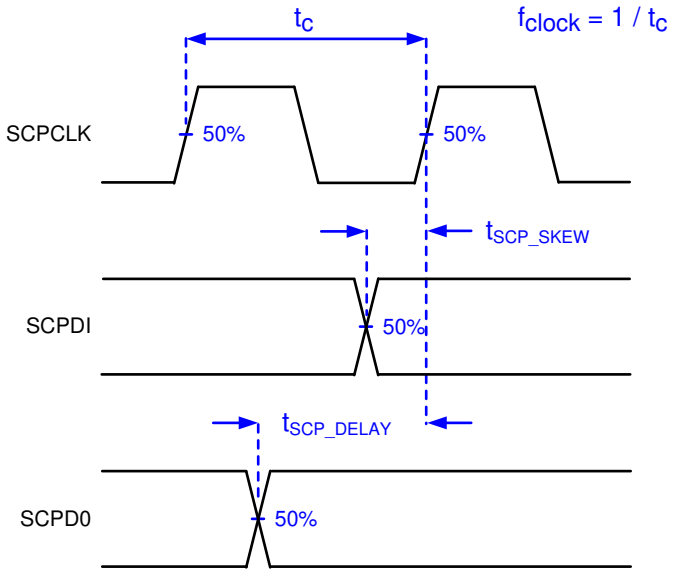


図 7-3. Serial Communications Bus Timing Parameters

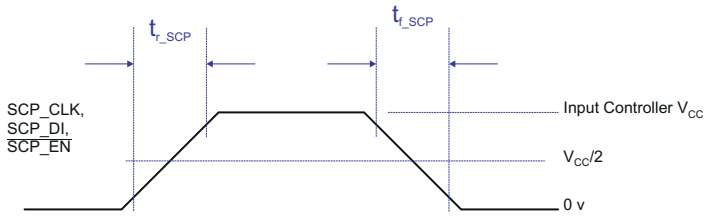


図 7-4. Serial Communications Bus Waveform Requirements

7.10 Systems Mounting Interface Loads

PARAMETER		MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:	Thermal interface area (see 図 7-5)			111	N
	Electrical interface area			423	N
	Datum *A* Interface area (see 図 7-5) (1)			400	N

(1) Combined loads of the thermal and electrical interface areas in excess of Datum *A* load shall be evenly distributed outside the Datum *A* area (423 + 111 – Datum *A*).

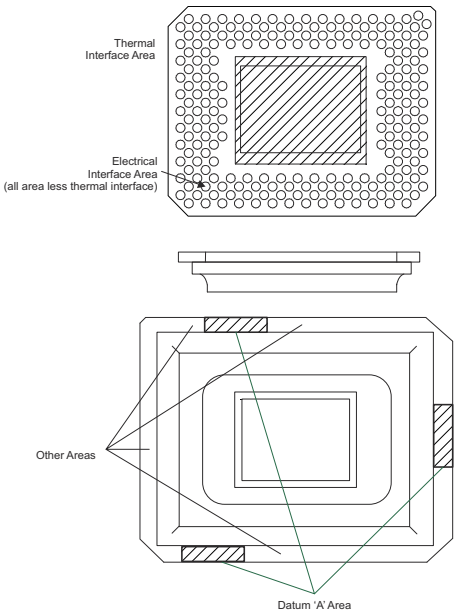
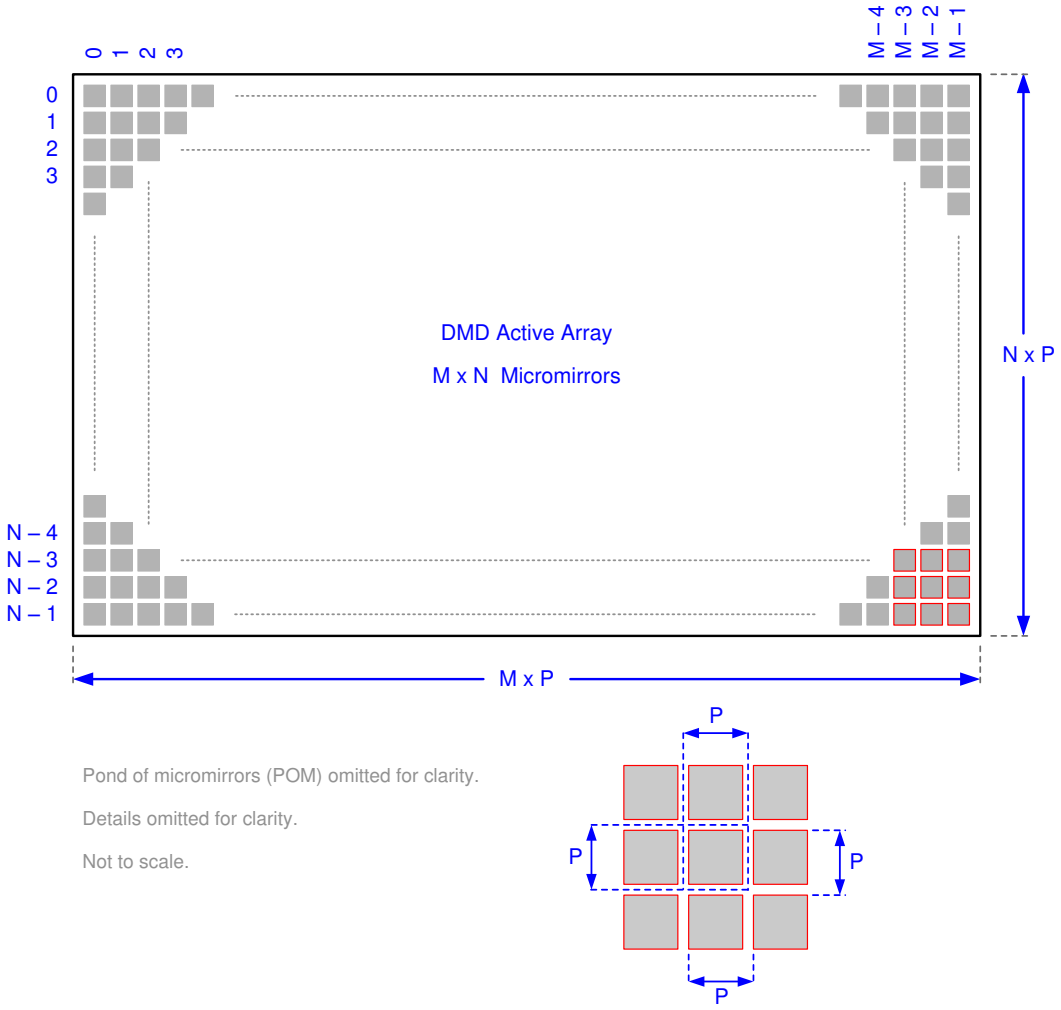


図 7-5. System Interface Loads

7.11 Micromirror Array Physical Characteristics

				VALUE	UNIT
M	Number of active columns		See 図 7-6	1024	micromirrors
N	Number of active rows			768	micromirrors
P	Micromirror (pixel) pitch			13.68	µm
	Micromirror active array width	M × P		14.008	mm
	Micromirror active array height	N × P		10.506	mm
	Micromirror active border	Pond of micromirror (POM) (1)		6	micromirrors/side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.



Refer to *セクション 7.11* for M, N, and P specifications.

図 7-6. Micromirror Array Physical Characteristics

7.12 Micromirror Array Optical Characteristics

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters.

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
a	Micromirror tilt angle	DMD *parked* state (1) (2) (3), See 図 8-6		0		degrees
		DMD *landed* state (1) (4) (5) See 図 8-6		12		
β	Micromirror tilt angle tolerance (1) (4) (6) (7) (8)	See 図 8-6	–1		1	degrees
	Micromirror crossover time (9)			4	22	µs
	Micromirror switching time (10)			12.5		µs
	Array switching time at 400 MHz with global reset (11)		43			µs
	Non operating micromirrors (12)	Non-adjacent micromirrors			10	micromirrors
		Adjacent micromirrors			0	
	Orientation of the micromirror axis-of-rotation (13)	See 図 8-5	44	45	46	degrees
	Micromirror array optical efficiency (14) (15)	363 to 420 nm, with all micromirrors in the ON state		66%		

(1) Measured relative to the plane formed by the overall micromirror array.
(2) *Parking* the micromirror array returns all of the micromirrors to an essentially flat (0°) state (as measured relative to the plane formed by the overall micromirror array).
(3) When the micromirror array is *parked*, the tilt angle of each individual micromirror is uncontrolled.
(4) Additional variation exists between the micromirror array and the package datums, as shown in the *Mechanical, Packaging, and Orderable Information*.
(5) When the micromirror array is *landed*, the tilt angle of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 will result in a micromirror *landing* in an nominal angular position of +12°. A binary value of 0 results in a micromirror *landing* in an nominal angular position of –12°.
(6) Represents the *landed* tilt angle variation relative to the Nominal *landed* tilt angle.
(7) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(8) For some applications, it is critical to account for the micromirror tilt angle variation in the overall System Optical Design. With some System Optical Designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some System Optical Designs, the micromirror tilt angle variation between devices may result in colorimetry variations and/or system contrast variations.
(9) Micromirror crossover time is primarily a function of the natural response time of the micromirrors and is the time it takes for the micromirror to crossover to the other state, but does not include mechanical settling time.
(10) Micromirror switching time is the time before a micromirror may be addressed again. Crossover time plus mechanical settling time.
(11) Array switching is controlled and coordinated by the DLPC410 (DLPS024) and DLPA200 (DLPS015). Nominal Switching time depends on the system implementation and represents the time for the entire micromirror array to be refreshed (array loaded plus reset and mirror settling time).
(12) Non-operating micromirror is defined as a micromirror that is unable to transition nominally from the –12° position to +12° or vice versa.
(13) Measured relative to the package datums *B* and *C*, shown in the *Mechanical, Packaging, and Orderable Information*.
(14) The minimum or maximum DMD optical efficiency observed depends on numerous application-specific design variables, such as:

- Illumination wavelength, bandwidth/line-width, degree of coherence
- Illumination angle, plus angle tolerance
- Illumination and projection aperture size, and location in the system optical path
- Illumination overfill of the DMD micromirror array
- Aberrations present in the illumination source and/or path
- Aberrations present in the projection path

The specified nominal DMD optical efficiency is based on the following use conditions:

- Visible illumination (363 to 420 nm)
- Input illumination optical axis oriented at 24° relative to the window normal
- Projection optical axis oriented at 0° relative to the window normal
- f / 3.0 illumination aperture
- f / 2.4 projection aperture

Based on these use conditions, the nominal DMD optical efficiency results from the following four components:

- Micromirror array fill factor: nominally 92%
- Micromirror array diffraction efficiency: nominally 85%
- Micromirror surface reflectivity: nominally 88%
- Window transmission: nominally 98% for wavelengths 363 nm to 420 nm, applies to all angles 0° to 30° AOI (Angle of Incidence) (single pass, through two surface transitions)

(15) Does not account for the effect of micromirror switching duty cycle, which is application dependent. Micromirror switching duty cycle represents the percentage of time that the micromirror is actually reflecting light from the optical illumination path to the optical projection path. This duty cycle depends on the illumination aperture size, the projection aperture size, and the micromirror array update rate.

7.13 Window Characteristics

PARAMETER (1)	CONDITIONS	MIN	TYP	MAX	UNIT
Window material designation	Corning 7056				
Window refractive index	At wavelength 589 nm		1.487		
Window flatness(2)	Per 25 mm			4	fringes
Window artifact size	Within the Window Aperture (3)			400	µm
Window aperture	See (4)				
Illumination overfill	Refer to *Illumination Overfill*				
Window transmittance, single–pass through both surfaces and glass (5)	Within the wavelength range 363 nm to 420 nm. Applies to all angles 0 to 30 AOI		98%		

(1) See *Window Characteristics and Optics* for more information.
(2) At a wavelength of 632.8 nm.
(3) See the *Mechanical, Packaging, and Orderable Information* section at the end of this document for details regarding the size and location of the window aperture.
(4) For details regarding the size and location of the window aperture, see the package mechanical characteristics listed in the *Mechanical, Packaging, and Orderable Information* section.
(5) See the TI application report *Wavelength Transmittance Considerations for DMD Window*, DLPA031.

7.14 Chipset Component Usage Specification

The DLP7000UV is a component of one or more DLP chipsets. Reliable function and operation of the DLP7000UV requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices for operating or controlling a DLP DMD.

8 Detailed Description

8.1 Overview

Optically, the DLP7000UV consists of 786432 highly reflective, digitally switchable, micrometer-sized mirrors (*micromirrors*), organized in a two-dimensional array of 1024 micromirror columns by 768 micromirror rows (図 8-5). Each aluminum micromirror is approximately 13.68 microns in size (see the *Micromirror Pitch* in 図 8-5), and is switchable between two discrete angular positions: –12° and +12°. The angular positions are measured relative to a 0° *flat state*, which is parallel to the array plane (see 図 8-6). The tilt direction is perpendicular to the hinge-axis which is positioned diagonally relative to the overall array. The *On State* landed position is directed towards *Row 0, Column 0* (upper left) corner of the device package (see the *Micromirror Hinge-Axis Orientation* in 図 8-5). In the field of visual displays, the 1024 by 768 *pixel* resolution is referred to as *XGA*.

Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents, after the micromirror *clocking pulse* is applied. The angular position (–12° or +12°) of the individual micromirrors changes synchronously with a micromirror *clocking pulse*, rather than being synchronous with the CMOS memory cell data update. Therefore, writing a logic 1 into a memory cell followed by a micromirror *clocking pulse* will result in the corresponding micromirror switching to a +12° position. Writing a logic 0 into a memory cell followed by a micromirror *clocking pulse* will result in the corresponding micromirror switching to a –12° position.

Updating the angular position of the micromirror array consists of two steps. First, updating the contents of the CMOS memory. Second, application of a Micromirror Clocking Pulse to all or a portion of the micromirror array (depending upon the configuration of the system). Micromirror Clocking Pulses are generated externally by a DLPA200, with application of the pulses being coordinated by the DLPC410 controller.

Around the perimeter of the 1024 by 768 array of micromirrors is a uniform band of *active border* micromirrors. The pond of micromirror (POM) is not user-addressable. The border micromirrors land in the –12° position once power has been applied to the device. There are 10 border micromirrors on each side of the 1024 by 768 active array.

図 8-1 shows a DLPC410 and DLP7000UV Chipset Block Diagram. The DLPC410 and DLPA200 control and coordinate the data loading and micromirror switching for reliable DLP7000UV operation. The DLPR410 is the programmed PROM required to properly configure the DLPC410 controller. For more information on the chipset components, see *Application and Implementation*. For a typical system application using the DLP Discovery 4100 chipset including the DLP7000UV, see 図 9-2.

8.2 Functional Block Diagram

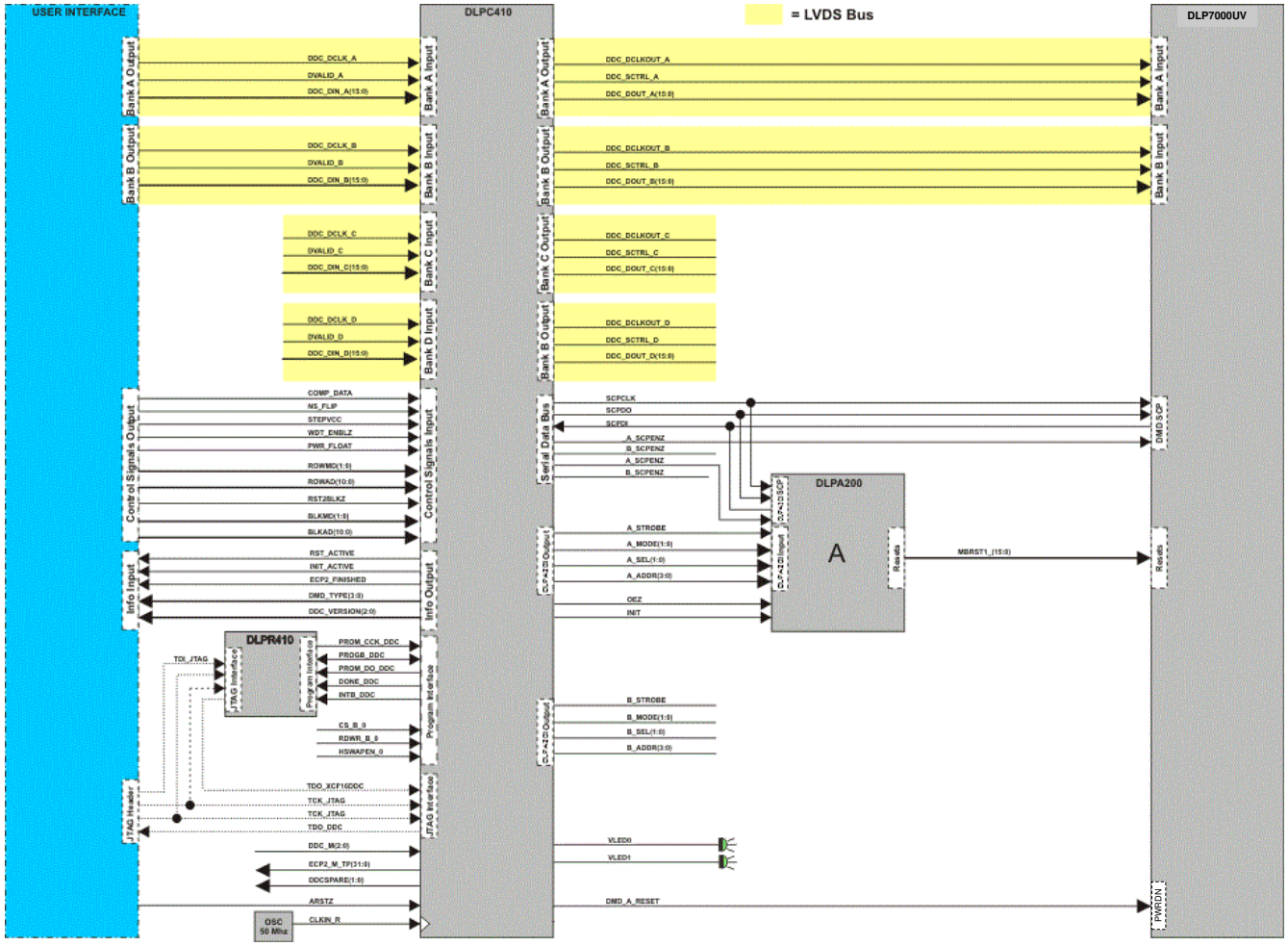


図 8-1. DLPC410 and DLP7000UV Chipset Block Diagram

8.3 Feature Description

表 8-1. DLPC410 DMD Types Overview

DMD	ARRAY	PATTERNS/s	DATA RATE (Gbs)	MIRROR PITCH
DLP7000UV - 0.7” XGA	1024 × 768	32552 (1)	25.6	13.6 µm

(1) This is for single block mode resets.

図 8-1 is a simplified system block diagram showing the use of the following components:

- DLPC410 – Xilinx [XC5VLX30] FPGA configured to provide high-speed DMD data and control, and DLPA200 timing and control
- DLPR410 – [XCF16PFSG48C] serial flash PROM contains startup configuration information (EEPROM)
- DLPA200 – DMD micromirror driver for the DLP7000UV DMD
- DLP7000UV – Spatial Light Modulator (DMD)

8.3.1 DLPC410 - Digital Controller for DLP Discovery 4100 Chipset

The DLP7000UV chipset includes the DLPC410 controller which provides a high-speed LVDS data and control interface for DMD control. This interface is also connected to a second FPGA used to drive applications (not included in the chipset). The DLPC410 generates DMD and DLPA200 initialization and control signals in response to the inputs on the control interface.

For more information, see the DLPC410 data sheet (DLPS024).

8.3.2 DLPA200 DMD Micromirror Driver

DLPA200 micromirror driver provides the micromirror clocking pulse driver functions for the DMD. One DLPA200 is required for DLP7000UV.

For more information on the DLPA200, see the DLPA200 data sheet (DLPS015).

8.3.3 DLPR410 - PROM for DLP Discovery 4100 Chipset

The DLPC410 is configured at startup from the serial flash PROM. The contents of this PROM can not be altered. For more information, see the DLPR410 data sheet (DLPS027) and the DLPC410 data sheet (DLPS024).

8.3.4 DLP7000 - DLP 0.7 XGA 2xLVDS UV Type-A DMD

8.3.4.1 DLP7000UV Chipset Interfaces

This section will describe the interface between the different components included in the chipset. For more information on component interfacing, see *Application and Implementation*.

8.3.4.1.1 DLPC410 Interface Description

8.3.4.1.1.1 DLPC410 IO

表 8-2 describes the inputs and outputs of the DLPC410 to the user. For more details on these signals, see the DLPC410 data sheet.

表 8-2. Input/Output Description

PIN NAME	DESCRIPTION	I/O
$\overline{\text{ARST}}$	Asynchronous active low reset	I
CLKIN_R	Reference clock, 50 MHz	I
DIN_[A,B,C,D](15:0)	LVDS DDR input for data bus A,B,C,D (15:0)	I
DCLKIN[A,B,C,D]	LVDS inputs for data clock (200 - 400 MHz) on bus A, B, C, and D	I
DVALID[A,B,C,D]	LVDS input used to start write sequence for bus A, B, C, and D	I
ROWMD(1:0)	DMD row address and row counter control	I
ROWAD(10:0)	DMD row address pointer	I
BLK_AD(3:0)	DMD mirror block address pointer	I
BLK_MD(1:0)	DMD mirror block reset and clear command modes	I
PWR_FLOAT	Used to float DMD mirrors before complete loss of power	I
DMD_TYPE(3:0)	DMD type in use	O
RST_ACTIVE	Indicates DMD mirror reset in progress	O
INIT_ACTIVE	Initialization in progress	O
VLED0	System *heartbeat* signal	O
VLED1	Denotes initialization complete	O

8.3.4.1.1.2 Initialization

The *INIT_ACTIVE* (表 8-2) signal indicates that the DLP7000UV, DLPA200, and DLPC410 are in an initialization state after power is applied. During this initialization period, the DLPC410 is initializing the DLP7000UV and DLPA200 by setting all internal registers to their correct states. When this signal goes low, the system has completed initialization. System initialization takes approximately 220 ms to complete. Data and command write cycles should not be asserted during the initialization.

During initialization the user must send a training pattern to the DLPC410 on all data and DVALID lines to correctly align the data inputs to the data clock. For more information, see the DLPC410 data sheet – Interface Training Pattern.

8.3.4.1.1.3 DMD Device Detection

The DLPC410 automatically detects the DMD type and device ID. DMD_TYPE (表 8-2) is an output from the DLPC410 that contains the DMD information. Only DMDs sold with the chipset or kit are recognized by the automatic detection function. All other DMDs do not operate with the DLPC410.

8.3.4.1.1.4 Power Down

To ensure long term reliability of the DLP7000UV, a shutdown procedure must be executed. Prior to power removal, assert the PWR_FLOAT (表 8-2) signal and allow approximately 300 µs for the procedure to complete. This procedure assures the mirrors are in a flat state.

8.3.4.2 DLPC410 to DMD Interface

8.3.4.2.1 DLPC410 to DMD IO Description

表 8-3 lists the available controls and status pin names and their corresponding signal type, along with a brief functional description.

表 8-3. DLPC410 to DMD I/O Pin Descriptions

PIN NAME	DESCRIPTION	I/O
DDC_DOUT_[A,B,C,D](15:0)	LVDS DDR output to DMD data bus A, B, C, D (15:0)	O
DDC_DCLKOUT_[A,B,C,D]	LVDS output to DMD data clock A, B, C, D	O
DDC_SCTRL_[A,B,C,D]	LVDS DDR output to DMD data control A, B, C, D	O

8.3.4.2.2 Data Flow

図 8-2 shows the data traffic through the DLPC410. Special considerations are necessary when laying out the DLPC410 to allow best signal flow.

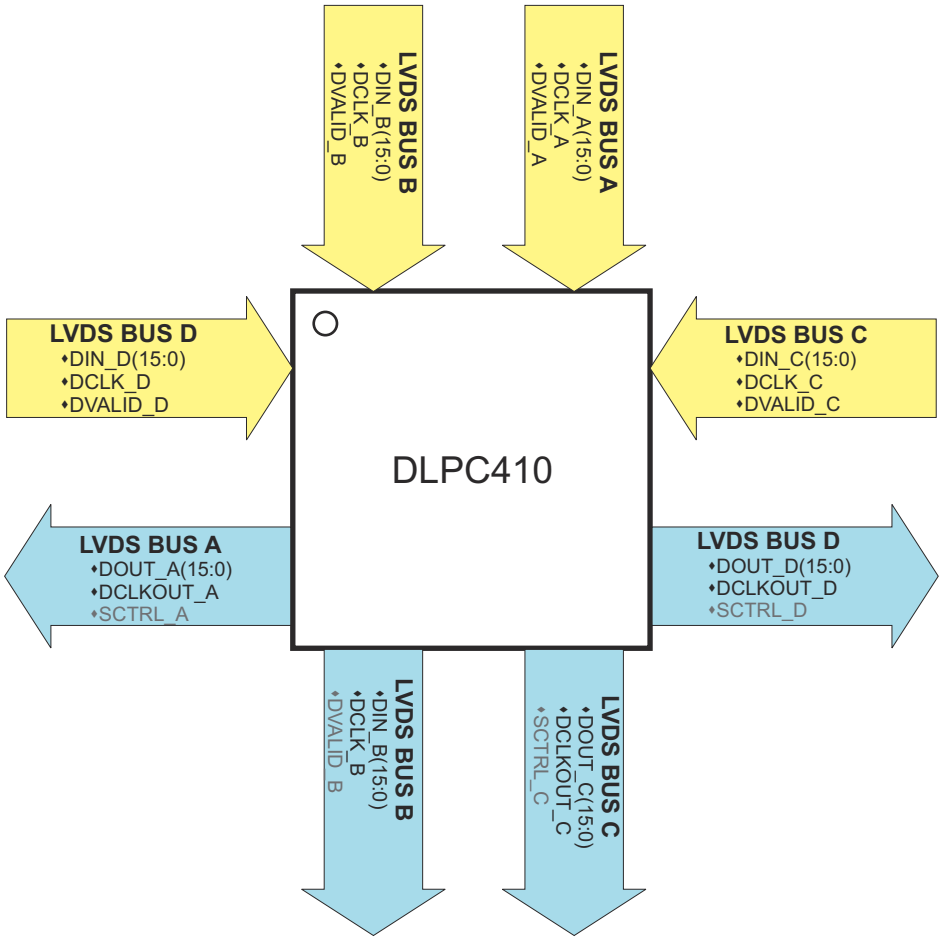


図 8-2. DLPC410 Data Flow

Two LVDS buses transfer the data from the user to the DLPC410. Each bus has its data clock that is input edge aligned with the data (DCLK). Each bus also has its own validation signal that qualifies the data input to the DLPC410 (DVALID).

Output LVDS buses transfer data from the DLPC410 to the DLP7000UV. Output buses LVDS A and LVDS B are used as highlighted in 図 8-2.

8.3.4.3 DLPC410 to DLPA200 Interface

8.3.4.3.1 DLPA200 Operation

The DLPA200 DMD Micromirror Driver is a mixed-signal Application Specific Integrated Circuit (ASIC) that combines the necessary high-voltage power supply generation and Micromirror Clocking Pulse functions for a family of DMDs. The DLPA200 is programmable and controllable to meet all current and anticipated DMD requirements.

The DLPA200 operates from a +12 volt power supply input. For more detailed information on the DLPA200, see the DLPA200 data sheet.

8.3.4.3.2 DLPC410 to DLPA200 IO Description

The Serial Communications Port (SCP) is a full duplex, synchronous, character-oriented (byte) port that allows exchange of commands from the DLPC410 to the DLPA200. One SCP bus is used for the DLP7000UV.

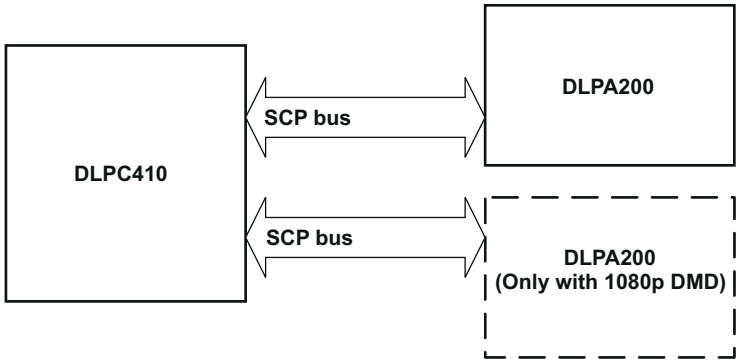


図 8-3. Serial Port System Configuration

There are five signal lines associated with the SCP bus: $\overline{\text{SCPEN}}$, SCPCK, SCPDI, SCPDO, and $\overline{\text{IRQ}}$.

表 8-4 lists the available controls and status pin names and their corresponding signal type, along with a brief functional description.

表 8-4. DLPC410 to DLPA200 I/O Pin Descriptions

PIN NAME	DESCRIPTION	I/O
$\overline{\text{A\_SCPEN}}$	Active low chip select for DLPA200 serial bus	O
A_STROBE	DLPA200 control signal strobe	O
A_MODE(1:0)	DLPA200 mode control	O
A_SEL(1:0)	DLPA200 select control	O
A_ADDR(3:0)	DLPA200 address control	O
$\overline{\text{B\_SCPEN}}$	Active low chip select for DLPA200 serial bus (2)	O
B_STROBE	DLPA200 control signal strobe (2)	O
B_MODE(1:0)	DLPA200 mode control	O
B_SEL(1:0)	DLPA200 select control	O
B_ADDR(3:0)	DLPA200 address control	O

The DLPA200 provides a variety of output options to the DMD by selecting logic control inputs: MODE[1:0], SEL[1:0] and reset group address A[3:0] (表 8-4). The MODE[1:0] input determines whether a single output, two outputs, four outputs, or all outputs, will be selected. Output levels (VBIAS, VOFFSET, or VRESET) are selected by SEL[1:0] pins. Selected outputs are tri-stated on the rising edge of the STROBE signal and latched to the selected voltage level after a break-before-make delay. Outputs will remain latched at the last Micromirror Clocking Pulse waveform level until the next Micromirror Clocking Pulse waveform cycle.

8.3.4.4 DLPA200 to DLP7000UV Interface Overview

The DLPA200 generates three voltages: VBIAS, VRESET, and VOFFSET that are supplied to the DMD MBRST lines in various sequences through the Micromirror Clocking Pulse driver function. VOFFSET is also supplied directly to the DMD as DMDVCC2. A fourth DMD power supply, DMDVCC, is supplied directly to the DMD by regulators.

The function of the Micromirror Clocking Pulse driver is to switch selected outputs in patterns between the three voltage levels (VBIAS, VRESET and VOFFSET) to generate one of several Micromirror Clocking Pulse waveforms. The order of these Micromirror Clocking Pulse waveform events is controlled externally by the logic control inputs and timed by the STROBE signal. DLPC410 automatically detects the DMD type and then uses the DMD type to determine the appropriate Micromirror Clocking Pulse waveform.

A direct Micromirror Clocking Pulse operation causes a mirror to transition directly from one latched state to the next. The address must already be set up on the mirror electrodes when the Micromirror Clocking Pulse is initiated. Where the desired mirror display period does not allow for time to set up the address, a Micromirror Clocking Pulse with release can be performed. This operation allows the mirror to go to a relaxed state regardless of the address while a new address is set up, after which the mirror can be driven to a new latched state.

A mirror in the relaxed state typically reflects light into a system collection aperture and can be thought of as *off* although the light is likely to be more than a mirror latched in the *off* state. System designers should carefully evaluate the impact of relaxed mirror conditions on optical performance.

8.3.5 Measurement Conditions

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. 図 8-4 shows an equivalent test load circuit for the output under test. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving. All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL} MAX and V_{OH} MIN for output clocks.

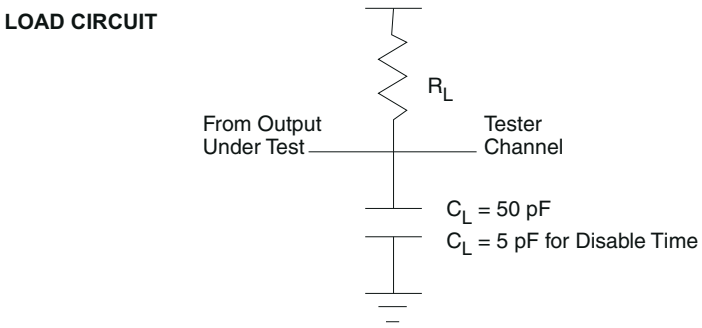


図 8-4. Test Load Circuit for AC Timing Measurements

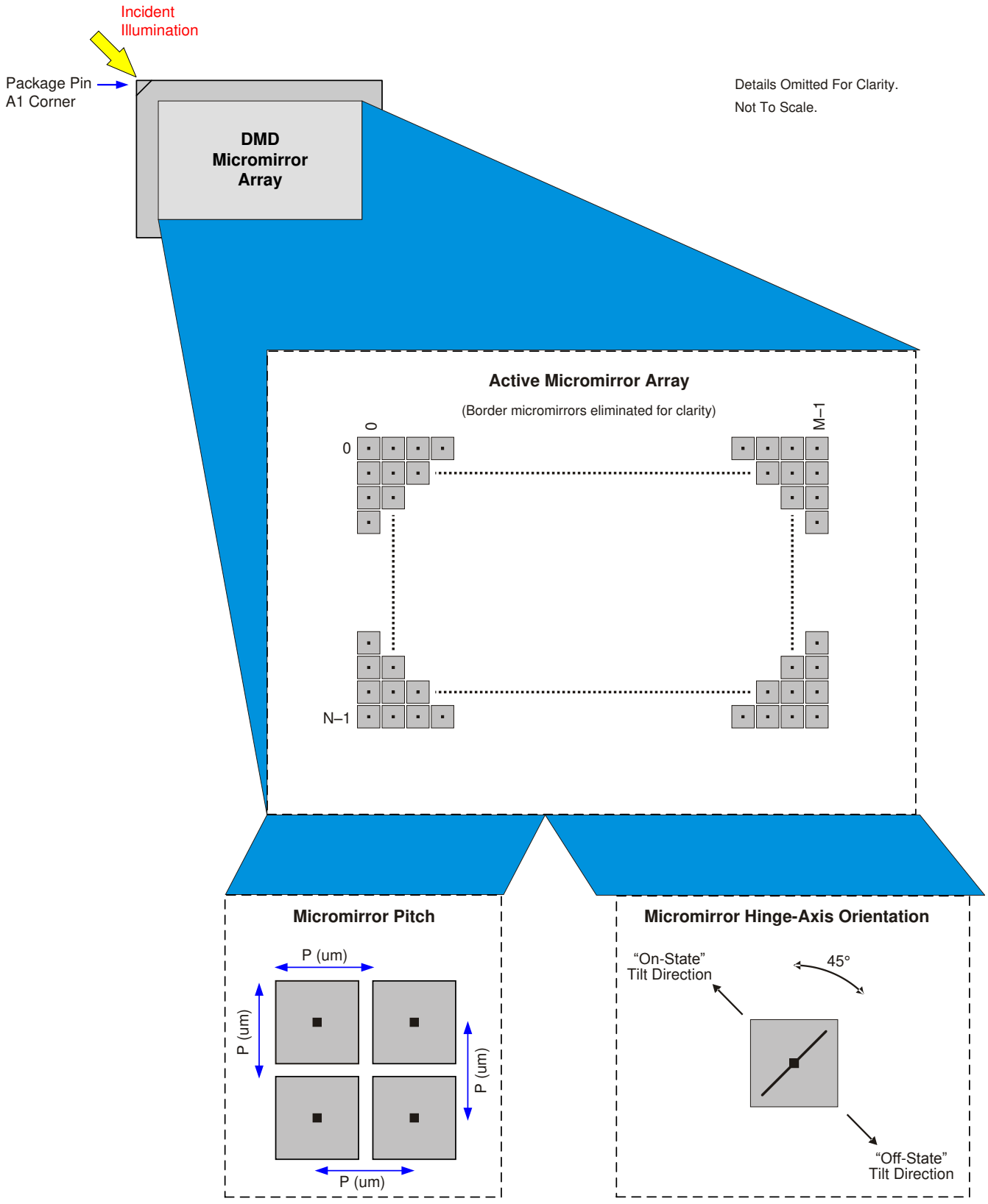


図 8-5. DMD Micromirror Array, Pitch, and Hinge-Axis Orientation

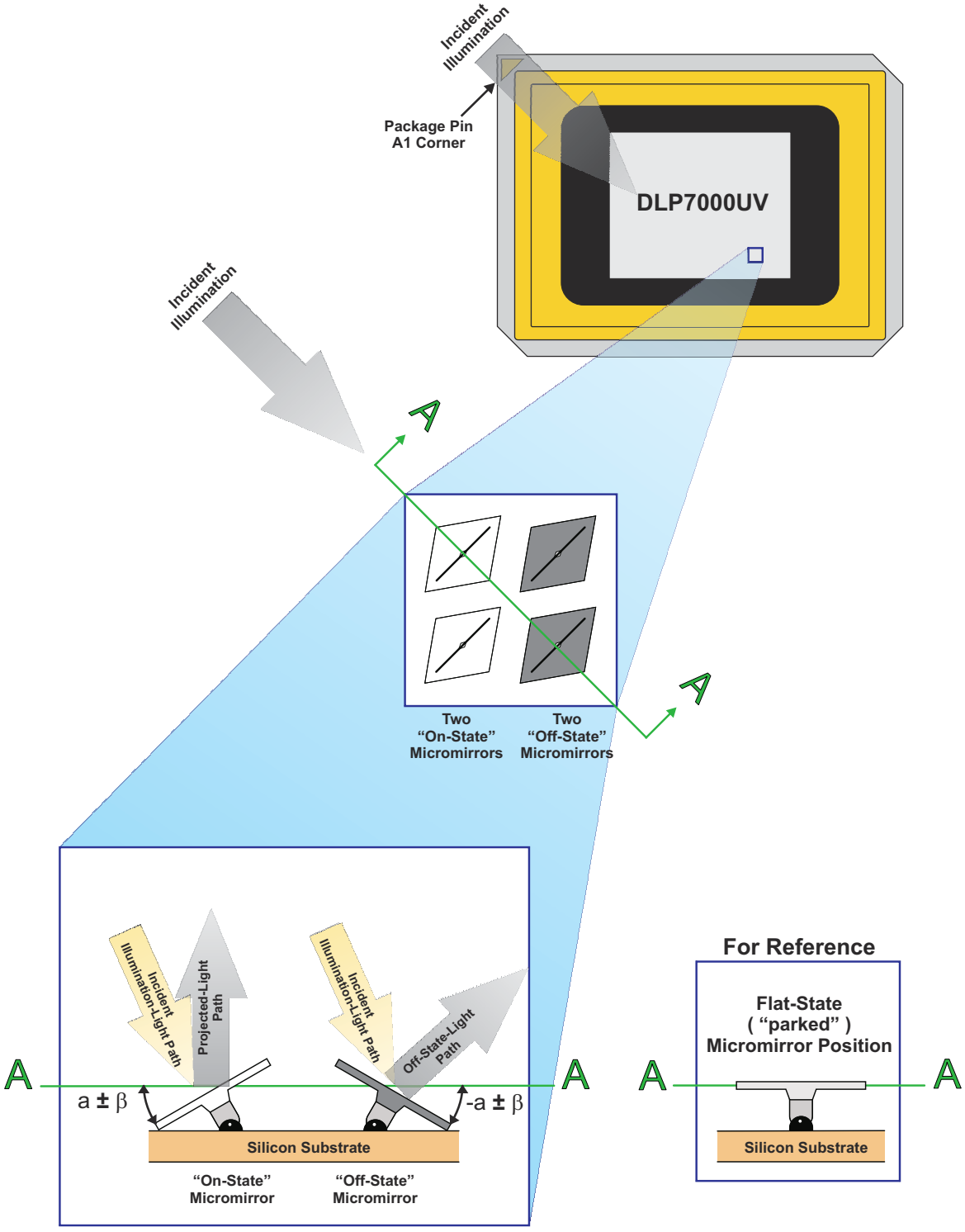


図 8-6. Micromirror Landed Positions and Light Paths

8.4 Device Functional Modes

8.4.1 DMD Operation

The DLP7000UV has only one functional mode, it is set to be highly optimized for low latency and high speed in generating mirror clocking pulses and timings.

When operated with the DLPC410 controller in conjunction with the DLPA200 driver, the DLP7000UV can be operated in several display modes. The DLP7000UV is loaded as 16 blocks of 48 rows each. 図 8-7, 図 8-8, 図 8-9, and 図 8-10 show how the image is loaded by the different Micromirror Clocking Pulse modes.

There are four Micromirror Clocking Pulse modes that determine which blocks are *reset* when a Micromirror Clocking Pulse command is issued:

- Single block mode
- Dual block mode
- Quad block mode
- Global mode

8.4.1.1 Single Block Mode

In single block mode, a single block can be loaded and reset in any order. After a block is loaded, it can be reset to transfer the information to the mechanical state of the mirrors.

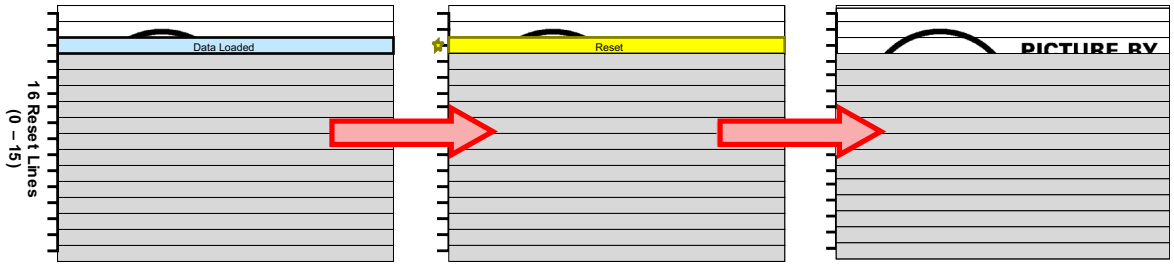


図 8-7. Single Block Mode

8.4.1.2 Dual Block Mode

In dual block mode, reset blocks are paired together as follows (0-1), (2-3), (4-5) . . . (14-15). These pairs can be reset in any order. After data is loaded a pair can be reset to transfer the information to the mechanical state of the mirrors.

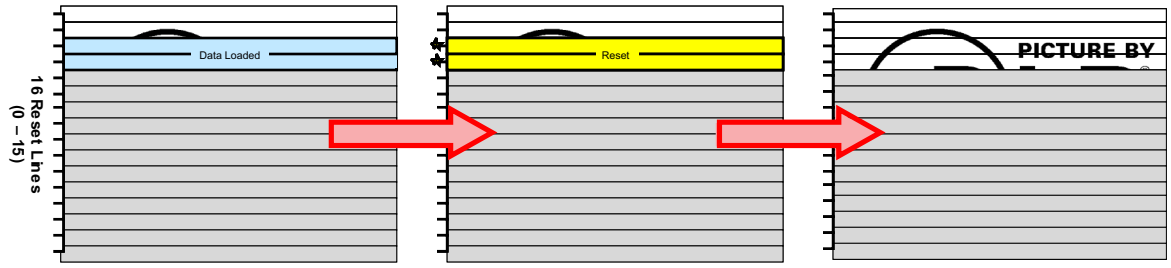


図 8-8. Dual Block Mode

8.4.1.3 Quad Block Mode

In quad block mode, reset blocks are grouped together in fours as follows (0-3), (4-7), (8-11) and (12-15). Each quad group can be randomly addressed and reset. After a quad group is loaded, it can be reset to transfer the information to the mechanical state of the mirrors.

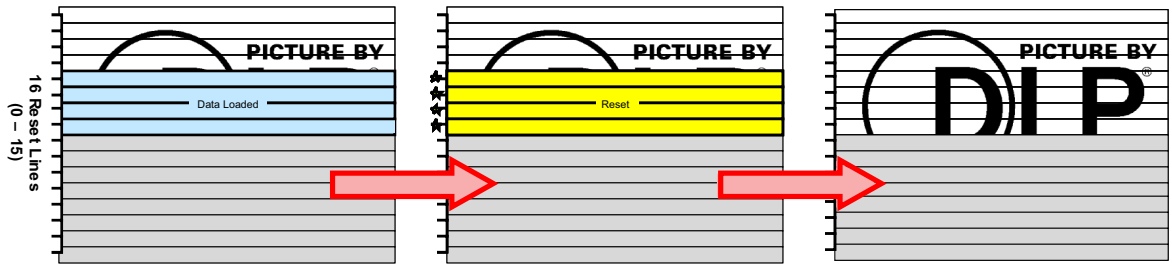


図 8-9. Quad Block Mode

8.4.1.4 Global Mode

In global mode, all reset blocks are grouped into a single group and reset together. The entire DMD must be loaded with the desired data before issuing a Global Reset to transfer the information to the mechanical state of the mirrors.

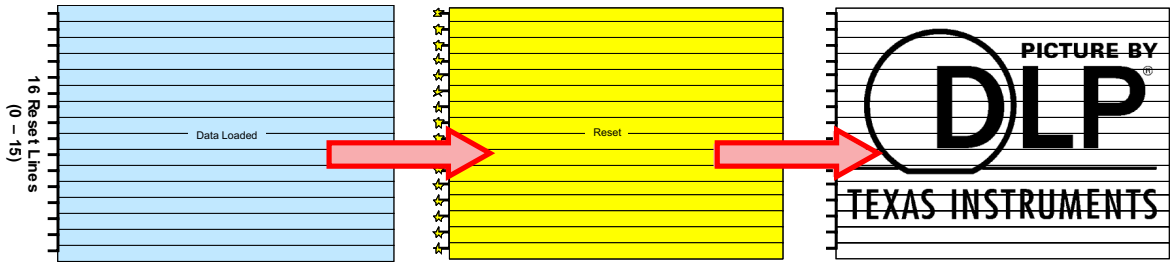


図 8-10. Global Mode

8.5 Window Characteristics and Optics

注

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

8.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

8.5.2 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the *ON* optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

8.5.3 Pupil Match

TI recommends the exit pupil of the illumination is nominally centered within 2° (two degrees) of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

8.5.4 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

8.6 Micromirror Array Temperature Calculation

Achieving optimal DMD performance requires proper management of the maximum DMD case temperature, the maximum temperature of any individual micromirror in the active array, the maximum temperature of the window aperture, and the temperature gradient between case temperature and the predicted micromirror array temperature (See 図 8-11).

See the *Recommended Operating Conditions* for applicable temperature limits.

8.6.1 Package Thermal Resistance

The DMD is designed to conduct absorbed and dissipated heat to the back of the Type A package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the specified operational temperatures, refer to 図 8-11. The total heat load on the DMD is typically driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.

8.6.2 Case Temperature

The temperature of the DMD case can be measured directly. For consistency, Thermal Test Point locations 1, 2, and 3 are defined, as shown in 図 8-11.

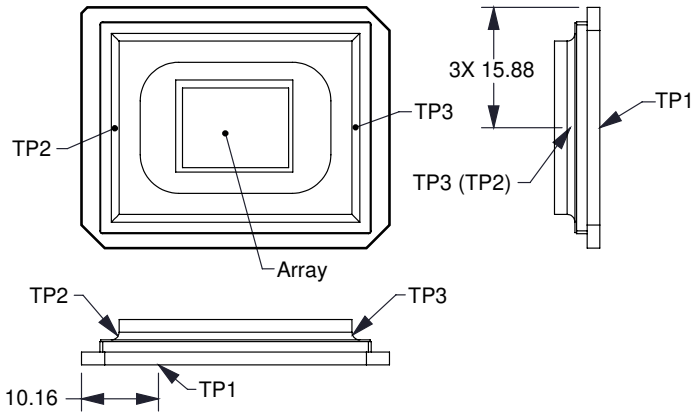


図 8-11. Thermal Test Point Location

8.6.3 Micromirror Array Temperature Calculation

Active array temperature cannot be measured directly; therefore, it must be computed analytically from measurement points on the outside of the package, package thermal resistance, electrical power, and illumination heat load. The relationship between array temperature and the reference ceramic temperature (test point number 1 in 図 8-11) is provided by the following equations:

$$T_{Array} = \text{Measured Ceramic temperature at location (test point number 3)} + (\text{Temperature increase due to power incident to the array} \times \text{array-to-ceramic resistance}) \quad (1)$$

$$= T_{Ceramic} + (Q_{Array} \times R_{Array\text{-}To\text{-}Ceramic}) \quad (2)$$

where

- $T_{Ceramic}$ = Measured ceramic temperature (°C) at location (test point number 3)
- $R_{Array\text{-}To\text{-}Ceramic}$ = DMD package thermal resistance from array to outside ceramic (°C/W)
- Q_{Array} = Total DMD array power, which is both electrical plus absorbed on the DMD active array (W)
- $Q_{Array} = Q_{Electrical} + (Q_{Illumination} \times \text{DMD absorption constant (0.42)})$

where

- $Q_{Electrical}$ = Approximate nominal electrical internal power dissipation (W)
- $Q_{Illumination}$ = [Illumination power density × illumination area on DMD] (W)
- DMD absorption constant = 0.42

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. The nominal electrical power dissipation of the DMD is variable and depends on the operating state of mirrors and the intensity of the light source. The DMD absorption constant of 0.42 assumes nominal operation with an illumination distribution of 83.7% on the active array, 11.9% on the array border, and 4.4% on the window aperture. A system aperture may be required to limit power incident on the package aperture since this area absorbs much more efficiently than the array.

Sample Calculation: (3)

- Illumination power density = 2 W/cm^2
- Illumination area = (1.4008 cm × 1.0506 cm) / 83.7% = 1.76 cm^2 (assumes 83.7% on the active array and 16.3% overfill)
- $Q_{Illumination}$= 2 W/cm^2 × 1.76 cm^2 = 3.52 W
- $Q_{Electrical}$= 2.0 W
- $R_{Array\text{-}To\text{-}Ceramic}$ = 0.9°C/W
- $T_{Ceramic}$= 20°C (measured on ceramic)
- Q_{Array} = 2.0 W + (3.52 W × 0.42) = 3.48 W
- T_{Array} = 20°C + (3.48 W × 0.9°C/W) =23.1°C

8.7 Micromirror Landed-On/Landed-Off Duty Cycle

8.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On−state versus the amount of time the same micromirror is landed in the Off–state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On-state 100% of the time (and in the Off-state 0% of the time); whereas 0/100 would indicate that the pixel is in the Off-state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

8.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

8.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life.

In practice, this curve specifies the Maximum Operating DMD Temperature that the DMD should be operated at for a given long-term average Landed Duty Cycle.

8.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in 表 8-5.

表 8-5. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

9 Application and Implementation

注

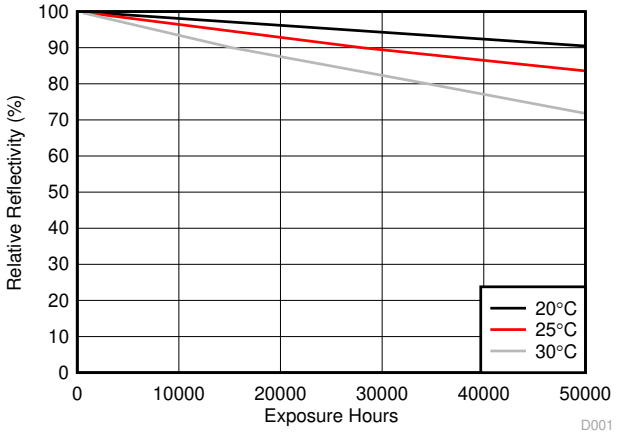
以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The DLP7000UV devices require they be coupled with the DLPC410 controller to provide a reliable solution for many different applications. The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC410. Applications of interest include lithography, 3D Printing, medical systems, and compressive sensing.

9.1.1 DMD Reflectivity Characteristics

TI assumes no responsibility for end-equipment reflectivity performance. Achieving the desired end-equipment reflectivity performance involves making trade-offs between numerous component and system design parameters. DMD reflectivity characteristics over UV exposure times are represented in 図 9-1.



2.3 W/cm^2, 363 to 400 nm

図 9-1. Nominal DMD Relative Reflectivity Percentage and Exposure Hours

DMD reflectivity includes micromirror surface reflectivity and window transmission. The DMD was characterized for DMD reflectivity using a broadband light source (200-W metal-halide lamp). Data is based off of a 2.3-W/cm^2 UV exposure at the DMD surface (363-nm peak output) using a 363-nm high-pass filter between the light source and the DMD. (Contact your local Texas Instruments representative for additional information about power density measurements and UV filter details.)

9.1.2 Design Considerations Influencing DMD Reflectivity

Optimal, long-term performance of the digital micromirror device (DMD) can be affected by various application parameters. Below is a list of some of these application parameters and includes high level design recommendations that may help extend relative reflectivity from time zero:

- Illumination spectrum – using longer wavelengths for operation while preventing shorter wavelengths from striking the DMD
- Illumination power density – using lower power density
- DMD case temperature – operating the DMD with the case temperature at the low end of its specification

- Cumulative incident illumination – limiting the total hours of UV illumination exposure when the DMD is not actively steering UV light in the application. For example, a design might include a shutter to block the illumination or LED illumination where the LEDs can be strobed off during periods not requiring UV exposure.
- Micromirror landed duty cycle – applying a 50/50 duty cycle pattern during periods where operational patterns are not required.

9.2 Typical Application

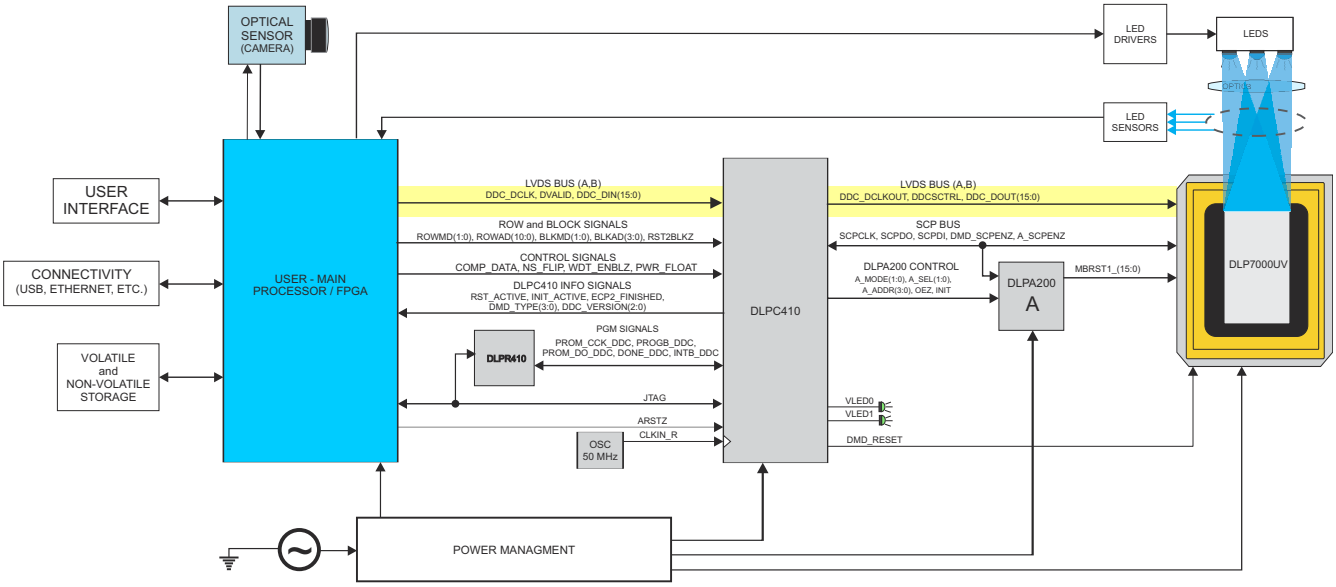


図 9-2. DLPC410 and DLP7000UV Embedded Example Block Diagram

9.2.1 Design Requirements

All applications using the DLP7000UV chipset require both the controller and the DMD components for operation. The system also requires an external parallel flash memory device loaded with the DLPC410 Configuration and Support Firmware. The chipset has several system interfaces and requires some support circuitry. The following interfaces and support circuitry are required:

- DLPC410 system interfaces:
  - Control interface
  - Trigger interface
  - Input data interface
  - Illumination interface
  - Reference clock
- DLP7000UV interfaces:
  - DLPC410 to DLP7000UV digital data
  - DLPC410 to DLP7000UV control interface
  - DLPC410 to DLP7000UV micromirror reset control interface
  - DLPC410 to DLPA200 micromirror driver
  - DLPA200 to DLP7000UV micromirror reset

Device Description:

The DLP7000UV XGA chipset offers developers a convenient way to design a wide variety of industrial, medical, telecom and advanced display applications by delivering maximum flexibility in formatting data, sequencing data, and light patterns.

The DLP7000UV XGA chipset includes the following four components: DMD Digital Controller (DLPC410), EEPROM (DLPR410), DMD Micromirror Driver (DLPA200), and a DMD (DLP7000UV).

DLPC410 Digital Controller for DLP Discovery 4100 chipset

- Provides high speed LVDS data and control interface to the DLP7000UV.
- Drives mirror clocking pulse and timing information to the DLPA200.
- Supports random row addressing.

DLPR410 PROM for DLP Discovery 4100 chipset

- Contains startup configuration information for the DLPC410.

DLPA200 DMD Micromirror Driver

- Generates Micromirror Clocking Pulse control (sometimes referred to as a *Reset*) of DMD mirrors.

DLP7000UV DLP 0.7XGA 2xLVDS UV Type-A DMD

- Steers light in two digital positions (+12° and –12°) using 1024 × 768 micromirror array of aluminum mirrors.

表 9-1. DLP Discovery 4100 Chipset Configuration: 0.7 XGA Chipset

QTY	TI PART	DESCRIPTION
1	DLP7000UV	DLP 0.7XGA 2xLVDS UV Type-A DMD
1	DLPC410	Digital Controller for DLP Discovery 4100 chipset
1	DLPR410	DLP Discovery 4100 configuration PROM
1	DLPA200	DMD micromirror driver

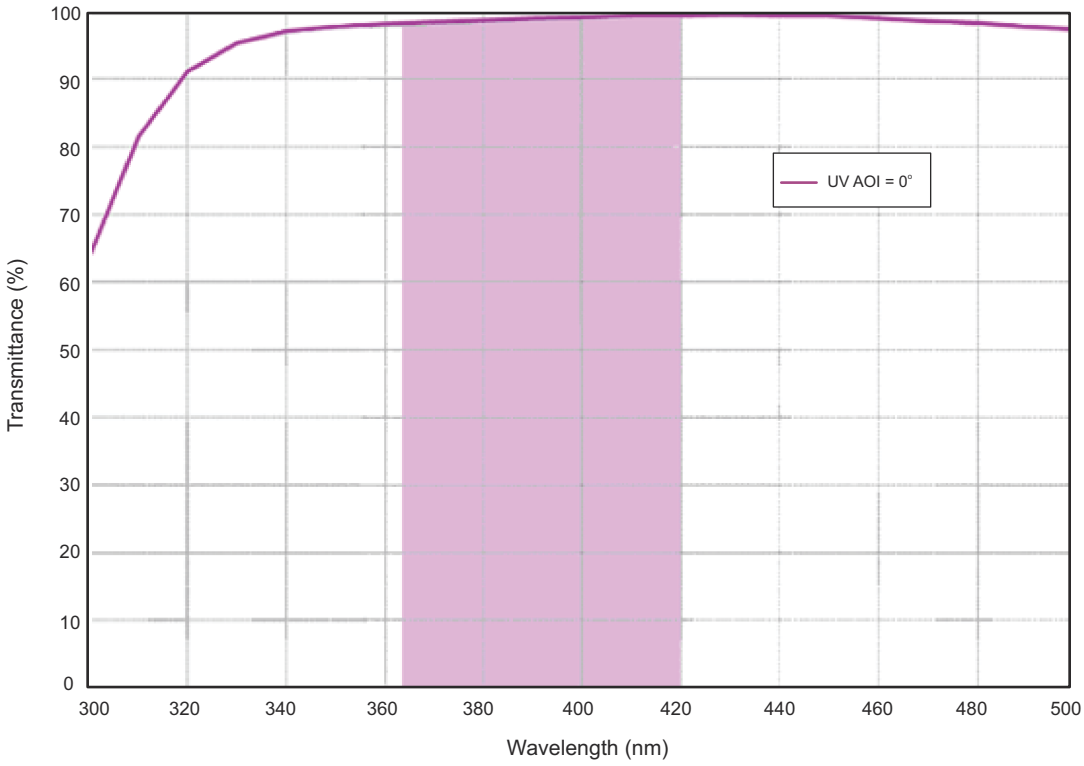
Reliable function and operation of DLP7000UV XGA chipsets require the components be used in conjunction with each other. This document describes the proper integration and use of the DLP7000UV XGA chipset components.

The DLP7000UV XGA chipset can be combined with a user programmable Application FPGA (not included) to create high performance systems.

9.2.2 Detailed Design Procedure

The DLP7000UV DMD is designed with a window which allows transmission of Ultra-Violet (UV) light. This makes it well suited for UV applications requiring fast, spatially programmable light patterns using the micromirror array. UV wavelengths can affect the DMD differently than visible wavelengths. There are system level considerations which should be leveraged when designing systems using this DMD.

9.2.3 Application Curve



Type A UVA on 7056 glass (3-mm thick)

図 9-3. Corning 7056 Nominal UV Window Transmittance (Maximum Transmission Region)

10 Power Supply Recommendations

10.1 Power-Up Sequence (Handled by the DLPC410)

The sequence of events for DMD system power-up is:

1. Apply logic supply voltages to the DLPA200 and to the DMD according to DMD specifications.
2. Place DLPA200 drivers into high impedance states.
3. Turn on DLPA200 bias, offset, or reset supplies according to driver specifications.
4. After all supply voltages are assured to be within the limits specified and with all micromirror clocking pulse operations logically suspended, enable all drivers to either VOFFSET or VBIAS level.
5. Begin micromirror clocking pulse operations.

Repeated failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. The DLP7000UV power-up and power-down procedures are defined by the DLPC410 data sheet (DLPS024). These procedures must be followed to ensure reliable operation of the device.

11 Layout

11.1 Layout Guidelines

The DLP7000UV is part of a chipset that is controlled by the DLPC410 in conjunction with the DLPA200. These guidelines are targeted at designing a PCB board with these components.

11.1.1 Impedance Requirements

Signals should be routed to have a matched impedance of 50 Ω ±10% except for LVDS differential pairs (DMD_DAT_Xnn, DMD_DCKL_Xn, and DMD_SCTRL_Xn), which should be matched to 100 Ω ±10% across each pair.

11.1.2 PCB Signal Routing

When designing a PCB board for the DLP7000UV controlled by the DLPC410 in conjunction with the DLPA200, the following are recommended:

Signal trace corners should be no sharper than 45°. Adjacent signal layers should have the predominate traces routed orthogonal to each other. TI recommends that critical signals be hand routed in the following order: DDR2 Memory, DMD (LVDS signals), then DLPA200 signals.

TI does not recommend signal routing on power or ground planes.

TI does not recommend ground plane slots.

High speed signal traces should not crossover slots in adjacent power and/or ground planes.

表 11-1. Important Signal Trace Constraints

SIGNAL	CONSTRAINTS
LVDS (DMD_DAT_xnn, DMD_DCKL_xn, and DMD_SCTRL_xn)	P-to-N data, clock, and SCTRL: <10 mils (0.25 mm); Pair-to-pair <10 mils (0.25 mm); Bundle-to-bundle <2000 mils (50 mm, for example DMD_DAT_Ann to DMD_DAT_Bnn) Trace width: 4 mil (0.1 mm) Trace spacing: In ball field – 4 mil (0.11 mm); PCB etch – 14 mil (0.36 mm) Maximum recommended trace length <6 inches (150 mm)

表 11-2. Power Trace Widths and Spacing

SIGNAL NAME	MINIMUM TRACE WIDTH	MINIMUM TRACE SPACING	LAYOUT REQUIREMENTS
GND	Maximize	5 mil (0.13 mm)	Maximize trace width to connecting pin as a minimum
VCC, VCC2	20 mil (0.51 mm)	10 mil (0.25 mm)	
MBRST[15:0]	10 mil (0.25 mm)	10 mil (0.25 mm)	

11.1.3 Fiducials

Fiducials for automatic component insertion should be 0.05-inch copper with a 0.1-inch cutout (antipad). Fiducials for optical auto insertion are placed on three corners of both sides of the PCB.

11.1.4 PCB Layout Guidelines

A target impedance of 50 Ω for single ended signals and 100 Ω between LVDS signals is specified for all signal layers.

11.1.4.1 DMD Interface

The digital interface from the DLPC410 to the DMD are LVDS signals that run at clock rates up to 400 MHz. Data is clocked into the DMD on both the rising and falling edge of the clock, so the data rate is 800 MHz. The LVDS signals should have 100-Ω differential impedance. The differential signals should be matched but kept as short as possible. Parallel termination at the LVDS receiver is in the DMD; therefore, on board termination is not necessary.

11.1.4.1.1 Trace Length Matching

The DLPC410 DMD data signals require precise length matching. Differential signals should have impedance of 100 Ω (with 5% tolerance). It is important that the propagation delays are matched. The maximum differential pair uncoupled length is 100 mils with a relative propagation delay of ±25 mil between the p and n. Matching all signals exactly will maximize the channel margin. The signal path through all boards, flex cables and internal DMD routing must be considered in this calculation.

11.1.4.2 DLP7000UV Decoupling

General decoupling capacitors for the DLP7000UV should be distributed around the PCB and placed to minimize the distance from IC voltage and ground pads. Each decoupling capacitor (0.1 µF recommended) should have vias directly to the ground and power planes. Via sharing between components (discreet or integrated) is discouraged. The power and ground pads of the DLP7000UV should be tied to the voltage and ground planes with their own vias.

11.1.4.2.1 Decoupling Capacitors

Decoupling capacitors should be placed to minimize the distance from the decoupling capacitor to the supply and ground pin of the component. It is recommended that the placement of and routing for the decoupling capacitors meet the following guidelines:

- The supply voltage pin of the capacitor should be located close to the device supply voltage pin(s). The decoupling capacitor should have vias to ground and voltage planes. The device can be connected directly to the decoupling capacitor (no via) if the trace length is less than 0.1 inch. Otherwise, the component should be tied to the voltage or ground plane through separate vias.
- The trace lengths of the voltage and ground connections for decoupling capacitors and components should be less than 0.1 inch to minimize inductance.
- The trace width of the power and ground connection to decoupling capacitors and components should be as wide as possible to minimize inductance.
- Connecting decoupling capacitors to ground and power planes through multiple vias can reduce inductance and improve noise performance.
- Decoupling performance can be improved by utilizing low ESR and low ESL capacitors.

11.1.4.3 VCC and VCC2

The VCC pins of the DMD should be connected directly to the DMD VCC plane. Decoupling for the VCC should be distributed around the DMD and placed to minimize the distance from the voltage and ground pads. Each decoupling capacitor should have vias directly connected to the ground and power planes. The VCC and GND pads of the DMD should be tied to the VCC and ground planes with their own vias.

The VCC2 voltage can be routed to the DMD as a trace. Decoupling capacitors should be placed to minimize the distance from the VCC2 and ground pads of the DMD. Using wide etch from the decoupling capacitors to the DMD connection will reduce inductance and improve decoupling performance.

11.1.4.4 DMD Layout

See the respective sections in this data sheet for package dimensions, timing and pin out information.

11.1.4.5 DLPA200

The DLPA200 generates the micromirror clocking pulses for the DMD. The DMD-drive outputs from the DLPA200 (MBRST[15:0]) should be routed with minimum trace width of 11 mil and a minimum spacing of 15 mil. The VCC and VCC2 traces from the output capacitors to the DLPA200 should also be routed with a minimum trace width and spacing of 11 mil and 15 mil, respectively. See the DLPA200 customer data sheet (DLPS015) for mechanical package and layout information.

11.2 Layout Example

For LVDS (and other differential signal) pairs and groups, it is important to match trace lengths. In the area of the dashed lines, 図 11-1 shows correct matching of signal pair lengths with serpentine sections to maintain the correct impedance.

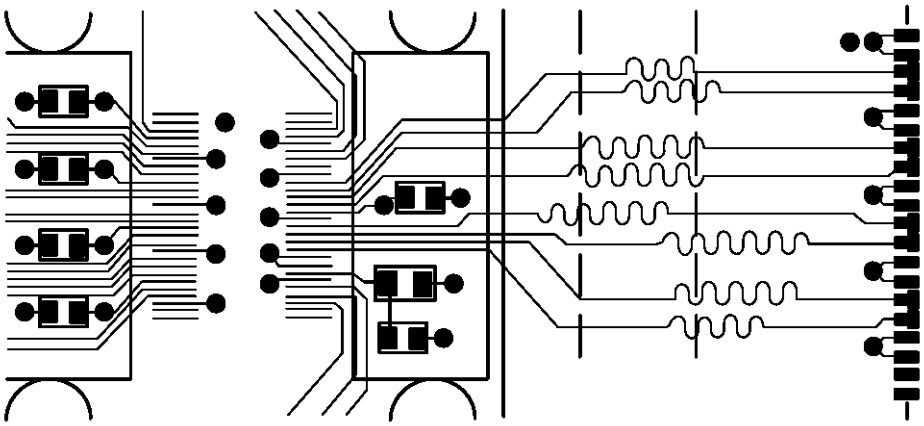


図 11-1. Mitering LVDS Traces to Match Lengths

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

図 12-1 provides a legend of reading the complete device name for any DLP device.

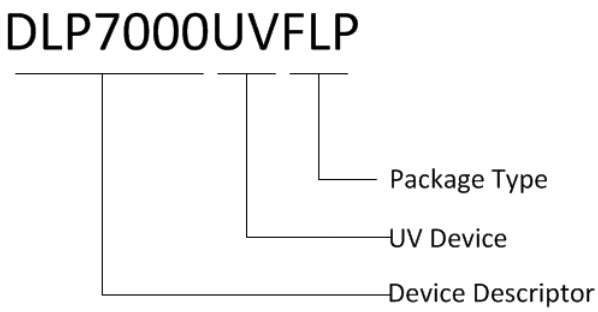


図 12-1. Device Nomenclature

12.1.1.1 Device Marking

The device marking consists of the fields shown in 図 12-2.

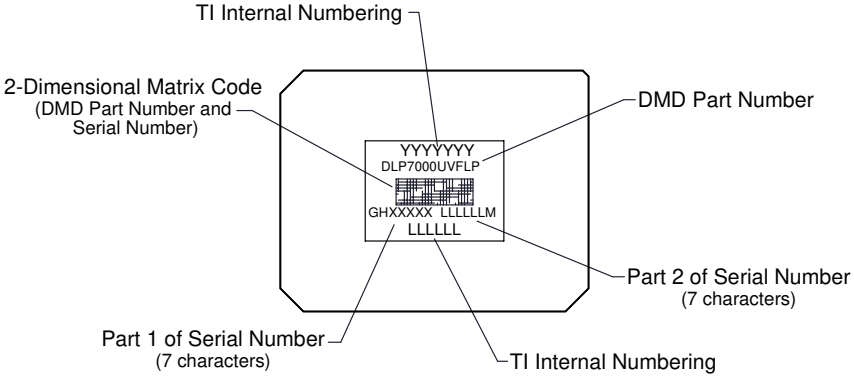


図 12-2. Device Marking

12.2 Documentation Support

12.2.1 Related Documentation

The following documents contain additional information related to the use of the DLP7000UV device:

表 12-1. Related Documentation

DOCUMENT TITLE	DOCUMENT LINK
DLPC410 Digital Controller for DLP Discovery 4100 chipset data sheet	DLPS024
DLPA200 DMD Micromirror Driver data sheet	DLPS015
DLPR410 PROM for DLP Discovery 4100 chipset data sheet	DLPS027

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DLP7000UV	Click here	Click here	Click here	Click here	Click here
DLPA200	Click here	Click here	Click here	Click here	Click here
DLPC410	Click here	Click here	Click here	Click here	Click here
DLPR410	Click here	Click here	Click here	Click here	Click here

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP7000UVFLP	Active	Production	CLGA (FLP) | 203	18 | JEDEC TRAY (5+1)	Yes	NIPDAU	N/A for Pkg Type	20 to 30	
DLP7000UVFLP.B	Active	Production	CLGA (FLP) | 203	18 | JEDEC TRAY (5+1)	Yes	NIPDAU	N/A for Pkg Type	20 to 30	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

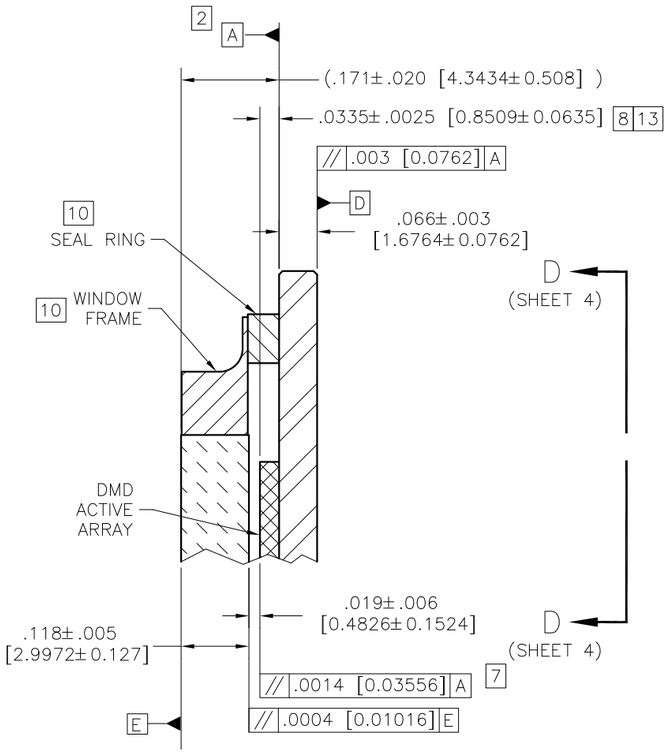
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

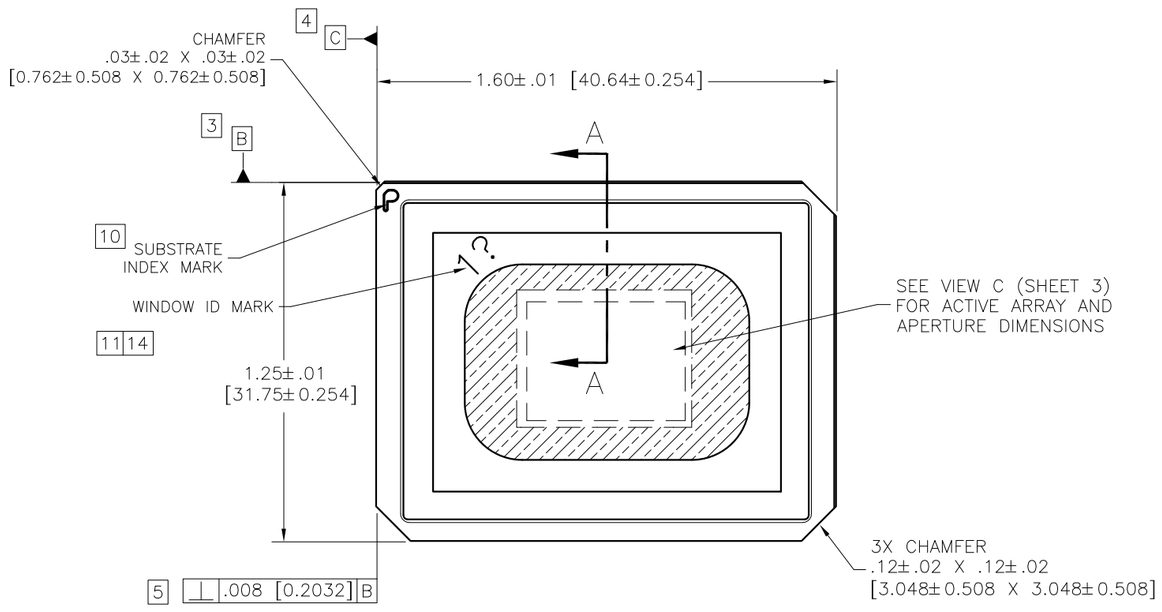
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2071155, INITIAL RELEASE	07/24/06	MRW
B	ECO 2077187, CHG DESG FROM 29	02/19/07	MRW
C	ECO 2150557, ADD NOTE 15, UPDATE VIEW D-D SHEET 4.	05/12/15	MAA
D	ECO 2179942, DELETE NOTE 12	03/01/19	BMH

NOTES: UNLESS OTHERWISE SPECIFIED:

1. INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994.
2. DATUM A (SYSTEM INTERFACE PLANE) ESTABLISHED BY THREE DATUM AREAS SHOWN IN VIEW B (SHEET 2).
3. DATUM B ESTABLISHED BY TWO DATUM AREAS SHOWN IN VIEW B (SHEET 2).
4. DATUM C ESTABLISHED BY DATUM AREA SHOWN IN VIEW B (SHEET 2).
5. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
6. LOCALIZED BACKSIDE SURFACE FLATNESS APPLIES TO ENTIRE CERAMIC SURFACE.
7. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
8. DIE HEIGHT TOLERANCE APPLIES TO CENTER OF DMD ACTIVE ARRAY ONLY.
9. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND IS THE MAXIMUM VALUE ALLOWED.
10. SUBSTRATE INDEX MARK, SYMBOLIZATION PAD, SEAL RING, AND WINDOW FRAME TO BE ELECTRICALLY CONNECTED TO VSS PLANE IN SUBSTRATE.
11. WINDOW SHALL BE ORIENTED SUCH THAT WINDOW ID MARK ALIGNS WITH SUBSTRATE INDEX MARK AS SHOWN.
12. (DELETED)
13. DMD ACTIVE ARRAY DIMENSIONS ARE RELATED TO DATUM A (PRIMARY), DATUM B (SECONDARY), AND DATUM C (TERTIARY).
14. ? IS A WILD CARD CHARACTER AND CAN BE ANY LETTER.
15. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING AS SHOWN ABOVE THE SYMBOLIZATION PAD. SUBSTRATES WITH Ni/Pd/Au SHALL HAVE MARKING IN THE ALTERNATE LOCATION BELOW THE SYMBOLIZATION PAD.



SECTION A-A
SCALE 6/1



-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES [MILLIMETERS]
- TOLERANCES: ANGLES ± 1°
  3 PLACE DECIMALS ±.005 [0.127]
  2 PLACE DECIMALS ±.01 [0.254]
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- ~~CONCENTRICITY MACHINED DIAMETERS .010 FIM~~
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .125 +.004 -.001	.126 THRU .250 +.005 -.001	.251 THRU .500 +.006 -.001
.501 THRU .750 +.008 -.001	.751 THRU 1.000 +.010 -.001	1.001 THRU 2.000 +.012 -.001

THIRD ANGLE PROJECTION

NEXT ASSY	USED ON
NONE	0314DA

APPLICATION

DWN	M. WILLIAMS	DATE 07/12/06
ENGR	A. ARAYATA	07/12/06
QA		
APVD		

TEXAS INSTRUMENTS
Dallas, Texas

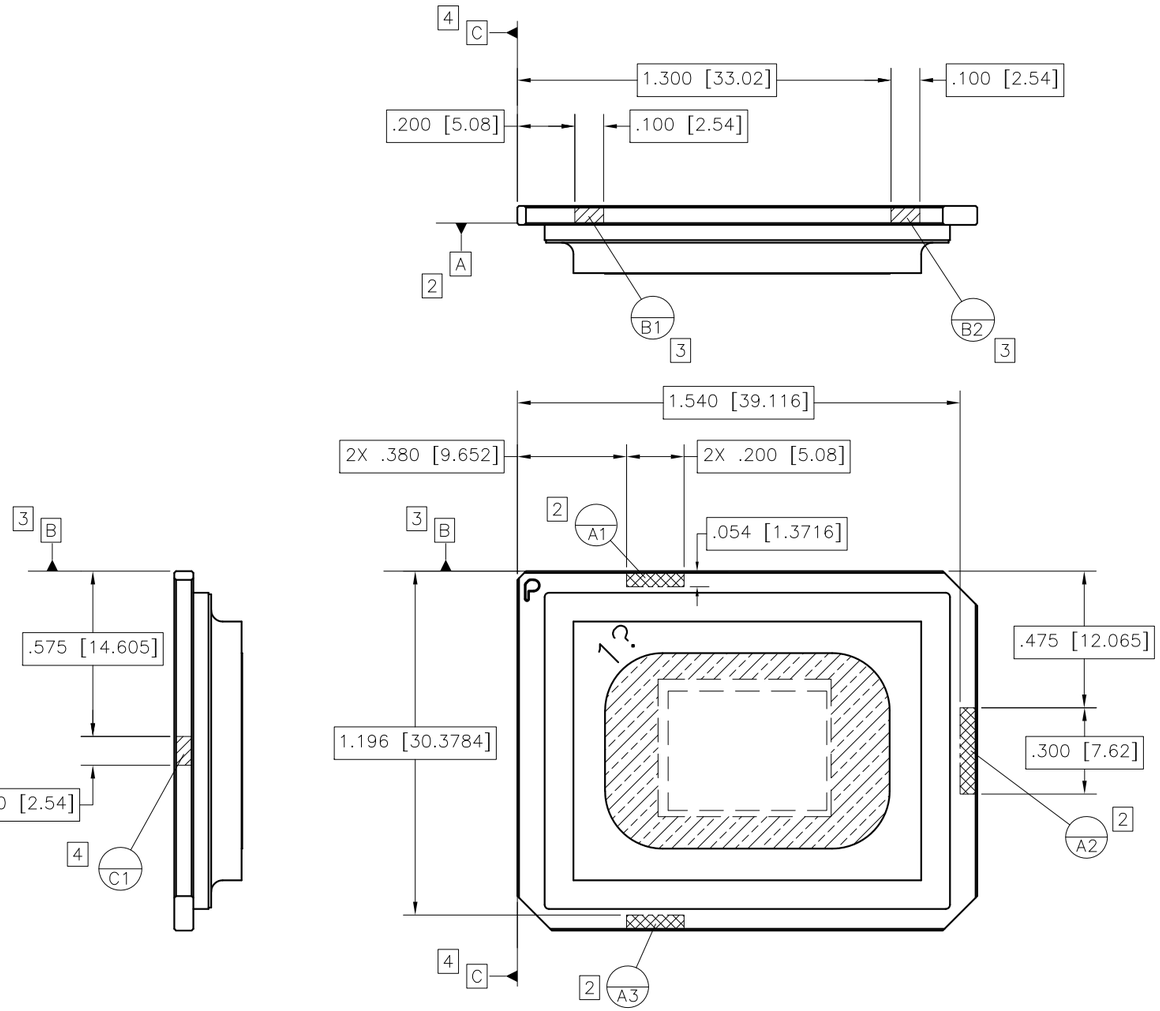
ICD, MECHANICAL, DMD
.7XGA 2xLVDS TYPE A (FLP)

SIZE	DRAWING NO	REV
C	2507867	D

SCALE 3/1 SHEET 1 OF 4

SH 1
DWG NO 2507867

ACEC1g

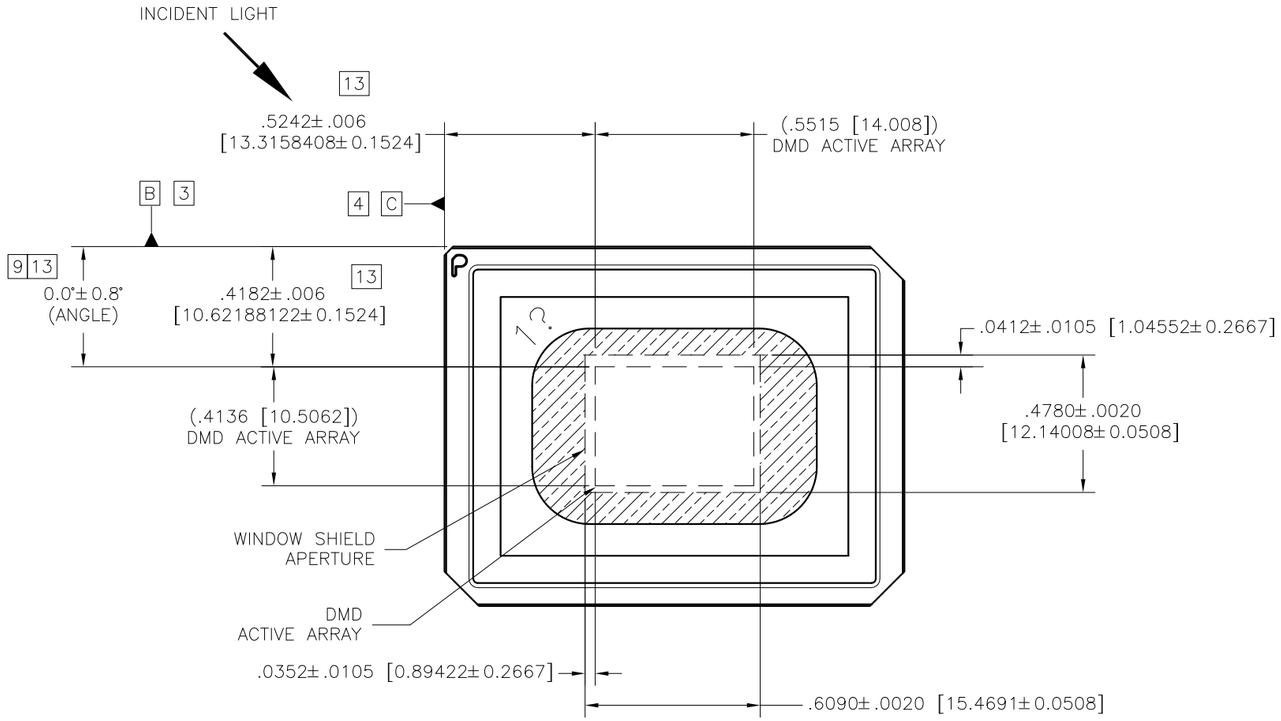


VIEW B (SHEET 1 NOTES)
DATUMS A, B, AND C

Texas Instruments, Dallas, Texas	DWN DATE	SIZE C		DRAWING NO 2507867	REV D
	ISSUE DATE	SCALE 3/1		SHEET 2	

DWG NO 2507867 SH 2

ACEC2c

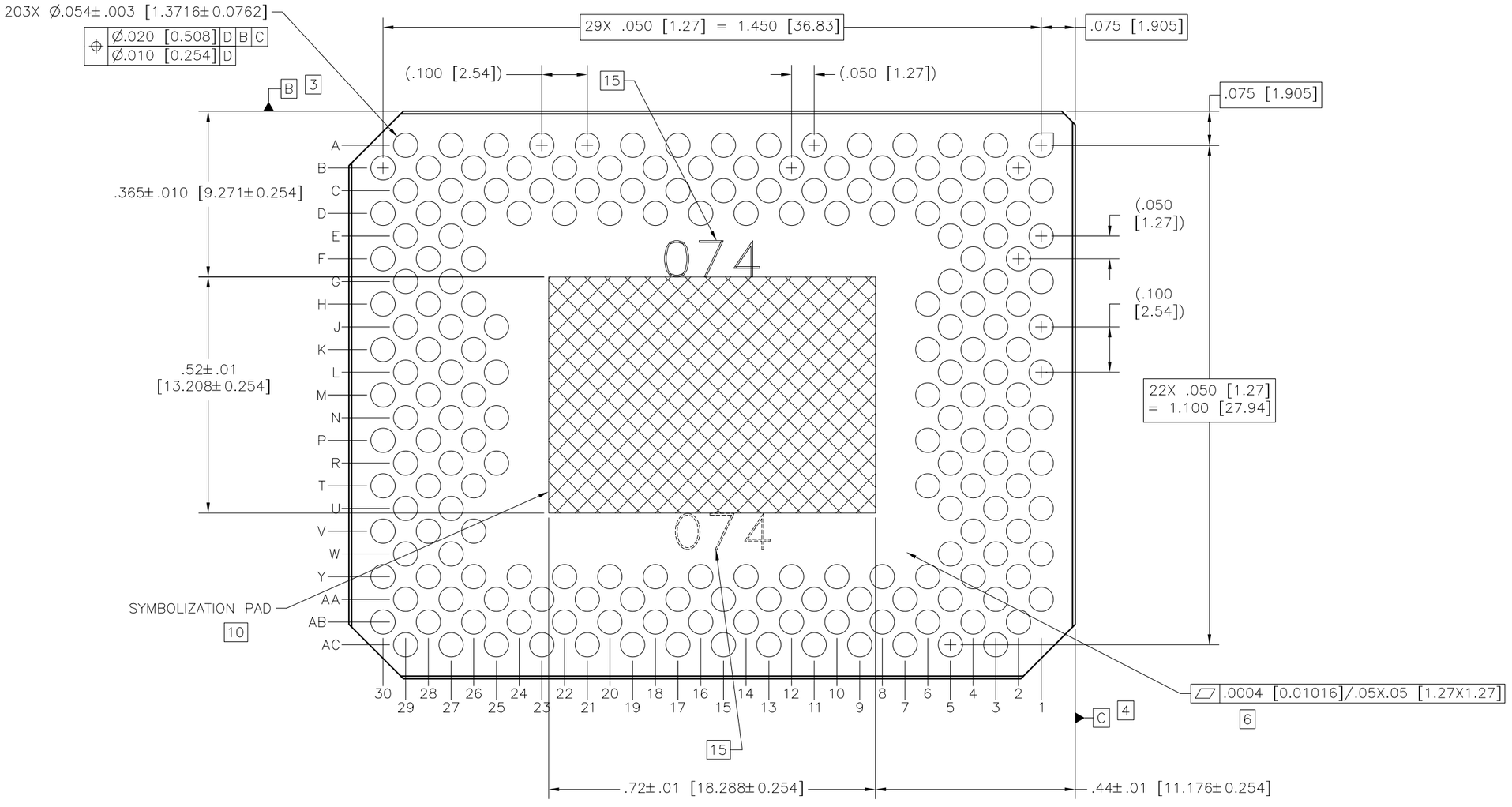


VIEW C (SHEET 1)
DMD ACTIVE ARRAY AND
WINDOW SHIELD APERTURE

DWG NO 2507867 SH 3

ACEC2c

Texas Instruments Dallas, Texas	DWN DATE	SIZE C		DRAWING NO 2507867	REV D
	ISSUE DATE	SCALE 3/1		SHEET 3	



VIEW D–D (SHEET 1)
SCALE 6/1

Texas Instruments Dallas, Texas	DWN DATE	SIZE C		DRAWING NO 2507867	REV D
	ISSUE DATE	SCALE 3/1		SHEET 4	

ACEC2c

SH 4
DWG NO 2507867

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最終更新日：2025 年 10 月