

DLP660TE 0.66 4K UHD デジタル・マイクロミラー・デバイス

1 特長

- 対角 0.66 インチのマイクロミラー・アレイ
 - 画面に 4K 超高解像度 (UHD) 3840 × 2160 ピクセルを表示
 - マイクロミラー・ピッチ: 5.4 ミクロン
 - マイクロミラー傾斜角: ±17° (平面に対して)
 - 下部光源
- 2 つの LVDS 入力データ・バス
- DLP660TE チップセットの構成部品:
 - DLP660TE DMD
 - DLPC4420 コントローラ
 - DLPA100 コントローラ・パワー・マネージメントおよびモーター・ドライバ IC

2 アプリケーション

- 4K UHD ディスプレイ
- デジタル・サイネージ
- レーザー TV
- プロジェクション・マッピング

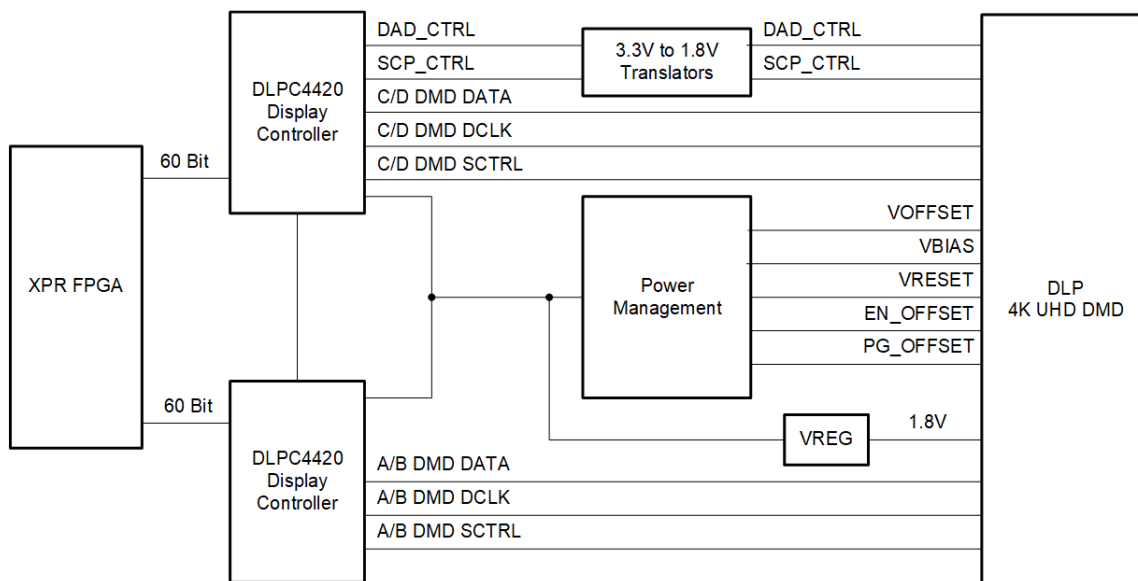
3 概要

テキサス・インスツルメンツの DLP® DLP660TE デジタル・マイクロミラー・デバイス (DMD) は、デジタル制御型の MOEMS (micro-opto-electromechanical system) 空間光変調器 (SLM) で、色鮮やかなフル 4K UHD ディスプレイ・ソリューションを手頃な価格で実現します。適切な光学システムと組み合わせることにより、DLP660TE DMD は真の 4K UHD 解像度 (画面上 8.3M ピクセル) を表示し、正確で高精細の画像を様々な表面上に表示できます。DLP660TE DMD と DLPC4420 ディスプレイコントローラの組み合わせにより、DLPA100 コントローラ・電源とモーター・ドライバは高性能システムを実現する能力を備えており、4K UHD 高輝度ディスプレイアプリケーションに最適です。

製品情報⁽¹⁾

部品番号	パッケージ	本体サイズ (公称)
DLP660TE	FYG (350)	35mm × 32mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



DLP660TE のアプリケーション概略図



Table of Contents

1 特長	1	6.6 Micromirror Array Temperature Calculation.....	25
2 アプリケーション	1	6.7 Micromirror Power Density Calculation.....	27
3 概要	1	6.8 Micromirror Landed-On/Landed-Off Duty Cycle.....	28
4 Pin Configuration and Functions	3	7 Application and Implementation	31
4.1 Pin Functions—Test Pads.....	10	7.1 Application Information.....	31
5 Specifications	11	7.2 Typical Application.....	32
5.1 Absolute Maximum Ratings.....	11	7.3 DMD Die Temperature Sensing.....	34
5.2 Storage Conditions.....	12	8 Power Supply Recommendations	36
5.3 ESD Ratings.....	12	8.1 DMD Power Supply Power-Up Procedure.....	36
5.4 Recommended Operating Conditions.....	12	8.2 DMD Power Supply Power-Down Procedure.....	36
5.5 Thermal Information.....	15	9 Layout	39
5.6 Electrical Characteristics.....	15	9.1 Layout Guidelines.....	39
5.7 Capacitance at Recommended Operating Conditions.....	15	9.2 Layout Example.....	39
5.8 Timing Requirements.....	16	10 Device and Documentation Support	41
5.9 System Mounting Interface Loads.....	19	10.1 サード・パーティ製品に関する免責事項.....	41
5.10 Micromirror Array Physical Characteristics.....	19	10.2 Device Support.....	41
5.11 Micromirror Array Optical Characteristics.....	21	10.3 Documentation Support.....	42
5.12 Window Characteristics.....	22	10.4 ドキュメントの更新通知を受け取る方法.....	42
5.13 Chipset Component Usage Specification.....	22	10.5 サポート・リソース.....	42
6 Detailed Description	23	10.6 Trademarks.....	42
6.1 Overview.....	23	10.7 静電気放電に関する注意事項.....	43
6.2 Functional Block Diagram.....	23	10.8 用語集.....	43
6.3 Feature Description.....	24	11 Revision History	43
6.4 Device Functional Modes.....	24	12 Mechanical, Packaging, and Orderable Information	44
6.5 Optical Interface and System Image Quality Considerations.....	24		

4 Pin Configuration and Functions

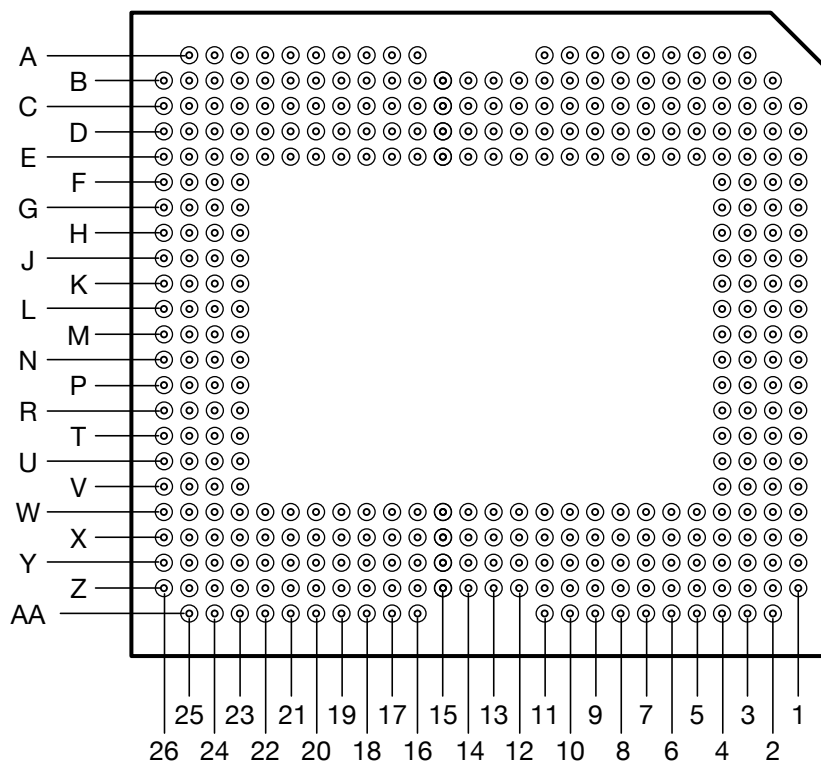


図 4-1. Series 610 350-pin FYG Bottom View

注意

For reliable, long-term operation of the 0.66-inch UHD S610 DMD, it is critical to properly manage the layout and operation of the signals identified in the table below. For specific details and guidelines, refer to the [PCB Design Requirements for TI DLP Standard TRP Digital Micromirror Devices](#) application report before designing the board.

表 4-1. Pin Functions

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
DATA INPUTS					
D_AN(0)	C7	Input	2xLVDS		LVDS pair for Data Bus A (15:0)
D_AP(0)	C8				
D_AN(1)	D4				
D_AP(1)	E4				
D_AN(2)	C5				
D_AP(2)	C4				
D_AN(3)	D6				
D_AP(3)	C6				
D_AN(4)	D8				
D_AP(4)	D7				
D_AN(5)	D3				
D_AP(5)	E3				
D_AN(6)	B3				
D_AP(6)	C3				
D_AN(7)	E11				
D_AP(7)	E10				
D_AN(8)	E6				
D_AP(8)	E5				
D_AN(9)	B10				
D_AP(9)	C10				
D_AN(10)	B8				
D_AP(10)	B9				
D_AN(11)	C13				
D_AP(11)	C14				
D_AN(12)	D15				
D_AP(12)	E15				
D_AN(13)	B12				
D_AP(13)	B13				
D_AN(14)	B15				
D_AP(14)	B16				
D_AN(15)	C16				
D_AP(15)	C17				

表 4-1. Pin Functions (続き)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
D_BN(0)	Y8	Input	2xLVDS		LVDS pair for Data Bus B (15:0)
D_BP(0)	Y7				
D_BN(1)	X4				
D_BP(1)	W4				
D_BN(2)	Z3				
D_BP(2)	Y3				
D_BN(3)	X6				
D_BP(3)	Y6				
D_BN(4)	X8				
D_BP(4)	X7				
D_BN(5)	X3				
D_BP(5)	W3				
D_BN(6)	W15				
D_BP(6)	X15				
D_BN(7)	W11				
D_BP(7)	W10				
D_BN(8)	W6				
D_BP(8)	W5				
D_BN(9)	AA9				
D_BP(9)	AA10				
D_BN(10)	Z8				
D_BP(10)	Z9				
D_BN(11)	Y13				
D_BP(11)	Y14				
D_BN(12)	Z10				
D_BP(12)	Y10				
D_BN(13)	Z12				
D_BP(13)	Z13				
D_BN(14)	Z15				
D_BP(14)	Z16				
D_BN(15)	Y16				
D_BP(15)	Y17				

表 4-1. Pin Functions (続き)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
D_CN(0)	C18	Input	2xLVDS		LVDS pair for Data Bus C (15:0)
D_CP(0)	C19				
D_CN(1)	A20				
D_CP(1)	A19				
D_CN(2)	L23				
D_CP(2)	K23				
D_CN(3)	C23				
D_CP(3)	B23				
D_CN(4)	G23				
D_CP(4)	H23				
D_CN(5)	H24				
D_CP(5)	G24				
D_CN(6)	B18				
D_CP(6)	B19				
D_CN(7)	C21				
D_CP(7)	B21				
D_CN(8)	D23				
D_CP(8)	E23				
D_CN(9)	D25				
D_CP(9)	C25				
D_CN(10)	L24				
D_CP(10)	K24				
D_CN(11)	K25				
D_CP(11)	J25				
D_CN(12)	B24				
D_CP(12)	A24				
D_CN(13)	D26				
D_CP(13)	C26				
D_CN(14)	G25				
D_CP(14)	F25				
D_CN(15)	K26				
D_CP(15)	J26				

表 4-1. Pin Functions (続き)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
D_DN(0)	Y18	Input	2xLVDS		LVDS pair for Data Bus D (15:0)
D_DP(0)	Y19				
D_DN(1)	AA20				
D_DP(1)	AA19				
D_DN(2)	N23				
D_DP(2)	P23				
D_DN(3)	Y23				
D_DP(3)	Z23				
D_DN(4)	U23				
D_DP(4)	T23				
D_DN(5)	T24				
D_DP(5)	U24				
D_DN(6)	Z18				
D_DP(6)	Z19				
D_DN(7)	Y21				
D_DP(7)	Z21				
D_DN(8)	X23				
D_DP(8)	W23				
D_DN(9)	X25				
D_DP(9)	Y25				
D_DN(10)	N24				
D_DP(10)	P24				
D_DN(11)	P25				
D_DP(11)	R25				
D_DN(12)	Z24				
D_DP(12)	AA24				
D_DN(13)	X26				
D_DP(13)	Y26				
D_DN(14)	U25				
D_DP(14)	V25				
D_DN(15)	P26				
D_DP(15)	R26				
DCLK_AN	B6	Input	LVDS		LVDS pair for Data Clock A
DCLK_AP	B5	Input	LVDS		LVDS pair for Data Clock B
DCLK_BN	Z6				
DCLK_BP	Z5	Input	LVDS		LVDS pair for Data Clock C
DCLK_CN	G26				
DCLK_CP	F26	Input	LVDS		LVDS pair for Data Clock D
DCLK_DN	U26				
DCLK_DP	V26				
DATA CONTROL INPUTS					
SCTRL_AN	A10	Input	LVDS		LVDS pair for Serial Control (Sync) A
SCTRL_AP	A9				

表 4-1. Pin Functions (続き)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
SCTRL_BN	Y4	Input	LVDS		LVDS pair for Serial Control (Sync) B
SCTRL_BP	Y5				
SCTRL_CN	E24	Input	LVDS		LVDS pair for Serial Control (Sync) C
SCTRL_CP	D24				
SCTRL_DN	W24	Input	LVDS		LVDS pair for Serial Control (Sync) D
SCTRL_DP	X24				
DAD CONTROL INPUTS					
RESET_ADDR(0)	R3	Input	LVCMOS		Reset Driver Address Select. The bond pad connects to an internal pulldown circuit.
RESET_ADDR(1)	R4				
RESET_ADDR(2)	T3				
RESET_ADDR(3)	U2				
RESET_MODE(0)	P4	Input	LVCMOS		Reset Driver Mode Select. The bond pad connects to an internal pulldown circuit.
RESET_MODE(1)	V3				
RESET_OEZ	R2	Input	LVCMOS		Active low. Output Enable signal for an internal reset driver circuitry. Bond Pad connects to an internal pullup circuit
RESET_SEL(0)	P3	Input	LVCMOS		Reset Driver Level Select. The bond pad connects to an internal pulldown circuit.
RESET_SEL(1)	V2				
RESET_STROBE	W8	Input	LVCMOS		Rising edge on RESET_STROBE latches in the control signals. The bond pad connects to an internal pulldown circuit.
RESETZ	U4	Input	LVCMOS		Active low. Places reset circuitry in known VOFFSET state. The bond pad connects to an internal pulldown circuit.
SCP CONTROL					
SCPCLK	W17	Input	LVCMOS		Serial communications port clock. SCPCLK is only active when SCPENZ goes low. The bond pad connects to an internal pulldown circuit.
SCPD1	W18	Input	LVCMOS		Serial communications port data. Synchronous to the rising edge of SCPCLK. The bond pad connects to an internal pulldown circuit.
SCPENZ	X18	Input	LVCMOS		Active low serial communications port enable. The bond pad connects to an internal pulldown circuit.
SCPDO	W16	Output	LVCMOS		Serial communications port output
EXTERNAL REGULATOR SIGNALS					
EN_BIAS	J4	Output	LVCMOS		Active high. Enable signal for external VBIAS regulator
EN_OFFSET	H3	Output	LVCMOS		Active high. Enable signal for external VOFFSET regulator
EN_RESET	J3	Output	LVCMOS		Active high. Enable signal for external VRESET regulator
OTHER SIGNALS					
RESET_IRQZ	U3	Output	LVCMOS		Active low. Output interrupt to DLP controller (ASIC)
TEMP_PLUS	E16	Analog			Temperature sensor diode anode ⁽¹⁾
TEMP_MINUS	E17	Analog			Temperature sensor diode cathode ⁽¹⁾

表 4-1. Pin Functions (続き)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
POWER					
VBIAS	A5, A6, A7	Power			Power supply for positive bias level of micromirror reset signal
V _{CC}	A8, B2, C1, D1, D10, D12, D19, E1, E19, E20, E21, F1, K1, L1, M1, N1, P1,V1, W1, W19, W20, W21, X1, X10, X12, X19, Y1, Z1, Z2, AA2, AA8,	Power			Power supply for low voltage CMOS logic. Power supply for normal high voltage at micromirror address electrodes. Power supply for offset level during power down sequence
V _{CCI}	A11, A16, A17, A18, A21, A22, A23, AA11, AA16, AA17, AA18, AA21, AA22, AA23,	Power			Power supply for low voltage CMOS LVDS interface
V _{OFFSET}	A3, A4, A25, B26, L26, M26, N26, Z26, AA3, AA4, AA25	Power			Power supply for high voltage CMOS logic. Power supply for stepped high voltage at micromirror address electrodes. Power supply for offset level of MBRST(15:0)
V _{RESET}	G1, H1, J1, R1, T1, U1	Power			Power supply for the negative reset level of the micromirror reset signal
V _{SS} (Ground)	B4, B7, B11, B14, B17, B20, B22, B25, C2, C9, C20, C22, C24, D2, D5, D9, D11, D14, D18, D20, D21, D22, E2, E7, E9, E22, E25, E26, F4, F23, F24, H2, H4, H25, H26, J23, J24, K2, L2, L3, L4, L25, M2, M3, M4, M23, M24, M25, N2, N3, N25, P2,R23, R24, T2, T4, T25, T26, V4, V23, V24, W2, W7, W9, W22, W25, W26, X2, X5, X9, X11, X20, X21, X22, Y2, Y9, Y20, Y22, Y24, Z4, Z7, Z11, Z14, Z17, Z20, Z22, Z25	Ground			Common return for all power
RESERVED SIGNALS					
RESERVED_PFE	E18	Ground			Connect to ground on the printed circuit board (PCB). The bond pad connects to an internal pulldown circuit.
RESERVED_TM	G4	Ground			Connect to ground on the printed circuit board (PCB). The bond pad connects to an internal pulldown circuit.
RESERVED_TP0	E8	Input			Do not connect on the printed circuit board (PCB).
RESERVED_TP1	J2	Input			Do not connect on the printed circuit board (PCB).
RESERVED_TP2	G2	Input			Do not connect on the printed circuit board (PCB).
RESERVED_BA	N4	Output			Do not connect on the printed circuit board (PCB).

表 4-1. Pin Functions (続き)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
RESERVED_BB	K4	Output			Do not connect on the printed circuit board (PCB).
RESERVED_BC	X17	Output			Do not connect on the printed circuit board (PCB).
RESERVED_BD	D17	Output			Do not connect on the printed circuit board (PCB).

(1) Connect VSS for proper DMD operation.

4.1 Pin Functions—Test Pads

PIN NUMBER	SYSTEM BOARD
E13	Do not connect.
C12	Do not connect.
D13	Do not connect.
C11	Do not connect.
E14	Do not connect.
E12	Do not connect.
C15	Do not connect.
D16	Do not connect.
W13	Do not connect.
Y12	Do not connect.
X13	Do not connect.
Y11	Do not connect.
W14	Do not connect.
W12	Do not connect.
Y15	Do not connect.
X16	Do not connect.

5 Specifications

5.1 Absolute Maximum Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

		MIN	MAX	UNIT
Supply Voltages				
V _{CC}	Supply voltage for LVCMOS core logic ⁽¹⁾	−0.5	2.3	V
V _{CCI}	Supply voltage for LVDS receivers ⁽¹⁾	−0.5	2.3	V
V _{OFFSET}	Supply voltage for HVCMOS and micromirror electrode ^{(1) (2)}	−0.5	11	V
V _{BIAS}	Supply voltage for micromirror electrode ⁽¹⁾	−0.5	19	V
V _{RESET}	Supply voltage for micromirror electrode ⁽¹⁾	−15	−0.3	V
V _{CC} − V _{CCI}	Supply voltage delta (absolute value) ⁽³⁾		0.3	V
V _{BIAS} − V _{OFFSET}	Supply voltage delta (absolute value) ⁽⁴⁾		11	V
V _{BIAS} − V _{RESET}	Supply voltage delta (absolute value) ⁽⁵⁾		34	V
Input Voltages				
	Input voltage for all other LVCMOS input pins ⁽¹⁾	−0.5	V _{CC} + 0.5	V
	Input voltage for all other LVDS input pins ^{(1) (5)}	−0.5	V _{CCI} + 0.5	V
V _{ID}	Input differential voltage (absolute value) ⁽⁵⁾		500	mV
I _{ID}	Input differential current ⁽⁶⁾		6.25	mA
Clocks				
f _{CLOCK}	Clock frequency for LVDS interface, DCLK_A		400	MHz
f _{CLOCK}	Clock frequency for LVDS interface, DCLK_B		400	MHz
f _{CLOCK}	Clock frequency for LVDS interface, DCLK_C		400	MHz
f _{CLOCK}	Clock frequency for LVDS interface, DCLK_D		400	MHz
Environmental				
T _{ARRAY} and T _{WINDOW}	Temperature, operating ⁽⁷⁾	0	90	°C
	Temperature, non-operating ⁽⁷⁾	−40	90	°C
T _{DELTA}	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1 ⁽⁸⁾		30	°C
T _{DP}	Dew Point Temperature, operating and non-operating (noncondensing)		81	°C

- (1) All voltages are referenced to common ground V_{SS}. V_{BIAS}, V_{CC}, V_{CCI}, V_{OFFSET}, and V_{RESET} power supplies are all required for proper DMD operation. V_{SS} must also be connected.
- (2) V_{OFFSET} supply transients must fall within specified voltages.
- (3) Exceeding the recommended allowable voltage difference between V_{CC} and V_{CCI} may result in excessive current draw.
- (4) Exceeding the recommended allowable voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
- (5) Exceeding the recommended allowable voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.
- (6) LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
- (7) The highest temperature of the active array (as calculated using セクション 6.6) or of any point along the window edge as defined in 図 6-1. The locations of thermal test points TP2, TP3, TP4 and TP5 in 図 6-1 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point is used.
- (8) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 図 6-1. The window test points TP2, TP3, TP4 and TP5 shown in 図 6-1 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point is be used.

5.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system

		MIN	MAX	UNIT
T _{DMD}	DMD storage temperature	– 40	80	°C
T _{DP-AVG}	Average dew point temperature (non-condensing) ⁽¹⁾		28	°C
T _{DP-MAX}	Elevated dew point temperature range (non-condensing) ⁽²⁾	28	36	°C
CT _{ELR}	Cumulative time in elevated dew point temperature range		24	Months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.

(2) Exposure to dew point temperatures in the elevated range during storage and operation is limited to less than a total cumulative time of CT_{ELR}.

5.3 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by recommended operating conditions. No level of performance is implied when operating the device above or below the limits.

		MIN	NOM	MAX	UNIT
Voltage Supply					
V _{CC}	LVC MOS logic supply voltage ⁽¹⁾	1.65	1.8	1.95	V
V _{CCI}	LVC MOS LVDS Interface supply voltage ⁽¹⁾	1.65	1.8	1.95	V
V _{OFFSET}	Mirror electrode and HVCMOS voltage ^{(1) (2)}	9.5	10	10.5	V
V _{BIAS}	Mirror electrode voltage ⁽¹⁾	17.5	18	18.5	V
V _{RESET}	Mirror electrode voltage ⁽¹⁾	–14.5	–14	–13.5	V
V _{CC} – V _{CCI}	Supply voltage delta (absolute value) ⁽³⁾		0	0.3	V
V _{BIAS} – V _{OFFSET}	Supply voltage delta (absolute value) ⁽⁴⁾			10.5	V
V _{BIAS} – V _{RESET}	Supply voltage delta (absolute value) ⁽⁵⁾			33	V
LVC MOS Interface					
V _{IH(DC)}	DC input high voltage ⁽⁶⁾	0.7 × V _{CC}		V _{CC} + 0.3	V
V _{IL(DC)}	DC input low voltage ⁽⁶⁾	–0.3		0.3 × V _{CC}	V
V _{IH(AC)}	AC input high voltage ⁽⁶⁾	0.8 × V _{CC}		V _{CC} + 0.3	V
V _{IL(AC)}	AC input low voltage ⁽⁶⁾	–0.3		0.2 × V _{CC}	V
t _{PWRDZ}	PWRDZ pulse width ⁽⁷⁾	10			ns
SCP Interface					
f _{SCPCLK}	SCP clock frequency ⁽⁸⁾			500	kHz
t _{SCP_PD}	Propagation delay, clock to Q, from rising edge of SCPCLK to valid SCPDO ⁽⁹⁾	0		900	ns
t _{SCP_NEG_ENZ}	Time between the falling edge of SCPENZ and the first rising edge of SCPCLK	2			μs
t _{SCP_POS_ENZ}	Time between the falling edge of SCPCLK and the rising edge of SCPENZ	2			μs
t _{SCP_DS}	SCPDI clock setup time (before SCPCLK falling edge) ⁽⁹⁾	800			ns

5.4 Recommended Operating Conditions (続き)

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by recommended operating conditions. No level of performance is implied when operating the device above or below the limits.

		MIN	NOM	MAX	UNIT
t _{SCP_DH}	SCPDH hold time (after SCPCLK falling edge) ⁽⁹⁾	900			ns
t _{SCP_PW_ENZ}	SCPENZ inactive pulse width (high level)	2			μs

LVDS Interface

f _{CLOCK}	Clock frequency for LVDS interface (all channels), DCLK ⁽¹⁰⁾			400	MHz
V _{ID}	Input differential voltage (absolute value) ⁽¹¹⁾	150	300	440	mV
V _{CM}	Common mode voltage ⁽¹¹⁾	1100	1200	1300	mV
V _{LVDS}	LVDS voltage ⁽¹¹⁾	880		1520	mV
t _{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			2000	ns
Z _{IN}	Internal differential termination resistance	80	100	120	Ω
Z _{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω

ENVIRONMENTAL

T _{ARRAY}	Array temperature, long-term operational ^{(12) (13) (14) (15) (22)}	10		40 to 70	°C
	Array temperature, short-term operational, 500-hr max ^{(13) (16)}	0		10	°C
T _{WINDOW}	Window temperature – operational ⁽¹⁷⁾			85	°C
T _{DELTA}	Absolute temperature delta between any point on the window edge and the ceramic test point TP1 ⁽¹⁸⁾			14	°C
T _{DP -AVG}	Average dew point temperature (non-condensing) ⁽¹⁹⁾			28	°C
T _{DP-ELR}	Elevated dew point temperature range (non-condensing) ⁽²⁰⁾	28		36	°C
CT _{ELR}	Cumulative time in elevated dew point temperature range			24	Months
ILL _θ	Illumination marginal ray angle ⁽²¹⁾			55	°

SOLID STATE ILLUMINATION

ILL _{UV}	Illumination power < 410 nm ^{(12) (23)}			10	mW/cm ²
ILL _{VIS}	Illumination power ≥ 410 nm and ≤ 800 nm ^{(22) (23)}			22	W/cm ²
ILL _{IR}	Illumination power > 800 nm ⁽²³⁾			10	mW/cm ²
ILL _{BLU}	Illumination power ≥ 410 nm and ≤ 475 nm ^{(22) (23)}			7	W/cm ²
ILL _{BLU1}	Illumination power ≥ 410 nm and ≤ 440 nm ^{(22) (23)}			1.1	W/cm ²

LAMP ILLUMINATION

ILL _{UV}	Illumination power < 395 nm ^{(12) (23)}			2	mW/cm ²
ILL _{VIS}	Illumination power ≥ 395 nm and ≤ 800 nm ^{(22) (23)}			18	W/cm ²
ILL _{IR}	Illumination power > 800 nm ⁽²³⁾			10	mW/cm ²

- (1) All voltages are referenced to common ground VSS. VBIAS, VCC, VCCI, VOFFSET, and VRESET power supplies are all required for proper DMD operation. VSS must also be connected.
- (2) VOFFSET supply transients must fall within specified max voltages.
- (3) To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than specified limit. See セクション 8, 図 8-1, and 表 8-1.
- (4) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit. See セクション 8, 図 8-1, and 表 8-1.
- (5) To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit. See セクション 8, 図 8-1, and 表 8-1.
- (6) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, “Low-Power Double Data Rate (LPDDR)” JESD209B. Tester Conditions for VIH and VIL.
 - Frequency = 60 MHz. Maximum Rise Time = 2.5 ns @ (20% – 80%)
 - Frequency = 60 MHz. Maximum Fall Time = 2.5 ns @ (80% – 20%)
- (7) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tristates the SCPDO output pin.

- (8) The SCP clock is a gated clock. Duty cycle must be $50\% \pm 10\%$. SCP parameter is related to the frequency of DCLK.
- (9) See [図 5-2](#).
- (10) See LVDS Timing Requirements in [セクション 5.8](#) and [図 5-6](#).
- (11) See [図 5-5](#) LVDS Waveform Requirements.
- (12) Simultaneous exposure of the DMD to the maximum [セクション 5.4](#) for temperature and UV illumination reduces device lifetime.
- (13) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point (TP1) shown in [図 6-1](#) and the package thermal resistance using the calculation in [セクション 6.6](#).
- (14) Per [図 5-1](#), the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to [セクション 6.8](#) for a definition of micromirror landed duty cycle.
- (15) Long-term is defined as the usable life of the device.
- (16) Short-term is the total cumulative time over the useful life of the device.
- (17) The locations of thermal test points TP2, TP3, TP4, and TP5 shown in [図 6-1](#) are intended to measure the highest window edge temperature. For most applications, the locations shown are representative of the highest window edge temperature. If a particular application causes additional points on the window edge to be at a higher temperature, test points should be added to those locations.
- (18) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in [図 6-1](#). The window test points TP2, TP3, TP4, and TP5 shown in [図 6-1](#) are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta in temperature, that point should be used.
- (19) The average over time (including storage and operating) that the device is not in the 'elevated dew point temperature range'.
- (20) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR} .
- (21) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including pond of micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document and may negatively affect lifetime.
- (22) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature (T_{ARRAY}).
- (23) To calculate, see the Micromirror Power Density Calculation.

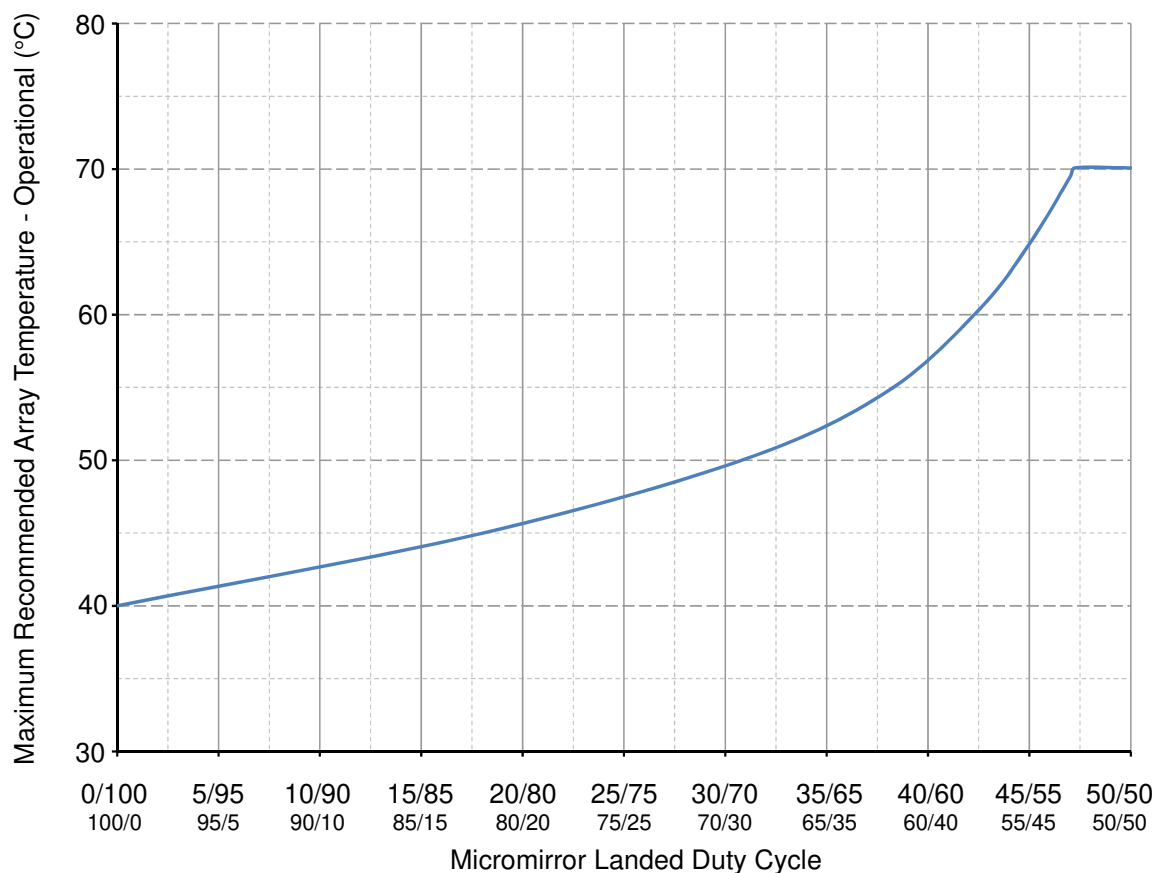


図 5-1. Max Recommended Array Temperature—Derating Curve

5.5 Thermal Information

THERMAL METRIC	DLP660TE	UNIT
	FYG Package	
	350 PINS	
Thermal resistance, active area to test point 1 (TP1) ⁽¹⁾	0.60	°C/W

- (1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the [セクション 5.4](#). The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems need to be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

5.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	High level output voltage V _{CC} = 1.8 V, I _{OH} = – 2 mA	0.8 × V _{CC}			V
V _{OL}	Low level output voltage V _{CC} = 1.95 V, I _{OL} = 2 mA		0.2 × V _{CC}		V
I _{OZ}	High impedance output current V _{CC} = 1.95 V	–40		25	μA
I _{IL}	Low level input current V _{CC} = 1.95 V, V _I = 0	–1			μA
I _{IH}	High level input current ⁽¹⁾ V _{CC} = 1.95 V, V _I = V _{CC}			110	μA
I _{CC}	Supply current VCC V _{CC} = 1.95 V			1200	mA
I _{CCI}	Supply current VCCI V _{CCI} = 1.95 V			330	mA
I _{OFFSET}	Supply current VOFFSET ⁽²⁾ V _{OFFSET} = 10.5 V			13.2	mA
I _{BIAS}	Supply current VBIAS ^{(2) (3)} V _{BIAS} = 18.5 V			–3.641	mA
I _{RESET}	Supply current VRESET ⁽³⁾ V _{RESET} = – 14.5 V			9.02	mA
Supply power dissipation total				3320.25	mW

- (1) Applies to LVCMOS pins only. Excludes LVDS pins and test pad pins.
(2) To prevent excess current, the supply voltage delta |V_{BIAS} – V_{OFFSET}| must be less than the specified limit in [セクション 5.4](#).
(3) To prevent excess current, the supply voltage delta |V_{BIAS} – V_{RESET}| must be less than specified limit in [セクション 5.4](#).

5.7 Capacitance at Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C _{I_lvds}	LVDS Input Capacitance 2xLVDS f = 1 MHz			20	pF
C _{I_nonlvds}	Non-LVDS Input capacitance 2xLVDS f = 1 MHz			20	pF
C _{I_tdiode}	Temp Diode Input capacitance 2xLVDS f = 1 MHz			30	pF
C _O	Output Capacitance f = 1 MHz			20	pF

5.8 Timing Requirements

			MIN	NOM	MAX	UNIT
SCP⁽¹⁾						
t_r	Rise time	20% to 80% reference points			30	ns
t_f	Fall time	80% to 20% reference points			30	ns
LVDS⁽²⁾						
t_r	Rise slew rate	20% to 80% reference points	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points	0.7	1		V/ns
t_C	Clock Cycle	DCLK_A, LVDS pair	2.5			ns
t_C	Clock Cycle	DCLK_B, LVDS pair	2.5			ns
t_C	Clock Cycle	DCLK_C, LVDS pair	2.5			ns
t_C	Clock Cycle	DCLK_D, LVDS pair	2.5			ns
t_W	Pulse Width	DCLK_A LVDS pair	1.19	1.25		ns
t_W	Pulse Width	DCLK_B LVDS pair	1.19	1.25		ns
t_W	Pulse Width	DCLK_C LVDS pair	1.19	1.25		ns
t_W	Pulse Width	DCLK_D LVDS pair	1.19	1.25		ns
t_{Su}	Setup Time	D_A(15:0) before DCLK_A, LVDS pair	0.325			ns
t_{Su}	Setup Time	D_B(15:0) before DCLK_B, LVDS pair	0.325			ns
t_{Su}	Setup Time	D_C(15:0) before DCLK_C, LVDS pair	0.325			ns
t_{Su}	Setup Time	D_D(15:0) before DCLK_D, LVDS pair	0.325			ns
t_{Su}	Setup Time	SCTRL_A before DCLK_A, LVDS pair	0.325			ns
t_{Su}	Setup Time	SCTRL_B before DCLK_B, LVDS pair	0.325			ns
t_{Su}	Setup Time	SCTRL_C before DCLK_C, LVDS pair	0.325			ns
t_{Su}	Setup Time	SCTRL_D before DCLK_D, LVDS pair	0.325			ns
t_h	Hold Time	D_A(15:0) after DCLK_A, LVDS pair	0.145			ns
t_h	Hold Time	D_B(15:0) after DCLK_B, LVDS pair	0.145			ns
t_h	Hold Time	D_C(15:0) after DCLK_C, LVDS pair	0.145			ns
t_h	Hold Time	D_D(15:0) after DCLK_D, LVDS pair	0.145			ns
t_h	Hold Time	SCTRL_A after DCLK_A, LVDS pair	0.145			ns
t_h	Hold Time	SCTRL_B after DCLK_B, LVDS pair	0.145			ns
t_h	Hold Time	SCTRL_C after DCLK_C, LVDS pair	0.145			ns
t_h	Hold Time	SCTRL_D after DCLK_D, LVDS pair	0.145			ns
LVDS⁽²⁾						
t_{SKEW}	Skew Time	Channel B relative to Channel A ⁽³⁾ ⁽⁴⁾ , LVDS pair	-1.25		+1.25	ns
t_{SKEW}	Skew Time	Channel D relative to Channel C ⁽⁵⁾ ⁽⁶⁾ , LVDS pair	-1.25		+1.25	ns

(1) See [Figure 5-3](#) for Rise Time and Fall Time for SCP.

(2) See [Figure 5-5](#) for Timing Requirements for LVDS.

(3) Channel A (Bus A) includes the following LVDS pairs: DCLK_AN and DCLK_AP, SCTRL_AN and SCTRL_AP, D_AN(15:0) and D_AP(15:0).

(4) Channel B (Bus B) includes the following LVDS pairs: DCLK_BN and DCLK_BP, SCTRL_BN and SCTRL_BP, D_BN(15:0) and D_BP(15:0).

(5) Channel C (Bus C) includes the following LVDS pairs: DCLK_CN and DCLK_CP, SCTRL_CN and SCTRL_CP, D_CN(15:0) and D_CP(15:0).

(6) Channel D (Bus D) includes the following LVDS pairs: DCLK_DN and DCLK_DP, SCTRL_DN and SCTRL_DP, D_DN(15:0) and D_DP(15:0).

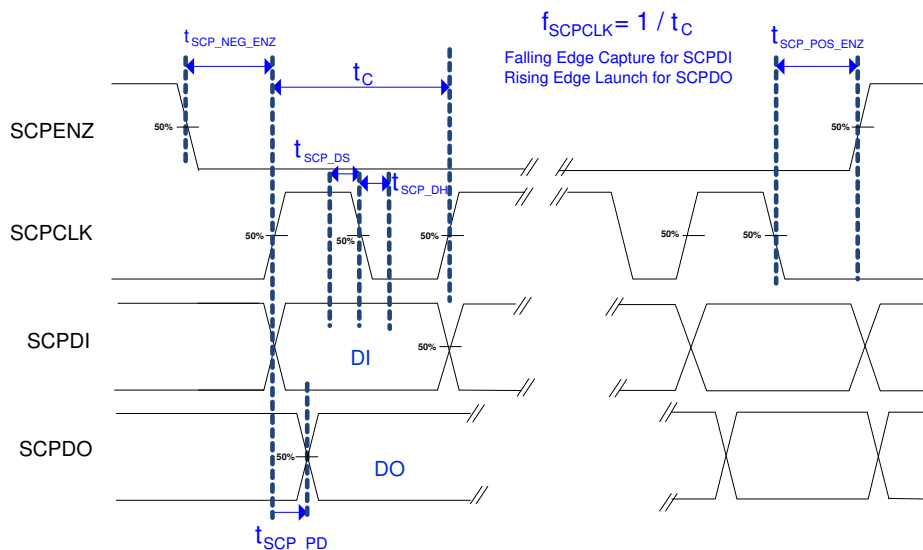


図 5-2. SCP Timing Requirements

See セクション 5.4 for f_{SCPCLK} , t_{SCP_DS} , t_{SCP_DH} , and t_{SCP_PD} specifications.

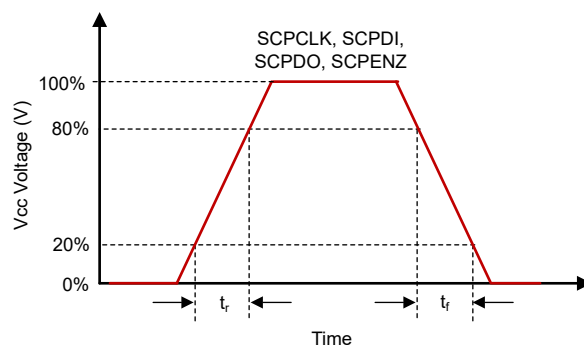


図 5-3. SCP Requirements for Rise and Fall

See セクション 5.8 for t_r and t_f specifications and conditions.

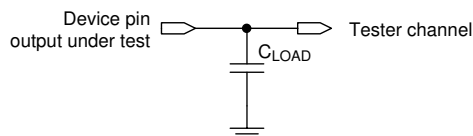


図 5-4. Test Load Circuit for Output Propagation Measurement

For output timing analysis, the tester pin electronics and its transmission line effects must be considered. System designers use IBIS or other simulation tools to correlate the timing reference load to a system environment.

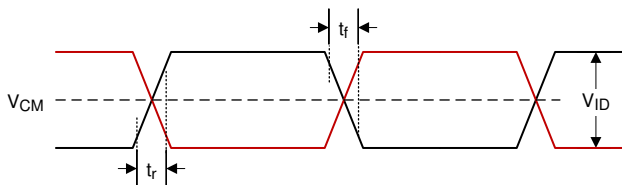


図 5-5. LVDS Waveform Requirements

A. See 式 1 and 式 2.

$$V_{LVDS(max)} = V_{CM(max)} + \left| \frac{1}{2} \times V_{ID(max)} \right| \quad (1)$$

$$V_{LVDS(min)} = V_{CM(min)} - \left| \frac{1}{2} \times V_{ID(max)} \right| \quad (2)$$

See セクション 5.4 for V_{CM} , V_{ID} , and V_{LVDS} specifications and conditions.

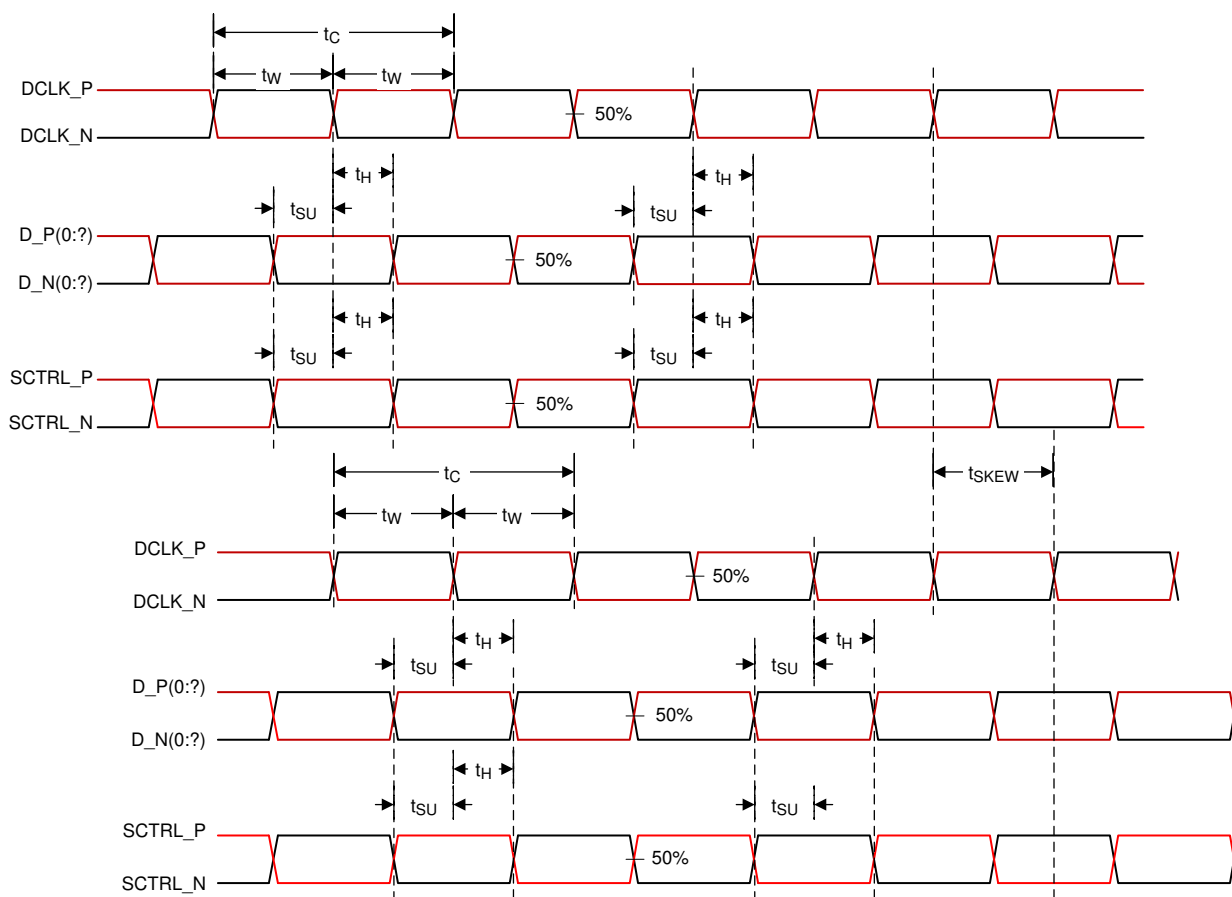


図 5-6. Timing Requirements

See セクション 5.8 for timing requirements and LVDS pairs per channel (bus) defining D_P(0:?) and D_N(0:?).

5.9 System Mounting Interface Loads

表 5-1. System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
When loads are applied on both electrical and thermal interface areas				
Maximum load to be applied to the electrical interface area ⁽¹⁾			111	N
Maximum load to be applied to the thermal interface area ⁽¹⁾			111	N
When load is applied on the electrical interface areas only				
Maximum load to be applied to the electrical interface area ⁽¹⁾			222	N
Maximum load to be applied to the thermal interface area ⁽¹⁾			0	N

(1) The load must be uniformly applied in the corresponding areas shown in 図 5-7.

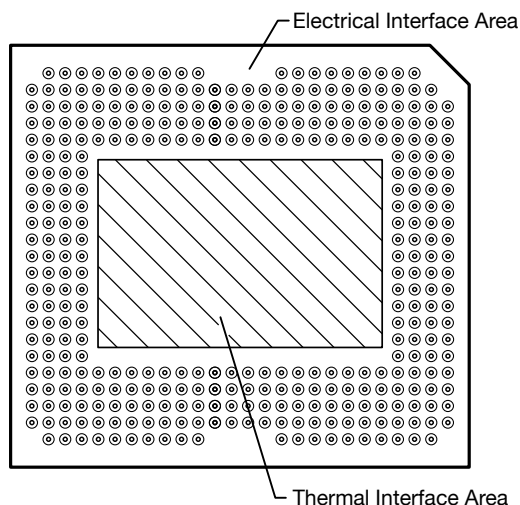


図 5-7. System Mounting Interface Loads

5.10 Micromirror Array Physical Characteristics

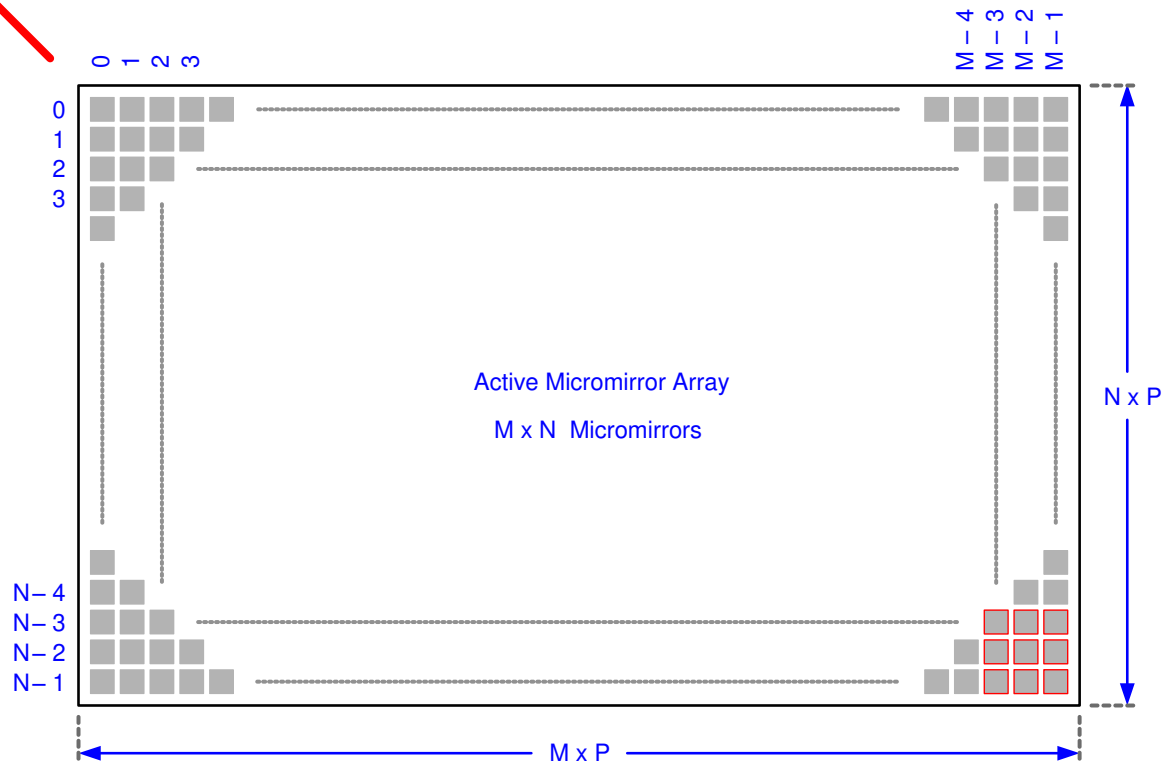
表 5-2. Micromirror Array Physical Characteristics

PARAMETER	DESCRIPTION	VALUE	UNIT
M	Number of active columns ⁽¹⁾	2716	micromirrors
N	Number of active rows ⁽¹⁾	1528	micromirrors
P	Micromirror (pixel) pitch ⁽¹⁾	5.4	μm
Micromirror active array width ⁽¹⁾	Micromirror pitch x number of active columns	14.67	mm
Micromirror active array height ⁽¹⁾	Micromirror pitch x number of active rows	8.25	mm
Micromirror active border (Top / Bottom) ⁽²⁾	Pond of micromirror (POM)	56	micromirrors / side
Micromirror active border (Right / Left) ⁽²⁾	Pond of micromirror (POM)	20	micromirrors / side

(1) See 図 5-8.

(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the “Pond Of Mirrors” (POM). These micromirrors are prevented from tilting toward the bright or “on” state but still require an electrical bias to tilt toward “off.”

Off-State
Light Path

Incident
Illumination
Light Path



Pond Of Micromirrors (POM) omitted for clarity.

Details omitted for clarity. Not to scale.

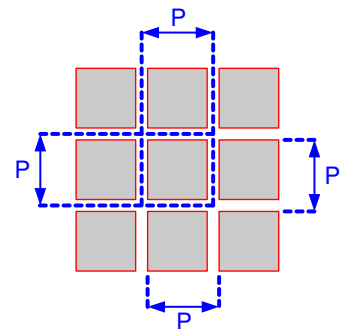


図 5-8. Micromirror Array Physical Characteristics

Refer to [セクション 5.10](#) for M, N, and P specifications.

5.11 Micromirror Array Optical Characteristics

表 5-3. Micromirror Array Optical Characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Micromirror tilt angle ^{(2) (3) (4) (5)}	Landed state ⁽¹⁾	15.6	17.0	18.4	degrees
	Micromirror crossover time ⁽⁶⁾	typical performance		1		μs
	Micromirror switching time ⁽⁷⁾	typical performance	6			μs
	DMD Efficiency (420 nm — 680 nm) ⁽⁸⁾			68		%
Image performance ⁽⁹⁾	Bright pixel(s) in active area ⁽¹⁰⁾	Gray 10 screen ⁽¹³⁾			0	micromirrors
	Bright pixel(s) in the POM ^{(10) (12)}	Gray 10 screen ⁽¹³⁾			2	
	Dark pixel(s) in the active area ⁽¹¹⁾	White screen ⁽¹⁴⁾			8	
	Adjacent pixel(s) ⁽¹⁵⁾	Any screen			0	
	Unstable pixel(s) in active area ⁽¹⁶⁾	Any screen			0	

- (1) Measured relative to the plane formed by the overall micromirror array.
- (2) Additional variation exists between the micromirror array and the package datums.
- (3) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
- (4) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
- (5) See [Figure 5-9](#).
- (6) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
- (7) The minimum time between successive transitions of a micromirror.
- (8) Efficiency numbers assume 34-degree illumination angle, F/1.7 illumination and collection cones, uniform source spectrum, and uniform pupil illumination. Efficiency numbers assume 100% electronic micromirror duty cycle and do not include optical overfill loss. The efficiency is a photopically-weighted number corresponding to 17.5-degree tilt angle. Note that this number is specified under conditions described above and deviations from the specified conditions could result in decreased efficiency.
- (9) Conditions of Acceptance: all DMD image performance returns are evaluated using the following projected image test conditions:
Test set degamma shall be linear.
Test set brightness and contrast shall be set to nominal.
The diagonal size of the projected image shall be a minimum of 60 inches.
The projections screen shall be 1× gain.
The projected image shall be inspected from an 8-foot minimum viewing distance.
The image shall be in focus during all image performance tests.
- (10) Bright pixel definition: a single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels.
- (11) Dark pixel definition: a single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels.
- (12) POM definition: rectangular border of off-state mirrors surrounding the active area.
- (13) Gray 10 screen definition: a full screen with RGB values set to R = 10/255, G = 10/255, B = 10/255
- (14) White screen definition: a full screen with RGB values set to R=255/255, G = 255/255, B = 255/255
- (15) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster.
- (16) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

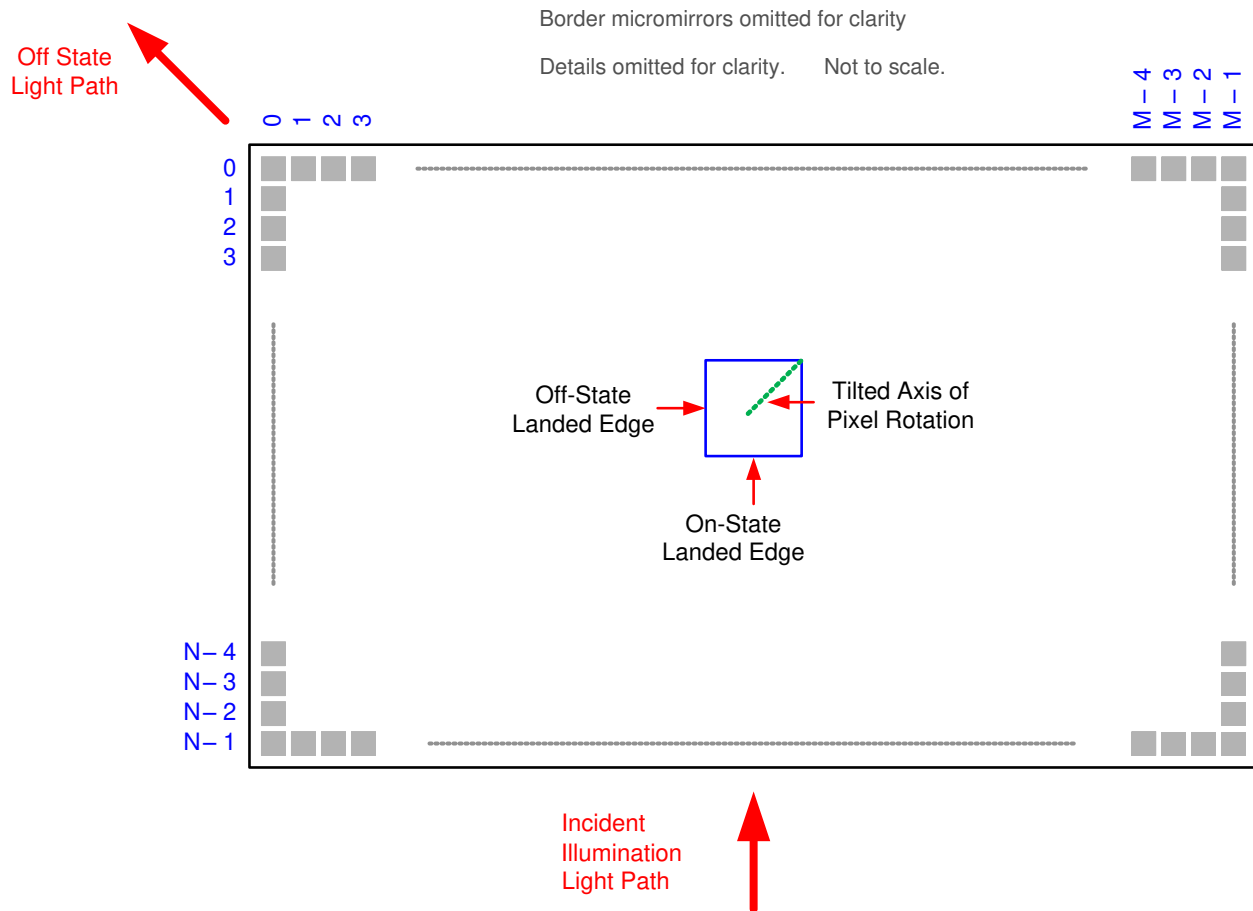


図 5-9. Micromirror Landed Orientation and Tilt

Refer to [セクション 5.10](#) for M, N, and P specifications.

5.12 Window Characteristics

表 5-4. DMD Window Characteristics

PARAMETER	MIN	NOM	MAX	UNIT
Window material		Corning Eagle XG		
Window refractive index at 546.1 nm		1.5119		
Window transmittance, minimum within the wavelength range 420–680 nm. Applies to all angles 0°–30° AOI ^{(1) (2)}	97%			
Window Transmittance, average over the wavelength range 420–680 nm. Applies to all angles 30°–45° AOI. ^{(1) (2)}	97%			

(1) Single-pass through both surfaces and glass

(2) AOI—angle of incidence is the angle between an incident ray and the normal to a reflecting or refracting surface.

5.13 Chipset Component Usage Specification

Reliable function and operation of the DLP660TE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

6 Detailed Description

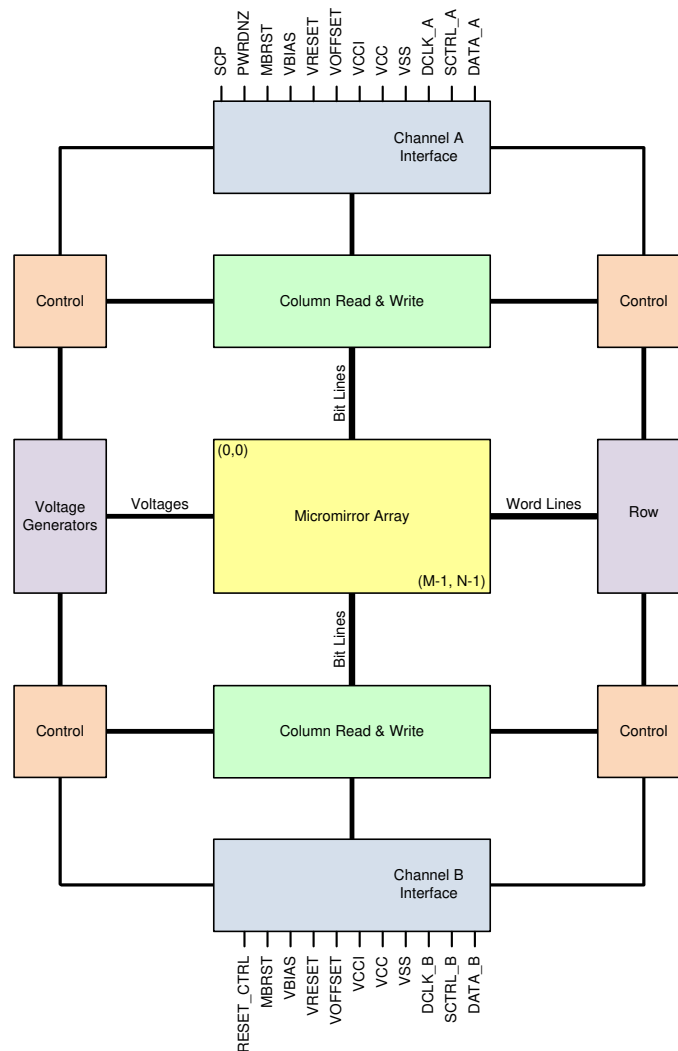
6.1 Overview

The DMD is a 0.66-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is low voltage differential signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to [セクション 6.2](#). The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP660TE DMD is part of the chipset comprising of the DLP660TE DMD, the DLPC4420 display controller and the DLPA100 power and motor driver. For reliable operation, the DLP660TE DMD must always be used with the DLPC4420 display controller and the DLPA100 power and motor driver.

6.2 Functional Block Diagram

Not to Scale. Details Omitted for Clarity. See Accompanying Notes in this Section.



For pin details on Channels A, B, C, and D, refer to [セクション 4](#) and the LVDS Interface section of [セクション 5.8](#). RESET_CTRL is used in applications when an external reset signal is required.

6.3 Feature Description

6.3.1 Power Interface

The DMD requires 5 DC voltages: DMD_P3P3V, DMD_P1P8V, VOFFSET, VRESET, and VBIAS. DMD_P3P3V is created by the DLPA100 power and motor driver and is used on the DMD board to create the other 4 DMD voltages, as well as powering various peripherals (TMP411, I2C, and TI level translators). DMD_P1P8V is created by the TI PMIC LP38513S and provides the VCC voltage required by the DMD. VOFFSET (10V), VRESET (-14V), and VBIAS(18V) are made by the TI PMIC TPS65145 and are supplied to the DMD to control the micromirrors.

6.3.2 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered.  5-4 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

6.4 Device Functional Modes

DMD functional modes are controlled by the DLPC4420 display controller. See the DLPC4420 display controller data sheet or contact a TI applications engineer.

6.5 Optical Interface and System Image Quality Considerations

6.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

6.5.1.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area are the same. This angle cannot exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and active area can occur.

6.5.1.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

6.5.1.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

6.6 Micromirror Array Temperature Calculation

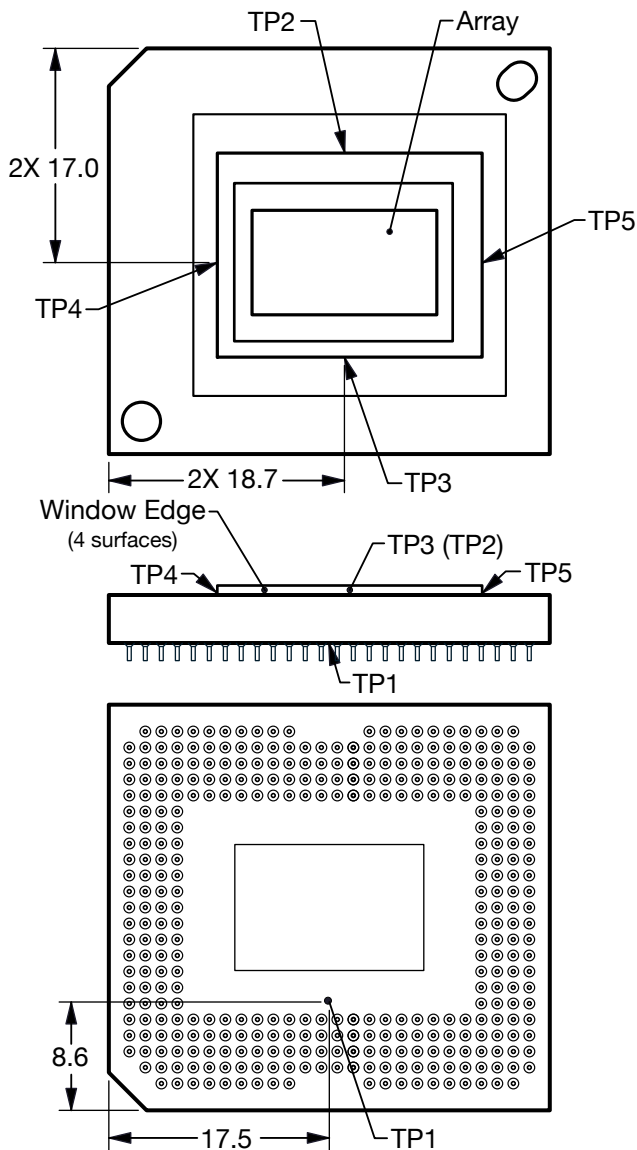


図 6-1. DMD Thermal Test Points

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from a measurement point on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The following equations show the relationship between array temperature and the reference ceramic temperature, thermal test TP1, shown above:

$$T_{\text{ARRAY}} = T_{\text{CERAMIC}} + (Q_{\text{ARRAY}} \times R_{\text{ARRAY-TO-CERAMIC}}) \quad (3)$$

$$Q_{\text{ARRAY}} = Q_{\text{ELECTRICAL}} + Q_{\text{ILLUMINATION}} \quad (4)$$

where

- T_{ARRAY} = Computed array temperature (°C)
- T_{CERAMIC} = Measured ceramic temperature (°C) (TP1 location)
- $R_{\text{ARRAY-TO-CERAMIC}}$ = Thermal resistance of package specified in [セクション 5.5](#) from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{\text{ELECTRICAL}}$ = Nominal electrical power (W)
- Q_{INCIDENT} = Incident illumination optical power (W)
- $Q_{\text{ILLUMINATION}}$ = (DMD average thermal absorptivity $\times$ Q_{INCIDENT}) (W)
- DMD average thermal absorptivity = 0.40

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 3.0 W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single chip or multichip DMD system. It assumes an illumination distribution of 83.7% on the active array, and 16.3% on the array border.

The sample calculation for a typical projection application is as follows

$$Q_{\text{INCIDENT}} = 30 \text{ W (measured)}$$

$$T_{\text{CERAMIC}} = 55.0 \text{ °C (measured)}$$

$$Q_{\text{ELECTRICAL}} = 3.0 \text{ W}$$

$$Q_{\text{ARRAY}} = 3.0 \text{ W} + (0.40 \times 30 \text{ W}) = 15.0 \text{ W}$$

$$T_{\text{ARRAY}} = 55.0 \text{ °C} + (15.0 \text{ W} \times 0.6 \text{ °C/W}) = 64.0 \text{ °C}$$

6.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{UV} = [OP_{UV-RATIO} \times Q_{INCIDENT}] \times 1000 \div A_{ILL} \text{ (mW/cm}^2\text{)}$
- $ILL_{VIS} = [OP_{VIS-RATIO} \times Q_{INCIDENT}] \div A_{ILL} \text{ (W/cm}^2\text{)}$
- $ILL_{IR} = [OP_{IR-RATIO} \times Q_{INCIDENT}] \times 1000 \div A_{ILL} \text{ (mW/cm}^2\text{)}$
- $ILL_{BLU} = [OP_{BLU-RATIO} \times Q_{INCIDENT}] \div A_{ILL} \text{ (W/cm}^2\text{)}$
- $ILL_{BLU1} = [OP_{BLU1-RATIO} \times Q_{INCIDENT}] \div A_{ILL} \text{ (W/cm}^2\text{)}$
- $A_{ILL} = A_{ARRAY} \div (1 - OV_{ILL}) \text{ (cm}^2\text{)}$

where:

- ILL_{UV} = UV illumination power density on the DMD (mW/cm²)
- ILL_{VIS} = VIS illumination power density on the DMD (W/cm²)
- ILL_{IR} = IR illumination power density on the DMD (mW/cm²)
- ILL_{BLU} = BLU illumination power density on the DMD (W/cm²)
- ILL_{BLU1} = BLU1 illumination power density on the DMD (W/cm²)
- A_{ILL} = illumination area on the DMD (cm²)
- $Q_{INCIDENT}$ = total incident optical power on DMD (W) (measured)
- A_{ARRAY} = area of the array (cm²) (data sheet)
- OV_{ILL} = percent of total illumination on the DMD outside the array (%) (optical model)
- $OP_{UV-RATIO}$ = ratio of the optical power for wavelengths <410 nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{VIS-RATIO}$ = ratio of the optical power for wavelengths ≥410 and ≤800 nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{IR-RATIO}$ = ratio of the optical power for wavelengths >800 nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU-RATIO}$ = ratio of the optical power for wavelengths ≥410 and ≤475 nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU1-RATIO}$ = ratio of the optical power for wavelengths ≥410 and ≤440 nm to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array (OV_{ILL}) and the percent of the total illumination that is on the active array. From these values the illumination area (A_{ILL}) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation:

$$Q_{\text{INCIDENT}} = 30 \text{ W (measured)} \quad (5)$$

$$A_{\text{ARRAY}} = (14.6664 \text{ mm} \times 8.2512 \text{ mm}) \div 100 = 1.2102 \text{ cm}^2 \text{ (data sheet)} \quad (6)$$

$$OV_{\text{ILL}} = 16.3\% \text{ (optical model)} \quad (7)$$

$$OP_{\text{UV-RATIO}} = 0.00017 \text{ (spectral measurement)} \quad (8)$$

$$OP_{\text{VIS-RATIO}} = 0.99977 \text{ (spectral measurement)} \quad (9)$$

$$OP_{\text{IR-RATIO}} = 0.00006 \text{ (spectral measurement)} \quad (10)$$

$$OP_{\text{BLU-RATIO}} = 0.28100 \text{ (spectral measurement)} \quad (11)$$

$$OP_{\text{BLU1-RATIO}} = 0.03200 \text{ (spectral measurement)} \quad (12)$$

$$A_{\text{ILL}} = 1.2102 \text{ cm}^2 \div (1 - 0.163) = 1.4458 \text{ cm}^2 \quad (13)$$

$$ILL_{\text{UV}} = [0.00017 \times 30 \text{ W}] \times 1000 \div 1.4458 \text{ cm}^2 = 3.527 \text{ mW/cm}^2 \quad (14)$$

$$ILL_{\text{VIS}} = [0.99977 \times 30 \text{ W}] \div 1.4458 \text{ cm}^2 = 20.74 \text{ W/cm}^2 \quad (15)$$

$$ILL_{\text{IR}} = [0.00006 \times 30 \text{ W}] \times 1000 \div 1.4458 \text{ cm}^2 = 1.245 \text{ mW/cm}^2 \quad (16)$$

$$ILL_{\text{BLU}} = [0.28100 \times 30 \text{ W}] \div 1.4458 \text{ cm}^2 = 5.83 \text{ W/cm}^2 \quad (17)$$

$$ILL_{\text{BLU1}} = [0.03200 \times 30 \text{ W}] \div 1.4458 \text{ cm}^2 = 0.66 \text{ W/cm}^2 \quad (18)$$

6.8 Micromirror Landed-On/Landed-Off Duty Cycle

6.8.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On state versus the amount of time the same micromirror is landed in the Off state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On state 100% of the time (and in the Off state 0% of the time); whereas 0/100 indicates that the pixel is in the Off state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

6.8.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry or asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

6.8.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life. This is quantified in the de-rating curve shown in [図 5-1](#). The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature that the DMD ideally will be operated at for a given long-term average Landed Duty Cycle.

6.8.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in [表 6-1](#).

表 6-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

$$\text{Landed Duty Cycle} = (\text{Red_Cycle_}\% \times \text{Red_Scale_Value}) + (\text{Green_Cycle_}\% \times \text{Green_Scale_Value}) + (\text{Blue_Cycle_}\% \times \text{Blue_Scale_Value})$$

where

- Red_Cycle_% represents the percentage of the frame time that Red displays to achieve the desired white point.
- Green_Cycle_% represents the percentage of the frame time that Green displays to achieve the desired white point.
- Blue_Cycle_% represents the percentage of the frame time that Blue displays to achieve the desired white point.

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities will be as shown in 表 6-2 and 表 6-3.

表 6-2. Example Landed Duty Cycle for Full-Color, Color Percentage

Red Cycle Percentage	Green Cycle Percentage	Blue Cycle Percentage
50%	20%	30%

表 6-3. Example Landed Duty Cycle for Full-Color

Red Scale Value	Green Scale Value	Blue Scale Value	Landed Duty Cycle
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

Texas Instruments DLP technology is a micro-electro-mechanical systems (MEMS) technology that modulates light using a digital micromirror device (DMD). DMDs vary in resolution and size and can contain over 8-million micromirrors. Each micromirror of a DMD can represent either one or more pixels on the display and is independently controlled, synchronized with color sequential illumination, to create stunning images on any surface. DLP technology enables a wide variety of display products worldwide, from tiny projection modules embedded in smartphones to high powered digital cinema projectors, and emerging display products such as digital signage and laser TV.

The most recent class of chipsets from Texas Instruments is based on a breakthrough micromirror technology, called TRP. With a smaller pixel pitch of 5.4 μm and increased tilt angle of 17 degrees, TRP chipsets enable higher resolution in a smaller form factor and enhanced image processing features while maintaining high optical efficiency. DLP chipsets are a great fit for any system that requires high resolution and high brightness displays.

The following orderables have been replaced by the DLP660TE.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)	MECHANICAL ICD
2715-7132P	FYG (350)	35 mm × 32 mm	2514366
2715-7137P	FYG (350)	35 mm × 32 mm	2514366
2715-7139P	FYG (350)	35 mm × 32 mm	2514366
2715-713AP	FYG (350)	35 mm × 32 mm	2514366

7.2 Typical Application

The DLP660TE DMD is the first full 4K UHD DLP digital micromirror device. When combined with two display controllers (DLPC4420), an FPGA, a power management device (DLPA100), and other electrical, optical and mechanical components the chipset enables bright, affordable, full 4K UHD display solutions. [Figure 7-1](#) and [Figure 7-2](#) shows a typical 4K UHD system application using the DLP660TE DMD.

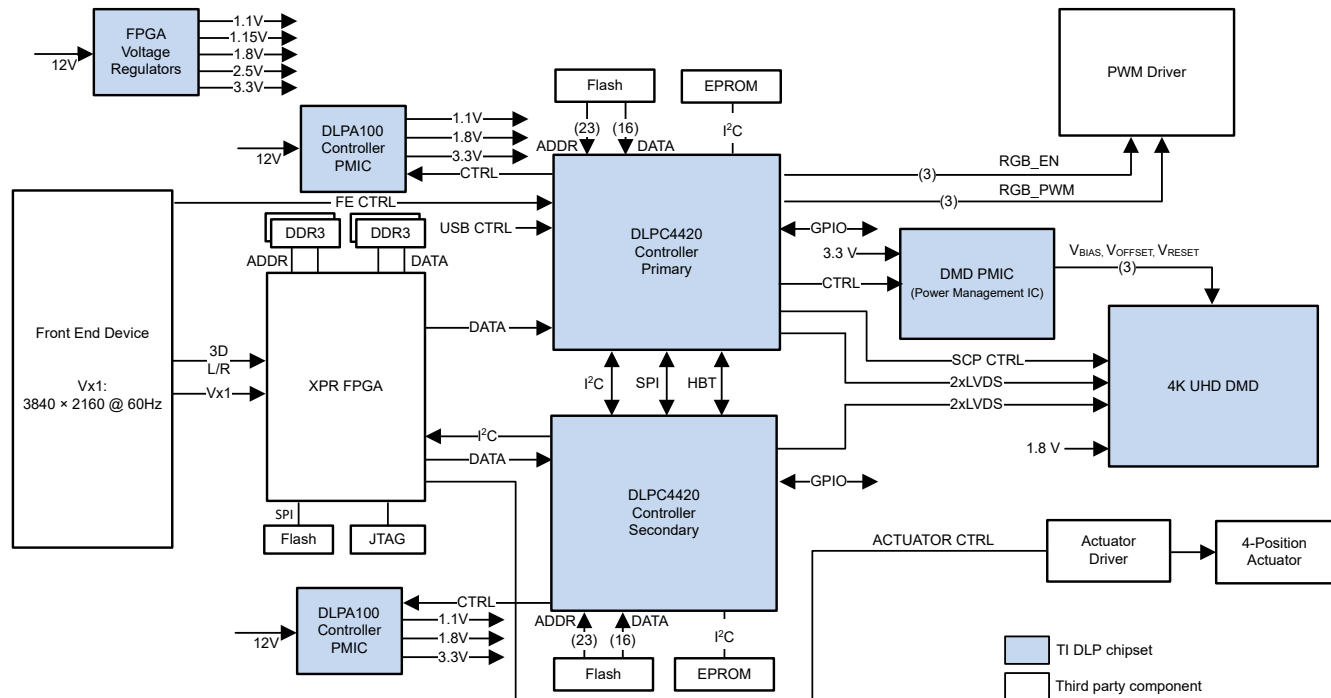
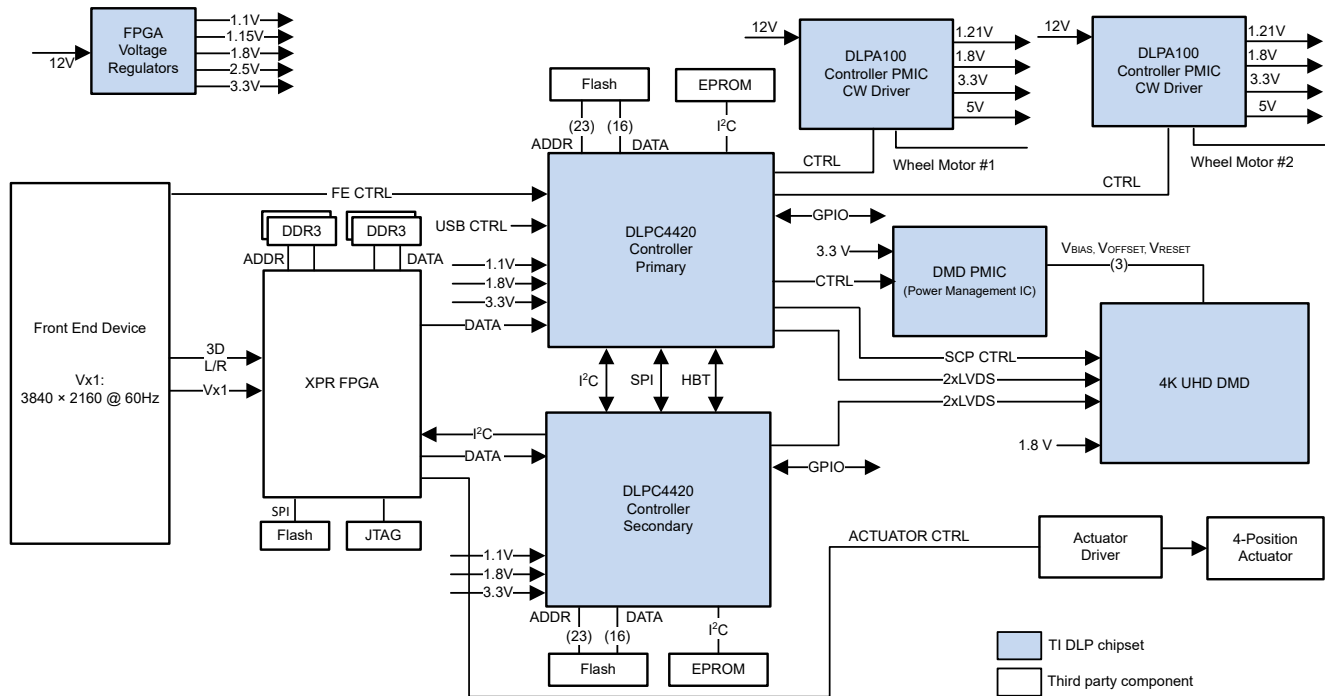


Figure 7-1. Typical DLPC4420 4K UHD LED Illumination Application



7-2. Typical DLPC4420 4K UHD Laser Phosphor Illumination Application

7.2.1 Design Requirements

At the high level, DLP660TE DMD systems will include an illumination source, a light engine, electronic components, and software. The designer must first choose an illumination source and design the optical engine taking into consideration the relationship between the optics and the illumination source. The designer must then understand the electronic components of a DLP660TE DMD system, which is made up of a DMD board and formatter board. The DMD board channels image data to and powers the DMD chip. The formatter board supports the rest of the electronic components, which can include an FPGA, the DLPC4420 display controller, power supplies, and drivers for illumination sources, color wheels, fans, and dynamic optical components.

7.2.2 Detailed Design Procedure

For connecting the DLPC4420 display controller and the DLP660TE DMD, see the reference design schematic. Follow the layout guidelines to achieve a reliable projector. To complete the DLP system, an optical module or light engine is required that contains the DLP660TE DMD, associated illumination sources, optical elements, and necessary mechanical components.

7.2.3 Application Curves

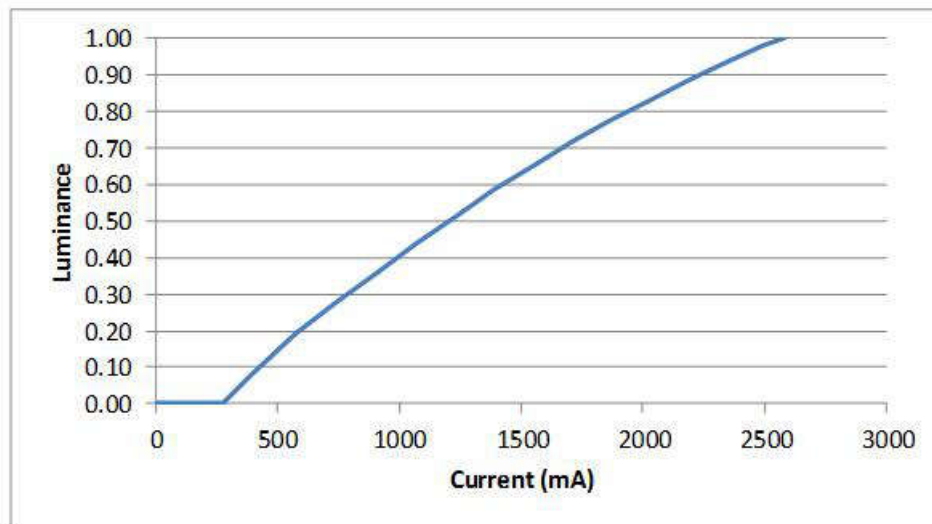
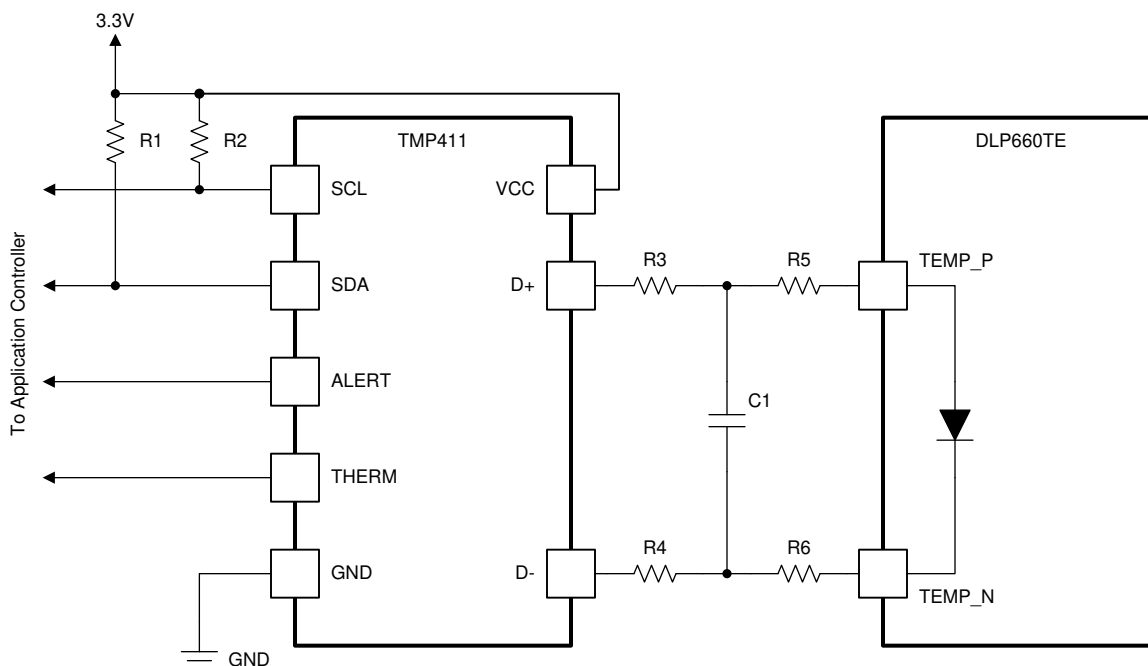


図 7-3. Luminance vs. Current

7.3 DMD Die Temperature Sensing

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The thermal diode can be interfaced with the TMP411 temperature sensor as shown in [図 7-4](#). The serial bus from the TMP411 can be connected to the DLPC4420 display controller to enable its temperature sensing features. See the DLPC4420 Programmers' Guide for instructions on installing the DLPC4420 controller support firmware bundle and obtaining the temperature readings.

The software application contains functions to configure the TMP411 to read the DMD temperature sensor diode. This data can be leveraged to incorporate additional functionality in the overall system design such as adjusting illumination, fan speeds, and so forth. All communication between the TMP411 and the DLPC4420 controller will be completed using the I²C interface. The TMP411 connects to the DMD via pins E16 and E17 as outlined in [セクション 4](#).



- A. Details omitted for clarity, see the [TI Reference Design](#) for connections to the DLPC4420 controller.
- B. See the [TMP411](#) data sheet for system board layout recommendation.
- C. See the [TMP411](#) data sheet and the TI reference design for suggested component values for R1, R2, R3, R4, and C1.
- D. R5 = 0 Ω. R6 = 0 Ω. Zero ohm resistors need to be located close to the DMD package pins.

図 7-4. TMP411 Sample Schematic

8 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- VSS
- VCC
- VCCI
- VBIAS
- VOFFSET
- VRESET

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

注意

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See [図 8-1](#) DMD Power Supply Sequencing Requirements.

VBIAS, VCC, VCCI, VOFFSET, and VRESET power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. Common ground VSS must also be connected.

8.1 DMD Power Supply Power-Up Procedure

- During power-up, VCC and VCCI must always start and settle before VOFFSET plus Delay1 specified in [表 8-1](#), VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage delta between VBIAS and VOFFSET must be within the specified limit shown in [セクション 5.4](#).
- During power-up, there is no requirement for the relative timing of VRESET with respect to VBIAS.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in [セクション 5.1](#), in [セクション 5.4](#), and in [図 8-1](#).
- During power-up, LVCMOS input pins must not be driven high until after VCC and VCCI have settled at operating voltages listed in [セクション 5.4](#).

8.2 DMD Power Supply Power-Down Procedure

- During power-down, VCC and VCCI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within the specified limit of ground. See [表 8-1](#).
- During power-down, it is a strict requirement that the voltage delta between VBIAS and VOFFSET must be within the specified limit shown in [セクション 5.4](#).
- During power-down, there is no requirement for the relative timing of VRESET with respect to VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in [セクション 5.1](#), in [セクション 5.4](#), and in [図 8-1](#).
- During power-down, LVCMOS input pins must be less than specified in [セクション 5.4](#).

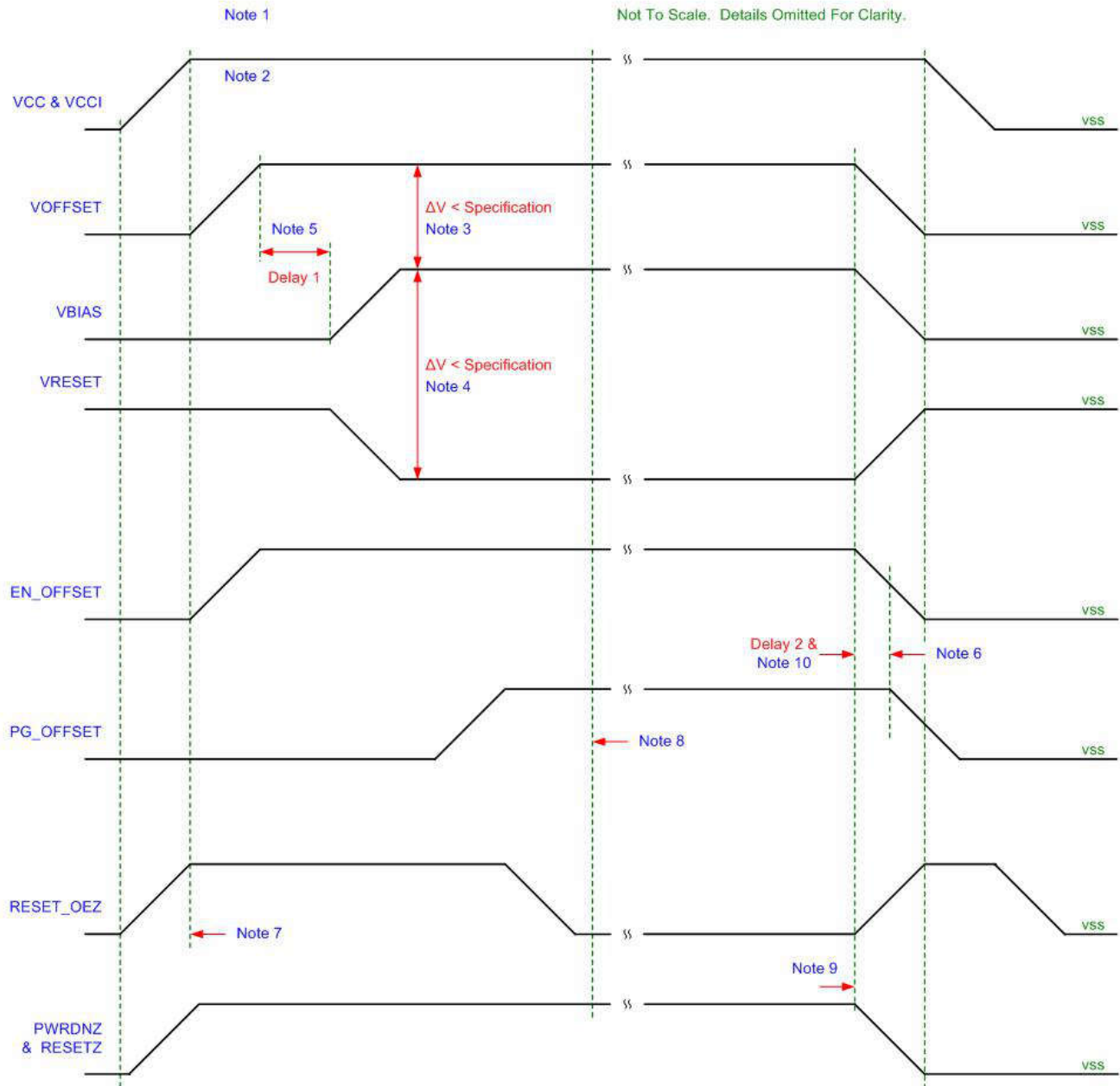


図 8-1. DMD Power Supply Requirements

1. See セクション 4 and セクション 5.4.
2. To prevent excess current, the supply voltage delta $|VCCI - VCC|$ must be less than specified limit in セクション 5.4.
3. To prevent excess current, the supply voltage delta $|VBIAS - VOFFSET|$ must be less than specified in セクション 5.4.
4. To prevent excess current, the supply voltage delta $|VBIAS - VRESET|$ must be less than specified limit in セクション 5.4.
5. VBIAS must power up after VOFFSET has powered up, per the Delay1 specification in 表 8-1.
6. PG_OFFSET must turn off after EN_OFFSET has turned off, per the Delay2 specification in 表 8-1.
7. DLP controller software enables the DMD power supplies to turn on after RESET_OEZ is at logic high.
8. DLP controller software initiates the global VBIAS command.

9. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates PWRDNZ and disables VBIAS, VRESET and VOFFSET.
10. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware, EN_OFFSET may turn off after PG_OFFSET has turned off. The OEZ signal goes high prior to PG_OFFSET turning off to indicate the DMD micromirror has completed the emergency park procedures.

表 8-1. DMD Power-Supply Requirements

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
Delay1	Delay from VOFFSET settled at recommended operating voltage to VBIAS and VRESET power up	1	2		ms
Delay2	PG_OFFSET hold time after EN_OFFSET goes low	100			ns

9 Layout

9.1 Layout Guidelines

The DLP660TE DMD is part of a chipset that is controlled by the DLPC4420 display controller in conjunction with the DLPA100 power and motor driver. These guidelines help to design a PCB board with the DLP660TE DMD. The DLP660TE DMD board is a high-speed multilayer PCB, with primarily high-speed digital logic using dual-edge clock rates up to 400 MHz for DMD LVDS signals. The remaining traces are comprised of low speed digital LVTTTL signals. TI recommends that mini power planes are used for VOFFSET, VRESET, and VBIAS. Solid planes are required for DMD_P3P3V(3.3 V), DMD_P1P8V, and Ground. The target impedance for the PCB is 50 Ω $\pm$ 10% with the LVDS traces being 100- Ω $\pm$ 10% differential. TI recommends using an 8-layer stack-up as described in 表 9-1.

9.2 Layout Example

9.2.1 Layers

The layer stack-up and copper weight for each layer is shown in 表 9-1. Small sub-planes are allowed on signal routing layers to connect components to major sub-planes on top or bottom layers if necessary.

表 9-1. Layer Stack-Up

LAYER NO.	LAYER NAME	COPPER WT. (oz.)	COMMENTS
1	Side A - DMD only	1.5	DMD, escapes, low frequency signals, power sub-planes.
2	Ground	1	Solid ground plane (net GND).
3	Signal	0.5	50 Ω and 100 Ω differential signals
4	Ground	1	Solid ground plane (net GND)
5	DMD_P3P3V	1	+3.3-V power plane (net DMD_P3P3V)
6	Signal	0.5	50 Ω and 100 Ω differential signals
7	Ground	1	Solid ground plane (net GND).
8	Side B - All other Components	1.5	Discrete components, low frequency signals, power sub-planes

9.2.2 Impedance Requirements

TI recommends that the board has matched impedance of 50 Ω $\pm$ 10% for all signals. The exceptions are listed in 表 9-2.

表 9-2. Special Impedance Requirements

SIGNAL TYPE	SIGNAL NAME	IMPEDANCE (Ω)
A channel LVDS differential pairs	D_AP(0:15), D_AN(0:15)	100 $\pm$ 10% differential across each pair
	DCLKA_P, DCLKA_N	
	SCTRL_AP, SCTRL_AN	
B channel LVDS differential pairs	D_BP(0:15), D_BN(0:15)	100 $\pm$ 10% differential across each pair
	DCLKB_P, DCLKB_N	
	SCTRL_BP, SCTRL_BN	
C channel LVDS differential pairs	D_CP(0:15), D_CN(0:15)	100 $\pm$ 10% differential across each pair
	DCLKC_P, DCLKC_N	
	SCTRL_CP, SCTRL_CN	
D channel LVDS differential pairs	D_DP(0:15), D_DN(0:15)	100 $\pm$ 10% differential across each pair
	DCLKD_P, DCLKD_N	
	SCTRL_DP, SCTRL_DN	

9.2.3 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005-inch/0.005-inch design rule. Minimum trace clearance from the ground ring around the PWB has a 0.1-inch minimum. An analysis of impedance and stack-up requirements determine the actual trace widths and clearances.

9.2.3.1 Voltage Signals

表 9-3. Special Trace Widths, Spacing Requirements

SIGNAL NAME	MINIMUM TRACE WIDTH TO PINS (MIL)	LAYOUT REQUIREMENT
GND	15	Maximize trace width to connecting pin
DMD_P3P3V	15	Maximize trace width to connecting pin
DMD_P1P8V	15	Maximize trace width to connecting pin
VOFFSET	15	Create mini plane from U2 to U3
VRESET	15	Create mini plane from U2 to U3
VBIAS	15	Create mini plane from U2 to U3
All U3 control connections	10	Use 10 mil etch to connect all signals/voltages to DMD pads

10 Device and Documentation Support

10.1 サード・パーティ製品に関する免責事項

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10.2 Device Support

10.2.1 Device Nomenclature

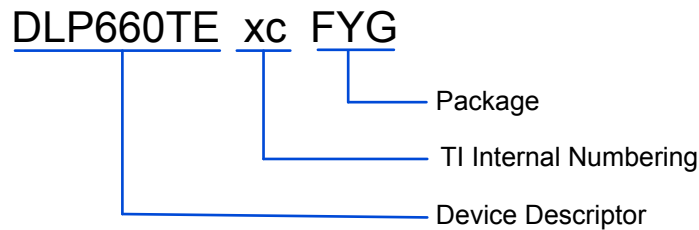


図 10-1. Part Number Description

10.2.2 Device Markings

The device marking will include both human-readable information and a 2-dimensional matrix code. . The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, Part 1 of Serial Number, and Part 2 of Serial Number. The first character of the DMD Serial Number (part 1) is the manufacturing year. The second character of the DMD Serial Number (part 1) is the manufacturing month. The last character of the DMD Serial Number (part 2) is the bias voltage bin letter.

Example: DLP660TE GHXXXXX LLLLLLM

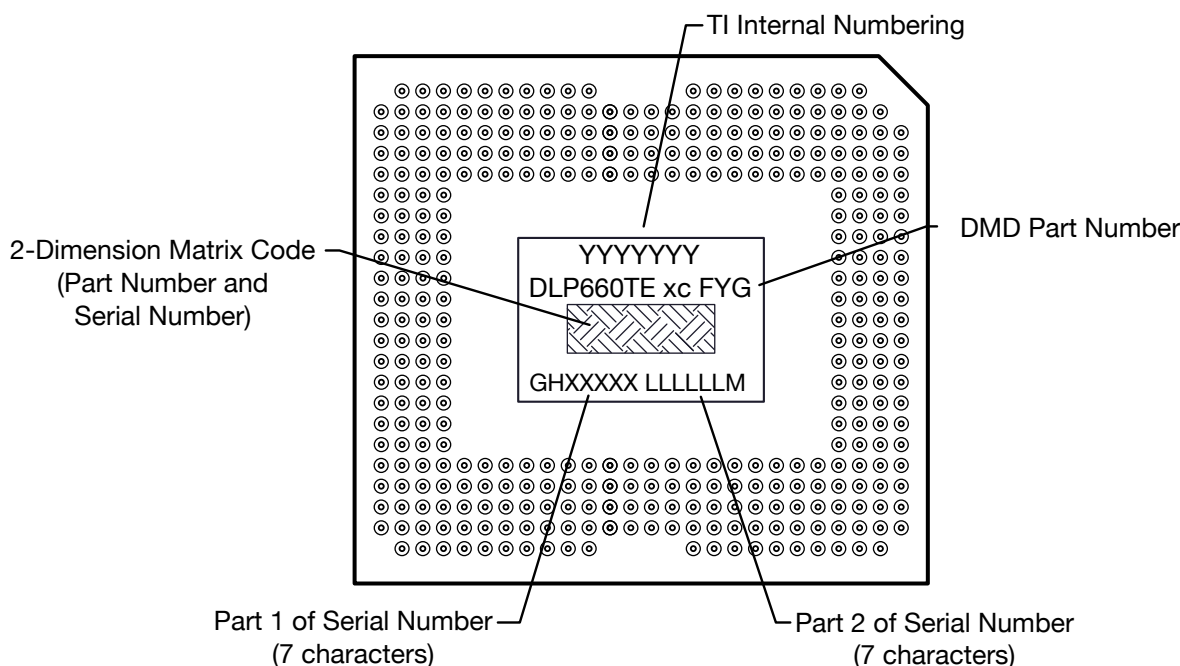


図 10-2. DMD Marking Locations

10.3 Documentation Support

10.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLP660TE:

- [DLPC4420 Display Controller](#)
- [DLPA100 Power and Motor Driver Data Sheet](#)

10.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.5 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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10.6 Trademarks

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DLP® is a registered trademark of Texas Instruments.

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10.7 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.8 用語集

テキサス・インスツルメンツ用語集 この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (February 2023) to Revision D (December 2023)	Page
• Updated the description Absolute Maximum Ratings	11
• Updated Recommended Operating Conditions.....	12
• Updated table and max values in System Mounting Interface Loads	19
• Updated the table format in Micromirror Array Physical Characteristics	19
• Updated Micromirror Array Optical Characteristics	21
• Updated values in Micromirror Array Temperature Calculation	25
• Added section on Micromirror Power Density Calculations	27
• Updated DLP660TE Device Nomenclature	41
• Updated DLP660TE Device Markings	41

Changes from Revision B (July 2022) to Revision C (February 2023)	Page
• コントローラを DLPC4420 に変更し、チップセット・コンポーネントを製品ページにリンク.....	1
• コントローラを DLPC4420 に変更、図を更新.....	1
• Changed controller to DLPC4420.....	23
• Changed controller to DLPC4420.....	24
• Changed controller to DLPC4420, added a table with legacy part numbers and mechanical ICD.....	31
• Changed controller to DLPC4420.....	33
• Changed the controller to DLPC4420.....	33
• Changed controller to DLPC4420.....	34
• Changed controller to DLPC4420.....	39
• Changed controller to DLPC4420.....	42

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP660TEAAFYG	Active	Production	CPGA (FYG) 350	1 JEDEC TRAY (5+1)	Yes	Call TI	N/A for Pkg Type	0 to 70	
DLP660TEAAFYG.B	Active	Production	CPGA (FYG) 350	1 JEDEC TRAY (5+1)	Yes	Call TI	N/A for Pkg Type	0 to 70	

- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

8

7

6

5

4

3

DWG NO 2514366

SH 1

1

NOTES: UNLESS OTHERWISE SPECIFIED:

- 1 DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
- 2 ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
- 3 SUBSTRATE SYMBOLIZATION PAD AND PLATING AT BOTTOM OF DATUMS B AND C HOLES ARE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
- 4 BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
- 5 MAXIMUM ENCAPSULANT PROFILE SHOWN
- 6 ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
- 7 SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.

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REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 2146754, INITIAL RELEASE	11/18/2014	M. AVERY
B	ECO 2147303, ADD GLASS DIMS	12/18/2014	F.ARMSTRONG
C	ECO 2149265, CHG ARRAY TO 1528 ROWS	03/17/2015	F.ARMSTRONG
D	ECO 2156970, CHG NUMERICAL IDENTIFIER TO 317	03/17/2016	F. ARMSTRONG

3 PLACES INDICATED

DATUM PLANE 'F'

SEE VIEW E (SHEET 3)
FOR WINDOW AND ACTIVE
ARRAY DIMENSIONS

DATUM PLANE 'E'

F - SHT. 4

E

C

32.200±0.250

24.371±0.150

(13.500)

2.014±0.150

(ø3.065) B

4.108±0.150

(14.900)

28.916±0.150

35.000±0.250

INCIDENT LIGHT

SUBSTRATE

ENCAPSULANT

0.800 MAX

WINDOW

WINDOW APERTURE

3 PLACES
INDICATED
(SHEET 2)

(0.753)

3.810±0.240

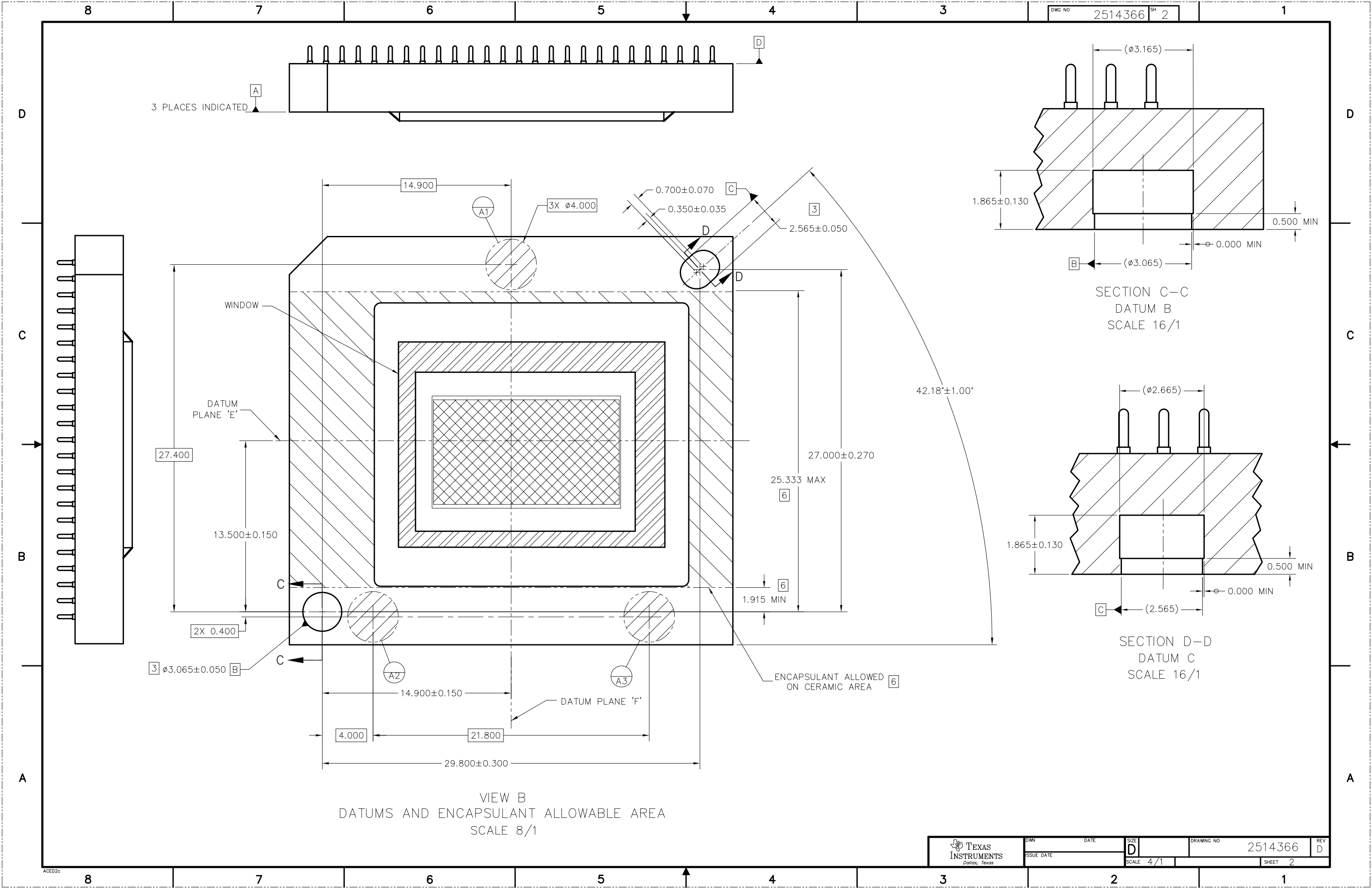
350X 1.400±0.100

(ø0.305)

SECTION A-A
SCALE 20/1// 0.0254 A 1
0.020 G

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES
PARTS LIST				
OWN	M. AVERY	DATE	11/18/2014	
ENGR	F. ARMSTRONG	DATE	11/18/2014	
QA	P. KONRAD	DATE	12/04/2014	
E	CARPENTER	DATE	12/04/2014	
CQE	M. DORAK	DATE	12/04/2014	
S.	SUSI	DATE	12/04/2014	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS TOLERANCES: ANGLES ± 1° 2 PLACE DECIMALS ±0.25 3 PLACE DECIMALS ±0.50		REMOVE ALL BURRS AND SHARP EDGES INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5-1994 DIMENSIONAL LIMITS APPLY BEFORE PROCESSES PARENTHEICAL INFO FOR REF ONLY		
THIRD ANGLE PROJECTION		NONE 0314DA		
NEXT ASSY		USED ON		
APPLICATION				
		DRAWING NO 2514366		
		SHEET 1 OF 4		

ACED1g



3 PLACES INDICATED

14.900

3X $\phi 4.000$

0.700 $\pm$ 0.070

0.350 $\pm$ 0.035

2.565 $\pm$ 0.050

27.000 $\pm$ 0.270

25.333 MAX

1.915 MIN

27.400

13.500 $\pm$ 0.150

2X 0.400

3 $\phi 3.065\pm 0.050$

14.900 $\pm$ 0.150

4.000

21.800

29.800 $\pm$ 0.300

ENCAPSULANT ALLOWED ON CERAMIC AREA

DATUM PLANE 'E'

DATUM PLANE 'F'

WINDOW

A1

A2

A3

B

C

D

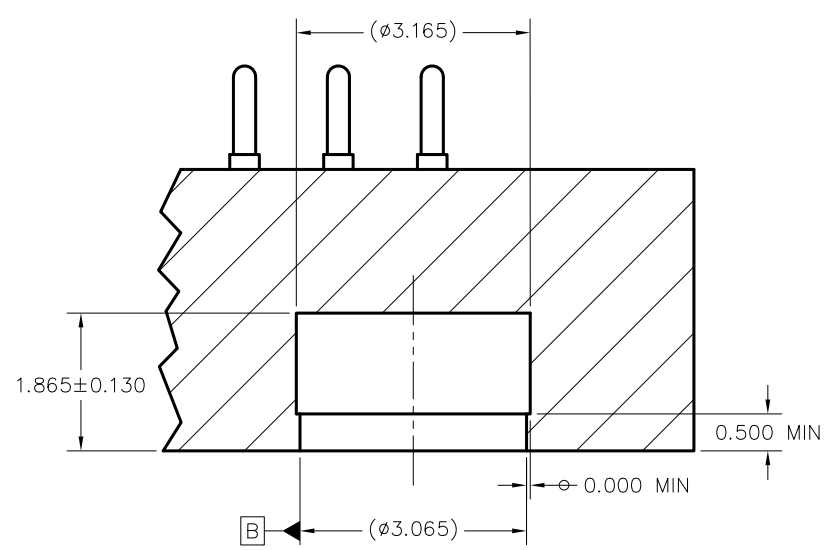
6

3

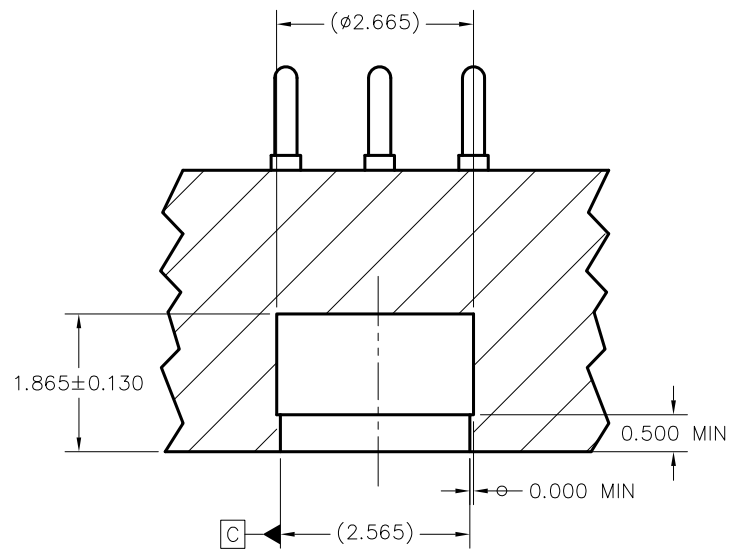
6

6

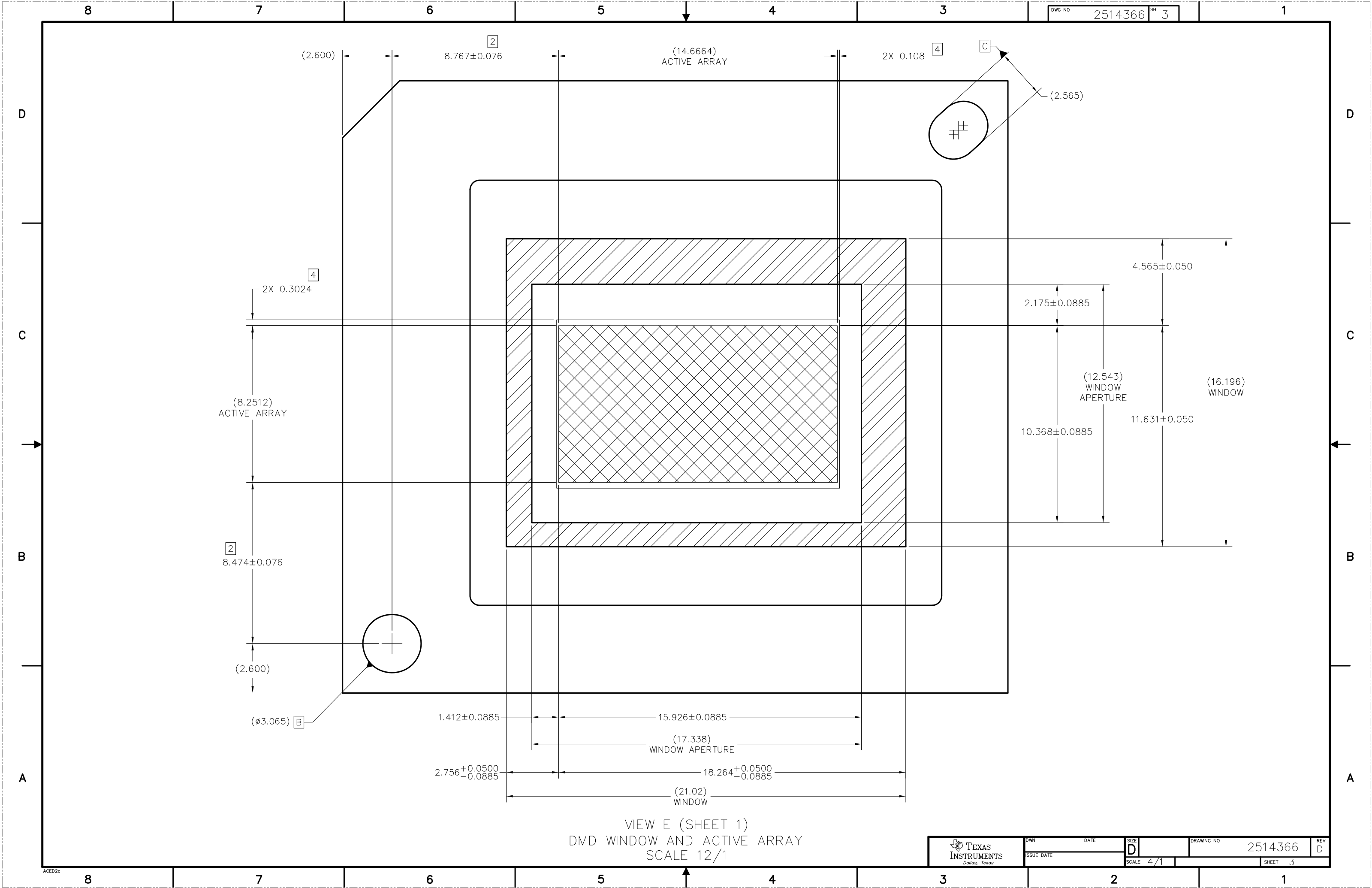
VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1



SECTION C-C
DATUM B
SCALE 16/1



SECTION D-D
DATUM C
SCALE 16/1



8

7

6

5

4

3

DWG NO

2514366

SH 4

1

D

D

C

C

B

B

A

A

3 PLACES INDICATED

DATUM PLANE 'E'

 10.000 ± 0.250 11.100 ± 0.250

SEE DETAIL G

350X $\phi 0.305^{+0.050}_{-0.025}$ PINS

ϕ	$\phi 0.500$	D	E	F
	$\phi 0.250$	D		

[3] SYMBOLIZATION PAD

 (35.000) $25X 1.270 = 31.750$ 15.875

DATUM PLANE 'F'

 (1.625) (PINS A1, A2, A12, A13, A14,
A15, A26, B1, AA1, AA12, AA13,
AA14, AA15, AA26 OMITTED)

A

B

C

D

E

F

G

H

J

K

L

M

N

P

R

T

U

V

W

X

Y

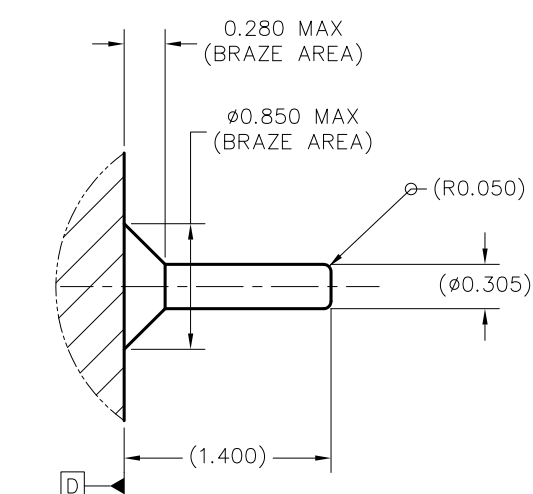
Z

AA

 $22X 1.270 = 27.940$ 13.970 (2.130) (32.200)

317

317

VIEW F-F (SHEET 1)
PINS AND SYMBOLIZATION PAD
SCALE 8/1DETAIL G (350 PLACES)
PIN & BRAZE DIMENSIONS
SCALE 40/1

DWN DATE

ISSUE DATE

SIZE
D

SCALE 4/1

DRAWING NO

2514366

REV
D

SHEET 4

8

7

6

5

4

3

2

1

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